A 2.14-GHz Chireix Outphasing Transmitter

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***Abstract*—A Chireix outphasing system for 2.14 GHz including two saturated class-B pseudomorphic high electron-mobility transistor power amplifiers (PAs) and a Chireix power-combining circuit is reported in this paper. In an outphasing system, an arbitrary input signal is divided into two constant envelope branches. The phase-only modulated branches are then amplified with high-efficiency nonlinear PAs. By controlling the phases of these branches, the original signal waveform can be reconstructed, ideally with high efficiency and perfect linearity.**

In this paper, the design and implementation of an experimental Chireix outphasing system for a wide-band code division multiple access 2.11–2.17-GHz downlink band is presented. The measured system efficiency for 7-dB backed-off quadrature phase-shift keying signal was 42.2% with a channel power of 31.2 dBm.

***Index Terms*—High efficiency, outphasing, RF power amplifiers (PAs), transmitters.**

I. Introduction

COMPLEX AND bandwidth-efficient digital modulation methods used in modern wireless communication systems have considerably increased the linearity requirements of transmitter power amplifiers (PAs). The substantial loss of transmitter efficiency due to the stringent linearity requirements has forced the industry to look for alternative solutions to alleviate the tradeoff between efficiency and linearity. One potential solution is the outphasing system, first introduced by Chireix in 1935 [1]. Outphasing/linear amplification using nonlinear components (LINC) has been the subject of several recent papers, which have mostly concentrated on the signal separation and gain/phase-imbalance issues, e.g., [2]–[5]. Some theoretical treatises have also addressed the power-combining efficiency of the outphasing system [6]–[8], but actual implementation appears scarce.

In the outphasing system, an input signal containing both amplitude and phase modulation is divided into two constant envelope phase-modulated signals. An amplified version of the original signal is achieved by varying the phases of these two signals and summing the amplified branch signals with a passive power combiner. The maximum envelope condition is obtained when the branches are in-phase and the low envelope condition when the branches are almost antiphase. Highly efficient nonlinear PAs can be used to amplify the constant envelope signals without traditional AM–AM or AM–PM distortion taking place in the individual branches. Ideally, this method enables the high efficiency of the nonlinear PAs to be exploited without disrupting the signal integrity.

Unfortunately, if a conventional matched combiner is used at the output, much of the efficiency inherent in the outphasing system is lost. When the signal branches are in-phase, a very small amount of power is wasted in the summing operation, but when the phase difference between the branches grows, the out-of-phase components of the combined signals are directed to the isolated port load and dissipated. In effect, this means that with a conventional combiner, the power-combining efficiency degrades rapidly as the crest factor of the original input signal grows. This problem can be avoided to certain extent, although at the expense of linearity [8], [9], by using a nonisolating power-combiner structure. The resulting linearity deterioration can be overcome with the use of modern predistortion techniques.

The nonisolating combiner presents time-varying impedances to the PAs as the phase difference between the branches alters. If the used PAs exhibit ideal voltage source behavior, the dc-power consumption will scale according to the load impedance, i.e., the efficiency remains high regardless of the phase difference between branches. Realistic PAs do not behave as ideal voltage sources, but the output voltage characteristics of switching PAs and saturated class-B/C PAs are such that some of the potential efficiency benefit can be reaped. The difficulty with the use of saturated class-B/C PAs is their inability to cope with reactive load impedances. To alleviate the problem with reactive loads, the original paper by Chireix [1] introduced a special nonisolating power combiner, known as the Chireix combiner, which uses compensating reactive elements to enhance the power-combining efficiency.

The purpose of this paper is to investigate the practical possibilities of Chireix power combining [10]. This paper begins with a theoretical overview of the outphasing system principle and the operation of the Chireix combiner. The analysis of the Chireix combiner is extended to include the effect of source resistances. The realization of a Chireix power-combining system consisting of pseudomorphic high electron-mobility transistor (pHEMT)-based saturated class-B high-efficiency PAs and a microstrip Chireix combiner is explained. Measurement systems for sinusoidal and quadrature phase-shift keying (QPSK)-modulated signals are described, and measured results for both situations are presented.

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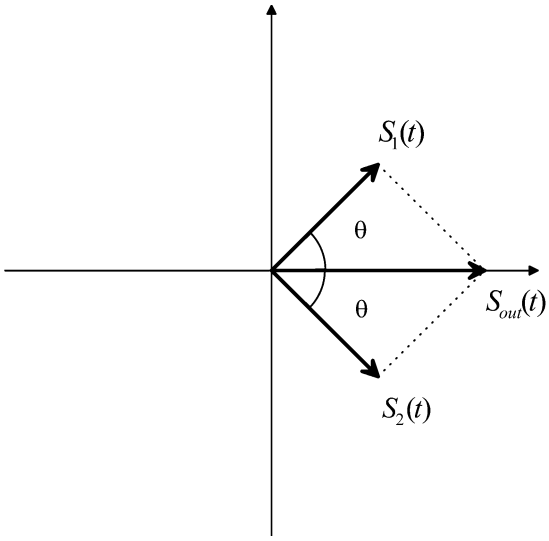

Fig. 1. Vector representation of the outphasing operation.

II. Theory of Operation

A. Outphasing System

In the outphasing system, an arbitrary input signal $S_{\rm in}(t)$ is separated into two constant envelope signals $S_1(t)$ and $S_2(t)$, as illustrated in Fig. 1. If the input signal is defined as

$$S_{\rm in}(t) = A(t)\cos\left[\omega t + \varphi(t)\right] \tag{1}$$

then

$$S_1(t) = V_0\cos\left[\omega t + \varphi(t) + \theta(t)\right] \tag{2}$$
$$S_2(t) = V_0\cos\left[\omega t + \varphi(t) - \theta(t)\right] \tag{3}$$

where

$$\theta(t) = \arccos\left[\frac{A(t)}{V_0}\right] \tag{4}$$

where V_0 denotes the amplitude of the branch signal at peak envelope power (PEP). The output signal $S_{\rm out}(t)$ can be written as the sum of $S_1(t)$ and $S_2(t)$ as follows:

$$S_{\rm out}(t) = 2V_0A(t)\cos\left[\omega t + \varphi(t)\right]. \tag{5}$$

Basically, this ideal presentation means that if the two amplifier branches are perfectly matched, i.e., their gain and phase characteristics are precisely the same, an amplified replica of the original signal can be achieved as the in-phase components add together and the out-of-phase components cancel each other. A simplified block diagram is shown in Fig. 2.

In practice, perfect match between the branches, and thereby complete out-of-phase component cancellation, is very difficult to achieve and the dynamic range of the signal is thus degraded. Even a small imbalance in gain and/or phase will disrupt the cancellation to a degree and introduce intermodulation distortion (IMD) products. Several methods have been proposed in order to minimize the effect of these imbalances [4], [5], [11].

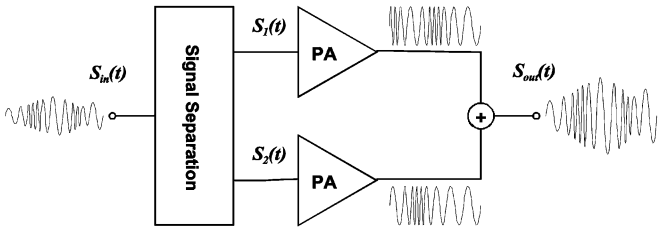

Fig. 2. Simplified diagram of the outphasing operation.

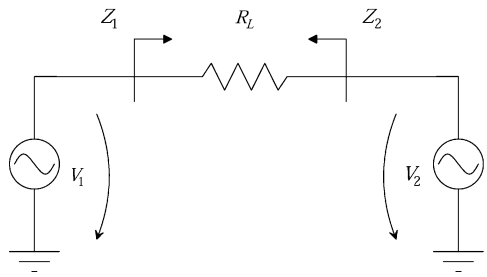

Fig. 3. Schematic of the voltages applied to a common load.

B. Chireix Combiner

In order to exploit the inherent efficiency benefit of the outphasing system, the problem of power combining needs to be addressed. From this point on, the more convenient phasor representation is adopted. The instantaneous output voltages V_1 and V_2 of the two PAs connected differentially to a common load resistance R_L can be written as

$$V_1 = V_0(\cos\theta + j\sin\theta) \tag{6}$$
$$V_2 = V_0(\cos\theta - j\sin\theta). \tag{7}$$

The total output voltage is now written as the difference between the PA outputs $(V_1 - V_2)$, whereas the previously presented analysis takes the sum. This, however, has little impact on the result and is merely a matter of making the formulation somewhat easier. The maximum value $2V_0$ is achieved at $\theta = \pi/2$ and the minimum value zero at $\theta = 0$. The load impedances Z_1 and Z_2 seen by the amplifier branches are thereby

$$Z_1 = R_L\frac{V_1}{V_1 - V_2} = \frac{R_L}{2}(1 - \cot\theta) \tag{8}$$
$$Z_2 = R_L\frac{V_2}{V_2 - V_1} = \frac{R_L}{2}(1 + \cot\theta). \tag{9}$$

A simplified circuit diagram is given in Fig. 3. It can be noticed from (8) and (9) that the effective load impedance seen by each amplifier constitutes of a series connection of half of the original load resistance and a varying reactive part, which is inductive for one PA and capacitive for the other. The basic idea of the Chireix combiner is to add parallel reactive elements in order to cancel the reactive part of the load at a certain predefined phase offset value, thereby allowing maximum efficiency to also be achieved at a phase difference value other than $\pi/2$ when nonideal voltage sources are used.

In order to analyze the use of reactive compensation elements, the load impedance Z_1 can be written in a parallel expression

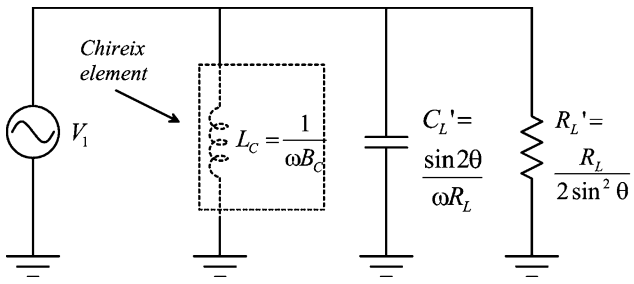

Fig. 4. Parallel expression of Z_1 with compensating inductance.

form. In Fig. 4, the *new* expression for Z_1 is shown to constitute a resistive part R_L' and a capacitive part C_L'. The capacitive part can be compensated at a certain phase offset with a parallel inductive element, denoted with L_C in this figure.

B_C denotes the susceptance of the inductor. The sum of these three terms form the admittance Y_1' seen by the voltage source V_1, which can be used to write the instantaneous input power as

$$P_{\text{IN}} = |V_1|^2|Y_1'| = \frac{2}{R_L}V_0^2\sqrt{\sin^4\theta + \frac{1}{4}(\sin 2\theta - R_L B_C)^2}. \tag{10}$$

Thus, the power-combining efficiency η can be written as the ratio of the power delivered to the load resistor R_L' and the instantaneous power

$$\eta = \frac{|V_1|^2}{R_L'}\Big/P_{\text{IN}} = 1\Big/\sqrt{1+\frac{1}{4}\left(\frac{\sin 2\theta - R_L B_C}{\sin^2\theta}\right)^2}. \tag{11}$$

Efficiency function maxima are achieved when

$$\theta = \frac{1}{2}\arcsin R_L B_C$$

or

$$\theta = \frac{\pi}{2} - \arcsin R_L B_C, \qquad 0 \le \theta \le \frac{\pi}{2} \tag{12}$$

which indicates that there are two maxima, the positions of which can be controlled with the selection of the susceptance B_C. As the efficiency versus phase relation is rather unintuitive, it is preferable to plot the efficiency function with respect to the output power backoff (BO). In the outphasing system, the relation between the power BO level (in decibels) and the phase offset θ is

$$\text{BO} = 20\log(\sin\theta). \tag{13}$$

Similar analysis can be carried out for the V_2 source, in which case, the compensating reactance needs to be capacitive. Fig. 5 shows the Chireix power-combiner efficiency curves as functions of BO with three different $R_L B_C$ values. A reference curve, depicting the situation when conventional Wilkinson combiner is used, is also shown.

In the above analysis, it has been assumed that the voltage sources V_1 and V_2 have zero internal impedance. This is not a very practical assumption as ideal voltage sources are not realizable. To study a more realistic situation, the internal resistances of the voltage sources have to be taken into account. In Fig. 6, the common load situation is shown with the compensating Chireix elements L_C, C_C and source resistances R_S in place.

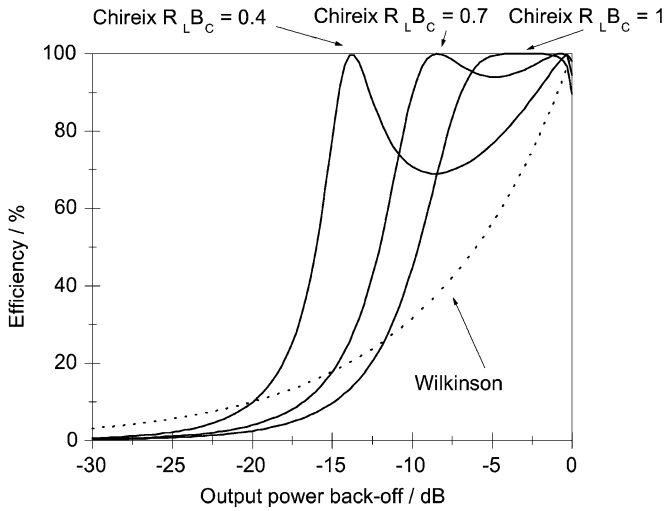

Fig. 5. Computational Chireix combiner efficiency versus power BO. Zero source resistances.

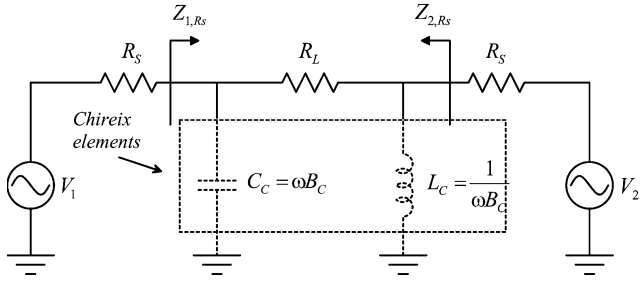

Fig. 6. Common load with source resistances and Chireix elements included.

With these terms included, the effective load impedance Z_{1,R_s} seen by V_1 takes the form

$$Z_{1,R_s} = \frac{R_L}{2}\left(1 + j\frac{R_S B_C \tan\theta - k}{\tan\theta + R_S B_C}\right) \quad k = 1 + \frac{2R_S}{R_L}. \tag{14}$$

Zero output power is attained when the effective load impedance goes to infinity. This takes place when

$$\tan\theta + R_S B_C = 0 \Leftrightarrow \quad \theta = -\arctan R_S B_C \tag{15}$$

which means that zero output power no longer coincides with $\theta = 0$. The nonzero source resistance thereby introduces an offset angle, which can be denoted with θ_0. This correction term must be added to the input signal phase to correctly match the input and output signal minima and maxima. With this term taken into account, the power delivered to the load is

$$P_L = \frac{2V_0^2}{R_L}\frac{1 + R_S^2 B_C^2}{(k + R_S^2 B_C^2)^2}\sin^2(\theta - \theta_0) \tag{16}$$

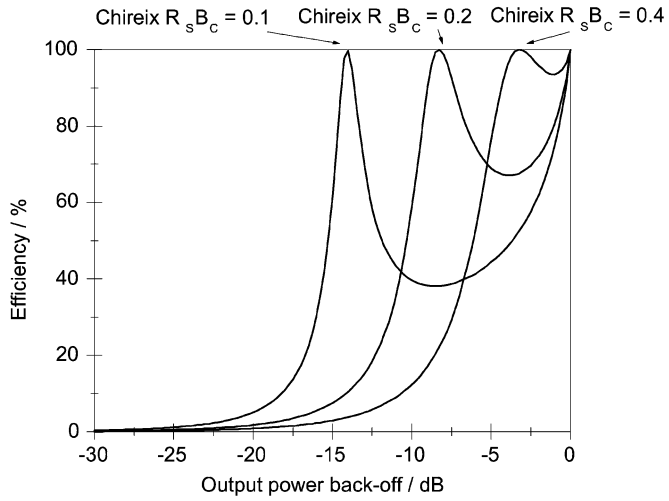

Fig. 7. Computational nonideal Chireix combiner efficiency versus power BO. Source resistances R_s included.

which follows the ideal outphasing power transfer characteristics, except for the offset angle introduction. Maximum output power is achieved with load resistance value

$$R_{L,P\max} = \frac{2R_S}{1+R_S^2B_C^2} \tag{17}$$

at which point the impedance Z_{1,R_s} reduces to

$$Z_{1,R_s,P\max} = \frac{R_S}{1+R_S^2B_C^2}\Big\{1-j\big[2\cot(\theta-\theta_0)+R_SB_C\big]\Big\}. \tag{18}$$

The component values for the effective load network of the nonideal Chireix combiner can now be derived. The load network consists of R_S in series with a parallel connection of $L_C, C_L{}''$, and $R_L{}''$. The expressions for $C_L{}''$ and $R_L{}''$ are

$$C_L{}'' = \frac{1+R_S^2B_C^2}{\omega R_S}\frac{2\cot(\theta-\theta_0)+R_SB_C}{1+\big[2\cot(\theta-\theta_0)+R_SB_C\big]^2} \tag{19}$$

and

$$R_L{}'' = \frac{R_S}{1+R_S^2B_C^2}\Big\{1+\big[2\cot(\theta-\theta_0)+R_SB_C\big]^2\Big\}. \tag{20}$$

The maximum instantaneous efficiency is reached when the load network is purely real, which takes place when

$$\cot(\theta-\theta_0)=0 \text{ or } \cot(\theta-\theta_0)=\frac{1-R_S^2B_C^2}{2R_SB_C}. \tag{21}$$

It can be observed that one of the efficiency maxima is always located at PEP when the optimum load resistance value is used. The location of the other maximum can still be controlled with the selection of B_C. At these two points, the combining efficiency is 100%, and the classical Chireix efficiency behavior with two maxima is still evident. New efficiency curves for nonideal Chireix combiner are plotted in Fig. 7. The shapes of the curves are different from those of the ideal situation presented in Fig. 5, and the valleys between the efficiency maxima are deeper. It is, therefore, clear that the introduction of source resistance R_S degrades the power-combining efficiency, especially at higher BO values, but does not undermine the feasibility of the concept.

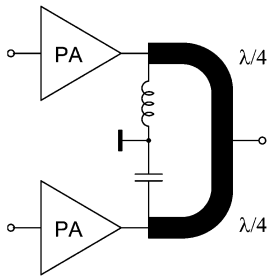

Fig. 8. Chireix combiner test setup.

At this point, it is important to emphasize a couple of issues concerning the efficiency of the Chireix combiner and the outphasing system as a whole. Firstly, the outphasing system efficiency is the sum of the PA efficiency and the combiner efficiency. However, these two can be treated as separate entities only up to a certain degree because of the interaction between the PA and combiner. If a nonisolating combiner structure (see Fig. 3) is placed at the output of outphasing system, the *average* efficiency is not improved compared to a situation with an isolating combiner. The *instantaneous* combining efficiency, however, is fixed to 100%, as no power is dissipated in the reactive part of load impedance, but this "outphased" power is reflected back to the PA. Depending on the amplifier type, this reflected power is either dissipated altogether or "stored" in the amplifier by, in effect, lowering the amplifier's dc power consumption. A true voltage source behavior, i.e., perfect independence of load impedance, can only be expected from switch-mode PAs, and even then just to an extent. Therefore, the average efficiency does not give a truthful picture of outphasing system's performance when traditional PAs are used, and should not be used as the primary measure of efficiency.

The above-presented analysis, however, shows that the addition of reactive compensation elements to the nonisolating combiner structure creates a second maximum for the *instantaneous* power-combining efficiency. With saturated class-B/C PAs, this means that the full potential of the amplifiers can be utilized at this maximum point where the load impedance is purely real. As the result, the system efficiency is also increased in the proximity of the instantaneous efficiency maximum.

III. Realization of Amplifiers and Chireix Combiner

In order to test the basic functionality of the Chireix power combiner with saturated PAs, a test setup was built consisting of two saturated class-B push–pull PAs, a Chireix combiner realized with microstrip lines, and the transmission lines used for connecting the PAs to the combiner. A conceptual picture of the test setup is shown in Fig. 8.

The PAs utilized discrete unpackaged power transistors wire-bonded directly to the microstrip matching circuitry in order to reduce the effect of package parasitics. The transistors were TriQuint TQPHT 0.25-μm pHEMTs, sized

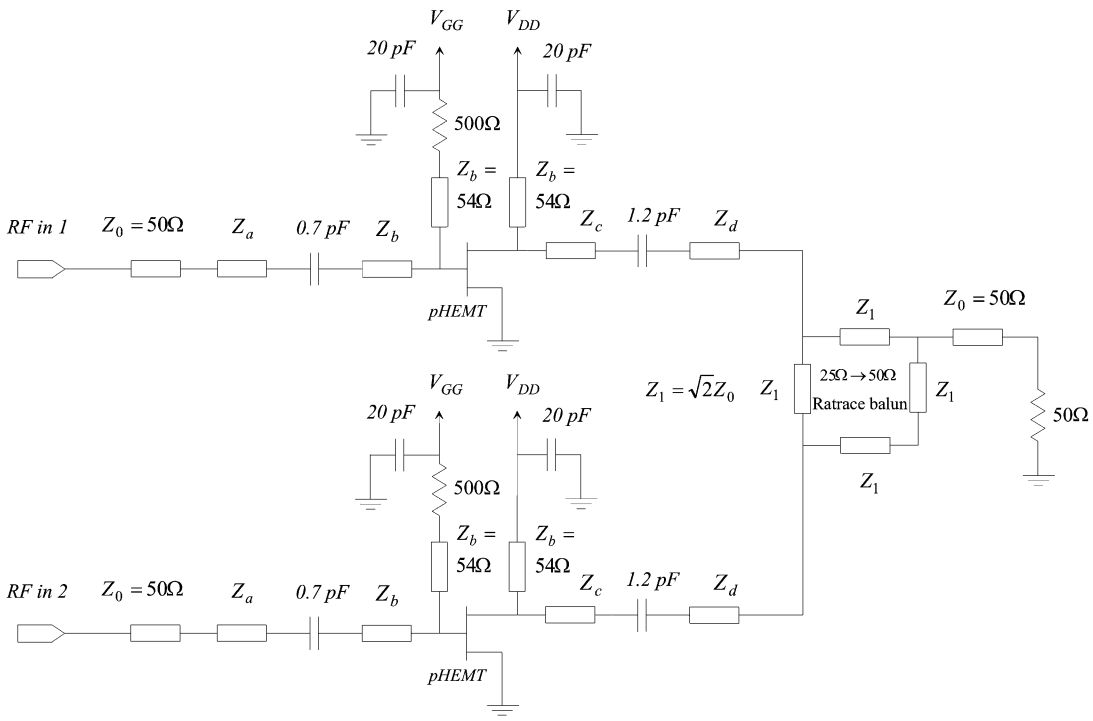

Fig. 9. Schematic of the PA with multistage microstrip matching circuitries at the input and output, denoted for simplicity by Z_a, Z_b, Z_c, and Z_d.

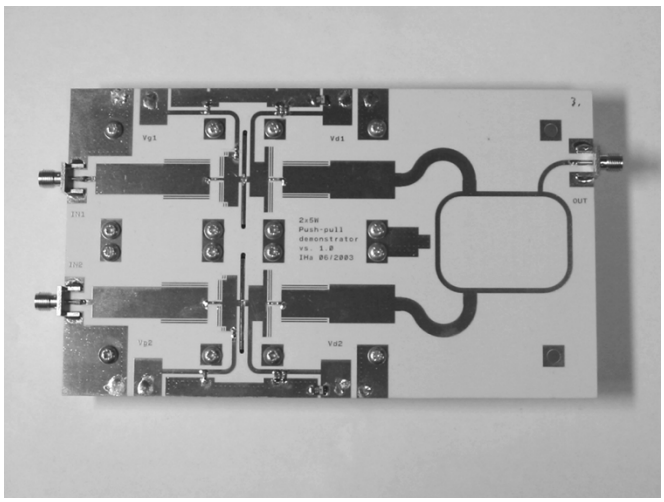

Fig. 10. High-efficiency pHEMT push–pull PA (10 × 17 cm).

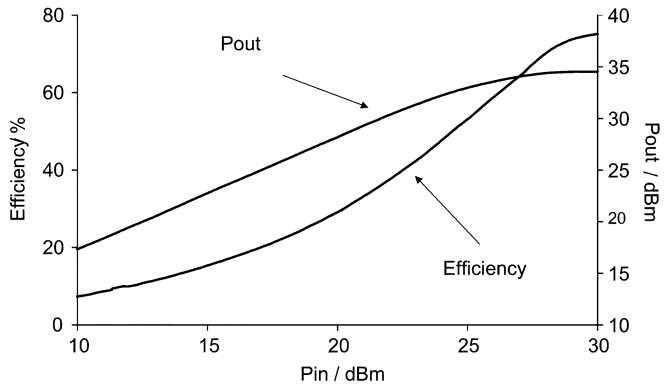

Fig. 11. Measured output power and drain efficiency of the PA.

TABLE I
MEASURED PERFORMANCE OF THE PA BIASED AT $V_{DD} = 5$ V, $V_{GG} = -0.5$ V

	50Ω load condition
Center frequency	2.14 GHz
Output power	34.5 dBm
Input return loss	-9.5 dB
3dB Bandwidth	250 MHz
Gain	5.4 dB
Drain efficiency	75%
PAE	54%

40×250 μm. A Rogers RO4350B high-frequency substrate with $\varepsilon_r = 3.48, \tan\delta = 0.0031$ and substrate thickness of 0.768 mm was used for both the PAs and Chireix combiner. The load–pull simulation method was used for determining the optimum load and source impedances for saturated class-B operation. A rat-race-balun structure was used for connecting the push–pull amplifier branches. A simplified schematic diagram of the designed high-efficiency push–pull PA is given in Fig. 9 and a photograph of the PA is given in Fig. 10.

The PA was designed to exhibit very high efficiency when driven in saturation. In Fig. 11, the measured drain efficiency and output power of the amplifier are given with respect to the input drive level. Other measured performance parameters of the class-B biased PA are recapitulated in Table I.

The realization of the Chireix power combiner was done using microstrip lines instead of lumped components. The compensating reactances were implemented using microstrip lines and a movable short circuit realized by using a shunt capacitor. The shunt capacitor was soldered between the resonating microstrip line and ground, and the placement of

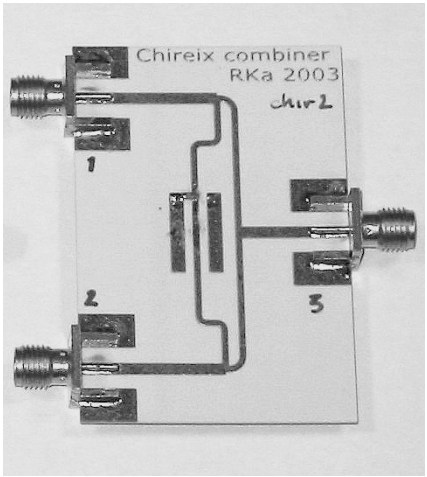

Fig. 12. Microstrip realized Chireix combiner (38 × 56 mm).

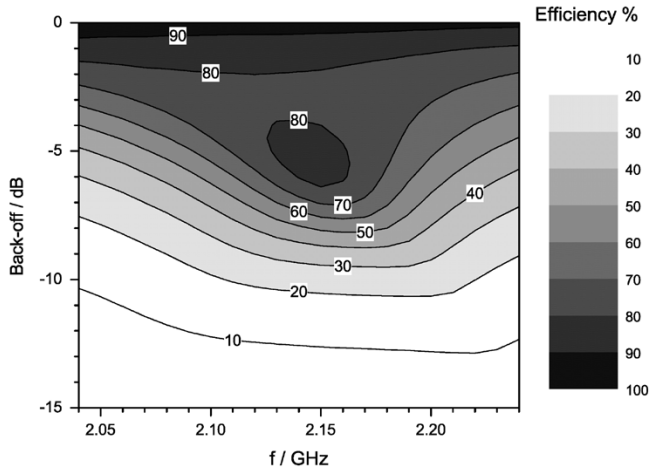

Fig. 13. Efficiency contour of the Chireix combiner.

the capacitor short determined the effective capacitance and inductance values of the compensating elements in the Chireix combiner. A photograph of the microstrip realized Chireix combiner having a shunt-capacitor placement corresponding to a second efficiency maximum at 7-dB BO is shown in Fig. 12.

An important practical detail in the PA–Chireix combiner connection is the length of the transmission lines/cables used between the PA and combiner, as they determine the phase shift between PAs and combiner. Ideally, the compensating Chireix elements in the combiner make the PAs see complex conjugate load impedances, as one combiner branch presents a capacitive parallel element and the other an inductive one. In reality, the connectors, transmission lines, etc. between the PA drains and the combiner compensating elements introduce a phase shift, which causes the load impedances seen by the PAs to change into noncomplex-conjugate values. Therefore, to reinstate the complex-conjugate condition, the lengths of the transmission cables between the PAs and combiner need to be carefully selected to represent a multiple of $\lambda/4$ electrical length between the PA drains and combiner.

Due to the slim $\lambda/4$ microstrip-line realization of the combiner and compensating elements, the bandwidth of the Chireix combiner is relatively narrow. The efficiency degrades rather steeply when the operating frequency varies from the designed center frequency of 2.14 GHz, which naturally restrict the bandwidth of the whole Chireix outphasing system. For demonstrating the functionality of the outphasing system, the bandwidth of the combiner was not critical and was thereby not optimized. The bandwidth of the Chireix combiner can be widened, for example, with a different choice of combiner topology and/or modifying the impedance level of the combiner. A simulated contour plot of the combiner bandwidth is shown in Fig. 13.

The nonisolating structure of the passive Chireix combiner makes the outphasing system inherently nonlinear, as the interaction between the PAs causes nonlinearities at the output. These nonlinearities have not been very extensively studied, and although they have been mentioned in some recent publications [8], [9], no measured data has been presented. A rigorous study of these nonlinearity mechanisms is outside the scope of this paper, but their effect on the linearity performance of the outphasing system is visible in the measurement results presented in Section IV.

IV. Outphasing System Testbench

The outphasing concept with the low-loss Chireix combiner was verified with a testbench, which allows realistic digitally modulated waveforms to be inputted. The achieved system efficiency (the final PA stages and Chireix combiner) was regarded as the top priority, as it is the fundamental potential benefit of the outphasing concept. Necessary tuning procedures for ensuring measurable results were applied, but more rigorous branch mismatch cancellation and phase predistortion routines for fulfilling, e.g., 3GPP specifications were not considered.

Few prior-art references for implemented Chireix outphasing systems are available. Recent advances have been reported in [12].

A. Testbench Construction

The block diagram of the testbench is shown in Fig. 14. The normal direct upconversion transmitter architecture was utilized for the two branches. The digital in-phase/quadrature (I/Q) input sequence, including the signal separation functions is created in the system PC with MATLAB and uploaded into the internal memories of two PCI I/O cards. The looped test vector is fed to the digital-to-analog converters (DACs) at the rate of 61.44 MHz. The four 16-bit interpolating DACs are clocked at 4× oversampling, which facilitates the filtering requirements. The analog outputs are filtered with third-order *LC* filters ($f_{-3\,\mathrm{dB}} = 50$ MHz) and fed into quadrature mixers where the signal is directly upconverted to RF. The RF signal is then preamplified and finally inputted into the class-B PAs and Chireix combiner. Feedback information is gathered from the individual branches, as well as from the composite output signal by a spectrum analyzer and transferred back to the PC via the general purpose interface bus (GPIB) bus.

B. Testbench Calibration

The system has three main error sources that need to be calibrated out before actual measurements: I/Q imbalance,

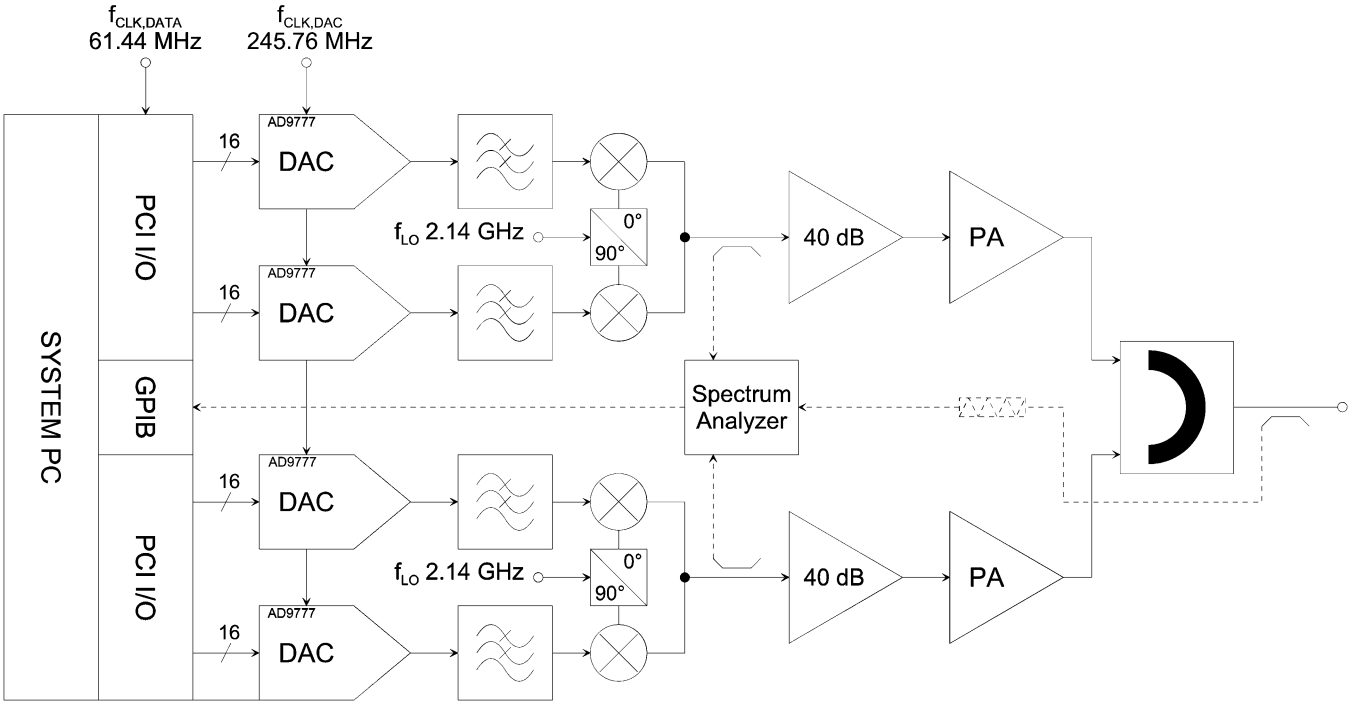

Fig. 14. Outphasing system testbench.

dc-offset, and mixer nonlinearity errors typical to a direct-conversion transmitter, branch gain, and phase-imbalance errors typical to an outphasing transmitter, and phase offset and linearity errors due to the Chireix combiner. The I/Q imbalances and dc offsets in each branch were first compensated by monitoring the upconverted branch signals (image and local oscillator (LO) frequencies). A sinusoidal calibration vector was fed through the system, and phase, gain, and dc compensation factors were calculated and applied to the test vector.

The branch imbalances were cancelled out by finding the output power minimum from the output feedback point and then minimizing it (fine tuning the branch phases). This algorithm was repeated in several frequency points in order to take the nonconstant group delays of the branch paths into account. The branch gain mismatch was manually set to minimum by tuning the PA supply voltages.

Finally, the nonlinearity caused by the Chireix combiner was compensated by applying phase predistortion to the branch signals. The power of a nonmodulated test signal was swept and the resulting output power level was monitored. The deviation from the linear power sweep response was calculated and a static correction lookup table was provided for the branch input signals. It should be noted that these simple calibration schemes will not be sufficient for actual radio system implementation, but adequate in terms of the system efficiency check with modulated signals.

C. Measured Results

To test the combiner–PA interaction before introducing modulated test signals, the two PAs were initially fed with purely sinusoidal signals. The signal phase between the branches was swept while the output power and the PAs' power consumption were monitored. The measured efficiency, i.e., the ratio

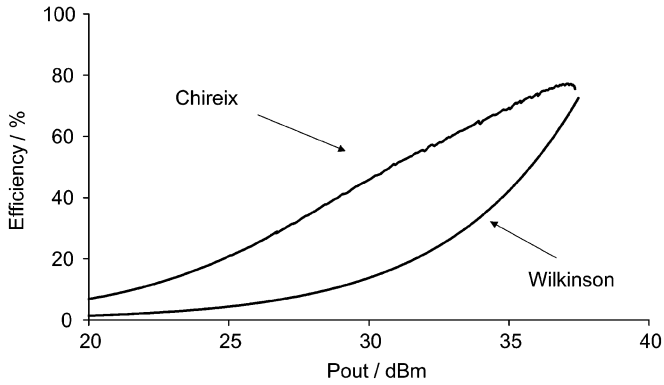

Fig. 15. Efficiency versus output power for sinusoidal signals.

of the output power and the PAs' power consumptions, versus output power for systems employing the Chireix and a regular Wilkinson combiner are shown in Fig. 15. For the Chireix combiner system, the efficiency at −7-dB BO was 45%, showing the efficiency improvement over the Wilkinson combiner system well. The nonlinearity due to the nonisolating structure of the Chireix combiner is visible in Fig. 16, where the output powers of both systems have been plotted with respect to the computational BO level acquired through (13). For the system employing the Chireix combiner, the curve adapts an expansive shape due to the interaction between the PAs.

True test-signal measurements were performed with a QPSK-modulated and raised root cosine (RRC)-filtered test vector comparable to the wide-band code division multiple access (WCDMA) downlink specifications. The probability distribution function (PDF) of a typical signal is plotted in Fig. 17. The signal statistic has a great effect on the achieved efficiency and, therefore, signals with different power BO levels were tested.

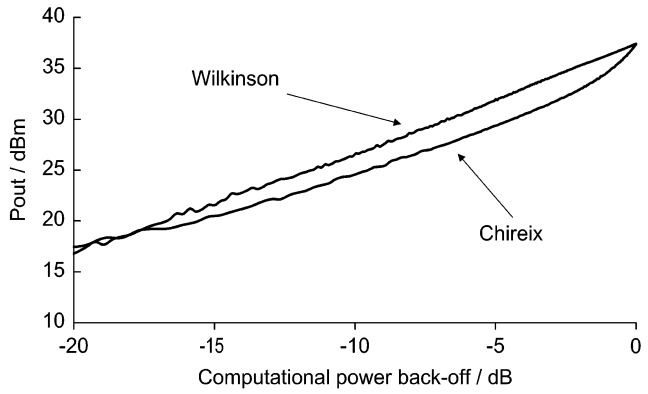

Fig. 16. Output power versus computational BO level.

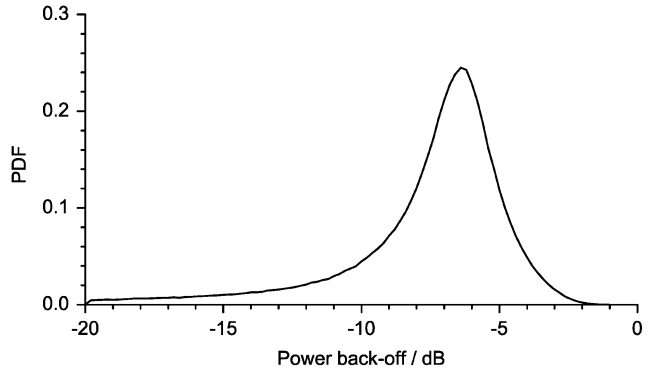

Fig. 17. Modulated input signal PDF signal peak-to-average power ratio (PAPR) is ∼5.5 dB.

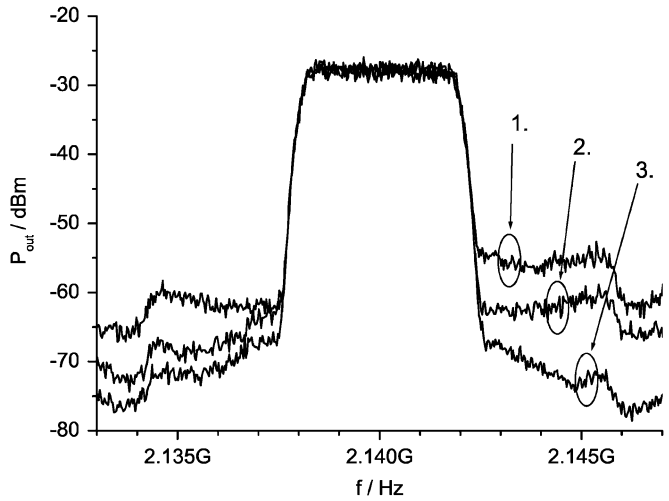

Fig. 18. Measured output spectrum (no PAs, a lossy Wilkinson combiner) with calibration effects shown. 1: Without any calibration ($\mathrm{ACPR_{UP}} = -29$ dBc). 2: With I/Q imbalance and dc offset calibration ($\mathrm{ACPR_{UP}} = -34$ dBc). 3: With I/Q imbalance, dc offset, and branch mismatch calibration ($\mathrm{ACPR_{UP}} = -43$ dBc).

The effect of calibration is shown in Fig. 18. The results are plotted for the testbench without PAs and with a traditional lossy Wilkinson combiner, thus, the Chireix nonlinearity is not visible. The adjacent channel power ratio (ACPR) result of −43 dBc can be regarded as the absolute limit with the current calibration methods.

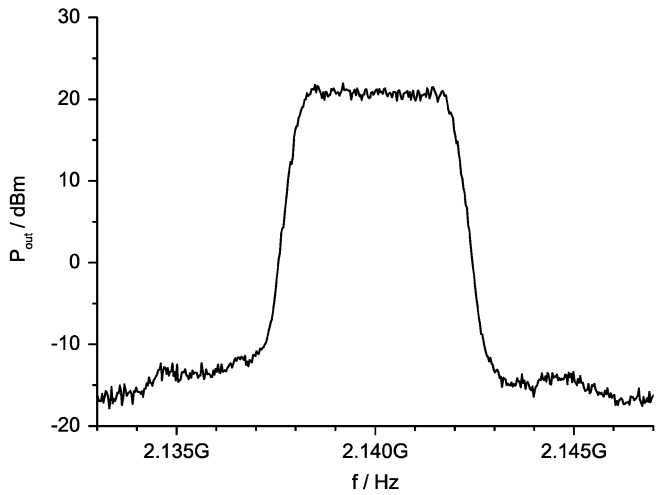

Fig. 19. Measured output spectrum from the testbench (PAs + Chireix combiner), input signal BO −7 dB, output $\mathrm{ACPR_{UP}} = -36$ dBc.

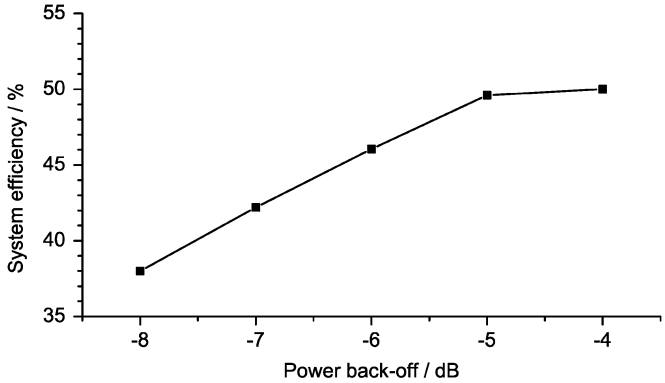

Fig. 20. System efficiency (PA + combiner efficiency) versus input power BO.

The QPSK output spectrum of the testbench including saturated class-B PAs and the Chireix combiner is plotted in Fig. 19. The nonlinearity and branch gain imbalance induced by the Chireix combiner is not fully compensated and, thus, the system linearity is somewhat deteriorated. The measured value for the upper ACPR is approximately −36 dBc.

As before, the efficiency of the system was defined as the ratio of the system output power and the dc input power of the two PAs. A more realistic measure would include the input power levels of the PAs and the power consumption of the previous transmitter parts like the preamplifiers and mixers. If the gain of the last PA stage is sufficiency high, the impact of the power consumption of the previous stages becomes small in comparison. In this case, however, the inclusion of these into the system efficiency figures would, to some extent, hide the crucial effects of the PA/combiner interaction as the gains, and thereby the PAEs, of the saturated PAs used in this experiment are low. Nevertheless, it is clear the high-PAE amplifiers will be absolutely necessary in further development of the outphasing system. The measured system efficiency at different input power BO levels is shown in Fig. 20. Good correspondence with results shown in Fig. 15 for sinusoidal signals can be noticed.

The linearity performance of the testbench is illustrated in Fig. 21, where the measured ACPR and error vector magnitude

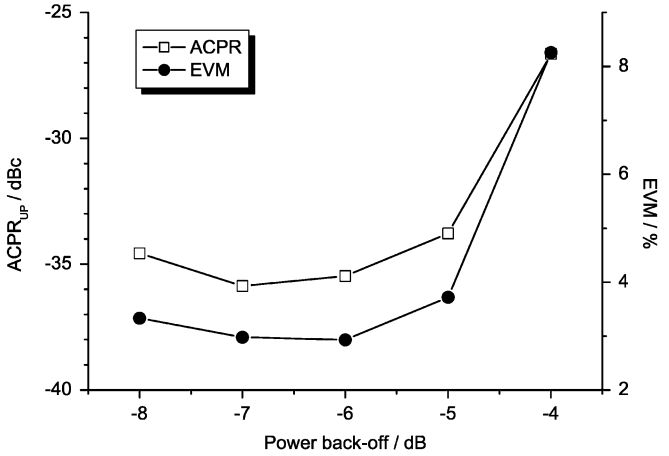

Fig. 21. Output upper ACPR and EVM versus input power BO.

TABLE II
MEASURED RESULTS OF THE OUTPHASING TESTBENCH

	Testbench without PAs, Wilkinson combiner	Testbench with PAs, Chireix combiner
Center frequency	2.14 GHz	2.14 GHz
Power back-off	-7 dB	-7 dB
Channel power	-12.7 dBm	+31.2 dBm
System efficiency	n/a	42.2%
$ACPR_{UP}$	-43.4 dBc	-35.9 dBc
$ACPR_{DOWN}$	-43 dBc	-34.5 dBc
EVM	1.2%	3.0%

(EVM) values are plotted as functions of the input signal BO. The values stay fairly constant at higher BO levels, which is understandable as the calibration accuracy is limiting the linearity performance. At lower BO power levels, the input signal is clipped before the signal separation takes place and the signal purity is degraded.

Measurement results are summarized in Table II. Results are shown for the reference system (no PAs, lossy combining) and for the Chireix system.

V. CONCLUSION

A Chireix outphasing system for WCDMA downlink band has been presented. A considerable efficiency improvement over conventional transmitter systems has been achieved for a high BO QPSK signal. The results are in agreement with the theoretical analysis of the nonideal Chireix combiner structure presented. Additional research needs to be conducted in order to bring the channel power and ACPR values to a required level for 3GPP basestation implementations. It has been verified that the outphasing concept with saturated class-B PAs and a Chireix combiner offers high-efficiency performance when utilized with high-PAPR signals. This makes the concept a potential candidate for high-efficiency transmitters, provided that effective baseband calibration and predistortion algorithms are applied.

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