NONLINEARITY AND NOISE MODELING OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS FOR CONTINUOUS TIME ANALOG FILTERS

A Thesis

by

ARUN RAMACHANDRAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2005

Major Subject: Electrical Engineering

NONLINEARITY AND NOISE MODELING OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS FOR CONTINUOUS TIME ANALOG FILTERS

A Thesis

by

ARUN RAMACHANDRAN

Submitted to Texas A&M University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Approved as to style and content by:

Edgar Sánchez-Sinencio (Chair of Committee)	Jose Silva-Martinez (Member)
Takis Zourntos (Member)	Steven M. Wright (Member)
Gerard L. Cote (Member)	Chanan Singh (Head of Department)

May 2005

Major Subject: Electrical Engineering

ABSTRACT

Nonlinearity and Noise Modeling of Operational Transconductance Amplifiers
for Continuous Time Analog Filters. (May 2005)
Arun Ramachandran, B.En., Birla Institute of Technology and Science-Pilani, India;
M.S., Birla Institute of Technology and Science-Pilani, India
Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

A general framework for performance optimization of continuous-time OTA-C (Operational Transconductance Amplifier-Capacitor) filters is proposed. Efficient procedures for evaluating nonlinear distortion and noise valid for any filter of arbitrary order are developed based on the matrix description of a general OTA-C filter model . Since these procedures use OTA macromodels, they can be used to obtain the results significantly faster than transistor-level simulation. In the case of transient analysis, the speed-up may be as much as three orders of magnitude without almost no loss of accuracy. This makes it possible to carry out direct numerical optimization of OTA-C filters with respect to important characteristics such as noise performance, THD, IM3, DR or SNR. On the other hand, the general OTA-C filter model allows us to apply matrix transforms that manipulate (rescale) filter element values and/or change topology without changing its transfer function. The above features are a basis to build automated optimization procedures for OTA-C filters. In particular, a systematic optimization procedure using equivalence transformations is proposed. The research also proposes suitable software implementations of the optimization process. The first part of the research proposes a general performance optimization procedure and to verify the process two application type examples are mentioned. An application example of the proposed approach to optimal block sequencing and gain distribution of 8^{th} order cascade Butterworth filter (for two variants of OTA topologies) is given. Secondly the modeling tool is used to select the best suitable topology for a 5^{th} order Bessel Low Pass Filter. Theoretical results are verified by comparing to transistor-level simulation with

CADENCE. For the purpose of verification, the filters have also been fabricated in standard 0.5µm CMOS process.

The second part of the research proposes a new linearization technique to improve the linearity of an OTA using an Active Error Feedforward technique. Most present day applications require very high linear circuits combined with low noise and low power consumption. An OTA based biquad filter has also been fabricated in 0.35µm CMOS process. The measurement results for the filter and the stand alone OTA have been discussed. The research focuses on these issues.

ACKNOWLEDGMENTS

I wish to express my sincere gratitude to my advisor, Professor Dr. Edgar Sánchez-Sinencio, for his guidance and support in all my academic endeavors at Texas A&M University. His creativity, insight into circuit design, and ability to keep me focused on the whole picture helped me a lot in my research. His sincere dedication to his teachings and his work inspires me a lot. I wish to thank him for not making me feel out of place at any point of time during my stay at Texas A&M University.

I wish to thank Dr. José Silva-Martinez for his constant guidance and encouragement in my thesis work. I have always relished the number of serious discussions we have had during the course of my research.

A special mention of thanks to Dr. Slawomir Koziel and Dr. Antonio Torralba, two visiting faculties from Poland and Seville, Spain, respectively, with whom I had the chance to interact, exchange ideas and learn a lot during my research. I am always indebted to them for the amount of knowledge I gained from them.

I am deeply indebted to Dr. Ugur Cilingiroglu who has always been a source of my inspiration during my academic stay at Texas A&M University. I have enjoyed and relished every lecture of his.

I wish to express my sincere gratitude to my committee members Dr. Takis Zourntos, Dr. Steven M. Wright, Dr. Gerard L. Cote, for being a part of my thesis committee and for sparing their time and valuable suggestions on my research work

A special note of thanks to Ms. Ella Gallagher, who has always been more than a friend to me. I have never missed home in her presence. She keeps giving me the courage and encouragement and she always installed the notion that we are here to achieve something. I owe a lot to her for this valuable lesson.

I wish to thank all my fellow graduate students here at the Analog and Mixed Signal Center for all their support during my stay here. We have shared a lot of information on the technical and cultural fronts. I thank them for the opportunity given to me learn about the various cultures across the globe.

I wish to acknowledge my roommates and friends here at Texas A&M University, who are not a direct part of the AMSC group, for having stood by me in all that I have done. I shall ever be indebted to them.

I could not have achieved this but for the help, guidance and blessings of my parents, my sister, her husband and my wonderful and most adorable niece Mytreyi. They have always believed that I could do it.

Words of thanks will not suffice to express my sincere gratitude to Bhagawan Sri Sathya Sai Baba, who has been the divine light within me. In my own words “Koti Pranams Swami”.

TABLE OF CONTENTS

Page

CHAPTER Page

CHAPTER Page

LIST OF FIGURES

Page

Page

Page

Page

Page

Page

LIST OF TABLES

Page

Page

CHAPTER I

INTRODUCTION

1.1. Motivation and Background

Real-world signals contain both wanted and unwanted information. Therefore, some kind of electronic signal filtering technique must separate the two before processing and analysis can begin. Every electronic design project produces signals that require electronic signal filtering, processing, or amplification, from simple gain to the most complex digital-signal processing (DSP). As mentioned, in any system that interfaces with the real world, the quantity to be measured and later processed is always contaminated with noise and interferes. A filter is usually used in order to eliminate the unwanted noise and reject the surrounding interferes. Although we are living in a digital age, any system that interfaces with the real world, i.e., the analog world, will find use for continuous-time filters.

Some of the common applications of filters are in communication systems [1]-[3], bio-medical systems [4] etc, where it is essential to eliminate or separate the useful information from the noise signals. A typical digital processing system is shown in Fig. 1.1. The physical quantity to be processed is converted to an electrical signal (current or voltage) via a transducer. This signal is then converted to a digital signal via an analog to digital converter (ADC) for further processing by the digital signal processor (DSP). The physical quantity, which is measured, is mixed with the noise signals present inherent in the environment, noise from the transducer circuits etc. These noise signals have some high frequency components. According to Nyquist theory and to avoid aliasing, the input signal must be band-limited before the analog to digital (A/D) conversion.

This thesis follows the style and format of *IEEE Journal of Solid-State Circuits*.

This is achieved by a low-pass filter (anti-aliasing filter) that limits the bandwidth of the signal to half the sampling rate of the ADC. The processed digital signal coming out of the DSP is converted back to an analog signal via a low-pass reconstruction filter. Both the anti-aliasing filter and the reconstruction filter are analog filters operating in continuous-time.

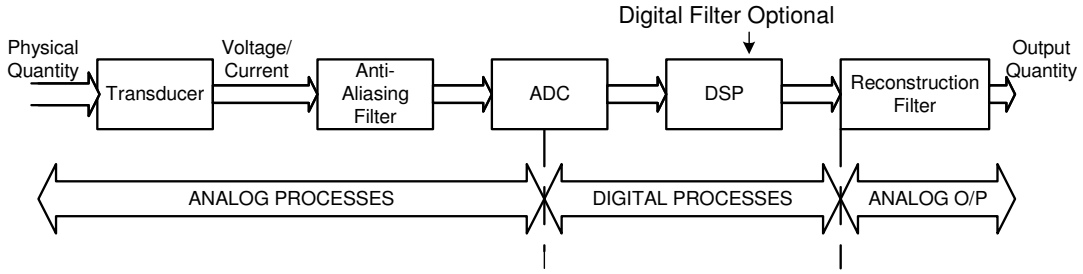


Fig. 1.1. A typical digital processing system

The filter circuit used in any application can be of three different types depending on the type of signals handled. The general types of filters used in most applications are digital filters, continuous-time filters (Analog) and sampled-data filters.

1.1.1 Digital Filters

A digital filter [5] uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general-purpose computer such as a PC, or a specialized DSP chip. The analog input signal must first be sampled and digitized using an ADC. The resulting binary numbers, representing successive sampled values of the input signal, are transferred to the processor, which carries out numerical calculations on them. These calculations typically involve multiplying the input values by constants and adding the products together. If necessary, the results of these calculations, which now represent sampled values of the filtered signal, are output through a DAC (digital to analog converter) to convert the signal back to analog form. In

a digital filter, the signal is always represented by a sequence of numbers, rather than a voltage or current. Fig. 1.2 shows the basic setup of such a system. Fig. 1.2 combines the anti-aliasing filter and ADC together and the reconstruction filter with that of the DAC to focus more on the digital filtering block.

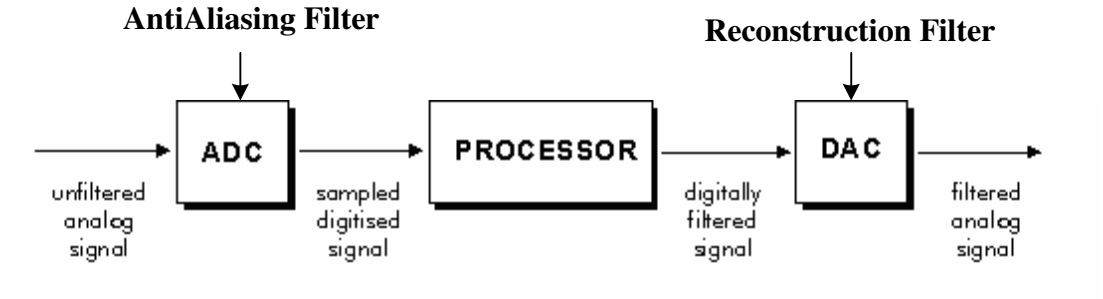


Fig. 1.2. A typical digital filtering example

1.1.2 Sampled-Data Filters

Sampled-data filters do not work with the digital representation of the signal samples, as digital filters do, they rather operate on samples of the signal itself. But both the digital filters and sampled-data filters are characterized in the Z-domain. Thus these filters are discontinuous in time but continuous in processed data values. The best-known example of such an approach is that of switched-capacitor (SC) filters. An SC filter is a continuous-amplitude, sampled-data system. This means that the amplitude of the signals can assume any value within the possible range in a continuous manner. On the other hand, these values are assumed at certain time instants and then they are held for the entire sampling period. Thus, the resulting waveforms are not continuous in time but look like a staircase. Fig. 1.3 describes how an input continuous time signal can be sampled. The sampling operation extracts from the continuous-time waveform the values of the input signal at the instant $n \cdot Ts$ $(n = 1,2,3, \ldots)$, where Ts is the sampling period $(Ts = 1/Fs)$.

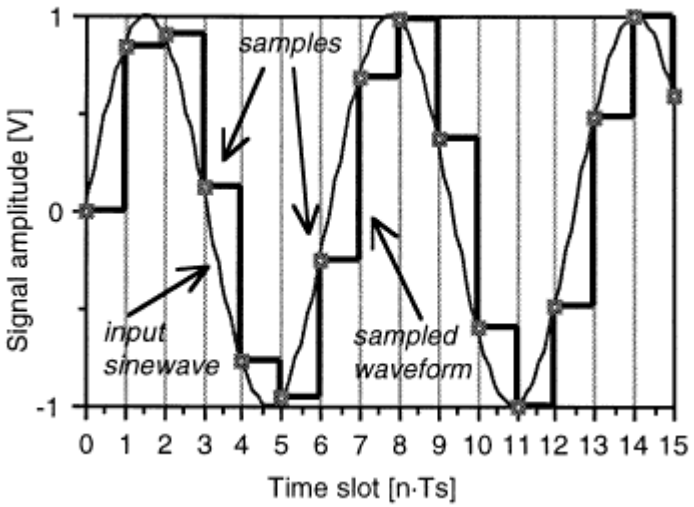


Fig. 1.3. Sampling of a continuous time waveform

The switched capacitor filter can be used in an application [6]-[7] similar to those shown in Fig. 1.1 and 1.2. Fig. 1.4 shows the usage of SC filter in the standard application example. Due to the sampling operation involved, continuous-time (CT) anti-aliasing filter and reconstruction (smoothing) filter are still needed in those kinds of switched-capacitor systems. However these CT filters are not required to have a high accuracy.

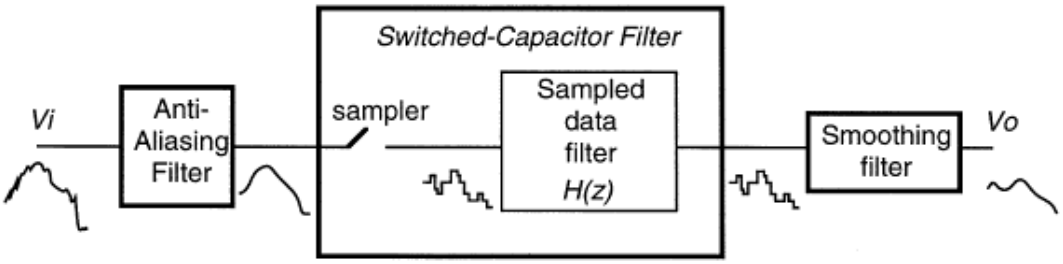


Fig. 1.4. A switched-capacitor (SC) filter application

1.1.3 Continuous Time Filters

An analog filter is any filter, which operates on continuous-time signals. In particular, Linear Time Invariant (LTI) analog filters can be characterized by their (continuous) differential equation. Instead of a difference equation as in digital and SC filters, analog filters are described by a differential equation. Instead of using the z transform to compute the transfer function, CT systems use the Laplace transform. In the real world, analog filters are usually electrical models, or “analogues", of mechanical systems working in continuous time. If the physical system is linear and time-invariant (LTI) (e.g. consisting of elastic springs and masses which are constant over time), an LTI analog filter can be used to model it. Before the widespread use of digital computers, physical systems were simulated on so-called ``analog computers." An analog computer was much like an analog synthesizer providing modular building-blocks (``integrators") that could be patched together to build models of dynamic systems.

Filters can be also categorized according to the relative size (depending on the frequency of operation) of the elements used with respect to the wavelength of the signal into two categories: Distributed [8] and Non-distributed filters. In a non-distributed [9] (lumped) filter, the physical dimensions of the used elements (resistance, inductance, or capacitance) are negligible compared to the wavelength of the fields associated with the signal. Thus they are considered as simple elements concentrated within the boundaries of the corresponding physical element. This is in contrast to the distributed filter, in which the physical elements have dimensions comparable to the wavelength of the fields associated with the signal and hence it is represented by a combination of physical elements.

1.2. Continuous Time Analog Filters

The main focus of this research is the design issues of continuous-time integrated filters. High frequency continuous-time filters have been widely used, in recent years for various applications, especially for medium dynamic range applications, in cases where

high speed and/or low power dissipation are needed. Those applications, as shown in Fig. 1.5, include video signal processing [10], hard-disk drive read channels [11], loop filters for phase-locked loops [12], and radio frequency wireless communication systems [13]. The low frequency applications include those filters used in the bio-medical applications [14] like Hearing-Aid etc. and also the filters used for seismic systems [15].

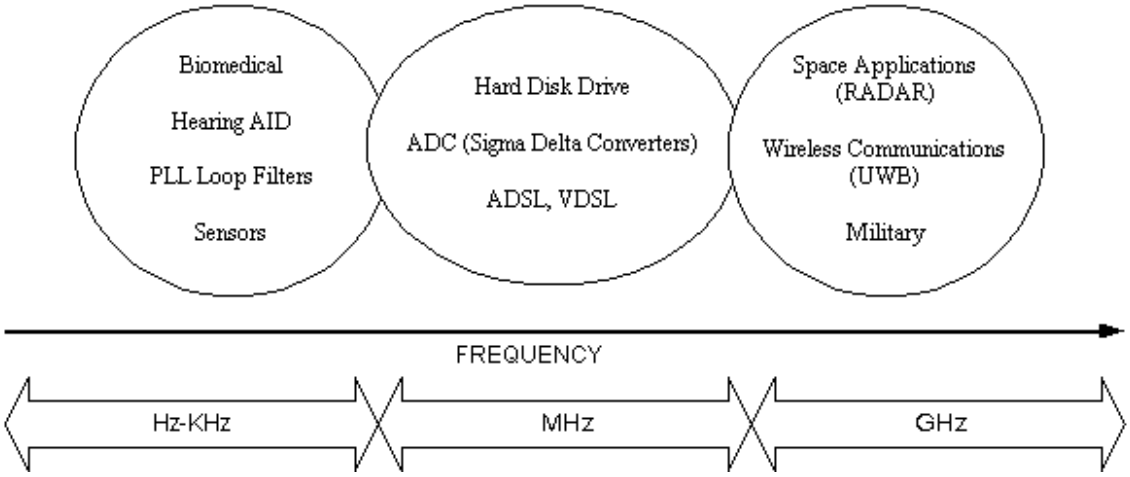


Fig. 1.5. Wide range of filter applications

Using digital filters is not feasible for high frequency applications because they are very power hungry at high frequencies, i.e., $power=f_{clock}V^2_{DD}/2$. Although switched capacitor filters can have good linearity and dynamic range properties, they are not suitable for those kinds of applications either. This is mainly due to their limited ability to process high frequency signals due to the sampling operation. The sampling frequency should be chosen larger than the filter bandwidth to avoid inaccurate filter frequency response. That requires the use of operational amplifiers (OpAmps) with very wide bandwidths, to provide proper settling, demanding large currents; it is required that the unity gain frequency of the used operational amplifier be at least five times larger than the clock frequency used. Another bottleneck is the inability of real switches to operate at high frequency and at low voltages. Thus continuous-time filters became the only

option in these types of applications. Continuous-time filters include two main categories: Passive filters and Active filters. A passive filter has all of its elements passive. Therefore, a passive filter may include among its elements resistors, capacitors, inductors and transformers. If the elements of the filter include amplifiers or negative resistances, this is called active.

1.2.1. Passive Filters

The passive filters are those, which do not employ active blocks like the OpAmps, OTA and other active blocks. They are built using passive elements like resistors, capacitors and inductors. They include three main topologies: RLC filters [16], Surface acoustic filters [17-18], and MEMS filters [19].

1.2.1.1. RLC Filters

Classic RLC filters built with resistors, inductors, and capacitors are still much in use in today's systems. They were first used to meet the needs of the early voice applications from the early 1920s. Although high performance on-chip resistors and capacitors can be fabricated in one or more forms in all IC processes, the performance of on-chip inductors is still unsatisfactory in silicon processes. Furthermore for low frequency applications, the area of the on-chip inductor is prohibitive. This renders RLC filters unsuitable for implementation in an integrated form in silicon technologies.

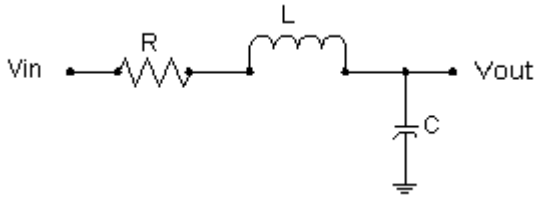


Fig. 1.6. A classical second order low pass RLC filter

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \tag{1.1}$$

Fig. 1.6 shows a classical example of a second order low pass RLC filter. Equation (1.1) gives the basic transfer function of the simple RLC filter. The terms ω_0 is the filter's characteristic frequency and Q is the quality factor of the second order low pass filter and they are equal to $\omega_0^2 = 1/LC$ and $Q = \omega_0 L/R$. The inductors used in the passive circuits are lossy in nature. The quality factor of an inductor is limited by resistive losses in metal traces, and by induced currents in both metal strips and lossy Si substrate.

1.2.1.2. Surface Acoustic Filters

Surface acoustic wave (SAW) filters are applied extensively in today's communication equipment [17]. These high performance components have reached a key position in current communication technology assisting the efforts to increase the spectral efficiency of limited frequency bands for higher bit rates. A SAW filter consists of a piezoelectric substrate with metallic structures, such as inter-digital transducers (IDTs) and reflection or coupling gratings deposited on its plain-polished surface. It is based on propagating and/or standing micro-acoustic waves. Triggered by the piezoelectric effect, a microwave input signal at the transmitting IDT stimulates a micro-acoustic wave that propagates along the surface of the elastic solid [18]. The associated particle displacement of this SAW is bounded in the vicinity of the surface only. Vice versa, a SAW generates an electric charge distribution at the receiving IDT, causing a microwave electrical output signal to occur. SAW technology has evolved to the GHz range in recent years and now routinely covers the frequency range up to 3GHz. This frequency band is used as carrier frequency for many new wireless communication and sensor applications. SAW filters are not suitable for monolithic implementation and are usually implemented off-chip since silicon is not a piezoelectric material. Fig. 1.7 shows a simple transversal SAW filter configuration.

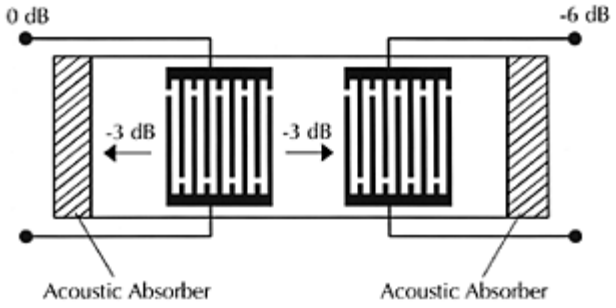


Fig. 1.7. Simple transversal SAW filter (Source: Triquint Semiconductor)

In its simplest form, a transversal SAW filter consists of two transducers with inter-digital arrays of thin metal electrodes deposited on a highly polished piezoelectric substrate such as Quartz or Lithium Niobate (Fig. 1.7). The electrodes that comprise these arrays alternate polarities so that an RF signal voltage of the proper frequency applied across them causes the surface of the crystal to expand and contract. This generates the Raleigh wave, or surface wave, as it is more commonly called. A Typical SAW filter's frequency of operations includes 0-250MHz. SAW filters finds its applications in most of the communication systems. They are also mostly compact devices.

1.2.1.3. MEMS Filters

Micro-Electro-Mechanical Systems (MEMS) [19] are integrated circuit (IC) devices or systems that combine both electrical and mechanical components. MEMS are fabricated using typical IC batch-processing techniques with characteristic sizes ranging from nanometers to millimeters. RF MEMS are micro-electromechanical systems that interact with a radio frequency (RF) signal [20]. The integration/implementation of RF MEMS provides engineers with an additional integration option for better performance, smaller size, and lower cost in their designs. RF MEMS provide microwave and RF engineers with low insertion loss, high Q, small size, very low current consumption, and potentially low cost options to solving their design problems. The low insertion loss is

obtained by replacing the moderate losses associated with semiconductors with lower metallic losses. Cost and size reduction is the result of utilizing semiconductor batch-processing techniques in RF MEMS manufacturing. Like existing semiconductor devices, the RF MEMS circuitry must be protected from the environment. But unlike semiconductors, the environmental protection is required due to either the mechanical movement and/or the mechanical fragility of the parts.

Some of the RF MEMS application devices belong to the general class of static devices, which includes transmission lines and resonators; active devices, such as switches and variable capacitors; and circuits, such as oscillators (fixed frequency and voltage controlled), and tunable filters.

Resonators (Filters) are a basic building block in frequency selective systems. Due to the diverse technologies involved and the low insertion loss associated with MEMS technology, several different resonator types exist. There are three types of resonant structures, demonstrated over widely different frequency ranges, mechanical (300 KHz to 100 MHz), cavity (greater than 20 GHz), and piezoelectric film (1.5 to 7.5 GHz) resonators.

1.2.2. Active Filters

Active filters are ubiquitous in electronic design today, performing signal-frequency manipulation and conditioning for audio, IF (intermediate frequency), and digital-signal processing. The success of active filters is due primarily to integration capability and the extensive body of theoretical knowledge. Although DSPs can outperform active filters in dynamic range, active filters can achieve good performance with significantly lower power demands.

Active filters [21] also use resistors and capacitors, but active devices capable of producing power gain replace the inductors. These devices can range from single transistors to integrated circuit (IC) -controlled sources such as the operational amplifier (OPAMP), and simpler devices, such as the operational transconductance amplifier (OTA) [22], the generalized impedance converter [23] (GIC), and the frequency-

dependent negative resistor [24] (FDNR). The general class of active filters includes the Active-RC filters, MOSFET-C, OTA-C, and Current mode types of filters.

1.2.2.1. Active-RC Filters

Despite the availability of active-filter ICs, most engineers still resort to RC (resistor/capacitor) active implementations consisting of operational amplifiers (OpAmp), resistors, and capacitors. Indeed, the popularity of RC active filters has not diminished since their heyday in the 1970s. They offer the opportunity to integrate complex filters on-chip, and do not have the problems that the relatively bulky, lossy, and expensive inductors bring in particular their stray magnetic fields that can provide unwanted coupling in a circuit or system.

Fig. 1.8 shows the simplest form of active-RC architectures, the Sallen and Key [25] circuit (which uses a voltage amplifier, resistors, and capacitors). It has been around for a long time, yet research into active-RC filters still proceeds after all that time. Sallen and Key types of filters are mainly used for designing high $Q\left(Q=\frac{\sqrt{R_1R_2C_1C_2}}{C_1(R_1+R_2)}\right)$ filters. Larger Qs are attainable by using a positive feedback amplifier. If the positive feedback is controlled—localized to the cut-off frequency of the filter—almost any Q can be realized, limited mainly by the physical constraints of the power supply and component tolerances. Fig. 1.8 shows a unity gain amplifier used in this manner. Capacitor C_2, no longer connected to ground, provides a positive feedback path.

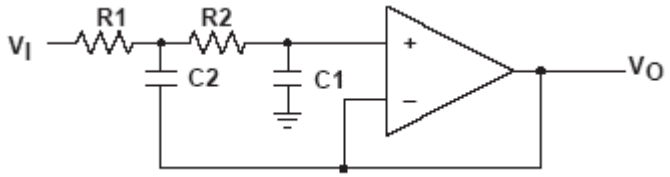


Fig. 1.8. Unity gain Sallen and Key low pass filter

OpAmps (active block represented by the triangular block in Fig. 1.8) are often the most critical elements in any RC-active-filter design and deserve much attention. Voltage-feedback OpAmps are still the mainstay of RC active filters, but current-feedback topologies [26] offer gain that's independent of bandwidth, as well as good current outputs at high frequencies. With more designs concentrating on portable systems, low-voltage CMOS op amps offer rail-to-rail [27]-[28] voltage-handling capability down to power supply voltages of 3V or less.

Active-RC filters have been widely used in various low frequency applications in telecommunication networks, signal processing circuits, communication systems, control, and instrumentation systems. However, they cannot work at higher frequencies due to OpAmp frequency limitations, i.e. higher order poles are created which needs to be compensated, and are not suitable for full integration if large resistors are required. They are also not electronically tunable and usually have complex structures. The most successful approach to overcome these drawbacks is to replace the conventional OpAmp in active-RC filters by an OTA giving rise to OTA-C filters.

1.2.2.2. OTA-C Filters

Programmable high-frequency active filters can be achieved by incorporating the Operational Transconductance Amplifier-Capacitor filters (OTA-C). OTA-C filters also have simple structures, and can operate up to several hundreds of MHz. In recent years OTA-based high frequency integrated circuits, filters and systems have been widely investigated [22]. This is due to their simplicity, electronic tunability, and suitability for high frequency operation due to open loop configuration.

The OTA has been implemented widely in CMOS and bipolar and also in BiCMOS and GaAs technologies. The typical values of transconductances are in the range of tens to hundreds of μS in CMOS and up to mS in bipolar technology. The CMOS OTA, for example, can work typically in the frequency range of 50MHz to several 100MHz. Linearization techniques [29]-[30] make the OTA able to handle input signals of the order of nearly volts with nonlinearities of a fraction of one percent.

Although OTA-C filters have the potential to operate at relatively high frequencies (MHz range), the linear signal range of the used transconductance limits the dynamic range. Also the OTA-C filters become very power hungry at GHz range.

This research focuses on the modeling of these OTA blocks, designing new highly linear OTA blocks for continuous time analog filters. Chapters II and III describe the OTA in detail. Several design issues of the OTA-C filters are also discussed.

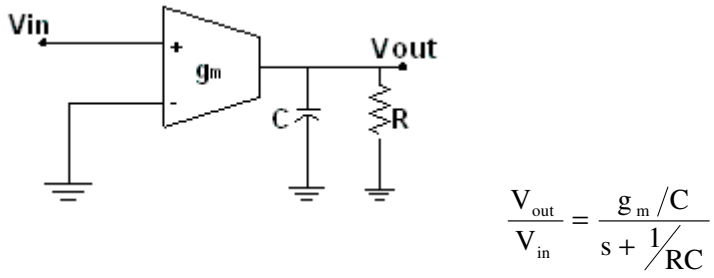


Fig. 1.9. Simple low pass OTA-C filter with a fixed pole and adjustable gain

Fig. 1.9 shows a typical example of a simple first order OTA-C circuit with a fixed pole, depending on the values of *R* and *C*, and an adjustable gain (adjusted using the transconductance g_m of the OTA.

1.2.2.3. MOSFET-C Filters

Today among some of the most proven reliable filter structures are a class called MOSFET-C filters. The MOSFET-C method follows the standard OpAmp based active filter techniques as mentioned in the previous section. The main difference is that the method replaces the resistors used in the conventional active RC integrating and summing circuitry by MOSFET devices based in the triode region (linear/ohmic region), where the MOS device acts as a linear resistor.

1.2.2.4. Current Mode Filters

Most of the techniques mentioned in the previous sections were all voltage mode filters where the input is a voltage variable and the output is either voltage or current. The class of active filters whose inputs are mainly current variables are called collectively as Current Mode filters. For the fully current mode filters [31] the inputs and the outputs are current forms. Fig. 1.10 shows the current mode form of the first order filter whose voltage mode is shown in Fig. 1.9.

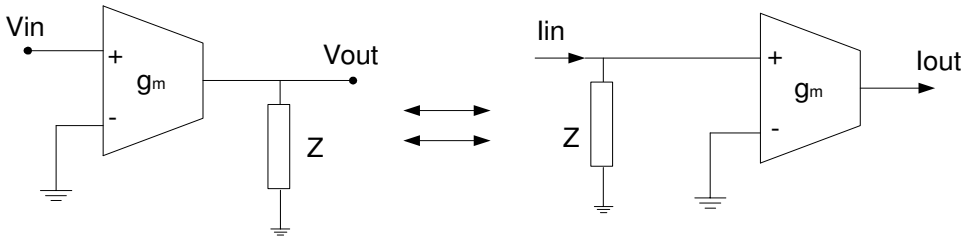


Fig. 1.10. Voltage mode to current mode transformation

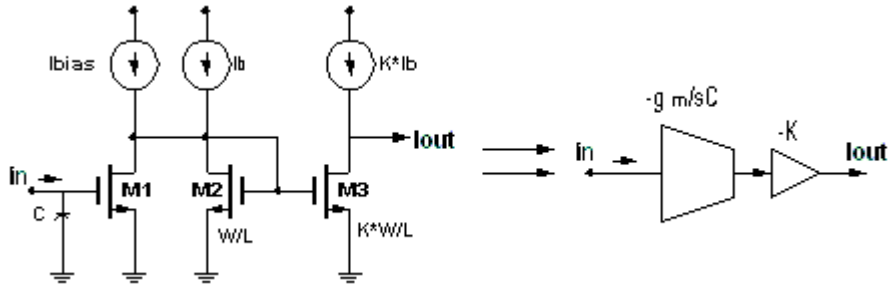


Fig. 1.11. Non-inverting current mode integrator

The most primitive form of the transconductance mode architecture is that of a simple inverting transistor. A simple MOS transistor (a NMOS for e.g.) produces a drain currents I_{ds} corresponding to the voltage input and also its transconductance g_m

parameter. A current amplifier can be implemented using a simple current mirror. Fig 1.11 shows a simple non-inverting integrator in the current mode operation.

The performance comparisons between the voltage mode and current mode almost yield the same response. This might be due to inherent transconductance-mode of both the types. There are however few differences depending on the type of circuit design. In most of the papers proposing very fast current-mode circuits, open-loop current amplifiers are compared to results obtained with closed-loop voltage amplifiers [31]. Many of the amplifiers derived with a current-mode approach base on current mirrors and provide a specific, low gain without feedback around the amplifier. The typical low-gain voltage amplifier uses feedback around a high-gain amplifier. This feedback stabilizes the gain and reduces harmonic distortion, it also improves the terminal impedances of the amplifier.

The voltage-mode filter has ideally a high-impedance output and the current-mode filter has a high-impedance input. Therefore, on a real IC, the voltage mode circuit might need an output buffer, since a resistive load connected to the output node would otherwise change the transfer function, and the current-mode circuit might need an input buffer, since the input nodes must be driven by a high-resistance device. However, the noise of the current buffer is filtered, but not the noise of the voltage buffer, and the performance difference between the two filters is reduced to the performance difference between the circuits used to insert signals into the feedback loop and extract signals from it. The resulting performance difference is certainly small, and it is not a question of signal representation, but of transistor-level design.

Some of the research works indicates that the current-mode circuits are considered to be faster than voltage-mode circuits: although both would be similarly good from an ideal point of view. In general the advantages of current-mode circuits that are often cited in the literature, like a potential for reaching higher frequencies, lower power consumption, and smaller chip area, are in fact real, but the reason is not technical, and has nothing to do with choosing voltages or currents to represent signals.

The reasons for the difference are mainly the design preferences of the proponents of the current-mode approach.

Tables.1.1 and 1.2 show a comparison of the various filter types.

Table 1.1. Comparison of Filter Categories

Parameter	Digital	Sampled-data	Continuous-time
Time samples	Discrete	Discrete	Continuous
Data samples	Discrete	Continuous	Continuous
Need anti-aliasing and reconstruction	Yes	Yes	No
Mathematical Description	Z-transform	Z-transform	S-transform (Laplace)

Table 1.2. Comparison of the Continuous Time Filter Types

Parameter	Active		Passive RLC
	Active-RC	OTA-C	
Frequency of Operation	Upto a few 100of MHz	Upto GHz	Upto a few MHz
Block	OpAmp	OTA	R, L and C
Limitations	Power consumption OpAmp has frequency Limitations Tunability	Linearity Power Noise Tuning	Bulky inductors for higher frequencies
Area	Less	Less	Very large
Silicon Integration	Easy	Easy	Difficult

1.3. Filter Design Procedure

The design of a filter (be it continuous time, digital or sampled-data) involves a series of steps, which will end up in the final filter design to meet the required application. Depending on the application, the specifications of the filter needs to mentioned clearly. There are various ways of approaching the design procedure to achieve the specifications. To select the best approach depends on the choice of the appropriate system transfer function, which will satisfy the specifications. This process involves choosing the right approximation technique. With the filter transfer function chosen the next would be to choose the class of the filter type which needs to be used, be it Active-RC, OTA-C, MOSFET-C etc. Depending on the order of the filter chosen, possible filter implementations needs to be considered like the cascade [32], leap-frog [33], follow the leader feedback, multiple feedback loop [34] etc, if the order is more than 2. If the order is 2, the filter can be a simple biquad. The next step would be to define the passive element values and also the specifications of the active block in the circuit. Designing of the active block to match the specifications follows this step. The final step is to verify the complete filter functionality. Fig. 1.12 gives the data flow diagram for the continuous time filter design. Each of the steps are explained in detail in the following sub-sections.

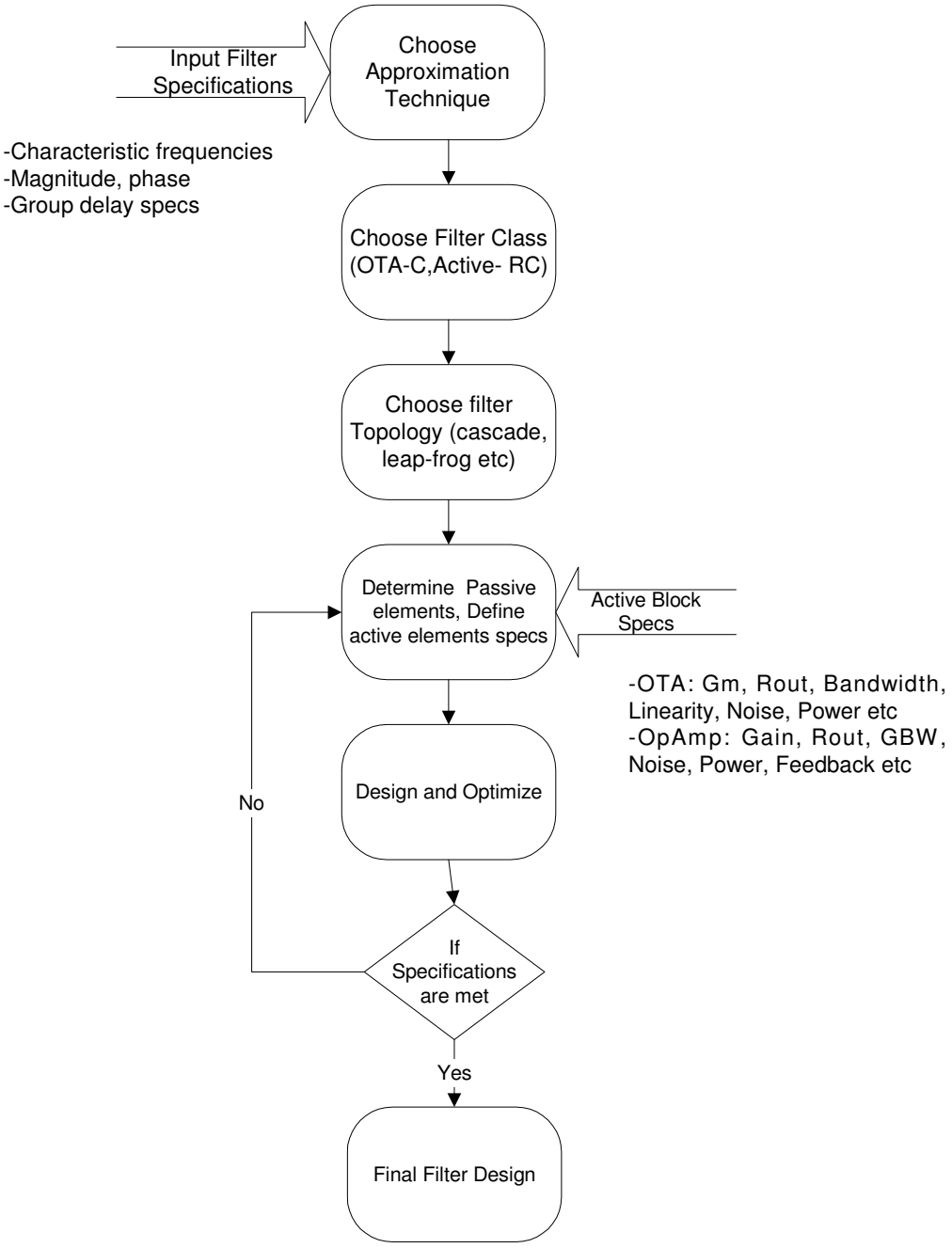


Fig. 1.12. Data flow for continuous time filter design procedure

1.3.1. Filter Specifications

Each application requires some specifications, which may be based on the magnitude, phase, and group delay specifications. Some of the filter specifications are explained in brief.

Magnitude Response: Magnitude Response is defined as the ratio of the output amplitude to the input amplitude versus frequency and is usually plotted on a log/log scale. Some of the magnitude specifications are maximum attenuation in the pass band, minimum attenuation in the stop band, the maximum allowable ripple etc.

Frequency Response: Along with the magnitude specifications are the frequency specifications. The frequency limit till which the filters need to perform is an important measure. A commonly used term is the “Corner” frequency, or the “3dB” frequency. It is defined as the frequency at which the magnitude response drops by 3dB from its desired level, in the case of low pass or high pass filter. The range of frequencies till this level would be termed as the pass band and the range of frequencies above/below, which the signal is totally attenuated, is termed as the stop band. In the case of band-pass filters or band-reject filters, the important specification is the center frequency and the bandwidth within which the signal is contained. Other frequency and magnitude related specification includes “Quality factor Q” of the filter, which is related to peaking factor around the corner frequency.

Phase Response/Group Delay Response: All non-ideal filters introduce a time delay between the filter input and output terminals. This delay can be represented as a phase shift if a sine wave is passed through the filter. The extent of phase shift depends on the filter's transfer function. For most filter shapes, the amount of phase shift changes with the input signal frequency. The normal way of representing this change in phase is through the concept of Group Delay, the derivative of the phase shift through the filter with respect to frequency.

Some of the other specifications of the filter which are not directly involved in choosing the filter transfer function, but are very critical factors are, Noise performance related to signal to noise ratio (SNR), Linearity performance defined using a term called

"Total Harmonic Distortion (THD)" and dynamic range, power consumption etc. These issues are dealt in detail in chapters II and III.

1.3.2. The Approximation Problem

Solution of the approximation problem [35] is a major step in the design procedure of a filter. It is through the solution of this problem that the filter designer determines the filter function, the response that satisfies the above mentioned specifications. In practice, the specifications of a low pass filter are often given in terms of the cutoff frequency the maximum allowable deviation (error) in the passband, the stop band edge frequency, and the minimum attenuation in the stop band. In general, from those specifications, one is able to draw a frequency response magnitude plot. This plot can be approximated by a function that is then implemented using a low pass filter.

The approximation problem has been solved mathematically in various ways. Some of the best-known and most popular lows pass functions in the frequency domain for magnitude responses are: Butterworth, Chebyschev, Elliptic functions, Equal ripple delay and Bessel-Thomson function for phase response. With the aid of any of the computer programs that are available nowadays, such as Fiesta-II [35], one can obtain the appropriate approximating function for any particular specifications. Then, since these basic functions are low pass, a suitable frequency transformation is applied in order to obtain high pass, band pass, or band stop filters according to the requirement.

1.3.3. Filter Class

The next step in the filter design process is the selection of the appropriate filter classes i.e. the type of filter to be used, be it active-RC, OTA-C or MOSFET-C. This has been described in detail in the previous section. The best class of filter is chosen depending on the application. OTA-C is chosen for high frequency applications. Active-RC is chosen if the application has stringent noise and Signal to noise requirements etc. This thesis focuses on the application and usage of OTA-C filters for continuous time

analog applications. The specifications of the active and passive components of the filter are mentioned in the forth-coming sections.

1.3.4. Filter Topology

The filter transfer function obtained from the approximation used, indicates the order of the filter required to meet the filter specifications. In cases, where the order of the filter is 2, a simple biquad (a second order filter) can be used to achieve the response. In most cases, the selectivity that is provided by a second order filter is not sufficient. Higher order filters are needed in order to satisfy the tough selectivity requirements in telecommunication systems, and many other applications. There are two main approaches to realize a high order filter; (1) to cascade second order stages without feedback (Cascade) [32] or through the application of negative feedback [34] (multiple-loop feedback MLF), and (2) simulation of passive LC ladder filters [36]. Selection of the filter topology would depend on some of issues like sensitivity and area available. Some of the filter topologies may not require many active elements; hence the effective silicon area and power can be reduced. Some of the known filter topologies are discussed below.

1.3.4.1. Cascade Topology

In this approach biquadratic second order sections are cascaded and the high order function is realized as the product of biquadratic factors. These sections are simply cascaded by connecting the output of each section to the input of the following one. This method has the advantage of simplicity in designing the filter, provided that the output of each section is very low impedance or the input of each section is very high impedance. Fig. 1.13a shows a simple biquad OTA-C filter and Fig. 1.13b shows a 5^{th} order Bessel OTA-C filter designed by cascading two biquads and a first order filter.

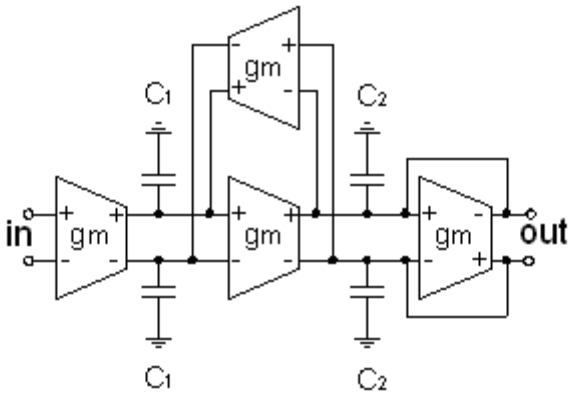


Fig. 1.13a. OTA-C biquad section

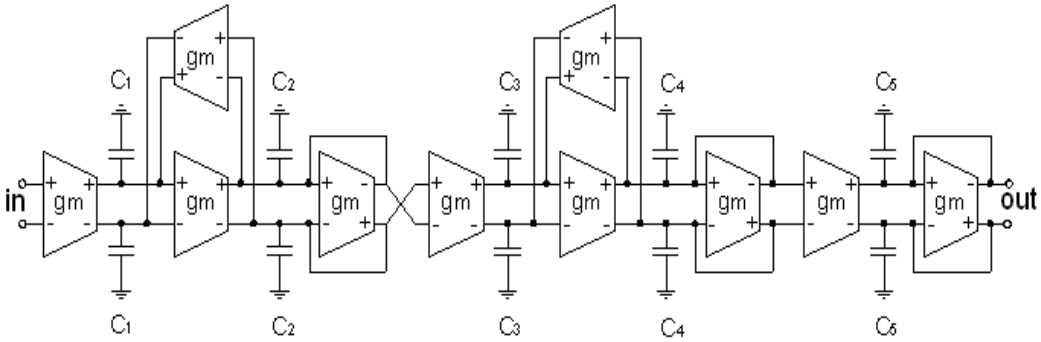


Fig. 1.13b. 5th order Bessel OTA-C filter (cascade 2:2:1)

In the above approach there is no feedback between the biquadratic sections. However the second class of cascading techniques involves feedback across the biquadratic sections. In this approach multiple feedback is applied in a cascade connection of biquadratic sections. This leads to a better sensitivity performance of the overall circuit compared to the corresponding circuit obtained using the Cascade approach. This approach has two general topologies: the leapfrog topology [33], and the summed-feedback topology [34].

1.3.4.2. Leapfrog Topology

The leapfrog (LF) configuration is shown in Fig. 1.14. Each of the boxes named T_i realizes a second order losssless filter transfer function (biquad) except for the terminations at the input and output. The feedback loop always comprises of two sections; thus, inverting and non-inverting sections must alternate to keep the loop gains negative and the loops stable [33]. If the circuit is derived from a resistively terminated lossless ladder filter, as is normally the case, T_1 and T_n are lossy and all the internal sections are lossless. A lossless block implies a function T_i with infinite Q, which may not be stable by itself, but the overall feedback connection guarantees stability. This topology is useful in the functional simulation of LC ladder filter.

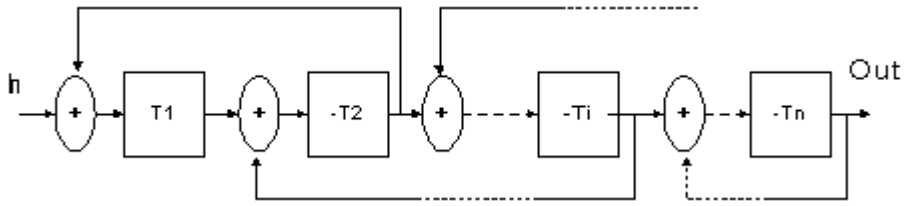


Fig. 1.14. Leapfrog topology

1.3.4.3. Summed-feedback Topology

The summed-feedback topology [34], as shown in Fig. 1.15, is not suitable for realizing any finite transmission zeros. To overcome this problem, one of two techniques can be used: (1) the multiple-or distributed-input technique, in which the input signal is also fed to the input of all cascading sections, or (2) the summation of the input signal and the output signals from all cascaded sections.

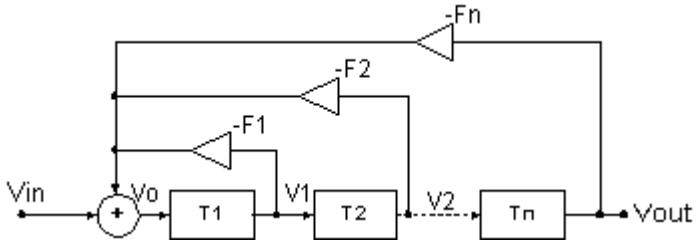


Fig. 1.15. Summed-feedback topology

There are three other design methods based on that topology: the primary-resonator block (PRB) [14] where all the used T_i stages are identical, the follow-the-leader feedback (FLF) [37], and the shifted-companion form (SCF) [38]. Both the FLF and SCF methods are generalizations of the PRB method. The general block diagram of FLF [37] method is shown in Fig. 1.16. In this case, T_i can be first order low pass or high pass functions or alternatively second order biquadratic sections. The summation of the feedback voltages is responsible for the realization of the poles of the function, while the second summation is required for the realization of any finite transmission zeros.

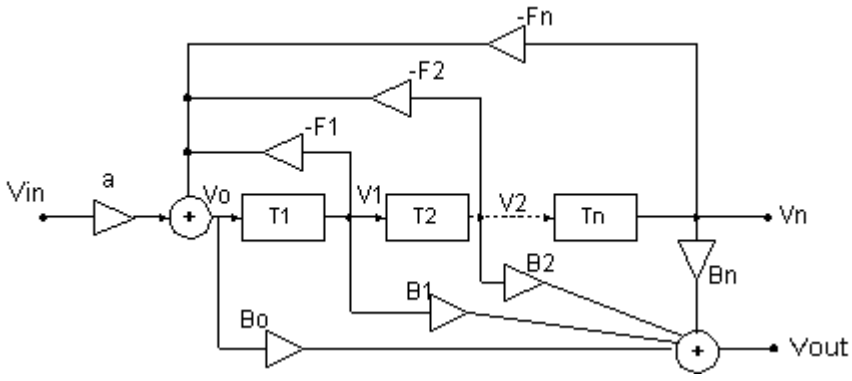


Fig. 1.16. Follow-the-leader feedback (FLF) topology

1.3.4.4. LC Ladder Simulation

Simulating either functionally or using active elements to implement the inductances of the ladder can achieve simulation of passive resistively terminated lossless ladder networks. Functional simulation [36] is implemented by realizing the currents and node voltages in the ladder. The LC ladder simulation method is attractive, because it leads to active filters of lower sensitivities the other two approaches, i.e., Cascade and multiple loop feedbacks.

Table 1.3 gives an overall comparison of the various filter topologies.

Table 1.3. Comparison of Filter Topologies

Type	Approach	Sensitivity	Design
Cascade	Biquadratic sections are cascaded	Bad	Simple and easily tunable
Multiple-loop feedback	Multiple feedback is applied in cascade of biquadratic sections	Good	Complex More critical nodes due to feedback
LC ladder simulation	Simulation of passive lossless ladder networks	Best	Simple

1.4. Active Blocks Design Considerations

The next step, having defined the class and topology is the specification of the active and passive elements used in the filter design. The passive elements are chosen to minimize area consumed in actual silicon and other parasitics introduced. The active block needs further investigation. Some of the commonly mentioned active block

specifications for the case of an Active-RC filter are DC gain, output resistance, gain bandwidth product for the OpAmp used. The specifications for the case of OTA-C filters are the transconductance (g_m)of the OTA, bandwidth, linearity, noise performance of the OTA etc. Apart from the specifications particular for the active block in the filter design, there are some performance criteria specific for the filter applications. Some typical analog filter performance criteria are transfer function accuracy, linearity, noise performance, power consumption, and silicon area.

1.4.1. Noise

Noise (created by both passive and semiconductor devices), unwanted signal, is present at the output of any filter. In most cases, later filter stages remove stop-band noise from earlier stages, but they leave noise in the pass-band unaffected. High-Q filter stages amplify noise near their corner frequencies. In an active filter, for example, the noise spectrum in the stop-band is usually flat and low level, resulting largely from the output amplifier. At the low-frequency end of the pass-band, the noise spectrum is also flat, but with a magnitude two to four times the level of the stop-band noise. Near the corner frequency, noise levels peak at magnitudes that depend on the filter's transfer function. The importance of noise will depend on the system bandwidth and the level of signals passing through the filter [17]. The noise in analog integrated circuits in general can be of two major types. They are:

Flicker Noise: The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since the Silicon crystal reaches an end at this interface, many dangling bonds appear giving rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing flicker noise in the drain current. In addition to trapping, several other mechanisms are believed to generate flicker noise. The flicker noise cannot be predicted easily. Depending on the cleanliness of the oxide-Silicon interface, flicker noise may assume considerably different values. The flicker noise in general is modeled as a voltage source in series with the gate and given by equation (1.2),

$$\overline{V}_n^2 = \frac{K}{C_{ox} WL} \times \frac{1}{f} \tag{1.2}$$

where K is a process dependant constant on the order of 10^{-25} V^2F, C_{ox} is the gate oxide capacitance, W and L are the device dimensions, f is the frequency. The noise spectral density is inversely proportional to the frequency. Hence it is seen to be dominating in the lower frequency zone and almost negligible for high frequency applications.

Thermal Noise: The random motion of electrons in the conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. The noise spectrum is proportional to absolute temperature. The thermal noise spectrum for the case of a resistor is given by equation (1.3).

$$\overline{V}_n^2 = 4kTR \tag{1.3}$$

The thermal noise of a resistor R can be modeled by a series voltage source with one sided spectral density as shown in (1.3). It is expressed in terms of V^2/Hz. As can be observed from the equation, this is a flat spectrum, also called the white spectrum. MOS transistors also exhibit thermal noise. The most significant source is the noise generated in the channel. It is proved that for the long-channel MOS devices operating in saturation, the channel noise can be modeled by a current source between the drain and the source terminals with a spectral density as shown in (1.4).

$$\overline{I}_n^2 = 4kT\gamma g_m, \quad \gamma = \frac{2}{3} \tag{1.4a}$$

$$\overline{V}_n^2 = 4kT\gamma g_m \times r_o^2 \tag{1.4b}$$

It can also be represented by a voltage source at the output by multiplying the current with the output resistance of the MOS device r^2_o. More analysis of the noise in MOS devices and in OTA-C filters are discussed in the following chapters.

1.4.2. Non-Linearity

Nonlinearity is the behavior of a circuit, particularly an amplifier, in which the output signal strength does not vary in direct proportion to the input signal strength. The

large signal analysis of most of the single stage and differential amplifiers exhibit a nonlinear input/output characteristic as shown in Fig. 1.17.

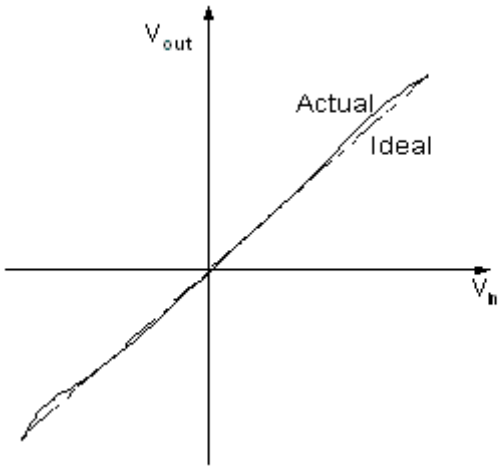


Fig. 1.17. Input/output characteristic of a nonlinear system

Depicted in Fig. 1.17. such a characteristic deviates from the ideal straight line as the input swing increases. The output variations become heavily nonlinear as the input level increases [39]. This variation is due to the nonlinearities introduced in the system. For a simple differential pair, the gain of the input stage relies on the input transconductance, g_m, which is dependent on the input signal variations, V_{gs}. As this term increases more nonlinearity is introduced. The means of reducing the nonlinearities would involve reducing the dependence of the g_m on the input voltage signal at the gate. These techniques are dealt in detail in chapter III. A brief introduction to nonlinearity is given below.

Consider a nonlinear system [40] described by the following equation:

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{1.5}$$

where *y(t)* and *x(t)* is the ouput and input of the system respectively. Assume $x(t) = A\cos(\omega t)$, then from equation (1.1),

$$y(t) = \alpha_0 + \alpha_1 A\cos(\omega t) + \alpha_2 A^2\cos^2(\omega t) + \alpha_3 A^3\cos^3(\omega t) \tag{1.6a}$$

$$y(t) = \left(\alpha_0 + \frac{\alpha_2 A^2}{2}\right) + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \left(\frac{\alpha_2 A^2}{2}\right)\cos(2\omega t) + \left(\frac{\alpha_3 A^3}{4}\right)\cos(3\omega t) \tag{1.6b}$$

In equation (1.6b) the term with the input frequency is called the fundamental and the higher order terms the harmonics. Harmonic distortion factors (HD_i) provide a measure for the dostortion introduced by each harmonic for a given input signal level (using a single tone at a given frequency). HD_i is defined as the ratio of the output signal level of the i^{th} harmonic to that of the fundamental. The *THD* is the geometric mean of the distortion factors. The second harmonic distortion HD_2, the third harmonic distortion HD_3, and the total harmonic distortion *THD* are defined as (assuming $\alpha_1 A >> 3\alpha_3 A^3/4$),

$$HD_2 = \frac{\alpha_2 A}{2\alpha_1} \tag{1.7a}$$

$$HD_3 = \frac{\alpha_3 A^2}{4\alpha_1} \tag{1.7b}$$

$$THD = \sqrt{HD_2^2 + HD_3^2 + HD_4^2 + ...} \tag{1.7c}$$

For fully differential systems, even harmonics will vanish and only odd harmonics remain. In reality, however, mismatches corrupt the symmetry, yielding finite even order harmonics. In a fully differential system with ε% mismatch and from equation (1.7a), HD_2 is given by:

$$HD_2 = \varepsilon\frac{\alpha_2 A}{2\alpha_1} \tag{1.8}$$

More analysis of the non-linearity in analog circuits is discussed in chapters II and III. Some of the other design constraints include Dynamic range, which is related to the non-linearity and also the minimum noise permissible in the system. Dynamic range is defined as the range of desirable signal power levels over which the hardware will

operate successfully. Noise, signal compression, and interfering signals and their power levels limit it.

The other related constraints are Speed, Power dissipation, Voltage swings, Input/Output impedances and Supply voltages. Most of the present day applications demand high speed. They expect the circuit to act very fast to the input signal. Speed has its own tradeoffs with the circuit topology and other frequency dependant parameters. Most of the applications focuses on portability, long life etc. Thus they have a major stress on the power dissipated in the circuitry. Also technology advances fast enough to meet the demands of the electronics industry, hence this reduces the effective voltage supply (power supply). The input/output impedances determine how the circuit interacts with the preceding and subsequent stages. Some applications like the VDSL, ADSL for base band communication systems require the input voltage to swing from rail-to-rails (from V_{dd} to the Gnd). This requires a serious examination of the circuit design, cause the output stages of the circuit should allow such voltage swings. Also the input stage should be linear enough to handle such wide variations. In practice, most of these parameters trade with each other making the design a multi-dimensional optimization problem. Illustrated in the “Analog Design Octagon” in Fig. 1.18, such trade-offs present many challenges in the design of high performance amplifiers, requiring intuition and experience to achieve at an acceptable compromise.

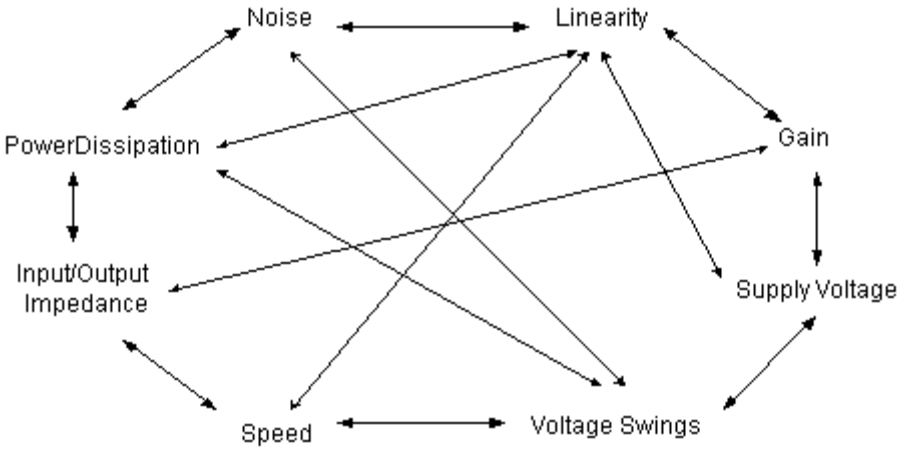


Fig. 1.18. Analog design octagon showing the relation between various parameters

1.5. Organization

The thesis mainly concentrates on the design issues of the OTA-C filter class for continuous time filters. It has several reasons as mentioned in the previous sections and also in the following chapters. The implementation of fully integrated, high-selectivity filters operating at tens to hundreds of MHz provides benefits for wireless transceiver design, including chip area economy and cost reduction. The main disadvantages of on-chip active filter implementations when compared to off-chip passives include increased power dissipation, deterioration in the available dynamic range with increasing Q, and Q and resonant frequency integrity (because of process variations, temperature drifts, and aging). The Operational Transcondutance Amplifier-Capacitor (OTA-C) technique is a popular technique for implementing high-speed continuous time filters [22] and is widely used in many industrial applications. [1]-[3]

Chapter I gives a very brief introduction of the basic filter types, topologies, design considerations etc. Chapter II introduces the general class of the Operational Transconductance Amplifiers (OTA), their modes of operation, their different types (voltage mode, current mode), various applications like the summer, integrator, negative resistor etc. More focus in given on the integrators or the OTA-C filters. The various

types of filters (first order, second order, higher order) are introduced. Two of the main design considerations linearity and noise is given more importance. The basic modeling of these two parameters are considered. A general framework to describe an OTA-C filter using matrix method is introduced and explained. Using this matrix descriptions, the non-linearity and noise of any general order OTA-C filter is determined. The process is explained in detail with elaborate examples (theoretical, simulated and experimental results). Using these techniques the performance optimization of a general order cascade filter is explained. The example of the performance optimization of a 8^{th} order Butterworth low pass filter in cascade realization is mentioned. The chief parameters optimized are the non-linearity (in terms of THD), noise and the dynamic range.

Because OTA-C filters are based on integrators built from an open-loop transconductance amplifier driving a capacitor, they are typically very fast but have limited linear dynamic range. Linearization techniques that reduce distortion levels can be used, but often lead to a compromise between speed, dynamic range, and power consumption. Chapter III deals with the standard linearization techniques available in literature. It introduces to most of the existing techniques to reduce the distortion. Chapter III also proposes two new techniques for improving the linearity of the circuit. The first one being the combination of capacitor division, source degeneration and complimentary input pair OTA for the applications like the VDSL [41] and ADSL [42]. Secondly, a highly linear operational transconductance amplifier (OTA) based on an active-error feed forward linearization scheme is proposed. Feedforward linearization is widely used to reduce nonlinear distortion in amplifiers. The proposed technique gives effective linearization, facilitates the implementation of the OTA circuit which has extremely low power consumption, extended linear range of operation, as well as good transconductance tuning capability. Moreover, the effective excess phase compensation can be easily applied, which makes the circuit suitable for high-frequency applications. The work also aims in verifying the above-mentioned advantages of the OTA on silicon. The theoretical results mentioned about the OTA are also verified with those of silicon measured values to have a proof of concept.

Finally, Chapter IV summarizes the main contributions of this research work. Discussion of different design considerations and trade-offs: high frequency, low voltage, power consumption, linearity, noise is dealt with as we advance through the thesis in the following chapters.

CHAPTER II

NONLINEARITY AND NOISE MODELING OF OTA-C FILTERS*

2.1. Motivation and Background

Continuous-time analog filters [22] and equalizers [43] based on transconductance amplifiers and capacitors (OTA-C filters) are suitable solutions for various voltage-mode and current-mode signal-processing tasks over wide frequency ranges when compared to the Active-RC counterpart. The Active-RC filters have been widely used in various low frequency applications in telecommunication networks, signal processing circuits, communication systems, control, and instrumentation systems for a long time. However, active RC filters cannot easily work at higher frequencies (over 200kHz) due to OpAmp frequency limitations and are not suitable for full integration. They are also not electronically tunable and usually have complex structures. The most successful approach is to use the operational transconductance amplifier (OTA) to replace the conventional integrator in active RC filters. In recent years OTA-based high frequency integrated circuits, filters and systems have been widely investigated [44]-[45].

Many synthesis and design methods for different types and architectures of the OTA-C class of filters have been reported [44]-[51]. In recent years, continuous-time OTA-C filters, often realized as integrated circuits (ICs), have received considerable attention in various applications, such as hard-disc drives [2], video filters, wireless communications [3], computer systems, biomedical circuits [4], and control and instrumentation systems [52]-[53].

The main attractions of these filters is their excellent high-frequency performance, but many of their other properties still need improving, among them are

operation at reduced supply voltages and power consumption, less dependence on parasitic effects, lower noise level, better linearity and wider dynamic range [54]-[63].

In this chapter, the focus is on the noise in OTA-C filters where, it is important to have available efficient tools for nonlinear distortion and noise analysis, in particular, tools that can be embedded into computer-aided filter-design systems. The main requirements for such tools are that they have to be general (so that the same evaluation formulas and software packages can be used to handle all possible filter topologies) and fast enough to be integrated with numerical optimization algorithms.

In the model presented, both requirements are satisfied due to deriving the analysis tools and evaluation formulas from the general OTA-C filter model [49] that uses nonlinear OTA macromodels. The model proposed allows the designer to obtain the results significantly faster than transistor-level simulation. In case of transient analysis, the speed-up may be as much as three orders of magnitude without almost no loss of accuracy. This makes it possible to carry out direct numerical optimization of OTA-C filters with respect of important characteristics including noise performance, nonlinear distortion and dynamic range. On the other hand, the general OTA-C filter model allows us to apply matrix transforms that manipulate (rescale) filter and/or change topology without changing its transfer function. The above features are a basis to build automated optimization procedures for OTA-C filters. In particular, a systematic optimization procedure using equivalence transformations is presented.

2.1.1. Transconductor Amplifier

An ideal operational transconductance amplifier is a voltage-controlled current source, with infinite input and output impedances and constant transconductance. The OTA has two attractive features: changing the external dc bias current or voltage can control its tranconductance, and it can work at high frequencies. Fig. 2.1a shows a general model of the transconductor cell and Fig. 2.1b shows the simple NMOS transistor as the simplest transconductor cell.

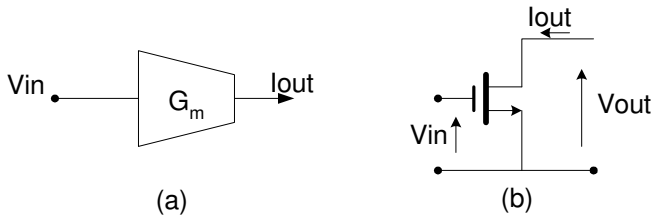


Fig. 2.1. (a) Transconductor cell (b) Simple MOS transconductor cell

A brief overview of the physics involved in the operation of a transconductor cell is given below. The current-voltage relation given by equation (2.1) governs a MOS transistor in the saturation region, neglecting λ effects. The model's output current *Iout* = i_D, is the total

$$i_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(v_{GS} - V_t)^2 \tag{2.1}$$

drain current , which includes the DC and the ac small signal current. The input voltage *Vin* = v_{GS} , also includes the DC voltage (V_{GS}) and the ac component (v_{gs}). The remaining terms are μ: the carrier mobility, C_{ox}: the oxide capacitance per unit area of the channel, V_t: the threshold voltage, *W* and *L* are the width and length of the channel. The derivative of (2.1), leads to a first order relation between current and voltage, as shown in (2.2a) , (2.2b) and (2.3).

$$g_m = \frac{i_d}{v_{gs}} = \frac{\partial i_D}{\partial v_{GS}}\Big|_{I_D, V_{GS}} = \mu C_{ox}\frac{W}{L}(v_{GS} - V_t) \tag{2.2a}$$

$$g_m = f(I_D) \tag{2.2b}$$

$$i_d = g_m v_{gs} \tag{2.3a}$$

The term g_m is called the transconductance and hence the name transconductor amplifier. Alternate forms of (2.2) establish the relation between the device dimensions, the bias current and the transconductance value. The transconductance can be adjusted by the width to length ratio, *W/L*, of the gate and is proportional to the square root of the bias current I_D. The unit of transconductance is Siemens (S).

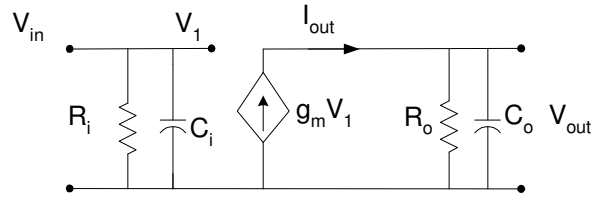


Fig. 2.2. Macromodel of transconductor cell in Fig. 2.1b

Macromodels are simplified circuit descriptions whose behavior resembles very closely that of a transistor level circuit, but use less and simpler components [44]. The macro model of the transconductor cell shown in Fig. 2.1b is shown in Fig. 2.2. The input impedance represented by R_i is ideally infinity as the input is open at DC. The output resistance R_o can be defined as the ratio of the early voltage, V_A, and the bias current, I_D.

$$R_o = \frac{1}{g_o} = \frac{V_A}{I_D} \tag{2.3b}$$

The input capacitance in saturation region of operation, C_i, is approximately given as ¾th of WLC_{ox} product, where C_{ox} is the gate oxide capacitance per unit area. The output capacitance C_o depends on the device size, connections, and layout and is usually is of the order of 0.01pF or less.

There are various single input implementations of the OTA based on the model discussed in this section. Fig. 2.3 shows some of the single input implementations. A detailed discussion of these structures is not the current focus of the research. In all the cases mentioned in Fig. 2.3, the transconductor is a function of the bias current I_{bias} *(i.e.* $g_m = f(I_{bias})$ and the exact relation is a function of the transistor region of operation (refer to Tables 2.1 and 2.2).

Table 2.1. Transconductance for Various Modes of Operation

Parameter/Region Of Operation	G_m
Saturation (MOS)	$\sqrt{2\mu_n C_{ox}(W/L)I_D}$
Ohmic (MOS)	$\mu_n C_{ox}(W/L)V_{DS}$
Sub-threshold (MOS)	$\frac{q}{nkT}I_D$
Bipolar	$\frac{I_C}{V_T}$

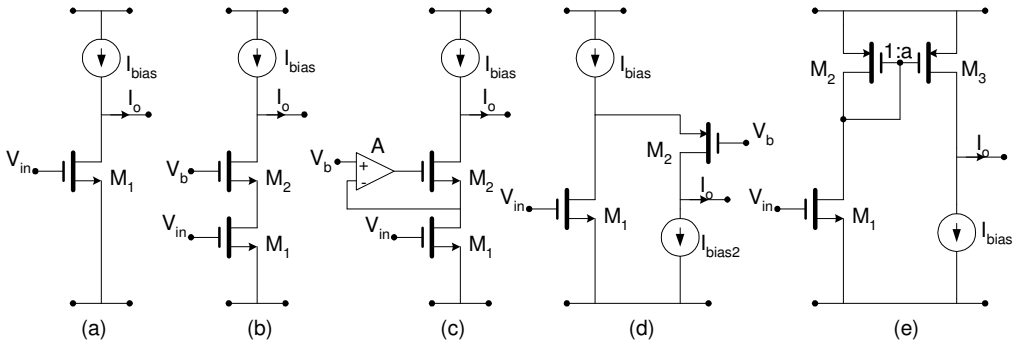


Fig. 2.3. Single input transconductor implementations: (a) Simple negative, (b) Cascode, (c) Enhanced, (d) Folded-cascode, (e) Simple positive transconductors

The single input transconductor has some applications. However their linearity performance is not good. Most of the OTA-C filters utilize the differential transconductor, or differential OTA without two inputs, a negative and a positive one. The differential OTA can have a single ended output (one output) or a differential output (a positive and negative one). Also the implementation can be fully differential or pseudo-differential. Their differences and implementations are discussed in the coming sections.

Table 2.2. Properties of Simple (Single Input/Single Output) Transconductors

Structure /Figure	G_m	R_{out}	Min V_{DD*}
Simple 2.3(a)	g_{m1}	$1/g_{ds1}$	$\sqrt{\frac{2I_B}{k}} + V_{sat,I}bias$
Cascode 2.3(b)	g_{m1}	$\frac{g_{m2}}{g_{ds1} * g_{ds2}}$	$(1+m)\sqrt{\frac{2I_B}{k}} + V_{sat,I}bias$
Enhanced 2.3(c)	g_{m1}	$\frac{A\, g_{m2}}{g_{ds1} * g_{ds2}}$	$(1+m)\sqrt{\frac{2I_B}{k}} + V_{sat,I}bias$
Folded-Cascode 2.3(d)	g_{m1}	$\frac{g_{m2}}{g_{ds1} * g_{ds2}}$	$\sqrt{\frac{2I_B}{k}} + V_{TP} + V_{sat,I}bias$

* The bottom devices of the cascode pairs have an aspect ratio of (W/L)1/(W/L)2=m2. *k* is a technological parameter determined by the mobility, and the gate oxide; V_{sat},I_{bias} is the saturation voltage for the I_{bias} current source.

2.1.2. Differential Input Operational Transconductor Amplifiers

There are two possible realizations of transconductance amplifiers, the bipolar implementation and the MOS implementation. This research thesis focuses on the MOS implementations of the transconductance amplifiers. The simplest MOS implementation was described in the previous section. An extended form of the transconductor cell is the Operational Transconductance Amplifiers also known as OTA. An OTA is a voltage controlled current source, more specifically the term “operational" comes from the fact that it takes the difference of two voltages as the input for the current conversion.

The ideal OTA is a differential-input voltage-controlled current source (DVCCS). Its symbol is shown in Fig. 2.4a, and its operation is defined by the following equation (2.4). Both voltages V_1 and V_2 are with reference to ground. The equivalent circuit of the ideal OTA is shown in Fig. 2.4b.

$$I_{out} = g_m(V_1 - V_2) \tag{2.4}$$

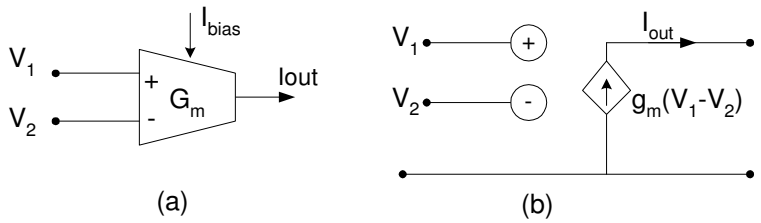


Fig. 2.4. (a) OTA symbol, (b) Ideal equivalent circuit

From the symbolic representation, the input and the output of the OTA are voltage and current respectively. The OTA is often used in open- loop applications and the transconductance parameter g_m is the gain of the OTA. The ideal OTA macromodel has infinite input and output impedances and the transconductance g_m is frequency independent. However in most circuit implementations a real macromodel including the non-idealities should be take into consideration. It is shown in Fig. 2.4, that the transconductance of the differential OTA is a function of the bias current (I_{bias}). If the input differential transistors are in the saturation region the transconductance g_m is proportional to the root of the bias current and if the transistors are in the weak inversion region the transconductance is directly proportional to the bias current. (refer Table 2.1)

As mentioned earlier, a differential input OTA can be have a single ended output or a differential output. They can also fully differential or pseudo-differential. Fig. 2.5 shows a simple single ended differential OTA (a) and a conventional fully differential OTA (b). The symbols for the same are also shown. Transistors M_1 and M_2 forms the input differential pair and M_3/ M_4 in Fig. 2.5a forms the current mirror. In both the forms of the differential OTA there exists a tail current source (I_{tail}). Most of the present day continuous time filter applications require the differential output for differential signal processing. Hence the fully differential version (Fig. 2.5b) is of more importance.

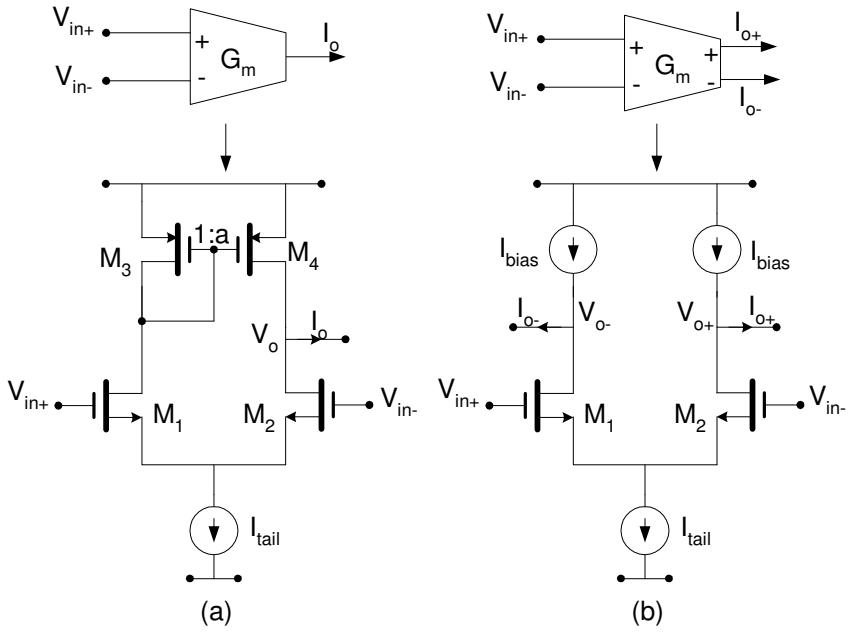


Fig. 2.5. (a) Single ended differential OTA, (b) conventional fully differential OTA

Some of the features of the fully differential version are: (1) It has a reasonable common mode gain, (2) The linearity of the input pair is better than the single input transconductor, cause the even order harmonics are cancelled out due to the differential signaling, (3) It has a reasonable power supply rejection ratio (PSRR), which is the ability of the circuit to be resistant to variations in the power supplies, (4) However the linear input range is limited due to the presence of the tail current source also (5) It has a limited tuning range. (Appendix B discusses the limitation of tuning range in MOS devices operating in saturation region).

Another variation of the differential input/output OTA is the pseudo-differential OTA. Fig. 2.6 shows a simple pseudo-differential OTA. The main visible difference between the fully differential and its pseudo differential counterpart is the absence of the tail current source. This would help in improving the linear input range (wider common mode input range) and also makes the circuit suitable to work for low voltage applications. The major drawbacks of the circuit is the requirement of a strong and fast

common mode feedback circuit to (1) Fix common mode output voltage, (2) Suppress common mode signals. The circuit also has a poor PSRR and a poor common mode gain.

Design of the common mode feedback loops or improving the circuit parameters is beyond the scope of this chapter. This chapter focuses on creating a valid model for the OTA-C filter that utilizes the OTA blocks, which are mentioned above. The voltage V_{bias} is derived from a common mode feedback control loop and it is used to fix the output common mode voltage.

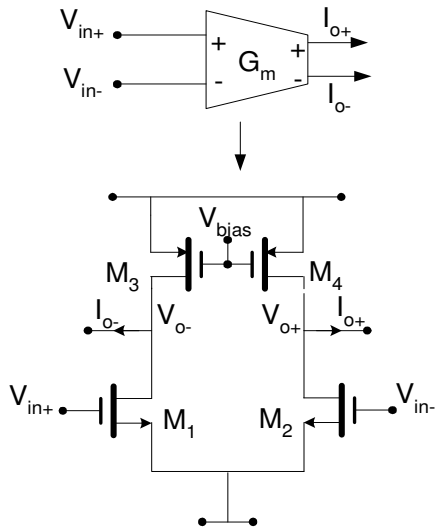


Fig. 2.6. A simple pseudo-differential OTA

Fig. 2.7 shows the concept of the common mode feedback (CMFB) circuits. A CMFB circuit is classically performed by means of an additional loop as shown in Fig. 2.7. The output common-mode level (V_{CM}) is sensed using a common-mode detector, i.e., $V_{CM} = (v_{OUT}^{+} + v_{OUT}^{-})/2$. It is then compared with the reference voltage $V_{REF,}$ and an error-correcting signal is injected to the biasing circuitry of the OTA. The CMFB loop has to be designed carefully to avoid potential stability problems. This increases the complexity of the design, the power consumption, and the silicon area used. The

frequency response of the differential path is often affected due to the added parasitic components involved in conventional CMFB schemes.

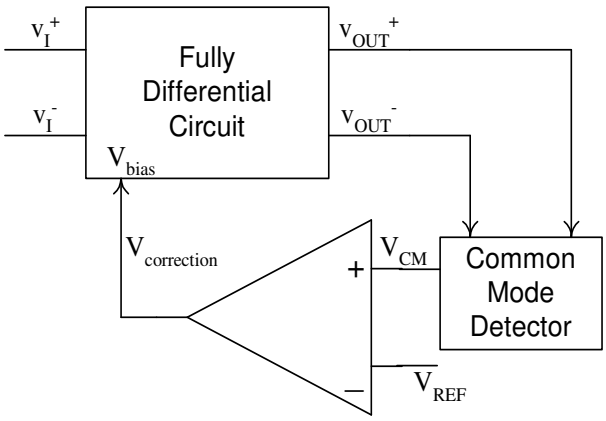


Fig. 2.7. Conventional common mode feedback (CMFB) loop

2.1.2.1. Macromodel of the OTA

A macromodel for the differential input OTA is presented in Fig. 2.8. The macro model [44] takes into account the frequency dependence of the transconductance parameter g_m. The linear transconductance can be represented by g_m. In all cases the transconductance is not the linear one. Hence there is a need to also consider the non linear effects of the transconductance term. The term G_m in the Fig. 2.8 exhibits the non-linear dependence of i_d on V_d as shown in equation set (2.5).

$$i_{out} = G_m(V_1 - V_2) = G_m v_d : \quad G_m = \text{Nonlinear Transconductance} \tag{2.5a}$$

$$i_{out} = g_1 v_d + g_3 v_d^3 + g_5 v_d^5 + ... \tag{2.5b}$$

$$g_n = \frac{1}{n!}\frac{\partial^n i_{out}}{\partial v_d^n}\bigg|_{v_d=0} : g_1 = g_m \ (\text{Linear Transconductance}) \tag{2.5c}$$

$$i_{out} \cong g_m v_d \rightarrow \text{linear case} \tag{2.5d}$$

It does not neglect the input and output impendence which would ideally be taken as infinity. The transconductance g_m is frequency dependant and is approximated with one dominant pole, which is represented as ω_p. The constant DC related transconductance term is represented by g_{mo} . Equation (2.5e) shows the frequency dependence of the transconductance term. The input capacitor C_p includes the input parasitic capacitances at the gate of the input differential transistor (which includes the gate to source capacitor C_{gs}, gate to drain capacitor C_{gd}).

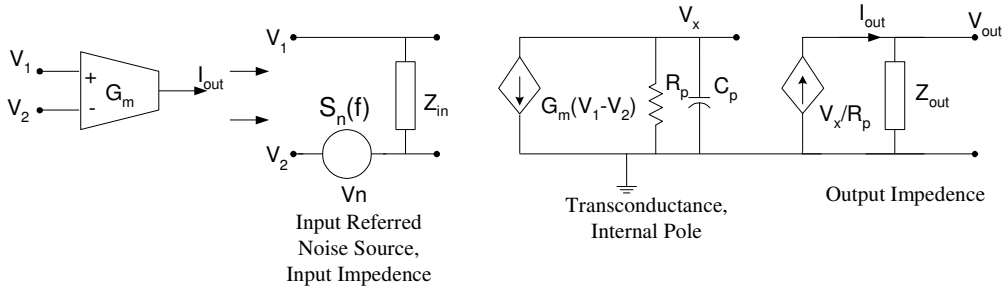


Fig. 2.8. Non-linear OTA macro model

$$g_m(s) = \frac{g_{mo}}{1 + s/\omega_p} \quad : \omega_p = \frac{1}{R_1 C_p} \tag{2.5e}$$

Also, the phase model is often used, which is described as follows: where $\Phi = \omega\tau$ is the phase delay with $\tau = 1/\omega_p$ giving the time delay. This can also be termed as excess phase, which is the difference between the actual phase and the minimum phase, the phase shift in excess of the minimum phase shift.

$$g_m(j\omega) = g_{mo} e^{-j\phi} \tag{2.5f}$$

The input impedance can be modeled by connecting a resistance R_i in parallel with a capacitance C_i from each input terminal of the ideal OTA to ground and a capacitance C_{in} in parallel with a resistance R_{in} between the input terminals. When one of the input terminals is grounded the input impedance is simplified being the parallel

combination of the resistances R_i, R_{in} and the capacitance $C_i + C_{in}$. In most cases like the one shown in Fig. 2.8 the resistors R_i and R_{in} are taken to be infinity and the capacitor C_i is negligible. The OTA output impedance is modeled by the parallel combination of a resistance R_{out} and a capacitance C_{out} connected between the OTA output terminal and the ground. There are secondary and other non-idealities that contribute to the non-linear behavior of the transconductance. The modeling tool should consider all these non-idealities. In spite of all these imperfections, though, careful design can minimize their effect on the available bandwidth, which remains much higher than that of an OpAmp. This makes OTAs very useful for the design of active filters at high frequencies.

The macro-model of the OTA presented in Fig. 2.8 also includes the noise components. The noise produced by the entire OTA circuit can be modeled as an input voltage source defined by a noise spectral density *Sn(f)*. This overall macromodel of the OTA is used extensively in this research thesis.

2.1.3. Simple Applications of OTA

The differential OTA can be used for various applications like simple resistor implementation, an amplifier, a voltage variable resistor, an integrator etc. These blocks [54] are explained in brief below. The single ended version of the OTA is shown in all cases.

2.1.3.1. Voltage Amplifier / Integrator

Inverting and non-inverting voltage amplification and also integration can be achieved using an OTA. Fig. 2.9 shows the simple OTA with a load . If Z_L is a passive resistor R_L, then the structure behaves like a voltage amplifier and depending on the polarity of the input the voltage amplifier could be a positive or negative one. Any desired gain can be achieved by a proper choice of g_m and R_L. It should be noted that the output voltage V_o is obtained from a source with output impedance equal to R_L.

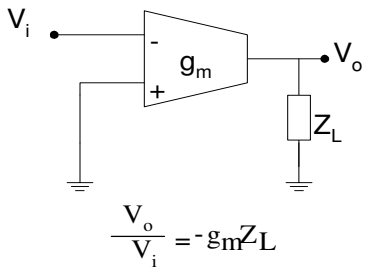


Fig. 2.9. OTA with load

If the load is a capacitor *C,* the structure behaves like a first order integrator. The integrator is also discussed in detail in the following sections. Zero output impedance can be achieved only if a buffer or voltage follower follows such circuits.

2.1.3.2. Voltage Variable Resistor

A grounded voltage-variable resistor can be easily obtained using the ideal OTA as shown in Fig. 2.10. Since $I_o = -I_i$,

$$Z_i = \frac{V_i}{I_i} = \frac{V_i}{-I_o} = \frac{V_i}{g_m V_i} = \frac{1}{g_m} \tag{2.6}$$

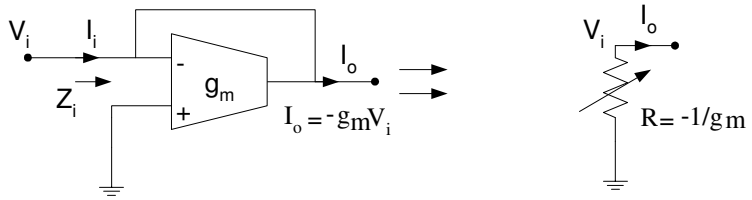


Fig. 2.10. Grounded voltage variable resistor

Using two such arrangements cross-connected in parallel, a floating VVR can be obtained. On the other hand, if in Fig. 2.10 the input terminals are interchanged, the

input resistance will be $1/g_m$. Thus, using OTAs, both positive and negative resistors become available without actually having to build them on the chip. These, coupled with capacitors, lead to the creation of the so-called active-C filters

2.1.3.3. Voltage Summation

Voltage summation can be obtained using OTAs, which in effect translate voltages to currents. These are easily summed as shown in Fig. 2.11 for two voltages V_1 and V_2. it is clear that from (2.7), (2.8) and (2.9), V_o is a function of V_1 and V_2. By adjusting the values of the transconductances, a voltage summer can be obtained. By changing the grounded input of one of the input OTAs, voltage subtraction can be achieved. These operations are useful for the realization of transfer functions.

$$I_{o1} + I_{o2} + I_o = 0 \tag{2.7}$$

$$g_{m1}V_1 + g_{m2}V_2 - g_{mo}V_o = 0 \tag{2.8}$$

$$V_o = \frac{g_{m1}}{g_{mo}}V_1 + \frac{g_{m2}}{g_{mo}}V_2 \tag{2.9}$$

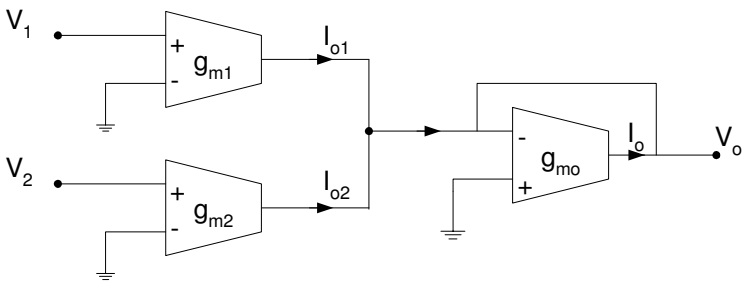


Fig. 2.11. Voltage summation

2.1.3.4. Integrator

The operation of integration can be achieved very conveniently using the OTA as is shown in Fig. 2.12. Clearly, It follows that both inverting and noninverting integration is easily achieved.

$$V_o = \frac{I_o}{sC} = \frac{g_m}{sC}(V_1 - V_2) \tag{2.10}$$

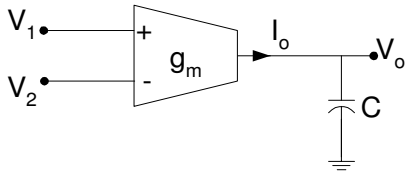


Fig. 2.12. First order integrator

Of course, in all cases, the output impedance of the circuit is nonzero. If a resistor is connected in parallel with C in Fig. 2.12, the integration will become lossy. On the other hand, connecting the circuit in Fig. 2.10 at the output of that in Fig. 2.12, the integration becomes both lossy and adjustable.

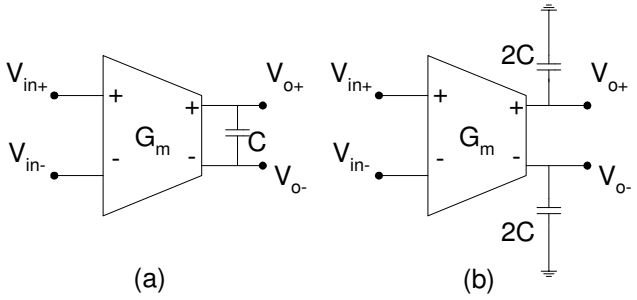


Fig. 2.13. Integrator with (a) floating capacitors, (b) grounded capacitors

Fig. 2.13 shows the fully differential version of the OTA integrator. The capacitors can be floating between the two outputs or grounded from each of the outputs to ground. Note that the grounded realization required 4 times the area for a single floating capacitor. There are other parasitic capacitors associated with the general OTA-C structure, Fig. 2.14 shows the parasitic capacitors. The transfer function, equation (2.10), is sensitive to unavoidable parasitic capacitors as well as to the OTA output conductance g_o. Observe from Fig. 2.14 that the output conductance is in parallel with the integrating capacitor C, and that the output capacitances C_o from the positive and negative output nodes of the OTA circuitry to ground add to the value of C. Furthermore, in IC technology floating capacitors have a substantial parasitic capacitance C_s (about 10% of the value of C) from the bottom plate to the substrate, i.e., to ac ground. To maintain symmetry, the integrating capacitor can be split into two halves connected such that the parasitic bottom plate capacitors $0.5C_s$ appear at the two OTA outputs.

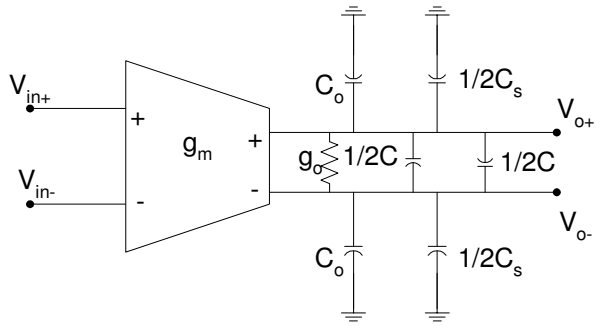


Fig. 2.14. Parasitic capacitors associated with OTA-C structure

Taking the parasitics into consideration, evidently, the integrator realizes (2.11),

$$\frac{V_o}{V_i} = \frac{g_m}{sC_{int} + g_o}\Big|_{s=j\omega} = \frac{g_m}{j\omega C_{int}\left(1 - \frac{j}{Q_{int}}\right)} \tag{2.11}$$

that is it becomes lossy with a finite integrator quality factor, equation (2.12), and an effective integrating capacitor C_{int}, as shown in (2.13).

$$Q_{int} = \frac{\omega C_{int}}{g_o} \tag{2.12}$$

$$C_{int} = C + \frac{1}{2}\left(\frac{C_s}{2} + C_o\right) \tag{2.13}$$

To give a numerical example for the effect of the parasitic capacitances, consider the output capacitance C_o of 0.15pF for an actual load capacitance of C=1pF. The value of C_s can be considered to be around 0.1pF. Thus due to the parasitic effects the total load capacitance is now around 1.1pF according to (2.13). For an output conductance around a few micro mhos, there will be a finite integrator quality factor introduced.

To maintain the correct integration constant as nominally designed, the circuit capacitor C should be predistorted to reflect the parasitics appearing at the integration nodes. The parasitics should be estimated as best as possible, for example from a layout process file, and their values subtracted from the nominal value of C in the final layout.

If grounded capacitors are used, the bottom plate should, of course, be connected to ground so that the substrate capacitances are connected between ground and the power supply. Thus, they are shorted out for the signals and play no role. Observe that the presence of parasitic capacitors tends to limit the high-frequency performance of these filters because high frequency filters require large time constants, g_m/C, i.e., small capacitors. The smallest capacitor C, however, must obviously be larger than the sum of all parasitics connected at the integrator output nodes to be able to absorb these parasitics. Because the values of the parasitic capacitors can generally only be estimated, one typically chooses C to be at least three to five times larger than the expected parasitics to maintain some predictability in the design. The reader will notice that integrators with grounded capacitors have a small advantage in high-frequency circuits where parasitic capacitors become large relative to C.

2.1.4. Non Idealities of OTA

There are many non-idealities to the design of an OTA-C filter, which includes the OTA as the basic active block. They include non-linearity of the input differential pair, mismatch between devices, offsets (systematic and random), capacitor non-linearities, noise from the circuit. However the non-ideal behavior of the circuit to mismatch, offsets can be reduced by effective layout techniques and also some design techniques and they are beyond the scope of this research. A brief overview is given regarding the non-linearities from the circuit and also the capacitor.

The effects of noise were already mentioned in the first chapter. Every active block is going to contribute to the output noise current in some form or the other. So do the resistive components. However a complete modeling tool should consider the noise injected by all components to its output.

2.1.4.1. Non-Linearity of the OTA

Basics of non-linearity of any circuit were introduced in the previous chapter. Every OTA used in the design of various blocks are differential in nature. They have a positive and a negative input counterpart. The simplest OTA introduced in the previous section is that of a simple differential pair with a tail current source. The input is a voltage variable and the output is current. The transconductance of the input transistor causes this conversion. The dependencies of the transconductance term on the input gate to source voltage, V_{GS}, of the transistors leads to the non-linear behavior of these circuits. A thorough study of non-linearities in differential circuits and their minimization is studied in the next chapter.

2.1.4.2. Capacitor Non-Linearity

The charge stored in the capacitor is a function of the value of the capacitance and is proportional to the voltage across it (i.e. $Q=CV$). The voltage dependencies of the capacitance could lead to non-linearities due to the capacitor [55]. This effects mostly

the switched capacitor circuits cause the main non-linear blocks would be the capacitance in those cases.

There are some modeling techniques to model the non-linearities of the OTA, [64-67] analyzing the frequency dependencies of the non-linear terms. Some of the known methods existing in the literature are Volterra series [68] of modeling of the non-linear behavior of analog integrated circuits and the Harmonic injection [69] method of analyzing non-linearities. The Volterra series method is very complex and it combines the theory of convolution and Taylor series expansion to describe a non-linear system with memory. The Volterra series expansion is a powerful yet complicated method since it involves breaking the non-linear system down into infinite parallel subsystems ranging from a linear subsystem, a quadratic subsystem, a cubic subsystem to an infinite-order subsystem. It is also limited to the modeling of weak non-linearities. The Harmonic injection method is a simpler method when compared to the Volterra series expansion method. It is used to describe the non-linear behavior of an analog circuit by analyzing every non-linear system as a linear system plus some weak nonlinearities. The weak nonlinearities at the input are considered as harmonics injected into the linear system. This method is also however restricted to weak non-linearities.

This thesis proposes a more intense and comprehensive way to model the non-linearities of the OTA used in the general order OTA-C filters. It is not restricted to the weak non-linearities. It is a very fast and simple approach. It is based on the matrix description of the general OTA-C filter. The following sections present the modeling tool in detail. Appendix A also shows the software tool created based on the modeling process.

2.2. Proposed Generalized Non-Linearity and Noise Modeling Approach

The proposed non-linearity and noise-modeling tool is explained in the following sections.

2.2.1. A General Structure of a Gm-C (OTA-C) Filter

Consider the general structure of a voltage-mode Gm-C filter in Fig. 2.15. The current-mode counterpart can be obtained by inverting all transconductors and interchanging input and output of the filter [64]. The structure in Fig. 2.15 contains n internal nodes labeled x_i; $i=1,2,3\ldots n$: n input transconductors G_{mbi}, a set of internal feedback and feedforward transconductors, G_{mij} , an output summer consisting of transconductors c_iG_m and $-G_m$ as well as a feedforward transconductor from input to output, dG_m. The transconductors form the active network, while the capacitors C_{bi}, $i=1,2,3\ldots.,n$ and C_{ij} $(1 \leq i, j \leq n)$ form the passive network. Of course, $C_{ij} = C_{ji}$. It is readily seen that any Gm-C filter can be obtained as a special case of the general structure in Fig. 2.15 by setting the appropriate elements to zero. Note that n is not necessarily equal to the degree of the filter transfer function.

To derive an analytical description of the structure in Fig. 2.15, the voltage-to voltage transfer function $H_v(s)$ of the filter in voltage mode can be calculated and shown that it is the same as the current-to-current transfer function $H_c(s)$ when the circuit operates in current-mode. For simplicity, the voltage at the ith node x_i can be denoted also by x_i. In the Laplace domain, the voltage-mode Gm-C filter in Fig. 2.15 can be described by the matrix equations (2.14) and (2.15).

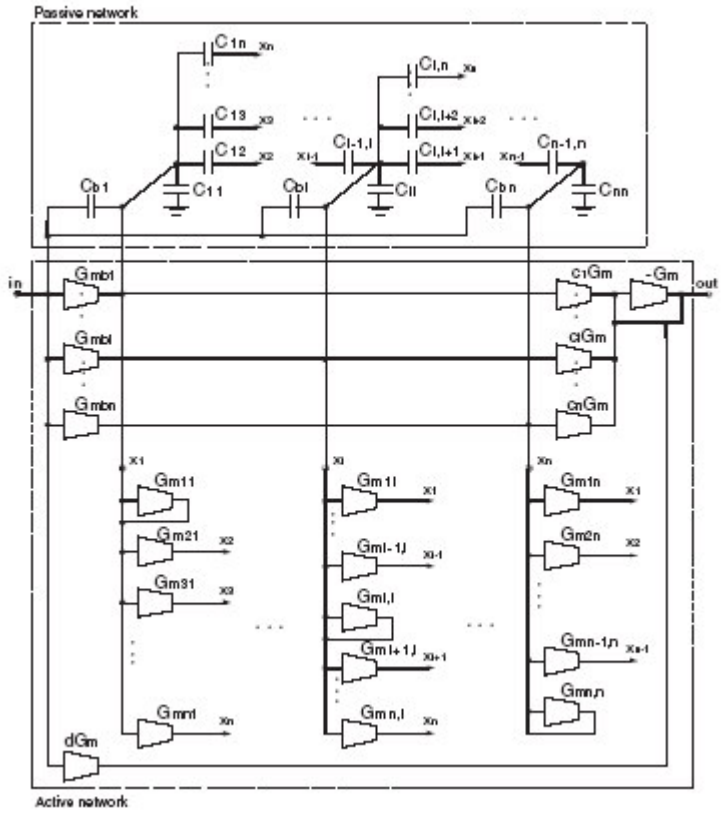


Fig. 2.15. The general structure of a voltage mode Gm-C filter (Source: [50])

$$\begin{bmatrix} \sum_{j=1}^{n} C_{1j} & -C_{12} & \cdots & -C_{1n} \\ -C_{12} & \sum_{j=2}^{n} C_{2j} & \cdots & -C_{2n} \\ \vdots & \vdots & \cdots & \vdots \\ -C_{1n} & -C_{2n} & \cdots & \sum_{j=1}^{n} C_{nj} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix} = \begin{bmatrix} u_i G_{mb1} + (u_i - x_1) sC_{b1} + \sum_{j=1}^{n} G_{m1j} x_j \\ u_i G_{mb2} + (u_i - x_2) sC_{b2} + \sum_{j=1}^{n} G_{m2j} x_j \\ \vdots \\ u_i G_{mbn} + (u_i - x_n) sC_{bn} + \sum_{j=1}^{n} G_{mnj} x_j \end{bmatrix} \quad (2.14)$$

and

$$u_o = \begin{bmatrix} c_1 & \cdots & c_n \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix} + du_i \quad (2.15)$$

where u_i, u_o are the input and output voltages, respectively. The vector on the right-hand side of (2.14) can be written in the form, as shown in (2.16).

$$\begin{bmatrix} G_{m11} & G_{m12} & \cdots & G_{m1n} \\ G_{m21} & G_{m22} & \cdots & G_{m2n} \\ \vdots & \vdots & \cdots & \vdots \\ G_{mn1} & G_{mn2} & \cdots & G_{mnn} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix} - s \begin{bmatrix} C_{b1} & 0 & \cdots & 0 \\ 0 & C_{b2} & \cdots & 0 \\ \vdots & \vdots & \cdots & \vdots \\ 0 & 0 & \cdots & C_{bn} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix} + \begin{bmatrix} G_{mb1} + sC_{b1} \\ G_{mb2} + sC_{b2} \\ \vdots \\ G_{mbn} + sC_{bn} \end{bmatrix} \quad (2.16)$$

To achieve more compact notation, some general matrices are introduced, like the T_c, G and C_c as shown in (2.17a), (2.17b), (2.17c) respectively.

$$T_c = \begin{bmatrix} \sum_{j=1}^{n} C_{1j} & -C_{12} & \cdots & -C_{1n} \\ -C_{12} & \sum_{j=2}^{n} C_{2j} & \cdots & -C_{2n} \\ \vdots & \vdots & \cdots & \vdots \\ -C_{1n} & -C_{2n} & \cdots & \sum_{j=1}^{n} C_{nj} \end{bmatrix}, \quad X = \begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix} \quad (2.17a)$$

$$G = \begin{bmatrix} G_{m11} & G_{m12} & \cdots & G_{m1n} \\ G_{m21} & G_{m22} & \cdots & G_{m2n} \\ \vdots & \vdots & \cdots & \vdots \\ G_{mn1} & G_{mn2} & \cdots & G_{mnn} \end{bmatrix}, \quad \tilde{C}_c = \begin{bmatrix} c_1 & \cdots & c_n \end{bmatrix} \quad (2.17b)$$

$$\tilde{C}_c = \begin{bmatrix} G_{mb1} + sC_{b1} & \cdots & G_{mbn} + sC_{bn} \end{bmatrix}, \quad D = d \quad (2.17c)$$

The matrix T_c is a symmetrical one i.e. T^T_c=T_c. The general equations of (2.14) and (2.15) can be modified to a much simpler form to handle, (2.18).

$$sT_cX = GX + \tilde{C}_c^T u_i \quad , \quad u_o = \tilde{C}_v X + Du_i \quad (2.18)$$

A similar set of equations can be obtained for the current mode filter using the general matrix set of (2.17). The general form for a current mode filter is shown in (2.19),

$$sT_cX = G^T X + \tilde{C}_v^T i_i \quad , \quad i_o = \tilde{C}_c X + Di_i \quad (2.19)$$

where as before, the entries x_i of the vector X denote the internal node voltages, and i_i, i_o are the input and output currents, respectively.

The transfer functions, equation (2.20a) and (2.20b) of the general voltage and current mode type of Gm-C filters can be evaluated from (2.18) and (2.19).

$$H_v(s) = \frac{u_o(s)}{u_i(s)} = \tilde{C}_v (sT_c - G)^{-1} \tilde{C}_c^T + D \tag{2.20a}$$

$$H_c(s) = \frac{i_o(s)}{i_i(s)} = \tilde{C}_c \left(sT_c - G^T\right)^{-1} \tilde{C}_v^T + D \tag{2.20b}$$

From these equations it is also easy to verify the dual behavior of the voltage and current mode filters. Using the fact as long as a matrix is scalar, $H^T=H$ also $(A^{-1})^T = (A^T)^{-1}$ for any invertible matrix A, also T_c being symmetrical, (2.21) proves that $H_v(s) = H_c(s)$.

$$\begin{aligned} H_v(s) = \frac{u_o(s)}{u_i(s)} = \tilde{C}_v (sT_c - G)^{-1} \tilde{C}_c^T + D = \left(\tilde{C}_v (sT_c - G)^{-1} \tilde{C}_c^T + D\right)^T \\ \Rightarrow = \tilde{C}_c \left(sT_c - G^T\right)^{-1} \tilde{C}_v^T + D = \frac{i_o(s)}{i_i(s)} = H_c(s) \end{aligned} \tag{2.21}$$

Since the two transfer function forms are equal, they can be represented as just $H(s)$ with no subscript to denote the filter transfer function. By labeling the adjoint matrix of sT_c-G as $\tilde{A}$, as in (2.22), the general transfer function $H(s)$ can be written as in (2.23).

$$\tilde{A}(s) = \text{adj}\,(sT_c - G) = \text{adj}\left(sT_c - G^T\right)^T = \left[\tilde{A}_{ij}(s)\right]_{i,j=1}^{n} \tag{2.22}$$

$$H(s) = \frac{1}{\det\,(sT_c - G)} \sum_{i,j=1}^{n} c_i \left(G_{mbj} + sC_{bj}\right) \tilde{A}_{ij}(s) + d \tag{2.23}$$

With these general expressions, the transfer function of any particular, more specialized Gm-C topology can easily be computed. For instance, many filters have no input capacitors, an input signal distribution, and the output is taken directly from one of the internal nodes. Then $\tilde{C}_c = [G_{mb1} \cdots G_{mbn}]$ and $\tilde{C}_v = [0 \cdots 0\ 1_k\ 0 \cdots 0]$ where the notation "1_k" denotes a "1" at the kth position. In this case, Equation (2.23) reduces to (2.24).

$$H(s) = \frac{1}{\det\,(sT_c - G)} \sum_{i=1}^{n} G_{mbi} \tilde{A}_{ki}(s) \tag{2.24}$$

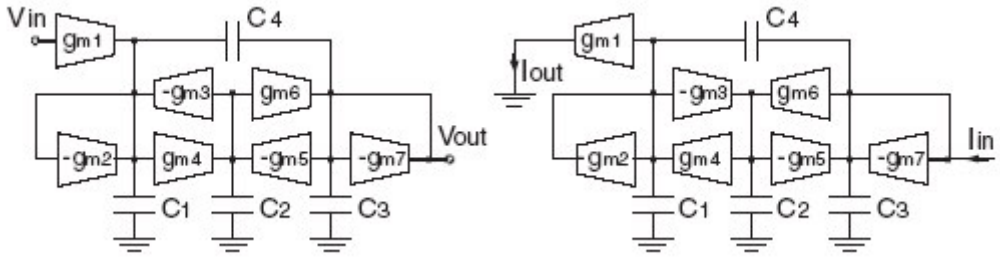
As an example of the general Gm-C topology in Fig. 2.15, a LC ladder simulation for a third-order elliptic filter, Fig. 2.16, is presented below. The matrices T_c,

G, $\tilde{C}_c$, $\tilde{C}_v$ and D for this circuit (internal nodes indexed from left to right) are as given in (2.25).

$$T_c = \begin{bmatrix} C_1 + C_4 & 0 & -C_4 \\ 0 & C_2 & 0 \\ -C_4 & 0 & C_3 + C_4 \end{bmatrix}, G = \begin{bmatrix} -g_{m2} & -g_{m3} & 0 \\ g_{m4} & 0 & -g_{m5} \\ 0 & g_{m6} & -g_{m7} \end{bmatrix}, \begin{pmatrix} \tilde{C}_c = [g_{m1}\ 0\ 0] \\ \tilde{C}_v = [0\ 0\ 1] \\ D = 0 \end{pmatrix} \tag{2.25}$$

The transfer function, H_3, of the filter can be calculated using (2.24) with $i=1$ and $k=3$. Assuming for simplicity that all transconductances are equal, i.e. $g_{mi} = g_m$ for $i=1,2, .. 7,$ the determinant can be obtained as shown in (2.26).

$$\begin{aligned} \det(sT_c - G) = {} & C_2(C_1C_3 + C_1C_4 + C_3C_4)s^3 + C_2(C_1 + C_3 + 2C_4)g_m s^2 \\ & + (C_1 + C_2 + C_3)g_m^2 s + 2g_m^3 \end{aligned} \tag{2.26}$$



(a) (b)

Fig. 2.16. Third order Elliptic Gm-C filter (a) voltage mode and (b) current mode

The adjoint vector can be derived to a simpler form as shown in (2.27).

$$\tilde{A}_{31}(s) = C_2C_4s^2 + g_m^2 \tag{2.27}$$

Now letting $C^2_x = C_1C_3 + C_1C_4 + C_3C_4$ the transfer function $H_3(s)$ becomes,

$$H_3(s)=\left(\frac{C_4 g_m}{C_x^2}\right)\times\frac{s^2+\left(g_m^2/C_2C_4\right)}{s^3+\left((C_1+C_3+2C_4)\frac{g_m}{C_x^2}\right)s^2+\left((C_1+C_2+C_3)\frac{g_m^2}{C_2C_x^2}\right)s+\left(\frac{2g_m^3}{C_2C_x^2}\right)} \tag{2.28}$$

The example illustrates the ease and elegance provided by the general approach presented in this section when calculating the transfer function of any Gm-C filter structure.

A general method to design any arbitrary linear OTA-C filter was presented in the previous section. This general flow can be used for modeling the non-linearities and also noise of any general OTA-C filter. Sections 2.2 and 2.3 focus more on the utilization of the general matrix method to derive the non-linearity and noise model for an OTA-C filter.

2.2.2. Dynamics of Nonlinear OTA-C Filters

To proceed with the modeling of non-linearities, the general figure of 2.15 is modified and used in Fig. 2.17. The structure in Fig. 2.17 contains n internal nodes denoted as x_i, i=1,...,n, n input transconductors G_{bi}, an output summer consisting of transconductors G_{ci}, G_o and a feedforward transconductor G_d, as well as a set of feedback and feedforward transconductors G_{ij}. The transconductors used are assumed to be nonlinear blocks. All transconductors form active network, while input capacitors C_{bi}, i=1,...,n and capacitors C_{ij}, $1\le i<j\le n$ form passive network. The capacitors are assumed to be linear, since in most practical filters inherent nonlinearities of capacitors can be neglected in comparison to those of active elements. It is easily seen that any OTA-C filter is a particular case of the general structure in Fig. 2.17. Note also that n is not necessarily equal to the order of the filter transfer function. The connection between the number n of internal nodes, the order of the filter and its particular structure was investigated in detail in [50].

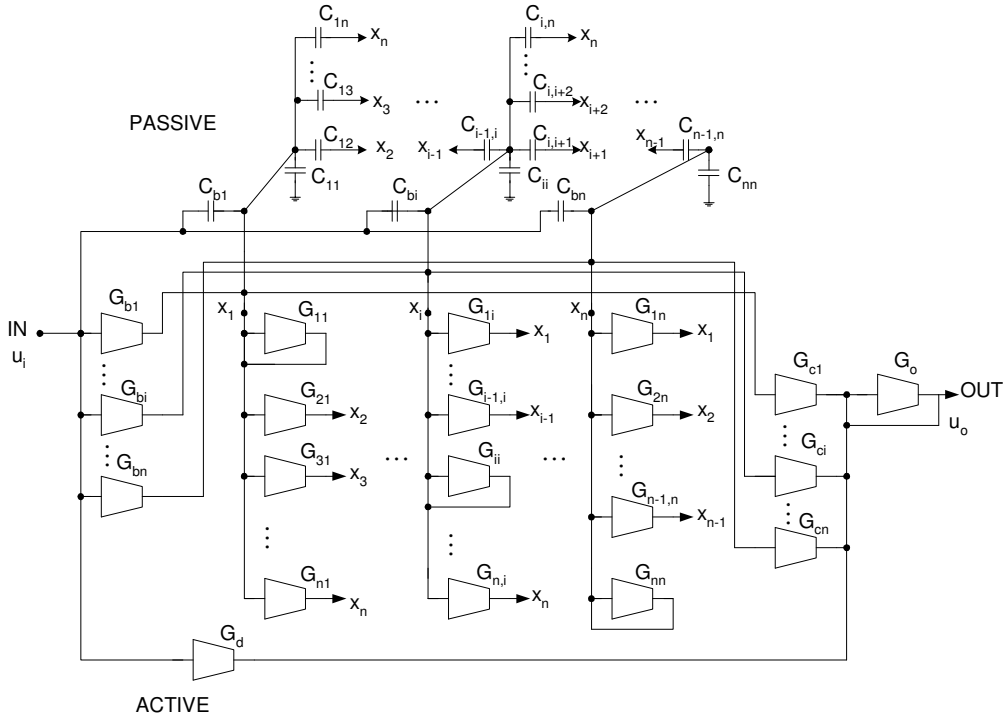


Fig. 2.17. Generalized structure of OTA-C filter

An analytical description of the considered structure in the time domain can be derived. To derive the same, the following considerations are made: the voltage at the ith node x_i can be denoted as by x_i. Symbols u_i, u_o will denote the input and output voltages, respectively. These notations., also some more are used and introduced in Fig. 2.17.

According to the notations given in Fig. 2.18 the general structure of OTA-C filter in Fig. 2.17 can be described by the following system of integral equations,

$$x_k(t) = \frac{1}{c_{kk}} \int_0^t i_k(\tau) d(\tau) + x_k(0), \quad k = 0,1,2...n \tag{2.29}$$

$$x_k(t) - x_1(t) = \frac{1}{c_{kl}} \int_0^t i_{kl}(\tau) d(\tau) + x_k(0) - x_1(0), \quad k,1 = 0,1,2...n : k \le 1 \tag{2.30}$$

$$u_i(t) - x_k(t) = \frac{1}{c_{bk}} \int_0^t i_{bk}(\tau) d(\tau) + u_i(0) - x_k(0), \quad k = 0,1,2...n \tag{2.31}$$

$$-\sum_{l=1, l\neq k}^{n} i_{lk}(t) + i_k(t) - i_{bk}(t) = \sum_{l=1}^{n} G_{kl}(x_l(t)) + G_{bk}(u_i(t)), \quad k = 1,2....n \tag{2.32}$$

$$u_o(t) = -G_o^{-1}\left(\sum_{l=1}^{n} G_{cl}(x_l(t)) + G_d(u_i(t)) \right) \tag{2.33}$$

The following initial conditions can be assumed

$$x_k(0) = x_{0k}\ , \quad k = 1,2.....n \qquad u_i(0) = u_{i0} \tag{2.34}$$

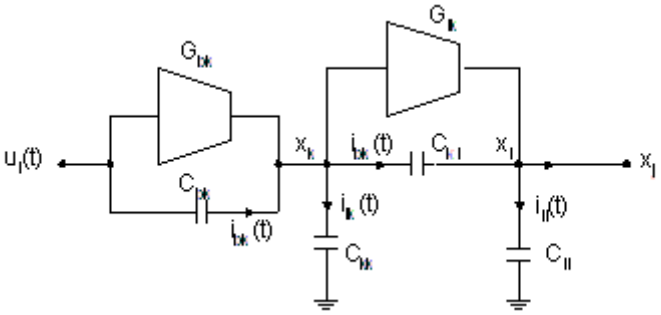


Fig. 2.18. Structure for notation representation

It can be noted that G_{kl}, G_{bk}, G_{cl}, G_d and G_o, k,l=1,2,...,n are in general nonlinear functions of their input variables. The system described by (2.29)-(2.31), (2.34) is equivalent to the following system of differential equations (2.35)-(2.37), with the initial condition (2.34).

$$i_k(t) = C_{kk} \frac{dx_k(t)}{dt}, \quad k = 1,2....n \tag{2.35}$$

$$i_{kl}(t) = C_{kl}\left(\frac{dx_k(t)}{dt} - \frac{dx_l(t)}{dt}\right), \quad k,l = 1,2.....n : k < l \tag{2.36}$$

$$i_{bk}(t) = C_{bk}\left(\frac{du_i(t)}{dt} - \frac{dx_k(t)}{dt}\right), \quad k,l = 1,2.....n \tag{2.37}$$

Inserting (2.35), (2.36) and (2.37) into (2.32) and denoting $dx_k(t)/dt$ by $x'_k(t)$ the following is obtained, for k=1,2,...,n,

$$-\sum_{l=1,l\neq k}^{n} C_{lk}\left(x'_l(t) - x'_k(t)\right) + C_{kk}x'_k(t) - C_{bk}\left(u'_i(t) - x'_k(t)\right) = \sum_{l=1}^{n} G_{kl}\left(x_l(t)\right) + G_{bk}\left(u_i(t)\right) \tag{2.38}$$

which can be rewritten as equation (2.39).

$$\left(C_{bk} + \sum_{l=1}^{n} C_{lk}\right)x'_k(t) - \sum_{l=1,l\neq k}^{n} C_{lk}x'_l(t) = \sum_{l=1}^{n} G_{kl}\left(x_l(t)\right) + G_{bk}\left(u_i(t)\right) + C_{bk}u'_i(t) \tag{2.39}$$

To simplify the notation, in (2.39), the symbols C_{kl} (k>l) that denote the same elements as C_{lk} are used.

Defining the vectors $x(t)$ and $x'(t)$ as (2.40),

$$\mathbf{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \\ x_n(t) \end{bmatrix}, \qquad \mathbf{x}'(t) = \begin{bmatrix} x'_1(t) \\ x'_2(t) \\ \vdots \\ x'_n(t) \end{bmatrix}, \qquad \mathbf{x}_0 = \begin{bmatrix} x_{01} \\ x_{02} \\ \vdots \\ x_{0n} \end{bmatrix} \tag{2.40}$$

and matrix T_c as, (2.41), the system of expressions represented in (2.39), (2.33) and (2.34) can be reframed. This is shown in equation (2.42) and (2.43).

$$T_C = \begin{bmatrix} C_{b1} + \sum_{j=1}^{n} C_{1j} & -C_{12} & \cdots & -C_{1n} \\ -C_{12} & C_{b2} + \sum_{j=1}^{n} C_{2j} & \cdots & -C_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{1n} & -C_{2n} & \cdots & C_{bn} + \sum_{j=1}^{n} C_{nj} \end{bmatrix} \tag{2.41}$$

$$T_C x'(t) = T_C\left(\begin{bmatrix} x'_1(t) \\ x'_2(t) \\ \vdots \\ x'_n(t) \end{bmatrix}\right) = \begin{bmatrix} \sum_{l=1}^{n} G_{1l}\left(x_l(t)\right) \\ \sum_{l=1}^{n} G_{2l}\left(x_l(t)\right) \\ \vdots \\ \sum_{l=1}^{n} G_{nl}\left(x_l(t)\right) \end{bmatrix} + \begin{bmatrix} G_{b1}\left(u_i(t)\right) + C_{b1}u'_i(t) \\ G_{b2}\left(u_i(t)\right) + C_{b2}u'_i(t) \\ \vdots \\ G_{bn}\left(u_i(t)\right) + C_{bn}u'_i(t) \end{bmatrix} \tag{2.42}$$

$$u_o(t) = -G_o^{-1}\left(\sum_{l=1}^{n} G_{cl}\left(x_l(t)\right) + G_d\left(u_i(t)\right)\right), \qquad x(0) = x_0, \quad u_i(0) = u_{i0} \tag{2.43}$$

Thus the general structure is represented in terms of differential equations, expressed in the matrix form as in (2.43).

Consider a special case, where all transconductors are linear, i.e. $G_{kl}(y)=G_{mkl}y$, $G_{bk}(y)=G_{mbk}y$, $G_{cl}(y)=G_{mcl}y$, $G_d(y)=G_{md}y$ and $G_o(y)=G_{mo}y$, $k,l=1,2,...,n$. The following matrices can be defined,

$$G = \begin{bmatrix} G_{m.11} & \cdots & G_{m.1n} \\ \vdots & \ddots & \vdots \\ G_{m.n1} & \cdots & G_{m.nn} \end{bmatrix}, \quad C = \begin{bmatrix} c_1 & \cdots & c_n \end{bmatrix}, \tag{2.44}$$

$$B = \begin{bmatrix} G_{m.b1} + C_{b1}\dfrac{d}{dt} & \cdots & G_{m.bn} + C_{bn}\dfrac{d}{dt} \end{bmatrix}^T, \quad D = d, \tag{2.45}$$

with $c_i = -G_{mci}/G_{mo}$, $i=1,2,...,n$ and $d = -G_{md}/G_{mo}$. Using the notation as prescribed by (2.44)-(2.45), the system of equations described by (2.44) and (2.45) can be rewritten in the time domain form as in (2.46),

$$\begin{aligned} T_C x'(t) &= Gx(t) + Bu_i(t) \\ u_o(t) &= Cx(t) + Du_i(t) \end{aligned}, \quad x(0) = x_0, \quad u_i(0) = u_{i0} \tag{2.46}$$

or, in the domain of Laplace transform (with zero initial conditions) as in (2.47).

$$\begin{aligned} sT_C X &= GX + Bu_i \\ u_o &= CX + Du_i \end{aligned} \tag{2.47}$$

in which X is the Laplace transform of the vector x. System (2.47) is nothing else but the matrix description of the general structure of a voltage-mode OTA-C filter introduced in

[50]. Thus, system (2.47) is a particular (linear) case of the general (nonlinear) system describing a filter circuit in Fig. 2.17.

Turning back to the general case note that under assumption of invertibility of the matrix T_C, equation (2.42) can be reformulated to the one shown in (2.48).

$$x'(t)=\begin{bmatrix} x'_1(t) \\ x'_2(t) \\ \vdots \\ x'_n(t) \end{bmatrix} = T_C^{-1}\left(\begin{bmatrix} \sum_{l=1}^{n} G_{1l}\left(x_1(t)\right) \\ \sum_{l=1}^{n} G_{2l}\left(x_1(t)\right) \\ \vdots \\ \sum_{l=1}^{n} G_{nl}\left(x_1(t)\right) \end{bmatrix} + \begin{bmatrix} G_{b1}\left(u_i(t)\right)+C_{b1}u'_i(t) \\ G_{b2}\left(u_i(t)\right)+C_{b2}u'_i(t) \\ \vdots \\ G_{bn}\left(u_i(t)\right)+C_{bn}u'_i(t) \end{bmatrix} \right) \tag{2.48}$$

The above assumption is very natural. In particular, it is satisfied if every internal node of the filter has a grounded capacitor (this is the case for any canonical OTA-C structure). The problem of invertibility of matrix T_C was thoroughly addressed in [50], where the necessary and sufficient conditions for T_C to be invertible were given.

The vector on the right-hand side of (2.48) can be denoted by $f\left(u_i(t), x(t)\right)$. Then, the differential system in question can be rewritten as

$$x'(t)=f\left(u_i(t), x(t)\right) \tag{2.49}$$

$$x(0)=x_0,\ u_i(0)=u_{i0} \tag{2.50}$$

together with the initial conditions, (2.50). This is a classical Cauchy problem which can be easily solved numerically.

The above model can be applied to calculate nonlinear distortion of any OTA-C filter for any given input signal. For example, for input signal of the form $u_i = U\cos(\omega t)$, after solving (2.49)-(2.50), the harmonics in the output signal can be calculated by evaluating the formula given in (2.51).

$$h_n=\frac{2}{T}\left|\int_{-T/2}^{T/2} u_0(t)\,e^{-j\frac{2n\pi t}{T}}dt\right|,\ n=1,2,...n \tag{2.51}$$

where T is input signal period. Integral in (2.51) can be evaluated numerically. From which some of the distortion parameters can be calculated, e.g. HD_3 and/or THD. In order to calculate other nonlinearity measures (2.49)-(2.50) has to be solved with different input excitation, e.g. to get IM_3 we need two harmonic signals, and so on.

In order to handle system (2.49), (2.50) one needs to know transfer characteristics of all filter transconductors, i.e. G_{kl}, G_{bk}, G_{cl}, G_d and G_o, k,l=1,2,...,n, i.e. the nonlinear macromodels of those transconductors is required. Transfer characteristic of a nonlinear transconductor can be modeled using a power series expansion but in order to get better accuracy it is advisable to model transfer characteristic as a table of input voltages and corresponding output currents and apply interpolation for the point out of a table. In this implementation of the model spline interpolation was put to use.

It should be emphasized that the method of evaluating nonlinear distortion described in this section is very fast and efficient. Unlike the approaches based on Volterra series representation ,[68], or harmonic injection method [69], it is not restricted to handle weak nonlinearities only. Also, since the presented formalism is based on the OTA-C filter model in Fig. 2.17, it is general enough to comprise all conceivable OTA-C filter structures.

2.2.3. Noise Analysis in General OTA-C Filters

The literature contains several intuitive ideas on calculating noise, and attempts to solve noise problems for specific filters [70]-[73]. In contrast, this section provides complete, explicit, and easily-evaluated formulas based on a general approach to noise analysis, and in addition presents simple methods for the optimization of noise performances of arbitrary OTA-C filters, based on their matrix description as developed in Section 2.2.1 and 2.2.2. The derived expressions can be applied to OTA-C filters with any known architecture and of any degree, and they can be easily implemented and used in computer-aided analysis/optimization software.

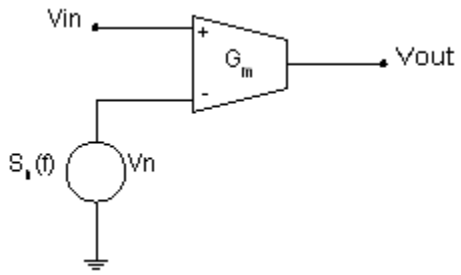


Fig. 2.19. Noise representation in an OTA with an equivalent voltage source

Assuming ideal, that is, lossless and, therefore, noiseless capacitors, the output noise of any OTA-C filter is a combination of the noise contributions of all its transconductors. As shown in Fig. 2.19, the noise of a CMOS transconductor with value g_m can be described by an equivalent input-referred noise-voltage source, v_n, whose spectral density, $S_n(f)$, can be modeled as [70],

$$S_n(f) = \frac{S_t}{g_m} + \frac{S_f}{f} \tag{2.52}$$

where the thermal noise component, S_t, and the flicker-noise component, S_f, depend on the transconductor topology and on biasing. It can be assumed that that noise sources associated with different OTAs are statistically independent.

The noise contribution in a CMOS circuit can be better understood using the example presented below. Fig. 2.20 shows the input stage of a traditional two stage OpAmp. Each transistor have been modeled using an equivalent voltage noise source. Voltage noise sources are used here since the low-frequency noise performance of this stage will be addressed. It is assumed that the transistors M_1, M_2 and M_3, M_4 are matched. From the theory of noise in CMOS devices presented, [70], the following set of equations can be derived.

Using the gain factors of the simple input stage, the output noise value seen at the output node can be written as shown in (2.53).

$$V_{no}^2(f) = 2(g_{m1}R_o)^2 V_{n1}^2(f) + 2(g_{m3}R_o)^2 V_{n3}^2(f) \tag{2.53}$$

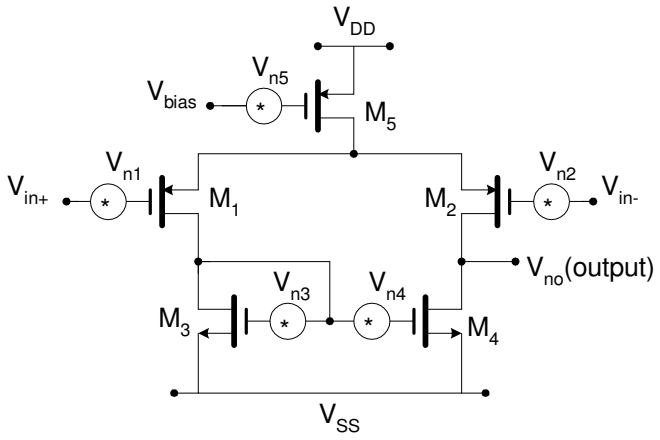


Fig. 2.20. A CMOS input stage with voltage noise sources

Equation (2.53) gives the noise component at the output node, where V_{n1} and V_{n3} are the noise voltages of transistors M1 and M3 respectively. The output noise can be related back to an equivalent input noise value $V_{neq}(f)$, by dividing it by the gain $g_{m1}R_o$, which results in (2.54)

$$V_{neq}^2(f) = 2V_{n1}^2(f) + 2V_{n3}^2(f)\left(\frac{g_{m3}}{g_{m1}}\right)^2 \tag{2.54}$$

For the white noise portion of $V_{n1}(f)$ and $V_{n3}(f)$, the substitution of (2.55) can be taken as a general case.

$$V_{ni}^2(f) = 4kT\left(\frac{2}{3}\right)\left(\frac{1}{g_{mi}}\right) \tag{2.55}$$

For the *1/f* noise component, flicker noise, which dominates at low frequencies, the general case for the noise spectral density of a CMOS transistor can be written as shown in equation (2.56), where K is dependant on device characteristics.

$$V_{ni}^2(f) = \frac{K_i}{W_i L_i C_{ox} f} \tag{2.56}$$

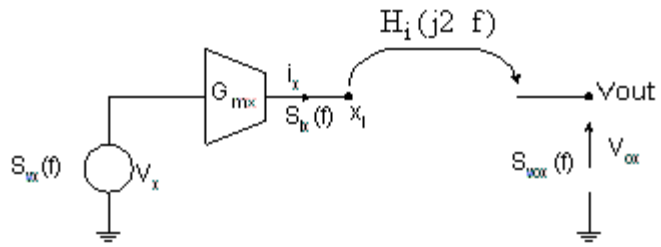


Fig. 2.21. Noise contributions of an individual filter transconductor to the output noise of the filter

To obtain the output- (and/or input-) noise spectrum of the general OTA-C topology in Fig. 2.17 (for the purpose of noise evaluation the filter model in Fig. 2.17 is used with transconductor values equal to linear transconductance of respective OTA, e.g. $G_{m.ij}=dG_{ij}(v)/dv$ at $v=0$) explicitly, the noise contribution of each individual transconductor to the output (and/or input) noise must be determined. This can be modeled as shown in Fig. 2.21. Let G_{mx} denote one of the filter transconductors (i.e. $G_{m.bi}$, $G_{m.ij}$, etc.), which is connected to one of the nodes, say x_i (if the filter contains a non-trivial output summer then it has an additional - output – node, which will be denoted as x_0). If the input-referred noise voltage of the noise source corresponding to G_{mx}, is labeled v_x with spectral density $S_{vx}(f)$, the transconductor G_{mx} injects its noise current $i_x = v_x G_{mx}$ into Node x_i. The spectral density $S_{ix}(f)$ of this current is given by, equation (2.57).

$$S_{ix}(f) = G_{mx}^2 S_{vx}(f) \tag{2.57}$$

The corresponding output noise voltage v_{ox} can be calculated as,

$$v_{ox} = i_x H_i = G_{mx} H_i v_x \tag{2.58}$$

where H_i is the current-to-voltage transfer function from Node x_i to the output of the filter. The corresponding spectral density $S_{vox}(f)$ is given by (2.59).

$$S_{vox}(f) = S_{ix}(f)\,|H_i(j2\pi f)|^2 = G_{mx}^2 S_{vx}(f)\,|H_i(j2\pi f)|^2 \tag{2.59}$$

Using expressions given in (2.37), it is easy to show that the transfer functions $H_j(s)$, j=1,2,…,n are components of the 1×n vector H_{cv} defined as,

$$\mathrm{H_{cv}}\left(\mathrm{s}\right)=\mathrm{C}\left(\mathrm{sT_C}-\mathrm{G}\right)^{-1} \tag{2.60}$$

If a non-trivial output summer is present (cf. Fig. 2.17) there is a need for the current-to-voltage transfer function also, which can expressed as,

$$\mathrm{H_0}=\mathrm{G_{mo}^{-1}} \tag{2.61}$$

from the output node to itself. Thus, each filter transconductor injects its noise current with spectral density (2.57) into one of the internal nodes of the filter (or directly into the output node if the filter has a nontrivial output summer). This current is then converted into the output noise voltage according to (2.59). To calculate the total output noise voltage of the filter the assumption of statistical independence of transconductor-noise sources, can be used and all the corresponding noise spectra can simply be added. In general, the outputs of one input transconductor G_{mbi}, and n transconductors G_{mij}, j=1,…,n, are connected to each internal node x_i. In the presence of a non-trivial output summer there is an additional output node, x_0, with outputs of transconductors G_{mj}, j = 1, …, n, G_{md}, and G_{mo}.

The auxiliary matrices can be defined as,

$$\begin{gathered}\mathrm{S_t}=\left[\mathrm{S_{t.ij}}\right]_{\mathrm{i,j=1}}^{\mathrm{n}},\ \mathrm{S_f}=\left[\mathrm{S_{f.ij}}\right]_{\mathrm{i,j=1}}^{\mathrm{n}},\ \mathrm{S_{tb}}=\left[\mathrm{S_{tb.1}}\quad\cdots\quad\mathrm{S_{tb.n}}\right]^{\mathrm{T}},\ \mathrm{S_{fb}}=\left[\mathrm{S_{fb.1}}\quad\cdots\quad\mathrm{S_{fb.n}}\right]^{\mathrm{T}}\\ \mathrm{S_{tc}}=\left[\mathrm{S_{tc.1}}\quad\cdots\quad\mathrm{S_{tc.n}}\right],\quad\mathrm{S_{fc}}=\left[\mathrm{S_{fc.1}}\quad\cdots\quad\mathrm{S_{fc.n}}\right]\\ \mathrm{S_{td}}=\mathrm{S_{td}},\quad\mathrm{S_{fd}}=\mathrm{S_{fd}},\quad\mathrm{S_{to}}=\mathrm{S_{to}},\quad\mathrm{S_{fo}}=\mathrm{S_{fo}}\end{gathered} \tag{2.62}$$

representing the thermal noise (subscript t) and flicker noise (subscript f) of transconductors G_{mij}, G_{mbi}, G_{mci}, G_{md}, and G_{mo}, respectively. To simplify the approach some simple notations are introduced in (2.63).

$$\begin{gathered}\overline{\mathrm{G}}=\left[\left|\,\mathrm{G_{mij}}\,\right|\right]_{\mathrm{i,j=1}}^{\mathrm{n}},\ \overline{\mathrm{B}}=\left[\left|\,\mathrm{G_{mb1}}\,\right|\quad\cdots\quad\left|\,\mathrm{G_{mbn}}\,\right|\right]^{\mathrm{T}},\\ \overline{\mathrm{C}}=\left[\left|\,\mathrm{G_{mc1}}\,\right|\quad\cdots\quad\left|\,\mathrm{G_{mcn}}\,\right|\right],\ \overline{\mathrm{D}}=\left|\,\mathrm{G_{md}}\,\right|,\ \overline{\mathrm{O}}=\left|\,\mathrm{G_{mo}}\,\right|\end{gathered} \tag{2.63}$$

Denote further by "∘" the Hadamard product [59] of two matrices, i.e., if $P=[p_{ij}]_{i,j=1}^{n}$ and $Q=[q_{ij}]_{i,j=1}^{n}$, we have $P\circ Q=[p_{ij}q_{ij}]_{i,j=1}^{n}$, and let $\hat{I}=\begin{bmatrix}1 & \cdots & 1\end{bmatrix}^{T}$ be an $n \times 1$ vector. The function $F(P,Q,R)(x)$ can be defined as shown in (2.64),

$$\mathrm{F}(\mathrm{P},\mathrm{Q},\mathrm{R})(\mathrm{x})=\mathrm{P}\circ\left[\mathrm{Q}+(2\pi/\mathrm{x})\,\mathrm{P}\circ\mathrm{R}\right] \tag{2.64}$$

where P, Q, and R are matrices of the same dimension and x is a real variable. It follows from (2.52) and (2.57), that the spectral densities, $S_i(\omega)$, of the total noise current injected into the nodes x_i, $i = 1, \ldots, n$, can be expressed, using (2.64), as components of the current spectral-density vector S, given by

$$\mathrm{S}(\omega)=\left[\mathrm{S}_1(\omega)\quad\cdots\quad\mathrm{S}_n(\omega)\right]^{\mathrm{T}}=\mathrm{F}(\bar{\mathrm{G}},\mathrm{S}_t,\mathrm{S}_f)(\omega)\cdot\hat{\mathrm{I}}+\mathrm{F}(\bar{\mathrm{B}},\mathrm{S}_{tb},\mathrm{S}_{fb})(\omega) \tag{2.65}$$

Analogously, if there is a non-trivial output summer, the spectral density $S_0(\omega)$ of the noise current injected into Node x_0 is given by (2.66),

$$\mathrm{S}_0(\omega)=\mathrm{F}(\bar{\mathrm{C}},\mathrm{S}_{tc},\mathrm{S}_{fc})(\omega)\cdot\hat{\mathrm{I}}+\mathrm{F}(\bar{\mathrm{D}},\mathrm{S}_{td},\mathrm{S}_{fd})(\omega)+\mathrm{F}(\bar{\mathrm{O}},\mathrm{S}_{to},\mathrm{S}_{fo})(\omega) \tag{2.66}$$

The spectral density $S_{no}(\omega)$ of the total output-noise voltage v_{no} can then be calculated as shown in (2.67).

$$\mathrm{S}_{no}(\omega)=|\mathrm{H}_{cv}(\omega)|^2\,\mathrm{S}(\omega)+\mathrm{H}_0^2\mathrm{S}_0(\omega) \tag{2.67}$$

here $|H_{cv}(\omega)|^2=H_{cv}(j\omega)\circ H_{cv}(-j\omega)$, with H_{cv} and H_0 given by (2.60) and (2.61) respectively. In general, $S_0(\omega)$ is a rational function of ω with numerator and denominator of order not larger than $2n+1$. Equation (2.33), permits the output-noise spectrum of any OTA-*C* filter to be calculated; the output-noise voltage is then obtained by integrating (2.67) over a suitable frequency range. The equivalent input-noise spectrum $S_{ni}(\omega)$ can be obtained by dividing (2.67) by the squared magnitude of a filter's transfer function (from (2.37)) we have $H(s)=C(sT_C-G)B+D$). If there is no output summer in the filter, this leads to simplified formulas because the determinant of sT_C–G cancels. It is also worth noting that the matrix formulation makes implementing the presented expressions in a computer program particularly convenient, which permits the noise analysis of arbitrary OTA-*C* filters to be carried out automatically.

In practice, frequently all filter transconductors are identical, that is, $S_{t.ij} = S_t$, $S_{f.ij} = S_f$, $i, j = 1, \ldots, n$, $S_{tb.i} = S_{tc.i} = S_t$, $S_{fb.i} = S_{fc.i} = S_f$, $i = 1, \ldots, n$, $S_{td} = S_{to} = S_t$, $S_{fd} = S_{fo} = S_f$ (cf. (2.62)), where S_t and S_f are the noise parameters of the transconductors. Then, (2.65) and (2.66) take the form,

$$S(\omega) = \left(\bar{G}\hat{I} + \bar{B}\right)S_t + \frac{2\pi}{\omega}\left(\bar{G} \circ \bar{G}\hat{I} + \bar{B} \circ \bar{B}\right)S_f \tag{2.68}$$

$$S_0(\omega) = \left(\bar{C}\hat{I} + \bar{D} + \bar{O}\right)S_t + \frac{2\pi}{\omega}\left(\bar{C} \circ \bar{C}\hat{I} + \bar{D} \circ \bar{D} + \bar{O} \circ \bar{O}\right)S_f \tag{2.69}$$

Hence the approach presented in this thesis can be used to model the noise and non-linearity for any general order OTA-C filter. The following sections verifies the approach using some example circuits.

2.2.4. Verification of the Nonlinearity and Noise Analysis Tool

In order to verify the accuracy of the proposed approach, comparisons between theoretical results and SPICE simulations have been carried out. The numerical results have been obtained using 4th order Adams-Bashforth's [74] method to integrate differential equation (2.49) and three-point composite Newton-Cotes quadrature [74] to calculate coefficients h_n in (2.51).

For the first comparison a simple differential-pair transconductor as in Fig. 2.22 is considered. The circuit is implemented in standard 0.35μm AMS technology and simulated using SPICE. The OTA macromodel parameters extracted from the DC simulations are given by the general expression of the voltage to current (input/ output) relationship as shown in (2.70).

$$\begin{aligned} i_{out}(v_{id}) &= g_m v_{id} + g_{m3}(v_{id})^3 + g_{m5}(v_{id})^5 \\ &= 10^{-4} v_{id} - 4.2\times10^{-5}(v_{id})^3 - 3.4\times10^{-5}(v_{id})^5 \end{aligned} \tag{2.70}$$

where v_{id} in volts; accuracy of the series better than 0.1% for v_{id}<0.75V. The transconductance of the differential pair was designed to be g_m=100μA/V. The noise parameters from the noise simulations in SPICE were found to be S_t=5.2·10^{-16} V·A/Hz and S_f=2.3·10^{-10} V^2.

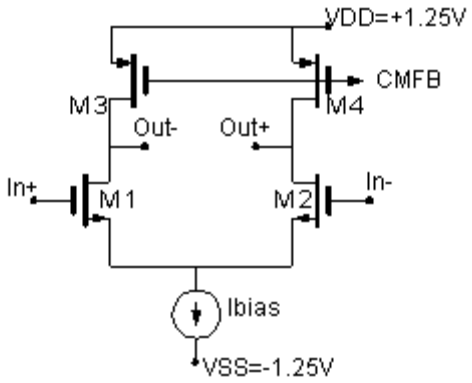


Fig. 2.22. Simple differential pair

The OTA circuit in Fig. 2.22 was used to implement the 3rd order Butterworth low-pass filter in a leap-frog (LF) structure shown in Fig. 2.23 (actual filter was implemented in fully differential structure). The total capacitor elemental values are: C_1=2.37pF, C_2=2.11pF, C_3=0.79pF. The OTAs in Fig. 2.22 was used as active elements of the filter. The 3dB frequency of the filter was designed to be 10MHz. Using the approach introduced in sections 2.2.3 and 2.2.4, the noise and non-linearity performances of the filter were simulated. The theoretical values predicted by the model were verified against those of the simulated ones. The THD vs. Input signal Frequency (Fig. 2.24) THD vs. Input signal amplitude (Fig. 2.25) and the output noise spectrum were compared and plotted (Fig. 2.26).

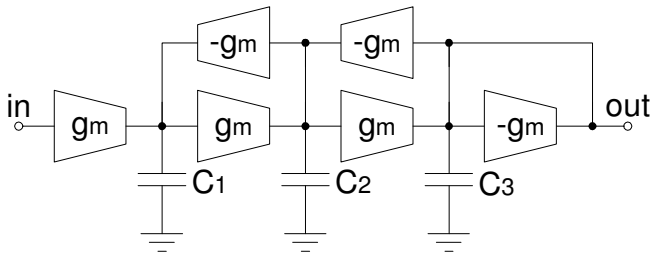


Fig. 2.23. 3rd order Butterworth low pass filter (leap frog structure)

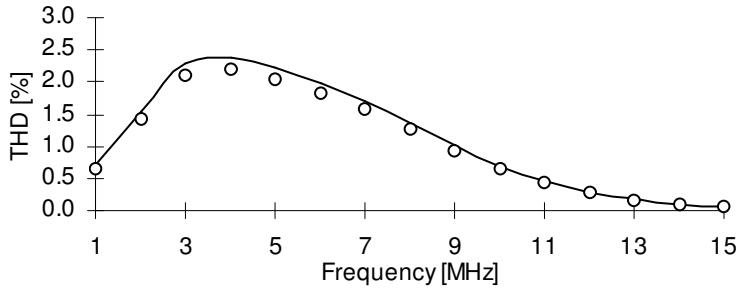


Fig. 2.24. THD vs. frequency for 3rd order low pass filter in Fig. 2.23 with 0.3V input amplitude: theoretical data (line), and simulation (points)

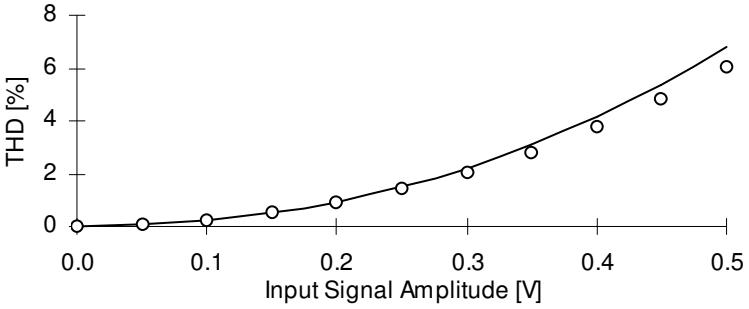


Fig. 2.25. THD vs. input signal amplitude for 3rd low pass filter in Fig. 2.23 with 5MHz sine wave: theoretical data (line), and simulation (points)

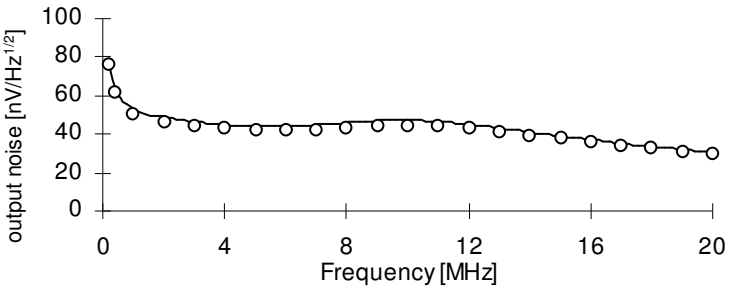


Fig. 2.26. Output noise spectrum vs. frequency for 3rd low pass filter in Fig. 2.23: theoretical data (line), and simulation (points)

From the above plots it can be verified that the simulated values are in accordance with those of the theoretically modeled values. This is a simple example using a simple differential pair to prove the concept. Example 2 is a more intense and complex structure and the comparisons also include the experimental measurements of the filter characteristics.

To validate the approach more intensely a comparison between the theoretical results with the SPICE simulated ones and also experimental results were carried out. The second example to validate the approach is the design of a 5th order Bessel Low Pass filter with a 3dB frequency of 10MHz. A 5th order filter can be designed in several possible topologies. A simple permutation and combination result yields 50 possible structures, which includes cascade (a first order followed by two biquads, a biquad and a 3rd order section etc.), leap-frog, follow the leader feedback and multi feedback loop. The best topology needs to be selected depending on the application. A particular structure might be very good with respect to its linearity performance, one structure for the noise etc. The modeling process proposed in this thesis can be used to determine the best topology of the OTA-C filter for a particular performance metric.

The OTA structure used for this example is shown in Fig. 2.27 [75]. The OTA is a Pseudo Differential OTA with inherent common mode feedforward and feedback. The principle of source degeneration is used in this technique. It is based on a fully balanced

fully symmetric circuit design. Source degeneration is used to increase the linearity of the OTA. Transistors M5 in the OTA operates in the triode region and these transistors introduces the source degeneration necessary to improve the linearity of the OTA. The bias voltage V_{bias} is used to tune the circuit. The biasing voltage controls the amount of source degeneration introduced. This controls the effective transconductance term and hence the frequency response.

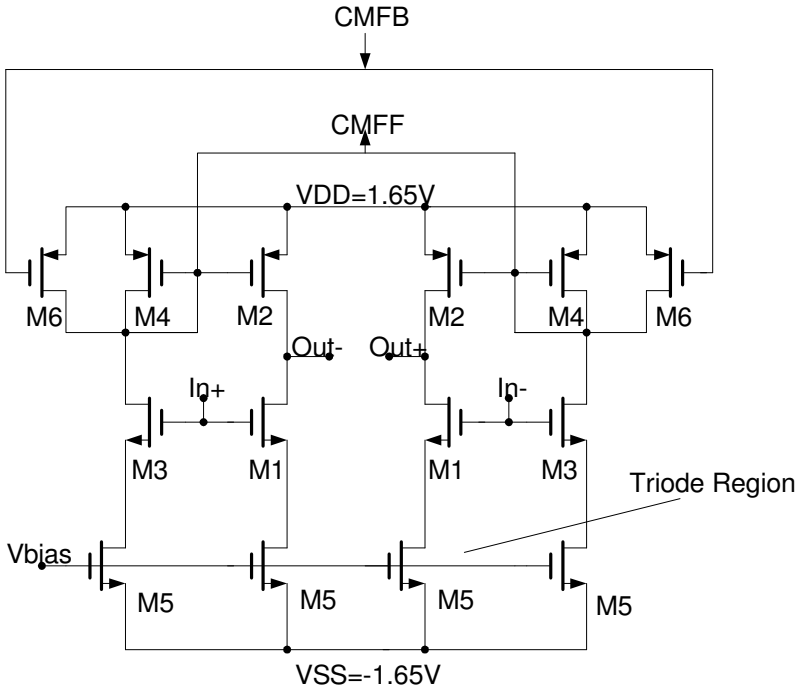


Fig. 2.27. Fully balanced fully symmetric pseudo differential OTA* [75]

The transconductance terms (first order and the higher order terms), similar to the equation (2.70), can be extracted from the DC characteristics of the OTA. The DC characteristics, i.e. the Output current vs. Input voltage, can be used to determine the

* © 2003 IEEE. Reprinted, with permission, from ,"An enhanced adaptive Q tuning scheme for a 100MHz fully symmetric OTA based band pass filter", P. Kallam, E. Sánchez-Sinencio and A. Karsilayan, *IEEE J. Solid-State Circuits*, vol. 38, pp. 585-593, 2003.

coefficients of the nonlinear terms, which includes the basic transconductance term (g_m), and the higher order terms. The transconductance of the OTA designed is 345μA/V. All OTA used in the filter have the same value of transconductance. Table 2.3 gives the design parameters of the OTA used in this example.

Table 2.3. Parameters for OTA Used in the 5th Order Bessel Filter [75]

Parameter	Value
g_{m1}	345 μA/V
g_{m3}	-9.084 μA/V^3
g_{m5}	-0.44 μA/V^5
S_w	8.17x10^{-20} VA/Hz
S_f	0
$(W/L)_{M1,M3}$	10.2/0.6 (μm)
$(W/L)_{M5}$	5/0.6 (μm)
$(W/L)_{M2}$	54/2 (μm)
$(W/L)_{M4,M6}$	27/2 (μm)
Vbias	1 V
$V_{DD,}$-Vss	1.65 V
Technology	CMOS 0.5μm

The noise parameters S_t and S_f are determined from the SPICE simulations of the OTA in CADENCE. The noise parameters can be estimated from the input referred noise simulated result of the stand alone OTA using the formulae given in equations (2.71) and (2.72),

$$S_t = g_m \times \left(\frac{f_1 S_{N1} - f_2 S_{N2}}{f_1 - f_2} \right) \quad \text{V.A/Hz} \tag{2.71}$$

$$S_f = \frac{(S_{N1} - S_{N2}) f_1 f_2}{f_2 - f_1}, \quad V^2 \tag{2.72}$$

where f_1 and f_2 are two selected frequencies where the noise spectral densities S_N are measured. Appendix A describes the method of extracting the nonlinear higher order coefficients and also the noise parameters.

A MATLAB code was written based on the modeling tool. This was done to create an user friendly tool which can be handled easily. The software takes in the inputs as the DC characteristic of the OTA for some 100 points and the noise parameters. For this example the value of transconductance g_m= 345μA/V and the values of S_t and S_f were 8.1705e^{-20} VA/Hz and 0 respectively. The value of S_f is taken to be 0, as the 3dB frequency is around 10MHz and the low frequency noise components due to the *1/f* noise can be considered as negligible. Along with these the tool also takes the capacitor arrangement for the Bessel approximation and the *T* matrix for the given filter for all 50 combinations.

The modeling tool compares the performance of all 50 structures and gives the overall performance chart as shown in Fig. 2.28. The x-axis represents the structure number (1-24 includes all combinations of leap-frog, feedback structures like the follow the leader feedback, multi feedback structures, 25-50 the various cascade combinations). From Fig. 2.28 the optimum filter structure for better linearity and better noise performance is structure numbered 45, which is a form of the cascade structure where two biquads is followed by a first order section. The structures numbered 1-6, which are the leap frog implementations are the best structures for noise. Based on the results derived from Fig. 2.28, two structures of the 5th order low pass Bessel filter was implemented, the cascade filter (2:2:1, two cascade sections followed by a first order stage, Number 45) and the leap frog structure (Number 1).

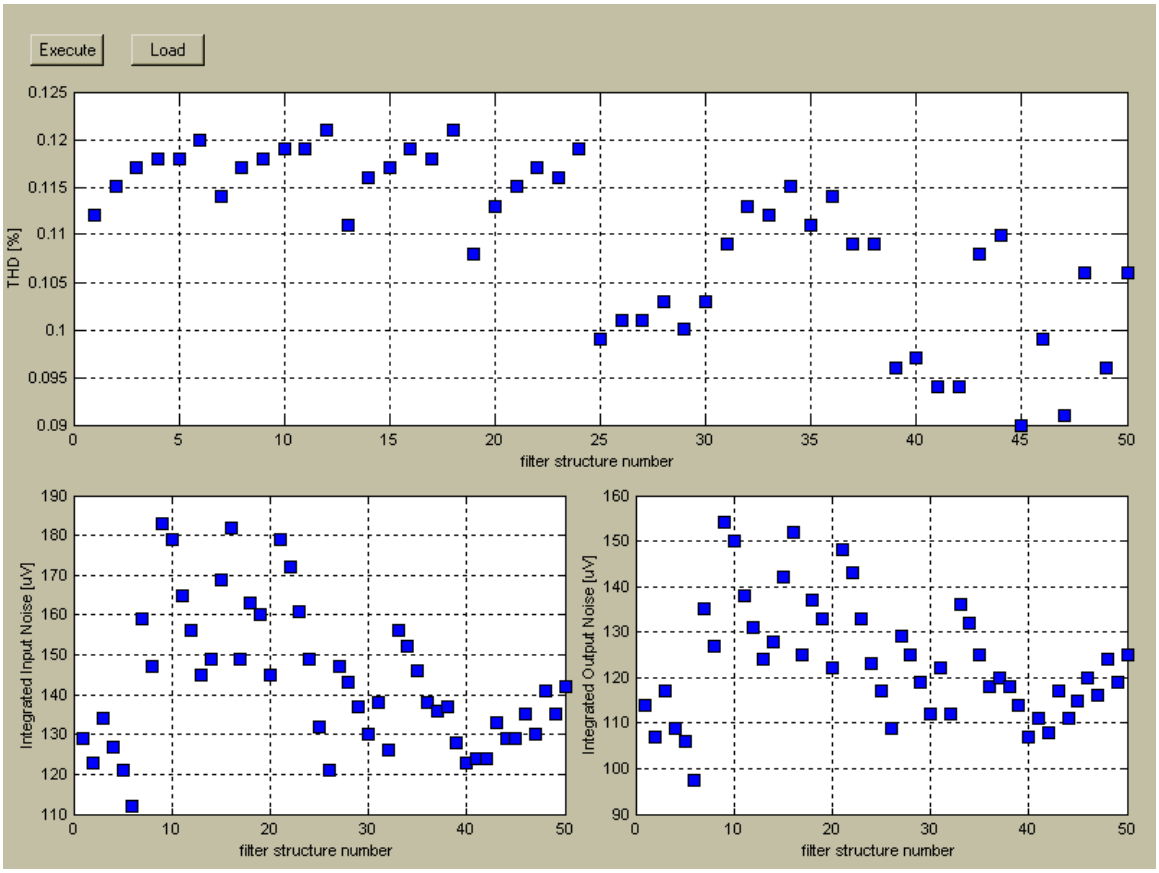


Fig. 2.28. Output window of the modeling tool showing the performance of the various structures for THD and noise

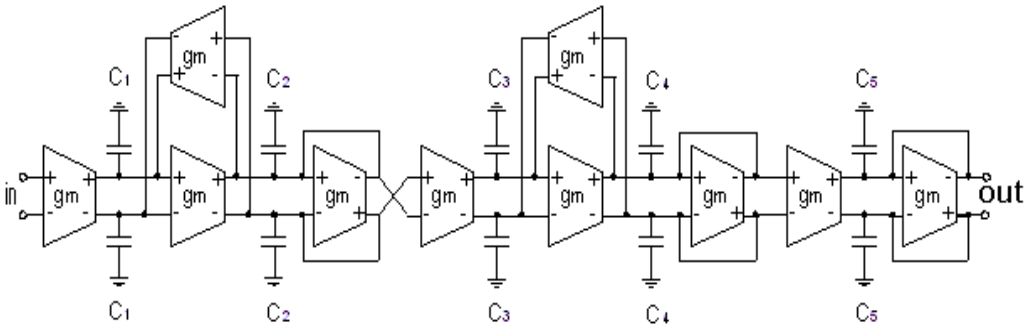


Fig. 2.29. Cascade structure for the 5th order Bessel filter (2:2:1)

Fig. 2.29 shows the cascade implementation of the 5th order Bessel low pass filter whose 3dB frequency is 10MHz. Each active block is the OTA shown in Fig. 2.27. The capacitor elemental values are C_1=2.79pF, C_2=2.34pF, C_3=5.11pF, C_4=1.625pF and C_5=2.98pF. These values are estimated based on the frequency response and also the Bessel approximation. The filter was designed in 0.5µm technology and also fabricated using AMI processes. The theoretical results of *THD* vs. frequency, input signal amplitude and noise vs. frequency are compared with those of the simulated and the experimental measurements made on Silicon.

Fig. 2.30 shows the set-up for the measurement of the filter transfer function. The Agilent 4395A (Spectrum/Network Analyzer) can be used as a network analyzer to measure the filter's transfer function. Using the network analyzer the filters transfer function and also the group delay performance can be measured.

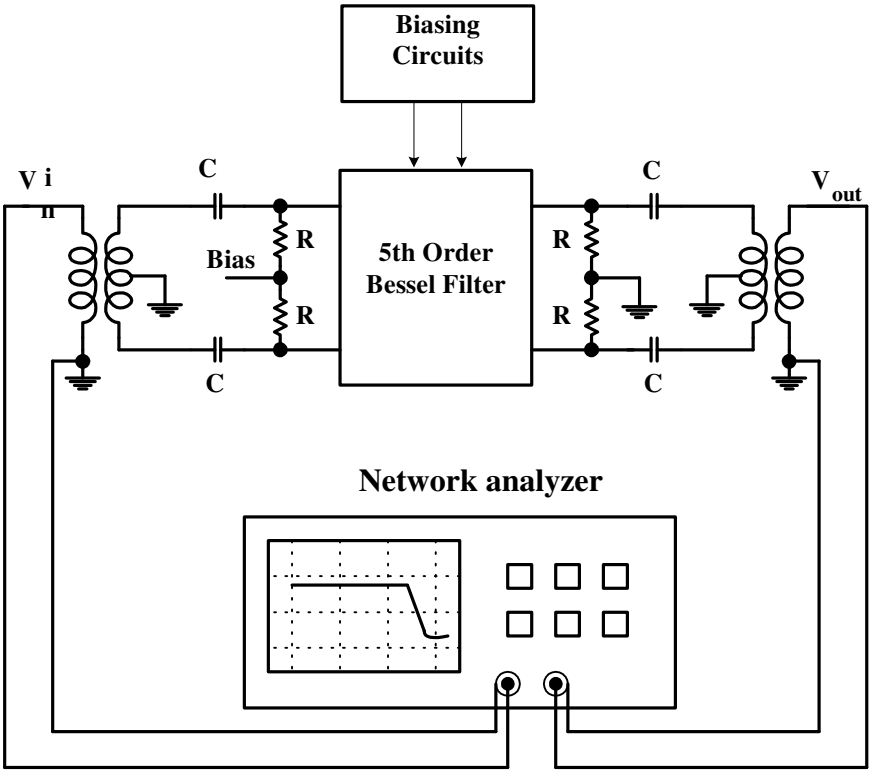


Fig. 2.30. Set-up for transfer function measurements

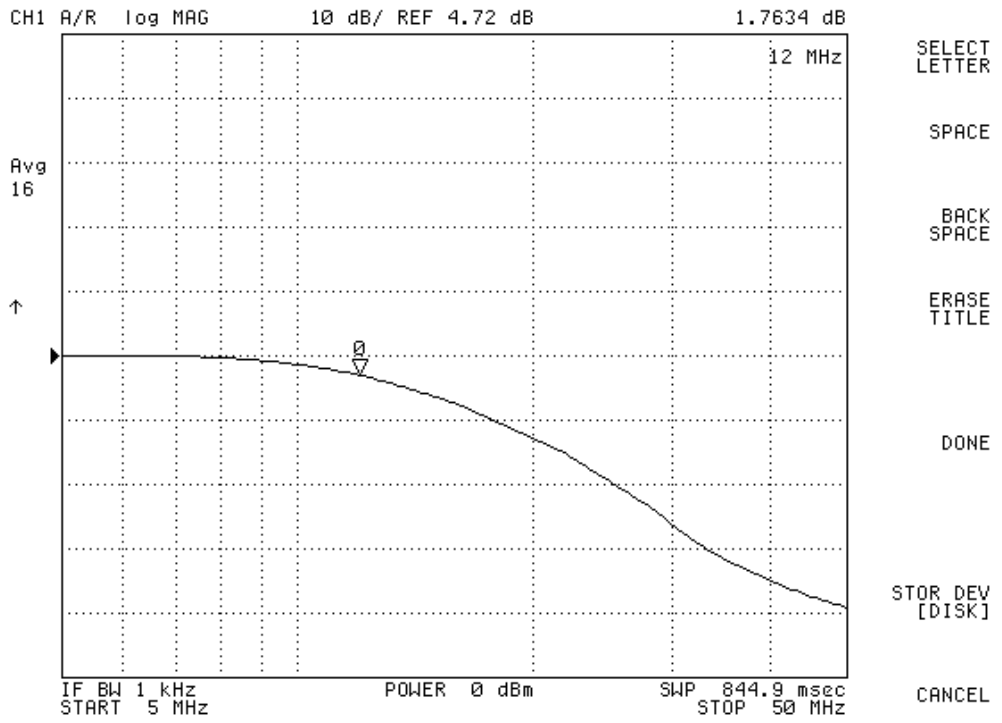


Fig. 2.31 Filter transfer function for the 5th order Bessel low pass filter –cascade structure using OTA shown in Fig. 2.27 [75]

Fig. 2.31 shows the transfer function of the 5th order Bessel filter built using the cascade topology (2:2:1) based on the OTA shown in Fig. 2.27. The 3dB frequency is around 12MHz. The corner frequency can be tuned to 10MHz using the *Vbias* voltage.

Fig. 2.32 shows the general set up to measure the IM_3 products. To measure linearity experimentally a two-tone analysis is used. Two signals of equal amplitude but different frequencies are generated using the signal generators and are combined together using the combiner and are fed to the OTA based filter (5th order Bessel Filter). The output waveforms are plotted and from the third order intermodulation products terms the third order Harmonic Distortion (HD_3) can be extracted. It is known that the

IM_3 is thrice that of the third order harmonics. The higher order harmonics can be neglected for analysis.

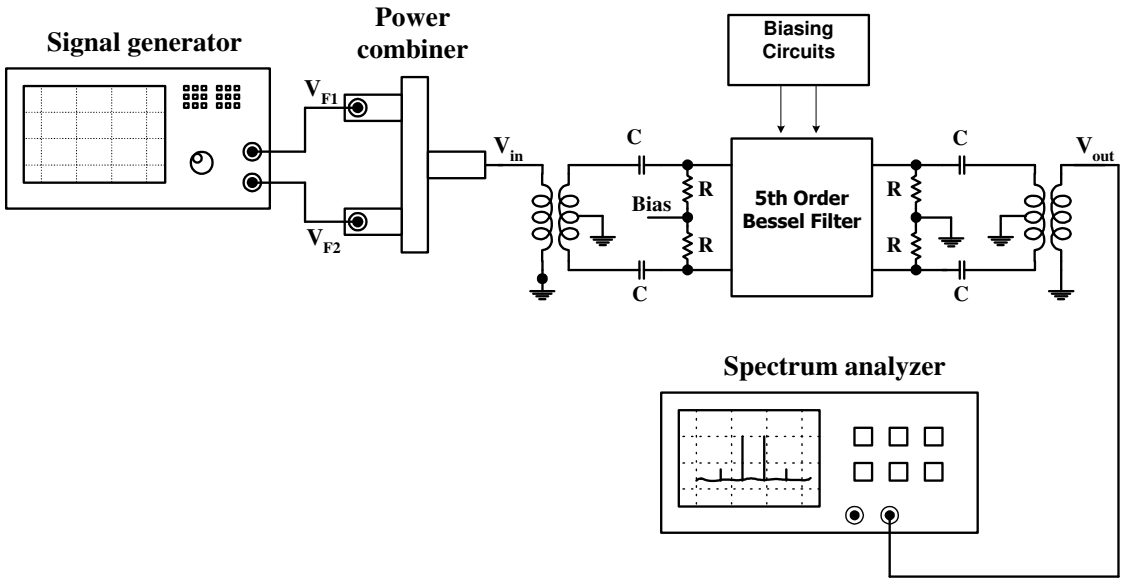


Fig. 2.32. Set-up to measure intermodulation distortion using the spectrum analyzer

Fig. 2.33 shows one of the experimental results for the measurement of IM_3 (intermodulation products). The IM_3 results for two equal tones at 10MHz and 11MHz with amplitudes of 0.5V is shown. The IM_3 value measured is -53dB. The HD_3 can be estimated from the IM_3. The third harmonic distortion parameter is taken into consideration cause the measurement results gives an accurate value of the the third order intermodulation products and from which the HD_3 can be estimated.

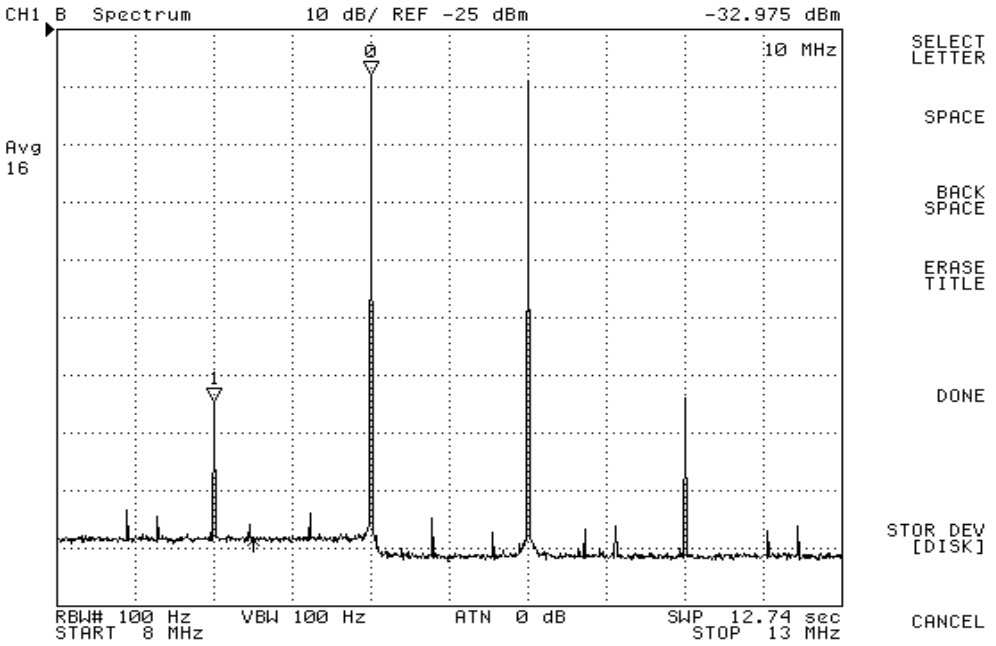


Fig. 2.33. Two tone measurement results for IM3 at 10MHz and 11MHz for a 0.5V input amplitude for the 5th order Bessel filter

Fig. 2.34 shows the HD_3 vs. input signal amplitude for an input 10MHz sine wave. This frequency is around the corner frequency of the filter. The theoretical data produced from the modeling tool is compared against those of the simulated values (CADENCE is used for the simulations of the post layout design) and the experimental data produced from the measurement of the 5th order Bessel Filter.

The maximum error between the theoretical and measured value is around 25% which is around the maximum amplitude value. The maximum error between the theoretical and simulated value is around 9% when the amplitude is 0.5V.

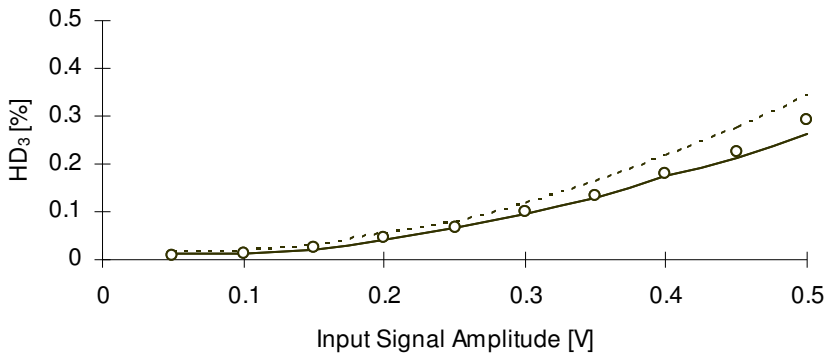


Fig. 2.34. HD_3 vs. input signal amplitude for filter in Fig.2. 29 with 10MHz sine wave: theoretical data (solid line), SPICE simulation (points), and experimental measurements (dashed line)

Fig. 2.35 shows that the theoretical model results predicted (solid line) matches very well with those of the simulated ones (points) and the experimental data (dashed line). The OTA used for the design of the filter is shown in Fig. 2.27.

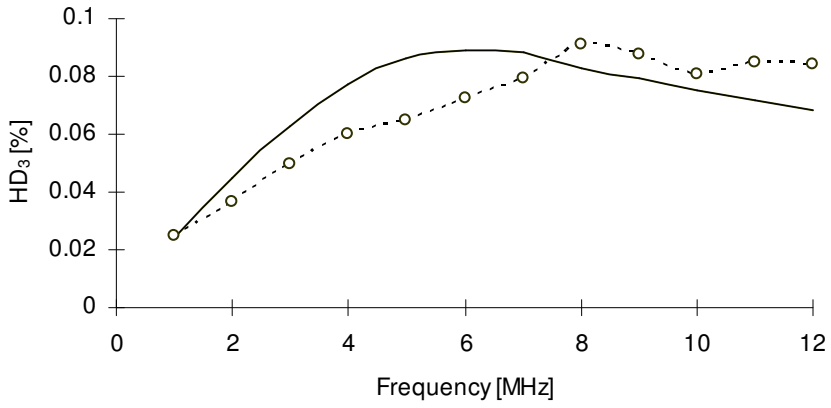


Fig. 2.35. HD_3 vs. input signal frequency for filter in Fig. 2.29. for an input signal amplitude of 0.25 V: theoretical (solid line), experimental (dashed line)

Fig. 2.35 shows the HD_3 vs. Frequency for an input signal amplitude of 0.25V. The theoretical results (solid line) matches those of the experimental results (dashed line) for most of the low frequency components. There is a slight variation in the results above the 3dB frequency (10MHz). The reason for this variation needs to be investigated.

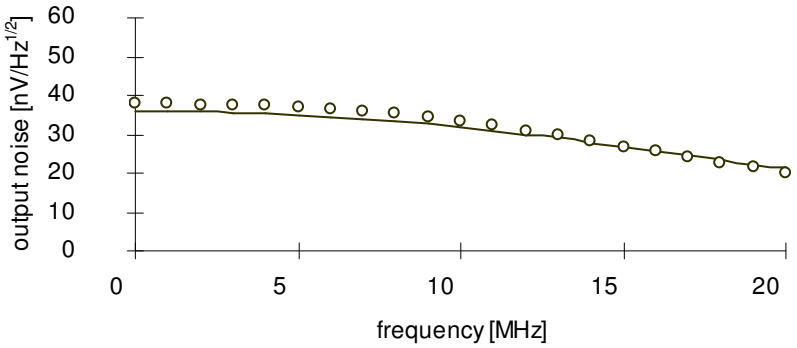


Fig. 2.36. Output noise spectrum vs. frequency for filter in Fig. 2.29: theoretical data (solid line), and Spice simulation (points)

Fig. 2.36 shows the output noise spectrum for the filter. The theoretical data (solid lines) matches perfectly with those of the simulated results from the post-layout design. The post-layout design was used to compare cause the experimental data would be a complex one for the output noise spectrum vs. frequency. Fig. 2.37 shows the chip microphotograph of the 5th order Bessel filter in cascade topology. The capacitor bank is also shown.

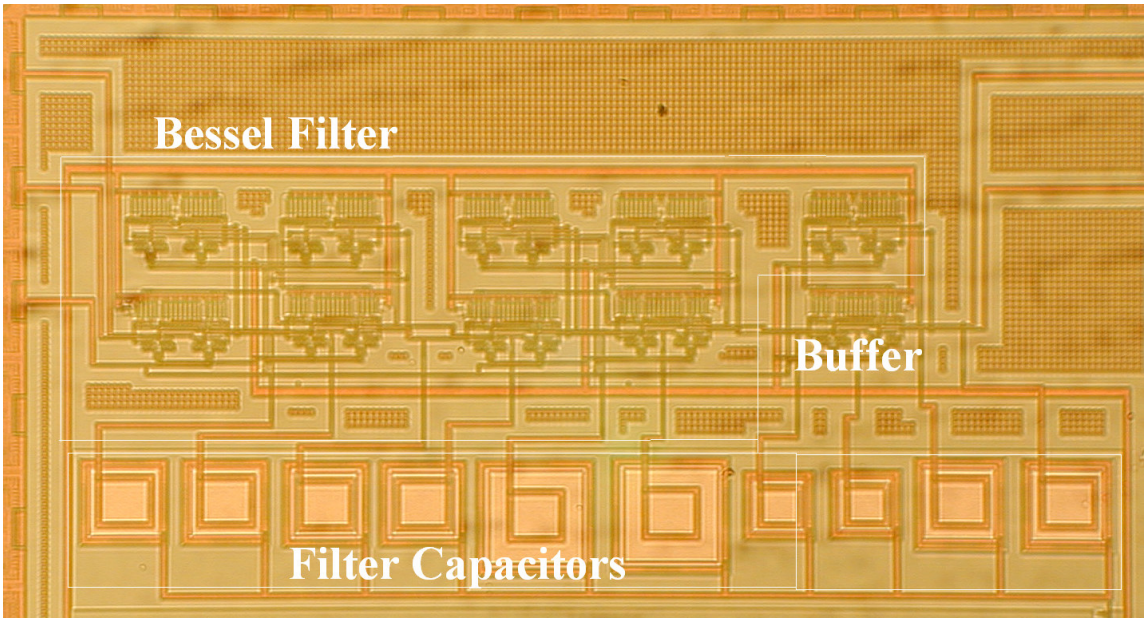


Fig. 2.37. Micro photograph of the 5th order Bessel low pass filter (cascade)

The main advantages of this approach can be seen from two perspectives (1) The CAD person's perspective and (2) The designer's perspective. This approach can be used to do a very fast computation of various filter topologies irrespective of the order of the filter in one go. The various parameters like noise and non-linearity are all combined into one program. The other important parameters like power, area and the sensitivity analysis need to be done. They will serve as some of the trade-offs when choosing the best structure. This approach mainly focuses on the linearity and noise optimization. The same matrix description can also be used to do the sensitivity analysis, which is very well described in the literature [50]. A designer would consider all the trade-offs and also the best results for noise and linearity and choose the best structure. To prove the advantage of this approach a simple analysis of the best and worst case structures with respect to noise and linearity is summarized in Table 2.4.

Table 2.4. Performance Comparisons Among the Structures for the 5th Order Bessel Filter

Parameter/ Structure	Cascade (45)	Leapfrog (1)	Multiple Feedback(12)
HD_3 for $0.5V_{in,amp}$ at 10MHz	-49.37 dB	-44.364 dB	-41.8 dB
Output Integrated Noise	87.5μVrms	91μVrms	130μVrms

From the results presented in Table 2.4, this approach can be used to improve the performance by 8dB for the case of linearity improvement and also the noise performance can be improved by 32% approximately. The other factors like power, area, complexity of the design, amount of parasitics introduced, sensitivity of the circuit needs to be considered before the overall decision is made. For applications where the noise and linearity performances are the critical issues, this approach would serve as a very good tool to optimize the design. A specific case of optimization is explained in detail in the next section.

2.2.5. Performance Optimization of OTA-C Filters

The nonlinear distortion and noise evaluation tools presented in Sections 2.2.2 and 2.2.3 are well suited to be used in computer-aided design and optimization of OTA-C filters. The optimization methodology, which takes advantage of the matrix description of the OTA-C filter model in Fig. 2.17, is presented in this section.

Let P and Q be two diagonal $n\times n$ matrices with positive elements, i.e

$$P=diag\{p_1,...,p_n\},\ \ Q=diag\{q_1,...,q_n\} \tag{2.73}$$

also assume that the matrix T is diagonal (i.e. the filter contains only grounded capacitors). Then the transfer function formula (linear case) can be rewritten as shown in (2.74).

$$\begin{aligned} \mathrm{H}(\mathrm{s}) &= \mathrm{C}(\mathrm{sT}-\mathrm{G})^{-1}\mathrm{B}+\mathrm{D} = \mathrm{CPP}^{-1}(\mathrm{sT}-\mathrm{G})^{-1}\mathrm{Q}^{-1}\mathrm{QB}+\mathrm{D} \\ &= \mathrm{CP}(\mathrm{sQTP}-\mathrm{QGP})^{-1}\mathrm{QB}+\mathrm{D} \end{aligned} \tag{2.74}$$

The following matrices can be defined such that it facilitates the optimization theoretical derivation,

$$\overline{\mathrm{T}}=\mathrm{QTP},\ \overline{\mathrm{G}}=\mathrm{QGP},\ \overline{\mathrm{C}}=\mathrm{CP},\ \overline{\mathrm{B}}=\mathrm{QB},\ \overline{\mathrm{D}}=\mathrm{D} \tag{2.75}$$

It is seen from (2.74) that the equivalence transformation of (2.75) leads to the matrices $\overline{T}$, $\overline{G}$, $\overline{C}$, $\overline{B}$ and $\overline{D}$, and they define a new filter, which has the same topology and transfer function but different (re-scaled) element values, and, usually, different performance parameters.

Note also that Q, P and T need not be diagonal, however, they cannot be arbitrary invertible matrices as well, because matrix $\overline{T}$ obtained as a result of transformation (2.75) has to be symmetric, positively definite with positive diagonal and non-positive non-diagonal entries in order to define an OTA-C filter. In particular, if P and Q are diagonal but T is general then matrices P and Q have to satisfy the condition $p_iq_j=p_jq_i$ whenever $i\neq j$ and $T_{ij}\neq 0$. For diagonal T, i.e. for the filter with only grounded capacitors the above condition is satisfied automatically so P and Q are independent.

The task is now to find the matrices P and Q so that the filter performance parameter(s) of interest is(are) optimized. A clear and definite optimization procedure is presented below.

(1) Take an initial realization of the transfer function $H(s)$ given by the set of matrices T, G, B, C and D.

(2) Use the matrix elements of P and Q, i.e. $p_1,...,p_n$, $q_1,...,q_n$, as optimization variables and optimize the target function $F=F(T,G,B,C,D;P,Q)$, which may be dynamic range, integrated noise, THD, etc.

Usually, there are some design constraints such as the maximum value of total capacitance of the filter, maximum power consumption of the filter which depends on transconductance value, allowable capacitance ratio, i.e. the ratio of maximum to minimum capacitance values in the filter, and so on. Some or all of these constraints have to be taken into account in the optimization process. In general, constraints can be written as follows

$$m_j \le c_j(T,G,B,C,D;P,Q) \le M_j,\ j=1,...,N_c \tag{2.76}$$

where N_c is the number of constraints, c_j is the j constraint function (e.g. total capacitance of the filter) which is dependent on matrices describing the filter and optimization variables, while m_j and M_j are minimum and maximum values of c_j (which may be finite or infinite).

The optimization itself can be carried out using any available numerical procedure embedded into the optimization system. Choice of the optimization procedure depends on the complexity of the problem and constraints.

For the rest of this section a representative example, performance optimization of OTA-C filters in cascade realization, is presented. The problem is to find the optimal pole-zero pairing, optimal cascading sequence, and optimal gain distribution so that the parameter of interest is optimized. There is a rich literature ([76]-[81]) discussing that problem and its solutions (usually quite complex procedures which are impracticable for high-order filters, or just rules of thumb) in more or less general setting and usually for some specific performance parameters. In practice, the only way to find truly optimal

solution of the general problem is exhaustive search through all possible cascade sequencing and performing parameter optimization for each of them. Fortunately, using the procedures described in the previous sections the optimization process is affordable because these tools are very fast.

For the sake of illustration, consider performance optimization of the 8th order Butterworth filter in cascade realization (Fig. 2.38) with biquads shown in Fig. 2.39. In the optimization process two degrees of freedom are assumed. The first one is biquad sequencing (which is equivalent to pole-zero pairing for Butterworth filter is an all-pole one). The second are biquad gains, which will be denoted as K_i, i=1,2,3,4. Gains are adjusted by changing transconductance g_b of input transconductor; the value of transconductance g_m=100μA/V is fixed; $g_b \in$ [70.7μA/V,141.4μA/V], which allows K_i to vary in the range $[2^{-1/2},2^{1/2}]$ ([-3dB,+3dB]). It is assumed that whole filter is set to unity gain, i.e. ($K_1+K_2+K_3+K_4$=1 V/V, 0dB if all K_i are in dB).

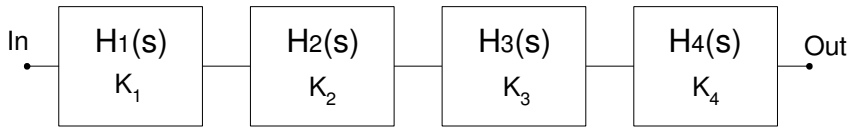


Fig. 2.38. Block diagram of 8th order cascade filter ($K_i=H_i(0)$)

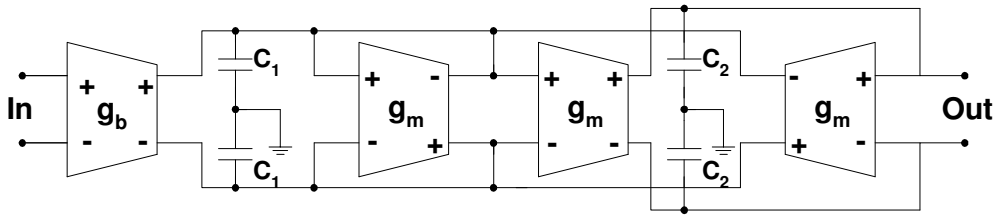


Fig. 2.39. Fully differential biquad used in the filter of Fig. 2.38

In terms of the general OTA-C filter model, the matrices corresponding to the filter in Fig. 2.38 are given in (2.77) and (2.78), where 0_2 is a 2*2 matrix.

$$G = \begin{bmatrix} G_1 & 0_2 & 0_2 & 0_2 \\ G_2 & G_1 & 0_2 & 0_2 \\ 0_2 & G_2 & G_1 & 0_2 \\ 0_2 & 0_2 & G_2 & G_1 \end{bmatrix} \tag{2.77}$$

$$G_1 = \begin{bmatrix} -g_m & -g_m \\ g_m & 0 \end{bmatrix},\ G_2 = \begin{bmatrix} 0 & g_m \\ 0 & 0 \end{bmatrix} \tag{2.78}$$

The matrices *T, C, B* and *D* are defined in (2.79).

$$T=\mathrm{diag}\{C_{11}, C_{12}, C_{21}, C_{22}, C_{31}, C_{32}, C_{41}, C_{42}\} \tag{2.79}$$
$$B=[g_m\ 0\ \ldots\ 0]^T,\ C=[0\ \ldots\ 0\ 1],\ D=0$$

where the first index of elements of matrix *T* refers to the biquad number (e.g. C_{i1} is C_1 in biquad H_i and so on). The initial value of input tranconductance g_b is equal to g_m for each biquad, this is an assumption. Setting gains as above is equivalent to using the transforms (2.75) with *P*, *Q* as in equation (2.73) with $q_1=q_2=K_1$, $q_3=q_4=K_1K_2$, $q_5=q_6=K_1K_2K_3$, $q_7=q_8=1$, and $p_i=1/q_i$, $i=1,...,8$. Thus, this is a constrained optimization problem with three independent variables.

Permutation of filter blocks is realized by permutation of corresponding elements of the matrix *T*. Original block sequencing: 1234 corresponds to original location of elements, i.e. $\{C_{11},C_{12},C_{21},C_{22},C_{31},C_{32},C_{41},C_{42}\}$. Any other permutation, e.g. *klpq* is given by $\{C_{k1},C_{k2},C_{l1},C_{l2},C_{p1},C_{p2},C_{q1},C_{q2}\}$.

To elaborate the optimization process three variants of OTA topologies were considered for the filter design. Variant I with differential pair transconductors (Fig. 2.40) implemented in standard 0.35μm CMOS process, variant II with linearized OTAs [75] (Fig. 2.41) implemented in 0.35μm technology, and variant III with linearized OTAs [78] (Fig. 2.42) implemented in 0.5μm. The 3dB cutoff frequency of the filter equals 8MHz for all variants. Capacitance values are: C_{11}=0.51pF, C_{12}=1.96pF, C_{21}=0.60pF, C_{22}=1.66pF, C_{31}=0.90pF, C_{32}=1.11pF, C_{41}=2.56pF, C_{42}=0.39pF.

Optimization was carried out using the software written in C, implementing both nonlinearity and noise evaluation procedures of Sections 2.2.3 and 2.2.4, and numerical optimization routines. OTA nonlinearity was represented, for the purpose of solving

equation (2.49), by spline interpolation of its tabularized transfer function. Both nonlinearity and noise parameters of transconductors depend on linear transconductance, which was modeled using polynomial approximation of appropriate coefficients.

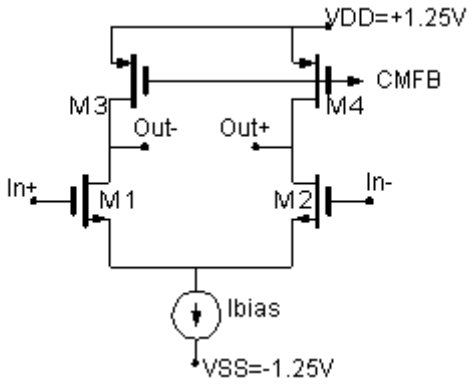


Fig. 2.40. Variant I- simple differential pair

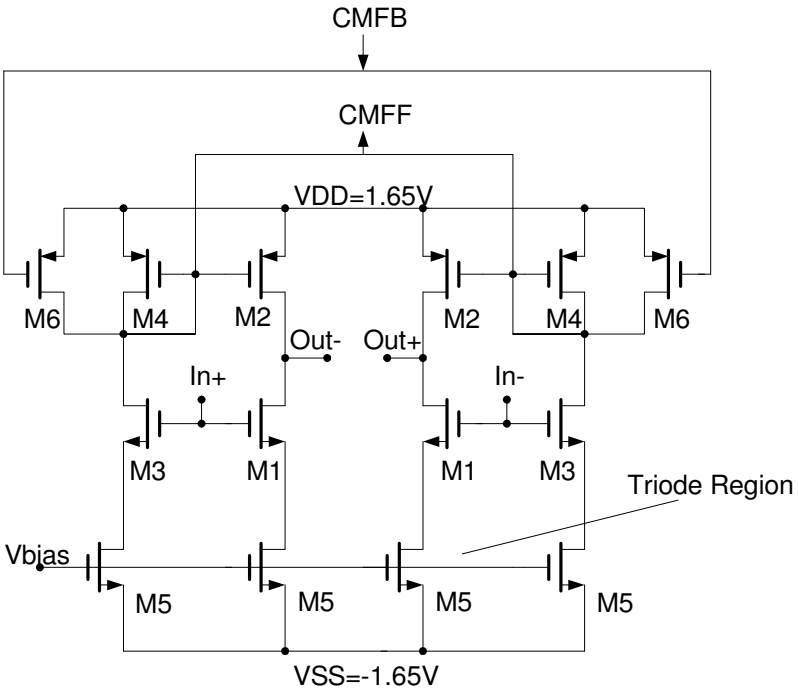


Fig. 2.41. Variant II – linearized OTA [75]

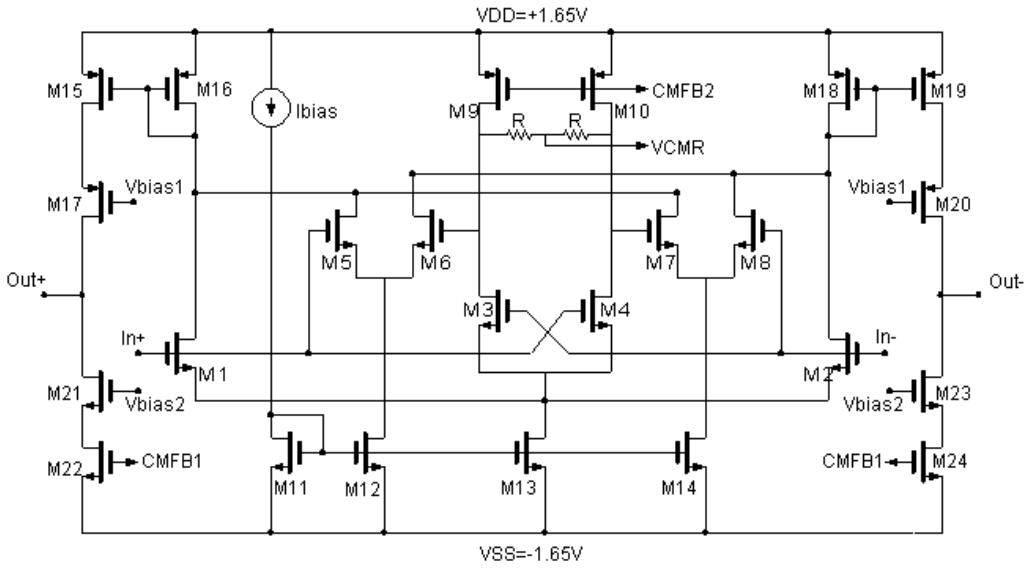


Fig. 2.42. Variant III- linearized OTA [78]

Optimization was carried out three times, each time for different objective: noise (goal: minimization of input noise integrated over the 3dB bandwidth), linearity (goal: minimization of THD for input signal level $0.15V_{pp}$ for variant I ($0.4V_{pp}$ for variant II, and $0.4V_{pp}$ for variant III) at frequency 1MHz) and dynamic range (goal: maximization of DR at THD=-40dB for variant I [-55dB for variant II & III] with input signal frequency 1MHz). The filter with biquad sequencing $H_1H_2H_3H_4$ and K_i=0dB, i=1,2,3,4, as the reference is treated as the reference. Table 2.5 shows target function values for the reference filter. Tables 2.6-2.8 show optimization results for the Filter in Fig. 2.38 in variant I (simple OTA), II (linearized OTA [75]), and III (linearized OTA [78]), respectively.

Table 2.5. Parameters for Reference Filter Combination $H_1H_2H_3H_4$ (with All Gains Ki=0 dB) (as in Fig. 2.38)

Target Parameter / Filter Realization	Noise [μV]	THD [dB]	DR [dB]
Variant I	432 [437]	-31.5 [-32.4]	40.7 [41.1]
Variant II [75]	705 [670]	-56.8 [-57.8]	49.9 [51.0]
Variant III [78]	1170 [1066]	-46.5 [-46.4]	42.3 [42.9]

Table 2.6. Optimization Results for the 8th Order Cascade Filter (in Fig. 2.38) Using Variant I OTA

Optimal Configuration							
Target Parameter	Biquad Sequence	Biquad Gains [dB]				Value	Improvement Over Ref. $H_1H_2H_3H_4$ [dB]
		K_1	K_2	K_3	K_4		
Noise [μV]	$H_3H_4H_2H_1$	3.0	3.0	-3.0	-3.0	169 [172]	8.2 [8.1]
THD [dB]	$H_3H_1H_2H_4$	-3.0	-2.1	2.1	3.0	-37.7 [-38]	6.2 [5.6]
DR [dB]	$H_4H_3H_2H_1$	1.8	-1.4	-0.9	0.5	47.4 [47.5]	6.7 [6.4]

Values in brackets are from simulations in CADENCE, outside brackets are from the theoretical model

* Noise is the output integrated noise in the bandwidth of 8MHz

** THD for 0.15Vpp input voltage at 1MHz for variant I and 0.4Vpp for variant II and III

** Dynamic Range for THD of -40dB for variant I, -55dB for variants II, III

Table 2.7. Optimization Results for the 8th Order Cascade Filter (in Fig. 2.38) Using Variant II OTA [75]

Optimal Configuration							
Target Parameter	**Biquad Sequence**	**Biquad Gains [dB]**				**Value**	**Improvement Over Ref. $H_1H_2H_3H_4$ [dB]**
		K_1	K_2	K_3	K_4		
Noise [μV]	$H_3H_4H_2H_1$	3.0	3.0	-3.0	-3.0	275 [342]	8.2 [5.8]
THD [dB]	$H_3H_1H_2H_4$	-1.7	-1.3	0.0	3.0	-60.5 [-59.8]	3.7 [2.0]
DR [dB]	$H_4H_3H_2H_1$	1.3	-1.1	-0.6	0.4	56.5 [56.0]	6.6 [5.0]

Table 2.8. Optimization Results for the 8th Order Cascade Filter (in Fig. 2.38) Using Variant III OTA [78]

Optimal Configuration							
Target Parameter	**Biquad Sequence**	**Biquad Gains [dB]**				**Value**	**Improvement Over Ref. $H_1H_2H_3H_4$ [dB]**
		K_1	K_2	K_3	K_4		
Noise [μV]	$H_3H_4H_2H_1$	3.0	3.0	-3.0	-3.0	458 [533]	8.1 [6.1]
THD [dB]	$H_3H_1H_2H_4$	-1.7	-1.3	0.0	3.0	-54.8 [-53.3]	8.3 [6.9]
DR [dB]	$H_4H_3H_2H_1$	2.4	-1.5	-1.0	0.1	48.9 [48.4]	6.6 [5.5]

* Values in brackets are from simulations in CADENCE, outside brackets are from the theoretical model

* Noise is the output integrated noise in the bandwidth of 8MHz

** THD for 0.15Vpp input voltage at 1MHz for variant I and 0.4Vpp for variant II and III

** Dynamic Range for THD of -40dB for variant I, -55dB for variants II, III

To give a better insight into the optimization process, the case of best dynamic range configuration for variant III ($H_4H_3H_2H_1$), has an output integrated noise of 632μV and the input voltage amplitude for the *THD* of -55dB is 0.167V. Though the noise and *THD* results compared to the best cases are less, the overall dynamic range of this configuration is the optimal one. This approach can be used to optimize any particular performance metric and also determine the other metrics.

In all the cases, the process only involves optimal placement of the cascade blocks. Hence the overall area is maintained at the same value, cause it just involves changing the cascade configurations. No changes are incurred to the capacitors values or the transistor dimensions. The gain of each block is controlled by bias voltages and this could cause slight variations in the power consumption. This variation for this cascade filter design is not very significant. But in general power consumption should also be considered.

There is a very good agreement between theoretical and transistor-level simulation results. It can be observed that optimal linearity, dynamic and noise performance is obtained for different biquad sequencing and gain distributions. Note also that optimal biquad sequencing does not depend on OTA used for filter implementation, which is not the case for gain distribution if target parameter involves linearity of the circuit. It should be emphasized that the optimization process including exhaustive search through all 24 biquad permutations and numerical optimization of target function involving multiple *THD* evaluations (note that in case of *DR* it is necessary to perform nested nonlinear optimization in order to find input signal level corresponding to required THD value) is fully automated and very fast. For example, transient analysis of the filter in Fig. 2.38 using OTA macromodeling and integration of equation (2.49) involves less then 0.04s of CPU time regardless filter variant vs. 16.2s (variant I), 17.2s (variant II), and 19s (variant III) for transistor-level simulation, with almost no loss of accuracy.

From a designer's perspective, the optimal cascading sequence could yield a significant improvement in the target parameter. It is not necessary for all the sequences

to be designed manually in simulators like CADENCE. This approach gives a better view of the results expected.

2.3. Conclusion

A framework for the modeling of non-linearities and noise in general OTA-C filters has been presented. Also a general framework for the performance optimization of continuous-time OTA-C filters has been presented based on matrix description of a general OTA-C filter model. In particular, a general description of OTA-C filters with nonlinear transconductors has been introduced. A nonlinear ordinary differential system that describes time evolution of output signal for an arbitrary OTA-C filter was formulated. The presented method allows carrying out an effective and fast transient analysis of any OTA-C filter using standard numerical methods and can be applied to determine the THD or other nonlinearity measures of filters containing nonlinear transconductors. On the other hand, universal expressions were derived that permit computing the filter noise. The model and all the formulas were implemented in a software package that allows calculating OTA-C filter nonlinearity, noise and dynamic range. Efficiency and accuracy of the approach were shown by comparing the results obtained using the theoretical models with simulation and experimental data. As an application, the optimal block sequencing and gain distribution for 8th order Butterworth filter in cascade realization was found. Comparison between the theoretical results and CADENCE simulation on transistor-level confirms high accuracy of the approach.

CHAPTER III

A LINEARIZED CMOS OTA USING ACTIVE ERROR FEED-FORWARD TECHNIQUE*

3.1. Motivation and Background

High-frequency continuous-time filters have many applications in analog signal processing such as anti-aliasing and reconstruction filters for A/D and D/A converters and radio and video frequency filtering in communication receivers. In Chapter I, a brief exposure to the various applications of the continuous-time filters were given, covering the entire bandwidth from low frequency zone to the region of GHz range. For realizing fully-integrated, high-frequency continuous-time filters, operational transconductance amplifiers (OTA) have been receiving much attention because of their superior high frequency characteristics compared with OpAmps and their suitability for implementing by a standard CMOS technology.

The OTA-C integrators operate in open loop configuration unlike the OpAmp based integrators. This places large signal linearity restriction on the OTA around the unity gain frequencies. In case of the OpAmp based integrators, as they have large feedback gain over their operating frequencies, reducing the signal swings at the inputs. The major source of non-linearity in CMOS transconductance amplifiers is due to the voltage to current conversion at the inputs stage, as mentioned in chapters I and II.

In this chapter, a highly linear operational transconductance amplifier (OTA) based on an active-error feedforward linearization scheme which was proposed theoretically in [78] is verified experimentally. In the active-error feedforward

---

technique, the error signal is generated using an additional differential pair transconductor and a linear resistor. Feedforward linearization is widely used to reduce nonlinear distortion in amplifiers [82]-[85]. The proposed technique gives effective linearization, allows us to implement the OTA circuit which has extremely low power consumption, extended linear range of operation, as well as good transconductance tuning capability. Moreover, the effective excess phase compensation can be easily applied, which makes the circuit suitable for high-frequency applications.

In this chapter another linearization technique based on complimentary input stage coupled with signal attenuation is introduced. This topology has a very good linearity performance when compared to the other topologies for a lesser power consumption. It can be used for base band applications like VDSL [86]-[87], ADSL etc.

3.1.1 Linearization Techniques

OTA-C filters based on transconductors working in open loop have the potential to operate at high frequencies, relative to the Active-RC filters based on OpAmp working in closed loop. However, the linear signal range of a transconductor is usually limited, also due to the open loop operation, which will consequently limit the dynamic range.

Linearization techniques [85]-[99] have been developed to make the OTA able to handle input signals of the order of volts with nonlinearities of a fraction of one percent. In general, the drawbacks of linearization techniques are degradation of the frequency response of the OTA especially if many additional nodes are introduced, and the deterioration of the noise performance of the OTA especially if many additional devices are introduced. This is translated to payments in terms of higher power consumption and additional silicon area. It is very desirable that those drawbacks are minimized to get a net benefit from the linearization technique.

A brief introduction to non-linearity and distortions were given in chapter I. The same approach can be put into use for a simple differential pair as shown in Fig. 3.1. The output differential current can be given as the difference between the individual drain

currents, I_1 and I_2 and their bias current is the summation of the two. This is shown in equation (3.1).

$$I_o = I_1 - I_2,\ I_{DC} = I_1 + I_2 \tag{3.1}$$

where I_1 and I_2 are given as in (3.2),

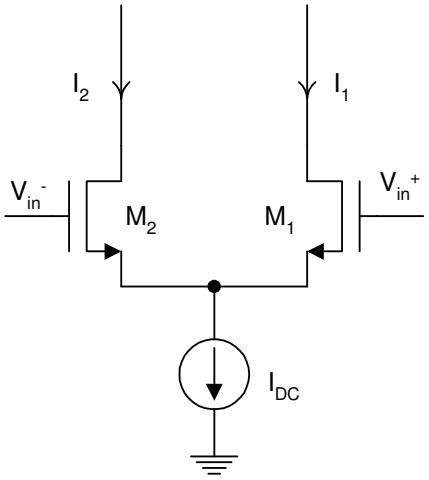


Fig. 3.1. Simple differential pair

$$I_1 = \frac{I_{DC}}{2} + \frac{I_o}{2},\ I_2 = \frac{I_{DC}}{2} - \frac{I_o}{2} \tag{3.2}$$

From the circuit level point of view, the drain currents can be described in terms of the effective voltages $(V_{GS} - V_T)$ as shown in equations (3.3a) and (3.3b). The effective differential voltage can also be determined using these equations.

$$I_1 = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\left(V_{GS1} - V_T\right)^2, I_2 = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\left(V_{GS2} - V_T\right)^2, \beta = \mu_n C_{ox}\frac{W}{L} \tag{3.3a}$$

$$V_{GS1} = V_T + \sqrt{\frac{2I_1}{\beta}},\ V_{GS2} = V_T + \sqrt{\frac{2I_2}{\beta}} \tag{3.3b}$$

It can be seen from Fig. 3.1 that the difference in their gate voltages is their differential input, v_d.

$$V_{GS1} - V_{GS2} = V_{in+} - V_{in-} = v_d \tag{3.3c}$$

The differential voltage v_d can be expressed as a function of the drain currents by substituting (3.3b) in (3.3c) as shown in equation (3.4).

$$v_d = \sqrt{\frac{2}{\beta}}\left(\sqrt{I_1} - \sqrt{I_2}\right) \tag{3.4}$$

Drain currents I1 and I2 were represented in terms of the output current and the bias current in (3.2), using the same in (3.4), vd can be expressed as,

$$v_d = \sqrt{\frac{2}{\beta}}\left(\sqrt{\frac{I_{DC}}{2} + \frac{I_o}{2}} - \sqrt{\frac{I_{DC}}{2} - \frac{I_o}{2}}\right) \tag{3.5}$$

and the output current can be modified as shown in (3.6).

$$I_o = v_d\sqrt{\beta I_{DC}}\left(1 - \frac{\beta v_d^2}{4I_{DC}}\right)^{1/2} \tag{3.6}$$

From the general description of a non-linear system, as introduced in chapter 1 (1.4), the input output relation of a non-linear system, in this case output current vs. input differential voltage, can be expressed as shown in (3.7).

$$I_o = \alpha_1 v_d + \alpha_3 v_d^3 + \alpha_5 v_d^5 + ... \tag{3.7}$$

Expanding *Io* is power series the coefficients can be correlated. The first order term α_1 ($\alpha_1 = \sqrt{\beta I_{DC}} = g_m$) is the linear transconductance g_m of the simple differential pair, and $\alpha_3 = \frac{1}{8}\sqrt{\beta I_{DC}}\,\frac{\beta}{I_{DC}} = \frac{1}{8}\frac{g_m}{(V_{GS} - V_T)^2} = \frac{1}{8}\frac{g_m}{V_{DSAT}^2}$. Substituting α_3 and α_1 in the general expression of the third order harmonic ($HD_3 = \alpha_3 V_{amp}^2/4\alpha_1$), where V_{amp} is the amplitude of the input signal. Thus the third order harmonic in terms of design equations becomes,

$$HD_3 = \frac{1}{32}\frac{V_{amp}^2}{(V_{GS} - V_T)^2} = \frac{1}{32}\frac{V_{amp}^2}{V_{DSAT}^2} \tag{3.8}$$

The higher order harmonics in most cases are very small, that they are considered negligible. The main contributor to non-linear distortions is the third harmonic term. Thus all attempts of linearization techniques focuses on reducing this term. This is done

by either increasing the V_{DSAT}, this has some basic trade-offs in terms of power, also limited supply voltages and limited swings. Another basic approach is to minimize the dependencies of the transconductance term on the input voltage. Some of the basic linearization techniques, and also the proposed techniques are mentioned below.

3.1.1.1 Source Degeneration

One of the most natural high-frequency linearization techniques often used is source degeneration, shown in Fig. 3.2. It can be shown that the small-signal transconductance is reduced by the factor $(1+g_mR)$ where g_m is the transconductance of transistors M_1 and $n=g_mR$ is the source degeneration factor. On the other hand, the third harmonic distortion improves relative to the case of a simple differential pair, as given in equation (3.9), by the factor $(1+n)^2$.

$$HD_3 = \frac{v_d^{\,2}}{32(1+n)^2(V_{GS}-V_T)^2} \tag{3.9}$$

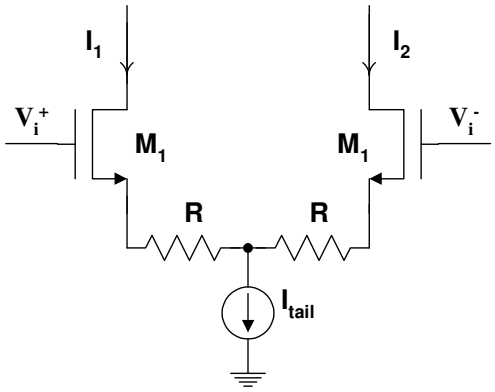


Fig. 3.2. Linearization using source degeneration

3.1.1.2 Attenuation

Another category of linearization techniques is attenuation. In this category, the input voltage is attenuated by a factor m, i.e., $V_{in,att}=mV_{in}$ $(m<1)$. This will result in

reducing the transconductance by the same factor, i.e., $g_{m,att}=mg_m$, and improving the linearity by the factor m^2. For an attenuation factor m, and using equation 3.8, the third order harmonic distortion can be derived as:

$$HD_3 = \frac{v_d^2}{32m^2(V_{GS} - V_T)^2} \tag{3.10}$$

There are many techniques in this category. One approach is to use a series of differential pairs, as shown in Fig. 3.3. This effectively split the voltage in the sections by *m* where *m* is the number of sections used. The major drawback of this approach is the degradation of the phase response with increasing the number of sections. For the case of two sections, the attenuation factor m is 2 and using equation (3.10), HD_3 of Fig. 3.3 can be written as shown in equation (3.11),

$$HD_3 = \frac{v_d^2}{128(V_{GS} - V_T)^2} \tag{3.11}$$

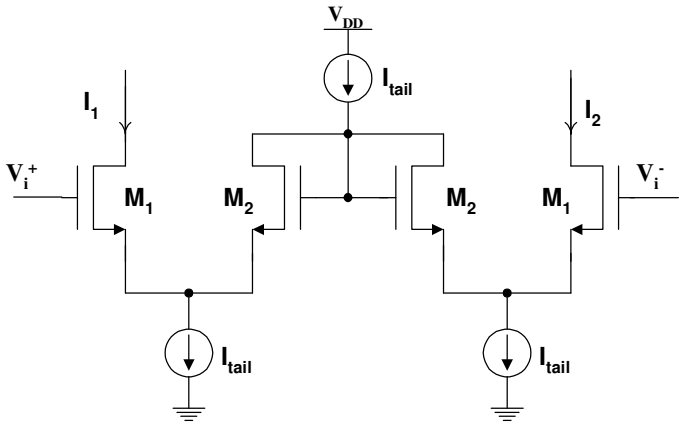


Fig. 3.3. Linearization using series of differential pairs

Another approach in this category is the use of floating gates [88], as shown in Fig. 3.4. Floating gates provide a natural capacitive divider for the input signal. Thus, the effective input ac voltage applied to the floating gate (FG) is reduced by the factor

$k=(C_1+C_2)/C_1$, where C_1 and C_2 are the capacitances associated with the input signal and the bias voltage, respectively. Although floating gate techniques are very attractive for low voltage applications [88]; their usage in high frequency is limited due to the capacitive coupling elements involved. Also very good layout techniques are required to lay the capacitors out. Though this method improves the linearity, the noise performance of the floating gate transistor is deteriorated with respect to its conventional counterpart. The output refereed noise is the same, but the input refereed noise is increased by the factor k^2.

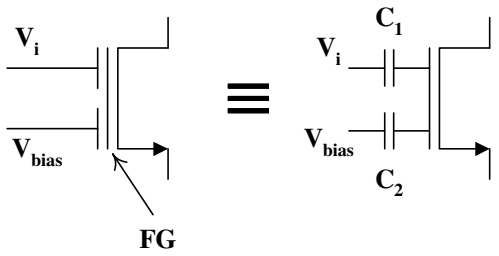


Fig. 3.4. Linearization using floating gates [88]

A third approach in the attenuation category is using bulk driven transistors [89], as shown in Fig. 3.5. The transconductance of a transistor driven from the bulk rather than the gate is reduced by a factor γ, where γ is in the range of 0.2 and 0.4 i.e. bulk-driven transconductance g_{mb} is typically round 0.2–0.4 times of g_m (3.12), but it is very process dependent. Shown in equation (3.12) is the transconductance of the bulk driven transistor.

$$g_{mb} = \left(\frac{\gamma_o}{2\sqrt{2\phi_{FB} + |V_{SB}|}} \right) \times g_m \tag{3.12}$$

where γ_0 is the body effect parameter, φ_{FB} is the bulk Fermi potential, V_{SB} is the bias voltage at the bulk and g_m is the transconductance of the amplifier which is gate driven.

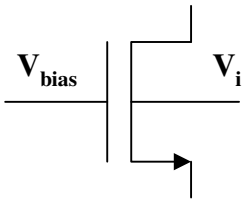


Fig. 3.5. Linearization using bulk driven transistor [89]

Bulk-driven technique is also attractive for low voltage applications but it suffers from worse frequency response, with respect to the conventional gate drive case. The equivalent noise and area of a bulk driven transistor is also larger than a conventional gate drive transistor. It also suffers form potential latch up problems.

Table 3.1. Attenuation Factors of Different Techniques

Attenuation Technique	Attenuation Factor (m)
Series of differential pairs	Number of sections used
Floating gate [88]	$(C_2+C_1)/C_1$
Bulk driven [89]	$2.5 < (1/\gamma) < 5$

Attenuation factors of different techniques are shown in Table 3.1. It is obvious in all of the attenuation techniques mentioned above that the transconductance is reduced by the attenuation factor and hence need to be compensated at the expense of power consumption and/or silicon area. Note that more than one linearization technique can be combined together to achieve better linearity [85].

3.1.1.3 Combination of Techniques

Some linearization techniques also involve a combination of some of the techniques mentioned above. For example, a linearization technique can include current

splitting and source degeneration to have an improved linearity performance. However the drawbacks of some of these combination methods is that they require more power to compensate for the other losses.

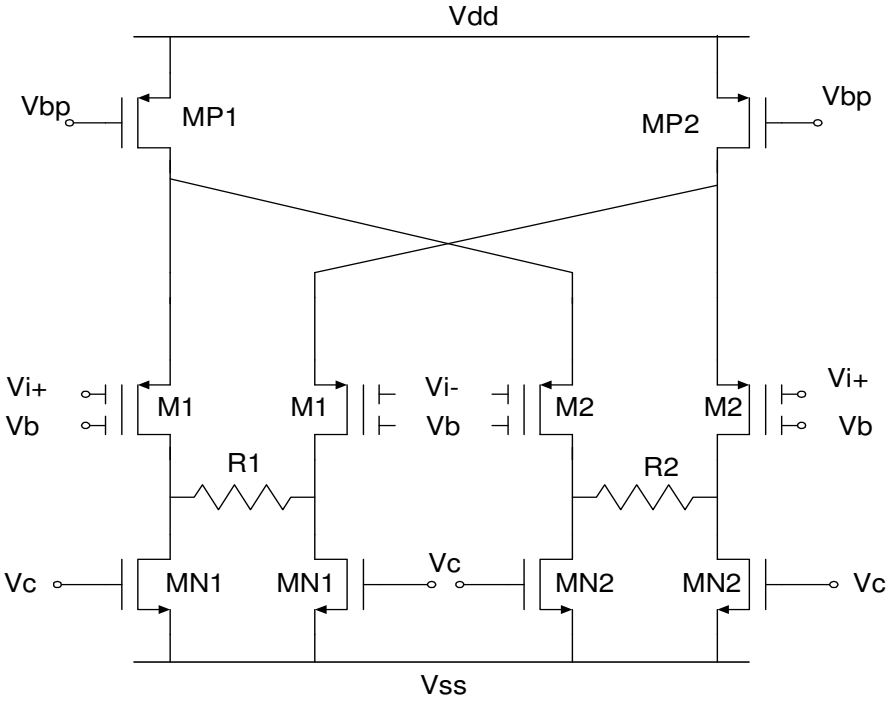


Fig. 3.6. Linearization technique using voltage division, source degeneration, cross coupling

Techniques like cross coupling of differential input stages are also performed. The main idea behind cross coupling of input stages is the elimination of the third order harmonics which is the main contributor of the non-linear distortion. Linearization techniques, as shown in Fig. 3.6, utilizing source degeneration, attenuation technique like floating gates input, cross coupling for elimination of third order harmonics using a double differential pair, all in the same design are discussed in [90].

The linearization techniques mentioned above holds good for both fully-differential OTA and also pseudo-differential OTA. Following is an example of a pseudo-differential OTA.

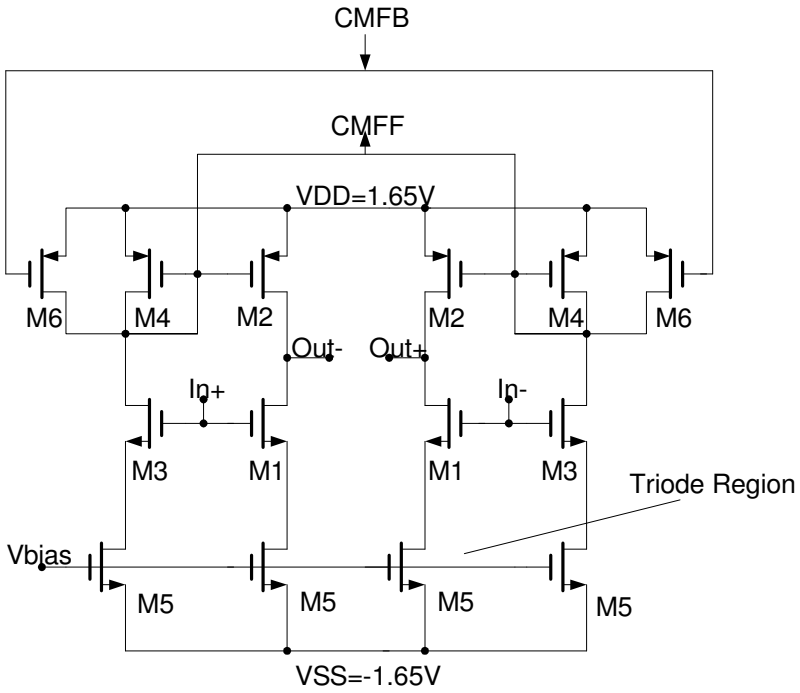


Fig. 3.7. Fully balanced, fully symmetric pseudo-differential OTA [75]

The OTA shown in Fig. 3.7 is OTA is a pseudo differential OTA with inherent common mode feedforward and feedback [75]. The principle of source degeneration is used in this technique. It is based on a fully balanced fully symmetric circuit design. Source degeneration is used to increase the linearity of the OTA. Transistors M_5 and M_7 in the above design operates in the triode region and these transistors introduces the source degeneration necessary to improve the linearity of the OTA.

3.1.1.4 Linearization Using Complimentary Differential Pairs

The OTA shown in Fig. 3.8 is a pseudo-differential OTA with a complimentary input stage [94]. The input stage has both the n type differential pair (M_1), and the p type differential pair (M_2). The OTA also has source degeneration established using transistors M_n and M_p.

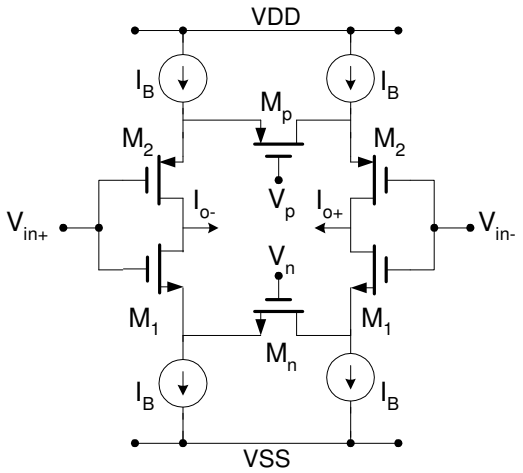


Fig. 3.8. Complimentary differential pair OTA

These transistors M_n and M_p are operating in the linear region and the amount of source degeneration can be adjusted using the bias voltages. The overall transconductance has a contribution from the n and the p differential input pairs respectively. The effect of source degeneration on the transconductance has been explained in the previous section. Thus the overall transconductance of this OTA can be derived as shown in (3.13),

$$G_m = \frac{g_{mn}}{1+N_n} + \frac{g_{mp}}{1+N_p}; \quad N_n = g_{mn}R_n, N_p = g_{mp}R_p \tag{3.13}$$

where R_n and R_p are the value of resistance offered by the transistors M_n and M_p in the linear region. The factor *N* is called the degeneration factor. The normal trade-off using

the approach of source degeneration is that the overall transconductance gets reduced and to maintain a higher gain more power is required and to maintain a linear performance *N* should be more. In this case of complimentary differential pair, the additional boast in the g_m comes from the other pair, without having the need to spend more power. The effect on HD_3 is shown in equation (3.14).

$$HD_3 = \frac{1}{32}\left(\frac{1}{N_n+1}\right)^2\left(\frac{v_{amp}}{V_{DS,satn}}\right)^2\frac{g_{mn}\left(N_p+1\right)}{g_{mn}\left(N_p+1\right)+g_{mp}\left(N_n+1\right)}+ \frac{1}{32}\left(\frac{1}{N_p+1}\right)^2\left(\frac{v_{amp}}{V_{DS,satp}}\right)^2\frac{g_{mp}\left(N_n+1\right)}{g_{mn}\left(N_p+1\right)+g_{mp}\left(N_n+1\right)} \tag{3.14}$$

This approach reduces this term to a greater extent and causes a highly linear system. Using this approach along with the attenuation technique, a particular design of an OTA is introduced for VDSL filter applications.

3.2. A Highly Linear OTA-C Based Filter for VDSL Applications

This section introduces a highly linear OTA topology for a 3rd order filter used in VDSL applications [87]. VDSL applications demand very high linearity performance and also the noise performance should be very good. Many OTA-C based filters are explored in the literature for this application. In this approach a highly linear OTA is introduced. The linearization techniques involved in this approach is a combination of source degeneration, attenuation of the input and this is all done using a complimentary differential pair. The effect on the third harmonic, HD_3, was already explained in equations (3.14) and results from Table 3.1. This method enables to achieve linearity to a higher level. It reduced the third harmonic value by a greater fraction. In Order to achieve this and also a reasonable gain, enough power needs to be spent.

The filter used for this application using the above mentioned approach is shown in Fig. 3.9.

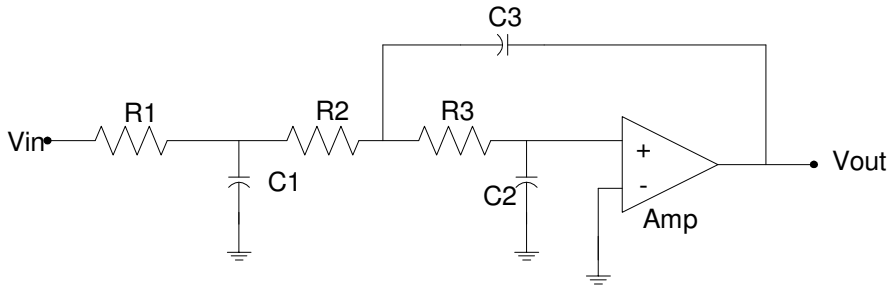


Fig. 3.9. 3rd order filter for VDSL applications

The active block mentioned in Fig. 3.9 is termed as amplifier. It is an OTA with a resistive load, hence the output is a voltage. The signal attenuation at the input can be achieved by splitting the capacitor C_2 into C_2' and C_2'' and the ratio between these capacitors decide the amount of attenuation required. The second order section of the filter with capacitive division at the input is shown in Fig. 3.10.

The active block used in this design is shown in Fig. 3.11. A low gain highly amplifier is designed for the VDSL filter. The amplifier has a complimentary input differential pair. Fig. 3.11 shows the transistor level implementation of the amplifier. The input stage includes a complimentary input differential pairs (M1 and M2). Resistors Rn and Rp provide the source degeneration for M1 and M2 respectively. Mb and Mp1 are the current sources for the input differential pair and transistor pair Mp2 acts as the by-pass path for the extra current. If a resistive load is connected at the output node with the other terminal connected to ground, the need for a common mode is also not required. This topology of the low gain amplifier is used in the design.

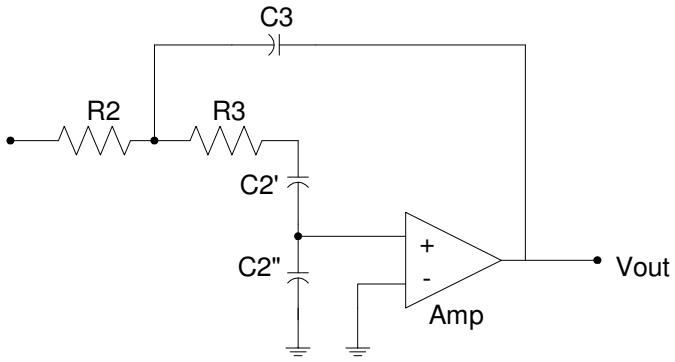


Fig. 3.10. Signal attenuation at the input of the amplifier

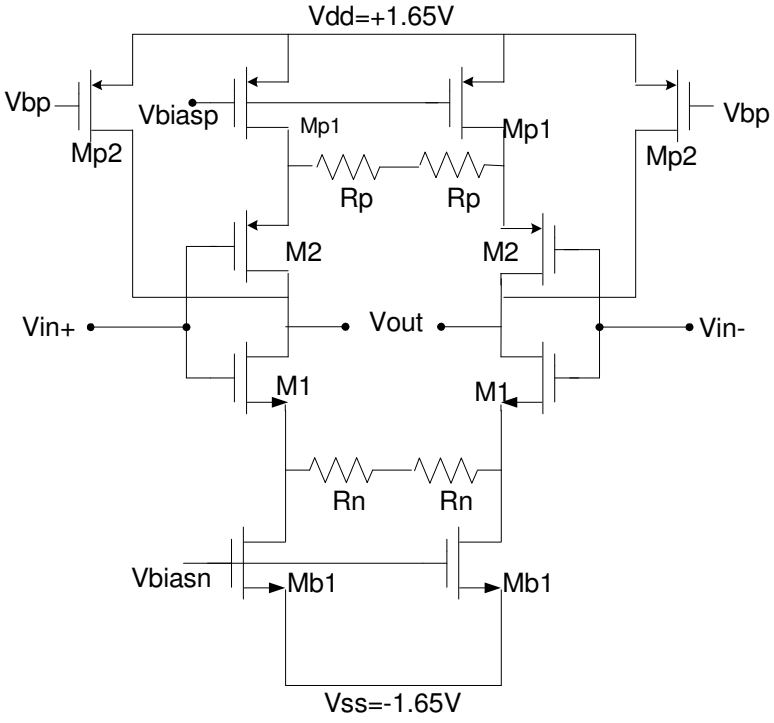


Fig. 3.11. Linear OTA for the VDSL filter

(Based on the research work of Arun Ramachandran, Dr. Antonio Torralba of Seville, Spain, Dr. Jose-Silva Martinez and Dr. Edgar Sánchez-Sinencio of Texas A&M University, College Station.)

The expressions for the overall g_m and the HD_3 are already explained in the previous section. Since the input signal attenuation is performed using a capacitor, which is also involved in the filter's characteristic performance, the attenuation ratio is compensated using the low gain of the amplifier. i.e. if the attenuation ratio at the input is 2, the amplifier is designed to have a gain of 2 (6dB), such that the overall gain is still 1, as per the filter requirements. Using equation (3.13), the gain of the amplifier can be given as shown in (3.15), where R_L is the load resistors connected between the output nodes and ground on the other end.

$$\text{Gain} = G_m R_L \tag{3.15}$$

To explain the performance of this amplifier in the filter structure, the specific application is taken for consideration. This filter shown in Fig. 3.9 is for the application of a VDSL front end block. The filter approximation used for the design of the filter is a Butterworth approximation. The Chebyshev approximation also has a magnitude response similar to that of the Butterworth approximation and has a ripple in the pass band, but the capacitors values to implement a Chebyshev filter is quite large when compared to those for the Butterworth implementation.

In Fig. 3.9, the first block is a first order low pass RC filter structure. The analysis of the filter design and the amplifier design for the time being includes the second order block comprised of the resistors R_2, R_3, capacitors C_2, C_3 and the amplifier. This second order block is the most important block as it decides the shape of the noise curve and also the filter characteristic curves.

3.2.1 Biquad Section

The biquad section comprises of the resistors R_2, R_3, capacitors C_2, C_3 and the amplifier. The biquad section of the filter is a unity-gain section. To determine the values of the resistors and capacitors equation (3.16) and (3.17) are used. For this the resistor and capacitor values are set as ratios of m and n respectively.

$$\begin{aligned} R_2 = R, R_2 = mR \\ C_2 = C, C_3 = nC \end{aligned} \tag{3.16}$$

$$F_c = \frac{1}{RC\sqrt{mn}} \quad : \quad Q = \frac{\sqrt{mn}}{m+1} \tag{3.17}$$

To implement a Butterworth filter with a 3dB frequency of 12MHz and a *Q* of 1, the values of *m* and *n* are chosen to be 2 and 4 respectively (*Q*=0.942). The values of resistors and capacitors are R_2 is 1.5KΩ and C_2=3.12pF.

3.2.2 Simulation Results

The performance of this OTA can be verified from simulation results from CADENCE. Since this design is not yet fabricated, the simulation results are mentioned below. The stand alone OTA and the filter were designed in CMOS 0.35µm technology. The gain of the amplifier was simulated to be 6dB. The Inter modulation product terms (IM_3) which measures the linear behavior of the OTA was found to be -72dB for an input signal with a differential peak-to-peak value of 2V at 10MHz and 11MHz. From this term the HD_3 can be estimated to be around -81dB. It can be observed that the above mentioned approach provides a very highly linear circuit for maximum voltage swing at the input. The power supply is ±1.65V. The input referred noise spectral density is around 33nV/√Hz. The total power consumed is around 19mW. Thus for a lower power consumption, a highly linear circuit can be designed. The simulated results of the OTA and the filter are tabulated in Tables 3.2 and 3.3.

The overall gain of the amplifier is 0dB and the 3dB frequency of the filter is at 12MHz. The frequency response is in accordance with the filter specifications. The maximum input differential signal is 2Vpp. An input at 1MHz was given to verify the output swing of the filter. To measure the linearity of the filter, two tones were given as inputs and the IM_3 was measured from the output spectrum.

Table 3.2. Amplifier Simulation Results

Parameter	Simulated Value
DC Gain	6dB
Input Referred Noise Density	33nV/sqrt(Hz)
IM3 (From Two Tone Test: Vin,pp=2Vpp at 10MHz and 11MHz	-71.33dB
THD (Estimated from IM3)	-80 dB
Power Consumed	19mW

From the output spectrum of the filter for a two tone given at 9MHz and 10MHz, the IM_3 is estimated to be around -64.5dB. Time domain measurement of the linearity was also done for two tones at 4MHz and 5MHz and from the output spectrum the IM_3 is around -65.5dB (THD= -74.5dB). The desired level is around -75dB.

Table 3.3. Filter Simulation Results

Parameter	Simulated Value
DC Gain	0dB
3dB Frequency	12MHz
Input Referred Noise Density	33nV/sqrt(Hz) and a maximum of 78nV/sqrt(Hz) around 12MHz
IM3 (From Two Tone Test: Vinpp=2Vpp at 10MHz and 11MHz	-64.5B
IM3 (From Two Tone Test: Vinpp=2Vpp at 4MHz and 5MHz	-65.5dB
THD (Estimated from IM3)	-74dB
Power Consumed	19mW

The input referred noise spectral density is around 33nV/sqrt(Hz). However the noise density takes the shape due to the resistors and capacitors in the filter structure. This was verified for the general case of Sallen and Key architectures. The main contribution was from the current source transistors. The value of *Gm* of the current source transistors needs to be reduced to reduce the slope of this curve and at the same time without affecting the linearity of the filter.

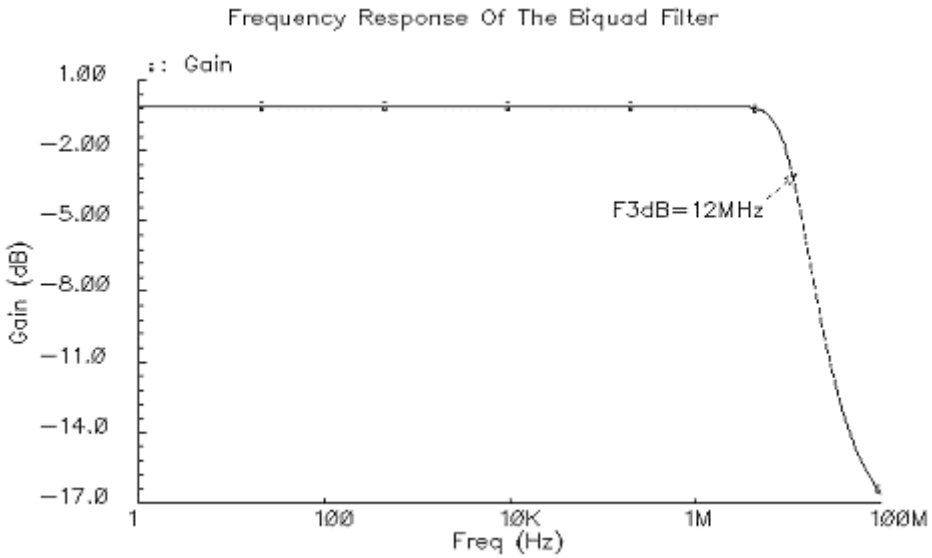


Fig. 3.12.3rd order Butterworth filter's magnitude response

Fig. 3.12, 3.13 and 3.14 shows the simulated results for the filter's magnitude performance, two tone tests at 10MHz and 11MHz for a 2Vpp input signal and the input referred noise spectral density.

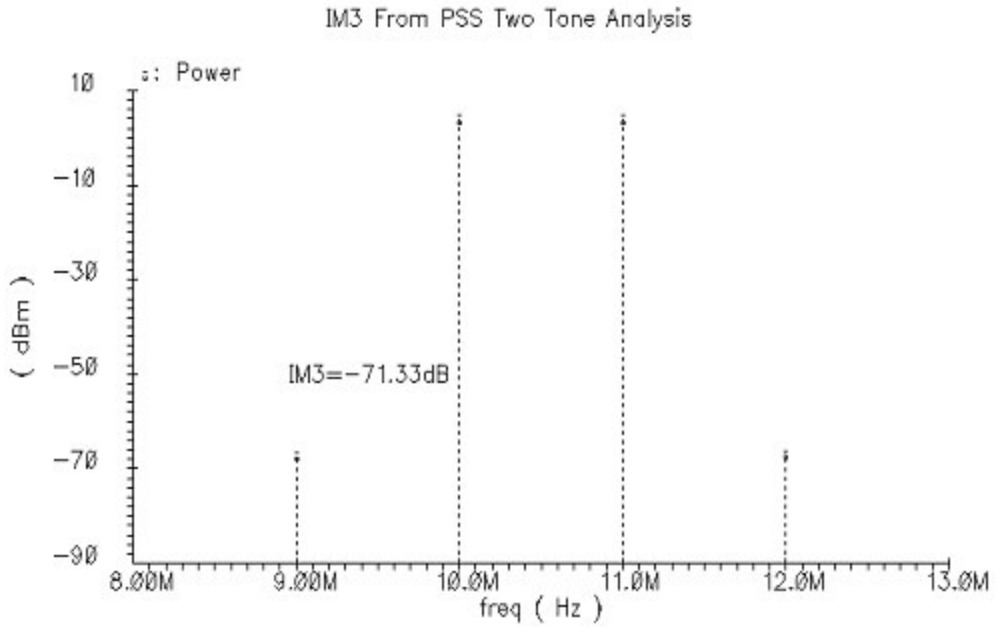


Fig. 3.13.Two tone analysis results for IM3 simulation for two equal tones of 1Vpp at 10MHz and 11MHz for the 3rd order filter

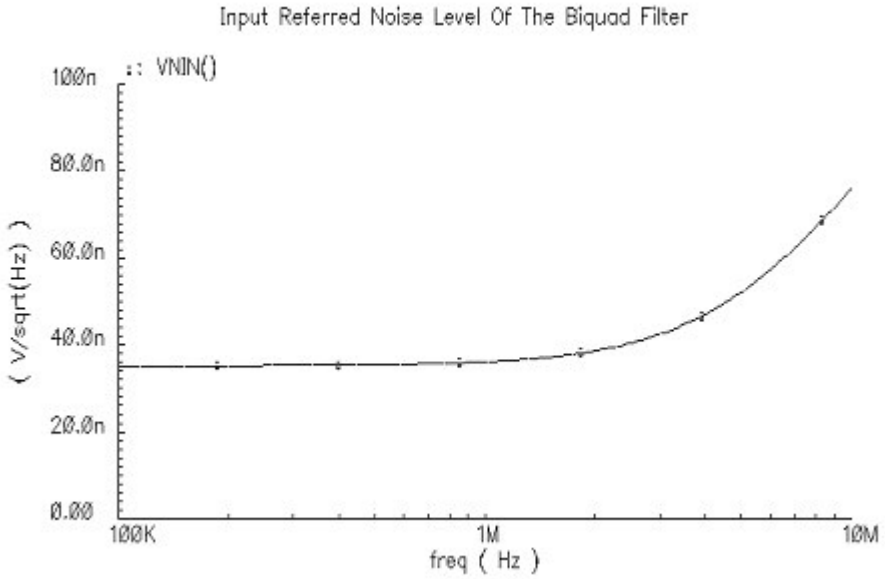


Fig. 3.14. Input referred noise spectral density for the 3rd order filter

The increase in the input referred noise spectral density is due the inherent structure of the Sallen and key low gain amplifier based filter structures. The same can also be verified using sensitivity analysis of the structure, which is not the focus of this section.

Most of the filter blocks discussed in literature ([100]-[101]), for VDSL/ADSL applications have considered the filter as an integral part of the analog front end for the system. Table 3.4 gives a comparison of some of works already published with the results of the filter described in the above section.

Table 3.4. Comparison Of VDSL Results

Reference/ Parameter	**CICC [87]**	**JSSC [100]**	**ISSCC [101]**	**This Work**
Technology	0.35µm + 0.5µm	0.13µm	0.13µm + 0.5µm	0.35µm
Power/Pole*	87.5mW	37.5mW	266mW	6.4mW
Input Integrated Noise	100nV/√Hz	22nV/√Hz	100nV/√Hz	33nV/√Hz
Supply Voltage	-	2.5 V	3.3 V	3.3 V
Input Signal Swing	-	1.6V	-	2 V
Filter Order/Type	4^{th} , Elliptic Low Pass	2^{nd}, Butterworth Low Pass	3^{rd} Low Pass	3rd, Butterworth Low Pass

***** Power is the overall power/pole of the channel in the case of all references and the stand alone filter for this work

3.2.3 Summary

A new topology of a highly linear OTA was introduced and the extension to its application in the case of a VDSL front end analog filter was also explained. The circuit

has a very highly linear characteristic, when the price is paid off in terms of the noise shape. The power consumed is also around 20mW, which is not very high to achieve a linearity level of -75dB. This topology can be used in applications whose noise performance is not very highly demanding. The structure needs to be fabricated to also analyze the performance in Silicon.

In the next section a new linear topology of OTA based on Active-Error Feedforward technique is introduced and the performance is verified using experimental measurements.

3.3. Proposed Highly Linear OTA

In this section, a highly linear operational transconductance amplifier (OTA) based on an active-error feedforward linearization scheme [78] is proposed. The error signal is generated using an additional differential pair transconductor and a linear resistor. Feedforward linearization is widely used to reduce nonlinear distortion in amplifiers. The proposed technique gives effective linearization, allows the implementation of the OTA circuit which has extremely low power consumption, extended linear range of operation, as well as good transconductance tuning capability. Moreover, the effective excess phase compensation can be easily applied, which makes the circuit suitable for high-frequency applications.

3.3.1 Feed-Forward Linearization

From the general description of a non-linear system, as introduced in chapter I (1.4) and (3.7), the input output relation of a non-linear system, in the case output for a simple transconductor (a general case, not necessarily differential one), the output current vs. input voltage, can be expressed as a power series expansion as shown in (3.18).

$$I_G\left(v_{in}(t)\right) = g_1 v_{in}(t) + g_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t) + ... = \sum_{n=1}^{\infty} g_n v_{in}^n(t) = G\left(v_{in}\right) \tag{3.18}$$

where v_{in} is the differential input voltage of the transconductor. By definition, coefficient g_1 is the linear transconductance g_m of the amplifier. For a differential input stage the even order terms vanish and only the odd terms of the power series exist.

Fig. 3.15 shows the concept of transconductance amplifier linearization based on active-error feedforward method.

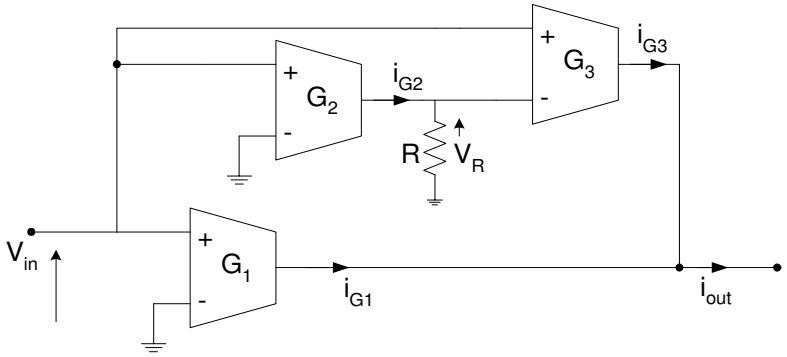


Fig. 3.15. Three block feed-forward transconductance amplifier

All amplifiers G_1, G_2, G_3, modeled as in (3.18), are assumed to be identical. Moreover, it is assumed that resistor R in Fig. 3.15 is linear and equal to $1/g_m$. In practice, e.g. in integrated circuit implementations some technologies offer high resistive poly which can be used to realize resistor R.

Using (3.18), the output current of the overall OTA, including the three intermediate OTA stages, shown in Fig. 3.15, can be written as,

$$i_{out}(t) = \sum_{n=1}^{\infty} g_n \left[v_{in}(t) \right]^n + \sum_{n=1}^{\infty} g_n \left[v_{in}(t) - v_R(t) \right]^n \tag{3.19}$$

where $v_R(t)$ can be expressed using the fact that the first term g_1 is the transconductance g_m of the OTA and the value of $R=1/g_m$.

$$v_R(t) = g_1^{-1} \sum_{n=1}^{\infty} g_n \left[v_{in}(t) \right]^n \tag{3.20}$$

This means that the voltage at the input of the transconductor G_3 (working as an error amplifier) equals,

$$v_{in}(t) - v_R(t) = -g_1^{-1}\sum_{n=2}^{\infty} g_n \left[v_{in}(t) \right]^n \tag{3.21}$$

From (3.19), (3.20) and (3.21), the output current can be written as,

$$i_{out}(t) = \sum_{n=1}^{\infty} g_n \left[v_{in}(t) \right]^n + \sum_{n=1}^{\infty} g_n \left[-g_1^{-1} \sum_{k=2}^{\infty} g_k \left[v_{in}(t) \right]^k \right]^n \tag{3.22}$$

Normally, $v_{in}(t)$-$v_R(t)$ is much smaller than the input voltage of transconductors G_1 and G_2, which allows us to neglect the higher order terms in the output current of G_3. This leads to the approximation of (3.22), which shows the perfect cancellation of nonlinearities of the overall transconductance amplifier in Fig. 3.15.

$$i_{out}(t) = \sum_{n=1}^{\infty} g_n \left[v_{in}(t) \right]^n - \sum_{n=2}^{\infty} g_n \left[v_{in}(t) \right]^n = g_1 v_{in}(t) \tag{3.23}$$

This approach leads to a perfectly linear system, in the theoretical sense. Second order and other process variations needs to be included which might hamper the overall performance.

3.3.2 Analysis of Linearity Performance

Consider a simple CMOS differential pair transconductor shown in Fig. 3.16. It can be shown, using square-law MOS transistor modeling ([91]) that its normalized transfer characteristic around zero is,

$$i_G(x) = 2I_{SS} x \sqrt{1 - x^2} \tag{3.24}$$

where x is a normalized input voltage defined as $x = v_{in}/2(V_{GS}-V_T)$, with v_{in} being a differential input voltage, V_{GS} and V_T - gate-source DC voltage and threshold voltage, respectively; I_{SS} is the biasing tail current of the differential pair. For small V_{in}, $x << 1$ (3.24), can be approximated by equation (3.25).

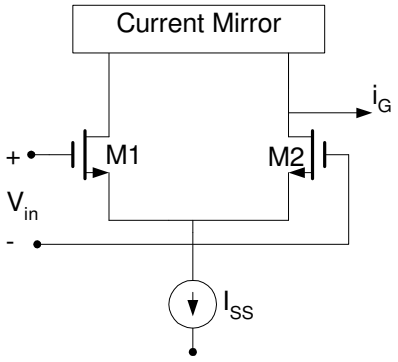


Fig. 3.16. Simple CMOS differential pair transconductor

$$i_G(x) = 2I_{SS}x\left(1 - 0.5x^2\right) \tag{3.25}$$

For a sinusoidal input like $x(t)=A\cos(\omega t)$, the system described by (3.24) yields,

$$i_G(x) = 2I_{SS}\left[\left(A - 0.375A^3\right)\cos\omega t - 0.125A^3\cos 3\omega t\right] \tag{3.26}$$

thus, the third order harmonic term (HD_3) can be approximated to $0.125A^2/(1-0.375A^2)$ or just $0.125A^2$.

Using the theoretical derivation of (3.22), for the active-error feedforward technique, for the same input, the output current can be derived as shown in (3.27).

$$i_G(x) = 2I_{SS}x - 2^{-3}I_{SS}x^9 = 2I_{SS}A\cos\omega t - 2^{-3}I_{SS}\left(A\cos\omega t\right)^9 \tag{3.27}$$

which can further be reduced to (3.28). In this case the third harmonic is $HD_3=0.02A^9$.

$$i_G(x) = 2I_{SS}\left[\left(A - \frac{126}{2^{12}}A^9\right)\cos\omega t - \frac{84}{2^{12}}A^9\cos 3\omega t + \ldots\right] \tag{3.28}$$

Note that linearized circuit has not only third harmonic component but also the 5th, 7th and the 9th harmonics. However, for small values of A, they are negligible. For A=0.1 the following are the values of the third harmonics: $HD_3=1.25\times10^{-4}$ (original circuit- simple differential pair) and $HD_3=2.05\times10^{-11}$(linearized circuit). For A=0.2 HD_3=1.0x10^{-3}(original circuit), $HD_3=1.05\times10^{-8}$ (linearized circuit).

One can calculate THD for both the simple differential pair and linearized circuit assuming the transfer characteristic as in (3.24), for all transconductors (in particular, without neglecting the higher order terms in the output current of G_3 as in (3.25)).

3.3.3 Second Order Effects

Since the OTA's output is current, one of the most important second order effect would be that of the mobility degradation. The influence of mobility degradation on linearity of the differential pair transconductor in Fig. 3.16 linearized using the active-error feedforward method, (i.e. assuming the simple differential pair as the basic block *G* in Fig. 3.15), is investigated below.

The square-law MOS model in saturation including mobility reduction effect [91] is shown in equation (3.29),

$$I_D = \frac{k\left(V_{GS} - V_T\right)^2}{1+\theta\left(V_{GS} - V_T\right)} \tag{3.29}$$

where I_D is the drain current, k - transconductance parameter and θ- the mobility reduction coefficient. Using (3.29) and assuming that $\overline{\theta} = 0.5\theta\left(V_{GS} - V_T\right)$ is small, the transfer characteristic of the circuit in Fig. 3.16 can be approximated as,

$$i_G^{\theta}(x) \cong 2I_{SS}c\left(x - 0.5\overline{c}c^3x^3\right) \tag{3.30}$$

where c and $\overline{c}$ are parameters which are used for simplification ($c = \left(1+2\overline{\theta}\right)/\left(\sqrt{1+2\overline{\theta}}+2\overline{\theta}\right)$, $\overline{c} = \left(1+2\overline{\theta}\right)^{-1/2}$). It can be observed that nonzero $\overline{\theta}$, actually reduces small signal transconductance by factor *c,* and also influences linearity of the circuit. In particular $HD_3 = 0.125\overline{c}c^3A^3$. The linearity is reduced by a factor of $\overline{c}c^3$ in comparison to the case without mobility degradation. While applying to the circuit with the active-error feedforward scheme,

$$i_{out}^{\theta}(x) \cong 2I_{SS}c\left(x - 2^{-3}I_{SS}\overline{c}^4c^{12}x^9\right) \tag{3.31}$$

Observe that small signal transconductance is reduced again by factor c. The third harmonic is now $HD_3=0.02\bar{c}^4c^{12}A^9$, so it is reduced by factor $\left(\bar{c}c^3\right)^4$ in comparison to the case without mobility degradation.

If the parasitics are taken into consideration such as input and output capacitances and output conductances of transconductors, the circuit in Fig. 3.15 becomes a two-zero and two-pole system. The first zero can be used to compensate an excess phase which arises due to other second order poles (if necessary this zero can be moved down in the frequency scale by adding an additional capacitor between the output of transconductor G_2 and the output of the circuit). The addition of the capacitor is explained in the transistor level diagram representation of the circuit.

3.3.4 Linearized OTA Circuit Architecture

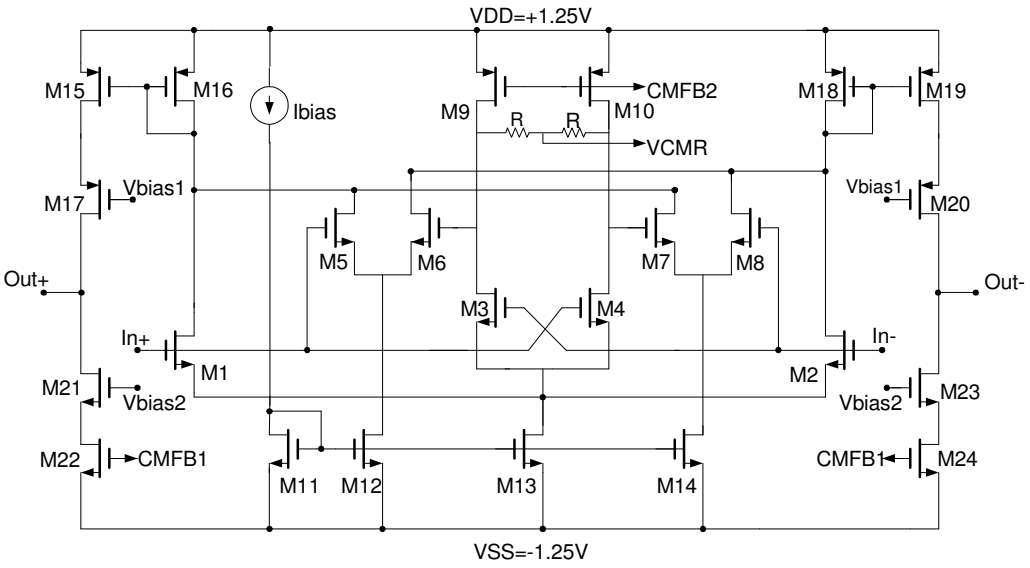


Fig. 3.17. Linearized CMOS OTA based on active-error feedforward technique [78]

Fig. 3.17. shows a circuit implementation of Fig. 3.15. The common mode feedback circuit (CMFB) is shown separately in the following sections. Note that the circuit in Fig. 3.17 is a fully differential OTA. Thus, it is a slight modification of the concept presented in Fig. 3.15. The pair M_1,M_2 implements two-output counterpart of transconductor G_1 Transistors M_3, M_4 implement the counterpart of transconductor G_2 loaded by resistors R ($R= 1/2g_m$). Differential pairs M_5,M_6 and M_7,M_8 with current sinks M_{12} and M_{14}, respectively, realize error amplifiers corresponding to G_3. Two differential pairs are necessary to implement the error amplifier cause the implementation is a fully differential version. The ratio between transistor dimensions of M_{11}, M_{12}, M_{14} and M_{13} is 1:2, cause M_{13} is the current sinks for two input differential pairs. The transconductors have common current sources realized by transistors $M_{15\text{-}17,21,22}$ and $M_{18\text{-}20,23,24}$. Note that in order to change the transconductance of the circuit in Fig. 3.17, the bias current I_{bias} and resistor $1/2g_m$ have to be adjusted simultaneously. This is explained in more detail in the tuning section.

3.3.5 Common Mode Feedback Circuits

Since the OTA implementation is a fully differential version and not pseudo differential, complex common mode feedback methods are not used. Fig. 3.18 and 3.19 shows the common mode circuits for the common mode voltages V_{CMFB1} and V_{CMFB2}. The circuit in Fig. 3.18 is the output common mode feedback circuit, where the differential output common mode voltages are set to the input common mode level, which is ground in this case. $Ibias_2$ is the biasing current source for the common mode block. The common mode signal is fed to the OTA through the gates of transistors M_{22} and M_{24}. Fig. 3.19 shows the common mode feedback circuit for the resistor block in the overall OTA. The detected common mode signal V_{CMR} in between the two resistors is compared with ground and the common mode feedback signal is fed to the gates of transistors M_9 and M_{10}.

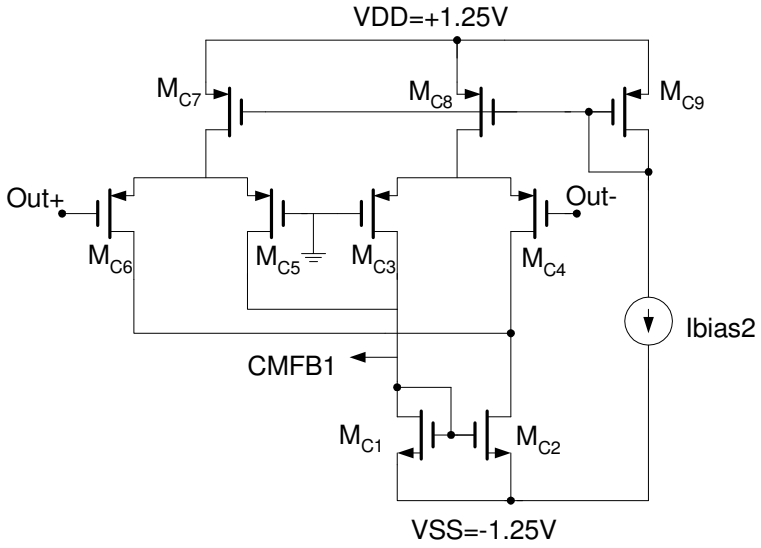


Fig. 3.18. Output common mode feedback circuit (CMFB1)

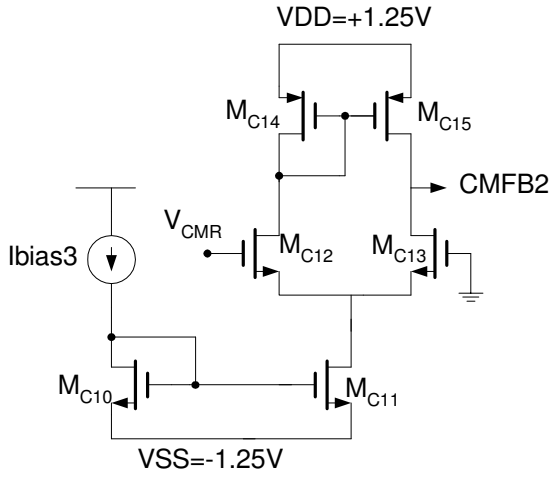


Fig. 3.19. Common mode feedback for the resistor biasing circuit (CMFB2)

3.3.6 Tuning of the OTA

The OTA also has a higher tuning capability. In order to perform frequency tuning of the filter using this OTA, the transconductance g_m of the filter can be tuned to larger range. The tuning control for this OTA is the biasing current I_{bias}. By increasing or

decreasing the amount of current supplied to the input differential pairs, the g_m of each blocks can be increased or decreased respectively. However to maintain the linear performance of the OTA, the resistance $R(R=1/g_m)$ should also be changed simultaneously in order to have perfect cancellations of the non-linear higher order terms. The selection of the resistor tuning block is very critical in this OTA design. One of the simplest methods of tuning the resistors is explained below.

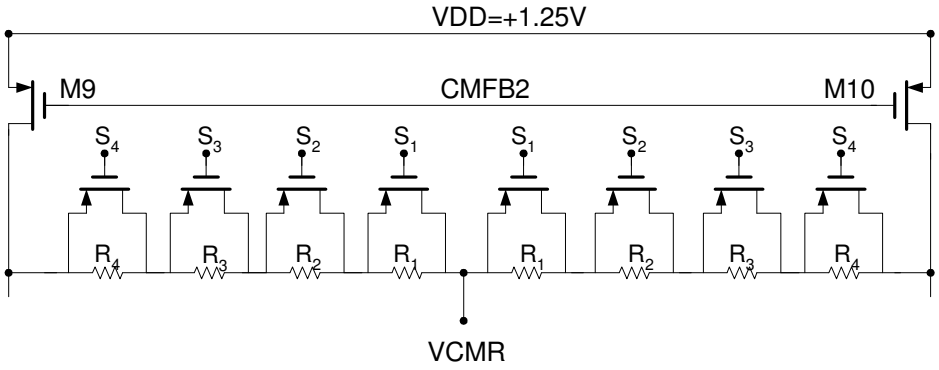


Fig. 3.20. Tuning circuitry for the OTA

In the tuning circuitry shown in Fig. 3.20, all the P type transistors act as switches, whose control voltages are set by $S_{1\text{-}4}$. The maximum resistance that can be got from this circuit is $R_1+R_2+R_3+R_4$. The minimum is just the on switch resistance of all the 4 switches. The transistors acting as switches have an "ON" resistance given by the triode region operations of the transistors.

$$R_{ON} = \frac{1}{\mu_n C_{ox} \left(W/L\right)(V_{GS} - V_T)} \tag{3.32}$$

Thus the value of resistances can be tuned in a larger range and this value needs to be equal to $1/g_m$. Thus the tuning range for the g_m is quite large. Fig. 3.21 shows the tuning range in terms of the transconductances and the biasing currents for this tuning circuit implementation.

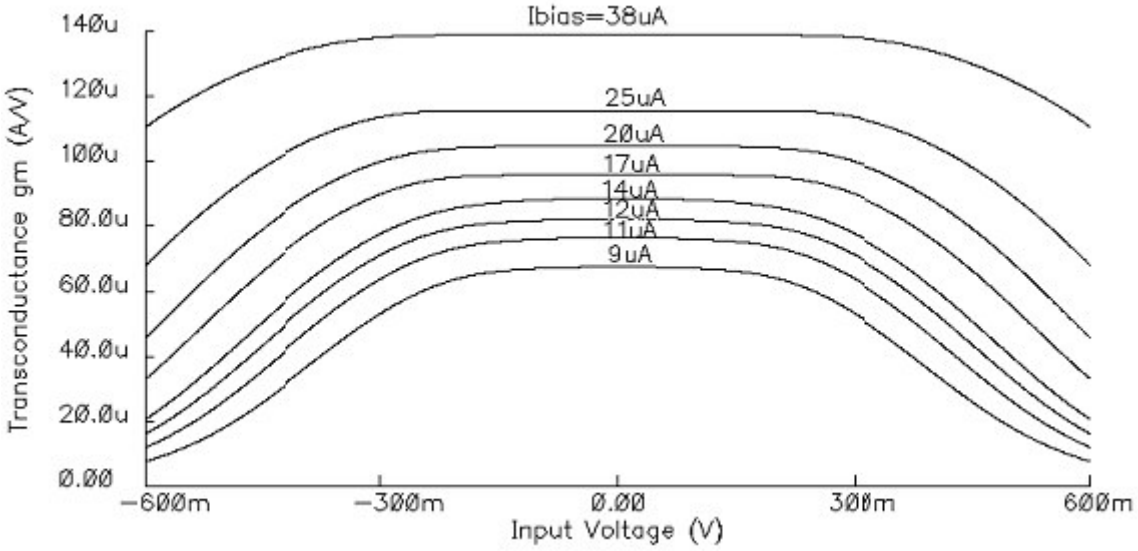


Fig. 3.21. Gm tuning from 70µA/V-140µA/V,of the OTA, using the biasing current

The flatness of the g_m values in all cases (70µA/V < g_m < 140µA/V) for a larger input voltage range indicates the linearity performance of the proposed OTA. To achieve better linearity the I_{bias} needs to be increased, cause the input range for higher bias currents is greater where the transconductance term is absolutely flat.

Tuning, mentioned above is achieved using a resistor bank and also switches. The resistors are passive ones and are laid out in Silicon using polysilicon covered by a resistor layer. The value of resistance obtained can vary due to process variations. The OTA's performance needs to be verified for the variations in the value of the resistors. For this the variations resistor values and its effect on the harmonic distortion is analyzed below. In order to analyze this, the HD_3 from the two tone measurement of the tunable OTA, using equal tones of 0.4V amplitudes at 9MHz and 10MHz can be measured for various % variations of the resistor values. Fig. 3.22 shows the effect of the % variation in the resistor values on the HD_3.

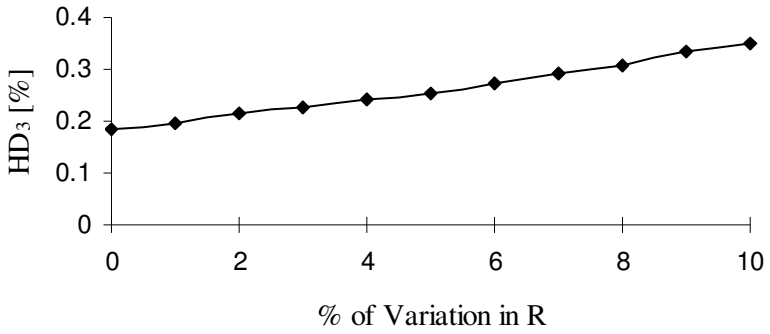


Fig. 3.22. Variations in HD_3 vs. % variations of the resistor values

From Fig. 3.22 the maximum variations in the third order harmonic distortion level for a 10% variation in the resistor value is around 5dB.

3.3.7 Measurement Results

The measurement results for the proposed OTA fabricated using CMOS 0.35µm process are presented below. The OTA is used to build a second order filter, having the same OTA at the output as a buffer. The biquad occupies 300µm*500µm. The power supply is ±1.25V. Fig. 3.23 shows the chip micrograph.

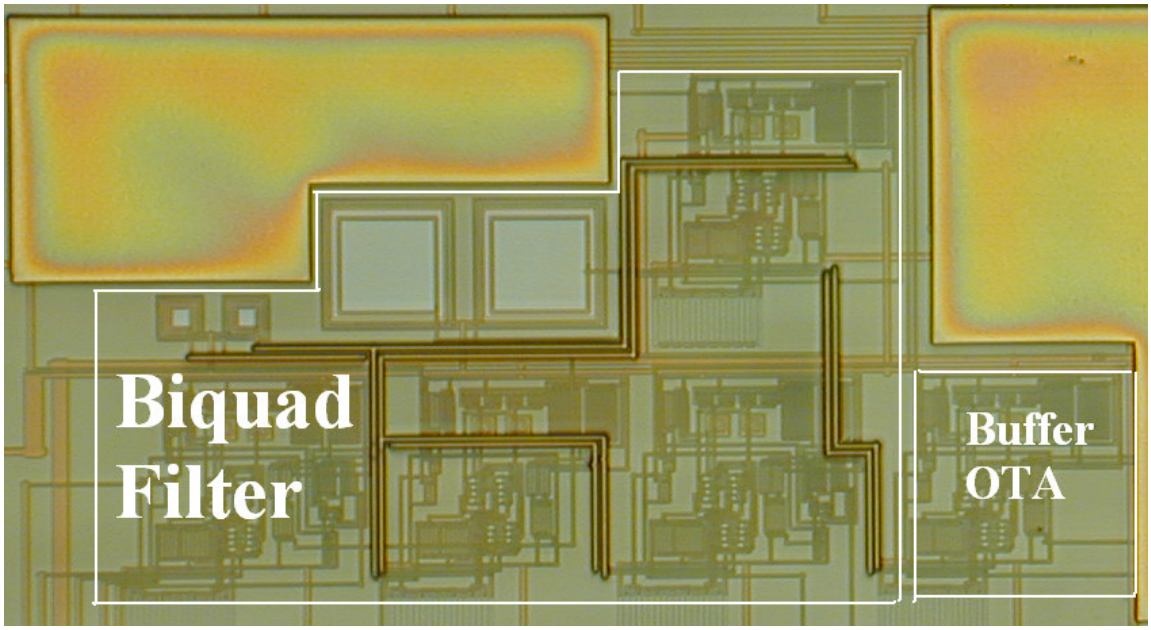


Fig. 3.23. Chip micrograph of the biquad filter along with the buffer OTA

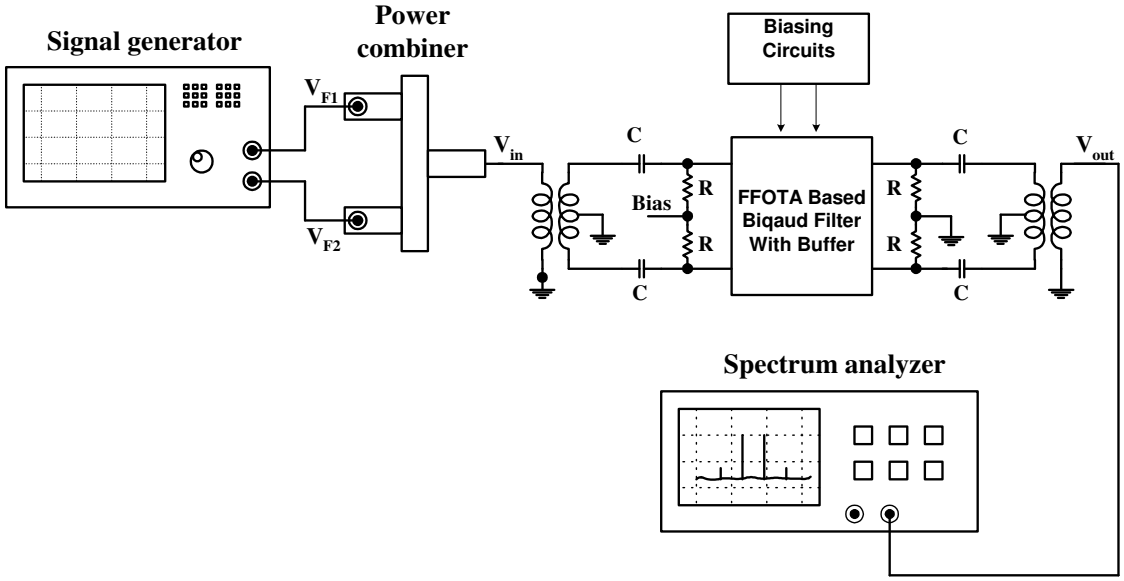


Fig. 3.24. Set-up to measure intermodulation distortion (IM_3, IM_5)

Fig. 3.24 shows the general set up to measure the IM_3 products. To measure linearity experimentally a two-tone analysis is used. Two signals of equal amplitude but different frequencies are generated using the signal generators and are combined together using the combiner and are fed to the Feedforward OTA based filter (FFOTA Based Filter). The output waveforms are plotted and from the third order intermodulation products terms the third order harmonic distortion (HD_3) can be extracted. It is known that the IM_3 is thrice that of the third order harmonics. The higher order harmonics can be neglected for analysis.

Fig. 3.25 shows the set-up for the measurement of the filter transfer function. The Agilent 4395A (Spectrum/Network Analyzer) can also be used as a network analyzer to measure the filter's transfer function.

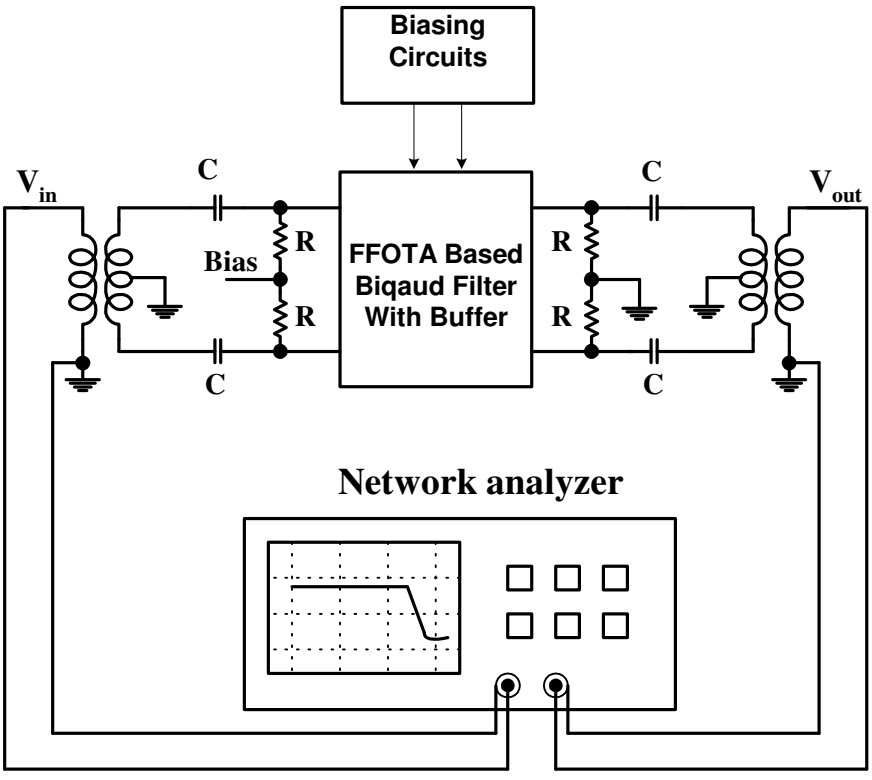


Fig. 3.25. Set-up for transfer function measurements

The feedforward OTA is used to build a second order low pass Butterworth filter whose 3dB frequency is 10MHz. Fig. 3.26 shows the filter's transfer function.

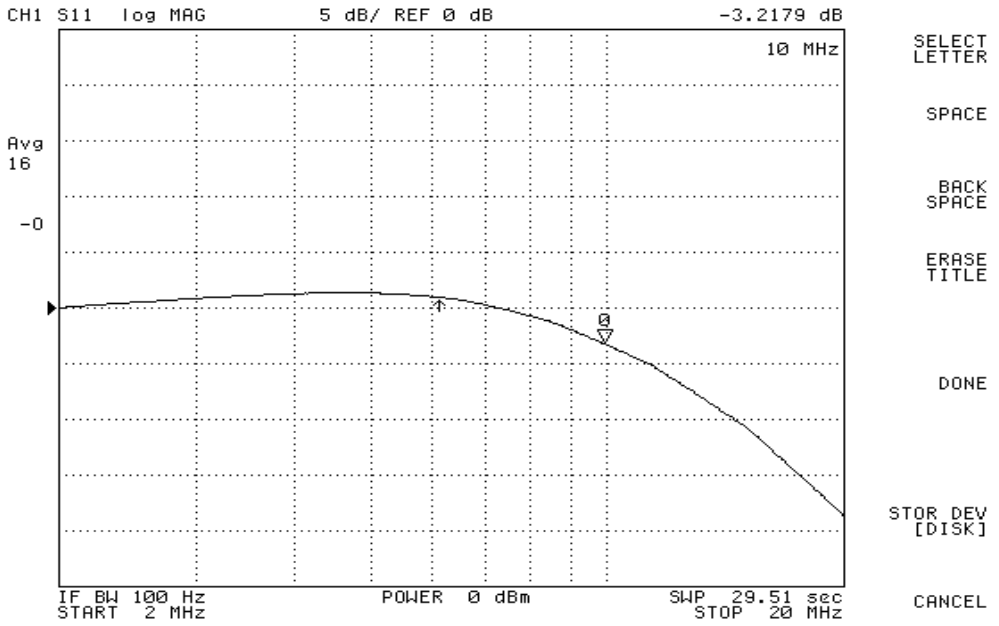


Fig. 3.26. Biquad filter transfer characteristic- magnitude response

Fig. 3.26 shows the filter's transfer characteristics. Taking into account for the buffer's gain, the overall small signal gain of the filter is 0dB and the gain at 10MHz, which is around the corner frequency is -3.21dB. The filter has a 3dB frequency around 10MHz.

Fig. 3.27 shows the two tone measurement results for the filter with two tones at 10MHz and 11MHz, for an input signal of 1.2Vpp at the maximum. The OTA has a very flat g_m performance up to ±0.6V input voltage, hence the linearity of the filter built using this OTA, is tested at the maximum voltage swing. The swing is limited by the

power supply which is ±1.25V. The IM_3 measured from the two tones at 10MHz and 11MHz is around -38dB and for two equal tones of 0.5V at 6MHz and 7MHz is -42dB.

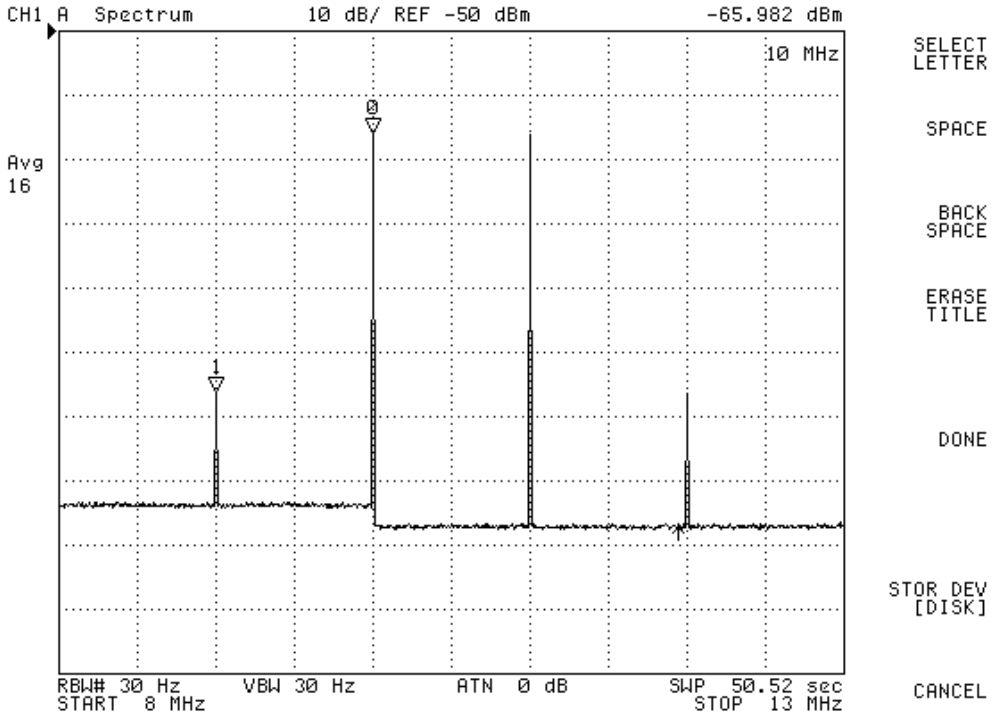


Fig. 3.27. IM_3 measurement for two equal tones of 0.6V at 10MHz and 11MHz

For the above mentioned measurement results, the resistor value used at the output of the buffer was 25Ω. This resulted in the value of the fundamental and the harmonics to be very low. In order to have a significant output signal, resistor values of 2KΩ was used. Fig. 3.28 and 3.29 shows the filter's magnitude response and the two tone measurement results for the filter with an output buffer of 2KΩ. This value of resistor along with the parasitic capacitances due to packaging shifted the corner

frequency, 3dB frequency to 8.2MHz. Hence for the measurement of the intermodulation products, two equal tones of 0.6V input amplitude at 6MHz and 7MHz were used as the input.

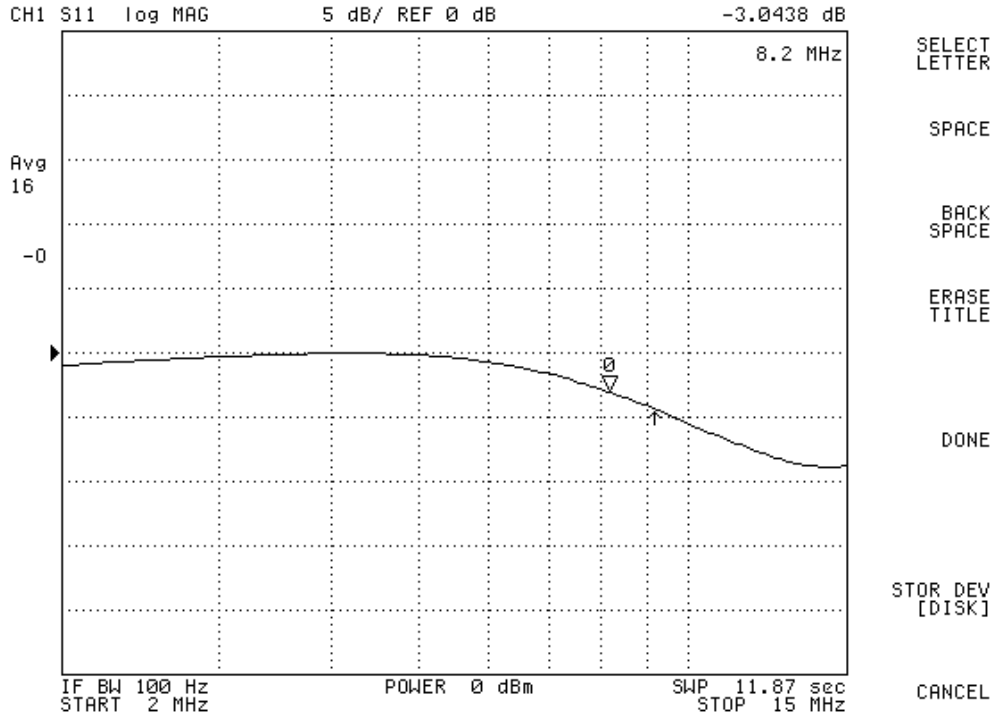


Fig. 3.28. Biquad filter's magnitude response for a 2KΩ resistor at the output of the buffer

Fig. 3.30 shows the experimental measurement of the variation of the HD_3 with respect to the input voltage amplitude for the filter at 10MHz. The variation of the third order harmonic term gives a good picture of the linearity performance of the OTA based filter.

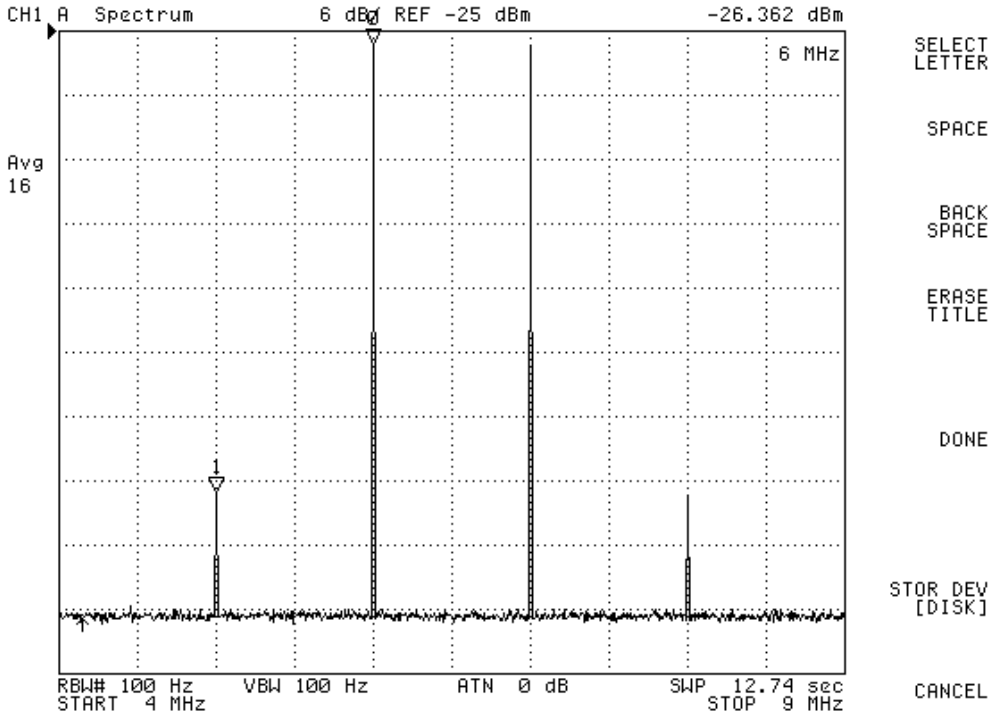


Fig. 3.29. Two tone measurement results for two equal tones of 0.5V amplitude at 6MHz and 7MHz for the biquad filter with 2KΩ at the output of buffer

The excess phase of the feedforward OTA is less 1^o , it is around 0.7^o. The excess phase can further be improved using an additional capacitor compensation across the drains of transistors $M_{3,4}$ and $M_{1,2}$. The CMRR, $PSRR_+$ and $PSRR_-$ of the biquad filter at 10MHz is around 80dB, 60.7dB and 42.21dB respectively. The power consumed by the single OTA is less than 1mW (≅ 0.94mW). The power consumed by the biquad filter along with the buffer OTA is 4.8mW. The power supply is ±1.25V. The bias current is set to 40μA. The total output noise generated in the bandwidth from 0 to 10MHz is

about 98μVrms. This corresponds to 72.6dB of dynamic range for the maximum input differential voltage of 1.2Vpp at 10MHz.

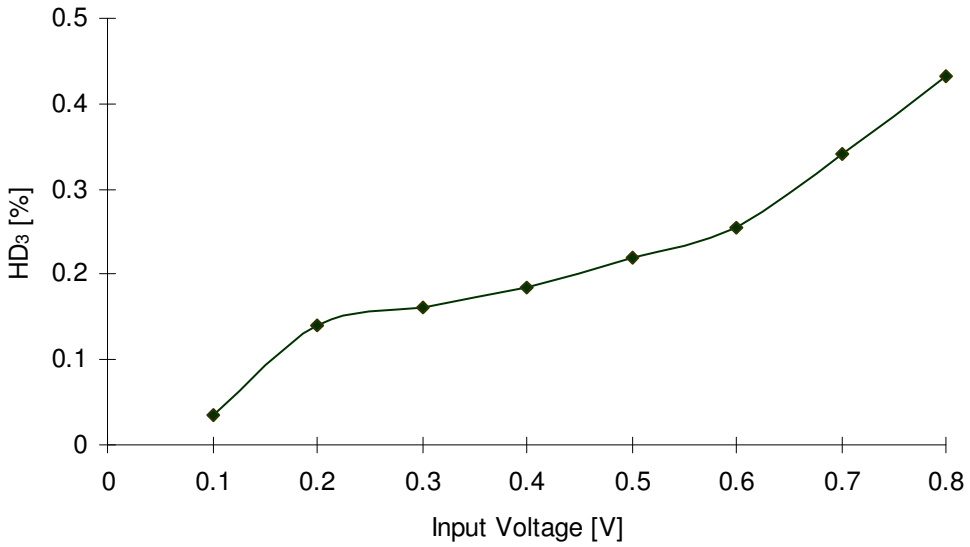


Fig. 3.30. HD_3 vs. input amplitude for an input signal at 10MHz for the biquad filter

Table 3.5 summarizes the performance of the filter. This research work is based on creating a new mechanism for improving the linearity of the OTA structure. For this case, a simple differential pair was taken as the reference OTA and using the active error feedforward technique the linearity of the simple differential pair was improved. If a differential pair, with know linearization techniques like source degeneration and/or signal attenuation using floating gates and cross coupling is used as the basic building OTA for the active-error feedforward technique, the performance of the overall OTA would be increased manifold.

Table 3.5. Filter Performance Parameters

Parameter	Measured Value
Filter Order & Type	2nd Butterworth Low Pass
F3dB	10MHz (25Ω At Buffer O/P) 8.2MHz (2KΩ)
IM3 & Max. Vin,pp	-38 dB for 1.2Vpp at 10MHz -42 dB for 1Vpp at 7MHz
Output Integrated Noise from 0-10MHz	98 µVrms
gm Tuning Range	70µA/V < *gm* < 150µA/V
SNR @ 1Vpp Input	71.15dB
SNDR @1Vpp Input for a THD of -50dB	46.5 dB
Power Supply	± 1.25V
Power Consumed	4.8mW
Power Per Pole	2.4mW
Area	300µm*500µm
Technology	CMOS 0.35µm

The performance of this OTA based filter is significantly better than using a simple differential pair based OTA. However the performance of this circuit when compared to the more complex schemes of linearization is not very significant, as the distortion ratio needs to be improved. The noise performance is very good however this when combined with the distortion ratio, reduces the SNDR of the filter. The main advantage of the technique is the savings in terms of power and area. Table 3.6 gives a comparison of the performance of this OTA based filter with some of the published works from the literature.

Table 3.6. Comparison of This Work with Published Material

Reference	Technology	Supply Voltage	IM3 @ Vin @Frequency	Power
JSSC 1991 [85]	CMOS 3 µm	5 V	-50 dB 2.4 Vpp 1 MHz	9mW p/pole
JSSC 1993 [97]	BiCMOS 2 µm	10 V	-65 dB 5 Vpp 4 MHz	157mW p/pole
CICC 1996 [98]	CMOS 0.8 µm	5 V	-61 dB 4 Vpp 0.6 MHz	5mW p/pole
JSSC 1997 [99]	CMOS 0.5 µm	3.3 V	-45 dB 1 Vpp 4 MHz	4mW p/pole
CICC [90]	CMOS 0.35 µm	3.3 V	<-65 dB 1.3 Vpp 20 MHz	26mW p/pole
This Work	CMOS 0.35 µm	2.5 V	-42 dB 1 Vpp 7 MHz	2.4mW p/pole

3.4. Conclusion

An effective linearization method based on the active-error feedforward concept has been developed for realizing a very linear CMOS OTA. The complete linearized OTA in differential-input two-output structure has been designed and fabricated using

the 0.35µm process. For a power supply of ±1.25V, total harmonic distortion for a 1MHz sinusoidal signal at 0.4Vpp is less than -72dB and the IM_3 for a maximum differential voltage swing of 1.2Vpp at 10MHz is -50dB (HD_3 = -59dB) and the same for simple differential pair is -35dB and around -10 to -15dB respectively. The circuit has very low power consumption, which is less than 1mW for bias current equal to 40µA. The obtained simulation results confirm that the linearity of the overall transconductance element is significantly improved in comparison to the reference circuit (i.e. simple differential pair transconductor).

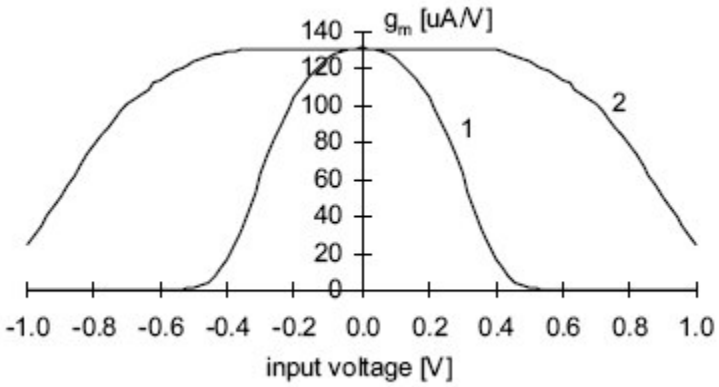


Fig. 3.31. Transconductance vs. input voltage (a) simple differential pair, (b) with linearization

Fig. 3.31 is the pictorial representation of the gain of this OTA. A significant increase of the linear input voltage range for the linearized circuit (>300%) was observed.

The OTA topology designed using the active-error feedforward technique was also used as the active building block in the design of a second order low pass filter with a 3dB frequency of 10MHz. The measured IM_3 of the filter is around -45dB over the entire pass band (1-10MHz) for a maximum input signal of 1.2Vpp. The active area of

the filter is 300µm*500µm (0.15µm^2). The filter design operates with a power supply of ± 1.25V. A SNR of 61.5dB was achieved for a maximum input signal sinusoid of 1.2Vpp at10MHz. The measured results assure the good performance of the proposed transconductance linearization technique.

A new topology of a highly linear OTA was introduced and the extension to its application in the case of a VDSL front end analog filter was also explained. The circuit has a very highly linear characteristic, when the price is paid off in terms of the noise shape. The power consumed is also around 20mW, which is not very high to achieve a linearity level of -75dB. This topology can be used in applications whose noise performance is not very highly demanding.

CHAPTER IV

CONCLUSION

In this thesis, the design issues continuous-time OTA-C based integrated filters have been examined. What mainly limit the performance of an analog filter are the non-idealities of the used building blocks and the circuit architecture, like the non-linearity, noise etc. A general description of non-linearity and noise modeling of OTA was presented.

A framework for performance optimization of continuous-time OTA-C filters was presented based on matrix description of a general OTA-C filter model. In particular, a general description of OTA-C filters with nonlinear transconductors was introduced. A nonlinear ordinary differential system that describes time evolution of output signal for an arbitrary OTA-C filter was formulated. The presented method allows carrying out an effective and fast transient analysis of any OTA-C filter using standard numerical methods and can be applied to determine the THD or other nonlinearity measures of filters containing nonlinear transconductors. On the other hand, universal expressions are derived that permit computing the filter noise. As an application, the optimal block sequencing and gain distribution for 8th order Butterworth filter in cascade realization was presented.

Two novel techniques to improve the linearity of OTA used in continuous time OTA-C filters were introduced. On the circuit level, new building blocks have been introduced.

A low gain highly linear filter for VDSL applications was introduced. The proposed design has a greater linearity performance, however the noise performance is affected by the loop gain of the amplifier.

A new topology of OTA based on active-error feedforward technique to improve the linearity of the OTA with minimum power consumption was also introduced. The

proposed architecture is shown to have significant area and power savings compared to the recently reported structures in the literature.

REFERENCES

[1] K.W.H. Ng, V.S.L. Cheung, and H. Luong, "A 3-V 44-MHz switched-capacitor bandpass filter for digital video application," *Proc. Int. Symp. Circuits Syst. (ISCAS),* Scottsdale, AZ, vol. 4, pp. 627-630, May 2002.

[2] S. Kiriaki, T. Lakshmi Viswanathan, G. Feygin, B. Staszewski, R. Person, B. Krenik, M. de Wit, and K. Nagaraj, "A 160-MHz analog equalizer for magnetic disk read channels," *IEEE J. Solid-State Circuits*, vol. 32, no. 11, pp. 1839-1850, Nov. 1997.

[3] K. Yido, H. Hyungki, C. Yongsik, L. Jeongwoo, P. Joonbae, L. K. Lee, J. Deog-Kyoon, and K. Wonchan, "A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 536-542, May 2002.

[4] C.D. Salthouse and R. Sarpeshkar, "A practical micropower programmable bandpass filter for use in bionic ears," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 63-70, Jan. 2003.

[5] I.R. Khan, M. Okuda and R. Ohba, "New designs of frequency selective FIR digital filters"*, Proc. Int. Symp. Circuits Syst. (ISCAS),* Bangkok, Thailand, vol. 4, pp. 25-28, May 2003.

[6] E. Sánchez-Sinencio and J. Silva-Martinez, *The Circuits and Filters Handbook: 2nd Edition: Switched Capacitor Filters*, Boca Raton, FL: CRC Press, 1995.

[7] E. Sánchez-Sinencio, J. Silva-Martinez, and R.L. Geiger, "Biquadratic SC filters with small GB effects," *IEEE Trans. Circuits and Systems*, vol. 31, no. 10, pp. 876-884, Oct. 1984.

[8] F. Taylor, "Block floating-point distributed filters", *IEEE Trans. Circuits and Systems*, vol. 31, no. 3, pp. 300-304, Mar. 1984.

[9] M.J. Schindler and Y. Tajima, "A novel MMIC active filter with lumped and transversal elements", *IEEE Trans on Microwave Theory and Techniques*, vol.-37, no. 12, pp. 2148-2153, Dec. 1989.

[10] S-S Lee and C.A. Laber, "A BiCMOS continuous-time filter for video signal processing applications", *IEEE J. Solid-State Circuits*, vol. 33, no. 9, pp. 1373-1382, Sept. 1998.

[11] L. Du, M. Spurbeck and R.T. Behrens, "A linearly constrained adaptive FIR filter for hard disk drive read channels", *IEEE International Conference on Communications* 1997, vol. 3, pp. 1613-1617, June 1997.

[12] T.M. Almaida and M.S. Piedade, "High performance analog and digital PLL design", *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Orlando, FL, vol. 4, pp. 394-397, June 1999.

[13] E. Sanchez-Sinencio, "Radio frequency wireless systems: basics and IC implementations", *Proceedings of the 5th IEEE International Caracas Conference on Devices, Circuits and Systems"*, vol. 1, pp. 1-4, Nov. 2004

[14] W.V. Subbarao, "Programmable bi-quad active filters for bio signal processing", *Proc. of the Annual International Conference on Engineering in Medicine and Biology Society"*, vol. 3, pp. 1100-1101, Nov. 1988.

[15] K. Peacock, "On the practical design of discrete velocity filters for seismic data processing", *IEEE Trans. Acoustics, Speech, and Signal Processing,* vol. 30, no. 1, pp. 52-60, Feb. 1982.

[16] P. Allemandou, "Transfer functions of RLC filters", *IEEE Trans. Circuits and Systems*, vol. 15, no. 4, pp. 483-485, Dec. 1968.

[17] S. Yoshimoto, Y. Yamamoto, Y. Takahashi and E. Otsuka, "Multi-band RF SAW filter for mobile phone using surface mount plastic package", *IEEE Proc. Ultrasonics Symposium*, vol. 1, pp. 113-118, Oct. 2002

[18] C.C.W. Ruppel, L. Reindl, and R. Weigel, "SAW devices and their wireless communications applications," *IEEE Microwave Magazine*, vol. 3, no.2, pp. 65-71, June 2002.

[19] R. Aigner, J. Ella, H.J. Timme, L. Elbrecht, W. Nessler and S. Marksteiner, "Advancement of MEMS into RF-filter applications", *Intl. Digest. Electron Devices Meeting*, San Francisco, CA, pp. 897-890, Dec. 2002.

[20] M..J. Golio, *The RF and Microwave Handbook*, Boca Raton, FL: CRC Press 2001.

[21] R. Geiger and G. Bailey, "Integrator design for high-frequency active filter applications", *IEEE Trans. Circuits and Systems*, vol. 29, no. 9, pp. 595-603, Sept. 1982.

[22] T. Deliyannis, Y. Sun, and J.K. Fildler, *Continuous-Time Active Filter Design*, Boca Raton, FL: CRC Press, 1999.

[23] S. Mitra and N. Herbst, "Synthesis of active RC one-ports using generalized impedance converters", *IEEE Trans. Circuits and Systems*, vol. 10, no. 4, pp. 532-632, Dec. 1963.

[24] J. Hutchison and F. Lee, "Some notes on practical FDNR filters", *IEEE Trans. Circuits and Systems*, vol. 28, no. 3, pp. 243-245, Mar. 1981.

[25] R.P. Sallen and E.L. Key, "A practical method of designing RC-active filters," *IEEE Trans. Circuit Theory*, vol. 2, pp. 74-85, Mar. 1955.

[26] J. Mahattanakul and C. Toumazou, "A theoretical study of the stability of high frequency current feedback op-amp integrators", *IEEE Trans. Circuit and Systems I: Fundamental Theory and Applications,* vol. 43, no. 1, pp. 2-12, Jan. 1996.

[27] R. Hogervorst, R. J. Wiegerink, P.A.L. de Jong, J. Fonderie, R.F. Wassenaar, and J.H. Huijsing, "CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage", *Proc. Int. Symp. Circuits Syst. (ISCAS),* San Diego, CA, vol. 6, pp. 2876-2879, May 1992.

[28] J.H. Botma, R.F. Wassenaar and R.J. Wiegerink, "A low voltage CMOS Opamp with a rail-to-rail constant gm input stage and a class AB rail-to-rail output stage", *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Chicago, IL, vol. 2, pp. 1314-1317, May 1993

[29] A. Katz, "Linearization: reducing distortion in power amplifiers", *IEEE Microwave Magazine*, vol. 2, no. 4, pp. 37-49, Dec. 2001

[30] Z.Y. Chang, D. Haspeslagh, J. Boxho and D. Macq, "A highly linear CMOS Gm-C bandpass filter for video applications," *Proc. IEEE Custom Integrated Circuits Conf.*, San Diego, CA, pp. 89-92, 1996.

[31] H. Schmid, "Why the terms current mode and voltage mode neither divide nor qualify circuits", *Proc. Int. Symp. Circuits Syst. (ISCAS),* Scottsdale, AZ, vol. 2, pp. 29-32, May 2002.

[32] W.M. Snelgrove and A.S. Sedra "Optimization of dynamic range in cascade active filters," *Proc. Int. Symp. Circuits Syst. (ISCAS)*, New York, NY, pp. 151-155. May 1978.

[33] F.C. Nunes and J.E. Franca, "Continuous-time leapfrog filter with precise successive approximation tuning", *Proc. Int. Symp. Circuits Syst. (ISCAS),* Chicago, IL, vol. 2, pp. 1271-1273, May 1993.

[34] K.R. Laker, R. Schaumann and M.S. Ghausi, "Multiple-loop feedback topologies for the design of low-sensitivity active filters," *IEEE Trans. Circuits & Systems*, vol. 26, pp. 1-21, Jan. 1979.

[35] W.V. Kenzle, "FIESTA-II a software tool for electronic filter design," M.S. thesis, Texas A&M University, College Station, 1997.

[36] P.O. Brackett and A.S. Sedra, "Direct SFG simulation of LC ladder networks with applications to active filter design," *IEEE Trans. Circuit & Systems*, vol. 23, pp. 61-67, Feb. 1976.

[37] C. Acar and M.S. Ghausi "Design of high-order active filters in integrated circuits," *IEEE J. Solid-State Circuits*, vol. 13, no. 2, pp. 273-276, April 1978.

[38] K. Martin and A.S. Sedra, "Design of signal-flow graph (SFG) active filters," *IEEE Trans. Circuit & Sytems*, vol. 25, pp. 185-195, April 1978

[39] B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York: McGraw-Hill, 2001.

[40] A.N. Mohieldin, "High performance continuous-time filters for information transfer systems", Ph.D Dissertation at Texas A&M University, College Station.

[41] C-C. Chang, M-T. Shieu and C-K. Wang, "A VLSI architecture of DMT based transceiver for VDSL system", *IEEE Asia-Pacific Conference on ASIC*, Taipei, Taiwan, pp. 363-366, Aug. 2002.

[42] S. Mehrmanesh and M. Atarodi, "A high dynamic range CMOS variable gain filter for ADSL," *Proc. Int. Symp. Circuits Syst. (ISCAS),* Scottsdale, AZ, vol. 4, pp. 257-260, 2002.

[43] W. Dehaene, M.S.J. Steyaert, and W. Sansen, "A 50-MHz standard CMOS pulse equalizer for hard disk read channels," *IEEE J. Solid-State Circuits*, vol. 32, pp. 977-988, July 1997.

[44] R. Schaumann, M.S. Ghausi, and K.R. Laker, *Design of Analog Filters, Passive, Active RC, and Switched Capacitor,* Englewood Cliffs, NJ: Prentice-Hall, 1990.

[45] R.L. Geiger and E. Sánchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuit and Devices Mag.*, vol. 1, pp. 20-32, 1985.

[46] B. Nauta, *Analog CMOS Filters for Very High Frequencies*, Boston, MA: Kluwer Academic Publishers, 1993.

[47] Y. Sun (Editor), *Design of High Frequency Integrated Analogue Filters*, London: The Institution of Electrical Engineers, 2002.

[48] E. Sánchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," *IEE Proc.-Circ. Dev. Syst.*, vol. 147, No. 1, pp. 3-12, Feb. 2000.

[49] S. Koziel and S. Szczepanski, "Structure generation and performance comparison of canonical elliptic G_m-C filters," *Proc. Int. Conf. Electron. Circuits Syst., ICECS*, Dubrovnik, Croatia, vol. 1, pp. 157-160, 2002.

[50] S. Koziel, S. Szczepanski, and R. Schaumann, “General approach to continuous-time G_m-C filters,” *Int. J. Circuit Theory Appl.*, vol. 31, pp. 361-383, July/Aug. 2003.

[51] Y.P. Tsividis, “Integrated continuous-time filter design - An overview,” *IEEE J. Solid-State Circuits*, vol. 29, pp. 166-176, 1994.

[52] S. Mehrmanesh, M.B. Vahidfar, H.A. Aslanzadeh and M. Atarodi, ”An ultra low-voltage Gm-C filter for video applications,” *Proc. Int. Symp. Circuits Syst. (ISCAS),* Bangkok, Thailand, vol. 1, pp. 561-564, 2003.

[53] Y. Palaskas and Y. Tsividis, ”Dynamic range optimization of weakly nonlinear, fully balanced, Gm-C filters with power dissipation constraints,” *IEEE Trans. Circuits Syst.-II*, vol. 50, no. 10, pp. 714-727, Oct. 2003.

[54] E. Sánchez-Sinencio, Class Notes for the course ELEN 622 Active Network Synthesis, Texas A&M University, College Station.

[55] S.A. El-Hamamsy and R.A. Fisher, “Inclusion of nonlinear output capacitor behavior in zero-voltage switched circuit design”, *IEEE Conf. Power Electronics Specialists*, vol. 2, pp. 1424-1430, June 1997.

[56] P.K.D. Pai and A.A. Abidi, “A 40-mW 55 Mb/s CMOS equalizer for use in magnetic storage read channels,” *IEEE J. Solid-State Circuits*, vol. 29, pp. 489-499, Mar. 1994.

[57] H. Khorramabadi, M.J. Tarsie, and N.S. Woo, “Baseband filters for IS-95 CDMA receiver applications featuring digital automatic frequency tuning,” in *Int. Solid State Circuits Conf.*, San Francisco, CA, pp. 172-173, 1996.

[58] A. Hassan, K. Sharaf, and H. El-Ghitani, H.F. Ragai, ”The design and implementation of a bandpass Gm-C filter for Bluetooth,” *Proc. Midwest Symp. on Circuits Syst., MWSCAS*, Tulsa, OK, vol. 2, pp. 629-632, 2002.

[59] S. Mehrmanesh and H.A. Aslanzadeh, M.B. Vahidfar and M. Atarodi, ”A 1.8V high dynamic range CMOS Gm-C filter for portable video systems,” *Proc. Int. Conf. Microelectronics, ICM*, Beirut, Lebanon, pp. 38-41, 2002.

[60] W. Jendernalik and S. Szczepanski, ”A CMOS OTA-C channel-select filter for mobile receiver,” *Proc. Int. Conf. Circuits Syst. Comm., ICCSC*, St. Petersburg, Russia, pp. 50-53, 2002.

[61] A.A. Emira and E.Sánchez-Sinencio, ”A pseudo differential complex filter for Bluetooth with frequency tuning,” *IEEE Trans. Circuits Syst. II*, vol. 50, no. 10, pp. 742-754, 2003.

[62] S. D'Amico and A. Baschirotto, ”0.18-μm CMOS Gm-C digitally tuned filter for telecom receivers,” *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Bangkok, Thailand, vol. 1, pp. 493-496, 2003.

[63] J. Shin, S. Min, S. Kim, J. Choi, S. Lee, H. Park and J. Kim, ”3.3-V baseband Gm-C filters for wireless transceiver applications,” *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Bangkok, Thailand, vol. 1, pp. 457-460, 2003.

[64] G.W. Roberts and A.S. Sedra, “A general class of current amplifier-based biquadratic filter circuits,” *IEEE Trans. Circuits Syst.-I*, vol. 38, pp. 257-263, 1992.

[65] S. Koziel and S. Szczepanski, ”Dynamic range comparison of voltage-mode and current-mode state-space G_m-C biquad filters in reciprocal structures,” *IEEE Trans. Circuits Syst.-I*, vol. 50, no. 10, pp. 1245-1255, 2003.

[66] S. Szczepanski and R. Schaumann, “Nonlinearity induced distortion of the transfer function shape in high-order OTA-C filters,” *Analog Integrated Circuits and Signal Processing*, vol. 3, pp. 143-151, 1992.

[67] Z.Q. Liang and S.A. Billings, “Evaluation of output frequency responses of nonlinear systems under multiple inputs,” *IEEE Trans. Circuits Syst.-II*, vol. 47, pp. 28-38, 2000.

[68] P. Wambacq, G.E. Georges, Gielen, P.R. Kinget and W. Sansen, “High frequency distortion analysis of analog integrated circuits”, *IEEE Transactions on Circuits and Systems-II, Analog and Mixed Signal Processing,* vol. 46, no. 3, pp. 335-345, Mar. 1999.

[69] J. Mahattanakul and C. Bunyakate, “Harmonic injection method: a novel method for harmonic distortion analysis,” *Proc. Int. Symp. Circuits Syst. ISCAS*, Sydney, Australia, vol. 3, pp. 85-88, 2001.

[70] A. Brambilla, G. Espinosa, F. Montecchi and E. Sánchez-Sinencio, ”Noise optimization in operational transconductance amplifier filters,” *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Portland, OR, vol. 1, pp. 118 -121, 1989.

[71] G. Ejthivoulidis, L. Toth and Y.P. Tsividis, ”Noise in Gm-C filters,” *IEEE Trans. Circuits Syst.*, vol. 45, no. 3, pp. 295-302, Mar. 1998.

[72] A.S. Korotkov and R. Unbehauen, ”Calculation and estimation of noise in all-pole G_m-C filters,” *Int. J. Electron. Commun.*, vol. 53, no. 3, pp. 151-154, 1999.

[73] K.A. Mezher and P. Bowron, ”Noise-flow-graph analysis of OTA-C filters,” *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Sydney, Australia, vol. 1, pp. 695-698, 2001.

[74] Z. Fortuna, B. Macukow and J. Wąsowski, *Metody Numeryczne,* Warszawa, Poland: WNT, 1993.

[75] P. Kallam, E. Sánchez-Sinencio and A. Karsilayan, "An enhanced adaptive Q tuning scheme for a 100MHz fully symmetric OTA based band pass filter", *IEEE J. Solid-State Circuits*, vol. 38, pp. 585-593, 2003.

[76] G.S. Moschytz and P. Horn, *Active Filter Design Handbook*, Chichester, NY: John Wiley & Sons, 1981.

[77] K.L. Su, *Analog Filters,* Norwell, MA: Kluwer Academic Publishers, 2002.

[78] S. Szczepanski, S. Koziel and E. Sánchez-Sinencio, "Linearized CMOS OTA using active-error feedforward technique", *Proc. Int. Symp. Circuits Syst.(ISCAS),* Vancouver, Canada, vol. 1, pp. 549-552, 2004.

[79] A.N. Mohieldin, E. Sánchez-Sinencio and J. Silva-Martinez, "Nonlinear effects in pseudo differential OTAs with CMFB", *IEEE Transactions on Circuits and Systems-II, Analog and Digital Signal Processing*, vol. 50, no. 10, pp. 762-770, Oct. 2003

[80] A.N. Mohieldin, E. Sánchez-Sinencio and J. Silva-Martinez, "A fully balanced pseudo differential OTA with common mode feedforward and inherent common mode feedback detector", *IEEE J. Solid-State Circuits*, vol. 38, pp. 663-668, April 2003

[81] E. Luneburg and S.R. Cloude, "Contractions, Hadamard products and their application to polarimetric radar interferometry", *IEEE Proceedings of Geoscience and Remote Sensing Symposium,* vol. 4, pp. 2224-2226, July 1009

[82] R.G. Meyer, R. Eschenbach and W. Edgerley, "A wide-band feedforward amplifier," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 6, pp. 422-428, Dec. 1974.

[83] E.E. Eid, F.M. Ghannouchi and F. Beauregard, "Optimal feedforward linearization system design," *Microwave Journal*, vol. 38, no. 11, pp. 78–86, Nov. 1995.

[84] P.B. Kenington and D.W. Bennett, “Linear distortion correction using a feedforward system”, *IEEE Trans. On Vehicular Tech.*, vol. 45, no. 1, pp. 74-81, Feb. 1996.

[85] J. Silva-Martínez, M.S.J. Steyaert, and W. Sansen, “A large-signal very low distortion for high-frequency continuous-time filters,” *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 946-955, July 1991.

[86] M.D. Nava and C. Del-Toso, “A short overview of the VDSL system requirements”, *IEEE Communications Magazine,* vol. 40, issue: 12, pp. 82-90, Dec. 2002.

[87] N. Tan, F. Caster, C. Eichrodt, S.O. George, B. Horng and J. Zhao, “A universal quad AFE with integrated filters for VDSL, ADSL, and G.SHDSL”, *Proc. IEEE Custom Integrated Circuits Conf.,* San Jose, CA, pp. 599-602, Sept. 2003.

[88] J. Ramírez-Angulo, R.G. Carvajal, J. Tombs, and A. Torralba, “Low-voltage CMOS Opamp with rail-to-rail input and output signal swing for continuous-time signal processing using multiple-input floating gate transistors,” *IEEE Trans. on Circuits and Systems-II*, vol. 48, no. 1, pp. 111-116, Jan. 2001.

[89] A. Veeravalli, E. Sánchez-Sinencio and J. Silva-Martinez, “Transconductance amplifier structures with very small transconductances: a comparative design approach”, *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 770-775, June 2002.

[90] A. Lewinski and J. Silva-Martinez, “OTA linearity enhancement technique for high frequency applications with IM3 below -65dB”, *Proc. IEEE Custom Integrated Circuits Conf.,* San Jose, CA, pp. 9-12, Sept. 2003.

[91] K. Bult and H. Wallinga, ”A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation,” *IEEE J. Solid-State Circuits*, vol. 22, no. 3, pp. 357-365, June 1987.

[92] E. Sánchez-Sinencio, Class Notes for the course ELEN 607 Advanced Analog Circuits, http://amesp02.tamu.edu/~sanchez, Texas A&M University, College Station.

[93] W-K. Chen, "*The Circuits and Filters Handbook"*, 2nd ed., Boca Raton, FL: CRC Press, 2003.

[94] G.O. Romero and J. Silva-Martinez, "A folded-cascode OTA based on complementary differential-pairs for HF applications", *Third International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, pp. 57-6, July 1999.

[95] S. Koziel, A. Ramachandran, S. Szczepanski and E. Sánchez-Sinencio, "Dynamic range, noise and linearity optimization of continuous-time OTA-C filters", presented at the *IEEE International Conference on Electronics, Circuits and Systems*, Israel, Dec. 2004.

[96] C.H.J. Mensink and B. Nauta, "CMOS tunable linear current divider", *Electron. Lett*, vol. 32, no. 10, pp. 889-890, May 1996.

[97] S.D. Willingham, K.W. Martin and A. Ganesan, "A BiCMOS low-distortion 8-MHz low-pass filter", *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1234-1245, Dec. 1993.

[98] Z.Y. Chang, D. Haspeslagh, J. Boxho and D. Macq, " A highly linear CMOS Gm-C bandpass filter for video applications", *Proc. Custom Integrated Circuits Conf.,* San Diego, CA, pp. 89-92, May 1996.

[99] C.H.J. Mensink, B. Nauta and H. Wallinga, "A CMOS "soft-switched" transconductor and its application in gain control and filters", *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp.989-998, July 1997.

[100] P. Pessl, R. Gaggl, J. Hohl, D. Giotta and J. Hauptmann, "A four-channel ADSL2+ analog front-end for CO applications with 75 mW per channel, built in 0.13µm CMOS", *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2371-2378, Dec. 2004

[101] S. Oswal, F. Mujica, S. Prasad, R. Srinivasa, B. Sharma, et.al, "An integrated ADSL CPE analog front-end in a 0.13µm CMOS SOC", *Int. Solid State Circuits Conf.*, San Francisco, CA, vol. 1, pp. 404-535, 2004.

[102] B. Xia, S. Yan and E. Sánchez-Sinencio, "An RC time constant auto-tuning structure for continuous time ∑Δ modulators and active filters", *IEEE Trans. Circuits and Systems*, vol. 51, no. 11, pp. 2179-2188, Nov. 2004.

[103] P.K.D. Pai, A.D. Brewster and A.A. Abidi, "A 160-MHz analog front-end IC for EPR-IV PRML magnetic storage read channels," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1803–1816, Nov. 1997.

[104] E. Sánchez-Sinencio and J. Silva-Martínez, "CMOS transconductance amplifiers, architectures and active filters: A tutorial," *Proc. Inst. Elect. Eng. Circuits Devices Systems*, vol. 147, no. 1, pp. 3–12, 2000.

APPENDIX A

THE MODELING TOOL-MANUAL

1. Introduction

A brief manual mentioning the various steps to be taken to run the modeling tool is given in this section. The steps include, determining the various inputs for the tool like the non-linear parameters, noise parameters and the other filter specifications. A specific example of the tool, the non-linearity and noise analysis of a 5^{th} order Bessel filter, is mentioned in this section.

2. Non-Linearity Parameter Extraction

The general input-output relation of a non-linear system can be described by equation (A.1).

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + a_4 x^4(t) + a_5 x^5(t) + ... \quad (A.1)$$

where a_1 is the linear term and the other coefficients a_i ($i > 2$) are the higher order non-linear coefficients. The extraction process involves the determination of these higher order terms. This will give a picture of the non-linear behavior of the system.

The main focus of this research is to model the OTA's for its non-linearity and noise performance. The OTA is differential in nature. The main advantage of the differential system is that the even order harmonics are eliminated ideally, i.e. the even order coefficients a_2, a_4 etc are all ideally equal to 0. However in actual circuit design, these terms are not equal to 0 but are very small and negligible. It is very essential to determine all the terms. For an OTA the first order term a_1 is defined as the linear transconductance of the OTA (g_m).

To extract these terms, the conventional way is to use the simulator tools like CADENCE, where the input-output DC characteristic is taken and differentiated each

time and the value for x=0 is estimated and thus these terms can be extracted. The method of using CADENCE for the same is explained below.

The DC characteristic of an OTA, giving the non-linear relation between the input differential voltage and the output current can be given as in (A.2).

$$i_{out} = g_1 v_d + g_2 v_d^2 + g_3 v_d^3 + g_4 v_d^4 + g_5 v_d^5 + \ldots \quad (A.2)$$

where as mentioned before, g_2, g_4 are very small (negligible). The DC characteristic for the OTA mentioned in chapter II [75] is shown in Fig. A.1.

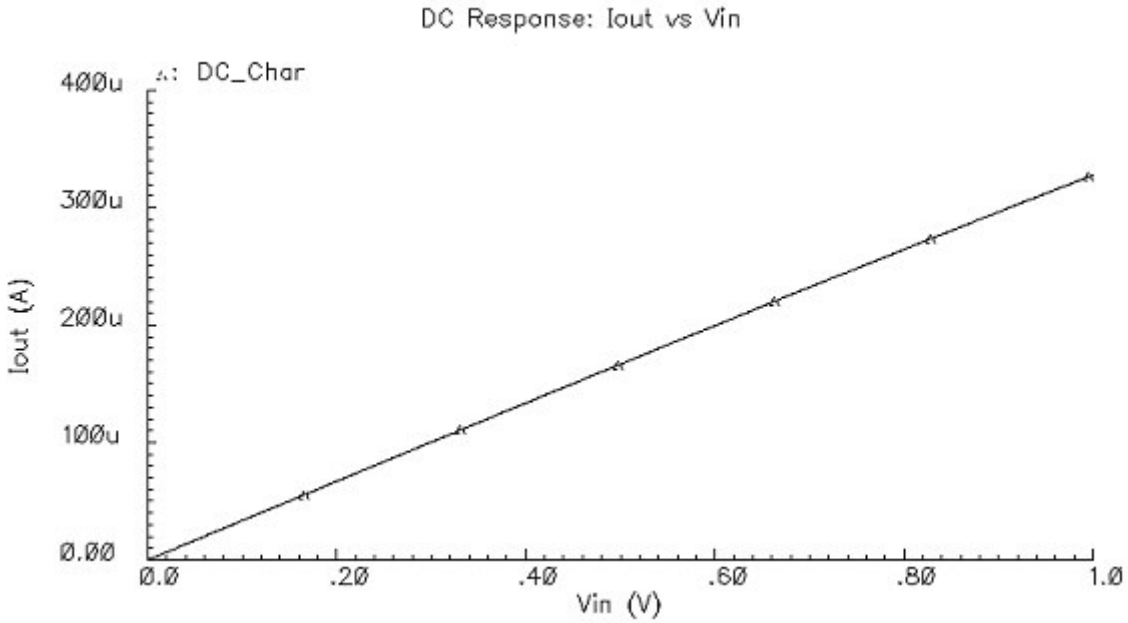


Fig. A.1. Non-linear DC characteristic: input-output relation for the OTA [75]

From the DC characteristic, the higher order coefficients can be determined by differentiating the response, which is characterized by (A.2) and equating the term to the point where v_d=0.

Equation set (A.3) gives the exact relation for all the coefficients with respect to the DC characteristic.

$$g_1 = \left.\frac{\partial i_{out}}{\partial v_d}\right|_{vd=0} ;\ g_2 = \frac{1}{2}\left.\frac{\partial^2 i_{out}}{\partial {v_d}^2}\right|_{vd=0} ;\ g_3 = \frac{1}{6}\left.\frac{\partial^3 i_{out}}{\partial {v_d}^3}\right|_{vd=0}$$
$$g_4 = \frac{1}{24}\left.\frac{\partial^4 i_{out}}{\partial {v_d}^4}\right|_{vd=0} ;\ g_5 = \frac{1}{120}\left.\frac{\partial^5 i_{out}}{\partial {v_d}^5}\right|_{vd=0} \qquad \text{(A.3)}$$

Fig. A.2, A.3 shows the extraction of these parameters based on equation (A.3), using CADENCE.

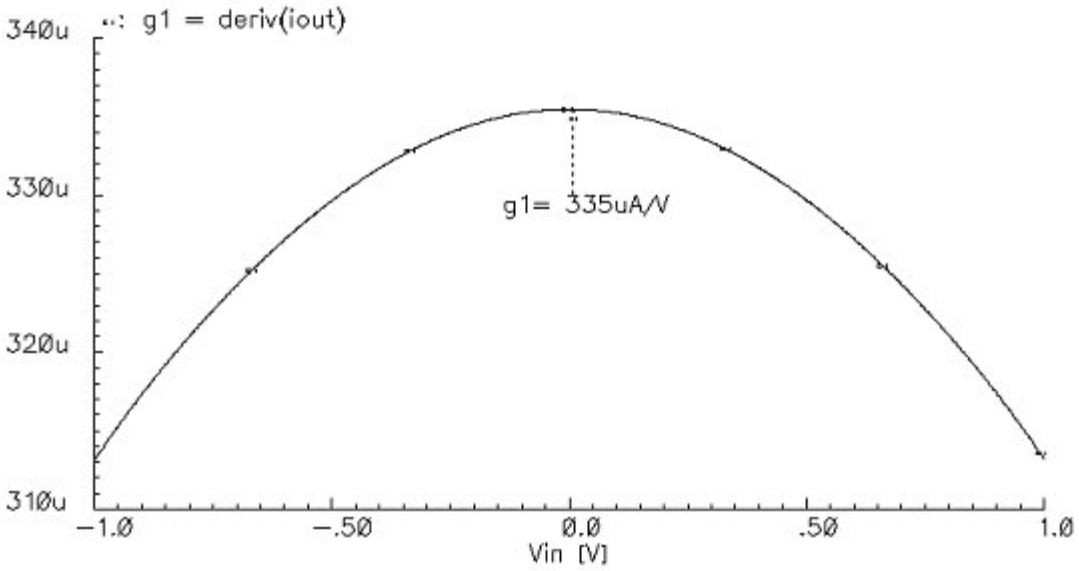


Fig. A.2. Extraction of g_1 from the nonlinear DC characteristic of the OTA [75]

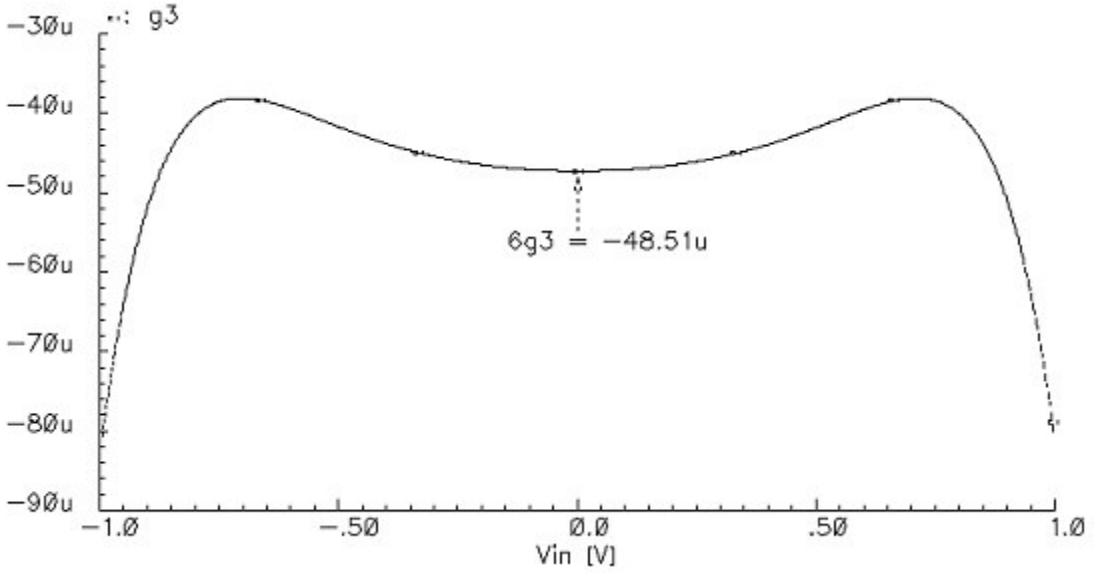


Fig. A.3. Extraction of g_3 from the nonlinear DC characteristic of the OTA [75]

The process of extraction of these parameters using the modeling tool is by using a simpler approach of curve fitting. From the DC characteristic of the OTA, N pairs of points (v_k,i_k) are taken and using the least mean square approach the coefficients are extracted. An approximation function, given by equation (A.4), is used.

$$G(v_{in}) = \sum_{i=0}^{N} g_i v_{in}^{\,i} \tag{A.4}$$

The parameters are extracted by minimizing the error function given by equation (A.5).

$$\xi = \sum_{k=1}^{N} [G(v_k) - i_k]^2 \tag{A.5}$$

The parameters extracted using CADENCE and also the modeling tool are compared in Table A.1. From the % error it can be concluded that the modeling tool's approach of extracting the nonlinear parameters is a very accurate.

Table A.1. Nonlinear Parameters Extraction

Nonlinear Coefficients	Transistor Level	This Approach (LMS)	% Error
$g_1(\mu A/V)$	142.65	142.71	0.042
$g_3(\mu A/V^3)$	-5.568	-5.572	0.071
$g_5(\mu A/V^5)$	-16.95	-17.08	0.77

* g_2 and g_4 are small enough to be considered negligible

These higher order coefficients also vary with biasing conditions. A brief description is given on the variations of these higher order coefficients based on the biasing condition. The OTA used for this example is the OTA discussed in chapter II [75]. To control the amount of source degeneration there is a biasing voltage V_{bias} which is fed to the gate of the transistors which operates in the triode region. By varying this voltage, the variations in these coefficients can be analyzed.

Fig. A.4 and A.5 shows the variation of the coefficients g_1 and g_3 with respect to the bias voltage. Fig. A.4 also shows how the transconductance of the OTA can be increased or varied using the bias voltage.

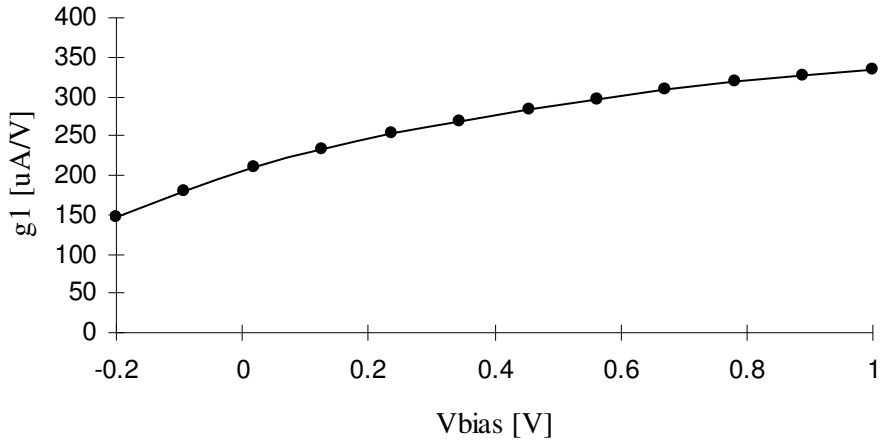


Fig. A.4. Variation of g_1 with respect to V_{bias} for the linear OTA [75]

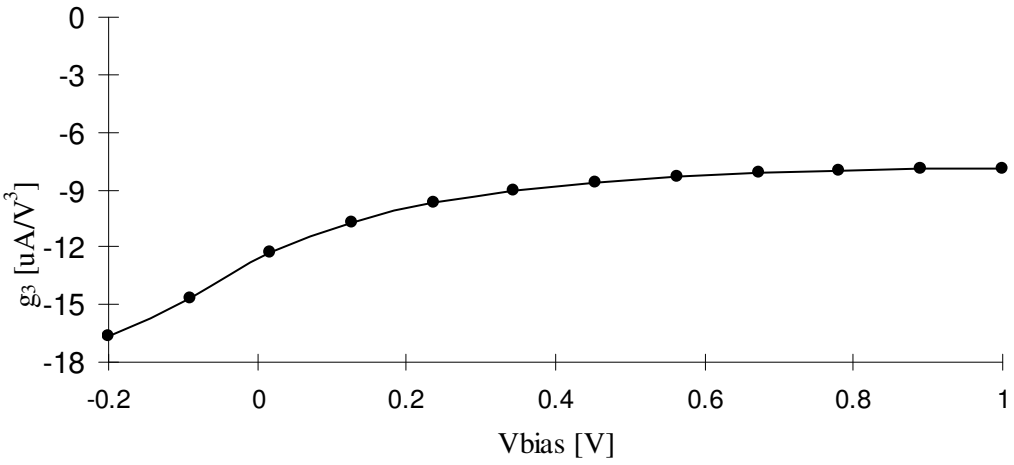


Fig. A.5. Variation of g_3 with respect to V_{bias} for the linear OTA [75]

3. Noise Parameter Extraction

The noise parameters required by the tool for modeling the noise of the whole filter are the two parameters S_w and S_f which is given by expression (A.6).

$$S_w = g_1 \frac{S_{n1} f_1 - S_{n2} f_2}{f_1 - f_2} \quad S_f = \frac{(S_{n1} - S_{n2}) f_1 f_2}{f_2 - f_1} \tag{A.6}$$

The terms S_{n1} and S_{n2} are the values of the noise spectral density at frequencies f_1 and f_2 respectively. The noise simulation can be performed in simulator tools like CADENCE and from the input squared noise response, the values of (S_{n1},f_1) and (S_{n2},f_2) can be extracted. The term g_1 is the linear transconductance of the OTA used. For this filter the corner frequency is around 10MHz and the flicker noise components are not very critical, hence the value of S_f can be taken as 0. Fig. A.6 shows the noise simulation window from CADENCE. The value of S_w estimated using this extraction is 8.17×10^{-20} VA/Hz.

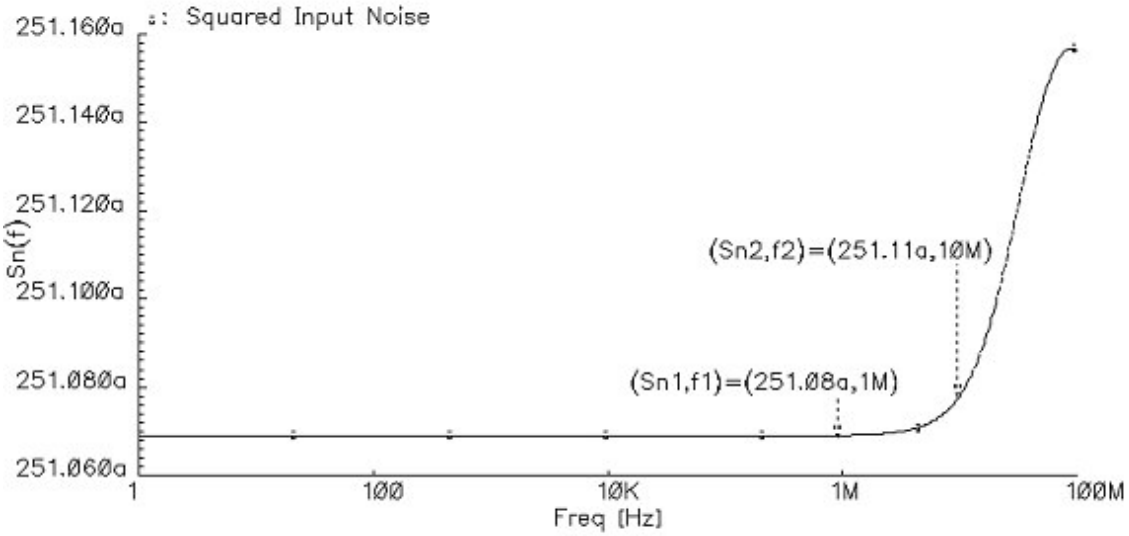


Fig. A.6. Noise simulation in CADENCE to extract the noise parameters

The procedure to estimate the non-linear parameters and the noise parameters for any OTA to be modeled was described in the above sections. For the tool to model the non-linearity and noise performance for any filter, the next set of information required is the basic specifications of the filter, like the corner frequency, signal amplitude for the estimation of *THD, HD_3* etc, also the various possible topologies.

To describe the various topologies, the matrix description of the topologies is required along with the values of the capacitors for the topologies. The matrix description of any Gm-C filter was explained in chapter II. Using the information, the matrix description for the a particular case is considered.

To design a 5th order Bessel low pass filter based on Gm-C structures, there are 50 different topologies which includes the various cascade topologies, leapfrog and also multiple feedback ones. The matrix description of each of these structures needs to be evaluated and put as a separate input file for the tool. Fig. A.7 shows the cascade structure (2:2:1) which is designed using two biquads followed by a first order structure.

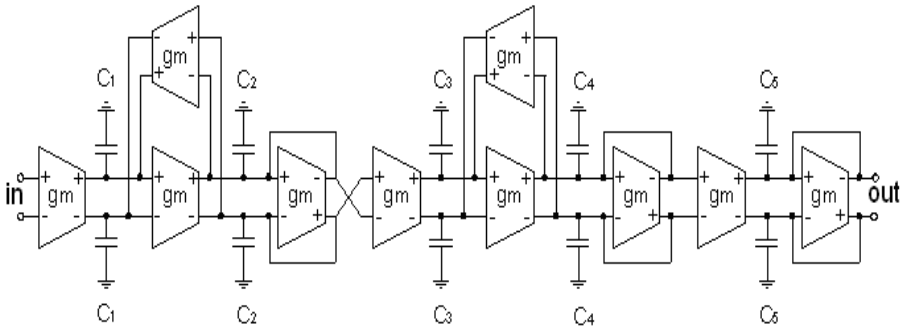


Fig. A.7. Cascade implementation of the 5th order Bessel filter using OTA [75]

The matrix description of this cascade implementation is shown in expression (A.7). The normalized capacitor values for this structure are 0.256, 0.215, 0.470, 0.150, 0.274.

$$\begin{matrix} 0 & -1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & -1 \end{matrix} \tag{A.7}$$

A GUI version of the tool was created using MATLAB which has some options for the user. The directory where the tool is executed should have the files containing all the matrices for the various topologies, their corresponding normalized capacitor values and an input file which has the DC characteristics along with the noise parameters S_w and S_f. A typical input menu would look like Fig. A.8.

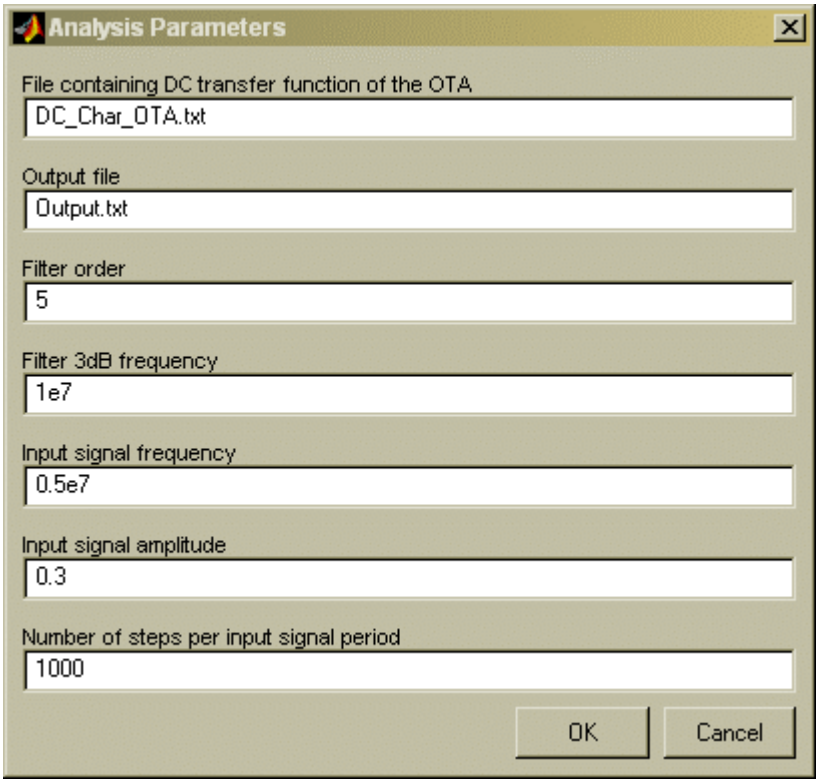


Fig. A.8. Input menu of the modeling tool

The input takes in the basic specifications of the filter. The input nonlinearity and noise parameter file (DC_Char_OTA.txt), the corner frequency of the filter, the signal amplitude to perform the THD analysis etc. The output files are stored in a text file under an extension of .txt. Fig. A.9 shows the result of the preliminary analysis.

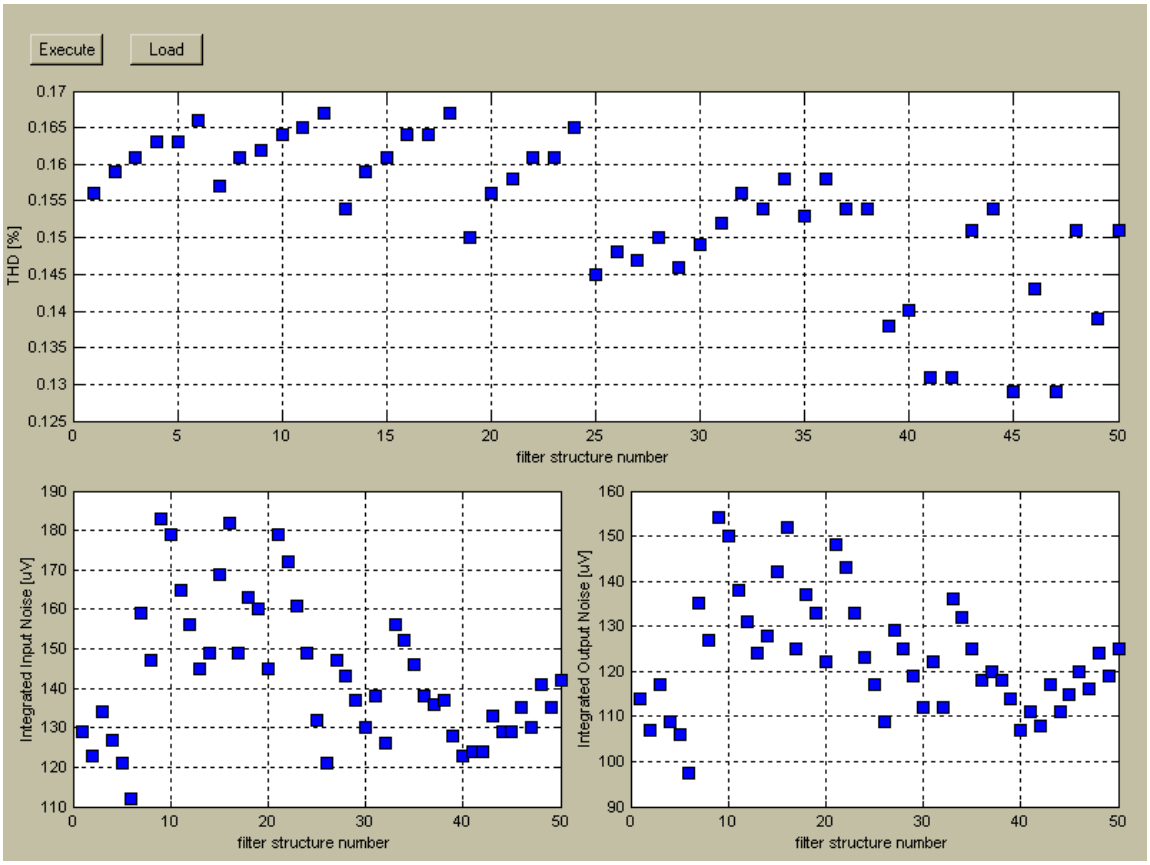


Fig. A.9. THD and noise results for all the 50 structures of the 5th order filter

Fig. A.9 shows the comparison result of non-linearity and noise performance of all the 50 possible structures for the 5th order filter. The most optimum structure can be determined using this window and the tool can be used to also study the particular structure in detail. To study a particular structure in detail more inputs are required. Fig. A.10 shows the second input menu.

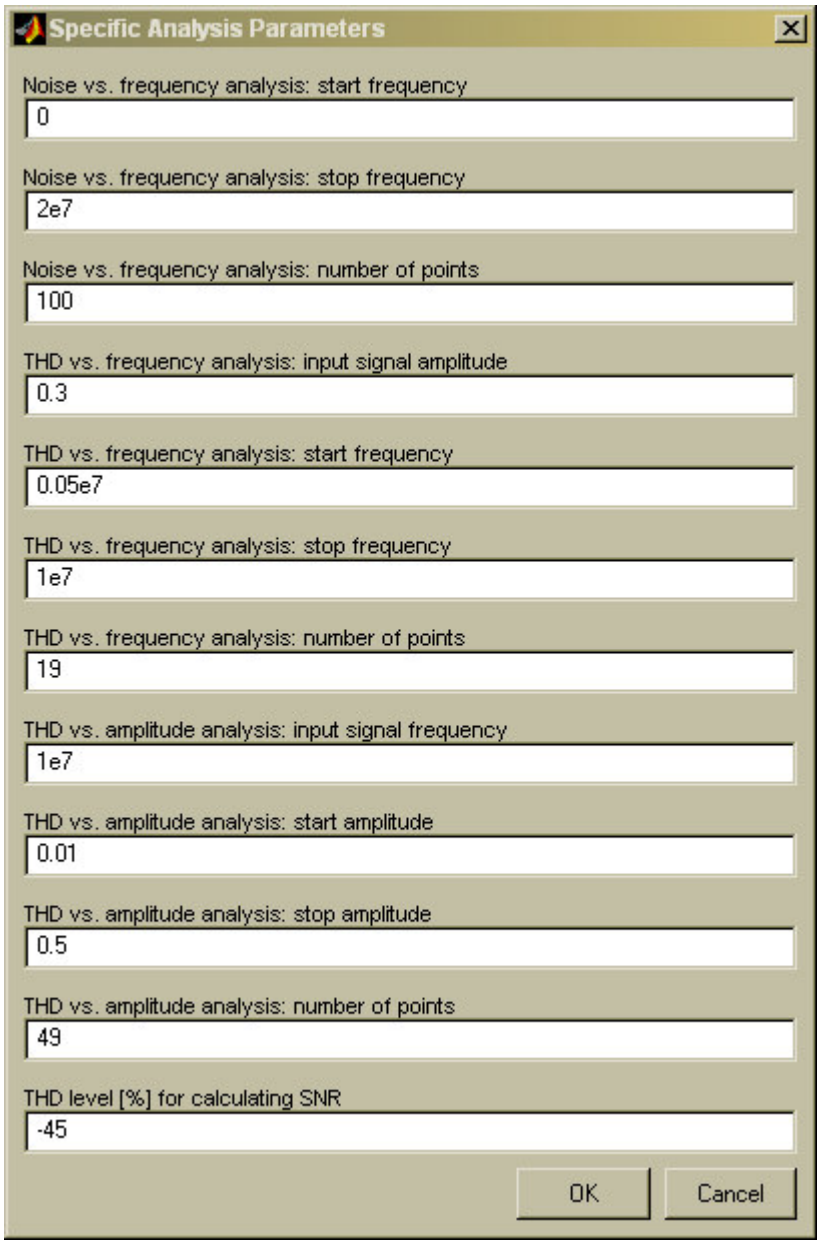


Fig. A.10. Input menu to analyze a particular structure

The cascade structure is structure numbered 45. Hence in the second input menu structure number is entered as 45 and the other details are also entered. The tool can also be used to estimate the SNR for a particular level of THD. This is done by estimating the input amplitude for a particular THD specification and accordingly the noise is also

estimated and the SNR is calculated. The output window of the this step is shown in Fig. A.11. The window also has a slide bar which can be used to estimate the SNR for various cases of THD.

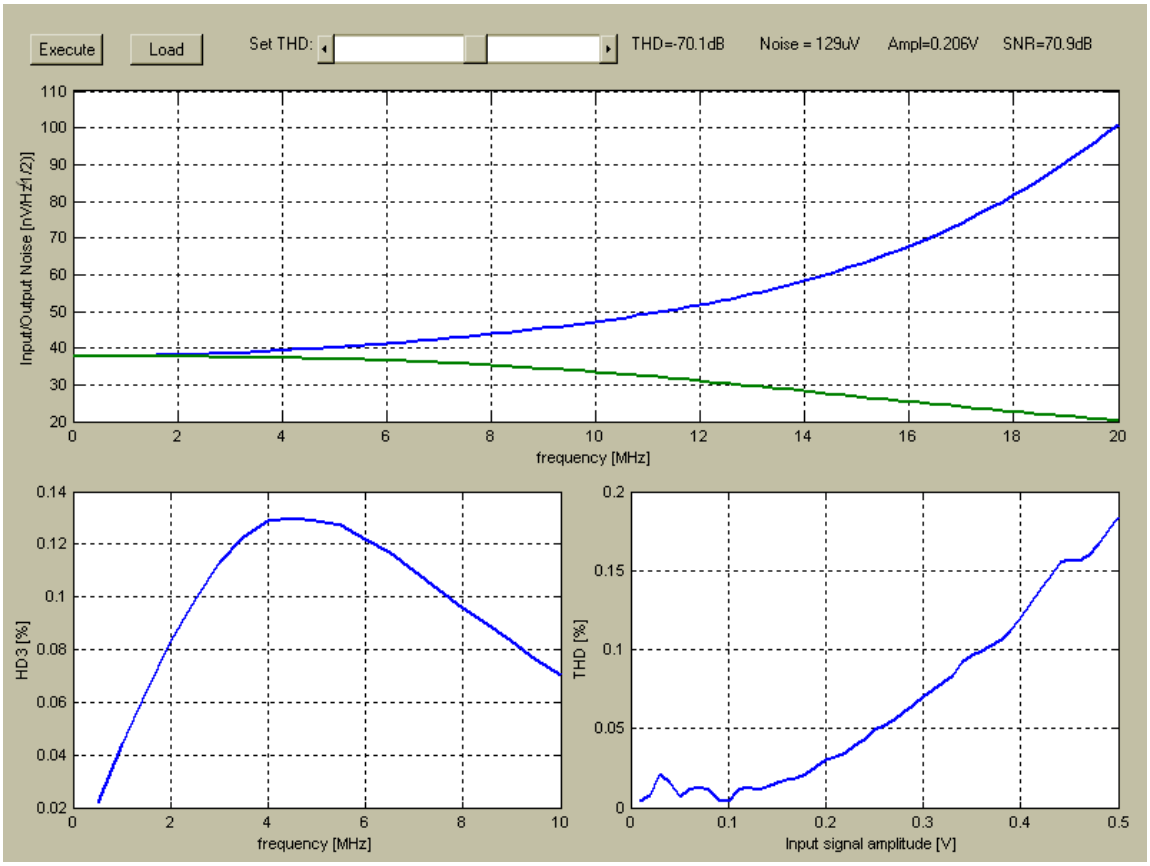


Fig. A.11. Output window for a single structure analysis

The output window has the variation of THD with respect to the input amplitude, variations of the HD_3 with respect to the input frequency and also the input referred and output referred noise. The output files can also be used for other analysis.

APPENDIX B

LIMITATIONS OF TUNING RANGE IN OTA

Many continuous-time systems, such as active filters and continuous-time sigma–delta analog–digital converters (ADCs), often require a reasonably precise cutoff frequency or *RC* time constant. Unfortunately, current CMOS technologies usually have large process variations, which could result in up to a 50% *RC* time constant uncertainty. To avoid using precise external passive components, an on-chip auto tuning circuit becomes a necessity [102].

The process of establishing an on-chip tuning scheme involves the tuning process of certain critical parameters of the Active-RC or Gm-C based circuits. There are two possible ways to tune the *RC* time constant, (1) active and (2) passive components tuning. The active components tuning involves a continuous tuning scheme which can be implemented by changing the transconductance g_m in an operational transconductance amplifier (OTA). In the passive components tuning, on the other hand, C or R is adjusted within a set of discrete values [103].

The main focus of this section would be the limitation on the active tuning process in the case of OTAs. It is essential to estimate the limit of tuning the transconductance of any OTA. The active tuning process involves tuning the transconductance parameter which will be directly reflected on the frequency response of the OTA, as the bandwidth is dependant directly on the transconductance value.

Taking the case of the simple differential pair as shown in Fig. B.1, the transconductance of the input differential pair, in saturation region can be described by equation (B.1), neglecting the second order effects.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}\left(V_{GS} - V_{TN}\right) = \mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} V_{eff} \qquad (B.1)$$

where I_D is the drain current through the transistors M_1 and M_2 ($I_D=I_{bias}=I_{tail}/2$) and V_{eff} is the effective voltage of transistor M_1/M_2.

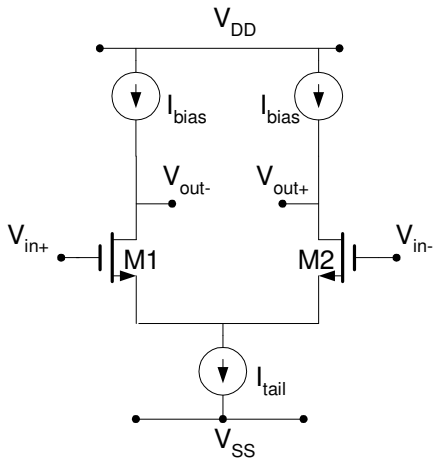


Fig. B.1. Simple differential pair with a tail current source

The transconductance can also be written as shown in equation (B.2),

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{V_{eff}} \tag{B.2}$$

To tune the OTA using an on-chip active tuning scheme, the only parameter that is available to the user is the drain current. The dimensions of the transistors can be changed on chip. To tune the g_m of the input pair, the drain current can be varied by tuning the tail current source or by introducing another block which will control the transconductance term, i.e. source degeneration.

Fig. B.2 shows the two tuning implementations. Fig. B.2a shows the tuning of the transconductance by varying the tail current, which is achieved by adjusting the gate control voltage of transistor M_3. The gate control voltage V_{cntr} controls the tail current of the differential pair. To determine the limiting factors in this tuning process, the expression for the transconductance term, based on the square model, should be related

to the control voltage. This relation can be derived using expressions (B.3), (B.4), (B.5). The second order effects like channel length modulation effect is considered for the transistor M_3 which defines the drain current.

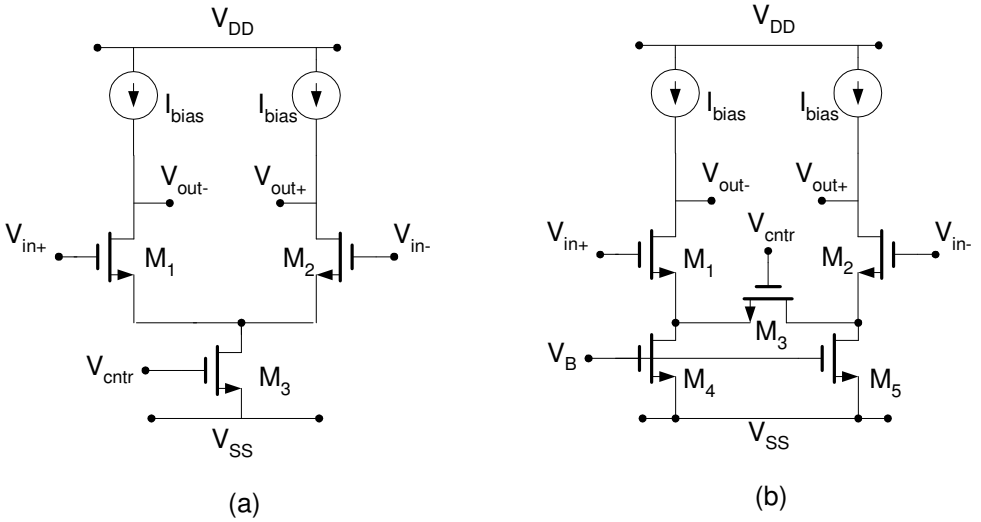


Fig. B.2. OTA g_m-tuning (a) tail current adjustment (b) source degeneration

$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} I_D} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}\left(\frac{I_{tail}}{2}\right)} \tag{B.3}$$

$$I_{tail} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{M3}\left(V_{cntr} - V_{SS} - V_{TN}\right)^2\left(1 + \lambda V_{DS,M3}\right) \tag{B.4}$$

$$g_{m1} = \sqrt{\frac{(\mu_n C_{ox})^2}{2}\left(\frac{W_1}{L_1}\right)\left(\frac{W_3}{L_3}\right)\left(V_{cntr} - V_{SS} - V_{TN}\right)^2\left(1 + \lambda\left(V_{IN+} - V_{GS1} - V_{SS}\right)\right)} \tag{B.5}$$

As can be seen from expression (B.5), the factor that controls the variations of the transconductance parameter is the control voltage. This control voltage cannot be increased beyond a particular limit, because above a particular value the transistor will leave the saturation region and would no longer follow the square law model. Thus for

this method of tuning the OTA, the limitation factor is the control voltage. From the explanation given in Appendix A, Fig. B.3. shows the variation of g_m using the bias voltage for the OTA used in chapter II [75].

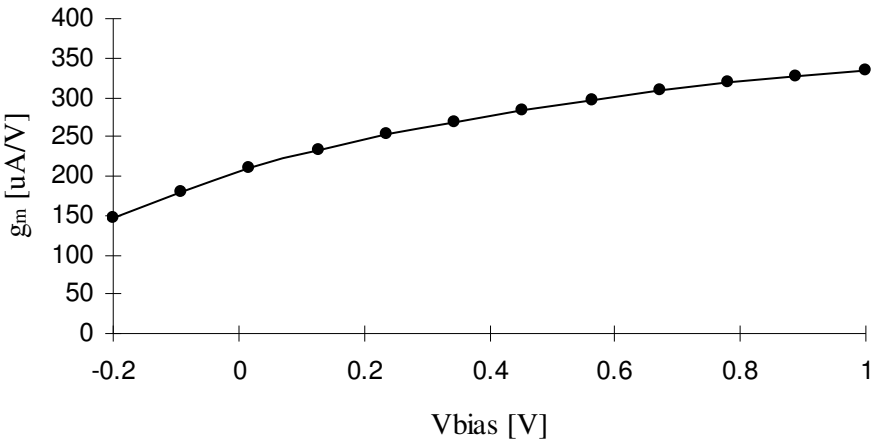


Fig. B.3 Variation of g_m with respect to V_{bias} for the linear OTA [75]

From Fig. B.3 it can be observed that even in the case of a very linear OTA, the maximum tuning range in the g_m, is twice the value compared to the value of g_m around 0 V (6dB variation in the g_m level).

Fig. B.2b shows another tuning approach [103] which is based on controlling the transconductance parameter by means of source degeneration. The OTA small-signal transconductance is tuned by adjusting the gate voltage of transistor M_3, which operates in the triode region. For large source degeneration factors, the OTA transconductance is dominated by the conductance of M_3 and can be expressed as shown in expression (B.6), [104],

$$g_{meff} = \frac{g_{M1}}{1+\frac{g_{M1}R_{M3}}{2}} * \sqrt{1-\left(\frac{V_{IN}}{2\left(1+\frac{g_{M1}R_{M3}}{2}\right)(V_{GS1}-V_{TN})}\right)} \tag{B.7}$$

$$R_{M3} = \mu_n C_{ox}\left(\frac{W}{L}\right)_{M3}(V_{GS3}-V_{TN}) \tag{B.8}$$

where R_{M3} is the equivalent source degeneration introduced by the transistor M_3 operating in the triode region.

In both the mentioned techniques, the overall g_m is dependent upon the input signal common mode voltage, which limits the linearity of the OTA. In the practical circuit design, the g_m is often optimized to achieve the required linearity. To achieve a larger g_m means to increase the drain current and this could possibly reduce the output voltage swing. These factors are dependant on each other. In most practical cases the maximum limit for tuning the value of transconductance is just twice its initial value. This variation doesn't affect the linearity much and also the output voltage swing. Thus most of the tuning schemes exhibit the maximum variation of g_m to be twice its value.

In CMOS transconductors, large tunability needed to correct for temperature and process variations gives a significant reduction in voltage swings at low supply voltages and consequently dynamic range reduction. The new technologies optimized for digital applications are impaired by second order effects like velocity saturation and mobility reduction. Most of the concepts used in the past cannot be used anymore. New transconductor concepts which do not rely upon the ideal square law of a MOST, are needed. Another issue is to achieve large tunability without conflicting with the large swing requirement.

VITA

Arun Ramachandran was born in Trivandrum, India. He received his B.En. degree in electrical engineering from Birla Institute of Technology and Science, Pilani, India, in 2002, his M.S. degree in biological sciences from Birla Institute of technology and Science, Pilani, India, in 2002, and his second M.S. degree in electrical engineering at Texas A&M University, in 2005.

He held a co-op at Analog Devices, India Product Development Center, Bangalore, India, from July 2001 to July 2002. He has been a Research Assistant in the Analog and Mixed Signal Center, Texas A&M University since September 2002. He held an internship at National Semiconductor, Austin, TX, from June 2003 to August 2003. His research includes continuous time active filter design and modeling of non-linearity and noise of Operational Transconductance Amplifiers.

He could be contacted at arun.ramachandran@gmail.com. His permanent address in India is A-161, Jai Nagar, Tiruverumbur Post, Trichy, Tamil Nadu India. His contact address in the USA is 4442 S.Wildflower Place, Chandler, Arizona.