Device description

The PM8953 0.18 µm HVCMOS device is available in 187-pin fan-out wafer nanoscale package (187 FOWNSP) that includes ground pins for improved electrical ground, mechanical stability, and thermal continuity.

The PM8953 device (Figure 1-1) plus its companion PMI8952 (80-NT391-x) device, integrates all wireless handset power management, general housekeeping (HK), and user interface support functions into two IC solutions.

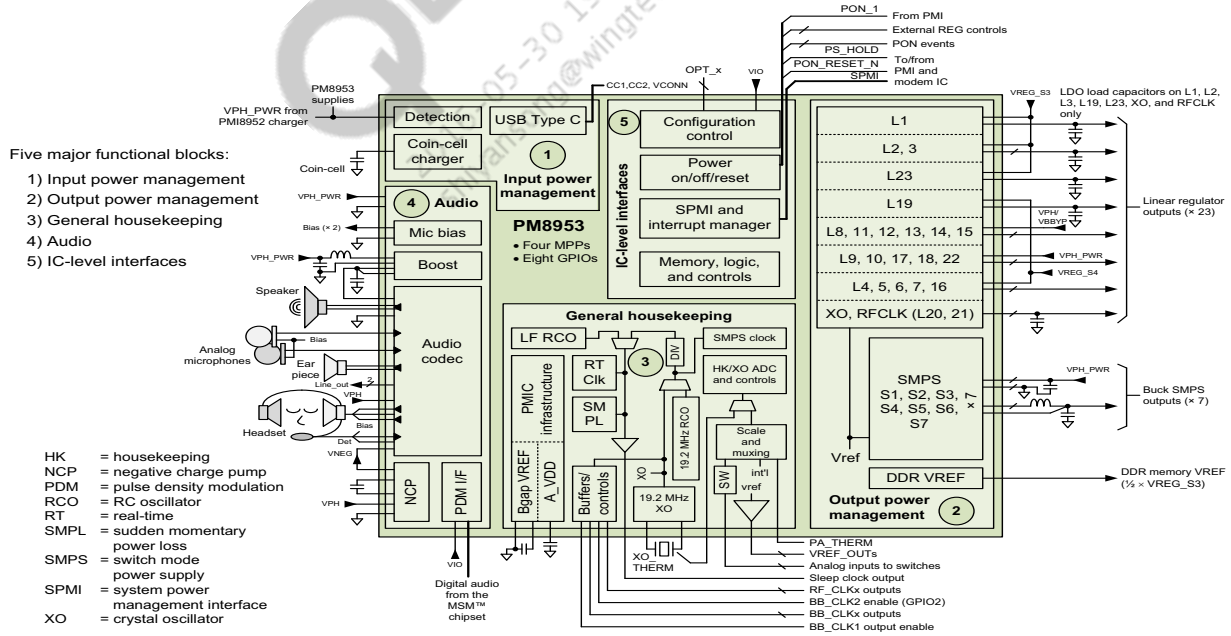
Since the PM8953 includes diverse functions, its operation is easily understood by considering major functional blocks individually. Therefore, the PM8953 document set is organized by the following device functionality:

- Input power management
- Output power management
- General HK
- Audio
- IC interfaces
- Configurable pins: either multipurpose pins (MPPs) or general-purpose input/output (GPIOs) that can be configured to function within some of the other categories

Key features (see Section 1.2 for details)

- Complete output power management with seven SMPS bucks and 23 LDOs optimized for the MSM8953 power grid
- Integrated high-performance codec with 5 V boost for class D amplifier
- Complete clock tree solution with 19.2 MHz XO, buffered RFCLK, BBCLK, and sleep CLK
- Integrated USB type-C support
- SPMI communication for interfacing with MSM8953

PM8953 high-level block diagram and 187 FOWNSP package drawing



Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

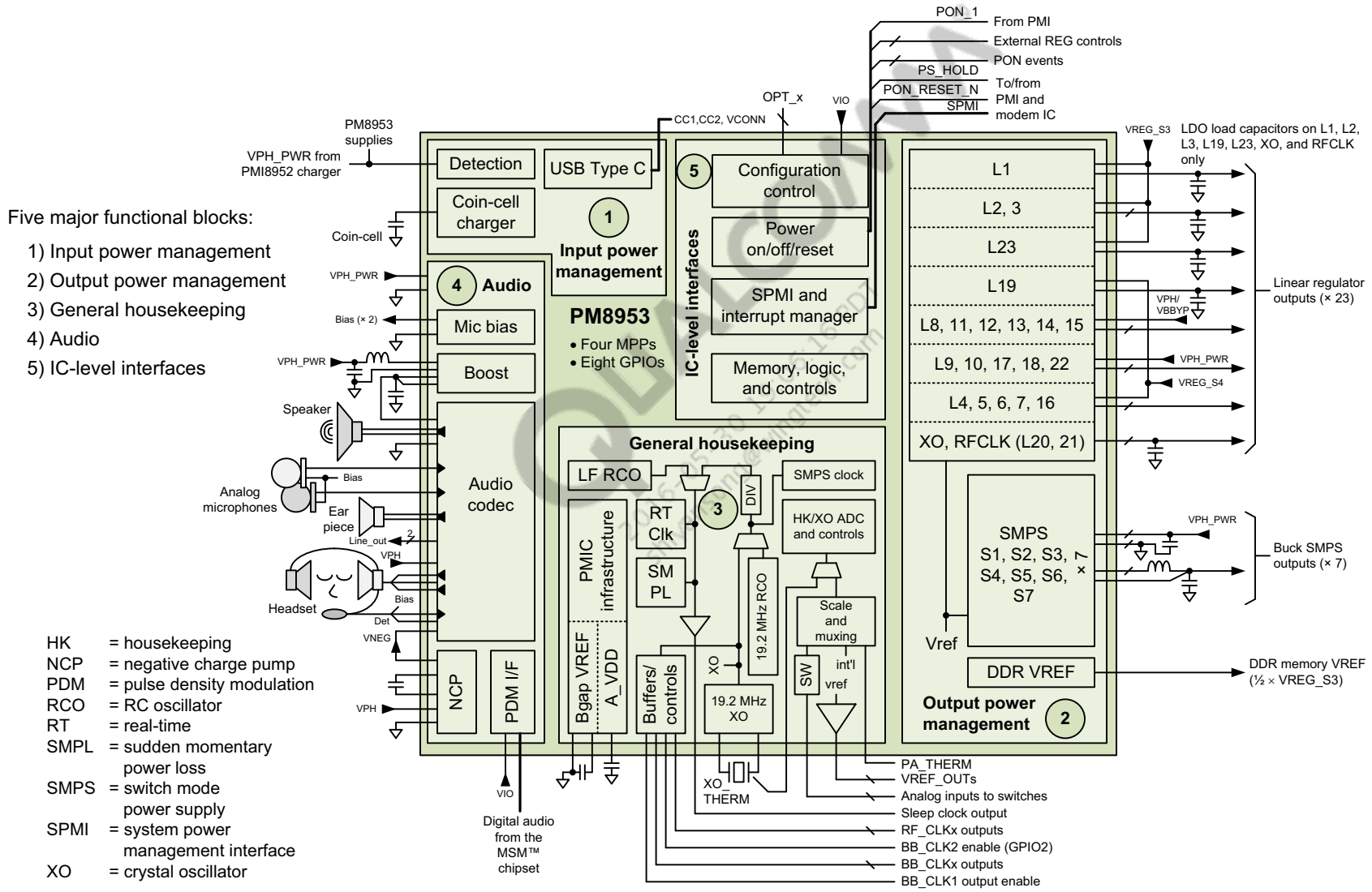


Figure 1-1 PM8953 functional block diagram and example application

1.2 PM8953 features

NOTE Some hardware features integrated within the PM8953 must be enabled through the IC software. See the latest version of the applicable software release notes to identify the enabled PMIC features.

Table 1-1 PM8953 features

Feature	PM8953 capability
Input power management	
Coin cell or capacitor backup	Keep-alive power source; orchestrated charging
VPH_PWR detector	Validates the primary VPH_PWR input voltage
USB type C support	■ Support for CC1 and CC2 pins to detect default, medium, and high current modes ■ Dual role ports ■ VCONN for USB 3.0 super speed cable support
Output voltage regulation	
Switched-mode power supplies (SMPS)	Seven, one rated for 4 A, one for 3 A, two for 3.75 A, and three for 2 A
Low-dropout linear regulators	23 total, eight different design types: one 1200 mA NMOS, four 600 mA NMOS, four 600 mA PMOS, one 450 mA PMOS, three 300 mA PMOS, four 150 mA PMOS, four 50 mA PMOS, and two for clocks
Pseudo-capless LDO designs	12 of 23 LDOs
LP DDR memory support	Voltage reference source
General HK	
On-chip ADC	Shared HK and XO support
Analog multiplexing for ADC ■ HK inputs ■ XO input	■ Many internal nodes and external inputs, including configurable MPPs ■ Dedicated pins for XO_THERM and PA_THERM
Overtemperature protection	Multistage smart thermal control
19.2 MHz oscillator support	XO (with on-chip ADC)
XO controller and XO outputs	Five sets: three low-noise outputs (RF) and two low-power outputs (BB)
Special purpose clock outputs	■ Sleep clock; 19.2, 9.6, 4.8, 2.4, and 1.2 MHz, including low-power mode ■ 2.4 MHz for MP3; two high-speed GPIOs for fast clocks
Real-time clock	RTC clock circuits and alarms
IC infrastructure circuits	Band-gap voltage reference and LDO for analog circuits
IC-level interfaces	
Primary status and control	Two-line SPMI
Interrupt managers	Supported by SPMI
Optional hardware configurations	OPT bits select hardware configuration
Power sequencing	Power on and power off

Table 1-1 PM8953 features (cont.)

Feature	PM8953 capability
Audio codec	
Audio inputs	■ Two single-ended and one differential (microphone) input ■ Integrated IEC ESD protection on microphone 2 input ■ Two ADCs
Multi-button headset control	■ Up to five buttons of MBHC headset support ■ One input for headset jack detection
Audio outputs	■ Five outputs: EAR, HPHL + HPHR, line out, and Class-D speaker driver ■ Three DACs ■ Overcurrent protection (OCP) on HPH, EAR, and speaker outputs
Multiple audio I/O sample rates	Supports 8, 16, 32, and 48 kHz sample rates
Audio-specific power supplies	■ +5 V boost SMPS for high-power audio ■ Negative charge pump for HPH negative supply ■ Microphone bias outputs (×2)
Configurable I/Os	
MPPs	Four; configurable as digital in/out; analog multiplexer inputs; current sinks; VREF buffer outputs; MPP_1 and MPP_3 are fixed for VDD_PX_BIAS and VREF_DAC respectively.
GPIO pins	Eight; configurable as digital inputs or outputs; all are faster than MPPs
Fabrication technology and package	
Fab	0.18 µm HV CMOS
Size	5.78 × 5.78 × 0.65 mm
Pin count and package type	187 FOWNSP

2 Pin definitions

The PM8953 is available in the 187 FOWNSP. Its bottom surface is equivalent to a 187 FOWNSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details.

Figure 2-1 shows a high-level view of the pin assignments for the PM8953.

1 GND_XO_ISO	2 XTAL_19M_IN	3 XTAL_19M_OUT	4 VREG_XO	5 VREG_RFCLK	6 VREG_L9		7 VREG_L7	8 VREF_LPDDR	9 VREG_L1	10 GND_S4	11 VSW_S4	12 VDD_S4	13 VDD_S4
14 VCOIN	15 GND_XO_ISO	16 GND_XO	17 GND_RFCLK	18 VREG_L18	19 BB_CLK2	20 VREG_L22	21 VDD_L4_5_6_7_16_19	22 VREG_L6	23 VREG_L19	24 GND_S4	25 VSW_S4	26 VDD_S4	27 PON_RESET_N
28 VREG_L12	29 VDD_L8_11_12_13_14_15	30 VREG_L8	31 VDD_XO_RFCLK	32 BB_CLK1	33 VDD_L9_10_17_18_22	34 VREG_L17		35 VDD_L4_5_6_7_16_19	36 VDD_L1	37 SPMI_DATA	38 VREG_S4	39 GND_S1	40 GND_S1
41 RF_CLK1	42 VREG_L11	43 RF_CLK2	44 VDD_L8_11_12_13_14_15	45 VREG_L14	46 RF_CLK3	47 VREG_L10	48 VREG_L16	49 VREG_L5	50 VREG_L4	51 SPMI_CLK	52 PS_HOLD	53 VSW_S1	54 VSW_S1
	55 BB_CLK1_EN		56 VREG_L13	57 REF_BYP	58 VREG_L15	59 VPH_PWR		60 AVDD_BYP	61 DVDD_BYP	62 VREG_S1	63 KPD_PWR_N	64 VDD_S1	65 VDD_S1
66 LINEOUT_M	67 LINEOUT_P	68 HPH_L	69 MIC_BIAS1	70 GND_REF	71 GND	72 GND_XOADC	73 XO_THERM	74 PA_THERM	75 VREG_S2	76 RESIN_N	77 PON_1	78 GND_S2	79 GND_S2
80 VNEG_HPH	81 VDD_HPH	82 HPH_REF	83 MIC_BIAS2	84 GND_CFILT	85 GND	86 GND	87 GND	88 GND	89 SLEEP_CLK1	90 GPIO_6		91 VSW_S2	92 VSW_S2
93 EARO_P	94 EARO_M	95 HPH_R	96 MIC1_IN_P	97 MIC1_IN_M	98 GND	99 GND	100 GND	101 CC2	102 GND	103 VREG_S7	104 GPIO_5	105 VDD_S2	106 VDD_S2
107 VDD_SPKR_PA		108 MIC2_IN	109 HS_DET	110 MPP_3	111 OPT_1	112 MPP_1	113 VCONN	114 CC1	115 VREG_S5	116 VREF_NEG_S5	117 GPIO_4	118 GND_S7	119 GND_S7
120 SPKR_DRV_P	121 SPKR_DRV_M		122 MIC3_IN	123 OPT_2	124 CBL_PWR_N	125 MPP_2		126 VDD_L23	127 VREG_S6	128 VREF_NEG_S6	129 GPIO_8	130 VSW_S7	131 VSW_S7
132 GND_SPKR_PA	133 CP_VNEG	134 PDM_RX0_DRE	135 PDM_RX0	136 PDM_SYNC	137 VREG_S3	138 VREG_L23	139 VDD_L2_3	140 VREG_L2	141 GPIO_2	142 GPIO_3	143 GPIO_7	144 VDD_S7	145 VDD_S7
146 CP_C1_M	147 GND_CP	148 PDM_RX1_DRE	149 PDM_TX	150 PDM_CLK	151 MPP_4	152 GPIO_1	153 VREG_L3	154 VDD_S6	155 VSW_S6	156 GND_S6	157 VDD_S5	158 VSW_S5	159 GND_S5
160 CP_C1_P	161 VDD_CP	162 BOOST_SNS	163 VDD_AUDIO_IO	164 PDM_RX2	165 VDD_S3	166 VSW_S3	167 GND_S3	168 VDD_S6	169 VSW_S6	170 GND_S6	171 VDD_S5	172 VSW_S5	173 GND_S5
174 GND_BOOST	175 GND_BOOST	176 VSW_BOOST	177 VREG_BOOST	178 PDM_RX1	179 VDD_S3	180 VSW_S3	181 GND_S3	182 VDD_S6	183 VSW_S6	184 GND_S6	185 VDD_S5	186 VSW_S5	187 GND_S5

Audio | Configurable IOs | Do not connect | General housekeeping | Ground | IC-level interfaces | Input power management | Output power management | Power

Figure 2-1 PM8953 bottom pin assignments

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
GND	Ground
PI	Power input; a pin that handles 10 mA or more of current flow into the device
PO	Power output; a pin that handles 10 mA or more of current flow out of the device
Z	High-impedance (high-Z) output
Pad-voltage groupings for baseband circuits	
dVdd	Internally generated 1.8 V supply voltage for some power-on circuits
aVdd	Internally generated 1.8 V supply voltage for some analog circuits
V_PAD	Supply for modem IC interfaces; connected internally to VREG_L5
V_XBB	Supply for XO low-power (BB) output buffers; connected internally to VREG_L7
V_XRF	Supply for XO low-noise (RF) output buffers; connected internally to VREG_RFCLK
V_G1	Selectable supply for GPIOs capable of high-speed clock outputs (GPIO_1 and GPIO_2); options include: ■ 0 = 1 = 3 = VREG_L5 ■ 2 = VREG_S3
V_G2	Selectable supply for all other GPIO circuits; options include: ■ 0 = 1 = VPH_PWR ■ 2 = VREG_S3 ■ 3 = VREG_L5
V_M	Selectable supply for MPP circuits; options include: ■ 0 = 1 = VPH_PWR ■ 2 = VREG_S3 ■ 3 = VREG_L5
GPIO pin configurations	
GPIO pins, when configured as inputs, have configurable pull settings	
NP	No internal pull enabled
PU	Internal pull-up enabled
PD	Internal pull-down enabled
GPIO pins, when configured as outputs, have configurable drive strengths	
H	High: ~ TBD mA at 1.8 V; ~ TBD mA at 2.6 V

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
M	Medium: ~ TBD mA at 1.8 V; ~ TBD mA at 2.6 V
L	Low: ~ TBD mA at 1.8 V; ~ TBD mA at 2.6 V

2.2 Pin assignments

2.2.1 Pin descriptions

Descriptions of bottom pins are presented in the following tables, organized by functional group:

Table 2-2: Input power management functions

Table 2-3: Output power management functions

Table 2-4: General HK functions

Table 2-5: Audio

Table 2-6: IC-level interface functions

Table 2-7: Configurable input/output functions – GPIO and MPPs

Table 2-8: Pin descriptions – DC power supply voltages

Table 2-9: Pin descriptions – grounds

Table 2-2 Input power management functions

Pad #	Pad name and/or function	Pad name or alternate function	Pad type	Functional description
59	VPH_PWR	–	PI	Primary phone power
14	VCOIN	–	AI, AO	Coin cell battery or backup battery; the last remaining available source to maintain xVdd backed registers
113	VCONN	–	AI	Power input pin (5 V, 210 mA from VBUS) to drive active cables during the DFP mode. An internal mux connects VCONN power to either CC1 or CC2 based on the cable orientation.
101, 114	CC1, CC2	–	AI, AO	USB type C connector configuration channel

Table 2-3 Output power management functions

Pad #	Pad name and/or function	Pad type[1]	Functional description
SMPS circuits			
64, 65	VDD_S1	PI	Buck converter S1 supply voltage
53, 54	VSW_S1	PO	Buck converter S1 switching node
62	VREG_S1	AI	Buck converter S1 sense point
39, 40	GND_S1	GND	Buck converter S1 ground
105, 106	VDD_S2	PI	Buck converter S2 supply voltage
91, 92	VSW_S2	PO	Buck converter S2 switching node
75	VREG_S2	AI	Buck converter S2 sense point
78, 79	GND_S2	GND	Buck converter S2 ground
165, 179	VDD_S3	PI	Buck converter S3 supply voltage
166, 180	VSW_S3	PO	Buck converter S3 switching node
137	VREG_S3	AI	Buck converter S3 sense point
167, 181	GND_S3	GND	Buck converter S3 ground
12, 13, 26	VDD_S4	PI	Buck converter S4 supply voltage
11, 25	VSW_S4	PO	Buck converter S4 switching node
38	VREG_S4	AI	Buck converter S4 sense point
10, 24	GND_S4	GND	Buck converter S4 ground
157, 171, 185	VDD_S5	PI	Buck converter S5 supply voltage
158, 172, 186	VSW_S5	PO	Buck converter S5 switching node
115	VREG_S5	AI	Buck converter S5 sense point
116	VREF_NEG_S5	AI	Buck converter S5 negative reference
159, 173, 187	GND_S5	GND	Buck converter S5 ground
154, 168, 182	VDD_S6	PI	Buck converter S6 supply voltage
155, 169, 183	VSW_S6	PO	Buck converter S6 switching node
128	VREF_NEG_S6	PI	Buck converter S6 negative reference
127	VREG_S6	AI	Buck converter S6 sense point
156, 170, 184	GND_S6	GND	Buck converter S6 ground
144, 145	VDD_S7	PI	Buck converter S7 supply voltage
130, 131	VSW_S7	PO	Buck converter S7 switching node
103	VREG_S7	AI	Buck converter S7 sense point
118, 119	GND_S7	GND	Buck converter S7 ground
Low dropout (LDO) linear regulators			
126	VDD_L23	PI	LDO 23 supply voltage
138	VREG_L23	PO	LDO 23 output
36	VDD_L1	PI	LDO 1 supply voltage

Table 2-3 Output power management functions (cont.)

Pad #	Pad name and/or function	Pad type[1]	Functional description
9	VREG_L1	PO	LDO 1 output
139	VDD L2_3	PI	LDO 2 and 3 supply voltages
140	VREG_L2	PO	LDO 2 output
153	VREG_L3	PO	LDO 3 output
21, 35	VDD_L4_5_6_7_16_19	PI	LDO 4, 5, 6, 7, 16, and 19 supply voltages
50	VREG_L4	PO	LDO 4 output
49	VREG_L5	PO	LDO 5 output
22	VREG_L6	PO	LDO 6 output
7	VREG_L7	PO	LDO 7 output
48	VREG_L16	PO	LDO 16 output
23	VREG_L19	PO	LDO 19 output
29, 44	VDD_L8_11_12_13_14_15	PI	LDO 8, 11, 12, 13, 14, and 15 supply voltages
30	VREG_L8	PO	LDO 8 output
42	VREG_L11	PO	LDO 11 output
28	VREG_L12	PO	LDO 12 output
56	VREG_L13	PO	LDO 13 output
45	VREG_L14	PO	LDO 14 output
58	VREG_L15	PO	LDO 15 output
33	VDD_L9_10_17_18_22	PI	LDO 9, 10, 13, 14, 15, 18, and 22 supply voltages
6	VREG_L9	PO	LDO 9 output
47	VREG_L10	PO	LDO 10 output
34	VREG_L17	PO	LDO 7 output
18	VREG_L18	PO	LDO 18 output
20	VREG_L22	PO	LDO 22 output
31	VDD_XO_RFCLK	PI	XO and RFCLK LDO supply voltages
5	VREG_RFCLK	PO	LDO for RF CLK outputs (L21)
4	VREG_XO	PO	LDO for XO circuits (L20)
8	VREF_LPDDR	AO	LPDDR memory reference

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 General HK functions

Pad #	Pad name and/or function	Pad name or alternate function	Pad type [3]	Functional description
Analog multiplexer and HK/XO ADC circuits				
73	XO_THERM	–	AI	ADC input – XO thermistor divider
74	PA_THERM	–	AI	AMUX input – PA thermistor divider
72	GND_XOADC	–	GND	HK/XO ADC reference ground
19.2 MHz crystal oscillator (XO) circuits and buffered outputs				
2	XTAL_19M_IN	–	AI	19.2 MHz crystal (XTAL) connection (in)
3	XTAL_19M_OUT	–	AO	19.2 MHz crystal connection (out)
16	GND_XO	–	GND	XTAL circuit ground
1, 15	GND_XO_ISO	–	GND	XO clock circuit ground for shielding; use single via directly to main ground plane; do not share with any other ground pads
41	RF_CLK1	–	DO	Buffered RF (low-noise) XO clock 1
43	RF_CLK2	–	DO	Buffered RF (low-noise) XO clock 2
46	RF_CLK3	–	DO	Buffered RF (low-noise) XO clock 3
17	GND_RFCLK	–	GND	RF output buffers ground
32	BB_CLK1	–	DO	Buffered baseband (low-power) XO clock 1 (to the modem IC's CXO input)
19	BB_CLK2	–	DO	Buffered baseband (low-power) XO clock 2
55	BB_CLK1_EN	–	DI	BB_CLK1 enable (from the modem IC)
Sleep clock				
89	SLEEP_CLK1	–	DO	32 kHz sleep clock to the modem IC
PMIC infrastructure circuits				
60	AVDD_BYP	–	AO	Bypass capacitor for LDO that supplies internal analog circuits; do not load externally
61	DVDD_BYP	–	AO	Bypass capacitor for LDO that supplies internal digital circuits; do not load externally
57	REF_BYP	–	AO	Bandgap reference bypass capacitor (0.1 μF)
70	GND_REF	–	GND	Bandgap reference ground; use single via directly to main ground plane at either capacitor pad or PMIC pad (not both); do not share with any other ground pads
GPIO assignments for general HK functions [1]				
MPP assignments for general HK functions [2]				

1. GPIOs can be used for other general HK functions not listed here. To assign a GPIO to a particular function, identify the application's requirements and map each GPIO to its function—carefully avoiding assignment conflicts. Table 2-7 lists all the GPIOs.

2. MPPs can be used for other general HK functions not listed here. To assign an MPP to a particular function, identify the application's requirements and map each MPP to its function—carefully avoiding assignment conflicts. Table 2-7 lists all the MPPs.
3. See Table 2-1 for parameter and acronym definitions.

Table 2-5 Audio

Pad #	Pad name and/or function	Pad name or alternate function	Pad type [1]	Functional description
Codec – analog audio outputs and related interfaces				
93	EARO_P	–	AO	Earpiece output, plus (+)
94	EARO_M	–	AO	Earpiece output, minus (-)
81	VDD_HPH	–	PI	Headphone positive supply
68	HPH_L	–	AO	Headphone output, left channel
95	HPH_R	–	AO	Headphone output, right channel
82	HPH_REF	–	AI	Headphone ground reference
80	VNEG_HPH	–	PI	Headphone negative supply
109	HS_DET	–	AI	Headset detection
107	VDD_SPKR_PA	–	PI	Class-D speaker power amplifier supply
120	SPKR_DRV_P	–	AO	Class-D speaker driver output, plus (+)
121	SPKR_DRV_M	–	AO	Class-D speaker driver output, minus (-)
132	GND_SPKR_PA	–	GND	Class-D speaker power amplifier ground
67	LINEOUT_P	–	AO	Audio line output, differential plus
66	LINEOUT_M	–	AO	Audio line output, differential minus
Codec – analog audio inputs and related interfaces				
96	MIC1_IN_P	–	AI	Microphone input 1, plus
97	MIC1_IN_M	–	AI	Microphone input 1, minus
108	MIC2_IN	–	AI	Microphone input 2
122	MIC3_IN	–	AI	Microphone input 3
69	MIC_BIAS1	–	AO	Microphone bias 1
83	MIC_BIAS2	–	AO	Microphone bias 2
84	GND_CFILT	–	GND	Microphone bias filter ground
Codec support – analog				
176	VSW_BOOST	–	PO	Audio boost converter switching node
177	VREG_BOOST	–	PI	Audio boost converter regulation node
162	BOOST_SNS	–	AI	Audio boost converter sense point
174, 175	GND_BOOST	–	GND	Audio boost converter ground
161	VDD_CP	–	PI	Charge pump power supply
133	CP_VNEG	–	AO	Charge pump negative output
160	CP_C1_P	–	AO	Charge pump fly capacitor terminal 1

Table 2-5 Audio (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad type [1]	Functional description
146	CP_C1_M	–	AO	Charge pump fly capacitor terminal 2
147	GND_CP	–	GND	Charge pump ground
Codec support – digital				
163	VDD_AUDIO_IO	–	PI	Audio digital I/O power supply
150	PDM_CLK	–	DI	PDM clock signal and codec master clock
136	PDM_SYNC	–	DI	PDM synchronization signal
149	PDM_TX	–	DO	PDM transmit data channel
135	PDM_RX0	–	DI	PDM receive data channel 0
178	PDM_RX1	–	DI	PDM receive data channel 1
164	PDM_RX2	–	DI	PDM receive data channel 2
134	PDM_RX0_DRE	–	DI	RX0 DRE data channel
148	PDM_RX1_DRE	–	DI	RX1 DRE data channel

1. See Table 2-1 for parameter and acronym definitions.

Table 2-6 IC-level interface functions

Pad #	Pad name and/or function	Pad name or alternate function	Pad type [3]	Functional description
Hardware configuration controls				
123	OPT_2	–	DI	Option configuration control bit 2; set to VDD, GND, or Hi-Z; defines internal PMIC characteristics
111	OPT_1	–	DI	Option configuration control bit 1; set to VDD, GND, or Hi-Z; defines internal PMIC characteristics
Power on/off/reset				
27	PON_RESET_N	–	DO	Power-on reset control to modem IC ■ HIGH: modem IC released from reset after successful PMIC power on ■ LOW: modem IC is reset when PMIC is reset or during shutdown
77	PON_1	–	DI	LOW to HIGH from PMI initiates power on
52	PS_HOLD	–	DI	Power-supply hold control input – keeps PMIC on when HIGH, or initiate a reset or power down when asserted LOW
76	RESIN_N	–	DI	PMIC reset input; initiates stage 2 or stage 3 reset if held LOW
124	CBL_PWR_N	–	DI	Cable power-on; internal pull-up to dVdd; initiates power on when grounded

Table 2-6 IC-level interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alternate function	Pad type [3]	Functional description
Hardware configuration controls				
63	KPD_PWR_N	–	DI	Internal pull-up to dVdd; keep C_load < 10 pF. Dual function: ■ Keypad power on; initiates power on when grounded ■ Can be configured as stage 2 or stage 3 reset if held LOW longer
System power management interface (SPMI)				
51	SPMI_CLK	–	DI	SPMI clock
37	SPMI_DATA	–	DI, DO	SPMI data
GPIO assignments for IC-level interface functions [1]				
MPP assignments for IC-level interface functions [2]				

1. GPIOs are used for other user interface functions not listed here; those details will be included in future revisions of this document. To assign a GPIO a particular function, identify the application's requirements and map each GPIO to its function – carefully avoiding assignment conflicts. Table 2-7 lists all the GPIOs.
2. MPPs are used for other user interface functions not listed here; those details will be included in future revisions of this document. To assign an MPP a particular function, identify the application's requirements and map each MPP to its function – carefully avoiding assignment conflicts. Table 2-7 lists all the MPPs.
3. See Table 2-1 for parameter and acronym definitions.

Table 2-7 Configurable input/output functions – GPIO and MPPs

Pad #	Pad name	Configurable function	Pad type [1]	Functional description
MPP functions				
112	MPP_1		AO-Z	Configurable MPP
		VREF_PX_BIAS	AO	Reference for the modem IC digital pads [2]
125	MPP_2		AI	Configurable MPP
		PA_THERM2	AI	PA temperature sense to AMUX
110	MPP_3		AO-Z	Configurable MPP
		VREF_DAC	AO	Reference for the modem IC DAC
151	MPP_4		AI	Configurable MPP
		QUIET_THERM	AI	Input for the QUIET_THERM input skin temperature thermistor
		WLED_PWM_CTRL	DO	PWM control for the external WLED driver
		HR_LED_SINK	AI	Home-row LED current sink
GPIO functions				
152	GPIO_1		DI-PD	Configurable GPIO (GPIOC)
		AUDIO_MCLK	DO	9.6 MHz audio master clock
		DIV_CLK2	DO	Divided clock output 2

Table 2-7 Configurable input/output functions – GPIO and MPPs (cont.)

Pad #	Pad name	Configurable function	Pad type [1]	Functional description
MPP functions				
141	GPIO_2		DI-PD	Configurable GPIO (GPIOC)
		NFC_CLK_REQ	DI	NFC clock request
142	GPIO_3		DI-PD	Configurable GPIO
		BATT_UICC_ALM	DI, DO	Battery UICC alarm (BUA)
117	GPIO_4 [2]		DI-PD	Configurable GPIO
		FORCE_BYPASS	DO	External boost/bypass SMPS: bypass
104	GPIO_5		DI-PD	Configurable GPIO
		BATT_ALM_IN	DI	Battery alarm input
90	GPIO_6		DI-PD	Configurable GPIO
		WLAN_SAD	DO	WLAN switched antenna diversity enable
143	GPIO_7		DI-PD	Configurable GPIO
		VBUS_MON	AI	VBUS monitor signal from type C connector
129	GPIO_8		Hi-Z	Configurable GPIO
		VCONN_EN/USB_HS_ID	DO	Disables and enables external regulator source for VCONN and also serves as the USB_ID pin control for PMI8952

1. See Table 2-1 for parameter and acronym definitions.
2. MPP_1 and GPIO_4 are part of the default power-on sequence.

NOTE All MPPs default to their high-Z state at power up and must be configured after power up for their intended purposes. All GPIOs default to 10 µA pull-down at power up and must be configured after power up for their intended purposes.

NOTE Configure unused MPPs as 0 mA current sinks (high-Z) and unused GPIOs as digital inputs with their internal pull-downs enabled.

NOTE Only even MPPs can be configured as current sinks and only odd MPPs can be configured as analog outputs.

Table 2-8 Pin descriptions – DC power supply voltages

Pad #	Pad name	Functional description
Audio		
See Table 2-5. Includes VDD_AUDIO_IO, VDD_CP, VDD_HPH, VDD_SPKR_PA, and VNEG_HPH.		
Output power management		
See Table 2-3. LDO supplies include VDD_L23, VDD_L1, VDD_L2_3, VDD_L4_5_6_7_16_19, VDD_L8_11_12_13_14_15, VDD_L9_10_17_18_22, and VDD_XO_RFCLK; SMPS supplies include VDD_S1, VDD_S2, VDD_S3, VDD_S4, VDD_S5, VDD_S6, and VDD_S7.		

Table 2-9 Pin descriptions – grounds

Pad #	Pad name	Functional description
General purpose (common) ground pins		
71, 85, 86, 87, 88, 98, 99, 100, 102	GND	Ground for nonspecialized circuits
Audio		
See Table 2-5. Includes GND_BOOST, GND_CFILT, GND_CP, and GND_SPKR_PA.		
Output power management		
See Table 2-3. Includes GND_S1, GND_S2, GND_S3, GND_S4, GND_S5, GND_S6, and GND_S7; and negative reference pins VREF_NEG_S5 and VREF_NEG_S6.		
General HK		
See Table 2-4. Includes GND_REF, GND_RFCLK, GND_XO, GND_XOADC, and GND_XO_ISO.		

3 Electrical specifications

3.1 Absolute maximum ratings

Operating the PM8953 device under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Power supply voltages				
VDD_xx ■ Steady state ■ Transient (<10 ms)	PMIC supply voltages not listed elsewhere	 -0.5 -0.5	 6.0 7.0	 V V
VPH_PWR	Handset supply voltage	-0.5	6.0	V
VCONN, CC1, CC2		-0.3	6.0	V
GPIO7, GPIO8	VPH_PWR+0.5V			
Signal pins				
V_IN	Voltage on any nonsupply pin [1]	-0.5	V_{XX} + 0.5	V
ESD protection and thermal conditions – see Section 7.1.				

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 3-2). The PM8953 device meets all performance specifications listed in Section 3.3 through Section 3.11 when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Units
Power supply voltages					
VDD_AUD_IO	Pad voltage for digital I/Os to and from the IC	1.75	–	1.85	V
VCOIN [1]	Coin cell voltage	2.0	3.0	3.25	V
VDD_xx [2]		3.0	3.6	TBD	V
VPH_PWR	Handset supply voltage	3.0	3.6	TBD	V
VCONN		3.7	–	6	V
CC1, CC2		0	–	5.5	V
Signal pins					
V_IN	Voltage on any nonsupply pin [3]	0	–	V_{XX} + 0.5	V
Thermal conditions					
T_A	Ambient temperature	-30	+25	85	°C
T_J	Junction temperature	-30	+25	125	°C

1. A minimum 2.0 V coin cell voltage guarantees stable and reliable logic operation.
2. The lowest battery and VDD voltage where parametric performance is guaranteed is 3.0 V. However, the UVLO comparators and other circuits must work properly below this voltage to the UVLO threshold.
3. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.3 DC power consumption

This section specifies DC power-supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default parameter settings.

Table 3-3 DC power-supply currents

Parameter		Comments	Min	Typ	Max	Units
I_BAT1	Supply current, active mode [1]	–	–	TBD	TBD	mA
I_BAT2	Supply current, sleep mode [2]	–	–	TBD	TBD	µA
I_BAT3	Supply current, off mode [3]	–	–	TBD	TBD	µA

1. I_BAT1 is the total supply current from the main battery with the PMIC on, 19.2 MHz XO on, BB_CLK1, and RF_CLK3 on but not loaded, and these voltage regulators on but not loaded, with these voltage settings: VREG_S1 = 1.225 V, VREG_S2 = 1.225 V, VREG_S3 = 1.2875 V, VREG_S4 = 2.05 V, VREG_S5 = 1.225 V, VREG_S6 = 1.225 V, VREG_L2 = 1.2 V, VREG_L3 = 1.225 V, VREG_L5 = 1.80 V, VREG_L6 = 1.80 V, VREG_L7 = 1.80 V, VREG_L8 = 2.90 V, VREG_L11 = 2.95 V, VREG_L12 = 2.95 V, VREG_L13 = 3.075 V, VREG_L17 = LCD TC Ctrl, VREG_XO = 1.80 V, VREG_RFCLK = 1.80 V, MPP_1 = 1.25 V (analog out), and VREF_LPDDR = 0.5 × (VREG_S3).
2. I_BAT2 is the total supply current from the main battery with the PMIC on, 19.2 MHz XO on, SLEEP_CLK on, the voltage regulators forced into their low-power modes, not loaded, with these voltage settings: VREG_S2 = 0.5 V, VREG_S3 = 1.2625 V, VREG_L2 = 1.2 V, VREG_L3 = 0.65 V, VREG_S4 = 1.9 V, VREG_L5 = 1.80 V, and MPP_1 = ON. All CLK_EN signals are low, VREF_LPDDR is on, and the master band gap (MBG) is in its low-power mode.
3. I_BAT3 is the total supply current from the main battery with the PMIC off and an on-chip oscillator on. This only applies from -30 to 60°C.

3.4 Digital logic characteristics

PM8953 digital I/O characteristics, such as voltage levels, current levels, and capacitance, are specified in Table 3-4.

Table 3-4 Digital I/O characteristics

Parameter		Comments [1]	Min	Typ	Max	Units
V_{IH}	High-level input voltage	–	0.65 × V_{IO}	–	V_{IO} + 0.3	V
V_{IL}	Low-level input voltage	–	-0.3	–	0.35 × V_{IO}	V
V_{SHYS}	Schmitt hysteresis voltage	–	15	–	–	mV
I_L	Input leakage current [2]	V_{IO} = maximum, V_{IN} = 0 V to V_{IO}	–	–	±0.20	µA
V_{OH}	High-level output voltage	I_{out} = I_{OH}	V_{IO} - 0.45	–	V_{IO}	V
V_{OL}	Low-level output voltage	I_{out} = I_{OL}	0	–	0.45	V
I_{OH}	High-level output current [3]	V_{out} = V_{OH}	3	–	–	mA
I_{OL}	Low-level output current [3]	V_{out} = V_{OL}	–	–	-3	mA
I_{OH_XO}	High-level output current [3]	XO digital clock outputs only	6	–	–	mA
I_{OL_XO}	Low-level output current [3]	XO digital clock outputs only	–	–	-6	mA
C_{IN}	Input capacitance [4]	–	–	–	5	pF

1. V_{IO} is the supply voltage for the MSM/PMIC interface (most PMIC digital I/Os).
2. MPP and GPIO pins comply with the input leakage specification only when configured as a digital input or set to the tri-state mode.
3. Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins (such as MPP and GPIO pins).
4. Input capacitance is guaranteed by design but is not 100% tested.

3.5 Input power management

3.5.1 Coin cell charging

Coin cell charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage source and a programmable series resistor. The modem IC reads the coin cell voltage through the PMIC's analog multiplexer to monitor charging. Coin cell charging performance is specified in Table 3-5.

Table 3-5 Coin cell charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Target regulator voltage [1]	V_{IN} > 3.3 V, I_{CHG} = 100 µA	2.50	3.10	3.20	V
Target series resistance [2]	–	800	–	2100	Ω
Coin cell charger voltage error	I_{CHG} = 0 µA	–	–	±5	%
Coin cell charger resistor error	–	–	–	±20	%
Dropout voltage [3]	I_{CHG} = 2 mA	–	–	200	mV
Ground current, charger enabled	PMIC = off; VCOIN = open				
■ VBAT = 3.6 V, T = 27ºC		–	4.5	–	µA
■ VBAT = 2.5–5.5 V		–	–	8	µA

1. Valid regulator voltage settings are 2.5, 3.0, 3.1, and 3.2 V.
2. Valid series resistor settings are 800, 1200, 1700, and 2100 Ω.
3. Set the input voltage (VBAT) to 3.5 V. Note the charger output voltage; call this value V_0. Decrease the input voltage until the regulated output voltage (V_1) drops 100 mV ($V_1 = V_0$ - 0.1 V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout}$ = VBAT - V_1).

3.5.2 Type-C interface

PM8953 has integrated Type-C interface support and works with the PMI8952 charger to provide multiple Type-C features, including mode configuration, channel configuration, current advertisement, and active cable support. The Type-C FSM interface is based on status of GPIO_7, GPIO_8, and VCONN. The Type-C interface performance is specified in Table 3-6.

Table 3-6 Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC operating characteristics						
TA = -30°C to +85°C, VUSBIN = +5.0 V, +9.0 V, VFLTmax = +4.4 V, VBATT = +3.9 V, and VCONN=5V, unless otherwise noted. All voltages are relative to GND and are based on PMI8952 interface charger.						
USB Type-C interface and detection						
DFP_I_SRC_ STDUSB	Standard USB current source	In downstream facing port (DFP) mode	64	80	96	µA
Rd	Rd pull-down resistor to ground	In upstream facing port (UFP) mode	4.59	5.1	5.61	kΩ
Ra	Ra pull-down resistor to ground	Powered cable attached	800	–	1200	kΩ
VCLAMP	CC UFP mode clamping threshold	Power off, Vbatt < VUVLO or battery missing	0.70	1.1	1.32	V
VCC_SINK	Voltage on CC pins when device is in sink role (initially UFP)	vRa detected	0.025	–	0.15	V
		vRd-connect detected	0.25	–	2.04	V
		vRd-USB detected	0.25	–	0.61	V
		vRd-1.5 detected	0.7	–	1.16	V
		vRd-3.0 detected	1.31	–	2.04	V
VCC_SOURCE_ DefaultUSB	Voltage on CC pins when device is in sink role (initially UFP) and advertising default USB current	vRa (powered cable/adapter) detected	0	–	0.15	V
		vRd (sink) detected	0.25	–	1.6	V
		No connect (vOPEN)	1.65	–	–	V
tCC_Debounce	The time a port waits before it can determine it is attached	Transitioning between the Attached.Wait state and the Attached.SRC or Attached.SNK states	100	–	200	ms

Table 3-6 Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tPD_Debounce	The time a port waits before it can determine it is either detached or there has been a change in the Type-C current advertisement	Transitioning between the Attached.Wait state and the Attached.SRC or Attached.SNK states	10	–	20	ms
VCONN	VCONN voltage range	VCONN enabled	4.75	–	5.25	V
ILIM_VCONN	VCONN current limit	VCONN enabled and powered from 4.75 V–5.5 V supply with a maximum output power ≥ 1.0 W	210	325	–	mA
tVCONN_ON	Maximum time from when PMI supplies Vbus in the Attached.SRC state to when Vconn reaches 5 V	DFP mode, Vbus ≥ 5 V, VCONN powering on	–	–	2	ms
t_{VBUS_ON}	Maximum time from entering the Attached.SRC state until Vbus reaches 5 V	DFP mode, charger boost enabled	–	275	–	ms

3.6 Output power management

Output power management circuits include:

- Band-gap voltage reference circuit
- Seven SMPS circuits
- 23 LDO linear regulators
- Voltage switches

The PM8953 device provides all the regulated voltages needed for most wireless handset applications. Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, to support power-management sequencing, and to meet different voltage-level requirements.

The PM8953 device provides a total of 30 programmable voltage regulators, with all outputs derived from a common band-gap reference circuit. Each regulator has a low-power mode setting for power savings.

Table 3-7 lists a high-level summary of all regulators and their intended uses.

Table 3-7 PM8953 regulators and their intended uses

Function	Circuit type	Default voltage (V) [1]	Specified range (V) [2] (MSM8953)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8953)
S1	SMPS	0.87	0.4–1.14	0.32–2.04	3000	N	MSM modem
S2	SMPS	0.87	0.4–1.14	0.32–2.04	4000	Y	MSM core and graphics
S3	SMPS	1.225	1.2–1.25	0.32–2.04	2000	Y	LPDDR2 and LPDDR3, MIPI CSI, and DSI. Low-voltage LDOs (1, 2, 3, and 23)
S4	SMPS	2.04	1.2–1.25	0.32–2.04	2000	Y	High-voltage LDOs (4, 5, 6, 7, 16, 19 RFCLK, and XO)
S5	SMPS	0.87	0.4–1.14	0.350–1.355	3750	Y	MSM applications processor
S6	SMPS	0.87	0.4–1.14	0.350–1.355	3750	Y	MSM applications processor
S7	SMPS	0.915	0.900-1.350V	0.375–1.5625	2000	Y	MSM VDD memory rail (VDDMX)
L1	NMOS LDO	1.000	1.000	0.375–1.5375	600	N	RFICs
L2	NMOS LDO	1.100	1.100	0.375–1.5375	1200	Y	Camera: digital
L3	NMOS LDO	0.925	0.925	0.375–1.5375	600	Y	MSM DSI PLL and USB
L4	PMOS LDO	1.800	1.800	1.750–3.3375	450	N	RFICs and GPS eLNA
L5 [3]	PMOS LDO	1.800	1.800	1.750–3.3375	600	Y	Most digital I/Os, MSM pad groups 3 and 7, LPDDR, and eMMC
L6	PMOS LDO	1.800	1.800	1.750–3.3375	300	N	MSM QFPROM, camera, touchscreen, display, and sensors
L7	PMOS LDO	1.800	1.800	1.750–3.3375	300	Y	MSM analog, USB and PLLs, WCN XO, and PM baseband clock driver
L8	PMOS LDO	2.900	2.900	1.750–3.3375	600	Y	eMMC
L9	PMOS LDO	V_{out} = 3.3 V for VBAT > 3.575 V; V_{out} = 3 V for VBAT < 3.575 V	3.000–3.300	1.750–3.3375	600	N	WCN
L10	PMOS LDO	3.0	3.0	1.750–3.3375	150	N	Sensors and touchscreen
L11 [4]	PMOS LDO	2.950	2.950	1.750–3.3375	800	Y	Micro SD

Table 3-7 PM8953 regulators and their intended uses (cont.)

Function	Circuit type	Default voltage (V) [1]	Specified range (V) [2] (MSM8953)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8953)
L12 [3]	PMOS LDO	2.950	1.800/2.950	1.750–3.3375	50	Y	MSM pad group 2
L13	PMOS LDO	3.125	3.125	1.750–3.3375	150	Y	MSM USB and PMIC and external codec audio
L14 [4]	PMOS LDO	1.800	1.800/3	1.750–3.3375	50	N	MSM pad group 5, dual-voltage UIM1, and NFC
L15 [4]	PMOS LDO	1.800	1.800/3	1.750–3.3375	50	N	MSM pad group 6 and dual-voltage UIM2
L16	PMOS LDO	1.800	1.800	1.750–3.3375	5	N	PMIC HKADC
L17	PMOS LDO	2.850	2.850	1.750–3.3375	300	N	Camera and display
L18	PMOS LDO	2.700	2.700	1.750–3.3375	150	N	QTI RF front-end
L19	NMOS LDO	1.350	1.350	0.375–1.5375	600	N	MSM analog, WCN, and WGR
L20	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC XO circuits
L21	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC RF clock buffers
L22	PMOS LDO	2.800	2.800	1.750–3.3375	150	N	Camera: analog
L23	NMOS LDO	1.15	1.15	0.375–1.5375	600	N	Camera: digital

1. All regulators have default voltage settings, whether or not they default on; the voltage and state depends upon the programmable boot sequencer (PBS) configuration.
2. The specified voltage range is the programmed range for which performance is guaranteed to meet all specifications.
   For usage outside this range, submit a case to QTI for approval.
   NOTE: LDO-rated current specifications are only valid while maintaining their specified headroom.
3. L5 powers internal circuits and limited to 1.8 V operation; its programmed voltage should not be changed, and it should not be turned off.
4. L11, L14, and L15, as well as all PMOS LDOs have OCP.

3.6.1 Reference circuit

All PMIC regulator circuits, and some other internal circuits, are driven by a common, on-chip voltage reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pin to create a low-pass function that filters the reference voltage distributed throughout the device.

NOTE Do not load the REF_BYP pin. Use an odd MPP configured as an analog output if the reference voltage is needed off-chip.

Applicable voltage reference performance specifications are given in Table 3-8.

Table 3-8 Voltage reference performance specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal internal VREF	At the REF_BYP pin	–	1.250	–	V
Output voltage deviations					
■ Normal operation, temperature only	■ Over temperature only, -20 to 120ºC	–	–	TBD	%
■ Normal operation, all	■ All operating conditions	–	–	TBD	%
■ Sleep mode, all	■ All operating conditions	–	–	TBD	%

3.6.2 SMPS S1-S4,S7

The PM8953 device includes five SMPS circuits; the corresponding output is VREG_S1 to VREG_S4 and VREG_S7. It supports PWM, HCPFM, retention mode (low quiescent current), PFM modes, and the automatic transition between PWM and PFM modes, depending on the load current. Pertinent performance specifications are given in Table 3-9.

Table 3-9 HF-SMPS performance specifications

Parameter	Comments [1, 2]	Min	Typ	Max	Units
Output voltage ranges	Programmable range	0.32		2.04	V
Rated load current (I_rated) [3]	Continuous current delivery				
■ PWM mode					
□ S1		3000	–	–	mA
□ S2		4000	–	–	mA
□ S3		2000	–	–	mA
□ S4		2000	–	–	mA
□ S7		2000	–	–	mA
■ PFM mode (all)		200	–	–	mA
■ Retention mode		TBD	–	–	
Over current limit	VREG pin shorted; set value = lim	TBD	TBD	TBD	mA

Table 3-9 HF-SMPS performance specifications (cont.)

Parameter	Comments [1, 2]	Min	Typ	Max	Units
Overall DC voltage output error	Over voltage, temperature, and process variations, plus load and line regulation				
■ PWM mode	■ V_{out} ≥ 0.8 V, I_rated/2	-2	–	2	%
	■ 0.32 ≤ V_{out} < 0.8 V, I_rated/2	-16	–	16	mV
■ PFM and retention mode	■ V_{out} ≥ 0.8 V, I_rated/2	-2	–	4	%
	■ 0.32 ≤ V_{out} < 0.8 V, 100mA	-16	–	40	mV
Enable settling time	Enable to 1% of final value; no load	–	–	500	µs
Enable overshoot	Slow start, no load				
■ V_{out} < 1.0 V		–	–	70	mV
Voltage step settling time per LSB	To within 1% of the final value	–	–	TBD	µs
Load transient response (auto and PWM)	400 mA load step, from 10 mA to I_rated range in > 1µs steps	-50	–	+70	mV
Response to mode transitions	TBD mA load				
■ PWM-to-PFM and vice versa		–50	–	+70	mV
Output ripple voltage	Tested at the switching frequency				
■ PWM pulse-skipping mode	■ 40 mA load; 20 MHz measurement bandwidth	–	20	40	mVpp
■ PWM nonpulse-skipping mode	■ I_rated; 20 MHz measurement bandwidth	–	10	20	mVpp
■ PFM mode	■ 50 or 100 mA load; 20 MHz measurement bandwidth	–	–	50	mVpp
■ High-current PFM	■ 50 or 100 mA load; 20 MHz measurement bandwidth	–	–	70	mVpp
■ Retention mode		–	55	–	mVpp
Load regulation	V_{in} ≥ V_{out} + 1 V; I_load = 0.01 × I_rated to I_rated	–	–	TBD	%
Line regulation	V_{in} = 3.2–4.2 V; I_load = 100 mA	–	–	TBD	%/V
Power-supply ripple rejection	PSRR				
■ 50 Hz–1 kHz		TBD	–	–	dB
■ 1 kHz–100 kHz		TBD	–	–	dB
■ 100 kHz–1 MHz		TBD	–	–	dB
Output noise	–				
■ F < 5 kHz		–	TBD	–	dBm/Hz
■ F = 5 kHz–10 kHz		–	TBD	–	dBm/Hz
■ F = 10 kHz–500 kHz		–	TBD	–	dBm/Hz
■ F = 500 kHz–1 MHz		–	TBD	–	dBm/Hz
■ F > 1 MHz		–	TBD	–	dBm/Hz
Ground current	No load				
■ PWM mode		–	550	–	µA
■ PFM mode (auto)		–	50	–	µA
■ Retention mode		–	1	–	µA

1. All specifications apply over the device's operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
2. Voltage error, efficiency, and output ripple voltage characteristics may degrade if the rated output current is exceeded.
3. The rated load current is the current the regulator can deliver and still maintain regulation. The minimum specification guarantees that the regulators can deliver at least these currents before losing regulation.

<TBD>

Figure 3-1 VREG_S3 efficiency plot (PWM, PFM, and auto mode)

3.6.3 SMPS S5 and S6

The PM8953 device includes two multiphase SMPS circuits that are combined to supply the MSM application processors; their corresponding output pins are VREG_S5 and VREG_S6. PWM, PFM, and pulse-skipping modes are supported. New features introduced in these SMPS are autonomous phase control (APC) and autonomous mode control (AMC).

- APC: During multiphase operation, the phase count is autonomously managed by the hardware to select the appropriate number of phases for optimal efficiency based upon the load current.
- AMC: The hardware manages the selection of PWM or PFM mode based upon the load current.

Table 3-10 lists pertinent **target** performance specifications.

Table 3-10 FT-SMPS performance specifications

Parameter	Comments [1, 2, 3]	Min	Typ	Max	Units
General characteristics					
Output voltage range	■ LV range ■ MV range	0.350 0.700	–	1.350 2.200	V V
CMC NPM or AMC NPM (any number of phases)					
Rated load current	I_rated per phase ■ Single phase ■ Multiphase	 3.75 7.5	 – –	 – –	 A A
DC output voltage accuracy	Including MBG, make tolerance, line and load regulation, and temperature (-30 to 125°C) ■ VREG ≥ 0.8 ■ VREG < 0.8	 -2 -16	 – –	 2 16	 % mV
Ripple voltage	Measured across C_{OUT} where sense lines are tapped	–	7	15	mVpp
Line transient response	GSM burst induced line transient is represented by: Rbat = 350 mΩ, Istep = 2 A with 10 µs slew, and VPH_PWR capacitance = 100 µF	–	–	20	mVpp
CMC NPM or AMC NPM (multiphase)					
Phase current mismatch	Relative to the ideal balanced current	-25	–	+25	%
Ground current					
Ground current CMC NPM	No load, single phase	–	0.55	0.80	mA
Ground current per phase CMC NPM or AMC NPM	No load, multiphase	–	1.9	2.3	mA
Ground current CMC LPM	No load, single or multiphase (sleep configuration commanded LPM)	–	55	90	µA
Ground current per phase AMC LPM	No load, single or multiphase	–	80	110	µA

Table 3-10 FT-SMPS performance specifications (cont.)

Parameter	Comments [1, 2, 3]	Min	Typ	Max	Units
CMC NPM or AMC load transient (any number of phases)					
Response to load transient (undershoot/overshoot)	2 A load step per phase Transient step ~100 ns, 1 V output [4]	-50	–	80	mV
CMC LPM or AMC LPM, CPC, or APC (any number of phases)					
DC output voltage accuracy	Including MBG, make tolerance, line and load regulation, and temperature (-30 to 125°C) ■ VSET ≥ 0.8 V ■ VSET < 0.8 V	 -2 -16	 – –	 4 32	 % mV
Ripple voltage	Measured across C_{OUT} where sense lines are tapped ■ Single phase ■ Multiphase	 – –	 25 20	 40 35	 mVpp mVpp
CMC LPM (any number of phases)					
Rated load current	–	–	0.8	–	A
Transition specifications					
Phase-adding warm up time	NPM CPC change in phase count	–	25	–	µs
Phase current settling time	Time to achieve the phase-current match (steady state loading, all active phases in CCM, and change in the phase count)	–	–	200	µs
Other general characteristics					
Enable settling time	V_{OUT} slewing to within 1% of the final value	–	200	–	µs
Voltage stepper (undershoot/overshoot)	1 LSB step slewing	-5	–	5	mV
Peak output impedance	1 kHz–1 MHz	–	–	40	mΩ
Discharge impedance	–	–	32	–	Ω

1. General specifications apply overall operating conditions of supply, temperature, process, and component variances, except where noted otherwise.
2. Default components are assumed (470 nH, 2 × 22 µF per phase) along with deployed configurations for the MSM8953 chipset.
3. Where parametric performance is influenced by external components, baseline components are assumed. Values listed are the component's specified values, not the derated values. Derating must be accounted for to ensure robustness. The initial assumption is 50% derating on capacitors pending further assessment of specific component selections (an approximate allowance for temperature, tolerance, and voltage derating).
4. + 100 mV maximum overshoot for V_{OUT} < 0.7 V.

TBD

Figure 3-2 VREG_S5 and VREG_S6 efficiency plot (auto mode)

3.6.4 Linear regulators

Eight designs are used to implement the 23 LDO linear regulators within the PMIC:

- NMOS rated for 1200 and 600 mA (N1200 and N600)
- PMOS rated for 600, 450, 300, 150, and 50 mA (P600, P450, P300, P150, and P50)
- Low-noise PMOS for on-chip clock circuits (VREG_L16 for HKADC circuits, VREG_L20 for XO circuits, and L21 for RF_CLK buffers)
  - Each design has a maximum no-load ground current of 80 µA.
  - Since these LDOs are not used off-chip, their other performance specifications are not published.

All other LDO performance specifications are presented in Table 3-11.

Table 3-11 LDO performance specifications

Parameter	Comments [1]	Min	Typ	Max	Units
Output voltage (programmable range)					
■ All NMOS	■ 12.5 mV steps	0.375	–	1.5375	V
■ All PMOS	■ 12.5 V steps	1.75	–	3.3375	V
Rated load current (I_rated), normal [2]	Continuous current delivery				
■ N1200		–	–	1200	mA
■ N600		–	–	600	mA
■ P600		–	–	600	mA
■ P450		–	–	450	mA
■ P300		–	–	300	mA
■ P150		–	–	150	mA
■ P50		–	–	50	
Rated load current, LPM [2]	Continuous current delivery				
■ N1200		–	–	100	mA
■ P50		–	–	5	mA
■ All others		–	–	10	mA
Maximum pass FET power dissipation	–	–	–	600	mW
Overall DC voltage output error	Over-voltage, temperature, and process variations plus load and line regulation				
■ Normal mode					
□ At default voltage		-2	–	2	%
□ At nondefault voltages		-3	–	3	%
■ Low-power mode					
□ At default voltage		-4	–	4	%
□ At nondefault voltages		-5	–	5	%
Temperature coefficient	–	-100	–	100	ppm/°C
Transient settling time [3]	To within 1% of the final value	20	100	200	µs
Load transient overshoot/undershoot [3]					
■ N1200	0.25 × I_rated to 0.75 × I_rated load step	-4	–	4	%
■ N600	0.01 × I_rated to I_rated load step	-3	–	3	%
■ All PMOS LDOs	0.10 × I_rated to 0.90 × I_rated load step	-70	–	100	mV
Dropout voltage [4, 5]	Load at I-rated				
■ N1200, normal mode		–	–	120	mV
■ N1200, LPM		–	–	15	mV
■ N600, normal mode		–	–	120	mV
■ N600, LPM		–	–	15	mV
■ All PMOS LDOs, both modes		–	–	300	mV

Table 3-11 LDO performance specifications (cont.)

Parameter	Comments [1]	Min	Typ	Max	Units
NMOS power-supply ripple rejection	PSRR				
■ Normal mode					
□ 50 Hz–1 kHz		60	70	–	dB
□ 1 kHz–10 kHz		–	60	–	dB
□ 10 kHz–100 kHz		–	TBD	–	dB
□ 100 kHz–1 MHz					
– N1200		–	TBD	–	dB
– N600		–	TBD	–	dB
■ Low-power mode					
□ 50 Hz–1 kHz		–	50	–	dB
□ 1 kHz–100 kHz		–	40	–	dB
PMOS power-supply ripple rejection	Normal mode				
■ 50 Hz–1 kHz		43	–	–	dB
■ 1 kHz–10 kHz		35	–	–	dB
■ 10 kHz–100 kHz		13	–	–	dB
■ 100 kHz–1 MHz		13	–	–	dB
Soft current limit during startup	Normal mode; current above I_rated				
■ NMOS LDOs		–	–	100	mA
■ PMOS LDOs		–	–	150	mA
Bypass mode on-resistance					
■ N1200		–	TBD	TBD	mΩ
■ N600		–	–	TBD	Ω
■ P600		–	0.56	0.84	Ω
■ P450		–	0.75	1.12	Ω
■ P300		–	1.10	1.66	Ω
■ P150		–	2.20	2.40	Ω
■ P50		–	6.60	10	Ω
Ground current with load	Percentage of load current	–	–	0.5	%
Ground current, no load	Measured at the battery. I and Q may be much higher if LDO is operated in dropout condition.				
■ Normal mode					
□ N1200		–	TBD	TBD	µA
□ N600		–	TBD	TBD	µA
□ All PMOS LDOs		–	TBD	TBD	µA
■ Low-power mode					
□ N1200		–	TBD	TBD	µA
□ N300		–	TBD	TBD	µA
□ All PMOS LDOs		–	TBD	TBD	µA

Table 3-11 LDO performance specifications (cont.)

Parameter	Comments [1]	Min	Typ	Max	Units
Ground current, bypass mode	–				
■ All NMOS LDOs		–	TBD	TBD	µA
■ All PMOS LDOs		–	–	1	µA
OCP threshold					
■ P50	–				
■ P150		163.3	245	411	mA
■ P300		309	477	641	mA
■ P450		583	747	993	mA
■ P600		TBD	TBD	TBD	TBD
		885.2	1277	1732	mA

1. All specifications apply over the device's operating conditions, load current range, and capacitor ESR range, unless noted otherwise.
2. Rated current is the current at which all specifications are met. Higher currents are allowed during normal operation, but more headroom is needed to maintain performance. The low-power mode's current rating should not be exceeded; if so, switch to the normal mode.
3. The stated transient response performance is achieved regardless of the transitory mode— turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.
4. LDO voltage dropout measurement:
   –Program the LDO for its desired operating voltage (V_set_d).
   –Measure the output voltage; call this value V_set_m.
   –Adjust the load so that the LDO delivers its rated output current (I_rated).
   –Adjust the input voltage until V_in = V_set_m + 0.5 V.
   –Decrease V_{in} until V_{out} drops 100 mV (until V_{out} = V_set_m - 0.1 V); call the resulting input value V_in_do, and call this output value V_out_do.
   –The voltage drop across the regulator under this condition is the dropout voltage (V_do = V_in_do - V_out_do).
   –The LDO can be in bypass mode where the output could potentially be lower than its input voltage. The input voltage to the LDO should be greater than 1 V when in bypass mode.
5. The dropout voltage is specified at the full rated current of the LDO. The voltage headroom required to maintain the LDO in regulation depends on the load current of the LDO. The current that an LDO can provide needs to be de-rated based on the headroom. For example, the 600 mA PMOS LDO has a dropout voltage of 300 mV. When headroom is 150 mV, the PMOS LDO can provide 600 × (150/300) = 300 mA current without going out of regulation.

3.6.5 Internal voltage-regulator connections

Some regulator supply voltages are connected internally to power other PMIC circuits. These circuits do not operate properly unless their supplies are correct; this requires:

- Certain regulator supply voltages must be delivered at the correct values.
- Corresponding regulator sources must be enabled and set to the proper voltages.

Table 3-12 summarizes these requirements.

Table 3-12 Internal voltage regulator connections

Regulator	Default	Usage	Comments
VREG_S3	1.225 V	MPPs, GPIOs, and VREF_LPDDR	Also loaded externally
VREG_L5	1.800 V	PON, SLEEP_CLK, SPMI, Digital I/Os, MPPs, and GPIOs	Also loaded externally
VREG_L7	1.800 V	Baseband clock drivers	Also loaded externally
VREG_L13	3.075 V	Microphone bias	Also loaded externally
VREG_L16	1.800 V	AMUX and HKADC circuits	Plus thermistor circuits only
VREG_XO	1.800 V	XO circuits	Do not load externally
VREG_RFCLK	1.800 V	RF clock output buffers	Do not load externally

3.7 General HK

The PMIC includes circuits that support handset-level HK functions—various tasks that must be performed to keep the handset in order. Integration of these functions reduces the external parts count and the associated size and cost. HK functions include an analog switch matrix, multiplexers, and voltage scaling; an HK/XO ADC circuit; system clock circuits; a real-time clock for time and alarm functions; and overtemperature protection.

3.7.1 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage-scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in Table 3-13.

Table 3-13 Analog multiplexer and scaling functions

Ch #	Description	Typical input range (V) 3	Scaling	Typical output range (V)
0–3	–	–	–	–
4	–	–	–	–
5	VCOIN pin	2.0–3.25	1/3	0.67–1.08
6	–	–	–	–
7	VPH_PWR pin	2.5–TBD	1/3	0.83–1.50
8	Die temperature monitor	0.4–0.9	1	0.4–0.9
9	0.625 V reference voltage	0.625	1	0.625
10	1.25 V reference voltage	1.25	1	1.25
11	–	–	–	–
12	Buffered 0.625 V reference voltage	0.63	1	0.63
13	–	–	–	–

Table 3-13 Analog multiplexer and scaling functions (cont.)

Ch #	Description	Typical input range (V) [3]	Scaling	Typical output range (V)
14–15 [1]	GND_REF and VDD_ADC	Direct connections to ADC for calibration	–	–
16–19	MPP_01–MPP_04 pins	0–1.7	1	0–1.7
20–31	–	–	–	–
32–35	MPP_01–MPP_04 pins	0.3–TBD	1/3	0–1.7
36–49	–	–	–	–
50	XO_THERM pin direct	0.1–(VL16 - 0.05)	1	0.1–(VL16 - 0.05)
51–53	–	–	–	–
54	PA_THERM pin	0.1–(VL8 - 0.05)	1	0.1–(VL8 - 0.05)
55-59	–	–	–	–
60	XO_THERM through AMUX	0.1–(VL16 - 0.05)	1	0.1–(VL16 - 0.05)
61–62	–	–	–	–
63	Module power off [2]	–	–	–

1. Channels 14 and 15 are for ADC calibration purposes; these signals do not connect to the AMUX input, but rather connect to the ADC input directly.
2. Channel ID 255 should be selected when the analog multiplexer is not being used; this prevents the scalers from loading the inputs.

NOTE Gain and offset errors are different through each analog multiplexer channel. Each path should be calibrated individually over its valid gain and offset settings for best accuracy.

Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 3-14.

Table 3-14 Analog multiplexer performance specifications

Parameter	Comments [1]	Min	Typ	Max	Units
Supply voltage (VL16)	Connected internally to VREG_L16	–	1.8	–	V
Output voltage range	–				
■ Full specification compliance		0.10	–	VL16 - 0.10	V
■ Degraded accuracy at edges		0.05	–	VL16 - 0.05	V
Input referred offset errors	–				
■ Channels with × 1 scaling		-2.0	–	2.0	mV
■ Channels with 1/3 scaling		-1.5	–	1.5	mV
■ Channels with 1/6 scaling		-3.0	–	3.0	mV
Gain errors, including scaling	Excludes VREG_L16 output error				
■ Channels with × 1 scaling		-0.20	–	0.20	%
■ Channels with 1/3 scaling		-0.15	–	0.15	%
■ Channels with 1/6 scaling		-0.30	–	0.30	%
Integrated nonlinearity (INL)	Input referred to account for scaling	-3	–	3	mV

Table 3-14 Analog multiplexer performance specifications (cont.)

Parameter	Comments [1]	Min	Typ	Max	Units
Input resistance	Input referred to account for scaling				
■ Channels with × 1 scaling		10	–	–	MΩ
■ Channels with 1/3 scaling		1	–	–	MΩ
■ Channels with 1/6 scaling		0.5	–	–	MΩ
Channel-to-channel isolation	1 V AC input at 1 kHz	50	–	–	dB
Output settling time [2]	C_{load} = 28 pF	–	–	25	µs
Output noise level	f = 1 kHz	–	–	2	µV/Hz$^{1/2}$

1. Multiplexer offset error, gain error, and INL are measured, as shown in Figure 3-3. Supporting comments include:
   - The nonlinearity curve is exaggerated for illustrative purposes.
   - Input and output voltages must stay within the ranges stated in Table 3-13; voltages beyond these ranges result in nonlinearity and are beyond the specification.
   - The offset is determined by measuring the slope of the endpoint line (m) and calculating its Y-intercept value (b): Offset = b = y_1 - m × x_1
   - The gain error is calculated from the ideal response and the endpoint line as the ratio of their two slopes (in percentage): Gain_error = [(slope of endpoint line)/(slope of ideal response) - 1] × 100%.
   - NL is the worst-case deviation from the endpoint line. The endpoint line removes the gain and offset errors to isolate nonlinearity:
     INL(min) = min[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]
     INL(max) = max[V_{out}(actual at V_x input) - V_{out}(endpoint line at V_x input)]
2. The AMUX output and a typical load is modeled in Figure 3-4. After S1 closes, the voltage across C2 settles within the specified settling time.

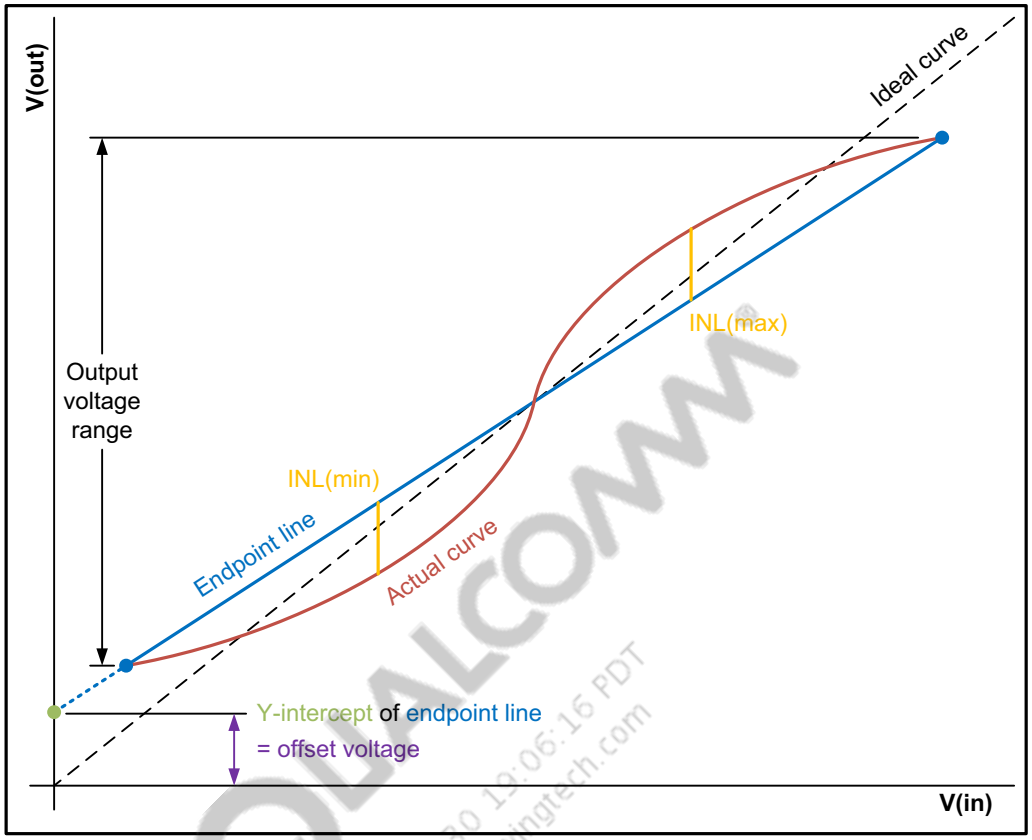


Figure 3-3 Multiplexer offset and gain errors

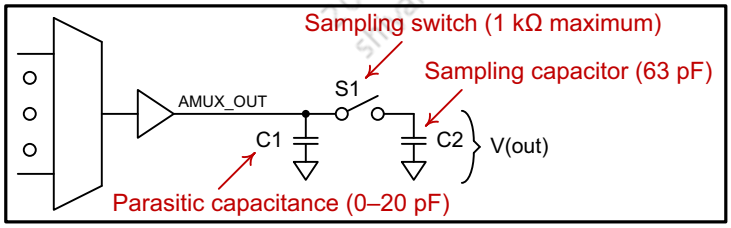


Figure 3-4 Analog multiplexer load condition for settling time specification

Table 3-15 AMUX input to ADC output end-to-end accuracy

AMUX Channel #	Function	Typical input range		Auto scale	Typical output range		AMUX input to ADC output, end-to-end accuracy corresponding to min or max input V, RSS(%) [1, 2]				AMUX input to ADC output, end-to-end accuracy corresponding to min or max input V, WCS(%)[1, 3]				Recommended calibration method [4]
		Min (V)	Max (V)		Min (V)	Max (V)	Without calibration		Internal calibration		Without calibration		Internal calibration		
							At min V	At max V	At min V	At max V	At min V	At max V	At min V	At max V	
5	VCOIN pin	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute
7	VPH_PWR pin	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute
8	Die-temp monitor	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute
9	0.625 V reference	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute, part of calibration
10	1.25 V reference	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute, part of calibration
12	Buffered 0.625 reference	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute, part of calibration
14, 15	ADC GND and VDD	Direct connections to ADC for calibration					–	–	–	–	–	–	–	–	–
16–19	MPP_01–MPP_04	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute or ratiometric depending on application
32–35	MPP_01–MPP_04	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Absolute or ratiometric, depending on application
50	XO_THERM direct	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Ratiometric
54	PA_THERM	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Ratiometric
60	XO_THERM through AMUX	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Ratiometric
255	Module power off	–	–	–	–	–	–	–	–	–	–	–	–	–	–

1. The minimum and maximum accuracy values correspond to the minimum and maximum input voltage to the AMUX channel.
2. Accuracy is based on the root sum square (RSS) of the individual errors.
3. Accuracy is based on the worst-case straight sum (WCS) of all errors.
4. Absolute uses 0.625 V and 1.25 V MBG voltage reference as calibration points. Ratiometric uses the GND_XO and VREF_XO_THM as the calibration points.

3.7.2 HK/XO ADC circuit

The analog-to-digital converter (ADC) circuit is shared by the HK and 19.2 MHz XO functions. A 2:1 analog multiplexer selects which source is applied to the ADC:

- The HK source: the analog multiplexer output discussed in Section 3.7.1

  or

- The XO source: the thermistor network output that estimates the 19.2 MHz crystal temperature

Table 3-16 lists HK/XO ADC performance specifications.

Table 3-16 HK/XO ADC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage	Connected internally to VREG_L16	–	1.8	–	V
Resolution	–	–	–	15	bits
Analog-input bandwidth	–	–	100	–	kHz
Sample rate	XO/8	–	2.4	–	MHz
Offset error	Relative to full-scale	-1	–	1	%
Gain error	Relative to full-scale	-1	–	1	%
INL	15-bit output	-8	–	8	LSB
DNL	15-bit output	-4	–	4	LSB

3.7.3 System clocks

The PMIC includes several clock circuits whose outputs are used for general HK functions and elsewhere within the handset system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an MP3 clock output, an RC oscillator, and sleep-clock outputs. Performance specifications for these functions are described in Section 3.7.3.1 to Section 3.7.3.5.

3.7.3.1 19.2 MHz XO circuits

An external crystal is supplemented by on-chip circuits to generate the desired 19.2 MHz reference signal. Using an external thermistor network, the on-chip ADC, and advanced temperature compensation software, the PMIC eliminates the large and expensive VCTCXO module required by previous generation chipsets. The XO circuits initialize and maintain valid pulse waveforms and measure time intervals for higher-level handset functions. Multiple controllers manage the XO warm-up and signal buffering and generate the desired clock outputs (all derived from one source):

- The low-noise RF outputs RF_CLK1, RF_CLK2, and RF_CLK3 are enabled internally.
- The low-power baseband output BB_CLK1 is enabled by a dedicated control pin BB_CLK1_EN; this output is used as the MSM clock signal.
- The low-power baseband output BB_CLK2 is enabled internally or can be enabled via a properly configured GPIO_2.

Since the different controllers and outputs are independent, circuits other than those needed for the WAN can operate even while the modem IC is asleep and its RF circuits are powered down.

The XTAL_19M_IN and XTAL_19M_OUT pins are incapable of driving a load; the oscillator is significantly disrupted if either pin is externally loaded.

As described in Section 3.7.3.4, an RC oscillator drives some clock circuits until the XO source is established.

Table 3-17 lists the 19.2 MHz XO circuit and related performance specifications.

Table 3-17 XO controller, buffer, and circuit performance specifications

Parameter	Comments	Min	Typ	Max	Units
XO circuits					
Operating frequency	Set by the external crystal	–	19.2	–	MHz
Startup time ■ Normal	–	 –	 –	 10	 ms
Supply voltage = VREG_XO (VREG_L20)	Input buffer and core XO circuits	–	1.80	–	V
Low-noise RF clock outputs: RF_CLKx					
Voltage swing	–	–	1.74	–	Vpp
Duty cycle	–	48	50	52	%
Buffer output impedance ■ At 1 × drive strength ■ At 2 × drive strength ■ At 3 × drive strength ■ At 4 × drive strength	–	 39 30 24 15	 50 40 30 50	 65 50 38 30	 Ω Ω Ω Ω
Phase noise, normal-power mode ■ At 10 Hz ■ At 100 Hz ■ At 1 kHz ■ At 10 kHz ■ At 100 kHz ■ At 1 MHz	–	 – – – – – –	 – – – – – –	 TBD TBD TBD TBD TBD TBD	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Output buffer supply	VREG_RFCLK (VREG_L21)	–	1.74	–	V
Power-supply current ■ One RF clock ■ Two RF clocks	VREG_RFCLK (VREG_L21)	 – –	 TBD TBD	 – –	 mA mA

Table 3-17 XO controller, buffer, and circuit performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Low-power baseband clock outputs: BB_CLKx					
Output levels	–				
■ Logic high (V_{OH})		0.65 × Vdd	–	–	V
■ Logic low (V_{OL})		–	–	0.35 × Vdd	V
Output duty cycle	–	44	50	56	%
USB jitter	Specified values are peak-to-peak period jitter				
■ 0.5–2 MHz		–	–	TBD	ps
■ > 2 MHz		–	–	TBD	ps
Equivalent phase noise [1, 2]	–				
■ 100 Hz–1 kHz		–	–	TBD	dBc/Hz
■ 1–10 kHz		–	–	TBD	dBc/Hz
■ 10–100 kHz		–	–	TBD	dBc/Hz
■ > 100 kHz		–	–	TBD	dBc/Hz
Buffer output impedance	Current drive capabilities meet the output levels specified in this table				
■ At 1 × drive strength		39	50	65	Ω
■ At 2 × drive strength		30	40	50	Ω
■ At 3 × drive strength		24	30	38	Ω
■ At 4 × drive strength		15	30	30	Ω
Output buffer supply voltage	VREG_L7	1.782	1.80	1.818	V
Power-supply current	VREG_L7	–	0.98	1.0	mA
Divided down XO clock outputs: DIV_CLKx					
Buffer output impedance	–				
■ At low GPIO drive strength		30	42	76	Ω
■ At medium GPIO drive strength		21	30	55	Ω
■ At high GPIO drive strength		17	22	45	Ω
Phase noise	–				
■ At 100 Hz		–	TBD	–	dBc/Hz
■ At 1 kHz		–	TBD	–	dBc/Hz
■ At 10 kHz		–	TBD	–	dBc/Hz
■ At 100 kHz		–	TBD	–	dBc/Hz
■ At 250 kHz		–	TBD	–	dBc/Hz
■ At 500 kHz		–	TBD	–	dBc/Hz

1. 20 pF load capacitor.
2. Phase noise and jitter specifications include all aggressor module loading use cases (not only the baseline specifications).

3.7.3.2 19.2 MHz XO crystal requirements

Crystal performance is critical to a wireless product's overall performance. Guidance is available within the *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* document (80-V9690-19). This document includes:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
- Description of various schematic options

3.7.3.3 MP3 clock

GPIO_1 can be configured as a 9.6 MHz clock output to support MP3 in low-power mode. This clock is a divided-down version of the 19.2 MHz XO signal. Output characteristics (voltage levels, drive strength, and so on) are defined in Section 3.4.

Table 3-18 MP3 clock performance specifications

Parameter	Comments	Min	Typ	Max	Units
Operating frequency	–	–	9.6	–	MHz
Output voltage swing	±1%	1.782	1.8	1.818	V
GPIOC output driver impedance	–				
■ Low strength driver		70	100	130	Ω
■ Medium strength driver		45	60	75	Ω
■ High strength driver		25	36	47	Ω
Phase noise	–				
■ At 100 Hz		–	–	-85	dBc/Hz
■ At 1 kHz		–	–	-95	dBc/Hz
■ At 10 kHz		–	–	-100	dBc/Hz
■ At 100 kHz		–	–	-105	dBc/Hz
■ At 250 kHz		–	–	-105	dBc/Hz
■ At 500 kHz		–	–	-105	dBc/Hz
■ At 1 MHz		–	–	-105	dBc/Hz

3.7.3.4 RC oscillator

The PMIC includes an on-chip RC oscillator that is used during startup and as a backup to other oscillators. Pertinent performance specifications are listed in Table 3-19.

Table 3-19 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Frequency (trimmed 25°C)	–	17	19	21	MHz
Frequency accuracy (trimmed 25°C)	–	-10.5	–	10.5	%
Frequency (trimmed, overall)	–	16	19	22	MHz
Frequency accuracy (trimmed, overall)	–	-16	–	16	%

Table 3-19 RC oscillator performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Temperature coefficient	–	–	300	–	ppm/°C
Duty cycle	–	30	50	70	%
Current	Current includes 50 µA from the 19.2 MHz RC oscillator + 25 µA load current from the dVdd digital clock driver loads.	–	TBD	–	µA

3.7.3.5 Sleep clock

The sleep clock is generated in one of three ways:

- Using the calibrated low-frequency RC oscillator, periodically uses the 19.2 MHz XO signal for calibration, achieving accuracy suitable for the real-time clock without an external crystal
- Using the 19.2 MHz XO circuit and dividing its output by 586 to create a 32.7645 kHz signal; this signal is used as the startup sleep clock
- Using the on-chip 19.2 MHz RC oscillator instead of the XO signal; this results in a much less accurate and less stable 32.7645 kHz signal that is used for backup only—it is never used in normal modes

The PMIC sleep-clock output is routed to the modem IC via SLEEP_CLK. It is also available for other applications using properly configured GPIOs.

Related specifications presented elsewhere include:

- 19.2 MHz XO circuits (Section 3.7.3.1)
- 19.2 MHz RC oscillator (Section 3.7.3.4)
- Output characteristics (voltage levels, drive strength, and so on.), as defined in Section 3.4.

Table 3-20 Sleep clock jitter specification

Parameter	Comments	Min	Typ	Max	Unit
Cycle-to-cycle jitter	32 kHz XO source (as defined in JEDEC)	–	–	250	ns peak
Period jitter	Same as cycle-to-cycle jitter	–	–	350	ns peak
Period jitter (RMS	19.2 MHz XO/586	–	–	10	ns RMS
Frequency drift	Shift in frequency in any 2.5 s window at a constant temperature	–	–	2	ppm

3.7.4 Real-time clock

Table 3-21 RTC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Tuning resolution	With known calibrated source	–	3.05	–	ppm
Tuning range	–	-192	–	192	ppm
Accuracy (phone off) ■ XO/586 as RTC source ■ CalRC as RTC source ■ CalRC as RTC source	 ■ Phone on ■ Phone off, valid battery present ■ Phone off, coin cell present	 – – –	 – – TBD	 TBD TBD TBD	 ppm ppm ppm

3.7.5 Overtemperature protection (smart thermal control)

The PMIC includes overtemperature protection in stages, depending on the level of urgency as the die temperature rises:

- Stage 0: these are normal operating conditions (less than 105°C).
- Stage 1: 110 to 130°C; an interrupt is sent to the modem IC without shutting down any PMIC circuits.
- Stage 2: 130 to 150°C; an interrupt is sent to the modem IC, and unnecessary high-current circuits are shut down.
- Stage 3: greater than 150°C; an interrupt is sent to the modem IC, and the PMIC is completely shut down.

Temperature hysteresis is incorporated so that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC powers up immediately.

3.8 Audio codec

NOTE All audio codec performance data are collected above PMIC Vbatt of 3.7 V, unless otherwise specified.

3.8.1 Audio codec inputs and Tx processing

All Tx performance parameters are measured with a 1.02 kHz sine wave input signal, capless differential or single-ended inputs, Fs = 48 kHz, 24-bit data, and MCLK = 9.6 MHz or 12.288 MHz.

Table 3-22 Analog microphone input performance [1]

Parameter	Test conditions	Min	Typ	Max	Units
Microphone amplifier gain = 0 dB (minimum gain)					
Input referred noise	Analog input = -200 dBV, A-weighted, bandwidth 20 Hz–20 kHz	–	19.0	24.5	µVrms
Signal-to-noise ratio [2]	Analog input = 0 dBV, A-weighted, bandwidth 20 Hz–20 kHz	92.0	94.0	–	dB
THD + N ratio	f = 1.02 kHz; bandwidth 20 Hz–20 kHz				
	■ Analog input = 0 dBV	–	-85.0	–80.0	dB
	■ Analog input = -1 dBV	–	-85.0	-79.0	dB
	■ Analog input = -60 dBV, A-weighted	–	-35.0	-32.0	dB
Microphone amplifier gain = 6 dB					
Input referred noise	Analog input = -200 dBV, A-weighted, bandwidth 20 Hz–20 kHz	–	10.2	13.0	µVrms
Signal-to-noise ratio [2]	Analog input = -6 dBV, A-weighted, bandwidth 20 Hz–20 kHz	91.0	94.0	–	dB
THD + N	f = 1.02 kHz; bandwidth 20 Hz–20 kHz				
	■ Analog input = -6 dBV	–	-84.0	–79.0	dB
	■ Analog input = -7 dBV	–	-85.0	-78.0	dB
	■ Analog input = -66 dBV, A-weighted	–	-34.0	-30.0	dB
Microphone amplifier gain = 12 dB					
Input referred noise	Analog input = -200 dBV, A-weighted, bandwidth 20 Hz–20 kHz	–	5.6	7.0	µVrms
Signal-to-noise ratio [2]	Analog input = -12 dBV, A-weighted, bandwidth 20 Hz–20 kHz	94.5	96.0	–	dB
THD + N	f = 1.02 kHz; bandwidth 20 Hz–20 kHz				
	■ Analog input = -12 dBV	–	-84.0	–78.0	dB
	■ Analog input = -13 dBV	–	-84.0	-78.0	dB
	■ Analog input = -72 dBV, A-weighted	–	-33.0	-30.0	dB
Microphone amplifier gain = 18 dB					
Input referred noise	Analog input = -200 dBV, A-weighted, bandwidth 20 Hz–20 kHz	–	3.4	5.3	µVrms
Signal-to-noise ratio [2]	Analog input = -18 dBV, A-weighted, bandwidth 20 Hz–20 kHz	87.0	91.0	–	dB
THD + N	f = 1.02 kHz; bandwidth 20 Hz–20 kHz				
	■ Analog input = -18 dBV	–	-84.5	–78.0	dB
	■ Analog input = -19 dBV	–	-84.0	-78.0	dB
	■ Analog input = -78 dBV, A-weighted	–	-31.0	-28.0	dB
Microphone amplifier gain = 21 dB					
Input referred noise	Analog input = -200 dBV, A-weighted, bandwidth 20 Hz–20 kHz	–	3.0	4.2	µVrms
Signal-to-noise ratio [2]	Analog input = -21 dBV, A-weighted, bandwidth 20 Hz–20 kHz	86.0	89.0	–	dB

Table 3-22 Analog microphone input performance [1] (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
THD + N	f = 1.02 kHz; bandwidth 20 Hz–20 kHz				
	■ Analog input = -21 dBV	–	-84.0	-78.0	dB
	■ Analog input = -22 dBV	–	-84.0	-78.0	dB
	■ Analog input = -81 dBV A-weighted	–	-29.5	-25.0	dB
Microphone amplifier gain = 24 dB (maximum gain)					
Input referred noise	Analog input = -200 dBV, A-weighted, bandwidth 20 Hz–20 kHz	–	2.7	3.8	µVrms
Signal-to-noise ratio [2]	Analog input = -24 dBV, A-weighted, bandwidth 20 Hz–20 kHz	84.0	87.0	–	dB
THD + N	f = 1.02 kHz; bandwidth 20 Hz–20 kHz				
	■ Analog input = -24 dBV	–	-82.0	-78.0	dB
	■ Analog input = -25 dBV	–	-82.0	-78.0	dB
	■ Analog input = -84 dBV A-weighted	–	-28.0	-23.0	dB
Frequency response (end-to-end) [3]					
Frequency response	Digital gain = 0 dB; analog gain = 0 dB; Analog input = -20 dBV				
	■ Passband: 20 Hz to 0.4 × Fs	-0.05	0	0.05	dB
	■ Transition band 1 at 0.4375 × Fs	-1.5	–	0.5	dB
	■ Transition band 2 at 0.499 × Fs	–	–	-25.0	dB
	■ Stop-band at 0.5625 × Fs	–	–	-80.0	dB
General requirements					
Absolute gain error	Analog input = 0 dBV, 1.02 kHz	-0.5	0	0.5	dB
Full-scale input voltage	1 kHz input; input signal level required to get 0 dBFS digital output	-0.5	0	0.5	dBV
Power supply rejection	100 mVpp sine wave imposed on PMIC VPH_PWR input; analog input = 0 Vrms, terminated with 0 Ω Terminate inputs with 0 Ω; gain = 0 dB				
	■ 0 < f < 1 kHz	75.0	86.0	–	dB
	■ 1< f < 5 kHz	75.0	82.0	–	dB
	■ 5 < f < 20 kHz	60.0	70.0	–	dB
Inter-modulation distortion (IMD2)	Analog input = 12993 Hz and 14993 Hz equal amplitude tones at -6 dBV; wideband (WB) audio	65.0	85.0	–	dB
	Analog input = 41 Hz and 7993 Hz equal amplitude tones at -6 dBV, WB voice	50.0	90.0	–	dB
	Analog input = 498 Hz and 2020 Hz equal amplitude tones at -6 dBV sine wave, Fs = 8 kHz narrowband (NB) voice	60.0	90.0	–	dB
Input impedance	Input disabled	3.0	–	–	MΩ
Input capacitance	Capless input	–	–	15.0	pF

Table 3-22 Analog microphone input performance [1] (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
Rx → Tx crosstalk attenuation	Tx path measurement with -5 dBFS Rx path signal; f = 1 kHz, separate Tx and Rx grounds				
	■ Rx = EAR	80	97	–	dB
	■ Rx = HPH	80	97	–	dB
	■ Rx = SPKR	80	97	–	dB
Inter-channel isolation	One input terminated with 1 kΩ and the other input gets 1, 10, or 20 kHz at -5 dBFS; 0 dB gain mode; measure the digital output of the terminated channel; separate Tx and Rx grounds				
	■ 1 kHz	90	100	–	dB
	■ 10 kHz	80	90	–	dB
	■ 20 kHz	70	80	–	dB

1. The performance numbers are similar for the MIC1 differential input.
2. The ratio of the output level with the input signal of mentioned dBV and 1.02 kHz sine wave applied to the output level with inputs = -200 dBV, bandwidth 20 Hz–20 kHz.
3. Decimators are in the MSM device's digital codec.

3.8.2 Audio codec outputs and Rx processing

Unless otherwise stated:

- All Rx performance parameters are measured with a 1.02 kHz sine wave input signal, MCLK = 9.6 MHz or 12.288 MHz.
- Receive noise is measured with no dither added to the input signal.
- SNR is calculated as follows:
  - 20 log (full-scale output voltage)/receive noise.

Table 3-23 Ear output performance, 32 Ω load unless specified

Parameter	Test conditions	Min	Typ	Max	Units
Ear: 8/16 kHz, 16 bits					
Receive noise [1]	A-weighted; input = -999 dBFS, 6 dB gain mode, bandwidth 20 Hz–20 kHz	–	7.0	16.0	µVrms
	A-weighted; input = -999 dBFS, 1.5 dB gain mode, bandwidth 20 Hz–20 kHz	–	5.0	12.0	µVrms
Signal-to-noise ratio [2]	Ratio of full-scale output to output noise level, VDD_SPKR_PA = 3.7 V, 6 dB gain mode, bandwidth 20 Hz–20 kHz	100.0	106.0	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_SPKR_PA = 3.7 V, 6 dB gain				
	■ PCMI = 0 dBFS	–	-60.0	–	dB
	■ PCMI = -1 dBFS	–	-80.0	-70.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-34.0	-30.0	dB

Table 3-23 Ear output performance, 32 Ω load unless specified (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
Ear: 48 kHz; 24 bits					
Receive noise [1]	A-weighted; input = -999 dBFS, 6 dB gain mode, bandwidth 20 Hz–20 kHz	–	7.0	12.0	µVrms
	A-weighted; input = -999 dBFS, 1.5 dB gain mode, bandwidth 20 Hz–20 kHz	–	5.0	12.0	µVrms
Signal-to-noise ratio [2]	Ratio of full-scale output to output noise level, VDD_SPKR_PA = 3.7 V, 6 dB gain mode, bandwidth 20 Hz–20 kHz	100.0	106.0	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_SPKR_PA = 3.7 V, 6 dB gain				
	■ PCMI = 0 dBFS	–	-84.0	-75.0	dB
	■ PCMI = -1 dBFS	–	-91.0	-86.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-50.0	-45.0	dB
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 6 dB gain mode	-0.5	–	0.5	Vrms
	f = 1.02 kHz, 1.5 dB gain mode	-0.5	–	0.5	Vrms
Output power [3]	f = 1.02 kHz, 0 dBFS input, 6 dB gain mode, 32 Ω	115.0	126.0	–	mW
	f = 1.02 kHz, -1.5 dBFS input, 6 dB gain mode, 16 Ω	235.0	243.0	–	mW
	f = 1.02 kHz, -3.5 dBFS input, 6 dB gain mode, 10.67 Ω	310.0	320.0	–	mW
Output load	Supported output load	10.0	32.0	–	Ω
Output capacitance	Total capacitance between EARO_P and EARO_M, including PCB capacitance and EMI	–	–	500	pF
Tx → Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal; f = 1 kHz, separate Tx and Rx grounds	90.0	100.0	–	dB
Power supply rejection	100 mVpp sine wave imposed on power supply VDD_SPKR_PA; PCMI = -999 dBFS, 6 dB gain mode				
	■ 0 < f < 1 kHz	70.0	90.0	–	dB
	■ 1 kHz < f < 5 kHz	60.0	82.0	–	dB
	■ 5 kHz < f < 20 kHz	50.0	78.0	–	dB
Disabled output impedance	Measured externally with amplifier disabled	1.0	–	–	MΩ
Output common mode voltage	Measured externally with amplifier disabled	1.50	1.60	–	V
Output DC offset	Input = -999 dBFS measured between differential output	0	0.2	3.0	mV
Turn on/off click-and-pop (CnP) level	A-weighted	–	0.5	2.0	uVpp

1. Receive noise is measured with no dither added to the input signal.
2. SNR is calculated as follows:
   Typical = 20 log (full-scale output voltage (typ))/receive noise (typ)
   Min = 20 log (full-scale output voltage (min))/receive noise (max)

3. For lower loads, the input signal needs to be backed off to avoid clipping. OCP can trigger if not appropriately set. The OCP limit is set to 280 mA for these tests.

Table 3-24 HPH output performance, 16 Ω load unless specified, DRE On

Parameter	Test conditions	Min	Typ	Max	Units
HPH: 8 kHz, 16 bits					
Receive noise (0 dB gain mode) [1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	–	–	dB
	■ PCMI = -1 dBFS	–	-80.0	-70.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-54.0	-50.0	dB
HPH: 48 kHz, 16 bits					
Receive noise (0 dB gain mode)[1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	–	–	dB
	■ PCMI = -1 dBFS	–	-89.0	-76.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-54.0	-50.0	dB
HPH: 48 kHz, 24 bits					
Receive noise (0 dB gain mode)[1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	-82.0	-70.0	dB
	■ PCMI = -1 dBFS	–	-90.0	-85.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-55.0	-49.0	dB
HPH: 96 kHz, 24 bits					
Receive noise (0 dB gain mode)[1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	–	–	dB
	■ PCMI = -1 dBFS	–	-90.0	-80.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-55.0	-50.0	dB

Table 3-24 HPH output performance, 16 Ω load unless specified, DRE On (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
HPH: 192 kHz, 24 bits					
Receive noise (0 dB gain mode)[1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	–	–	dB
	■ PCMI = -1 dBFS	–	-90.0	-80.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-55.0	-50.0	dB
HPH: 48 kHz, 16 bits, 32 Ω load					
Receive noise (0 dB gain mode) [1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	-85.0	-60.0	dB
	■ PCMI = -1 dBFS	–	-87.0	-82.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-55.0	-50.0	dB
HPH: 48 kHz, 24 bits, 32 Ω load					
Receive noise (0 dB gain mode) [1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	-89.0	-87.0	dB
	■ PCMI = -1 dBFS	–	-90.0	-85.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-56.0	-49.0	dB
HPH: 96 kHz, 24 bits, 32 Ω load					
Receive noise (0 dB gain mode) [1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	–	–	dB
	■ PCMI = -1 dBFS	–	-90.0	–	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-54.0	-50.0	dB

Table 3-24 HPH output performance, 16 Ω load unless specified, DRE On (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
HPH: 192 kHz, 24 bits, 32 Ω load					
Receive noise (0 dB gain mode) [1]	A-weighted; input = -999 dBFS, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	–	1.5	2.9	µVrms
Signal-to-noise ratio (0 dB gain mode) [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	110.0	116.4	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	–	–	dB
	■ PCMI = -1 dBFS	–	-90.0	–	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-55.0	-50.0	dB
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 0 dB FS; 16 Ω or 32 Ω load; VDD_CP = 1.95 V	0.90	1.0	–	Vrms
Output power	f = 1.02 kHz, 0 dB FS, 16 Ω load; VDD_CP = 1.95 V, 0 dB gain mode	54.0	62.0	–	mW
	f = 1.02 kHz, 0 dB FS, 32 Ω load; VDD_CP = 1.95 V, 0 dB gain mode	–	30.0	–	mW
Output load	Supported output load	13.0	16.0	–	Ω
Output capacitance	Total capacitance on HPH output (single-ended), including PCB capacitance and EMI	–	–	1000	pF
Tx-to-Rx crosstalk attenuation	Rx path measurement with -5 dBV Tx path signal; f = 1 kHz, separate Tx and Rx grounds	90.0	100.0	–	dB
Inter-channel isolation (separate GND for HPH_L & HPH_R)	Measured channel output = -999 dBFS, second DAC channel output = -5 dBFS, f = 1 kHz	90.0	97.0	–	dB
Interchannel gain error	Delta between left and right channels, input = 1 kHz at -20 dBFS	–	0	0.30	dB
Interchannel phase error	Delta between left and right channels, input = 1 kHz at -20 dBFS	–	–	0.50	deg
Power supply rejection	100 mVpp sine wave imposed on VPH_PWR; PCMI = -999 dBFS				
	■ 0 < f < 1 kHz	–	-102.0	-99.0	dB
	■ 1 kHz < f < 5 kHz	–	-90.0	-85.0	dB
	■ 5 kHz < f < 20 kHz	–	-75.0	-72.0	dB
Inter-modulation distortion (IMD2)	Digital input = 12993 Hz and 14993 Hz equal amplitude tones at -6 dBFs, WB audio	82.0	89.0	–	dB
	Digital input = 41 Hz and 7993 Hz equal amplitude tones at -6 dBFs, WB voice	80.0	84.0	–	dB
	Analog input = 498 Hz and 2020 Hz equal amplitude tones at -6 dBFS, Fs = 8 kHz, NB voice	85.0	100.0	–	dB
Disabled output impedance	Measured externally, with amplifier disabled	–	–	–	MΩ

Table 3-24 HPH output performance, 16 Ω load unless specified, DRE On (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
Output DC offset	Input = -999 dBFS	–	–	–	mV
Turn on/off CnP level	■ A-weighted, 5 ms, 16 Ω	–	0.15	0.43	mVpp
	■ 32 Ω	–	–	–	mVpp
	■ 10 kΩ	–	–	–	mVpp

1. Receive noise is measured with no dither added to the input signal.
2. SNR is calculated as follows:
   Typical = 20 log (full-scale output voltage (typical))/receive noise (typical)
   Min = 20 log (full-scale output voltage (minimum))/receive noise (maximum)

Table 3-25 Mono speaker driver outputs performance, 8 Ω load and + 12 dB gain unless otherwise specified

Parameter	Test conditions [1]	Min	Typ	Max	Units
SPKR_DRV; 48 kHz, 24 bits					
Receive noise [2]	A-weighted; input = -999 dBFS, VDD_SPKR_PA = 5 V, bandwidth 20 Hz–20 kHz	–	50.0	75.0	µVrms
THD + N	P_{out} = 1.5 W, 1 kHz, VDD_SPKR_PA = 5.5 V	–	-85.0	-80.0	dB
	P_{out} = 1.2 W, 1 kHz, VDD_SPKR_PA = 5 V	–	-86.0	–	dB
	P_{out} = 1 W, 1 kHz, VDD_SPKR_PA = 4.2 V	–	-34.0	-20.0	dB
	P_{out} = 700 mW, 1 kHz, VDD_SPKR_PA = 3.8 V	–	-76.0	-40.0	dB
	P_{out} = 500 mW 1 kHz, VDD_SPKR_PA = 3.7 V	–	-78.0	–	dB
Other characteristics					
Level translation	f = 1 kHz				
	■ Input = -1.5 dBFS, VDD_SPKR_PA = 5.5 V	9.0	10.0	12.0	dBV
Output power (P_{out})	f = 1 kHz				
	■ Vdd = 3.7 V THD + N ≤ 1%; 15 µH + 8 Ω + 15 µH	670	690	–	mW
	■ Vdd = 3.7 V THD + N ≤ 1%; 15 µH + 4 Ω + 15 µH			–	mW
	■ Vdd = 3.8 V THD + N ≤ 1%; 15 µH + 8 Ω + 15 µH	900	1100	–	mW
	■ Vdd = 4.2 V THD + N ≤ 1%; 15 µH + 8 Ω + 15 µH			–	mW
	■ Vdd = 5 V THD+N ≤ 1%; 15 µH + 4 Ω + 15 µH	700	790	–	mW
	■ Vdd = 5.5 V THD+N ≤ 1%; 15 µH + 8 Ω + 15 µH			–	mW
		929	956	–	mW
		1200	1500	–	mW
		1500	2000	–	mW
Power supply rejection	200 mVpp sine wave imposed on PMIC_VBATT; digital input = -999 dBFS [3]				
	■ f = 217 Hz	60.0	79.0	–	dB
	■ f = 1 kHz	60.0	79.0	–	dB
	■ f = 10 kHz	40.0	50.0	–	dB
	■ f = 20 kHz	40.0	50.0	–	dB

Table 3-25 Mono speaker driver outputs performance, 8 Ω load and + 12 dB gain unless otherwise specified (cont.)

Parameter	Test conditions [1]	Min	Typ	Max	Units
Output DC offset	Speaker driver enabled, input = -999 dBFs	-3.0	–	3.0	mV
Efficiency	Vdd = 3.7 V				
	■ P_{out} = 500 mW; 15 µH + 8 Ω + 15 µH	85.0	90.0	–	%
	■ P_{out} = 1 W; 15 µH + 4 Ω + 15 µH	78.0	85.0	–	%
	Vdd = 5 V [4]				
	■ P_{out} = 1 W, 15 µH + 8 Ω + 15 µH	73.0	81.0	–	%
	■ P_{out} = 2 W, 15 µH + 4 Ω + 15 µH	60.0	72.0	–	%
Shutdown current	Amplifier disabled	–	2.0	16.0	µA
Turn on time	–	–	0.2	10	ms
CnP level	No signal, turn on/off, mute/unmute, A-weighted	–	0.6	10	mVpp
Disabled output impedance	Amplifier off	25	–	–	kΩ
VDD/GND inductance	Vdd = 5.5 V, input = 0 dBFS square wave, 20 Hz–20 kHz, 40 hours	–	–	0.5	nH

1. OCP limit is 1.5 A for 8 Ω speaker; 2 A for 4 ohm speaker.
2. Receive noise is measured with no dither added to the input signal.
3. With 200 mVpp sine wave imposed on VSW_BOOST and digital input = -999 dBFS, PSRR is higher than 90 dB typical for all test cases.
4. Minimum efficiency for use cases when VPH_PWR > 4.5 V.

Table 3-26 Mono differential line output performance, 10 kO load and 1000 pF max capacitance unless otherwise specified

Parameter	Test conditions	Min	Typ	Max	Units
LINE_OUT: 8 kHz, 16 bits					
Receive noise [1]	A-weighted; input = -999 dBFS	–	5.5	8.0	µVrms
Signal-to-noise ratio [2]	Ratio of full-scale output to output noise level	100.0	105.0	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	-60.0	-40.0	dB
	■ PCMI = -1 dBFS	–	-79.0	-70.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-39.0	-36.0	dB
LINE_OUT: 48 kHz, 16 bits					
Receive noise [1]	A-weighted; input = -999 dBFS	–	5.5	8.0	µVrms
Signal-to-noise ratio [2]	Ratio of full-scale output to output noise level	100.0	105.0	–	dB

Table 3-26 Mono differential line output performance, 10 kO load and 1000 pF max capacitance unless otherwise specified (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	-60.0	-40.0	dB
	■ PCMI = -1 dBFS	–	-80.0	-70.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-39.0	-36.0	dB
LINE_OUT: 48 kHz, 24 bits					
Receive noise [1]	A-weighted; input = -999 dBFS	–	5.5	8.0	µVrms
Signal-to-noise ratio [2]	Ratio of full-scale output to output noise level, VDD_CP = 1.95 V, bandwidth 20 Hz–20 kHz	101.0	105.0	–	dB
THD + N	Band limited from 20 Hz–20 kHz, VDD_CP = 1.95 V				
	■ PCMI = 0 dBFS	–	-60.0	-40.0	dB
	■ PCMI = -1 dBFS	–	-81.0	-70.0	dB
	■ PCMI = -60 dBFS (A-weighted)	–	-45.0	-42.0	dB
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 0 dBFS	0.90	1.0	–	Vrms
Output load	Measured between LO_P and LO_M	1 K	10 K	–	Ω
Tx-to-Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal. f = 1 kHz	90.0	100.0	–	dB
Power supply rejection	100 mVpp sine wave imposed on VPH_PWR; PCMI = -999 dBFS				
	■ 0 < f < 1 kHz	61.0	72.0	–	dB
	■ 1 kHz < f < 5 kHz	61.0	72.0	–	dB
	■ 5 kHz < f < 20 kHz	60.0	70.0	–	dB
Disabled output impedance	Measured externally, with the amplifier disabled	37.5	–	–	kΩ
Output common mode voltage	PCMI = -999 dBFS	1.52	1.6	1.68	V
Turn on/off CnP level	A-weighted, 10 kΩ	–	0.75	3.0	mVpp

1. Receive noise is measured with no dither added to the input signal.
2. SNR is calculated as follows:
   Typical = 20 log (full-scale output voltage (typical))/receive noise (typical)
   Min = 20 log (full-scale output voltage (minimum))/receive noise (maximum)

3.8.3 Support circuits

Table 3-27 Microphone bias specifications

Parameter	Test conditions	Min	Typ	Max	Units
Output voltage	3 mA microphone load	1.6	–	2.9	V
Output voltage accuracy	–		2.0	3.0	%

Table 3-27 Microphone bias specifications (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
Output current	Two microphone loads of 1–1.5 mA each	2.0	3.0	–	mA
Output noise	0.1 µF bypass	–	3.6	–	µVrms
Power supply rejection	100 mVpp applied to PMIC Vbatt input; microphone bias source current = 1.5 mA; internal input M pin connected to bias				
	■ At 20 Hz	53.0	89.0	–	dB
	■ At 200 Hz–1 kHz	73.0	92.0	–	dB
	■ At 5 Hz	60.0	78.0	–	dB
	■ At 10 kHz	50.0	67.0	–	dB
	■ At 20 kHz	38.0	72.0	–	dB
Intermicrophone isolation	DC current = 50 µA, 2.2 kΩ bias resistor				
	■ 20–200 Hz	70.0	79.0	–	dB
	■ 200 Hz–1 kHz	67.0	70.0	–	dB
	■ 1–5 kHz	67.0	70.0	–	dB
	■ 5–10 kHz	60.0	65.0	–	dB
	■ 10–20 kHz	54.0	62.0	–	dB
	■ 20–80 kHz	32.0	60.0	–	dB
Output capacitor value	External bypass mode	0.08	0.1	0.5	µF
	No external bypass mode	–	–	270	pF

Table 3-28 Boost specifications [1]

Parameter	Test conditions	Min	Typ	Max	Units
Boost efficiency	3.7 V input, 2.2 µH inductor, 600 mA load	84.0	90.0	–	%
	3.7 V input, 2.2 µH inductor, 900 mA load	80.0	83.0	–	%
Absolute voltage accuracy	5.5 V	-3.0	–	3.0	%
Temperature coefficient	600 mA load current	-100	–	100	ppm/°C
Overshoot	Regulator turn on/off, load off, voltage step	–	–	9.0	%
Voltage dip due to transient	6–600 mA current step	–	–	500	mV
Voltage spike due to transient	600–6 mA current step	–	–	500	mV
Settling time	600 mA load current	–	–	200	µs
Load regulation	$V_{in} < V_{out} + 1$ V with load from $I_{rated}/100$ to I_{rated}	–	2.0	3.0	%
Line regulation	600 mA load current	–	–	2.0	%/V
Zero-load idle current	0 mA load current, Vbat = 3.7 V	–	0.5	–	mA
Boost output ripple	600 mA load, 20 µF capacitor, 1.6 MHz clock rate	–	–	80.0	mV

Table 3-28 Boost specifications [1] (cont.)

Parameter	Test conditions	Min	Typ	Max	Units
Boost output voltage	8 Ω	4.0	5.0	5.5	V
	4 Ω	4.0	5.0	5.0	V

1. The boost specifications are valid for both 8 Ω and 4 Ω speaker loads.

3.9 IC-level interfaces

The IC-level interfaces include power-on circuits, the SPMI, interrupt managers, and miscellaneous digital I/O functions like level translators, detectors, and controllers. Parameters associated with these IC-level interface functions are specified in Section 3.9.1 to Section 3.9.4. GPIO and MPP functions are also considered part of the IC-level interface functional block, but they are specified in their own sections (Section 3.10 and Section 3.11, respectively).

3.9.1 Power-on circuits and the power sequences

Dedicated circuits continuously monitor several events that might trigger a power-on sequence. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the modem IC is taken out of reset. The PM8953 device complements the PMI8952 device to meet the system's power management needs. Power sequencing details are shared between the two ICs, so this topic is addressed in the *PM8952/PM8956 and PMI8952 Power Management ICs Design Guidelines/Training Slides* (80-NT390-5), including:

- Power-on circuit block diagrams and descriptions
- Pin assignment descriptions and schematic details showing PMIC interconnections
- Types of triggers and turn on and off trigger events
- Power sequencing and detailed descriptions

The regulators that are included during the initial power-on sequence are determined by the hardware configuration controls (OPT[2:1]), as defined in Section 3.9.2. Example sequences are shown in Figure 3-5 followed by pertinent timing characteristics in Table 3-29.

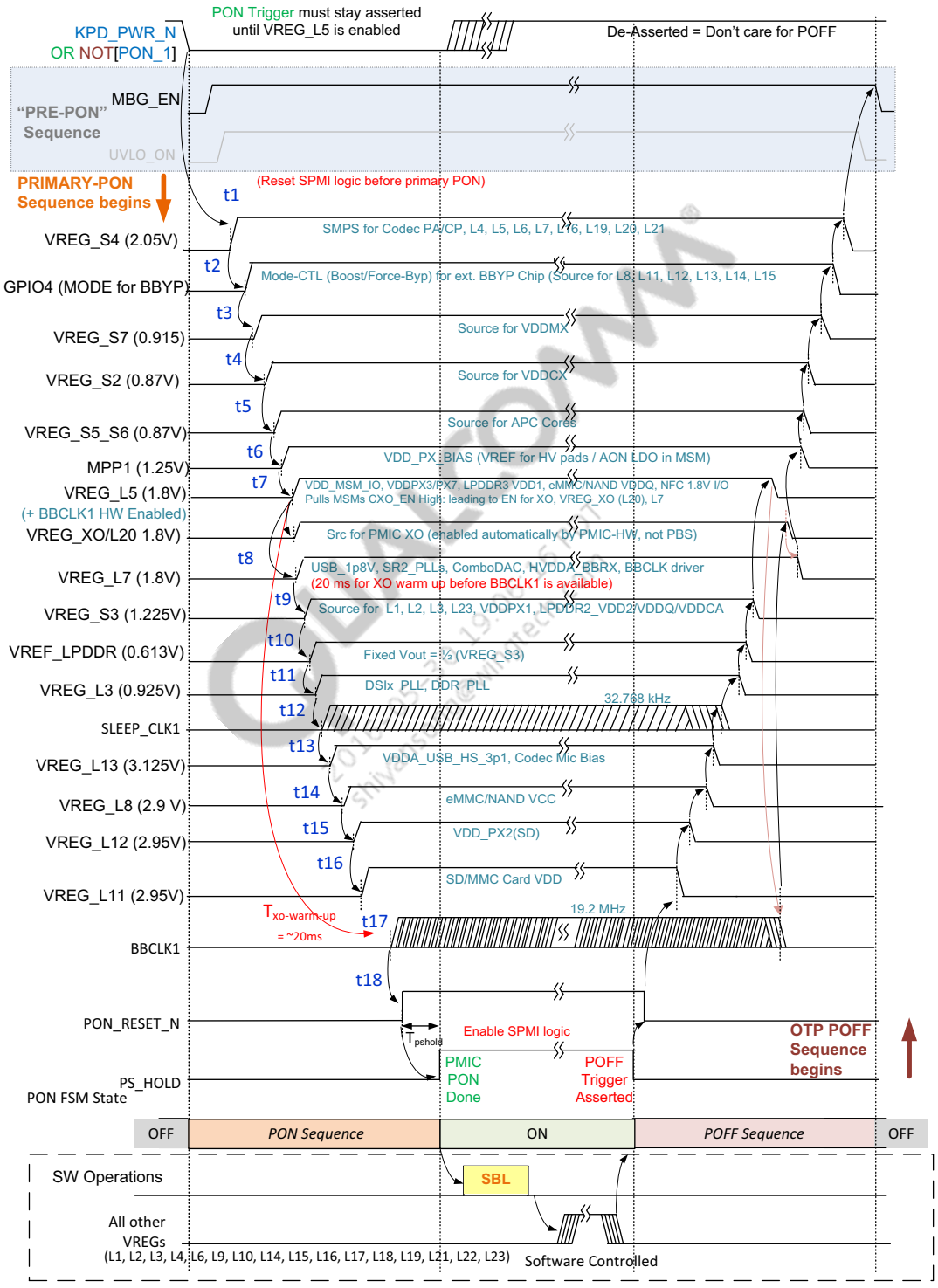


Figure 3-5 PM8953 power-on sequence

Table 3-29 Power-on timing specifications

Parameter	Comments	Min	Typ [2]	Max	Units
t(settle) [3]	Regulator settling time	–	–	300	µs
t(xo)	XO warm-up time	–	15	18	ms
t(ps_hold) [4, 5] ■ Default timeout	PS_HOLD timeout	–	–	240	ms
t(off)	Time between regulator disable signals	–	256	600	µs
KPDPWR_N initiated power-on					
KPDPWR_N	–	0	0	0	ms
VREG_S4 (t1)	–	–	60	–	ms
GPIO4 (t2)		–	0.3	–	ms
VREG_S7 (t3)	–	–	0.07	–	ms
VREG_S2 (t4)	–	–	0.3	–	ms
VREG_S5 (t5)	–	–	0.3	–	ms
MPP_1 (t6)	–	–	0.04	–	ms
VREG_L5, BBLCK1_EN (t7)	–	–	0.3	–	ms
VREG_XO	–	–	–	–	ms
VREG_L7 (t8)	–	–	0.1	–	ms
VREG_S3 (t9)	–	–	0.16	–	ms
VREF_LPDDR (t10)	–	–	0.255	–	ms
VREG_L3 (t11)	–	–	5	–	ms
SLEEP_CLK1 (t12)	–	–	0.15	–	ms
VREG_L13 (t13)	–	–	0.25	–	ms
VREG_L8 (t14)	–	–	0.3	–	ms
VREG_L12 (t15)	–	–	0.12	–	ms
VREG_L11 (t16)	–	–	0.3	–	ms
BBLCK (t17)	~	–	16	–	ms
PON_RESET_N (t18)	–	–	0.2	–	ms

1. Timing is derived from the divided-down XO clock source (32.7645 kHz typical); otherwise, its tolerance depends on the RC clock tolerance.
2. These timings are applicable for the KPDPWR_N initiated PON delay post SBL. Usually these times are higher for the first KPDPWR_N-initiated PON delay.
3. Each regulator settles to within its stated regulator accuracy within the stated regulator settling time. The specified values require the recommended load capacitors. If extra capacitance is used, the settling times can be significantly longer for both **t**(settle) and **t**(reg).
4. PS_HOLD timeout is 1 s during the power-on sequence if the power-on trigger reason is PON_1 and the PON_OPTION_BITS register WIPWR_DEBOUNCE_DLY field is set. PS_HOLD timeout is 200 ms during the power-on sequence for other power-on trigger reasons. PS_HOLD timeout is 200 ms for the warm reset sequence.
5. PS_HOLD timeout is the time after which the PMIC turns off, if PS_HOLD is not yet driven high enough by the MSM/APQ device.

The I/Os to and from the power-on circuits are basic digital control signals that must meet the voltage-level requirements stated in Section 3.4. The KPD_PWR_N and CBL_PWR_N inputs are pulled up to an internal voltage (dVdd). Additional power-on-circuit performance specifications are listed in Table 3-29. More complete definitions for time intervals included in the table are provided in the *PM8953 and PMI8952 Power Management ICs Design Guidelines/Training Slides* (80-P2536).

3.9.2 OPT[2:1] hardwired controls

Two pins (OPT_2 and OPT_1) must be hardwired to ground or VDD or be left open (high-impedance state or Hi-Z); this yields nine possible combinations. Table 3-30 lists the parameters that OPT[2:1] pins use.

Table 3-30 Hardware configuration options

Option pin	Parameter	Configuration
OPT_1 ■ GND ■ Hi-Z ■ VDD	–	 ■ Reserved ■ Reserved ■ Reserved
OPT_2 ■ GND ■ Hi-Z ■ VDD	–	 ■ Reserved ■ Reserved ■ Reserved

Each chipset that uses the PM8953 device must set the OPT pins correctly for its particular application; OPT_1 = Hi-Z and OPT_2 = Hi-Z for MSM8953 chipset.

3.9.3 SPMI and the interrupt managers

The SPMI is a bidirectional, two-line digital interface that meets the voltage and current level requirements stated in Section 3.4.

PMIC interrupt managers support the chipset modem and its processors, and communicate with the modem IC via SPMI. Since the interrupt managers are entirely embedded functions, additional performance specifications are not required.

3.9.4 Undervoltage (UVLO) lockout

The handset supply voltage (VDD) is monitored continuously by a circuit that automatically turns off the device at severely low VDD conditions. UVLO events do not generate interrupts. They are reported to the modem IC via the PON_RESET_N signal. UVLO-related voltage and timing specifications are listed in Table 3-31.

Table 3-31 UVLO performance specifications

Parameter	Comments	Min	Typ	Max	Units
Rising threshold voltage [1]	Programmable value, in 50 mV steps	1.675	2.825	3.225	V
Hysteresis [1]	175 mV setting	125	175	225	mV
	300 mV setting	250	300	350	mV
Falling threshold voltage [2]	175 mV hysteresis setting	1.500	2.650	3050	V
	300 mV hysteresis setting	1.375	2.525	2.925	V
	425 mV hysteresis setting	1.200	2.400	2.800	V
UVLO detection interval	–	–	1	–	µs

1. The hardware default UVLO rising threshold is 2.725 V, and the hysteresis is 175 mV. For handset applications, the UVLO rising threshold and hysteresis are reconfigured in SBL to 2.825 V rising and 425 mV, respectively.
2. The UVLO rising threshold is programmable. UVLO falling threshold = UVLO rising threshold - UVLO hysteresis.

3.10 GPIO specifications

The eight GPIO ports are digital I/Os that can be programmed for a variety of configurations (Table 3-32). Performance specifications for the different configurations are included in Section 3.4.

NOTE Unused GPIO pins should be configured as inputs with 10 µA pull-down.

Table 3-32 Programmable GPIO configurations

Configuration type	Configuration description
Input	■ No pull-up ■ Pull-up (1.5, 30, or 31.5 µA) ■ Pull-down (10 µA) ■ Keeper
Output	■ Open-drain or CMOS ■ Inverted or non-inverted ■ Programmable drive current; see Table 3-33 for options
Input/output pair	Requires two GPIOs; input and output stages can use different power supplies, thereby implementing a level translator (see Table 2-1 for supply options)

GPIOs default to a digital input with 10 µA of pull-down at power on. Before they can be used for their desired purposes, they need to be configured for use.

GPIOs are designed to run at a 4 MHz rate to support high-speed applications. The supported rate depends on the load capacitance and IR drop requirements. If the application specifies load capacitance, then the maximum rate is determined by the IR drop. If the application does not require a specific IR drop, then the maximum rate can be increased by increasing the supply voltage and adjusting the drive strength according to the actual load capacitance.

- GPIO1 is GPIOC-capable where DIV_CLK can be used as general purpose clock output.
- GPIO2, when configured properly, can be used as a pin-controlled BBCLK2 enable.
- GPIO6, when configured properly, can be used for switched antenna diversity for WLAN.
- GPIO5, when configured properly, can be used as BAT_ALARM_IN for BUA application.
- GPIO7, is used for scaled USB VBUS sense to support the USB type C function. Always use a 910 kΩ resistor to connect to the VBUS line.
- GPIO8 controls the external VCONN switch and USB_ID pin of PMI8952 to enable the USB_OTG mode for supporting USB Type C function. For right configuration, refer to the *MSM8953 + PMI8952 + PM8953 Preliminary Reference Schematic* (80-P2472-41).

3.11 Multipurpose pin (MPP) specifications

The PM8953 device includes four MPPs that can be configured for any of the functions specified within Table 3-33. All MPPs are Hi-Z at power on. During power on, PBS programs MPP_1 as an analog output that is used as a reference for modem IC 3 V I/Os.

Table 3-33 MPP performance specifications

Parameter	Comments	Min	Typ	Max	Units
MPP configured as digital input [1]					
Logic high input voltage	–	0.65 × V_M	–	–	V
Logic low input voltage	–	–	–	0.35 × V_M	V
MPP configured as digital output [1]					
Logic high output voltage	$I_{out} = I_{OH}$	V_M - 0.45	–	V_M	V
Logic low output voltage	$I_{out} = I_{OL}$	0	–	0.45	V
MPP configured as analog input (analog multiplexer input)					
Input current	–	–	–	100	nA
Input capacitance	–	–	–	10	pF
MPP configured as analog output (buffered VREF output)					
Output voltage error	-50–50 µA	–	–	30	mV
Temperature variation	Due to buffer only; does not include VREF variation (see Table 3-8)	-0.03	–	0.03	%
Load capacitance	–	–	–	25	pF
Power-supply current	–	–	0.17	0.20	mA
MPPs configured as current drivers (even MPPs only)					
Power supply voltage	–	–	VDD	–	V

Table 3-33 MPP performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Output current	Programmable in 5 mA increments	5	–	40	mA
Output current accuracy	Any programmed current value	-20	–	20	%
Dropout voltage	V_IN - V_OUT with I_OUT within the accuracy limits of its current setting	–	–	1000	mV
Leakage current	Driver disabled	–	105	115	nA

1. Input and output stages can use different power supplies, thereby implementing a level translator (See Table 2-1 for supply options). Other specifications are included in Section 3.4.

NOTE Only odd MPPs (for example, MPP_1 and MPP_3) can be configured as analog outputs. Only even MPPs (for example, MPP_2 and MPP_4) have current sink capability.

4 Mechanical information

4.1 Device physical dimensions

The PM8953 is available in the 187 FOWNSP that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 187 FOWNSP has a 5.78 mm by 5.78 mm body, with a maximum height of 0.65 mm. Pin 1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 187 FOWNSP outline drawing is shown in Figure 4-1.

NOTE Click the following link to download the 187 FOWNSP outline drawing (NT90-P1513-1) from the Qualcomm® CreatePoint website.
The first link is to the BGA pin list reference document; the second link is to the outline drawing.

https://createpoint.qti.qualcomm.com/chipcenter/download/title/0901003981bb721d

https://createpoint.qti.qualcomm.com/chipcenter/download/title/0901003981bb721e

After successfully logging in, the document is downloaded.

NOTE Make this package drawing a favorite to be notified of any change.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

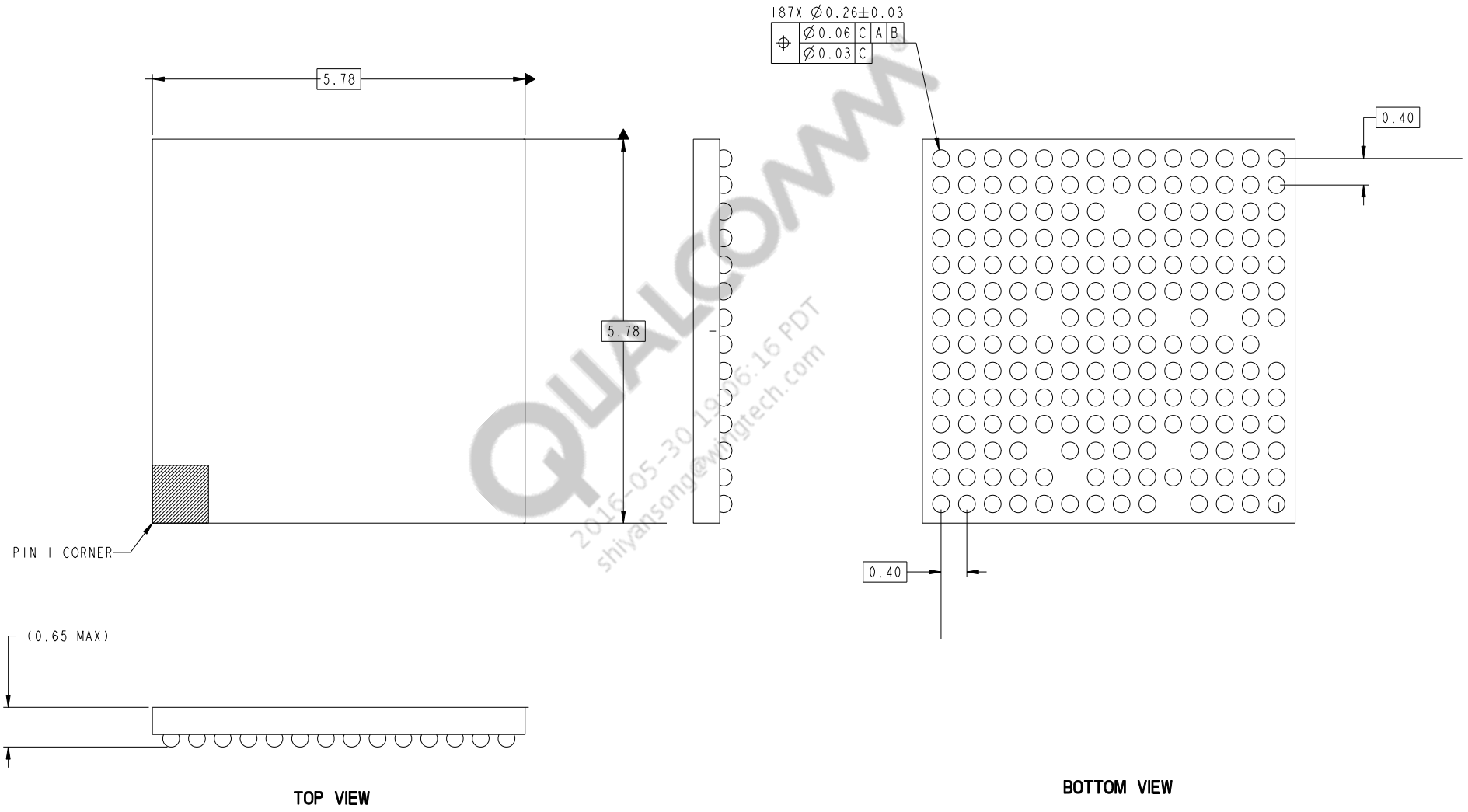


Figure 4-1 187 FOWNSP (5.78 x 5.78 x 0.65 mm) outline drawing

NOTE This is a simplified outline drawing. Click the following link to download the complete, up-to-date package outline drawing. The first link is to the BGA pin list reference document; the second link is to the outline drawing.

https://createpoint.qti.qualcomm.com/chipcenter/download/title/0901003981bb721d

https://createpoint.qti.qualcomm.com/chipcenter/download/title/0901003981bb721e

4.2 Part marking

4.2.1 Specification compliant device

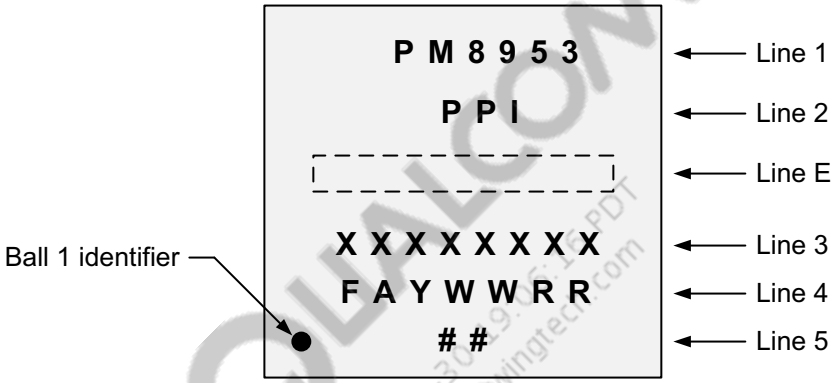


Figure 4-2 PM8953 device marking (top view – not to scale)

Table 4-1 PM8953 Power Management IC device marking line definitions

Line	Marking	Description
1	PM8953	Qualcomm Technologies, Inc. (QTI) product name
2	PPI	P = product configuration code (see Table 4-2) PI = program ID code (see Table 4-2)
E	Blank or random	Additional content as necessary
3	XXXXXXXXX	XXXXXXXXX = traceability information
4	FAYWWRR	F = wafer fab source of supply code ■ F = E for MagnaChip ■ F = P for SMIC A = assembly (ball drop) code ■ A = Z for Nanium, Portugal ■ A = M for STATS ChipPAC, Singapore Y = single-digit year WW = work week (based on calendar year) RR = product revision (see Table 4-2)
5	• ##	• = Dot identifying pin 1 ## = two-digit wafer number

4.3 Device ordering information

4.3.1 Specification compliant devices

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	PM-8953	— 0	— 187	FOWNSP	— TR	— 00	— 0	— VV

Figure 4-3 Device identification code

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

PMIC variant	P value	RR value	HW ID #	S value [1]	PI value [2]
ES/CS sample type					
PM8953 ES	0	00	v1.0	0	VV

1. *S* is the source configuration code that identifies all the qualified die fabrication source combinations available at the time a particular sample type were shipped. S values are defined in Table 4-3.
2. *PI* is the program ID code that identifies an IC's specific OTP programming that distinguishes it from other versions or variants.

Table 4-3 Source configuration code

PMIC	S value	F value
PM8953	S = 0	P = SMIC or E = MagnaChip

4.4 Device moisture-sensitivity level

Surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (Table 4-4) indicates its ability to withstand exposure after it is removed from its shipment bag, while on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device.

Table 4-4 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH; PM8953 rating
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use; after bake, must be reflowed within the time limit specified on the label	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM895x device are classified as MSL1; the qualification temperature was 250°C +0°/-5°C***. This qualification temperature (250°C +0°/-5°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for further discussion).

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the Qualcomm CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the link below to download the PM8953 187 FOWNSP thermal package model from the Qualcomm CreatePoint website.

Icepak model (HS11-P2536-5HW)

https://createpoint.qti.qualcomm.com/search/contentdocument/download/0901003981c1b29e

FLOTHERM model (HS11-P2536-6HW)

https://createpoint.qti.qualcomm.com/search/contentdocument/download/0901003981c1b1de

After you log in successfully, the document is downloaded (assuming you have permission to view it).

NOTE Make this document a favorite to be notified of any changes.

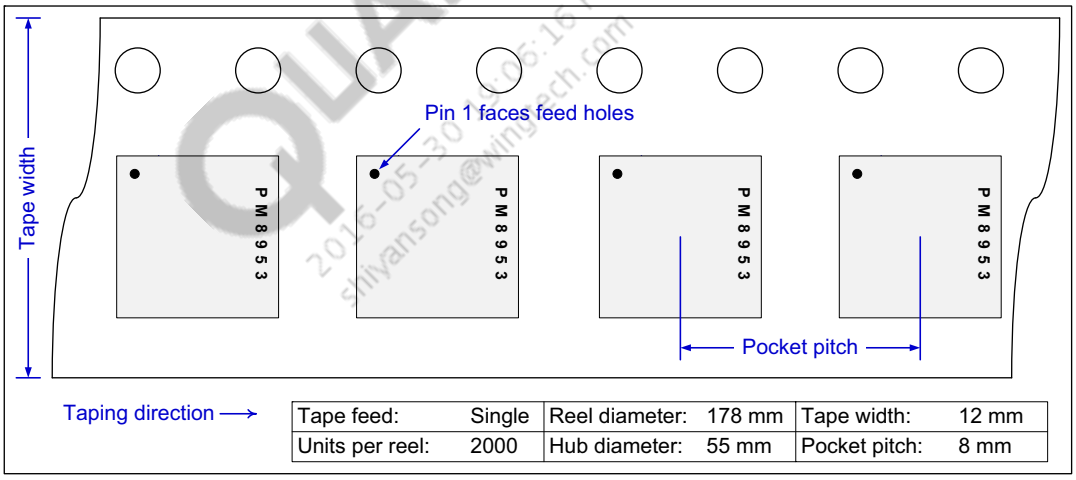
For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards. A simplified sketch of the PM8953 device's tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	178 mm	Tape width:	12 mm
Units per reel:	2000	Hub diameter:	55 mm	Pocket pitch:	8 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

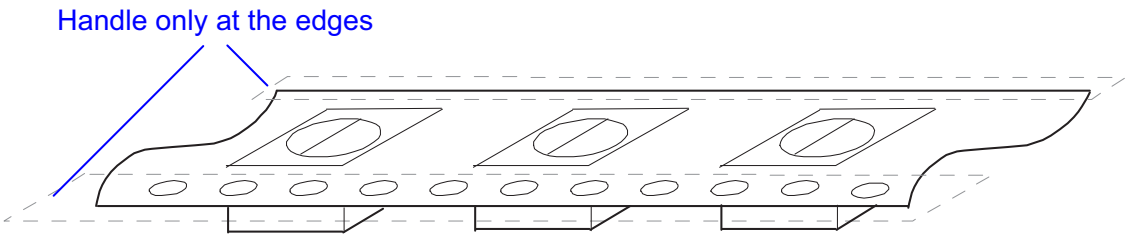


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PM8953 device delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

Wafer-level packages such as the 187 FOWNSP should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Section 7.1 for the PM8953 device's ESD ratings.

5.4 Barcode label and packing for shipment

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The PM8953 device is lead-free and RoHS-compliant. Its SnAgCu solder balls use a SAC405 composition. QTI defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. QTI package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all QTI IC products are described in the *IC Package Environmental Roadmap* (80-VA832-1).

6.2 SMT parameters

This section describes QTI board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land-pattern and stencil recommendations presented in this section are based on QTI internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

QTI recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land-pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solder-able area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). QTI recommends square apertures for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Interaperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

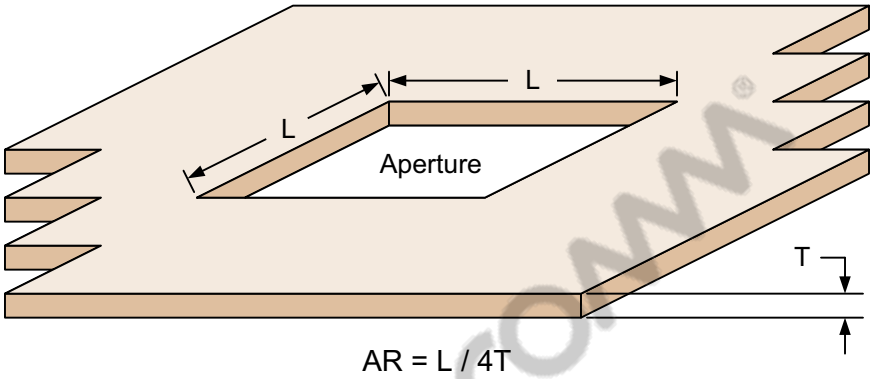


Figure 6-1 Stencil printing aperture AR

Guidelines for an acceptable relationship between L and T are listed below, and are shown in Figure 6-2:

- R = L/4T > 0.65: best
- 0.60 ≤ R ≤ 0.65: acceptable
- R < 0.60: not acceptable

Stencil Aperture L (µm)	Stencil thickness, T (µm)							
	75	80	85	90	95	100	105	110
210	0.70	0.66	0.62	0.58	0.55	0.53	0.50	0.48
220	0.73	0.69	0.65	0.61	0.58	0.55	0.52	0.50
230	0.77	0.72	0.68	0.64	0.61	0.58	0.55	0.52
240	0.80	0.75	0.71	0.67	0.63	0.60	0.57	0.55
250	0.83	0.78	0.74	0.69	0.66	0.63	0..60	0.57
260	0.87	0.81	0.76	0.72	0.68	0.65	0.62	0.59

Figure 6-2 Acceptable solder-paste geometries

QTI provides an example PCB land pattern and stencil design for the 163 FOWNSP package.

NOTE Click the link below to download the 163 FOWNSP land/stencil drawing (LS90-NG134-1) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/0901003981d11c45

After successfully logging on, the document is downloaded.

Make this document a favorite to be notified of any changes. Subscribe to the daisy-chain interconnect drawing to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.2.2 Reflow profile

Reflow profile conditions typically used by QTI for lead-free systems are listed in Table 6-1, and are shown in Figure 6-3.

Table 6-1 QTI typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temperature range	Condition
Preheat	Initial ramp	< 150°C	3°C/s maximum
Soak	Flux activation	150–190°C	60–75 s
Ramp	Transition to liquidus (solder-paste melting point)	190–220°C	< 30 s
Reflow	Time above liquidus	220–245°C [1]	50–70 s
Cool down	Cool rate: ramp-to-ambient	< 220°C	6°C/s maximum

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

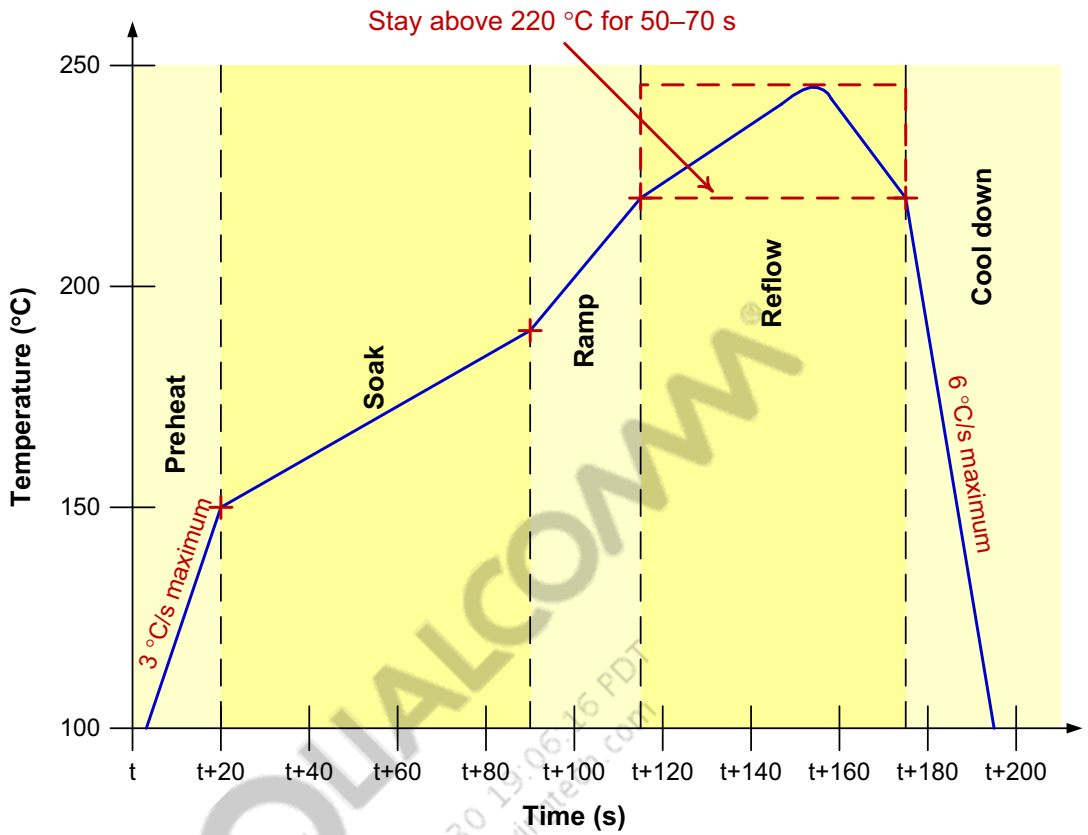


Figure 6-3 QTI typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document, and without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

1. Section 4.4: Device moisture-sensitivity level

   PM8953 device is classified as MSL1 at 250°C. The temperature (250°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained in #2 below.

2. Section 7.1: Reliability qualifications summary

   One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5°C (255–260°C).

3. Section 6.2.2: Reflow profile

   During a production board's reflow process, the temperature seen by the package must be controlled. The temperature must be high enough to melt the solder and provide reliable connections. However, it must not go so high that the device might be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (250°C or more).

6.2.4 SMT process verification

QTI recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow-profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. In fact, all SMT process recommendations discussed above can be performed using daisy-chain components.

Daisy-chain PCB routing recommendations are available for download.

NOTE Click the link below to download the 163 FOWNSP daisy-chain interconnect drawing (DS90-P1514-1) from the Qualcomm CreatePoint website.

After successfully logging on, the document is downloaded.

This link will be included in future revisions of this document.

NOTE Make this document a favorite to be notified of any changes. Subscribe to the daisy-chain interconnect drawing to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.4 Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

Board-level reliability data is available for download.

NOTE Click the link below to download the 187 FOWNSP board-level reliability data (BR80-TBD) from the Qualcomm CreatePoint website.

After successfully logging on, the document is downloaded.

This link will be included in future revisions of this document.

NOTE Make this document a favorite to be notified of any changes. Subscribe to the daisy-chain interconnect drawing to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

7 Part reliability

7.1 Reliability qualifications summary

This content will be available in a future revision of this document.

7.2 Qualification sample description

Device characteristics

Device name:	PM8953
Package type:	187 FOWNSP
Package body size:	5.78 mm × 5.78 mm × 0.65 mm
Lead count:	187
Lead composition:	SAC405
Fab process:	0.18 µm HV CMOS
Fab sites:	SMIC and MagnaChip
Assembly sites:	STATS ChipPAC, Singapore
	Nanium, Portugal
Solder ball pitch:	0.4 mm

8 Revision history

Revision	Date	Description
A	October 2015	Initial release
B	March 2016	■ Table 1-1, PM8953 features: Updated the value for SMPS ■ Table 2-7, Configurable input/output functions – GPIO and MPPs: □ Updated the value of Pad # and Configurable function for GPIO functions □ Deleted sleep clock details under GPIO functions ■ Added the following chapters: □ Chapter 3, Electrical specifications □ Chapter 5, Carrier, storage, and handling information □ Chapter 6, PCB mounting guidelines □ Chapter 7, Part reliability ■ Chapter 4, Mechanical information: Added the following sections: □ Section 4.2, Part marking □ Section 4.3, Device ordering information □ Section 4.4, Device moisture-sensitivity level □ Section 4.5, Thermal characteristics

For additional information or to submit technical questions go to https://createpoint.qti.qualcomm.com

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Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.