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Understanding Phase Noise in LC VCOs

A key problem in RF integrated circuits

The design of low-phase-noise inductor-capacitor voltage-controlled oscillators (LC VCOs) has been one of the most important topics in the field of radio frequency (RF) integrated circuits in last 20 years. A huge number of IEEE papers have been devoted to this subject, which is quite a unique circumstance for a circuit that typically embeds from three (sometimes two) to five transistors. The reasons for this widespread interest are well known, i.e., the phase noise of VCOs is one major obstacle encountered during the design of RF transceivers, and the power dissipated to meet the noise specs is often a nonnegligible portion of the total budget.

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A second reason is the intrinsic time-variant nature (often also nonlinear) of these circuits, which makes their analysis very difficult.

The efforts made in the last two decades have substantially deepened the understanding of the matter; yet the design and analysis of VCOs is an important research subject today. It is, therefore, important to point out what has been understood thus far. Of course, it is impossible to summarize 20 years of findings in a short article; therefore, only a selection of the main results is presented here. In particular, the discussion is focused on so-called white phase noise in differential current-biased metal–oxide–semiconductor (MOS) LC VCOs that, until today, have achieved the best phase noise versus power performance. Other important issues, such as the flicker noise impact and voltage-biased VCOs ring oscillators, are not discussed. Above all, the viewpoint of the designer

The increase of tank complexity to achieve a better phase noise has been very recently investigated in literature and could be a future research area.

is kept, and the physical understanding is privileged over the mathematical rigor.

LC Oscillator Basics

Essentially, the typical LC oscillator consists in the parallel between an inductor and a capacitor, the so-called LC tank, which ideally should oscillate at the tank resonant angular frequency, $\omega_0 = 1/\sqrt{LC}$, plus an active element, i.e., a transconductor, that balances the tank's unavoidable losses. These losses, for the frequencies in the typical 1–10-GHz range, are mainly due to the physical resistance of connections and via in series to the reactive elements and are quoted in terms of the quality factors of L and C (Figure 1).

To simplify the circuit's topology, an equivalent tank is derived, in which the losses are lumped in the parallel resistance R. It is easy to demonstrate that the equivalent circuit features with a good approximation the same L and C, while the value of R can be derived by equating the total quality factor of the real tank Q_T to the quality factor of the equivalent tank Q. The only unknown in the equation is R. The new circuit is equivalent to the real one for frequencies close to ω_0, hence being equivalent in term of losses, it is equivalent also in term of thermal noise. It is now straightforward to see that an ideal linear transconductor (with transconductance G_m) connected in positive feedback synthesizes a negative conductance $-G_m$ whose magnitude should be equal to $1/R$ to balance losses. The same result can be derived in a more rigorous way by evaluating the oscillator's loop gain. Starting from this simplified model, two questions arise. First, due to the process spreads, it is impossible to design a practical circuit having exactly $G_m = 1/R$. So how is it possible to ensure the oscillator's start-up? Second, the model does not say anything about the oscillation amplitude.

Both of these issues are resolved by considering a more realistic transconductor I-V characteristic, i.e., the saturating one in Figure 2. The slope at $V = 0$, i.e., the small signal G_m, is larger than $1/R$ so that the losses are overcompensated, and any disturbance or noise will start an oscillation with increasing amplitude (i.e., the circuit is unstable, featuring two complex poles in the right-hand complex plane). Of course, the oscillation amplitude cannot diverge and, when it increases beyond the linear input range of transconductor, its output current will be heavily distorted. The latter effect is the one that sets the oscillation amplitude. To grasp this point, let us simplify the analysis by considering a hard-limiter I-V characteristic saturating at $\pm I_s$. The small signal G_m is infinite and the start-up is ensured. We can now assume that the signal $V(t)$ across the tank is sinusoidal at ω_0 and we seek consistency. The output current is a square wave featuring odd harmonics injected in the tank. Only the fundamental at ω_0 with amplitude $(4/\pi)I_s$ survives, while the higher frequencies such as $3\omega_0$ and $5\omega_0$ are shunted to ground,

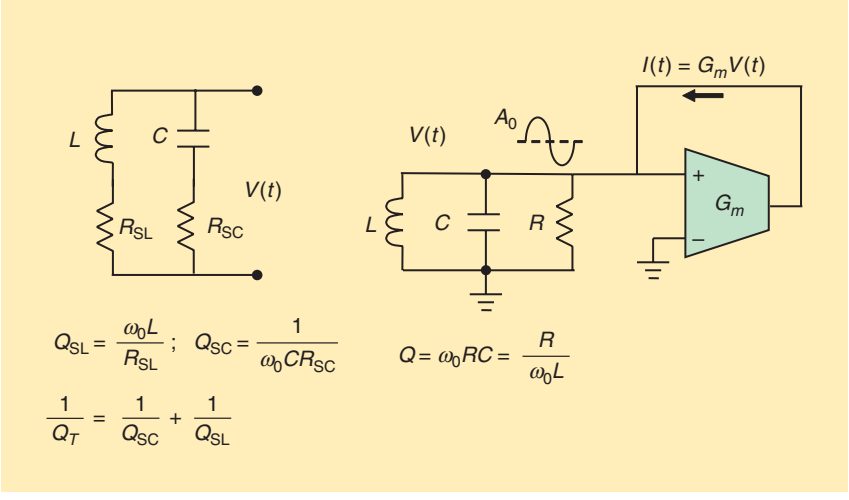


FIGURE 1: The real tank and its parallel equivalent with *Gm* balancing the losses.

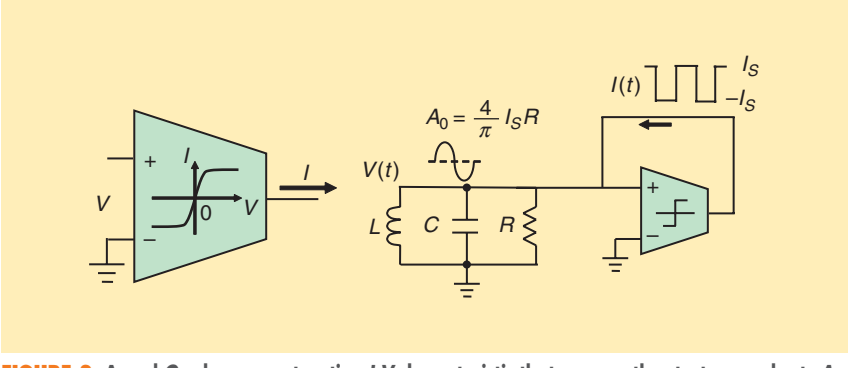


FIGURE 2: A real G_m shows a saturating *I-V* characteristic that ensures the start-up and sets A_0.

the resulting oscillation amplitude is $A_0 = (4/\pi) I_s R$. The tuning capability is typically achieved by using a variable capacitor (varactor) in the tank whose capacitance is controlled via a dc voltage V_{tune}.

Integrated oscillators are often implemented in a differential topology. Figure 3 shows how a standard spiral inductor can be symmetrically connected to the power supply, to the tunable varactor, and to a differential G_m. The availability of a thick upper metal layer in the inductor is a key factor for the design of an high-Q tank that, on the other hand, is fundamental to achieving a good power versus noise tradeoff, as discussed in the following. Figure 3 also shows a possible varactor structure, i.e., the small signal capacitance of an MOS transistor changes between depletion (low C) to inversion (high C) when the gate-source dc bias is varied. Other structures of varactors can be employed.

The simpler differential G_m is, of course, a source-coupled pair that can be connected in positive feedback in parallel to the tank, as in Figure 4. The dc bias of the two outputs is the supply voltage V_{DD}, while the start-up condition is $g_m/2 > 1/R$, where g_m is the transconductance of a single transistor. The oscillation amplitude increases until all of the tail current I_T is alternatively steered in the two transistors, so the current injected in the tank can thus be decomposed into a differential current i_{diff}(a $\pm I_T/2$ square wave) plus a common-mode dc term $I_T/2$. Being the differential zero-peak amplitude set by the first harmonic of i_{diff}, it is $A_0 = (2/\pi) I_T R$. Note that each differential output swings above the supply voltage by $A_0/2$ V.

In the following, it will be recalled that a large A_0 is beneficial for noise performance, which prompts a question about the maximum value of amplitude that can be achieved by increasing the dc current I_T. To simplify the discussion, it is typically assumed that, for negative polarity, the voltage can drop from V_{DD} to zero, neglecting the headroom necessary for the tail generator. Since the other output swings symmetrically, the ultimate amplitude limit should be $A_0 = 2V_{DD}$. Figure 4 also shows a schematic plot of the steady-state amplitude A_0 versus I_T. When the amplitude is proportional to I_T, the oscillator is said to operate in *current-limited regime*, and when A_0 is about $2V_{\text{DD}}$, the circuit enters in *voltage-limited regime*. As a rule of thumb, it is assumed that the optimum bias point is at the border of the two regimes where the maximum amplitude is reached, while a further increase of I_T would result only in higher power dissipation without any benefit.

The second benchmark circuit considered is the complementary MOS (CMOS) in Figure 5. The dc bias of the outputs in this case is below V_{DD}, while another difference is the start-up condition that now becomes $(g_{mN} + g_{mP})/2 > 1/R$. This higher efficiency in exploiting the current at the start-up is mirrored by a corresponding double efficiency with respect to the single-pair oscillator in Figure 4 when operating in the current limited regime. In the CMOS case, all of the current I_T flows differentially in the tank, thus resulting in $A_0 = (4/\pi) I_T$. However, the maximum value achievable by A_0 is halved with respect to the single-pair VCO. Assuming a dc bias at the output equal to $V_{\text{DD}}/2$ and neglecting the voltage drop across the tail generator, the maximum theoretical oscillation amplitude is $A = V_{\text{DD}}$.

Both of the VCOs discussed operate in class-B, and, in the two cases, the differential amplitude is quite large with respect to the input range of the differential pair, which is approximately

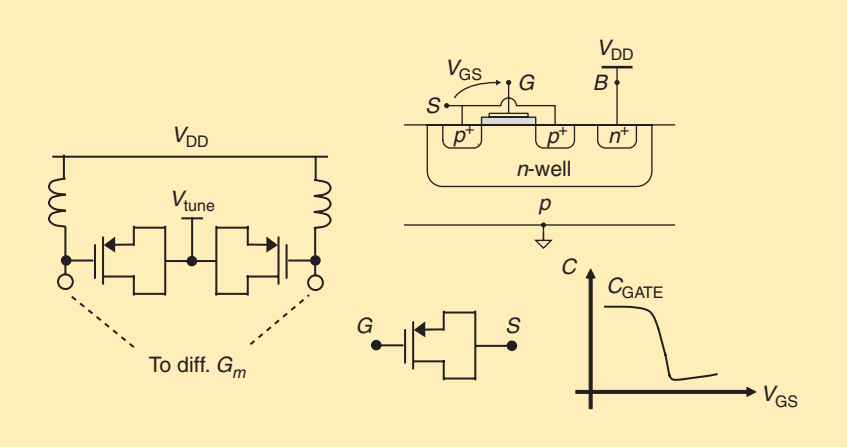


FIGURE 3: A differential tank topology and an example of a varactor (inversion-mode PMOS).

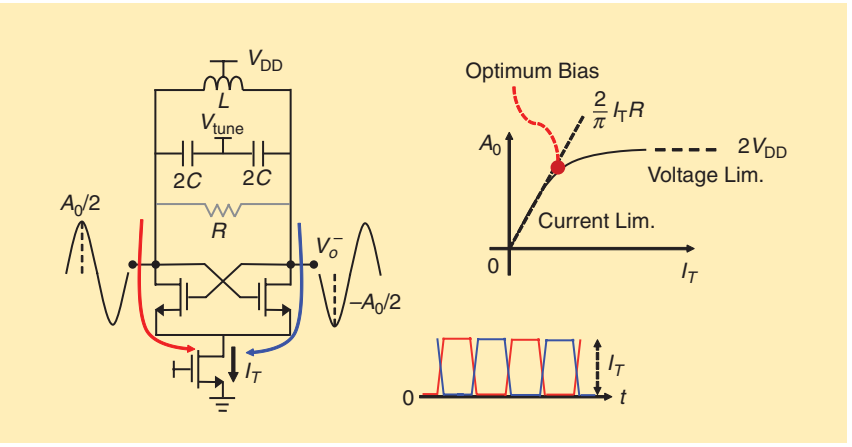


FIGURE 4: Steady-state currents in the single-pair VCO with the A_0 versus I_T characteristic.

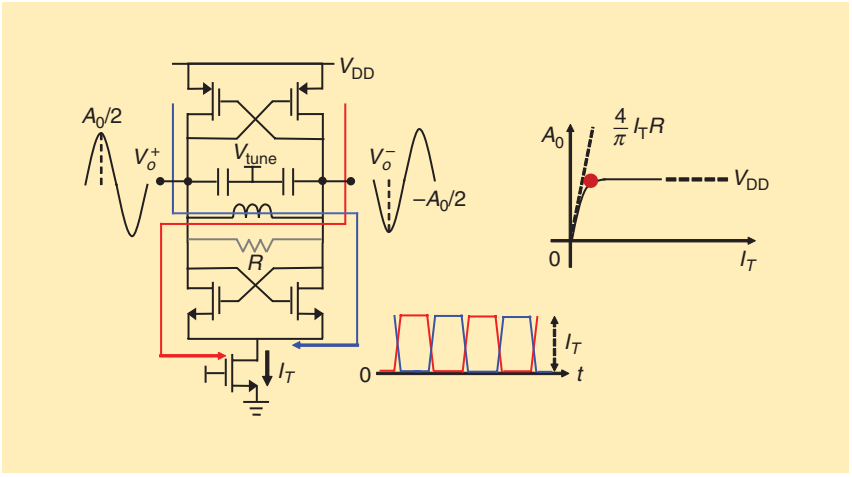


FIGURE 5: Steady-state currents in the CMOS VCO with the A_0 versus I_T characteristic.

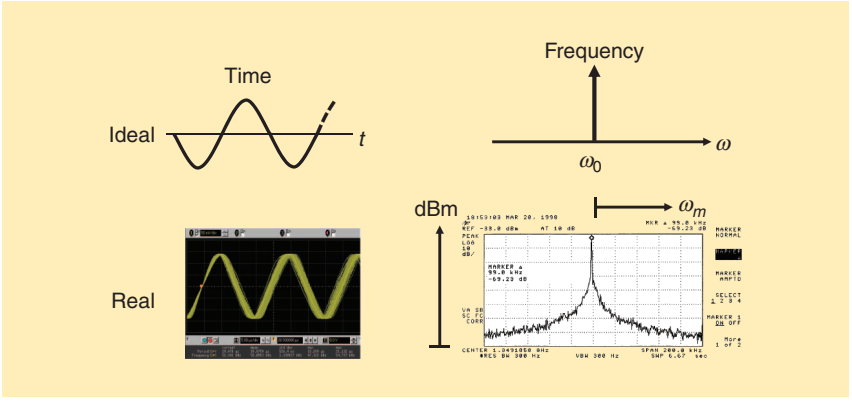


FIGURE 6: The impact of noise: ideal versus real VCO outputs in time and frequency.

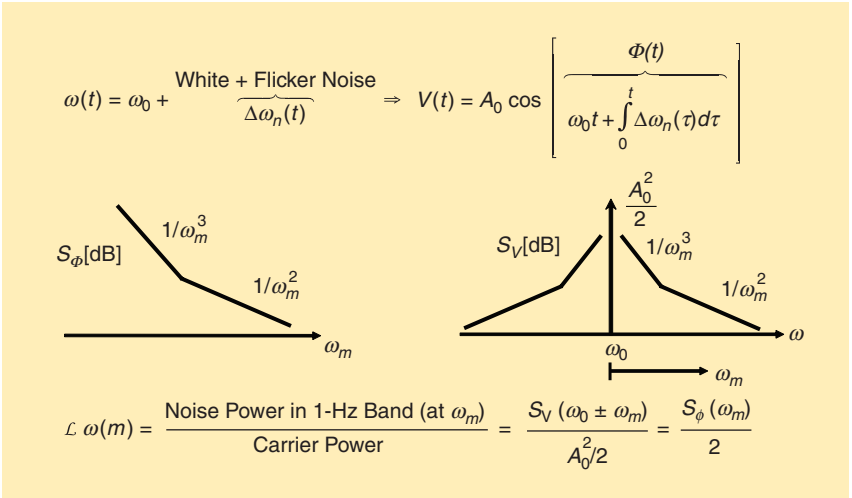


FIGURE 7: The link between frequency, phase, and voltage spectra. Usually, $\mathcal{L}$ is defined as phase noise.

twice the transistors' overdrive. This justifies why the hard-limiter model is a reasonable approximation. Comparing both circuits, the reliability issue should also be considered given the large value of A_0. Clearly, this problem is critical in the single-pair VCO, whose amplitude can be as large as $2V_{DD}$ and even larger in some advanced topologies (as discussed later). It is also important to highlight that, in both circuits, when the amplitude is close to the maximum value, the output waveforms are distorted since the transistors' nonlinearity are exploited.

Phase Noise

The main metric of an oscillator for RF applications is its phase noise. Figure 6 shows the ideal oscillator output both in the time and frequency domains versus what is observed in reality. In the time domain, the superposition of several waveforms starting synchronous shows an error at the zero crossing, which is called *time jitter*, equivalent to a phase error whose variance increases proportionally to the time. In the frequency domain, the spectrum shows symmetrical tails decreasing as $1/\omega_m^2$, where ω_m is the (angular) frequency offset from ω_0, which are referred to as the oscillator's phase noise. While jitter performance is fundamental in some fields (e.g., wireline circuits), usually phase noise specifications matter in RF applications, thus we will focus mainly on them. Of course, a link exists between phase noise and time jitter.

Both the accumulation of time jitter and the $1/\omega_m^2$ dependency suggest that a sort of integration of white noise is taking place in the circuit. Even if the mathematical description of the process is not straightforward, it is possible to say intuitively that any white noise in the circuit affects the period, and thus the frequency, of the oscillator. The link between the frequency and the phase is integration. Therefore, if we assume that a noisy term $\Delta\omega(t)$ is added to the resonant frequency ω_0, the excess phase $\Phi(t)$ is obtained through the integration, as in Figure 7. In the figure, it is assumed that $\Delta\omega(t)$ features both white and flicker (i.e., *1/f*) fluctuations, hence the phase power spectral density (PSD) $S_\Phi(\omega_m)$ shows a component $1/\omega_m^3$ called *close-in phase noise* or *flicker phase noise* and, for larger values of ω_m, a component $1/\omega_m^2$ sometimes referred to as *white* phase noise. The latter often

dominates above a few megahertz and is the only contribution considered in this tutorial. The corresponding voltage spectrum is usually derived by expanding the expression of $V(t)$ assuming that $\Phi(t) << 1$ rad. The resulting voltage spectrum S_V shows two symmetrical sidebands (with respect to the so-called carrier signal at ω_0) that are essentially the PSD $S_\Phi(\omega_m)$ up-converted at ω_0. The ratio between the noise PSD S_V evaluated at $\omega_0 \pm \omega_m$ and the carrier power is a function of ω_m, and it is represented as $\mathcal{L}(\omega_m)$ and defined as the phase noise at ω_m. Typically, it is measured as $10\log_{10}|\mathcal{L}|$ dBc/Hz (dBc = dB with respect to the carrier) and is, of course, 3 dB below $S_\Phi(\omega_m)$.

According to this simplified model, both $S_\Phi(\omega_m)$ and the voltage noise PSD diverge when ω_m approaches zero. This behavior should not represent a problem concerning $S_\Phi(\omega_m)$. As a matter of fact, it is a rigorous result that depicts the accumulation of phase error, as seen in Figure 6. On the other hand, the divergence of the voltage PSD is unphysical. The point is that the approximation $\Phi(t) << 1$ rad is no more valid when the phase error is too large, hence for the component close to the carrier, and the expansion of $V(t)$ in Figure 7 is not valid as well. [The same problem is encountered by comparing a narrowband FM with a wideband frequency modulation (FM).] When the problem is rigorously discussed, it results that, in case of white noise affecting the frequency, the voltage spectrum is Lorentzian: the spectrum flattens when it is very close to the carrier, while the $1/\omega_m^2$ behavior is a very good approximation at a large offset. The process is a phase diffusion one, as the Brownian motion.

Two papers that present this matter from an IC designer perspectives are [1] and [2]. This behavior, up to now, has no impact in RF applications for two reasons. First, only the noise at relatively large offset matters; let us say at least above 10 kHz but usually above a few megahertz. Second, the VCO is always embedded in a phase-locked loop that filters the oscillator noise close to the carrier (usually below 100 kHz and, in some cases, below 1 MHz). Therefore, the phase noise we are considering is the one that usually affects most of the performance of a transceiver. The main impact of the VCO phase noise is related to the reciprocal mixing effect that has been discussed in several papers; see, for instance, the article in a recent issue of *IEEE Solid-State Circuits Magazine* [3].

Integrated oscillators are often implemented in a differential topology.

The next step is the evaluation of phase noise starting from the circuit topology. In Figure 8, we are back to the very simplified oscillator topology. A current noise PSD S_{nI} is now added in parallel to the tank, consisting in the thermal noise ($4kT/R$) due to the tank losses (i.e., due to finite Q) plus another term ($4kT/R$)F, where F is an empirical parameter accounting for the noise of the active element.

We can imagine that, when the oscillator is running, a portion of this noise is injected in the ideal (i.e., lossless) tank, but how much is this fraction? This can be heuristically derived by assuming that S_{nI} consists only in a single noise tone added to the carrier. Figure 8 shows the phasors of both the carrier, with amplitude A_0, and the small noise tone at frequency $\omega_0 + \omega_m$, all of which are represented in the carrier frame. The single noise tone can be seen as the sum of two amplitude modulation (AM) and two phase modulation (PM) sidebands. (In both cases the sidebands are correlated.) In the case of white noise, half the power of it contributes to AM and half to PM. A hard limiter is sensitive only to PM; therefore, we can consider that, for half of the noise power, the losses are balanced by the hard limiter. Therefore, half of the white PSD is injected in the ideal tank whose impedance magnitude at $\omega_0 \pm \omega_m$ is approximately $1/2C\omega_m$. The corresponding phase noise is

$$\mathcal{L}(\omega_m) = \frac{1}{2}\cdot\frac{kT}{R}\cdot\frac{(1+F)}{C^2\omega_m^2 A_0^2/2} = \frac{1}{2}\cdot\frac{kT}{A_0^2/2R}\cdot\left(\frac{\omega_0}{\omega_m}\right)^2\cdot\frac{(1+F)}{Q^2} \quad (1)$$

(using $Q = \omega_0 RC$). This is the formula derived by Leeson [4] in his famous paper, though with a different procedure, accounting for the $1/\omega_m^2$ dependence.

What happened to the AM contribution? In this case, the hard limiter is unable to balance the losses, not being sensitive to AM, and the noise

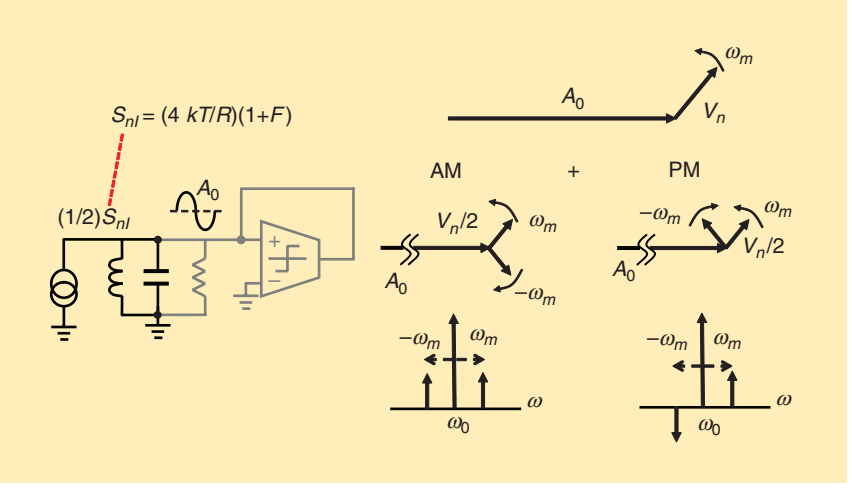


FIGURE 8: Only half of the total noise contributes to phase noise.

Both of the VCOs discussed operate in class-B, and, in the two cases, the differential amplitude is quite large with respect to the input range of the differential pair, which is approximately twice the transistors' overdrive.

is injected in the resistor-inductor-capacitor tank, so it is much less amplified. The AM noise is therefore negligible; however, it can be converted again into phase noise by the VCO nonlinearities. Its evaluation is therefore also important.

LTV Evaluation of Phase Noise

From the previous section, it may seem that everything has been understood, at least from 1966 when [4] was published. One may therefore wonder why in last 20 years so many papers were devoted to the calculation of phase noise. The problem is the rigorous evaluation of F that, by definition, is the ratio between the phase noise contribution coming from the transconductor and half of the thermal noise of the tank.

Other than in both of the circuits in Figures 4 and 5, only two different kinds of noise sources are present, i.e., the channel thermal noise from one of the transistors in the pairs (all else contributing in the same way) and the noise from the tail. The switching behavior of the circuit is such that a standard noise-transfer technique can not be employed. It is true that, today, powerful simulation tools for phase noise are available, but it is still fundamental for the designer to have an understanding of the noise behavior, the design tradeoffs and the fundamental ultimate limits. That's why the techniques described in this section were developed.

Typically, the oscillator is still considered a linear but also a time-variant (LTV) element. It is well known that in these systems, e.g., mixers and samplers, a signal can be moved from one frequency to another (e.g., the aliasing or folding effect). We will briefly discuss two different procedures, equivalent at the first order, that consider the LTV circuit behavior, the first of which focuses more in the frequency domain and the second more in the time domain.

LTV Approach in Frequency Domain

The LTV approach was proposed in [5] and then further developed in a general way in [6]. The idea is that, in the VCO, any noise source is transferred to the tank after the multiplication by a windowing function $H(t)$ that is periodical, since the switching is dominated by the carrier. This multiplication in the frequency domain will fold out-of-band noise components close to ω_0.

Consider, for instance, the channel thermal noise $4kT\gamma g_m$ of a single MOS. In Figure 9, it is sketched as a generic signal generator i_n placed between the same two nodes. The question is: what is the equivalent phase noise injected in the ideal tank? From Figure 9, we see that the signal i_n is injected only at the zero crossings for a short time window whose duration is T_w. The period of the function $H(t)$ is therefore $T_0/2$ (being $T_0 = 2\pi/\omega_0$ the carrier period), and its amplitude is one half since the transistor is degenerated by $1/g_m$

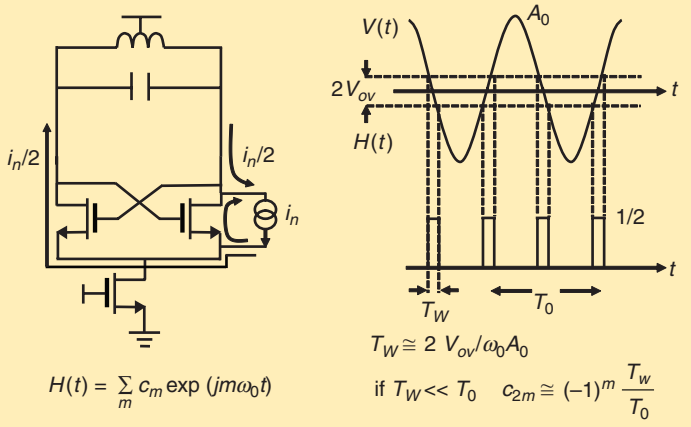


FIGURE 9: A time-variant injection of MOS thermal noise.

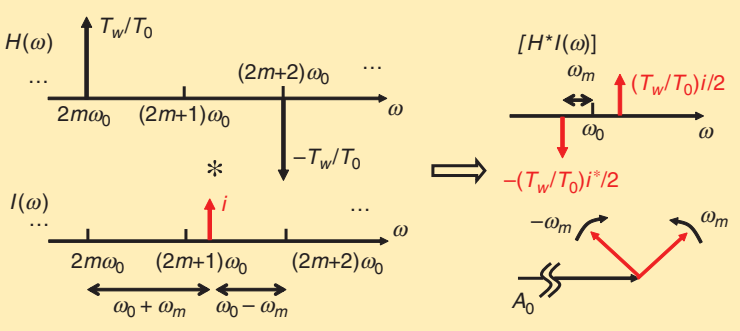


FIGURE 10: The folding of a noise tone produces a phase modulation signal (see Figure 8).

at the zero crossing. The time T_w is approximated as the ratio between two times the MOS overdrive and the carrier slope at the zero crossing.

Multiplication in time is convolution in frequency, the spectrum of $H(t)$ features harmonics at $2\omega_0$, $4\omega_0, \ldots, 2m\omega_0$ etc. Given that it is $T_w << T_0$, the main harmonics of $H(t)$ have approximately the same amplitude and alternate signs. If the signal consists in a single noise tones at $[2(m+1)\omega_0 + \omega_m]$, from Figure 10, it results that this tone is folded as two sidebands at $\omega_0 \pm \omega_m$. Given the signs of the folding coefficients, the resulting modulation is a pure PM at the rate ω_m. This is not a surprise since the noise is, in practice, injected at the zero crossing and only the phase is affected. If i_n features a white spectrum, the folding of all of the noise power components must be taken into account. F is evaluated as the ratio between the resulting noise and the PM component of the tank noise (see Figure 11). After a multiplication by two (two transistors in the pair), it is not difficult to derive that $F = \gamma$. Despite all the coarse approximations, this result is correct and can be obtained with a rigorous derivation [6].

As a second example, the noise from the tail can be evaluated by noting that it is transferred to the tank by a $H(t)$ that, in this case, is a square wave at ω_0 with an amplitude 1/2, just as in a single-balanced mixer. A noise tone at $[2m\omega_0 + \omega_m]$ is now folded close to the carrier, but, since the coefficients of the square wave don't have the same amplitudes, it will contribute both to AM and to PM. When a white noise is considered, the result is the phase noise injected in the ideal tank is 1/8 of the tail current noise PSD. This coefficient can be justified by noting that half of a tail signal is differentially injected in the tank, i.e., 1/4 in power, the other factor 1/2 comes from considering only the phase modulation component. The factor F is evaluated accordingly.

The main metric of an oscillator for RF applications is its phase noise.

LTV Approach in Time Domain: The Impulse Sensitivity Function

This is the very famous technique presented by Hajimiri and Lee in what is one of the most-cited papers in *IEEE Journal of Solid-State Circuits* [7]. Given its impact in this field, it is virtually impossible to write a paper about VCO phase noise without referring to it. The LTV system in this case is characterized through an impulse response that links a current impulse injected in a given node of the circuit and the resulting phase shift of the oscillating output. This response is considered a unit step function multiplied by the amplitude of the phase shift $\Delta\Phi$, and this amplitude would unavoidably depend on the injection time of the impulse itself. For instance, in Figure 12, when the impulse is injected at the peak of the oscillation, the phase shift is zero. On the other hand, when the signal is injected at the zero crossing, the phase error $\Delta\Phi$ is a maximum and, of course, it will be in between these extremes if the impulse is injected at a different point of the waveform.

This behavior is expressed by a dimensionless impulse sensitivity function (ISF), represented with the symbol Γ, that depends on the noise source considered. In a linear system, $\Delta\Phi$ is proportional to the impulse area (a charge Δq), given that the phase is also dimensionless, the ISF must be normalized to q_{max}, the maximum charge at the injection node. The phase shift due to a generic current signal i_n is evaluated by a superposition integral as in Figure 13. Clearly, Γ is periodic and can be expanded in Fourier series, as in Figure 13. For a white current noise, the derivation of phase spectrum $S_\Phi(\omega_m)$ is not difficult. Once Γ is known $S_\Phi(\omega_m)$ results related to the root mean square (rms) power of Γ (Γ^2_{rms} the sum of the Γ's squared

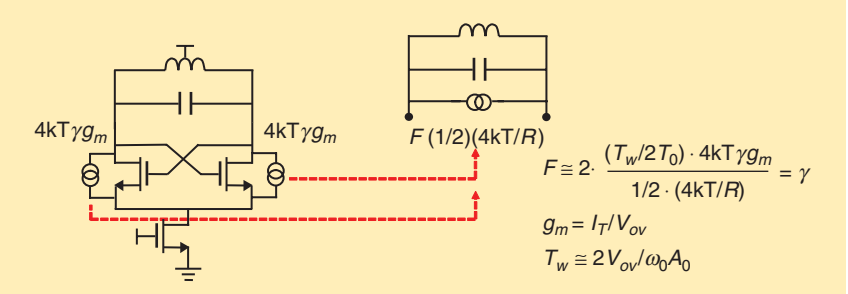


FIGURE 11: The noise contribution from the differential pair.

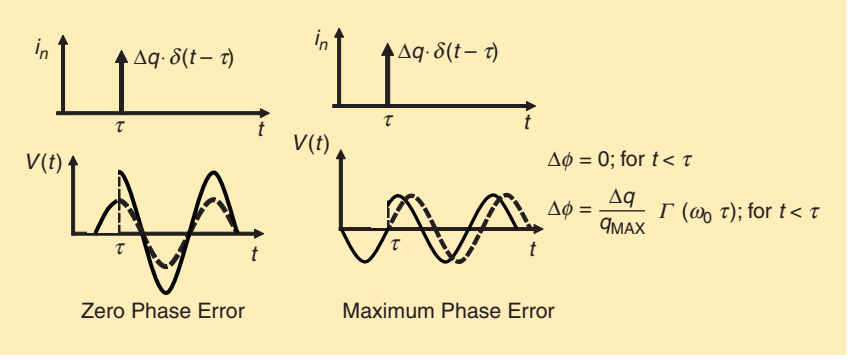


FIGURE 12: The impulse sensitivity function (ISF).

A second important tradeoff in VCOs is the one between phase noise and the tuning range, which is the ratio between the frequency range covered by the VCO and the average value of this range.

Fourier coefficients). It is interesting to note that the technique inherently implies (see Figure 13) 1) the folding of out-of-band noise, since a noise components at $n\omega_0+\omega_m$ will be folded at ω_m by multiplication with the Γ coefficients at $n\omega_0$; and 2) an integration effect (also evident from the impulse-to-step function link) that, in the case of white noise, produces a $1/\omega_m^2$ shaped $S_\Phi(\omega_m)$. From the latter spectrum, the phase noise $\mathcal{L}(\omega_m)$ will immediately follow.

The evaluation of the Γ for each noise source is not straightforward; a rigorous derivation for the two VCO topologies discussed here was provided in [8] and [9]. For instance, consider again the impact of the channel thermal noise. As a first approximation, we can imagine that the noise is injected only at the zero crossing for the same T_w used in Figure 9 (see Figure 14). Under this assumption, the evaluation of Γ_{rms}^2, thus of F, is easy. For the differential pair, it is again

$$\Gamma(t)=\frac{a_0}{2}+\sum_{n=1}^{\infty}a_n\cos(n\omega_0 t+\theta_n)$$

$$\Delta\phi(t)=\frac{1}{q_{\text{MAX}}}\int_{-\infty}^{t}\Gamma(\omega_0\tau)\cdot\overbrace{i_n(\tau)d\tau}^{\Delta q}$$

$$S_\Phi(\omega_m)=\frac{S_{nI0}}{4q_{\text{MAX}}^2}\cdot\frac{\sum a_n^2}{\omega_m^2}=\frac{S_{nI0}}{2q_{\text{MAX}}^2}\cdot\frac{\Gamma_{\text{rms}}^2}{\omega_m^2}$$

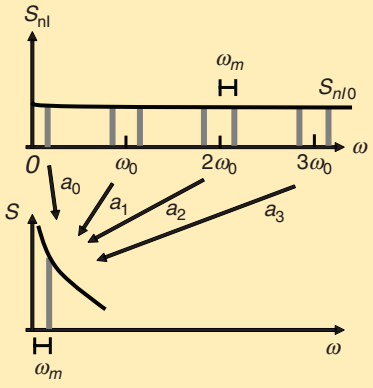
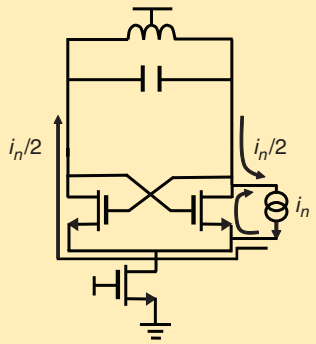
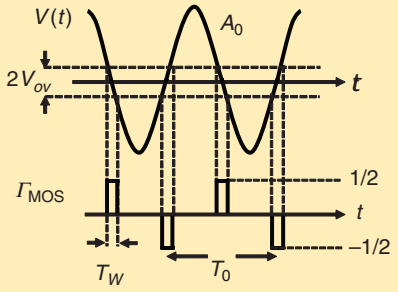


FIGURE 13: The folding and integration of a generic white noise obtained from the ISF.





$$F=2\cdot\frac{\Gamma_{\text{rms, MOS}}^2}{1/2}\cdot\frac{S_{nI,\text{ MOS}}}{4\text{kT}/R}\cong 2\cdot\frac{(T_W/2T_0)}{1/2}\cdot\frac{4\text{kT}\gamma g_m}{4\text{kT}/R}=\gamma$$

FIGURE 14: The contribution of MOS thermal noise to *F*, evaluated by the ISF.

$F=\gamma$, which is the value obtained by a rigorous analysis [8], [9]. Of course, the same technique can be applied to all the other noise sources of the VCO, e.g., the noise from the tail.

Minimum F

We will see that the noise contribution from the tail can be, at least in principle, eliminated. Instead, it seems that it is not possible to reduce F below γ. One may wonder whether the CMOS oscillator performs intrinsically better. From the analysis in [9], it seems that the answer is no. The minimum F is the average between γ_{PMOS} and γ_{NMOS} (i.e., $F=\gamma$, assuming $\gamma_{\text{PMOS}}=\gamma_{\text{NMOS}}=\gamma$).

This can also be intuitively recalled using the simplified model in Figure 14, comparing the two VCOs featuring the same tank, at the optimum bias point. Also assume that the nMOS transistors' (W/L)s are the same (the pMOS is scaled proportionally to the ratio between mobilities). If the single pair drains a current I_T, the CMOS VCO dissipates $I_T/4$ (half amplitude and doubled current efficiency), thus it features half overdrive and half g_m with respect to its nMOS-only counterpart. It also follows that the injection time T_w will be the same (in the CMOS, both the amplitude and the overdrive are halved with respect to the single pair VCO). Therefore, in this example, the noise power injected by a single transistor is halved in the CMOS VCO, but the number of noise sources is doubled.

As a matter of fact, an important general result has been demonstrated in [6] and [10], i.e., that under some conditions commonly achieved (e.g., the active element does not add losses to the tank, the transistors noise is proportional to g_m, etc.), for this topology of oscillators the minimum value for F is γ. This result is valid not only for MOS. For instance, the equivalent γ in bipolar transistors is 1/2, assuming the only noise source is the collector shot noise of the device, $2qI_c$. What is interesting to note is that, at the first order, the noise added by the active element does not depend on transistors' size

and bias, and it is γ times the one due to tank's resistive losses.

A way to reduce F below γ [10] is to embed an ideal noiseless voltage gain K (i.e., an ideal transformer) between the tank and the transconductor's input. This should reduce F by the gain K. The reason is that the signal at the transconductor's input is amplified by K, thus the noise injection window T_w is proportionally reduced (see Figure 14). The practical implementation of this solution is not easy and, despite some attempts, up to now, the results obtained are still not better than the ones achieved in standard VCOs.

Practical Tradeoffs in VCOs

Phase Noise Versus Power

From (1), it emerges that the phase noise reduces when A_0 increases (i.e., 6 dB of phase noise reduction every octave of A_0). When the oscillator is optimally biased at the border between the current- and voltage-limited regimes, A_0 is both proportional to V_{DD} and the tail current I_T. A tradeoff therefore exists between the dc power ($P_{DC} = V_{DD} I_T$) dissipated by the VCO and the white $1/\omega_m^2$ phase noise performance, as in most analog circuits, for instance, in small-signal amplifiers. But, how do we exploit this tradeoff if A_0 is already the maximum allowed by the VCO topology? To find out how, suppose the redesign of a VCO that is already optimally biased in the same technology and at the same frequency but with the target of improving the phase noise performance by 3 dB. Assuming a constant quality factor for the tank, if C is doubled and consequently L is halved to keep ω_0 constant, from the expression of Q, the resistance R also halves. In both of the topologies considered, to keep A_0 constant at the maximum value, I_T must be doubled. In this way, the dc power is doubled and the phase noise is reduced by 3 dB [see (1)].

It is therefore possible to achieve the phase noise performance desired if enough power is burned, of course within practical limits (e.g., the size of the capacitance cannot increase too much, etc.). This important property is captured by a figure of merit (FoM) (expressed in decibels) proposed in [11] that is the product between P_{DC} (measured in milliwatts) and the phase noise $\mathcal{L}(\omega_m)$ normalized by the factor $(\omega_m/\omega_0)^2$. The latter factor removes the dependences of the FoM on offset and oscillation frequencies. This FoM can also be easily written in a meaningful form by noting that the term $A_0^2/2R$ in (1) is the RF power dissipated in the tank and by expressing it as ηP_{DC}, where η is the power efficiency of the oscillator [12]:

$$\begin{aligned} FoM &= -10\log_{10}\left[\mathcal{L}P_{DC}\left(\frac{\omega_m}{\omega_0}\right)^2\right] \\ &= -10\log_{10}\frac{kT}{2} + 10\log_{10}Q^2 \\ &\quad - 10\log_{10}\frac{1+F}{\eta}. \end{aligned} \tag{2}$$

The term $kT/2$ at room temperature gives about 176.8 dB (since the dc power is measured in milliwatts). From the above expression, we see that what really matters is the Q factor of the technology. For instance, as anticipated, the availability of a thick metal layer for the inductor is an important factor. The last term represents a degradation of the performance due to the presence of the active element. The designer's job is to keep F close to the theoretical minimum and try to achieve the higher η. To this extent, η can be written as the product of current efficiency η_I, the ratio between the rms RF current flowing in the tank and tail current, and voltage efficiency η_V, the rms value of A_0 divided by V_{DD}. The two class-B oscillators in Figures 4 and 5 feature the same theoretical maximum η ($\eta = 2/\pi$). The single-pair oscillator, in fact, has double η_V (A_0 can theoretically reach $2V_{DD}$) with respect to the CMOS topology that, however, is two times more efficient in terms of current.

It is therefore possible to achieve the phase noise performance desired if enough power is burned, of course within practical limits.

Considering $F = \gamma = 1$ (a typical value) and $\eta = 2/\pi$, the last term $(1+F)/\eta$ is about 5 dB. In real circuits, unfortunately, it is very difficult to reach such a limit for several reasons. For instance, even when only a single MOS in the pair is on, it is not completely degenerated, as assumed in Figure 9. Because of the tail parasitic capacitance, the thermal noise finds a path to the tank, thus increasing F. Also, the maximum amplitude cannot be reached, since some voltage drop across the generator is needed, a condition that reduces η, and the tail noise is also present.

To provide some typical figures, consider a single-pair VCO, with $L = 1\,\text{nH}$, $C = 4\,\text{pF}$ ($\omega_0/2\pi$ about 2.5 GHz), $Q = 15$, and supply $V_{DD} = 1.2\,V$. The equivalent loss resistance is $R = 239\,\Omega$, thus, to get $A_0 = 2\,\text{V}$, the tail current must be 13 mA, resulting in a dissipation $P_{DC} = 15.6\,\text{mW}$. Given the available Q, the FoM in the ideal case ($\gamma = 1, \eta = 2/\pi$) should be 195.4 dB. Assume instead that a value of 185 dB is achieved because of the circuit nonidealities; it is possible now to evaluate the white phase noise from (2). For instance, at 3 MHz from the carrier, it is $\mathcal{L}$ =-138.5 dBc/Hz. If the same tank (i.e., the same L and C) is embedded in a CMOS VCO, the maximum amplitude is halved (6 dB higher phase noise), but I_T is divided by four keeping the same FoM [13].

Phase Noise Versus Tuning Range

A second important tradeoff in VCOs is the one between phase noise and the tuning range, which is the ratio between the frequency range covered by the VCO and the average value of this range. In several applications, the required tuning range can easily exceed 20%. A large tuning range has an indirect, detrimental impact on

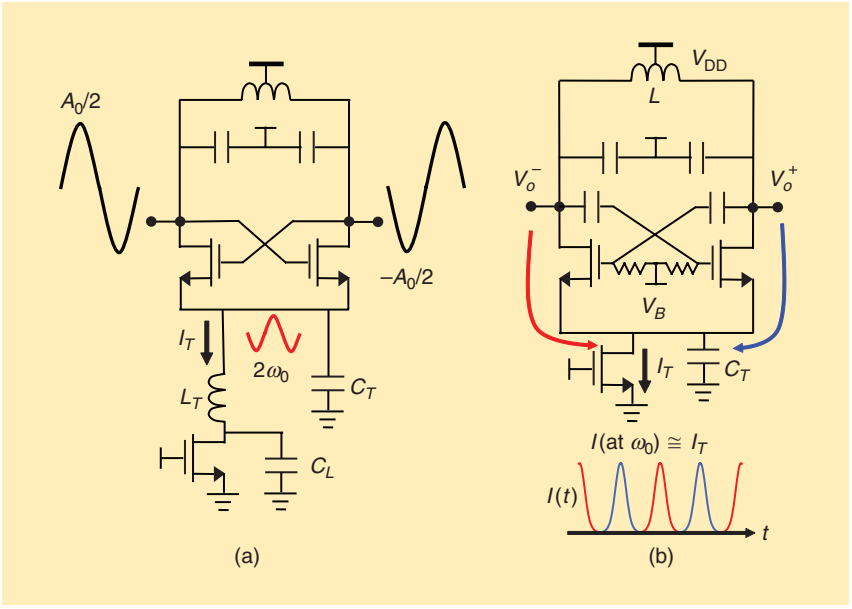


FIGURE 15: (a) A tail filter resonator and (b) a class-C VCO.

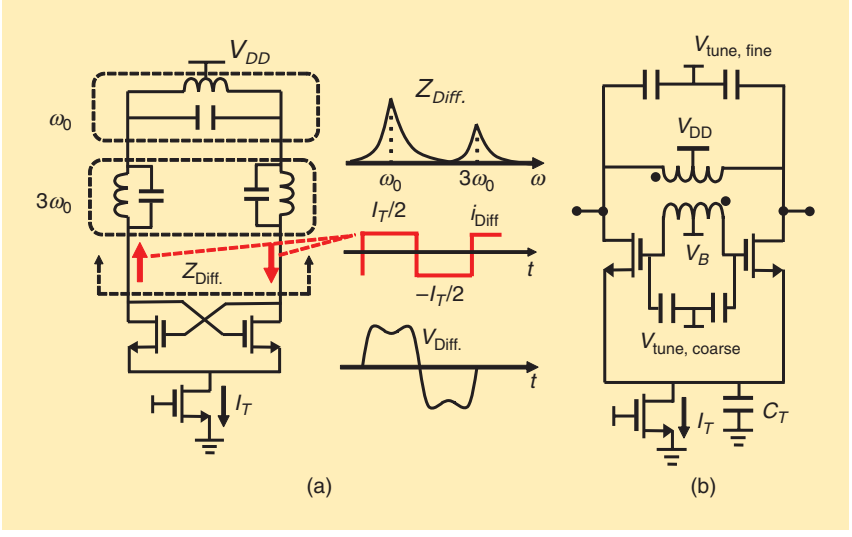


FIGURE 16: (a) An ideal class-F VCO and (b) a transformer coupled VCO.

phase noise. One reason is that, in a varactor, a large capacitance variation is often traded with the quality factor and thus with phase noise. In addition, let us consider an example in which a large frequency range has to be covered, for instance 1 GHz across an average frequency of 5 GHz (i.e., 20%). Since today's supply is limited, e.g., $V_{DD} = 1.2$ V, and assuming that V_{tune} swings in a fraction of the range 0-V_{DD}, the average slope of the frequency versus V_{tune} characteristic (indicated as *varactor gain* or K_{VCO}) cannot be much less than 1 GHz/V. This makes the VCO very sensitive to any noise on the tuning node. A white noise will be converted (proportionally to K_{VCO}^2) into white frequency noise and, therefore, into $1/\omega_m^2$ phase noise (see Figure 7). Typically, to limit this mechanism, a K_{VCO} below 10 MHz/V is desirable. A standard solution, called *switched tuning*, is to add in parallel to a varactor a bank of switchable standard capacitors to cover a large frequency with several overlapped characteristics featuring a low K_{VCO}.

This concept has been pushed to the ultimate limit by adopting only switchable capacitors to tune the frequency, thus realizing a digitally controlled oscillator. In this case, a continuous frequency range is covered by interpolating with a $\Delta\Sigma$ modulator the digital word controlling the bank. Whenever the tuning technique is adopted, a tradeoff tuning range versus phase noise does exist, and in some cases an additional factor is included in the FoM to account for it. At any rate, even if this tradeoff is not as manifested as the phase noise versus power one, the tuning range should always be provided (in addition to the FoM) to significantly gauge a VCO implementation.

Some Advanced VCOs Topologies

The factorization of η as the product of η_V and η_I is also instrumental to classify some advanced VCO topologies. Figure 15(a) shows an important example of the use of the so-called tail resonator (or tail filter) [14]. The key observation is that in a differential pair forced by a large differential input the common sources node runs at $2\omega_0$. In this circuit, C_L is a short at $2\omega_0$ while L_T and C_T are tuned at $2\omega_0$, therefore the common source node is AC-floating (open), and the oscillation amplitude can increase above $2V_{DD}$, thus improving η_V. Moreover, C_L shunts the tail noise to ground, as anticipated the tail noise impact can be eliminated, and the transcoductor does not load the tank. An FoM of above 195 dB was shown with $Q = 14$. Of course, an additional inductor is needed and the reliability issue is exacerbated. The same approach can be applied to the CMOS oscillator, thus relaxing the reliability problem [15], while a common-mode resonance at $2\omega_0$ has been obtained by modifying the VCO topology in [16] and [17] without adding any area penalty.

Since η_V is increased in the previous VCO, one may wonder if a dual approach, i.e., achieving a larger η_I, is possible. The answer is

the circuit in Figure 15(b) [10] that operates in class-C thanks to both the large capacitance C_T and the dc bias level of the gates. The differential pair's transistors are both off when the outputs are balanced, and the tail current is periodically shunted by C_T then delivered in spikes to the tank. Equivalently to what happens in the class-C amplifier, the first harmonic of the current is larger with respect to its class-B counterparts biased at the same I_T (a theoretical improvement of about 4 dB can be evaluated). Despite the fact that the implementation is not easy (i.e., the start-up needs additional circuits, the transconductor loads the tank, and the bias can be noisy), an FoM of 196 was still achieved.

Finally, it is interesting to point out how the research in this field is still active with the examples in Figure 16. The first circuit is a so-called class–F oscillator in which the additional series resonator at $3\omega_0$ makes the oscillation signal closer to a squared waveform, since the third harmonic of the current is not shunted. It has been theoretically demonstrated that, if the Q of the resonator at $3\omega_0$ was larger than the Q of the main tank, the entire tank noise would be reduced with respect to the standard case [12]. This condition has not been achieved in practice up to now, and the oscillator in Figure 16(a) was not implemented in [12]. It was also shown that it is not possible to achieve this condition by using a transformer's coupling [18]. A circuit as in Figure 16(b) [19] in any case can achieve a good FoM; one possible reason is the leveraging of the voltage amplification described in the previous section, but the discussion can be considered still open. The increase of tank complexity to achieve a better phase noise has been very recently investigated in literature and could be a future research area.

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