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ESD protection solutions for high voltage technologies

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Abstract

There is a trend to revive mature technologies while including high voltage options. ESD protection in those technologies is challenging due to narrow ESD design windows, NMOS degradation problems and the creation of unexpectedly weak parasitic devices. Different case studies are presented for ESD protection based on latch-up immune SCR devices.

1. Introduction

Many companies extend mature, less expensive CMOS technologies (0.35 μm and above) with new options and features such as high voltage (HV) or bipolar modules for specific automotive or consumer electronics applications. The strategy of technology upgrading offers significant economical advantages in this competitive market segment. For HV technology upgrades, HV MOS transistors are equipped with thick gate oxides and lowly doped drain/source implants to increase the voltage tolerance of the devices. This allows driving the maximum operating voltage to the limit of the process technology. ESD protection elements used in the HV domains need to be able to withstand these high voltages. However, the lowly doped implant envelopes applied for HV compatibility dramatically degrade the high current behavior of conventional protection elements, such as ggNMOS transistors. In addition, other issues as for example weak parasitic current paths and high latch-up susceptibility are commonly observed.

First, the paper reviews key issues commonly encountered for standard HV ESD transistors. The focus of the paper is on alternative solutions based on latch-up immune silicon controlled rectifiers (SCR). HV-compatible SCR power protection devices were already described in [1] and will therefore be briefly reviewed only. The ESD-on-SCR represents an efficient high voltage IO protection device for the ESD sensitive output drivers. A novel trigger concept preconditions the SCR for turn-on during ESD but avoids unintended triggering during normal circuit operation conditions.

2. ESD related issues in HV technologies

In mature low voltage technologies of 0.35 μm and earlier, the ggNMOS is still widely applied as the 'workhorse' for ESD protection design. This is possible due to

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straightforward implementation and sufficient high current capabilities in the parasitic NPN snapback mode. A normalized ESD performance per gate width of 10–15 mA/μm is typically found. Moreover, the clamping behavior indicated by the trigger and holding voltages as well as the dynamic on-resistance is sufficient to protect the relatively thick gate oxides (~15 nm) exposed to ESD stress in these LV technologies. The snapback holding voltage needs to exceed the maximum supply voltage specification not imposing any potential latch-up risk for power protection application.

The above described NMOS qualities are eliminated by introducing the upgrades required for MOS HV compatibility. The following sub-sections summarize the related problems commonly observed in high voltage technologies, e.g. in HV-CMOS.

2.1. Strong snapback

In high voltage technologies additional low doped implants are used as an envelope around the MOS drain and source diffusions, cf. Fig. 1, of the low-voltage MOS transistors to obtain the high junction breakdown voltage. These low doping concentrations strongly impact the snapback behavior. In some technologies, there is an additional FOX overlap region to increase the breakdown voltage between gate and drain/source junctions.

As shown in Fig. 2, the snapback trigger voltage V_{t1} of a ggNMOS (43 V 0.5 μm CMOS technology) is increased to 73 V, due to the high avalanche breakdown voltage of the drain-bulk junction. On the other hand, the snapback holding voltage V_{hold} still occurs at a relatively low value of 10 V. This value is comparable to the corresponding low-voltage NMOS elements.

Responsible for this behavior is the so-called Kirk or base-push-out effect appearing in the high-current bipolar mode [2,3]. This mechanism pushes the avalanche region from an initial location at the lowly doped drain curvature at breakdown (see spots at NN, ND in Fig. 1) to the highly doped N+ diffusion in a fully conducting bipolar mode. Hence, this shift to a high doping results eventually in a large intrinsic avalanche field that sustains parasitic NPN operation at a relatively low external (holding) voltage. When the gradual hot-spot migration to the N+ region occurs at elevated bipolar currents, the hot-spot transition is sometimes accompanied by a double-snapback effect: an initial higher holding voltage with a subsequent second snapback can be distinguished [4]. The low holding voltage limits the use of the ggNMOS for ESD protection.

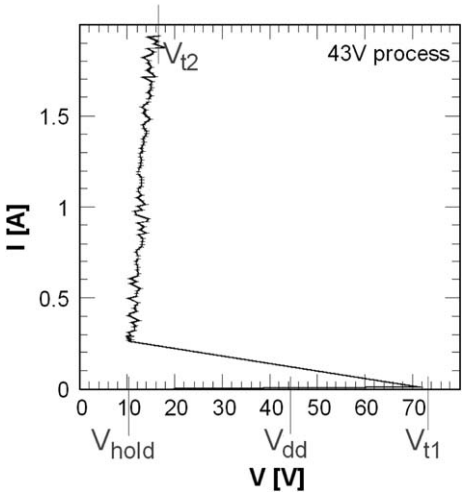

Fig. 2. Typical snapback TLP-*IV* curve of a HV-ggNMOS in a 43 V, 0.5 μm-CMOS technology. Characteristic is the strong snapback due to high triggering voltage and relatively low holding voltage.

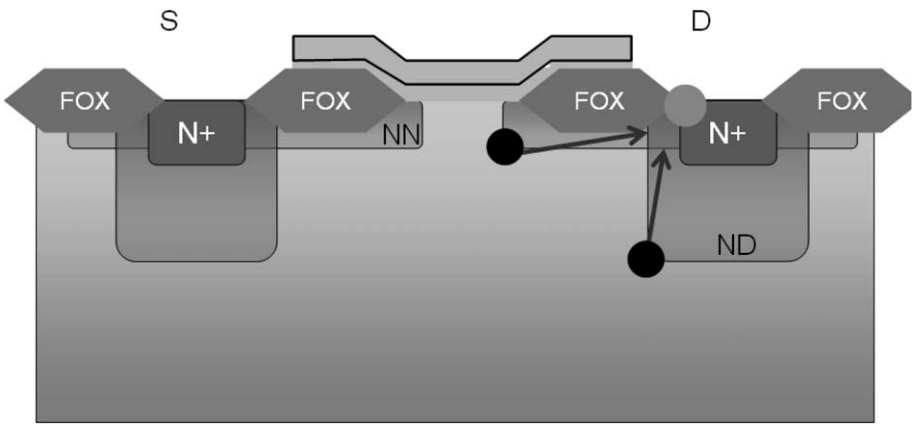

Fig. 1. Schematic cross-section of a typical high-voltage NMOS transistor equipped with lowly doped diffusions (NN, ND) enveloping N+ source and drain for high voltage compatibility. Hot-spot migration towards the FOX bird's beak caused by the Kirk-effect in high current bipolar operation is indicated.

2.2. Multi-finger non-uniformity issue

HV NMOS multi-finger triggering is difficult to accomplish due to the fact that the uniformity condition $V_{t1} < V_{t2}$ (trigger voltage smaller than failure voltage) is not met [5]. Simple ballast resistance integration into each finger does not solve the problem because of the huge voltage gap to be bridged. The ESD performance data of various HV-ggNMOS single- and multi-finger structures in Fig. 3 clearly demonstrates a poor scaling behavior. The performance scaling issue within a single finger is also caused by the strong snapback behavior in conjunction with a reliability issue discussed below.

In general, static gate/bulk biasing schemes for V_{t1} reduction cannot be successfully applied either since the maximum supply voltage is too high as compared to the holding voltage. A static V_{t1} reduction to the minimum allowed operating voltage would not significantly improve the multi-finger trigger behavior. Transient biasing schemes added at the HV NMOS output drivers (for example capacitive gate-coupling circuits) would interfere with normal circuit operation performance.

2.3. Intrinsic HV NMOS reliability issue

In particular for mature technologies with FOX-bound active areas, an intrinsic device reliability weakness occurs. During high-current bipolar operation, the impact ionization hot-spot is located at the N+ diffusion (high injection mode) closely to the FOX bird's beak as explained above, cf. Fig. 1. As a result, hot carriers can be injected into the SiO_2 material and are trapped there easily ('charge trapping'). The bird's beak is a region

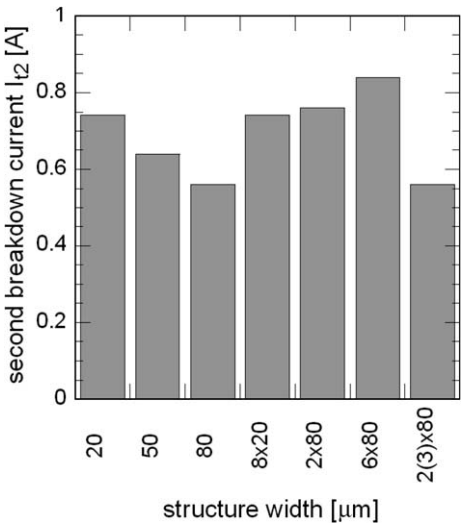

Fig. 3. TLP I_{t2} data for various HV ggNMOS single- and multi-finger structures indicating poor performance width scaling.

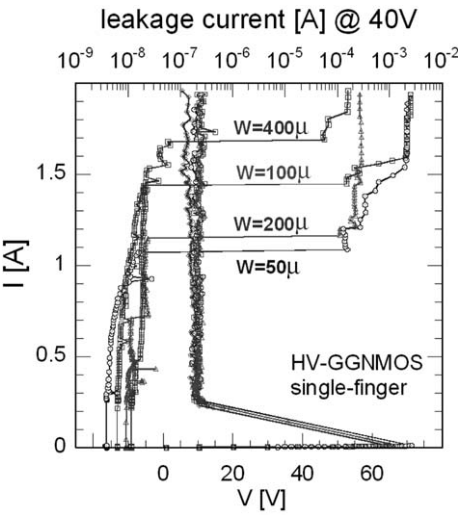

Fig. 4. Non-uniform conduction of ESD current demonstrated for different HV-ggNMOS transistors. The I_{t2} failure current does not scale with the total device width.

with a high defect density due to processing artifacts. This leads to a local reduction of the breakdown voltage and in turn results in a current focusing mechanism. Even single-finger structures are prone to non-uniform ESD performance scaling as demonstrated above in Fig. 3 and by the TLP data in Fig. 4.

Moreover, due to the charge trapping mechanism in the FOX at the bird's beak, the HV NMOS shows critical endurance test problems, if stressed with multiple ESD pulses. A gradual increase of leakage current occurs for multiple TLP zaps at roughly the same amplitude (Figs. 4 and 5). This leakage increase reflects gradual device degradation if the parasitic NPN operates under high current conditions. It is caused by a locally reduced junction breakdown voltage due to charge trapped in the FOX.

Fig. 5 shows TLP measurement results on two identical HV ggNMOS devices using different TLP stress step levels. This technique is used before to define the real failure current level [6]. The final degradation point (to µA leakage) occurs earlier when the stress steps are closer together (high pulse density on the figure). The effect is explained in Fig. 6, showing the current localization and increased degradation during each stress pulse.

2.4. High latch-up risk

In many HV technologies, the ggNMOS holding voltage is much smaller than the maximum supply voltage specification. When used as a power clamp between V_{dd} and V_{ss}, unintended triggering by static or transient latch-up stimuli may occur due to the relatively low holding current of the NMOS multi-finger device.

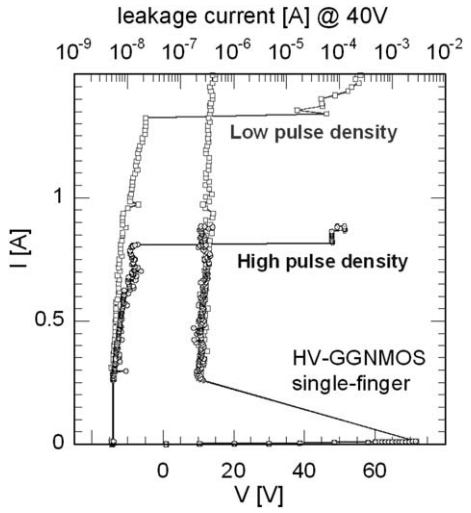

Fig. 5. TLP measurements of a grounded gate HV NMOS snapback clamp in a 0.5 μm (43 V) technology. After snapback, at roughly 73 V, a clear and steady degradation is visible in the leakage current. The final failure current is dependent on the pulse density. When a small stress step is applied, the I_{t2} failure current is much lower.

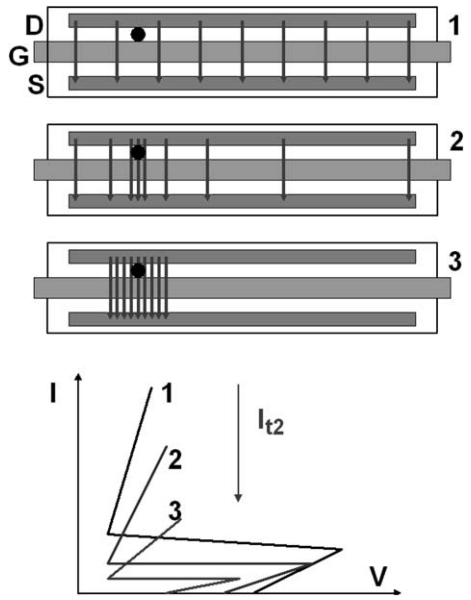

Fig. 6. Charge trapped in the field oxide at the bird's beak reduces the breakdown voltage locally, represented by the black spot at the drain. Due to the reduced breakdown voltage the next ESD stress current (2, 3) will be localized at the black spot, preventing uniform conduction through the whole finger.

Triggering is very critical since the supply voltage cannot recover without going thru a renewed power-up cycle. In the worst case the high DC supply current (from e.g. a car battery) could damage the power clamp. This latch-up issue prevents the application of HV ggNMOS devices as a power clamp.

2.5. Parallel NMOS output driver protection challenge

A major challenge is the design of ESD-robust HV NMOS output drivers due to the multi-finger triggering challenge but also due to an intrinsic device reliability weakness described above. Self-protective drivers based on parasitic bipolar operation are not feasible and often the introduction of an additional protection is required. However, trigger competition between the weak driver and the parallel ESD clamp must be prevented. This objective is difficult to accomplish due to the fact that the trigger voltage of the ESD device must satisfy the high voltage conditions (i.e. trigger voltage above V_{dd}). On the other hand, the protection must turn on at a voltage well below the trigger voltage of the parasitic NPN inherent to the NMOS driver. This sensitive parasitic in the driver can reveal a relatively low trigger voltage because transient gate-bias during ESD stress reduces V_{t1}. Thus, to fulfill normal operation requirements (high $V_{t1} > V_{dd}$) as well as ESD conditions (low V_{t1}(protection) $< V_{t1}$(driver)) it is often impossible to apply static voltage dependent trigger schemes for parallel NMOS driver protection. In this paper another solution is presented where the trigger condition of the local clamp is based on the V_{dd} potential.

2.6. High resistive ESD elements

In HV technologies, the edge of the depletion regions move over larger distances due to the lowly doped diffusions introduced for all HV compatible elements. In order to prevent punch- or reach-through problems that can lead to high IC leakage for instance, critical junction distances must be increased to large dimensions. This has a negative impact for example on the dynamic series resistance of ESD diodes where the anode–cathode spacing becomes relatively large. The TLP-*IV* characteristic of a typical HV N/Pwell diode in Fig. 7 reveals a resistance of almost 5 Ω ($W = 50$ μm). This is roughly one order of magnitude larger than the diode series resistance obtained in standard CMOS technologies for corresponding diode widths.

As mentioned before, HV technologies are mostly based on mature LV technologies. A key issue is the limited number of available metal layers (typically less than 4). The high voltage drop across ESD diodes combined with the high bus resistance leaves only little ESD design margin for critical stress cases.

In conclusion, in many high voltage technologies standard snapback based NMOS protection is not feasible due to intrinsic device weakness and serious ESD and latch-up design issues. This paper will describe an efficient SCR-based alternative.

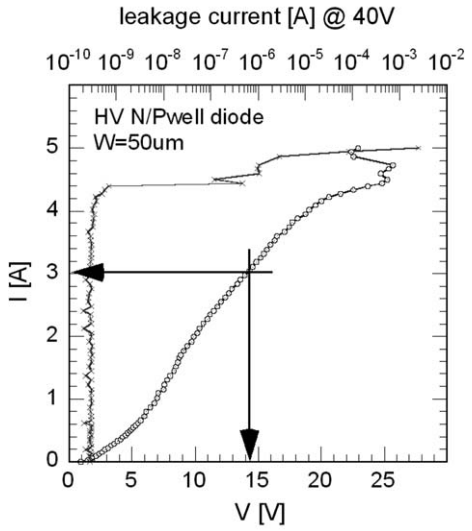

Fig. 7. TLP data of HV-N/Pwell diode ($W = 50$ μm) revealing a large dynamic series resistance.

3. SCR-based, latch-up immune power protection

Because the HV ggNMOS device has a very low holding voltage and non-uniform conduction in the parasitic NPN mode, it cannot be used as a power protection clamp. An alternative approach is to use RC triggered bigFET or Active MOSFET power protection in conjunction with dual diode protection for the IO circuits ('rail based protection scheme' as in [7–9]). In the Active clamp approach the destructive snapback mode is not used. However, due to the large voltage drops across the diode and bus resistance in typical HV applications, the voltage margin in the ESD design window is reduced drastically in those solutions.

SCR-based power protection can enable the ESD protection between V_{dd} and V_{ss} thanks to an excellent clamping behavior at high currents. Its low holding voltage opens the ESD design window and creates margin for the bus resistance and diode voltage drops.

To enable SCR-based power protection a number of issues have been solved.

(1) First, the SCR needs to be triggered into the low resistive mode. Typical for the HV technologies is the very high well-to-well breakdown voltage (~150 V) which is too high for a V_{t1} trigger voltage because the core breakdown voltage is much lower. An external, optimized trigger element is added to lower the V_{t1} trigger voltage. To prevent NMOS degradation and non-uniformity issues, the optimal trigger element for HV SCR-based protection is a PMOS device. In high voltage technologies the PNP does not show a snapback behavior when conducting in parasitic bipolar PNP mode. This allows the PMOS to be used as the trigger element. However, in advanced LV CMOS technologies this needs further confirmation because the PMOS devices can also exhibit a small snapback and failure could occur due to non-uniform conduction.

Since the holding voltage of the HV PMOS is above the V_{dd} potential, there is no latch-up risk when it is used as a V_{dd}–V_{ss} clamp. In principle, one could use a very large PMOS/PNP device as HV power protection clamp. However this requires a lot of Si-area due to the low failure current of the PNP device (1–2 mA/μm). Moreover, adjacent PMOS protection clamps need to be close together due to the high holding voltage and large bus resistance. A simple improvement consists of the PMOS element as a trigger element for the SCR device. The total gate width for the PMOS can then be reduced dramatically because it only needs to conduct the trigger current for the SCR. Because the SCR has a much larger ESD performance per area, the total protection element can be smaller as compared to the PMOS alone. Moreover, the protection clamps can be separated further apart, due to the lower holding voltage of the SCR as compared to the PMOS. Figs. 8–10 show a 43 V application where a HV PMOS transistor handles the low ESD stress currents. When the ESD stress current reaches 300 mA, defined by the external resistors at G2, the SCR is triggered into a low ohmic conduction.

(2) Secondly, the static trigger current and voltage for the SCR needs to be engineered to a high value to prevent unwanted triggering during normal operation. In one case of latch-up tests (Fig. 12, left side) one adds a

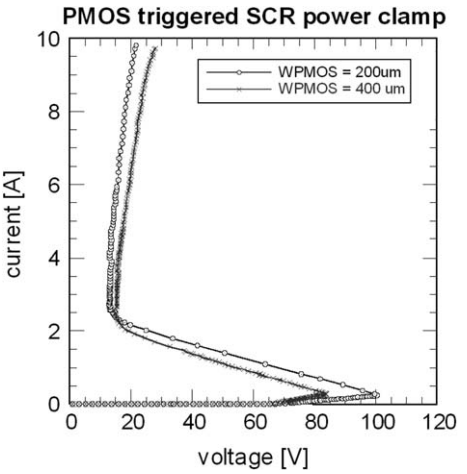

Fig. 8. TLP measurement data on PMOS triggered SCR for power protection. The V_{t1} trigger voltage and I_{t1} trigger current are determined by the external trigger circuit (PMOS and external resistances as in Fig. 10). The SCR-based protection shows a perfect low holding voltage clamping behavior and a very high ESD performance of more than 10 A for a 56 μm wide SCR.

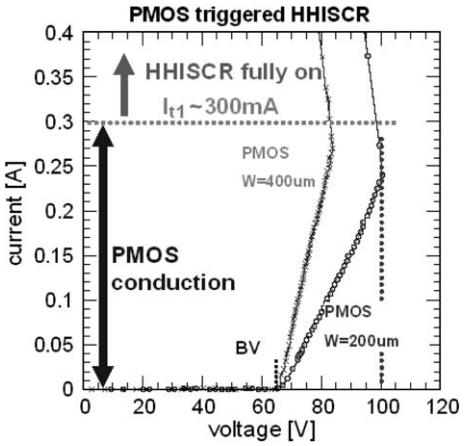

Fig. 9. TLP measurements on a PMOS triggered SCR in a 0.5 μm, 43 V CMOS technology, showing a high trigger current of about 300 mA due to low external resistances between G2 and anode.

fast, positive voltage pulse to the power supply. An increase of the steady-state operation leakage (I_{ddq}) after the pulse reveals a latch-up situation. A high SCR trigger current can be achieved by a correctly designed trigger element and shunt resistance (small value of ~5 Ω). Because the SCR holding voltage is low, the main idea is that the trigger path (trigger element and shunt resistance) has to pass the latch-up tests. This also means that the trigger element needs to generate the SCR trigger current at a voltage higher than the V_{dd} potential to ensure latch-up immune triggering. The PMOS trigger element has an advantage over NMOS based triggering. An NMOS would create a latch-up issue due to the low holding voltage in the parasitic bipolar conduction mode. Both in Fig. 9 and in Fig. 11 large trigger currents are demonstrated by the TLP measurements.

(3) Finally the SCR clamp needs to be designed with a sufficiently high holding current to prevent triggering by substrate current injected into a nearby IO-pad. This current injection is typically performed in a second type of latch-up test (Fig. 12, right side). The device is powered up and current pulses are injected at the different IO's. Good guard band protection around the IO's and power protection elements, sufficient spacing and a segmented layout of the SCR [1] can increase the latch-up immunity levels for this kind of requirement. Also small values for the external resistances at G1 and G2 can improve the latch-up immunity level because they provide a safe shunt path for nearby injected latch-up carriers. The segmentation technique is referred to as "high holding current" or "HHI-SCR".

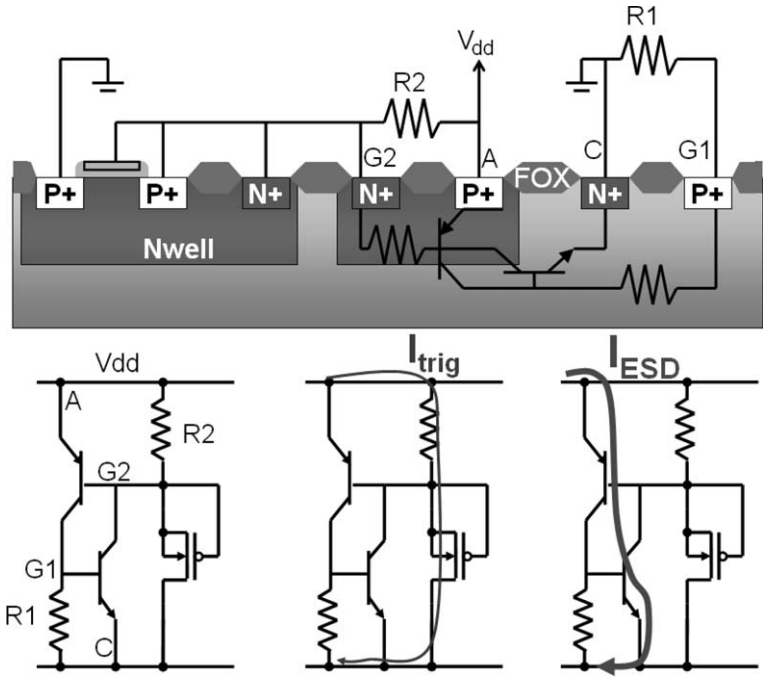

Fig. 10. PMOS triggered SCR schematic and cross-section. The low resistance values prevent unwanted triggering of the SCR during normal operation. The trigger current is determined mostly by the external resistance values ($R1, R2$) while the trigger voltage can be tuned to the desired voltage by selecting an appropriate size for the PMOS trigger element. The middle schematic shows the current flow before the SCR is triggered. The right schematic depicts the current flow during high current stress.

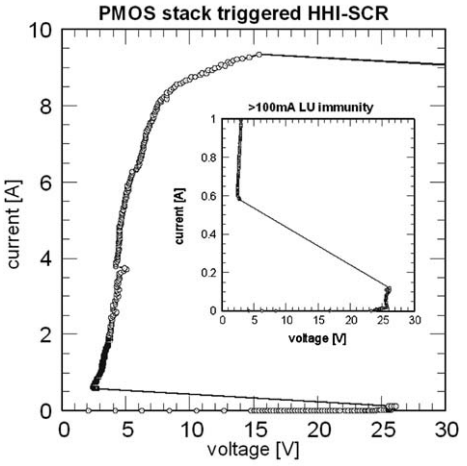

Fig. 11. TLP measurement data on an SCR-based power protection for a 22 V/0.5 μm BiCMOS technology. The SCR is triggered by a stack of two PMOS devices. On the inset of the figure a high trigger current of almost 200 mA can be seen. The high trigger current improves latch-up immunity by preventing unwanted triggering during normal operation. Thanks to the excellent clamping behavior of the SCR device, a very low holding voltage can be obtained which leaves a large voltage margin for other voltage drops in the ESD current path.

4. Local protection using ESD-on-SCR

The previous section described the different options for power protection in high voltage technologies. This section first discusses the issues with output driver protection. For input-only pads there is no danger because the transient gate oxide breakdown is very high thanks to the thick gate oxide used in high voltage applications. For input-only pads a dual diode ESD protection is sufficient and preferable. However for IO or output-only pads a local protection needs to be added due to the intrinsic weakness of the HV NMOS output driver. Moreover the V_{t1} trigger voltage of the NPN is typically lowered due to the 'floating gate' NMOS output drivers.

Many applications, e.g. in the automotive field only require HV on some output pins, but not on the supply. For HV pins with a strong drive capability (total gate width >5000 μm) it is possible to make them self-protecting in normal MOS mode preventing the destructive NPN snapback. This is e.g. described in [11].

First, the design window for output pads is determined for both the 0.5 μm HV CMOS and the 0.5 μm BiCMOS examples. Secondly, the operation principle of the ESD-on-SCR clamp is described. Finally, the influence of the circuit elements is discussed.

4.1. Design windows in the 43 V/0.5 μm CMOS application example

The 43 V technology is used for the automotive and display driver market. The application example is a 128× output OEL (Organic Electroluminescent) display driver chip. Although the maximum supply voltage is defined as 43 V, the power clamp leakage needs to be limited below 1 nA for voltages up to 54 V. Latch-up immunity (at room temperature) up to 300 mA is specified, by extrapolation from the LU specification of 100 mA at 125 °C. The 200 V MM (≈3 A peak current) specification further defines the ESD design window for the power clamp and demands a device with a rather low-ohmic clamping characteristic. The power clamp has been created using a PMOS triggered SCR as described above (Fig. 10). Latch-up immunity levels up

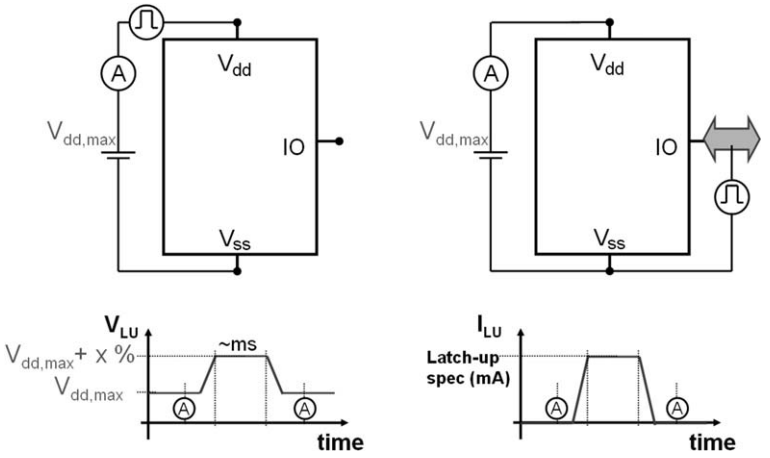

Fig. 12. Two main types of latch-up tests. On the left figure the chip is powered up and an additional short voltage pulse is applied on the V_{dd} line. On the right figure, the chip is powered up and a current pulse (~100–200 mA) is injected into the different IO's. Steady-state core leakage is compared before and after the pulse. In the case of a latched powerclamp the leakage measurement will show an increased value.

to 300 mA and ESD MM levels above 250 V have been achieved in a real product application.

The maximum IO output voltage during normal operation is defined as 43 V. For the local protection of the output driver, the minimum trigger voltage is defined by this maximum signal voltage plus 10% safety margin (47 V). On the other hand the maximum trigger voltage is defined by the lowest V_{t1} trigger voltage of the NMOS. This is limited to merely 54 V for the output driver NMOS device with floating gate (undefined potential at the gate during ESD). The local protection needs to prevent a snapback event in the output driver device because such snapback will cause degradation in the HV NMOS (see Fig. 4). A summary of the narrow design window is depicted in Fig. 13: The V_{t1} trigger voltage needs to be between 47 V and 54 V. Because it is challenging to tune a junction breakdown (as a trigger condition) to such a narrow window, another approach has been selected as will be discussed below.

4.2. Design windows in the 22 V/0.5 μm BiCMOS application example

The second example shows data in a 22 V technology. The minimum power clamp triggering voltage is 24 V. For latch-up considerations, the NMOS cannot be used to trigger the SCR clamp, because the NMOS holding voltage is below $V_{dd} = 22$ V. The PMOS breakdown is at 11 V. A stack/cascode of two PMOS devices is used as a back-up path for the first 200 mA of ESD or latch-up current. A TLP measurement (and zoom-in) that fits inside the design window is depicted in Fig. 11.

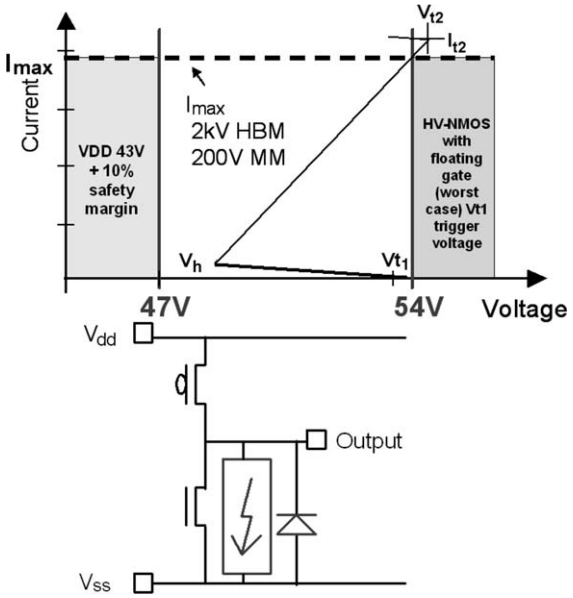

Fig. 13. Summary of the design window for the output driver in a 43 V/0.5 μm CMOS technology. The required robustness level ($I_{max} = 3$ A) of the local protection is defined by the HBM (2 kV) and MM (200 V) specifications and is based on correlation measurements in the process under study. The minimum static trigger voltage is 47 V as defined by the $V_{dd} + 10\%$ normal operation region. The maximum trigger voltage is defined to prevent triggering of the HV NMOS output driver (54 V).

4.3. Principle of ESD-on-SCR

In both examples the design window for the local protection of the NMOS output driver is narrow and a static voltage triggered protection is not feasible. A novel approach has been used instead.

A 'self-controlled' or 'self-aligned' protection element is created by connecting the G2 (Nwell) of an SCR to the V_{dd} line (similar approach as in [10]). The schematic and cross-section are shown in Fig. 14.

4.3.1. Low leakage

A DC measurement with a V_{dd} bias of 50 V (Fig. 15) shows that the leakage specification can be met because the anode–G2 diode is reverse biased for voltages up to ($V_{dd} + \sim 0.6$ V). A similar DC *IV* curve is measured whenever there is a 'diode up' between the pad and the V_{dd} line. Typical examples are the dual diode protection approach or the intrinsic parasitic P+/Nwell diode in PMOS output drivers. The 'diode up' between pad and V_{dd} starts to conduct once the pad voltage is above the applied V_{dd} potential.

4.3.2. V_{dd} voltage dependence

In HV technologies it is custom that the operating voltage depends on the specific (display) application. This means that the minimum trigger voltage for the

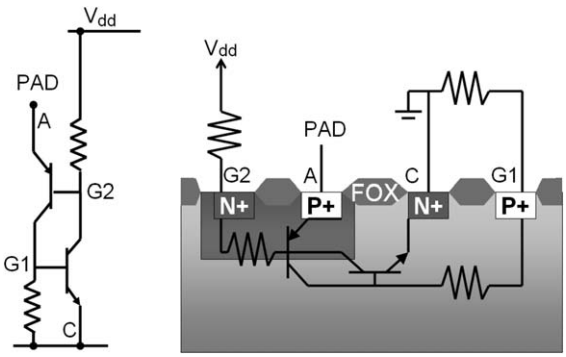

Fig. 14. Schematic and cross-section of the ESD-on-SCR. The G2 node (Nwell connection) is connected to V_{dd} to minimize leakage by keeping the SCR off during normal operation and to maintain a low capacitive input protection. During ESD stress between pad and V_{ss}, the V_{dd} is floating which enables very low voltage triggering. When the Nwell is floating, the SCR will turn on 'instantly'.

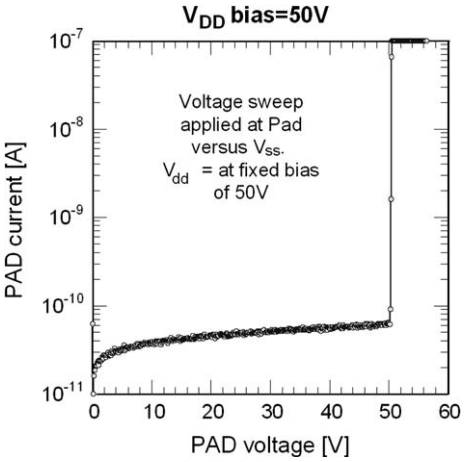

Fig. 15. DC measurement (on 0.5 μm 43 V technology) to detect the leakage level at the maximum operating voltage of the process (V_{dd} bias is at 50 V). The SCR only conducts current after the pad-V_{ss} voltage exceeds the V_{dd}. The Nwell connection (G2) of the SCR is connected to the V_{dd} supply line to prevent SCR triggering during normal operation.

local protection is not fixed. Fig. 16 shows measurement results for different V_{dd} supply voltages. The SCR has a low leakage value up to the applied V_{dd} voltage. The SCR triggers only when the voltage at the IO-pad rises above the V_{dd} potential. The trigger condition for ESD stress between IO-pad and V_{ss} is explained in the next part.

4.3.3. Triggering

In the case of an ESD stress between the pad and the V_{ss} line, the SCR triggers at a low voltage because the V_{dd} line (and thus G2) is floating which makes it easy to forward bias the anode–G2 (emitter-base junction) of the PNP. Because the SCR is instantly on during ESD, the device is called an 'ESD-on-SCR'.

In case of an ESD stress (as in the TLP measurements shown in Fig. 17) between IO-pad and V_{ss}, the V_{dd} line is coupled to the V_{ss} potential by the parasitic capacitance in the power domain connected to G2 (Fig. 18). The diode from anode to G2 is easily forward biased, charging up the V_{dd} to V_{ss} capacitance through the G2–V_{dd} connection.

Additionally, during this ESD stress case, the core between V_{dd} and V_{ss} is in an undefined state, which

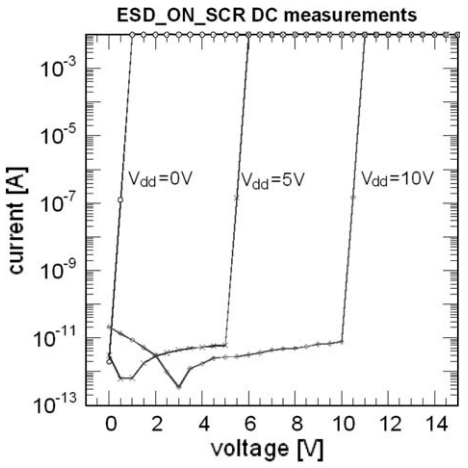

Fig. 16. DC measurements (on 0.5 μm 22 V technology) with different V_{dd} bias at G2 of an ESD-on-SCR device. The SCR is completely off for pad voltages below the applied V_{dd} voltage.

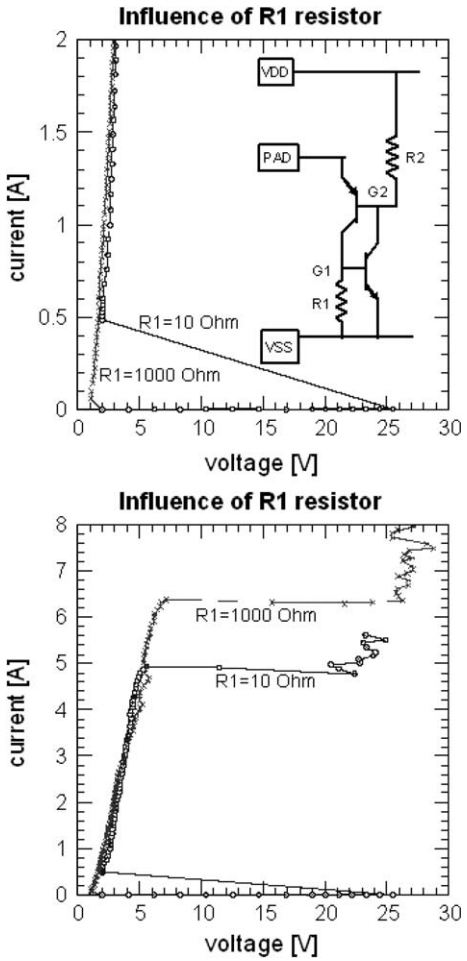

Fig. 17. TLP measurements on two ESD-on-SCR devices (22 V BiCMOS technology with isolated Pwell) with different G1 to substrate resistances. In the case of a small R1 value more current is needed through the PNP to forward bias the base emitter junction of the NPN device which shows up as a much higher SCR trigger voltage V_{t1}. The ESD-on-SCR devices show a current capability of more than 5 A for 100 μm total anode/cathode width.

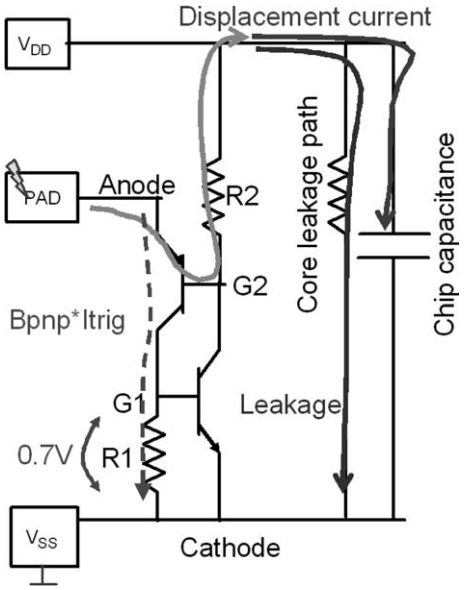

Fig. 18. Trigger concept of the ESD-on-SCR: (A) The anode–G2 junction is easily forward biased during an ESD event between pad and V_{ss} due to a floating G2 node. (B) The base current in the PNP will be amplified and flows to V_{ss} through the R1 resistor. The NPN and thus the SCR will be turned on when 0.7 V is created across resistor R1.

can be represented by a leakage path of a few kilo ohms. The current flowing from G2 to V_{dd} is the base current for the parasitic PNP device within the SCR. The current $I_{basePNP}$ is amplified between the collector and the emitter with a factor of $Beta_{PNP}$ (Fig. 18). When that amplified current creates a voltage drop of 0.7 V over the resistor R1 between G1 and the cathode, the SCR will latch into a low holding state, clamping the anode (IO-pad) and the cathode (V_{ss}) together thereby protecting the IO circuit. The trigger condition for the SCR can be written as:

$$I_{basePNP} \times R1 \times Beta_{PNP} = 0.7\ \text{V}.$$

The V_{t1} trigger voltage of the protection device is a function of the base current in the PNP that is needed to fulfill the above relation. The influence of the R1 resistor on the V_{t1} trigger point can be clearly seen in Fig. 17, where TLP measurements with two values of R1 are compared. For a small $R1$, a large current is needed through the PNP, which means that more base current is required. The higher base current will flow from V_{dd} to V_{ss} through the leakage path and increase the V_{dd} to V_{ss} potential. A higher voltage at the pad is needed to sustain a forward biased anode–G2 diode, resulting in a larger V_{t1}.

From this analysis it is clear that the parasitic capacitance and leakage between V_{dd} and V_{ss} have an influence on the triggering of the SCR. IC applications with a large number of elements between V_{dd} and V_{ss} will present both a large parasitic capacitance and a large leakage during ESD stress. For these applications the ESD-on-SCR approach can be used as is because the required trigger current will flow at a low V_{t1} trigger voltage.

For chips with sensitive IO's in a small power domain, the G2 node can be tied to a V_{dd} line from another domain with more parasitic capacitance. The main constraint is related to the normal operation voltage of this V_{dd} line: the V_{dd} voltage has to be higher than the maximum IO signal voltage to reverse bias the anode–G2 junction during normal operation. For all other cases a dedicated trigger path can be inserted with the sole purpose to create enough leakage between G2 and V_{ss} during ESD conditions.

As a conclusion, the ESD-on-SCR can trigger at a very low V_{t1} voltage and can remain in a low leakage state during normal operation.

4.4. Influence of circuit elements

There are some issues that need to be considered when implementing this type of local protection clamp. It is required that there is sufficient base current in the PNP device. Suppose a 'diode-up' is added between the IO-pad and the V_{dd} line. The ESD current injected at the IO-pad has now two parallel paths to flow to V_{dd}: through the emitter-base of the PNP and a second competing path through the 'diode-up'. In most cases the 'diode-up' is less resistive than the anode–G2 diode. This means that less current will flow through the PNP base. This has a negative impact on the V_{t1} trigger voltage however measurements have shown only a limited effect.

In the ESD-on-SCR approach, the anode and the G2 node are not connected together. This can introduce additional leakage between V_{dd} and IO-pad if the reverse breakdown voltage of the P+/Nwell diode is lower than the supply voltage. For positive ESD stress applied at the V_{dd} versus the IO-pad (Fig. 19), a part of the ESD current can flow through the anode–G2 junction of the ESD-on-SCR if the V_{t1} trigger voltage of the power clamp is higher than the P+/Nwell breakdown. The critical condition is determined by the V_{t2} failure voltage of the anode–G2 junction, the V_{t1} trigger voltage of the power clamp and the voltage drop over the 'diode-down':

$$V_{t2\_diode} > V_{t1\_Powerclamp} + V_{diode\_down}$$

The anode–G2 junction can be protected by adding another diode or the resistance $R2$. In both cases the V_{t2} failure voltage of this current path will increase. However, these additional elements have a negative effect on the V_{t1} trigger voltage of the ESD-on-SCR because more trigger current is required to turn on the SCR. This results in a slightly higher V_{t1} trigger voltage as can be seen in Fig. 20.

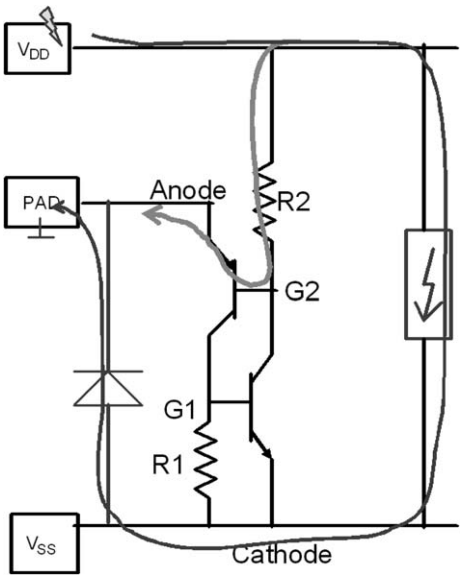

Fig. 19. ESD stress from V_{dd} to pad can damage the anode–G2 junction from the ESD-on-SCR when the trigger voltage V_{t1} of the power clamp is much higher than the failure voltage V_{t2} of this junction. This can be prevented by inserting a resistance $R2$ which then protects the anode–G2 junction. In some HV technologies, the failure current of this reverse diode can be small and as such a large $R2$ resistance value is required.

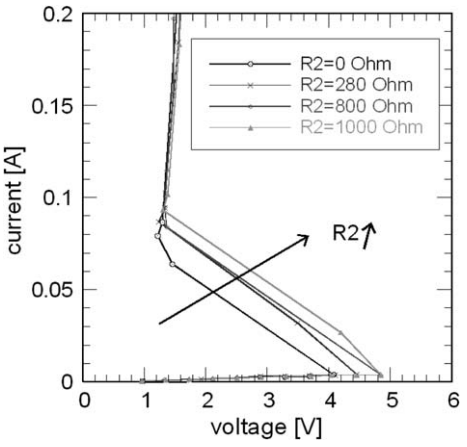

Fig. 20. Influence of the $R2$ resistance between G2 and V_{dd} on the trigger behavior of the ESD-on-SCR.

5. Conclusions

This paper reviewed different issues encountered in high voltage technologies. Measurement data from medium and high voltage technologies showed a degradation problem in the NMOS. This disables the parasitic NPN current conduction for use in ESD solutions due to current non-uniformity. Further, the low holding voltage at high injection (Kirk-effect) prevents the use of ggNMOS power protection clamps based on latch-up constraints.

Because of the high resistive voltage drops in basic ESD protection elements and power bus sections, the power clamps in HV applications need an extremely low holding voltage. This paper focused on SCR-based power protection triggered by PMOS elements. The technique is successfully applied in two different technologies showing very high ESD performance and high latch-up immune product applications.

The HV NMOS output driver has been successfully protected using an SCR-based local clamp in different technologies. Due to the extremely narrow design window, static voltage dependent triggering is not an option. In this paper a novel trigger scheme for SCR protection, based on V_{dd}-potential detection, has been shown and discussed in detail. The ESD-on-SCR allows protection of critical nodes at a low V_{t1} trigger voltage during ESD while ensuring low leakage operation during normal operation. Although this clamp was discussed for HV applications it can also be applied with the same ease to protect thin gate oxides in advanced CMOS technologies maintaining a low leakage and a low capacity at the input node.

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References

[1] Mergens M, Russ C, Verhaege K, Armer J, Jozwiak P, Mohn R. High holding current SCR (HHI-SCR) for ESD protection and latch-up immune IC operation. In: Proc EOS/ESD 2002. p. 10–7.
[2] Steinhoff R et al. Current filament movement and silicon melting in an ESD-robust DENMOS transistor. In: Proc EOS/ESD 2003. p. 98–106.
[3] Mergens M et al. Analysis of lateral DMOS devices under ESD stress conditions. IEEE TED 2000(November): 2128–36.
[4] De Heyn V, Groeseneken G, Keppens B, Natarajan M, Vacaresse L, Gallopyn G. Design and analysis of new protection structures for smart power technology with controlled trigger and holding voltage. IEEE international reliability physics symposium proc, 2001. p. 253–8.
[5] Mergens M et al. Multi-finger turn-on circuits and design techniques for enhanced ESD performance and width-scaling. In: Proc EOS/ESD 2001. p. 1–11.
[6] Keppens B et al. Contributions to standardization of transmission line pulse testing methodology. In: Proc EOS/ESD 2001. p. 461–7.
[7] Torres CA, Miller JW, Stockinger M, Akers MD, Khazhinsky MG, Weldon JC. Modular, portable, and easily

simulated ESD protection networks for advanced CMOS technologies. In: Proc EOS/ESD 2001. p. 82–95.
[8] Poon SS, Maloney TJ. New considerations for MOSFET power clamps. In: Proc EOS/ESD 2002. p. 1–5.
[9] Smith JC, Boselli G. A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies. In: Proc EOS/ESD 2003. p. 8–16.
[10] Chen JZ, Amerasekera A, Duvvury C. Design methodology for optimizing gate drive ESD protection circuits in submicron CMOS processes. In: Proc ESD/EOS 1997. p. 230–9.
[11] van Zwol et al. ESD protection by keep-on design for a 550 V fluorescent lamp control IC with integrated LDMOS power stage. In: Proc EOS/ESD 2002. p. 267–73.