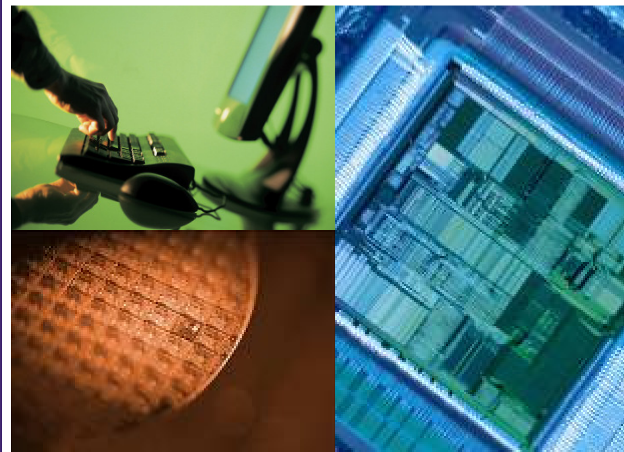
# Analog Design at 65 nm

Bob Lefferts, Navraj Nandra
Mixed-Signal IP
SNUG Israel 2007



SYNOPSYS®
Predictable Success

## •CONFIDENTIAL INFORMATION

•The following material is being disclosed to you pursuant to a non-disclosure agreement between you or your employer and Synopsys. Information disclosed in this presentation may be used only as permitted under such an agreement.

## •LEGAL NOTICE

•Information contained in this presentation reflects Synopsys plans as of the date of this presentation. Such plans are subject to completion and are subject to change. Products may be offered and purchased only pursuant to an authorized quote and purchase order. Synopsys is not obligated to develop the software with the features and functionality discussed in the materials.

# Outline

- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary



SYNOPSYS®
Predictable Success

# Outline

- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary



SYNOPSYS® Predictable Success

# Analog Versus Digital @ 65 nm

- Digital design
  - Significant density increase
  - Small, high speed, leaky devices
    - With lots of variation in timing…..
  - Effort focused on lower power techniques, SI effects, DFM
- Analog design
  - Increase in gate & off-state leakage
  - Decreased output impedance (poorer current sources)
  - Increased “Sources of Variation”
- Mixed signal design: using thin gate vs. thick gate circuits
  - Most analog designs use more than one gate oxide (core + I/O)
  - Analog device sizes set by precision, not minimum dimensions
  - “Same old” thick gate devices for slow speed analog circuits
    - *It is still possible to build high precision circuits*



SYNOPSYS®
Predictable Success

# Key Trends In Transistor Scaling

Strained Si, high mobility channel → $\mu_{eff}$

High K → $\varepsilon_{ox}$

Gate work function → $V_t$

$$\frac{1}{\tau} = \frac{I_{ds}}{C \times V_{dd}} \sim \frac{\mu_{eff}\,\varepsilon_{ox}}{\sum C}\,\frac{1}{L_g T_{ox}}\,\frac{(V_{dd} - V_t)^{1\sim 2}}{V_{dd}}$$

Intrinsic, parasitic interconnect → $\sum C$

Transistor scaling → $L_g$, $T_{ox}$, $V_{dd}$

© 2006 Synopsys, Inc. (6)

Bottom-line: technology scaling hurts analog
Scaling effects not understood & modeled hurts SoC

# Analog vs Digital Partitioning

- Move as much as possible into the digital domain
  - Digitally controlled PLL
    - PVT insensitive loop filter, loop dynamics
  - Digital control of simple analog function
- Digital access into analog domain – analog test bus
  - You need visibility into analog circuits to be able to verify device matching
- Use analog circuits (feedback) to remove normal variation
  - Examples:
    - PLL
    - Duty cycle correction
- Mixed Signal Design Example : DCC



SYNOPSYS®
Predictable Success

# Outline

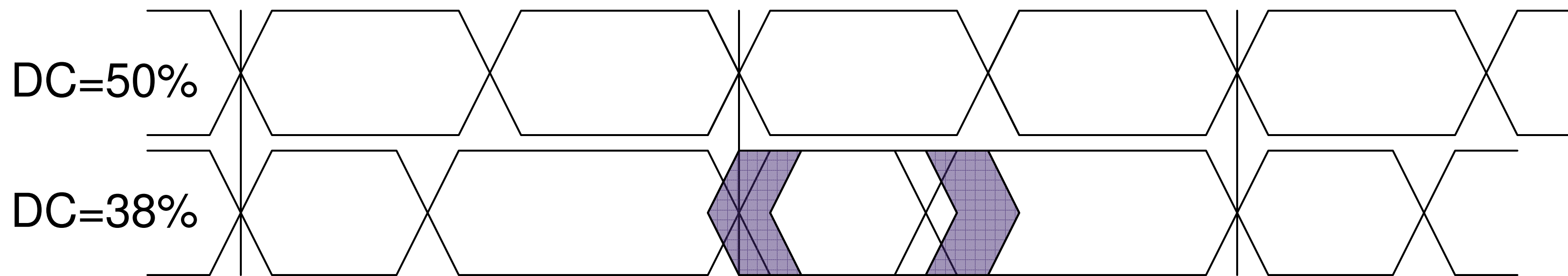
- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary



SYNOPSYS®
Predictable Success

# Duty Cycle Correction : Clocks

- Many systems use DDR (Double Data Rate) techniques where data transitions on BOTH edges of the clock
- PLL's can remove variation in period (frequency) but Duty Cycle variations show up as jitter with DDR




- Clock sources do not naturally produce exactly a 50% duty cycle
  - PMOS pulls up, NMOS pulls down
  - Difficult to "Dead Recon"
- Duty Cycle Correction
  - Actively force 50% duty cycle independent of the source clk



SYNOPSYS®
Predictable Success

# Duty-Cycle Corrector

The job of the DCC amp is to change the duty cycle of the 2nd stage to cancel any incoming duty cycle error or and error that is generated by the buffer stages in the clock distribution.

Core Supply (~1V)

IO S

Dcc amp

A variable duty cycle delay stage is built by controlling the strength of the pull-up device using a DC bias on the PMOS gate. The bias is controlled by a slow speed precise amplifier that is looking at the final output clocks

If the DCC amp is perfect, the two clocks CLK0 and CLKo bar will have EXACTLY a 50% duty cycle.

CLKo

CLKi

Core Logic Supply

Variable Duty Cycle

$\overline{\text{CLKo}}$

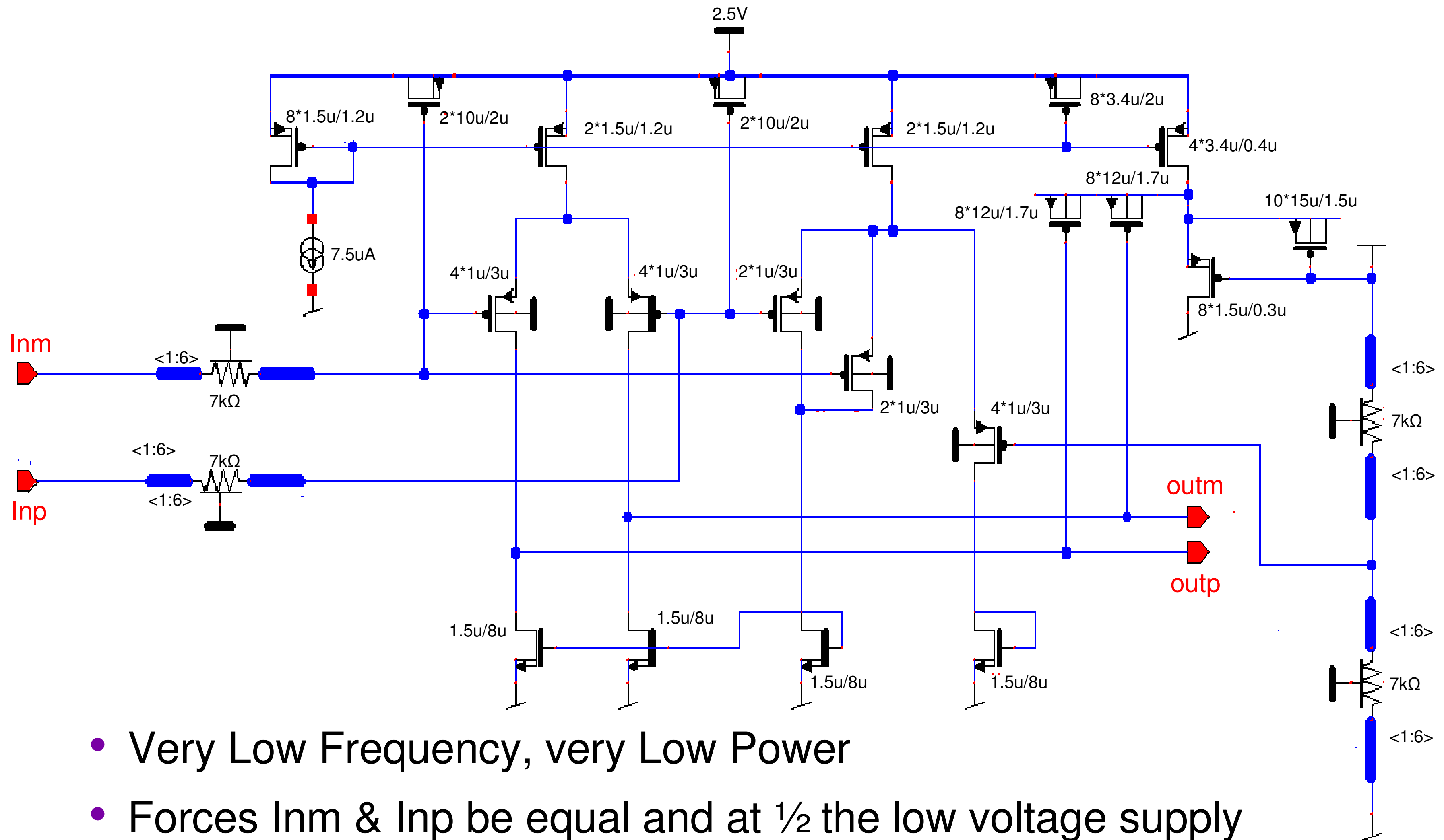
$\overline{\text{CLKi}}$

*Add a variation to cancel another variation…*



SYNOPSYS®
Predictable Success

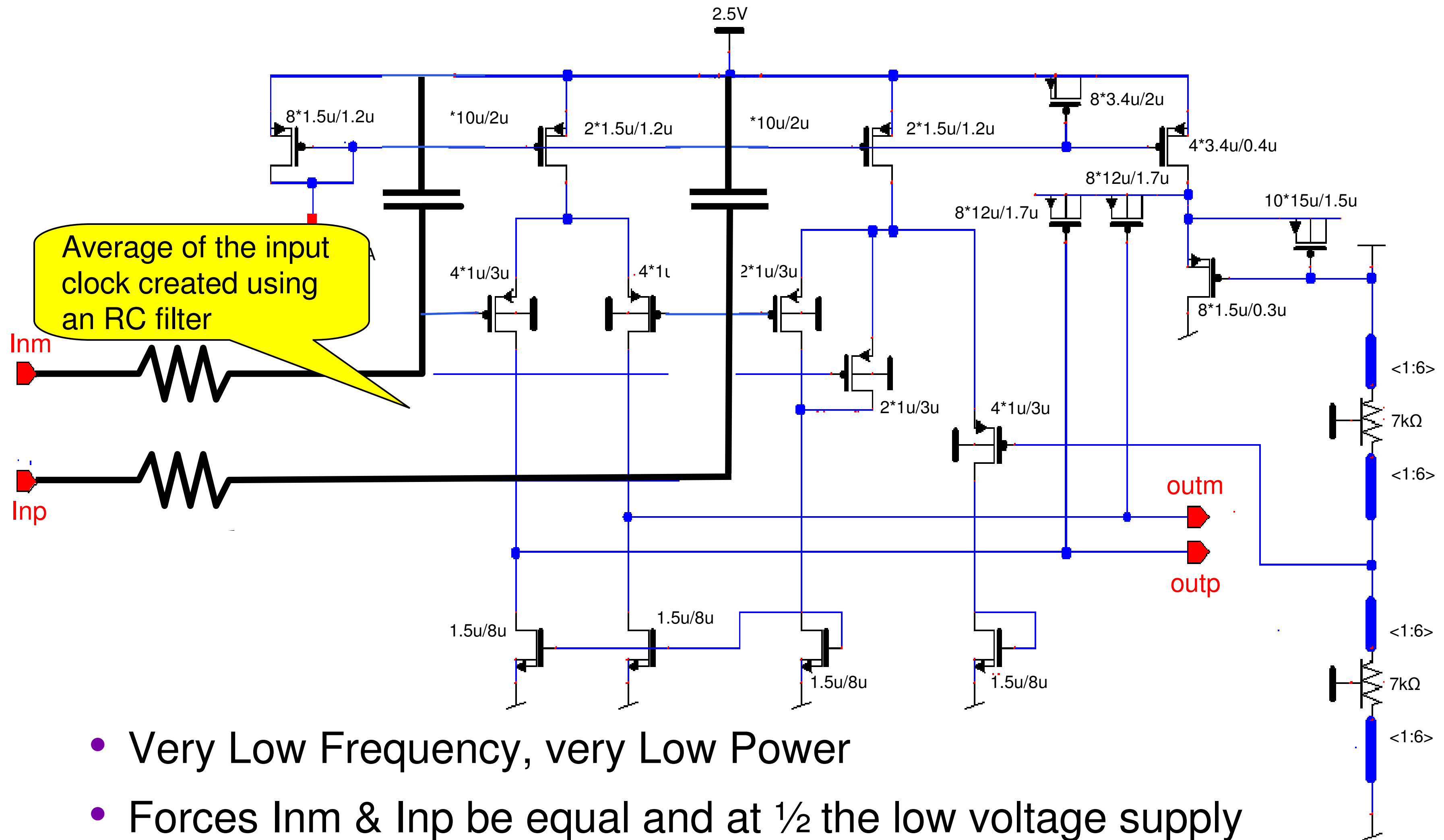
# DCC Amp Schematic




- Very Low Frequency, very Low Power
- Forces Inm & Inp be equal and at ½ the low voltage supply

© 2006 Synopsys, Inc. (12)

# DCC Amp Schematic

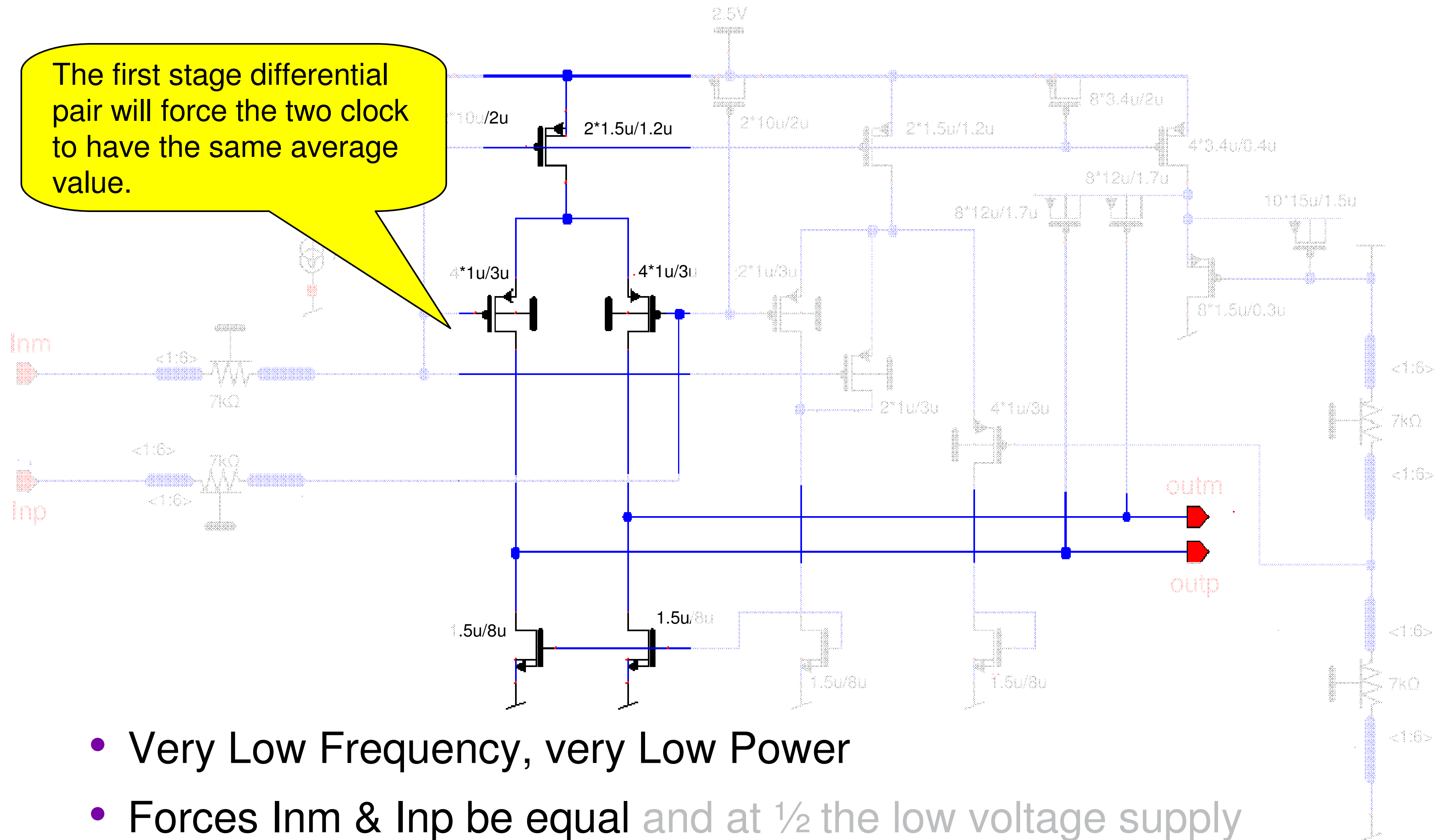



- Very Low Frequency, very Low Power
- Forces Inm & Inp be equal and at ½ the low voltage supply

© 2006 Synopsys, Inc. (13)

SYNOPSYS® Predictable Success

# DCC Amp Schematic

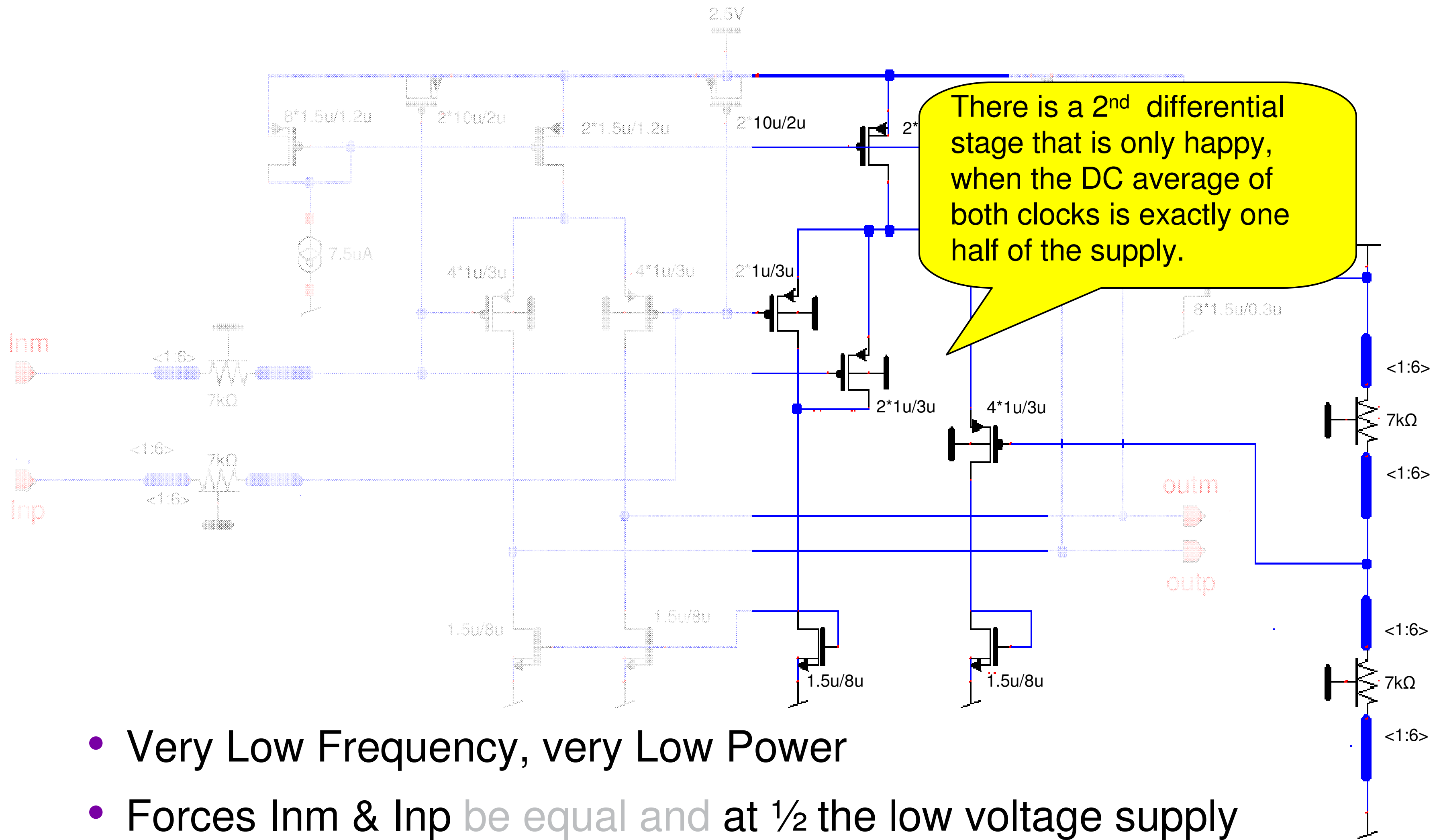



- Very Low Frequency, very Low Power
- Forces Inm & Inp be equal and at ½ the low voltage supply

© 2006 Synopsys, Inc. (14)

SYNOPSYS® Predictable Success

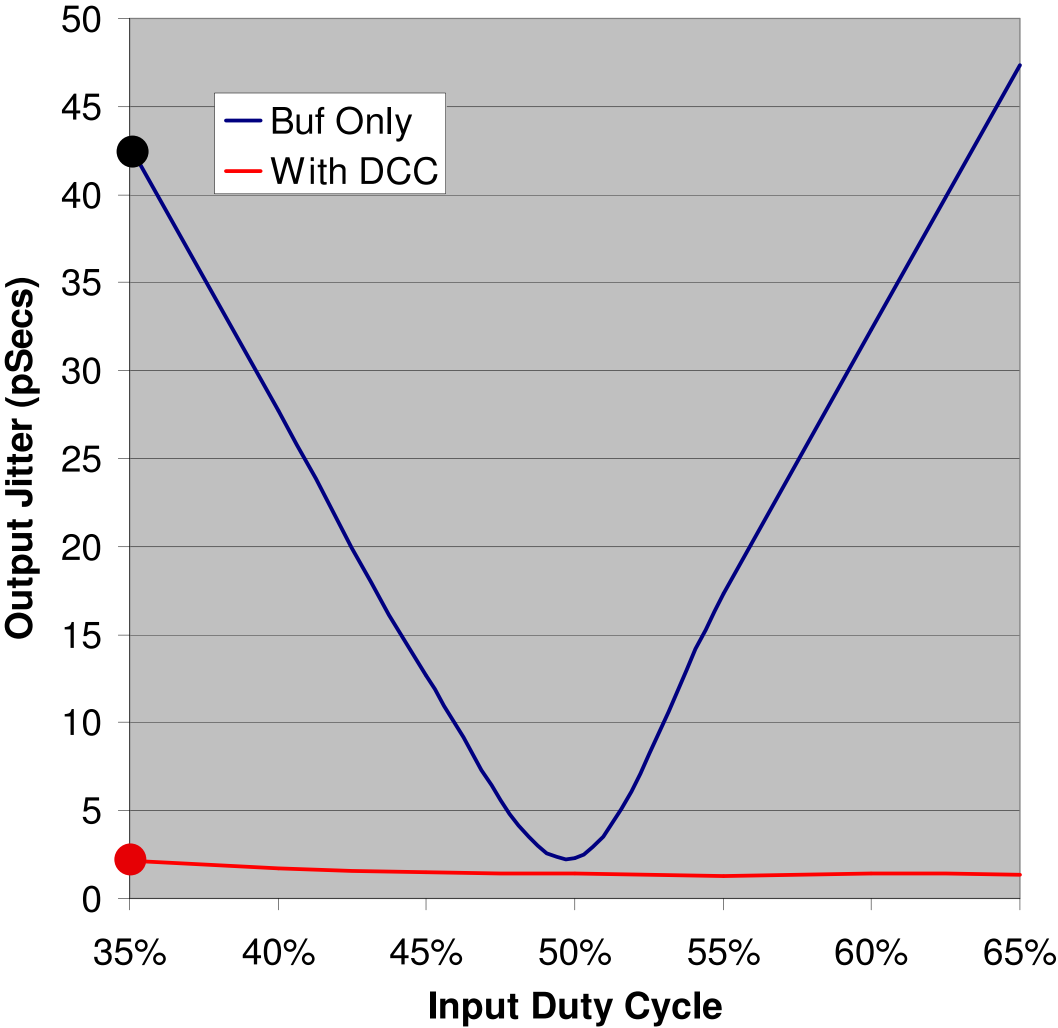
# DCC Amp Schematic

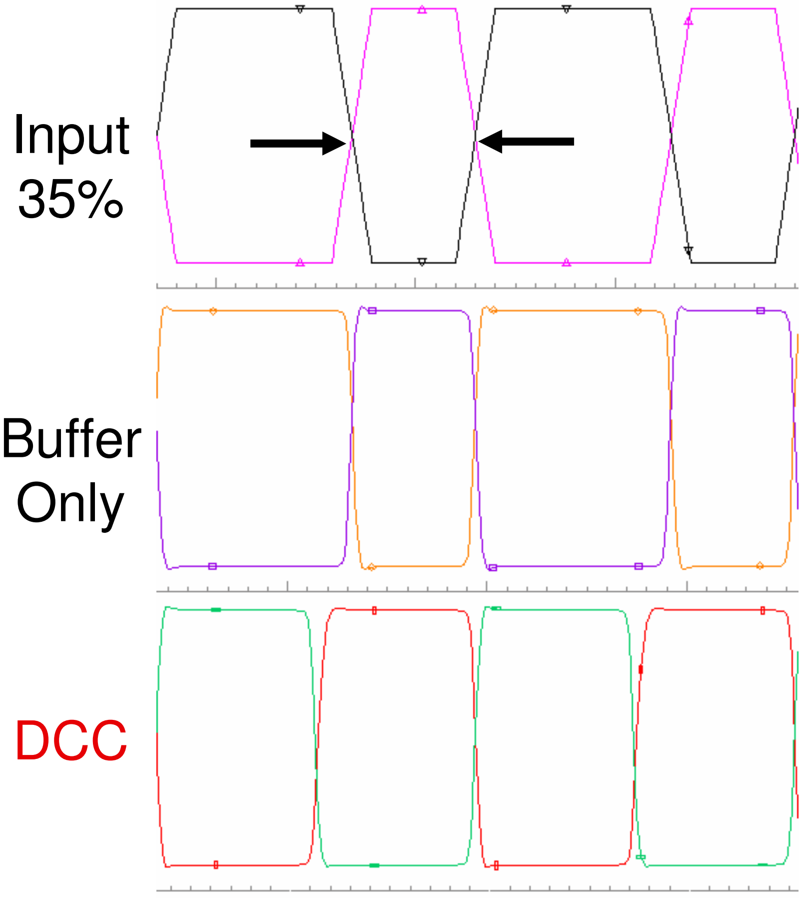



- Very Low Frequency, very Low Power
- Forces Inm & Inp be equal and at ½ the low voltage supply

© 2006 Synopsys, Inc. (15)

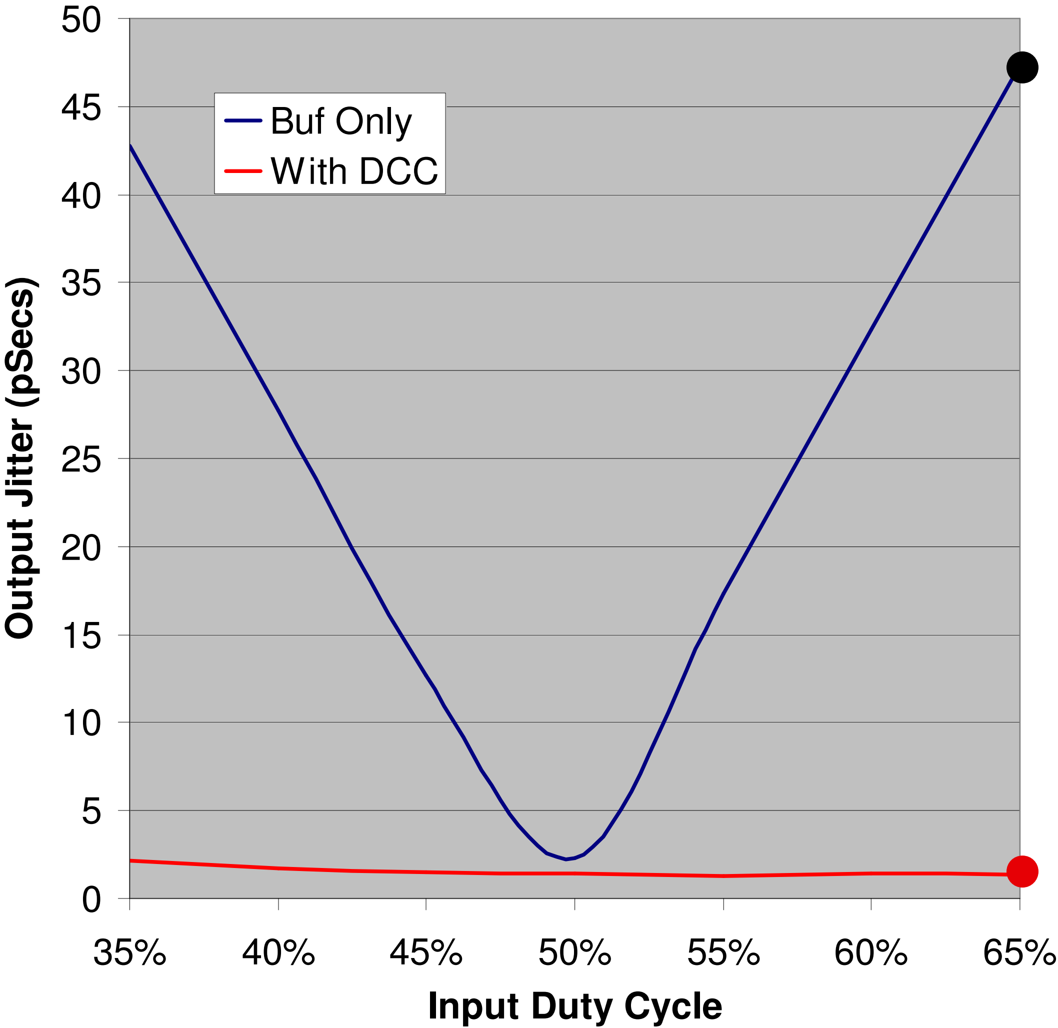
# Active Duty Cycle Correction : Results

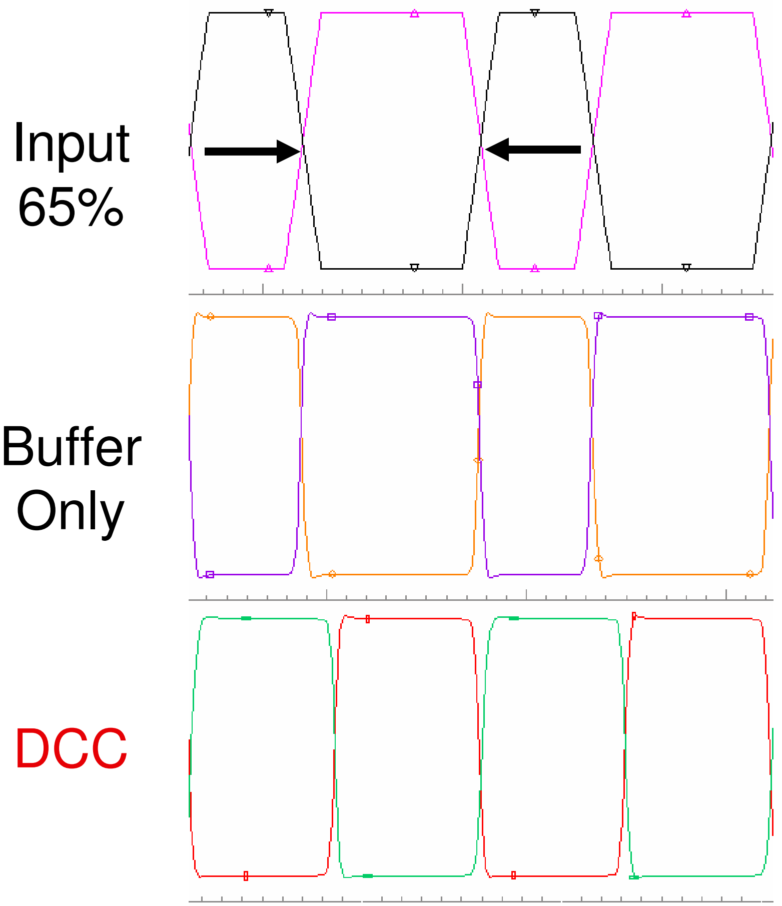



© 2006 Synopsys, Inc. (16)

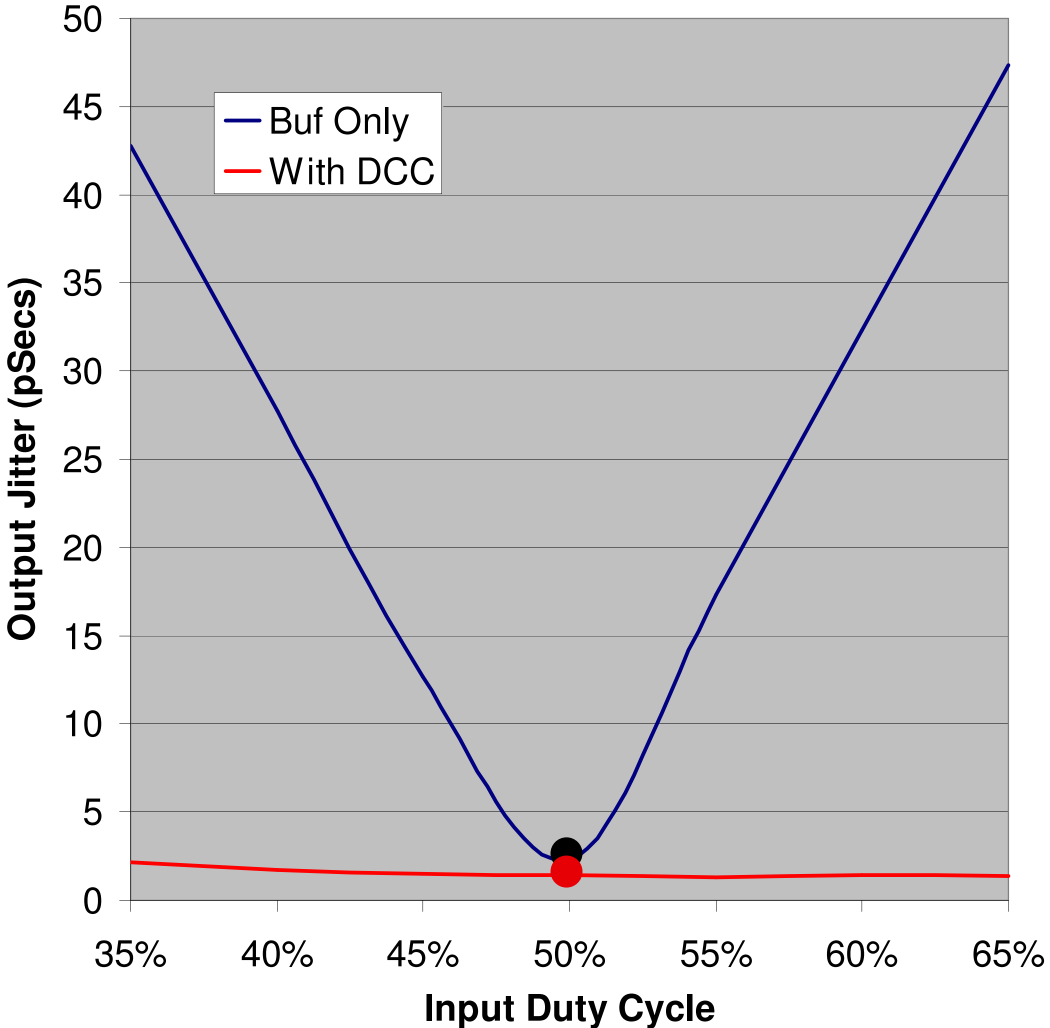
# Active Duty Cycle Correction : Results

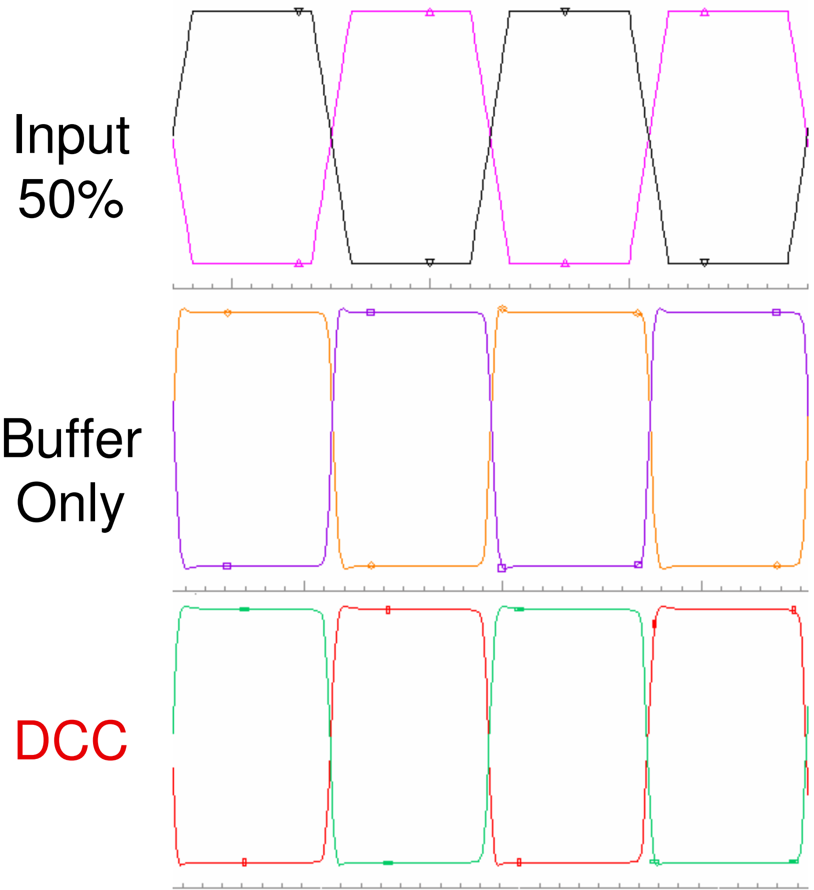



© 2006 Synopsys, Inc. (17)

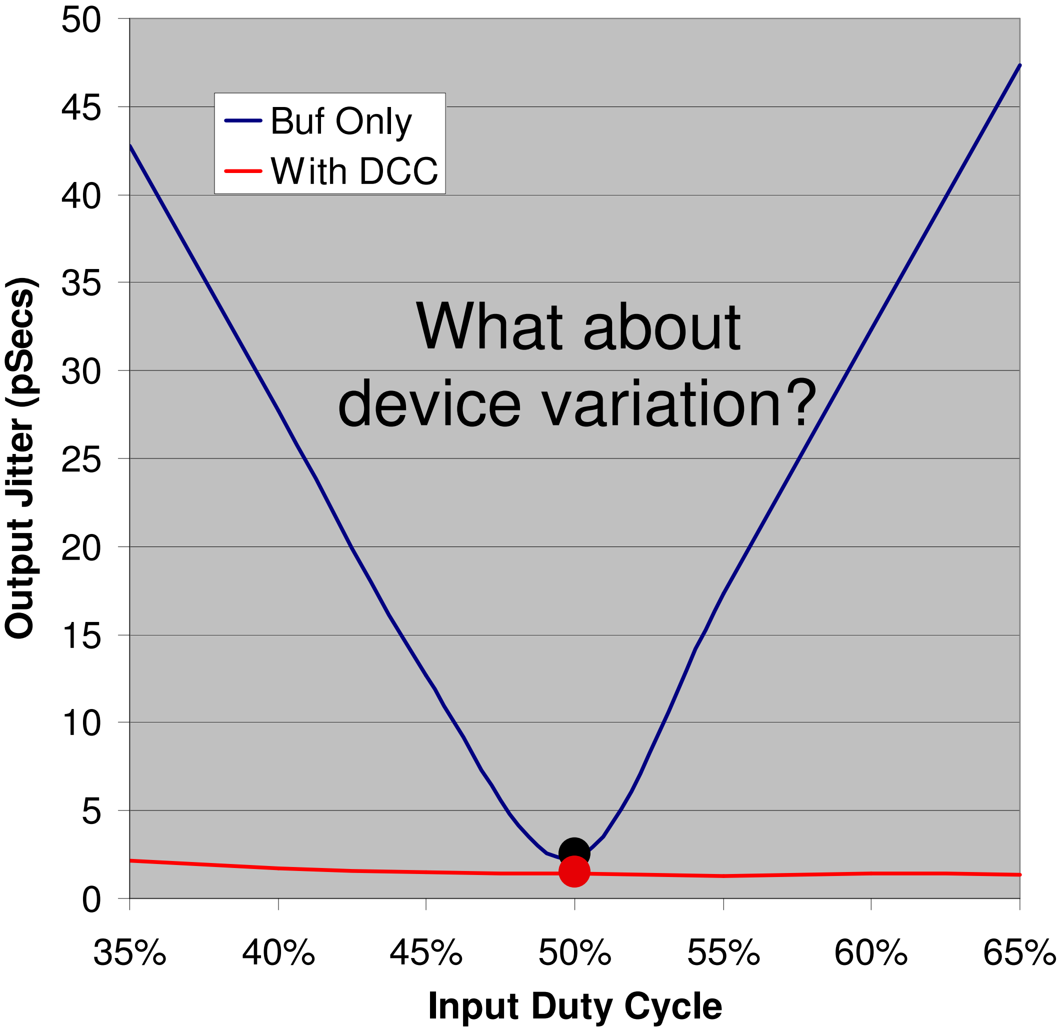
# Active Duty Cycle Correction : Results

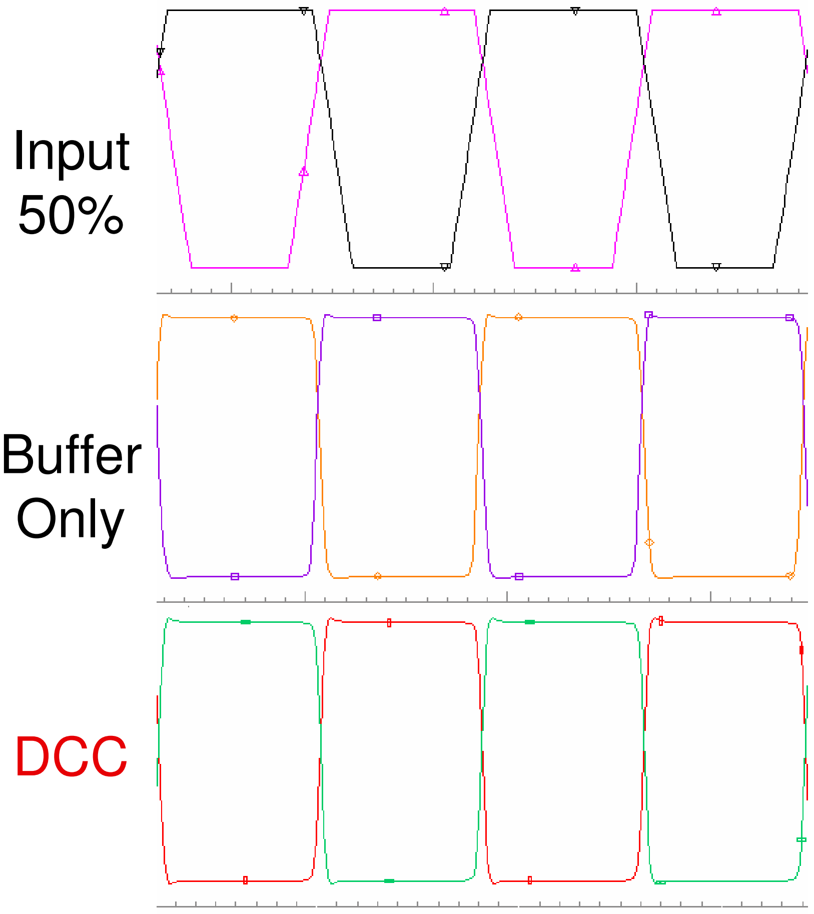



© 2006 Synopsys, Inc. (18)

# Active Duty Cycle Correction : Results





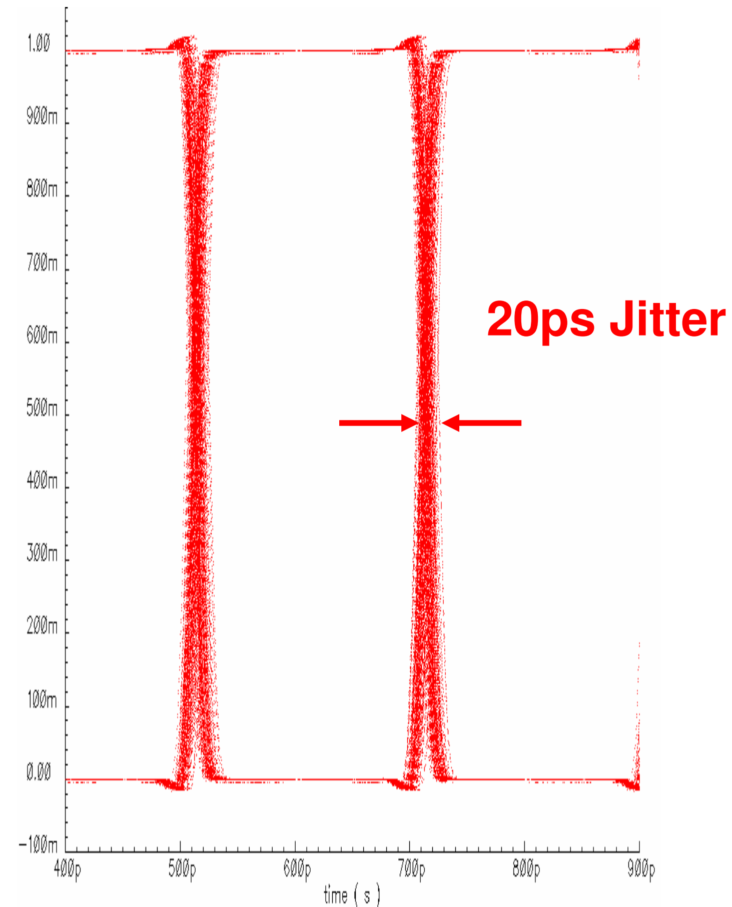

SYNOPSYS®
Predictable Success

# Variation due to device miss-match

- Buffer chain rise and fall times are dependent on the relative strengths of NMOS & PMOS.
- Variation in devices due to their small size causes variation in the output of a buffer chain
  - 3σ Idsat miss-match

$$\frac{\sim 3\%}{\sqrt{L \cdot W}}$$

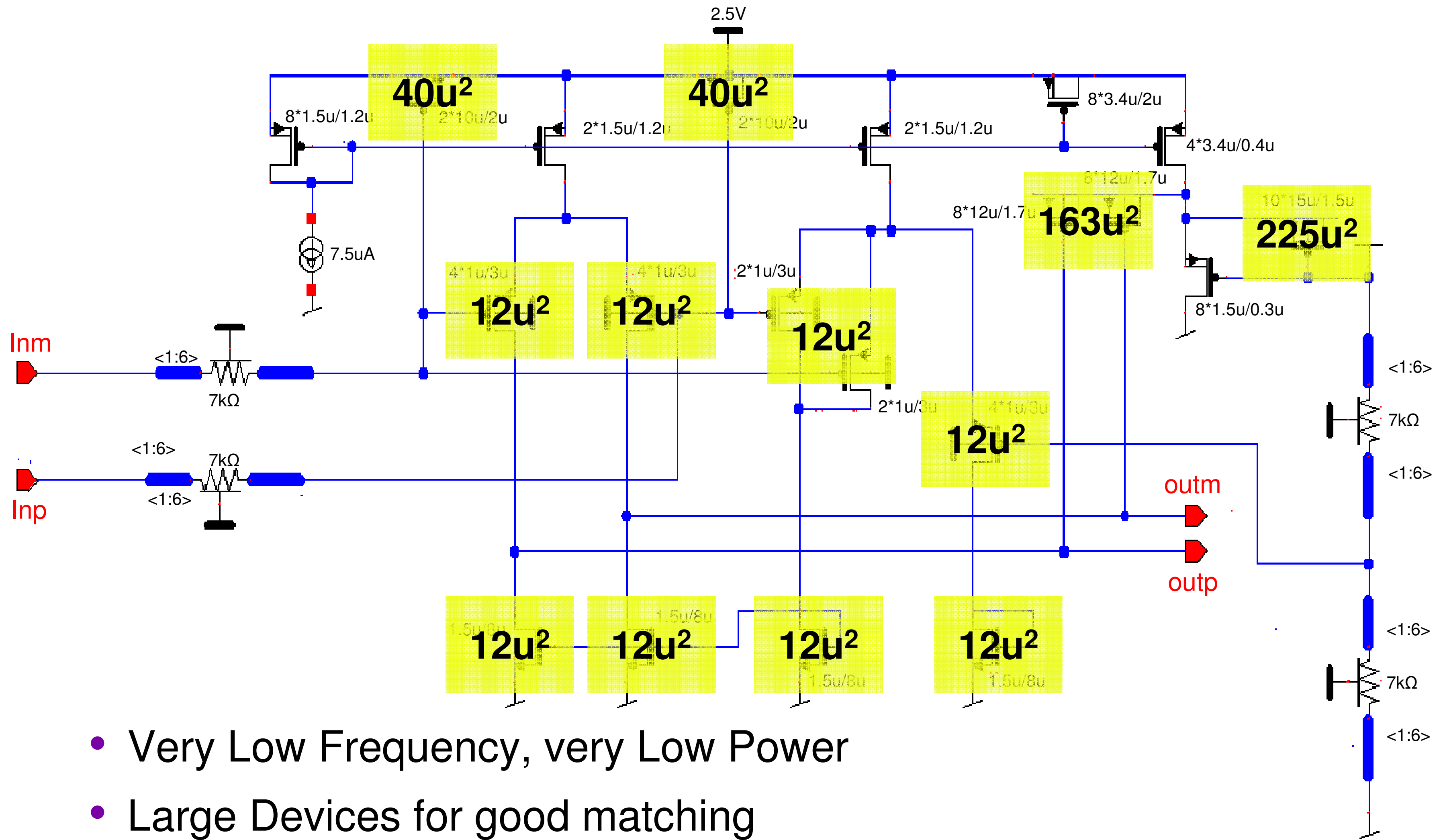
  - 0.5 X 0.065 device → 16%
- Variation in the Op Amp changes the performance of the analog correction






SYNOPSYS® Predictable Success

# DCC Amp Schematic



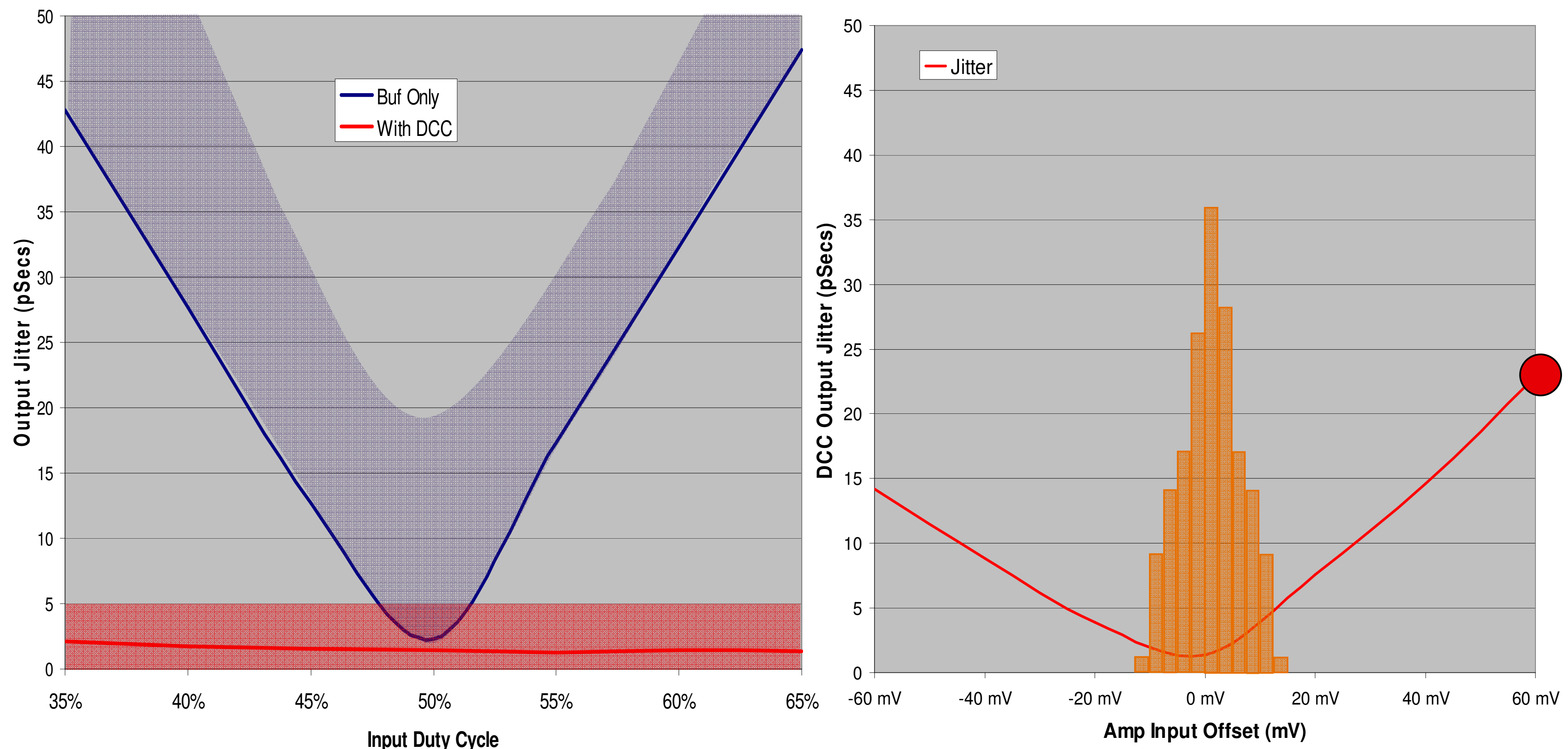

- Very Low Frequency, very Low Power
- Large Devices for good matching



SYNOPSYS® Predictable Success

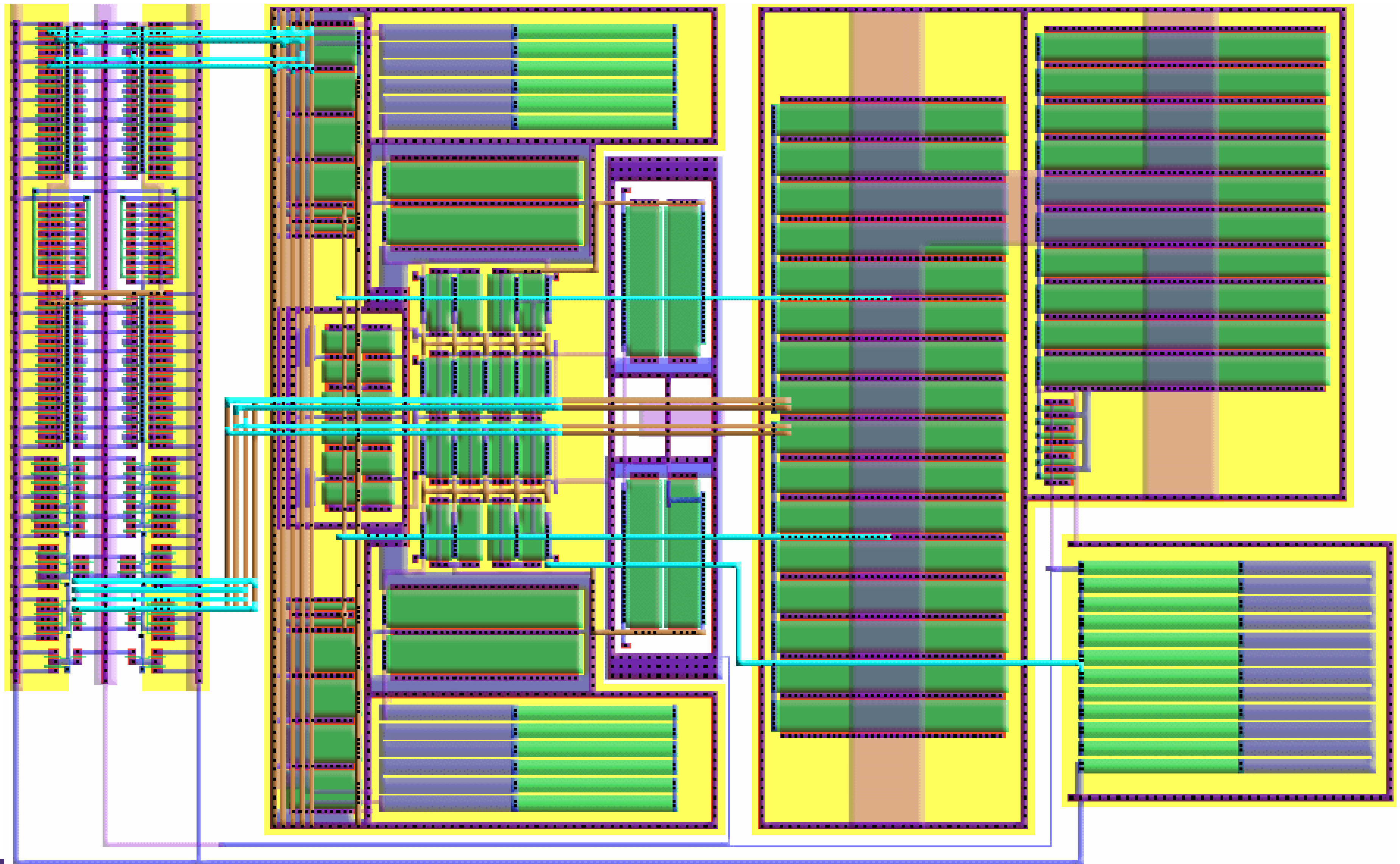
# Analog Functionality Depends on Device Matching

- Monte Carlo Simulations are mandatory in analog design
- **Systematic Offsets can Kill an Analog Circuit**



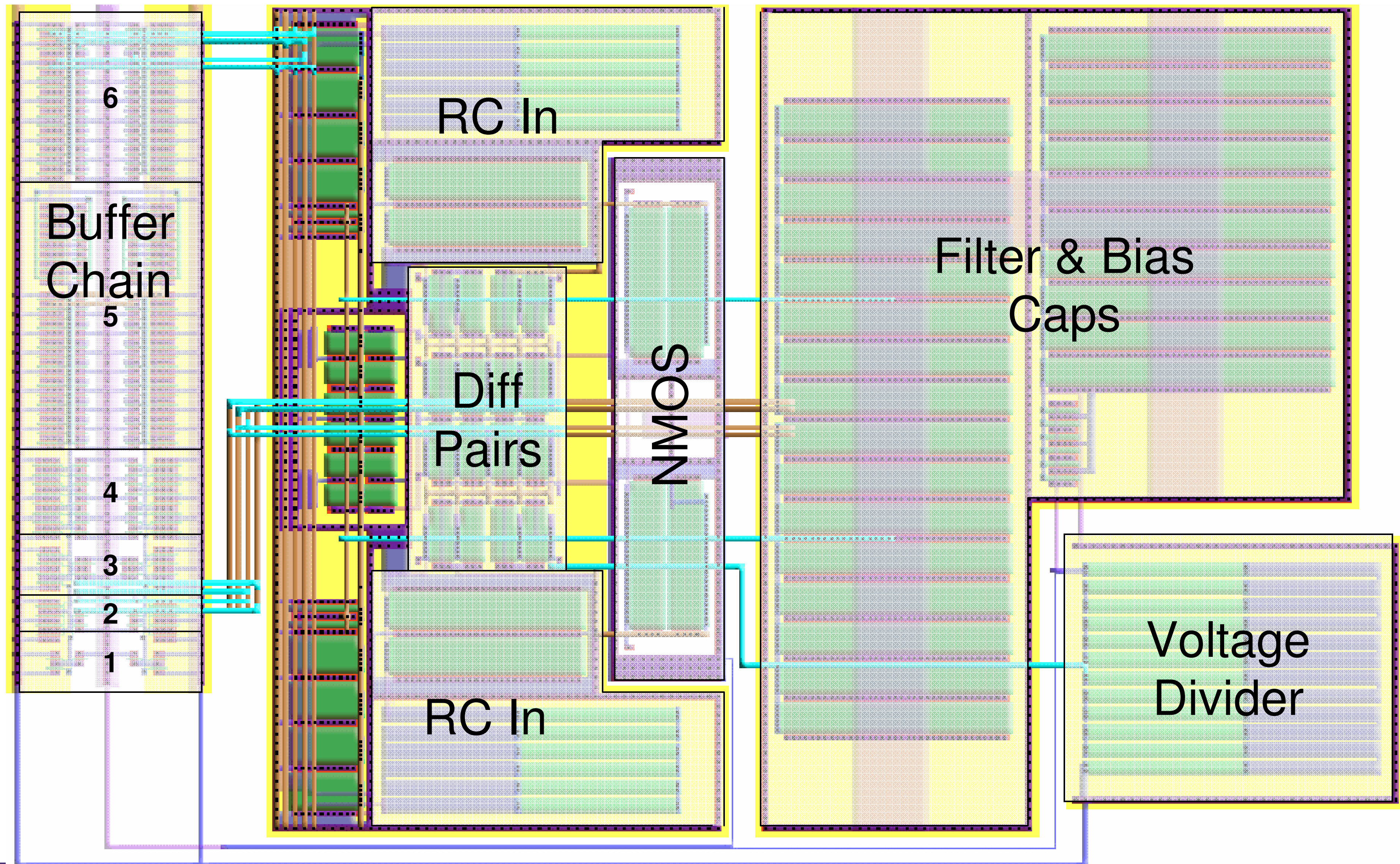

© 2006 Synopsys, Inc. (22)

# DCC Amp Layout @ 65nm



© 2006 Synopsys, Inc. (23)

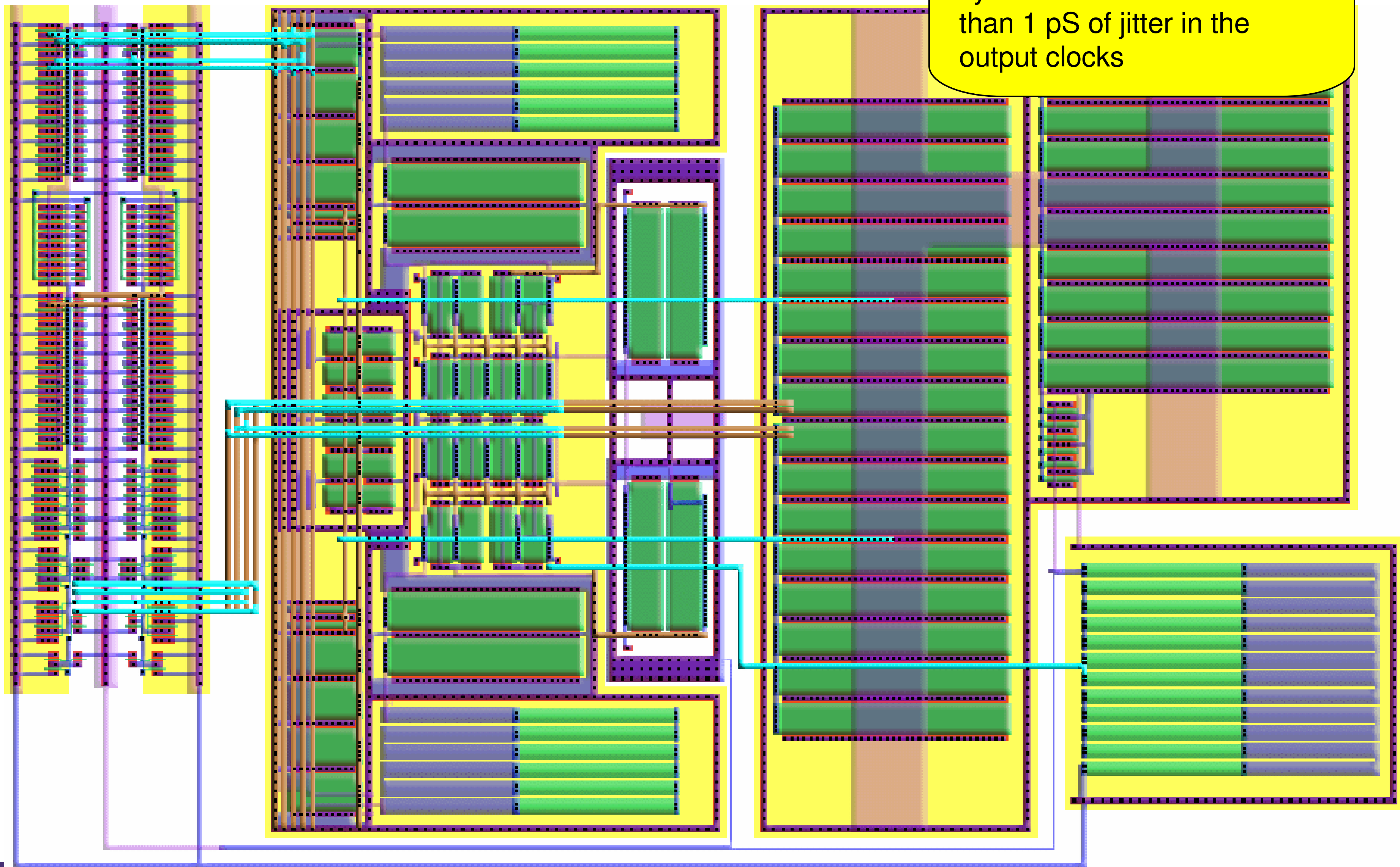
# DCC Amp Layout




© 2006 Synopsys, Inc. (24)

SYNOPSYS®
Predictable Success

# DCC Amp Layout – Good

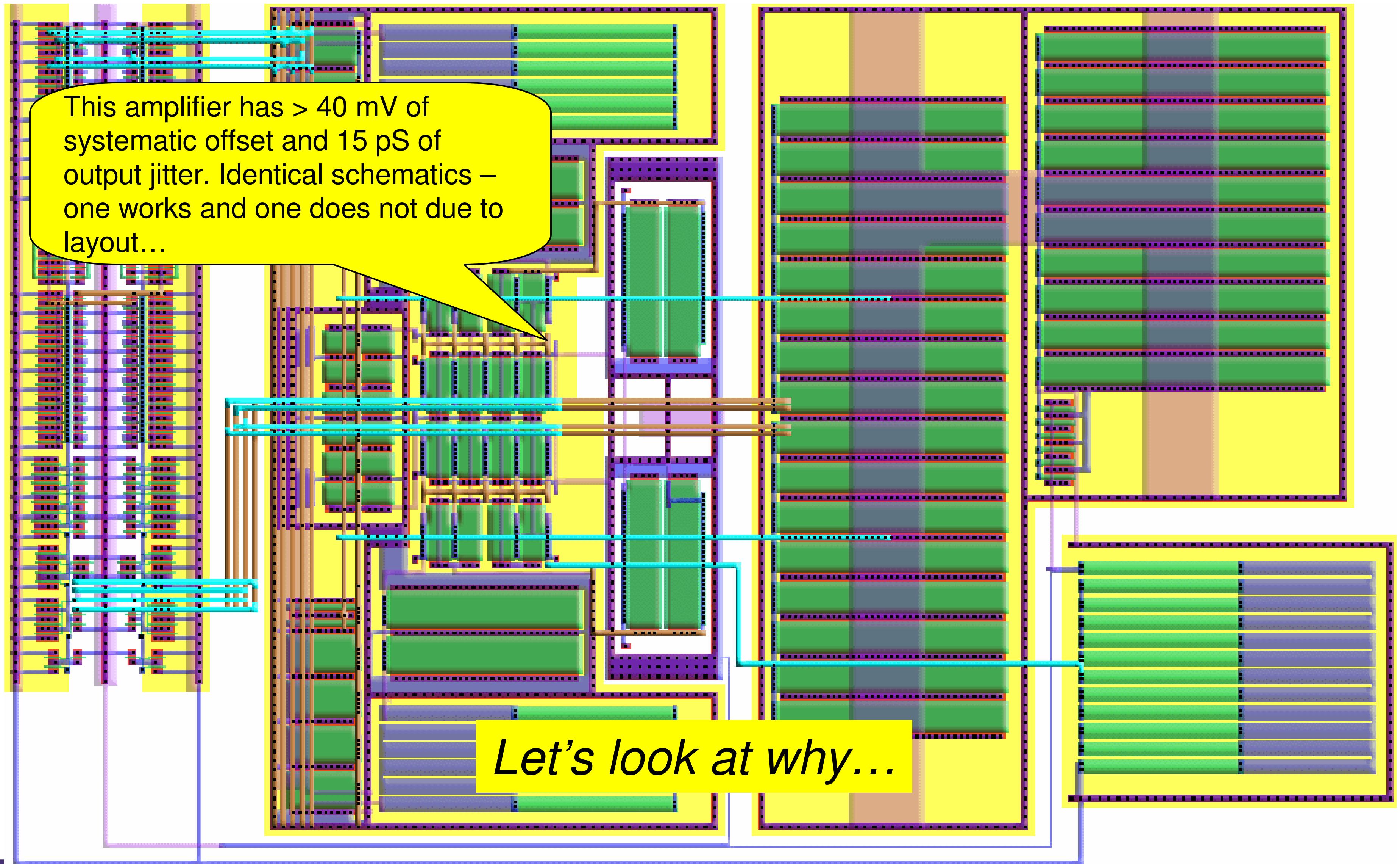


This amplifier has <1 mV of systematic offset and far less than 1 pS of jitter in the output clocks



SYNOPSYS®
Predictable Success

# DCC Amp Layout – BUSTED!






SYNOPSYS®
Predictable Success

# Outline

- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary



SYNOPSYS®
Predictable Success

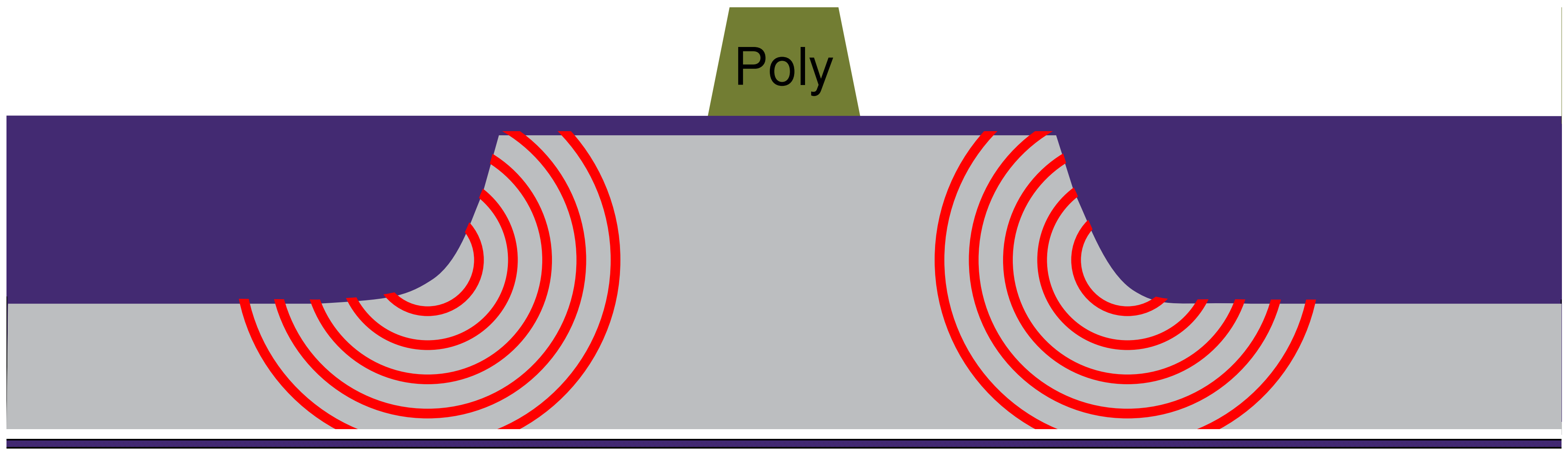
# Killer Sources of Variation

- Variation due to device size is well understood...
  - Monte Carlo simulations of Vt & Idsat miss-match
- Systematic Variation based on Physical Changes to the device
  - STI Stress
  - Well Proximity
  - Contact Stress
  - OPC/PSM Variations
- Time Dependent Variation
  - NBTI
  - HCI

We are operating in a regime well beyond what would have been described as already broken 10 yrs ago!

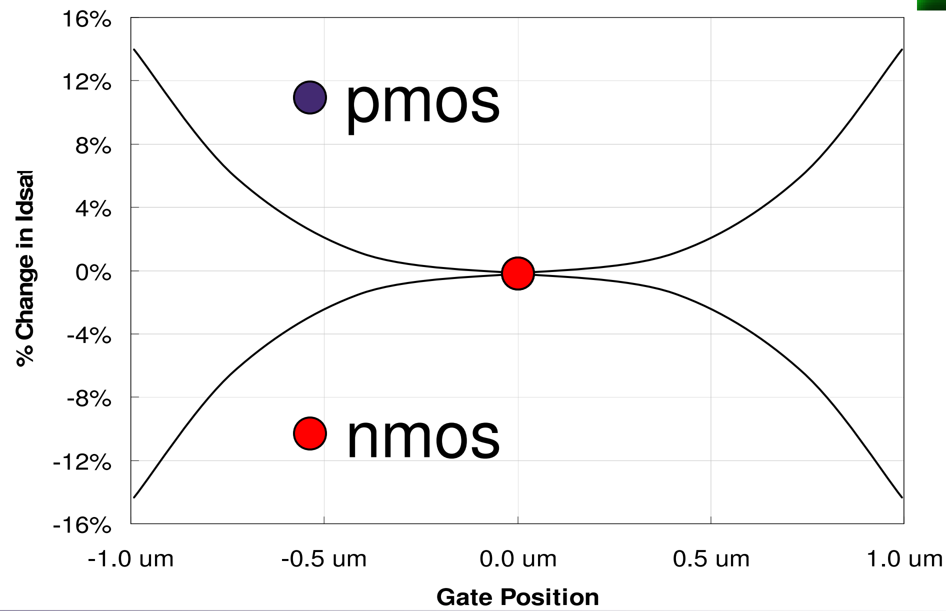
© 2006 Synopsys, Inc. (28)

# Stress due to Shallow Trench Isolation (Modulates Mobility)




© 2006 Synopsys, Inc. (8)

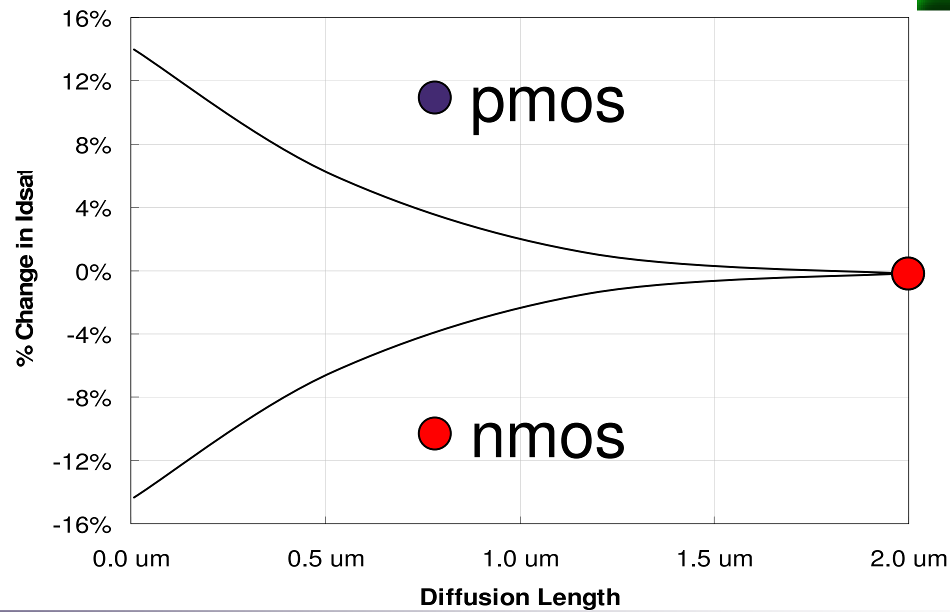
# STI Stress





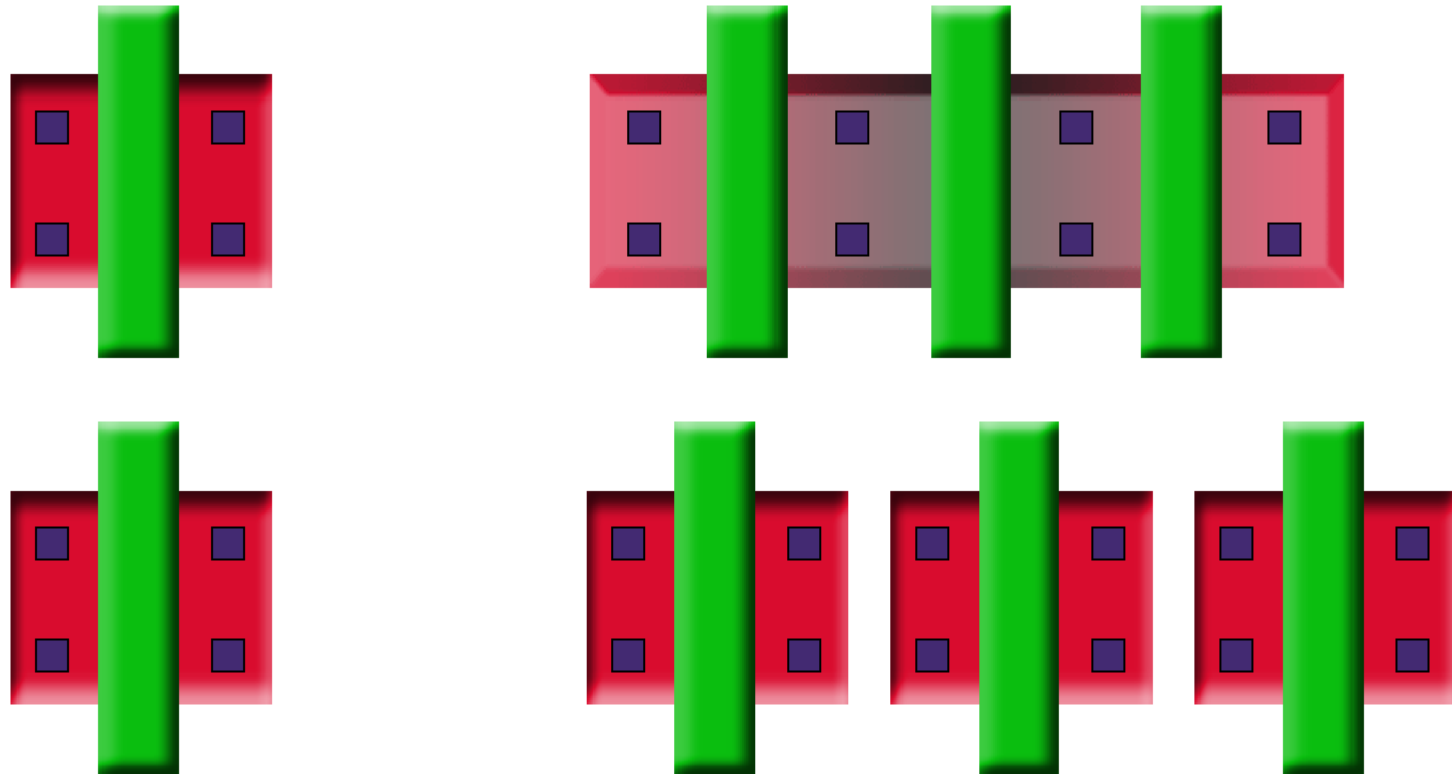

SYNOPSYS®
Predictable Success

# STI Stress




© 2006 Synopsys, Inc. (31)

# Device Matching and Current Scaling

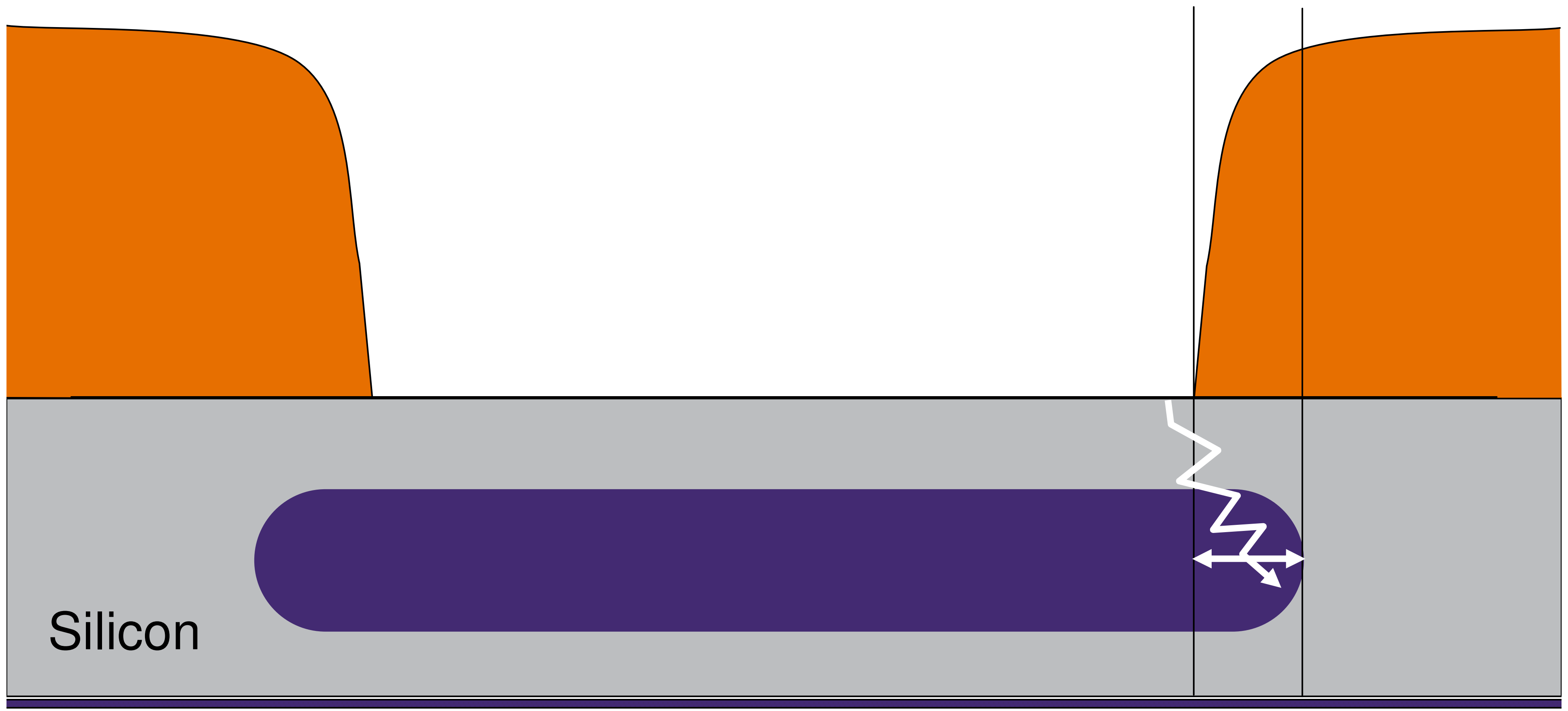


- Every Poly Leg of a multi-fingered device becomes a separate SPICE model to account for placement inside the diffusion
- Current scaling errors of up to 60mV & 25% are possible due to STI



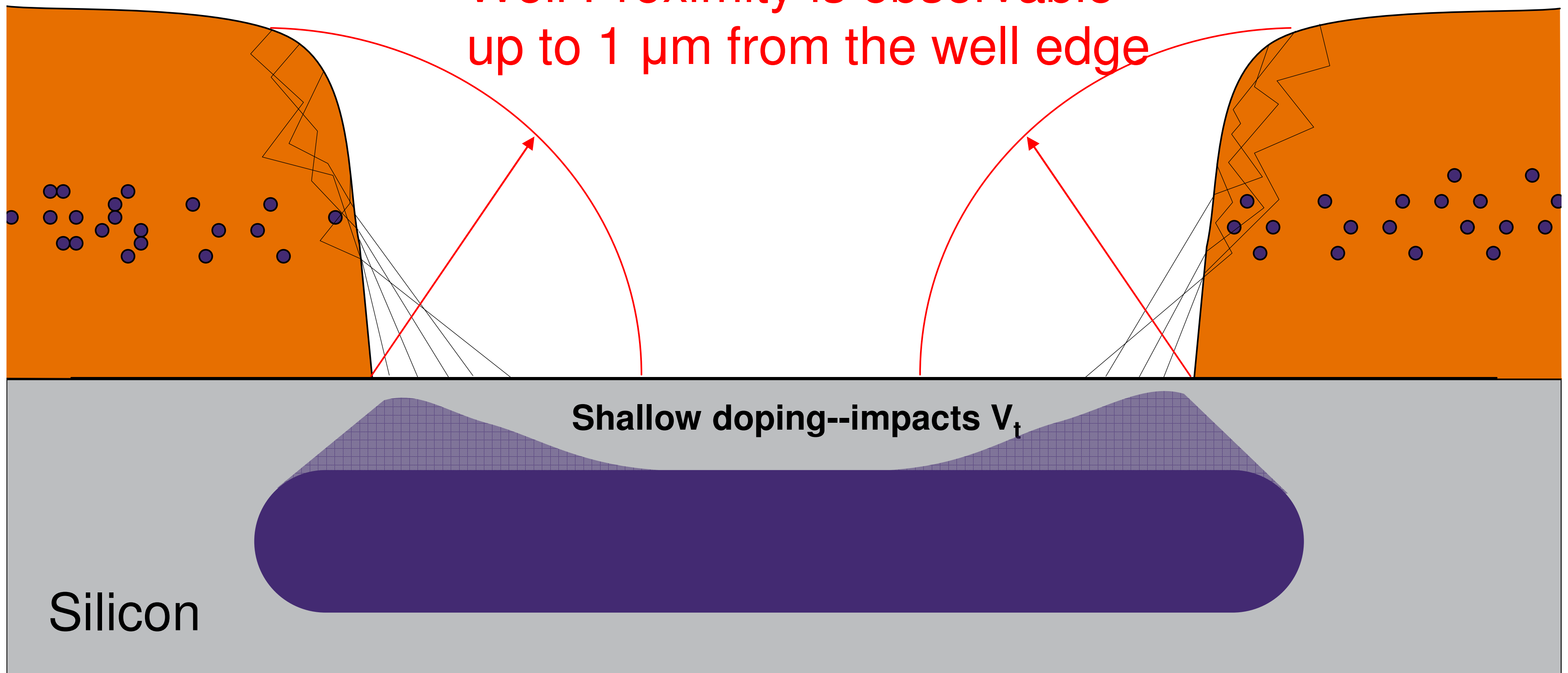
SYNOPSYS® Predictable Success

# Ion Implantation : High Energy Well Implants Miss-Match due to Well Proximity




© 2006 Synopsys, Inc. (8)

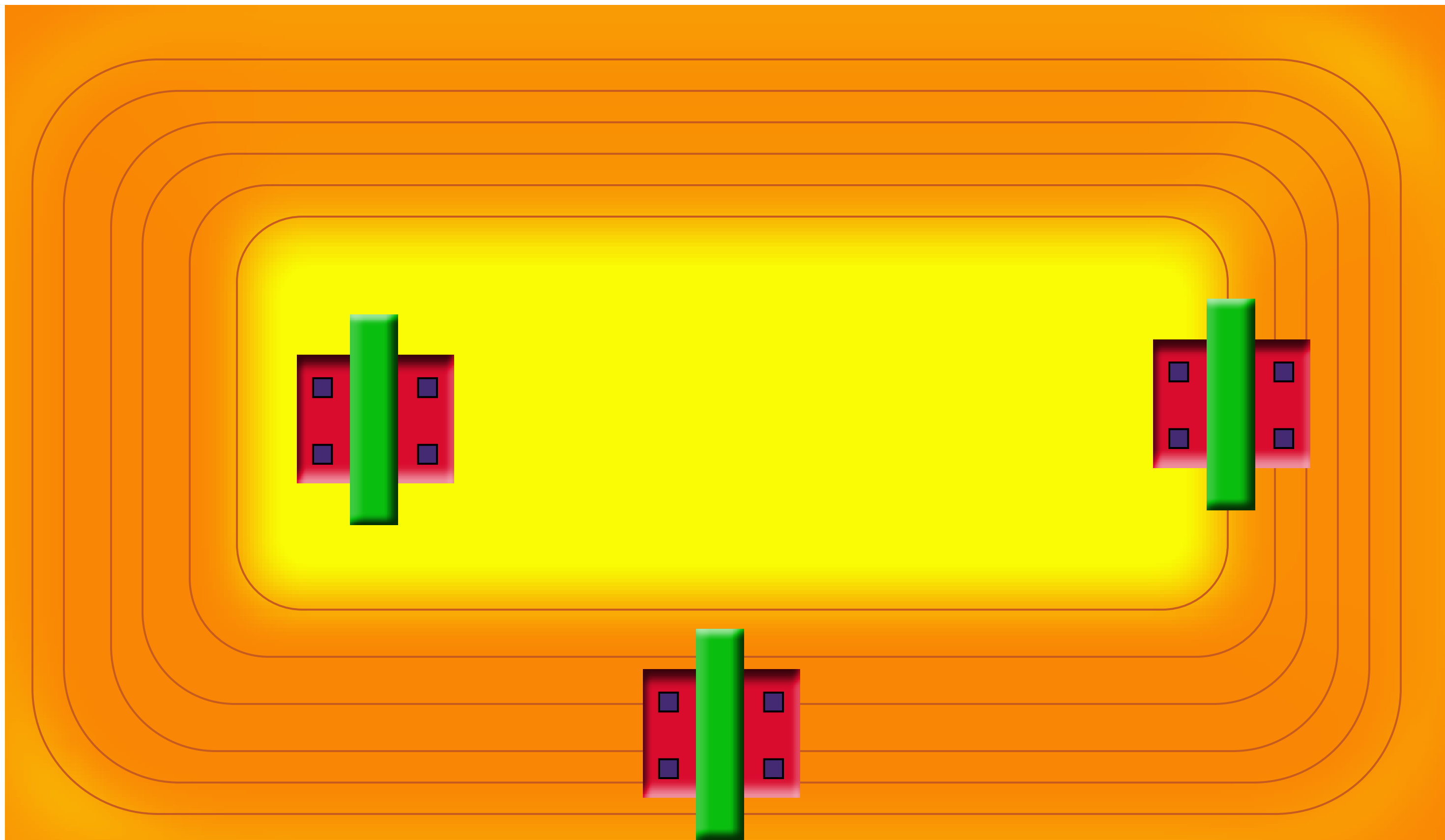
# Ion Implantation: High Energy Well Implants Miss-Match due to Well Proximity




© 2006 Synopsys, Inc. (34)

# Well Proximity

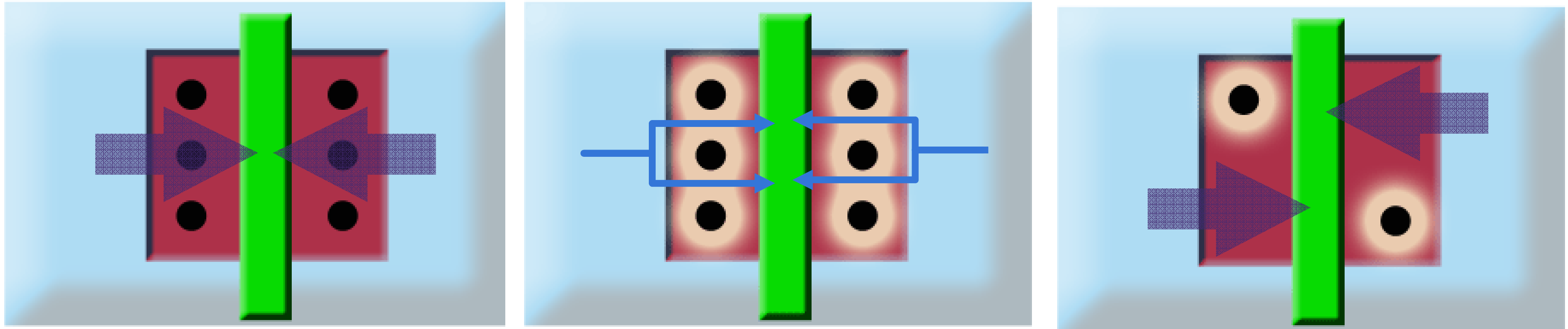
- 100 mV Threshold shift based on placement in a well
- Occurs for both N-Well and P-Well implants





SYNOPSYS® Predictable Success

# Contact Stress

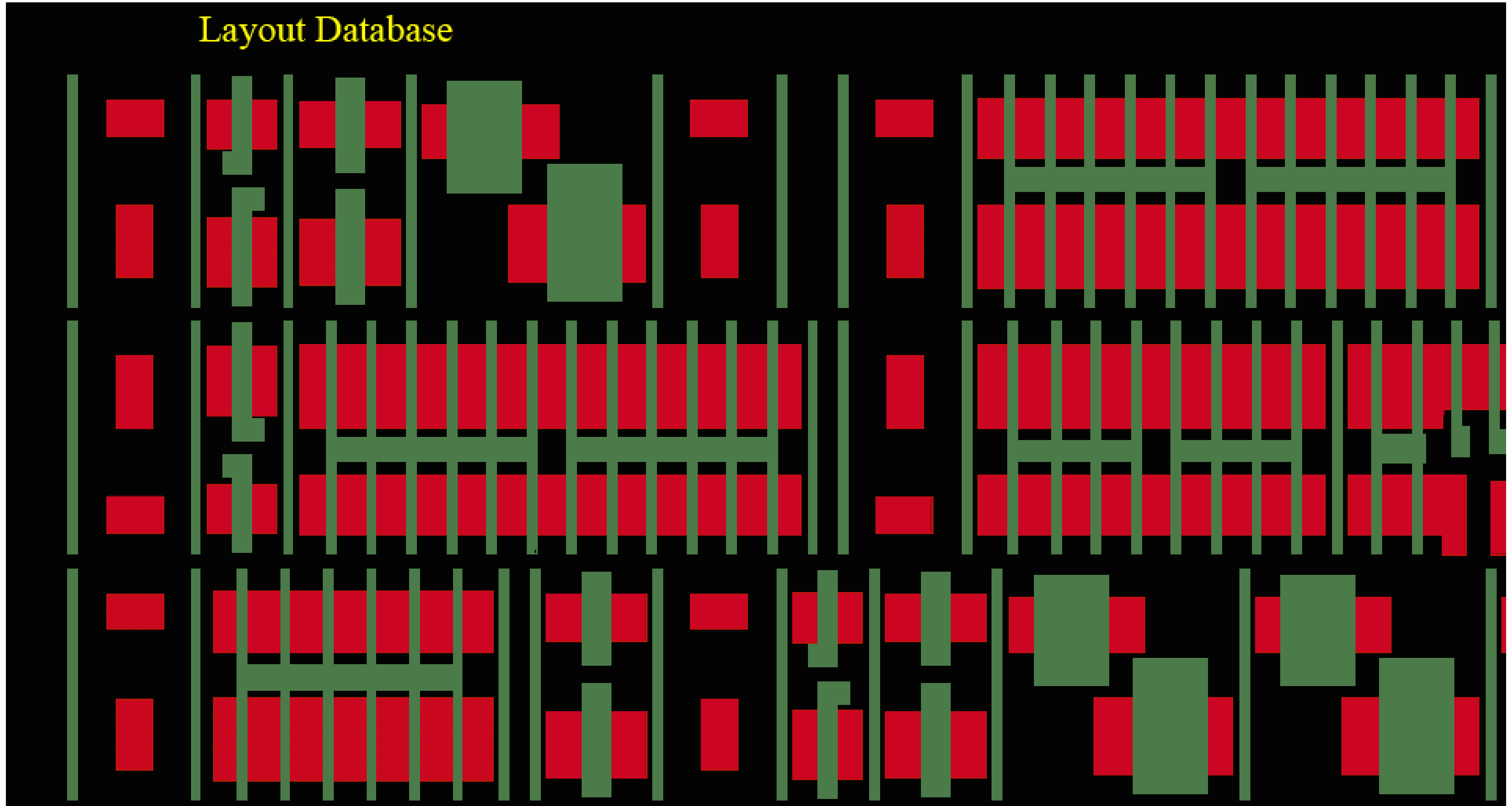


- If STI stress can change mobility – lets feature it
  - Add stress layers to increase device performance
  - Different stress for N & P Channel
- But contacts cut the stress layer & reduce the improvement
  - Device “On Current” becomes a function of contact density

© 2006 Synopsys, Inc. 

SYNOPSYS®
Predictable Success

# 65nm : Poly OPC/PSM Masks






SYNOPSYS®
Predictable Success

# Time Dependent Variation: NBTI

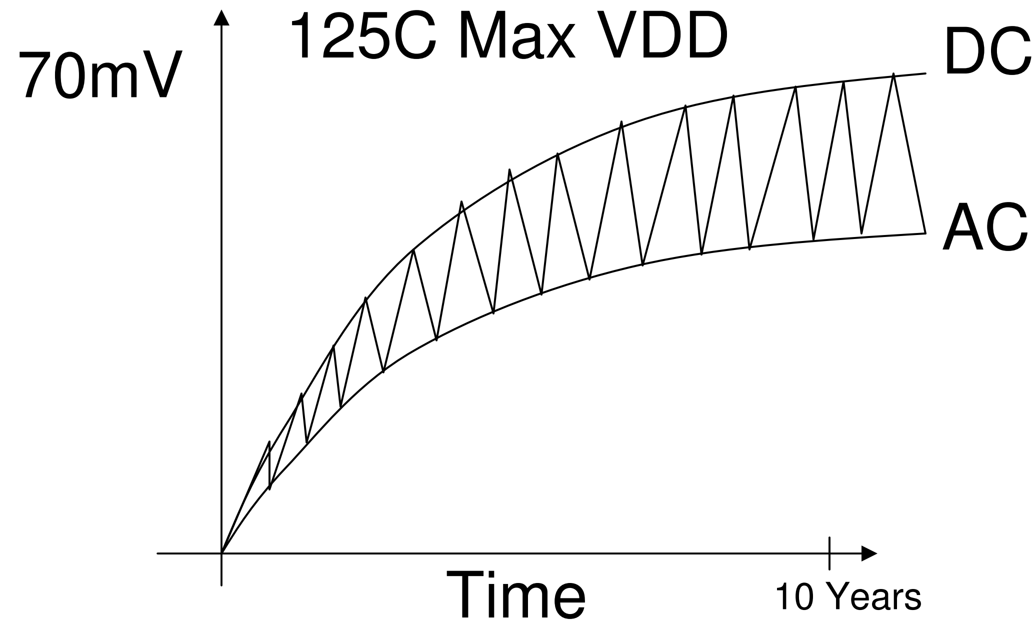
- PMOS devices that are "ON" have large gate field and high hole surface density
- This causes a molecular change in the gate oxide!
  - Hydrogen disassociates from the interface and diffuses away CHANGING the threshold Voltage
- If the voltage is removed, the hydrogen diffuses back!

Poly
VSS
Gate
H H H H H H H H H H H H H
Silicon
VDD

© 2006 Synopsys, Inc. (38)

SYNOPSYS®
Predictable Success

# Threshold Voltage vs. Time



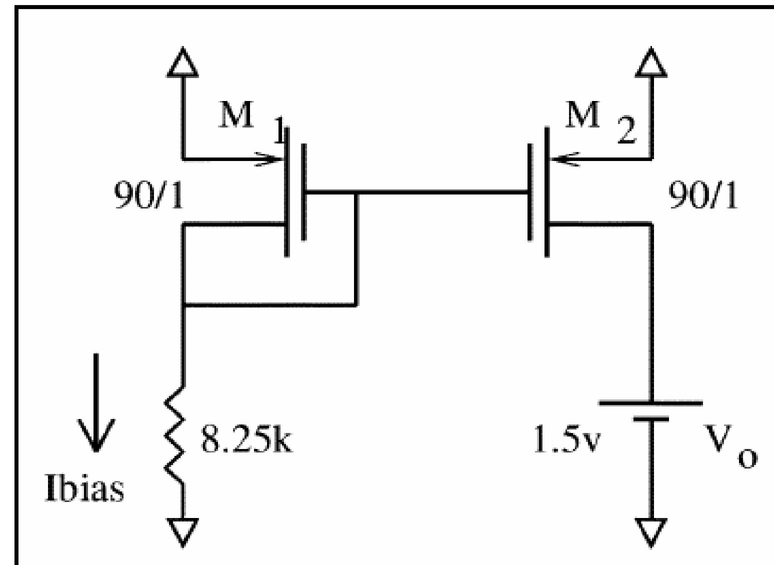

- NBTI has dramatic impact when matched PMOS devices do not have the same gate bias
  - This shows up more in power-down modes than in normal operation
- NBTI can be simulated using Verilog-A if you are clever
- Commercially available simulation capability will be released soon



SYNOPSYS®
Predictable Success

# NBTI Impact on Current Mirror (1)

- Simple mirror
- Used where high output resistance not needed
- As M1 and M2 undergo identical gate stress voltage, delta Vt will vary identically for both of them. The output current follows the bias current for the range considered
- The variation in gate-to-source voltage for transistors M1 and M2 causes a further increase in stress voltages, which therefore must be taken into account for lifetime prediction

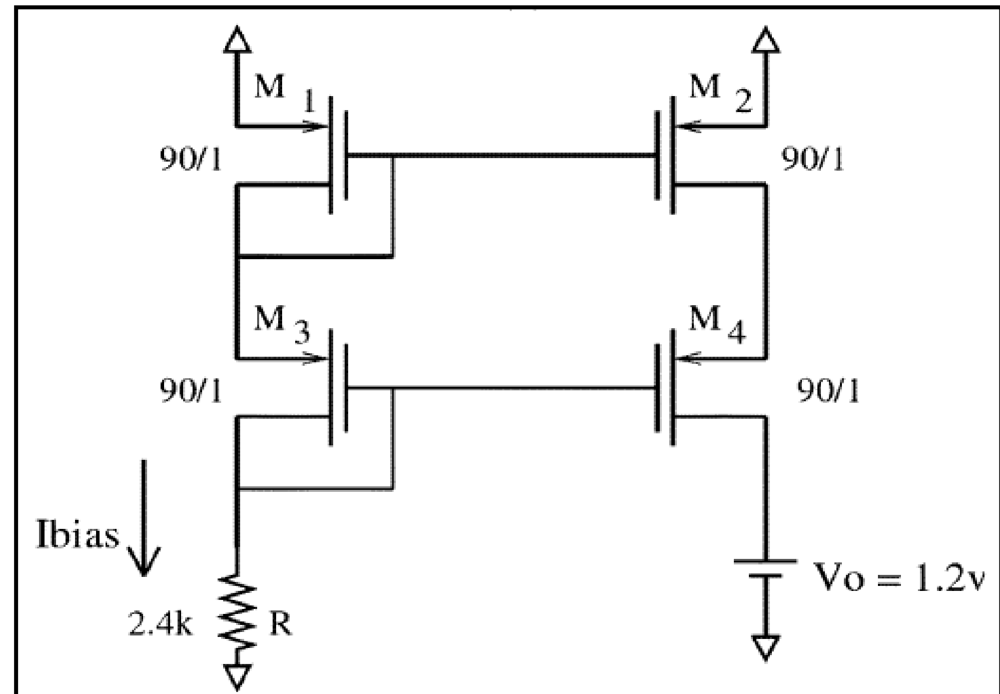





SYNOPSYS®
Predictable Success

# NBTI Impact on Current Mirror (2)

- Cascode current mirror
- Higher output impedance

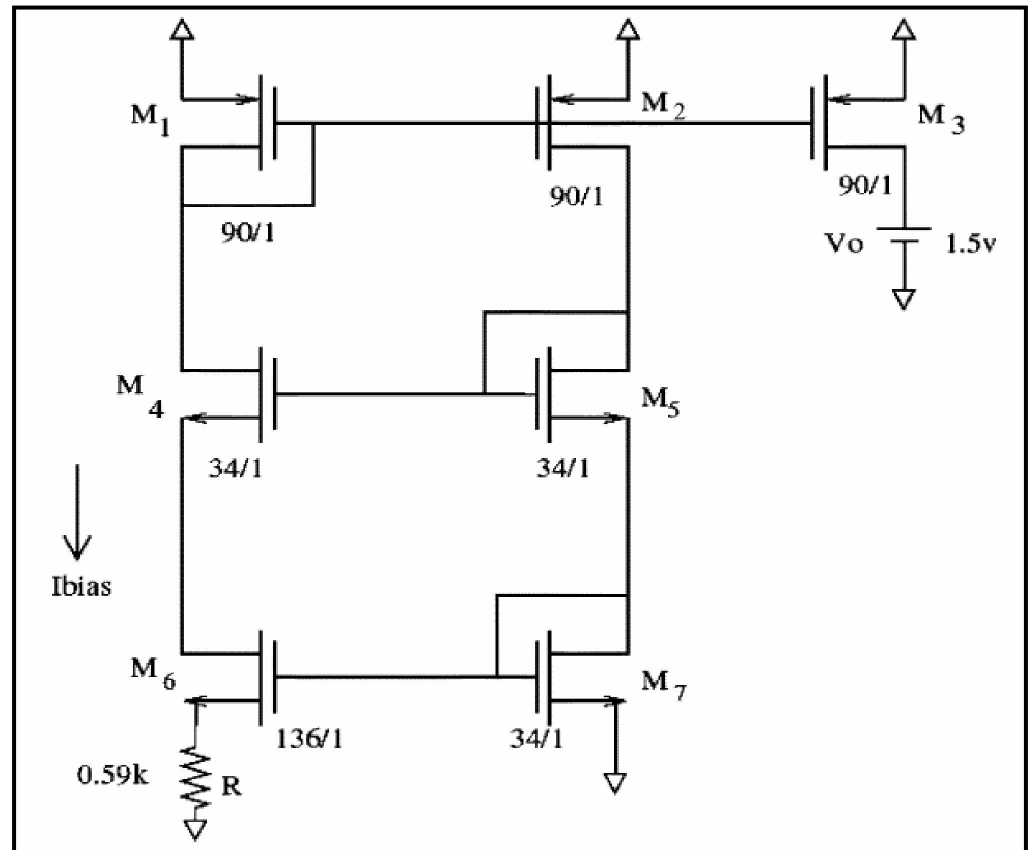





SYNOPSYS®
Predictable Success

# NBTI Impact on Current Mirror (3)

- Constant biasing (gm) circuit
- Applications where stable transconductances are required
- Positive feedback is always maintained to match all the gm's to the conductance of R
- Because of this reason, as long as R is constant, the bias currents are maintained at a constant value irrespective of PVT variations

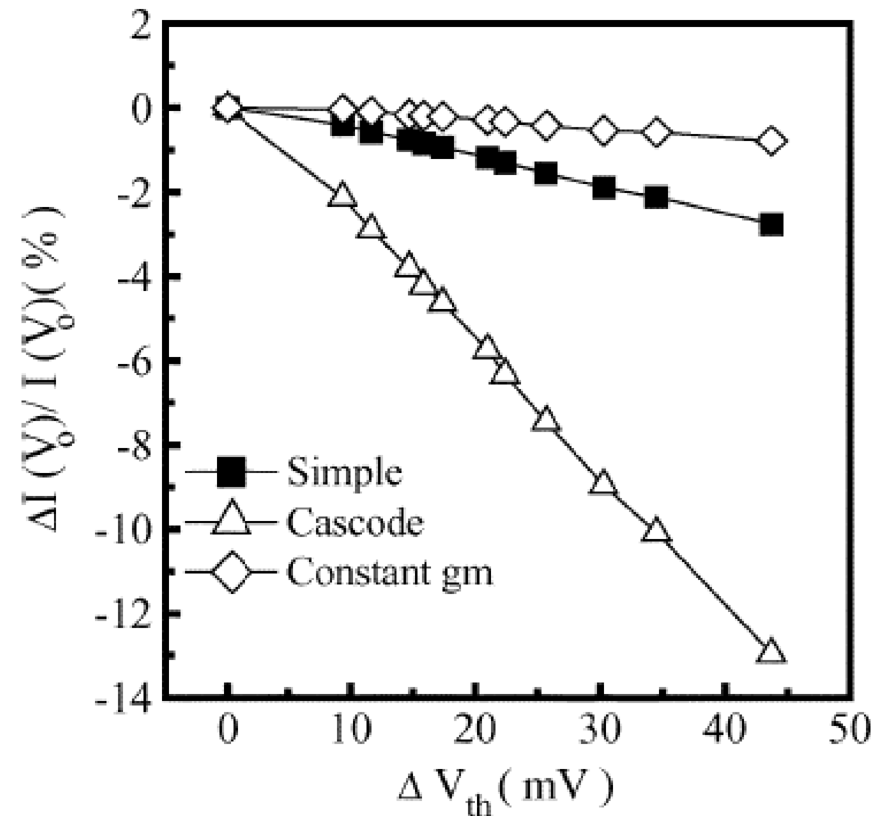





SYNOPSYS®
Predictable Success

# Drift Current For Equal NBTI Induced $\Delta V_{th}$ Degradation

- Cascode current mirror shows the maximum drift ( 12.5%) in the output current for the same amount of NBTI-induced degradation
- Constant biasing mirror shows the least degradation ( 1%)
- The highest degradation in the cascode current mirror because there are two diode connected transistors in series and hence the change in voltage across the biasing resistor is a result of change in the Vth's of M1, M3
- The least degradation observed in the constant gm biasing circuits a result of the positive feedback, which accounts for NBTI variation




"NBTI Degradation and Its Impact for Analog Circuit Reliability", Jha et al IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, NO. 12, DECEMBER 2005



SYNOPSYS®
Predictable Success

# Current Mirror Summary

- Therefore it is clear that for the same amount of variation due to NBTI, different current mirror configurations behave differently and hence must be chosen depending on the application



SYNOPSYS®
Predictable Success

# Outline

- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary



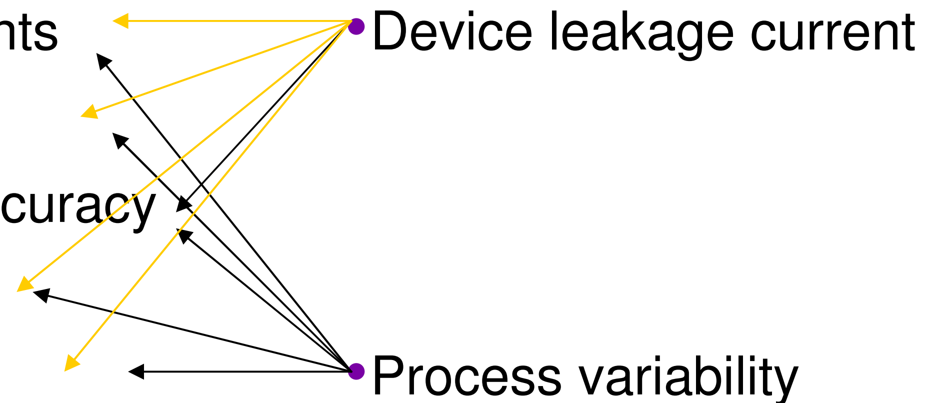
SYNOPSYS®
Predictable Success

# Trends: Fab/Design/EDA Cooperation

Circuit designers view

- Power dissipation constraints
- Analog design challenges
- Device variability/model accuracy
- Design methodology/tools
- Reliability

Process technologist's view




At ≤ 65 nm fab engineers need to work together with designers and EDA vendor to address power dissipation and process variability concerns



SYNOPSYS® Predictable Success

# Analog design trends @ 65 nm

- SPICE model complexity
- Layout re-use
- Dual oxide partitioning
- On-chip voltage regulators
- On-chip RF components
  - Inductors
  - Special Processing

Cost



SYNOPSYS® Predictable Success

# Compact Device Models

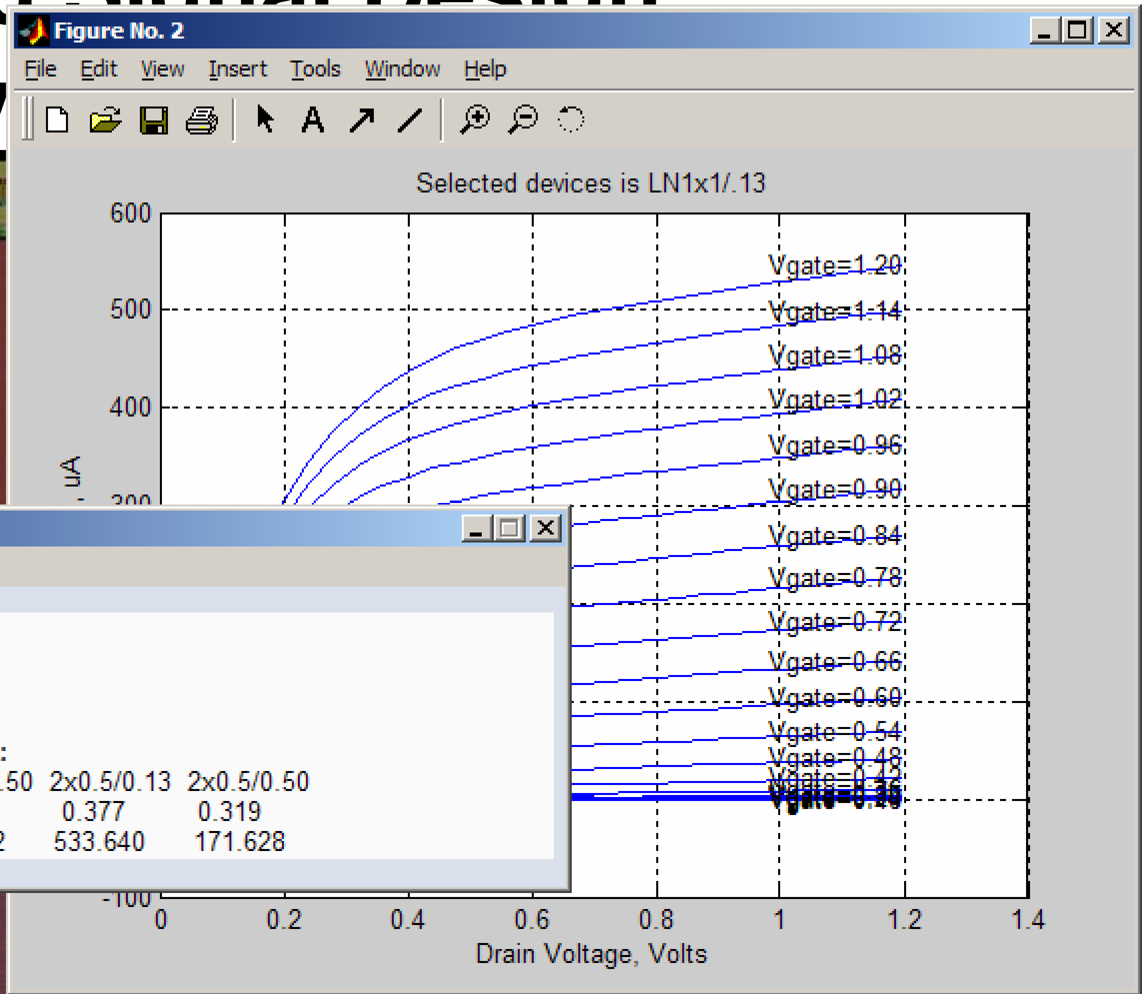
- BSIM continues to be used
- Modern models formulated as a function of surface potential, rather than threshold voltage, in the channel and s/d edges
- Compact models at 65 nm require:
  - Scalability of sub-threshold currents and output resistance from short to long channels due to lateral doping non-uniformities
  - Dependence



SYNOPSYS®
Predictable Success

# Analog/Mixed Signal Design Methodology

- **Archite**
  - Sim mar
- **Simula**




Measurement Results

File

**Nch Thinox (1V) Transistor Measurements**

Leff is longer than drawn by -0.026 microns.
Weff is wider than drawn by 0.022 microns.
Mobility * Cox product is 277.61 uA/square.

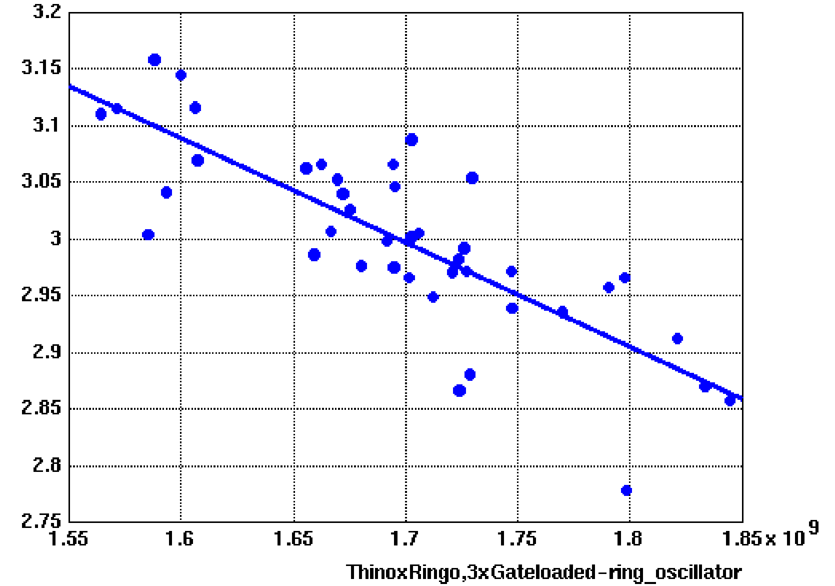
**Individual Transistor Measurements, sized at:**

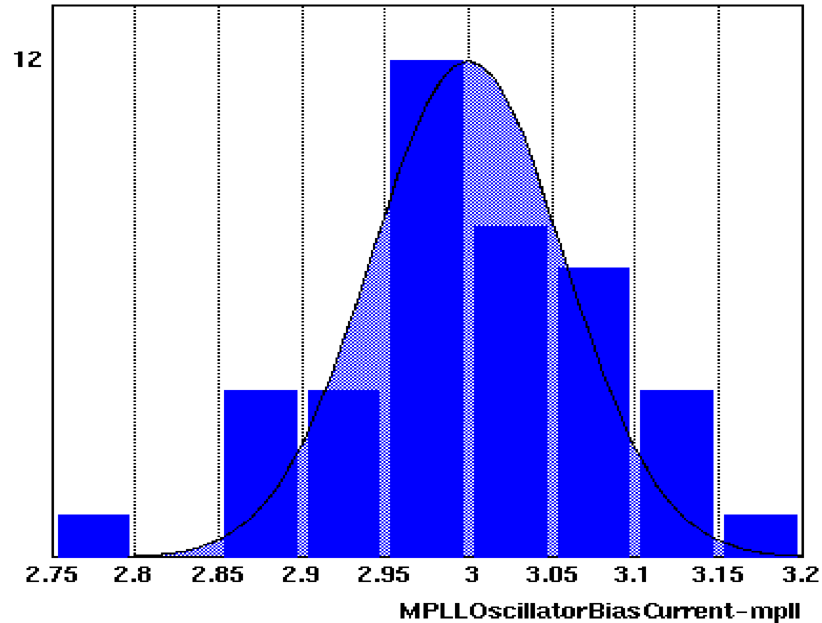
| | 1x1.0/0.13 | 1x1.0/0.50 | 2x0.5/0.13 | 2x0.5/0.50 |
|---|---|---|---|---|
| Vthreshold, Volts : | 0.392 | 0.333 | 0.377 | 0.319 |
| Idsat, uA/micron_width: | 535.536 | 162.052 | 533.640 | 171.628 |

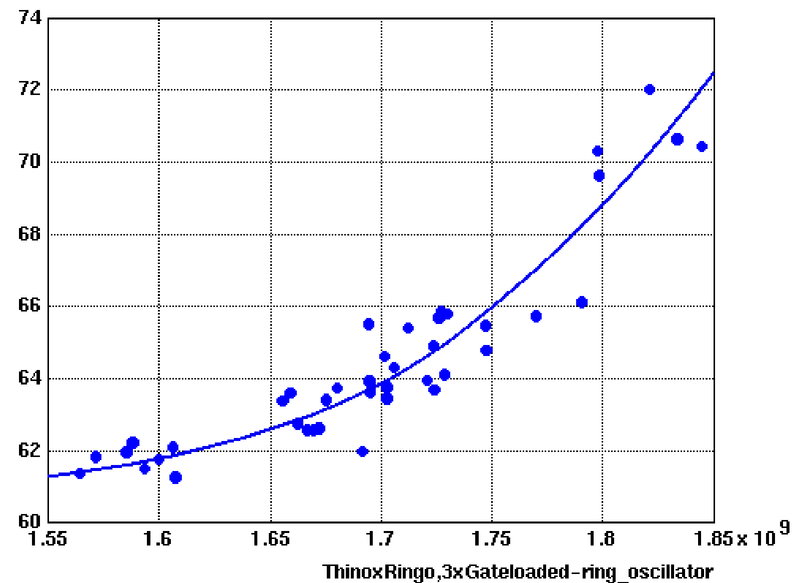
© 2006 Synopsys, Inc. (49)

# Analog Test-Bus

- Visibility into critical analog circuits - methodology allows analog voltages and currents to be measured



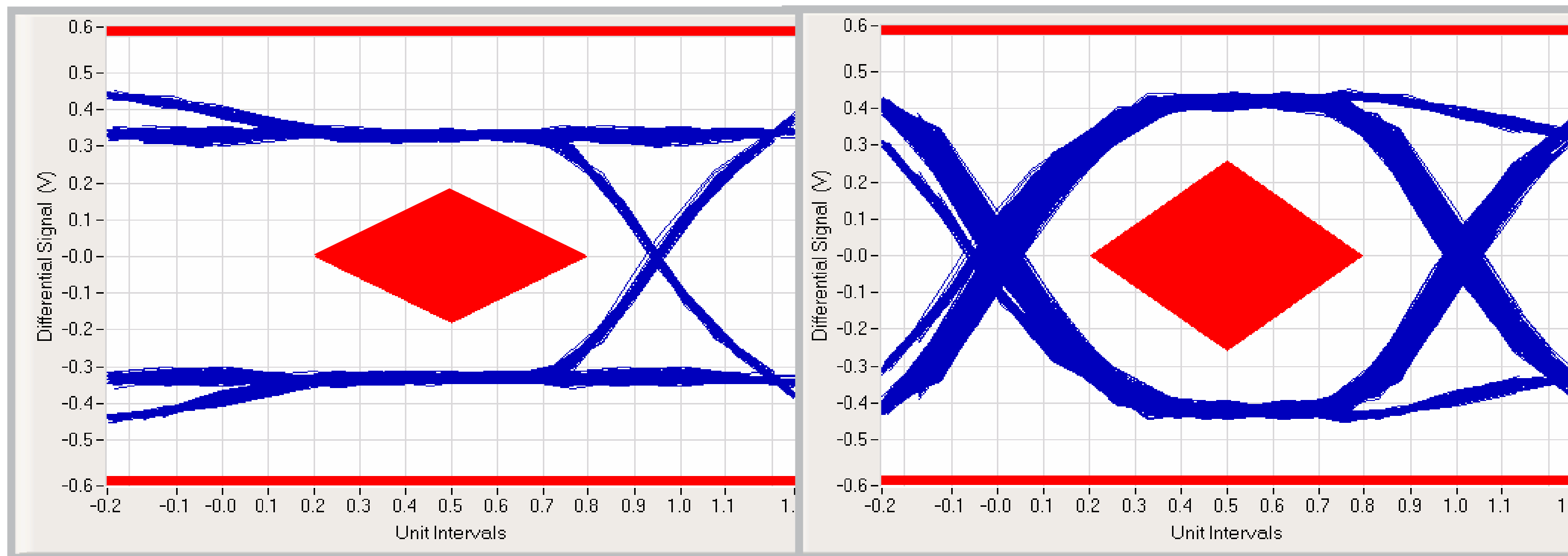



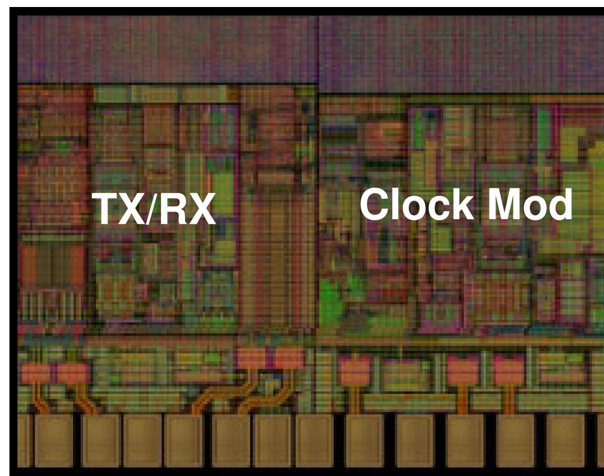

© 2006 Synopsys, Inc. (50)

# Outline

- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary

# Example: Low Jitter PCI Express® PHY




Dedicated x1 configuration

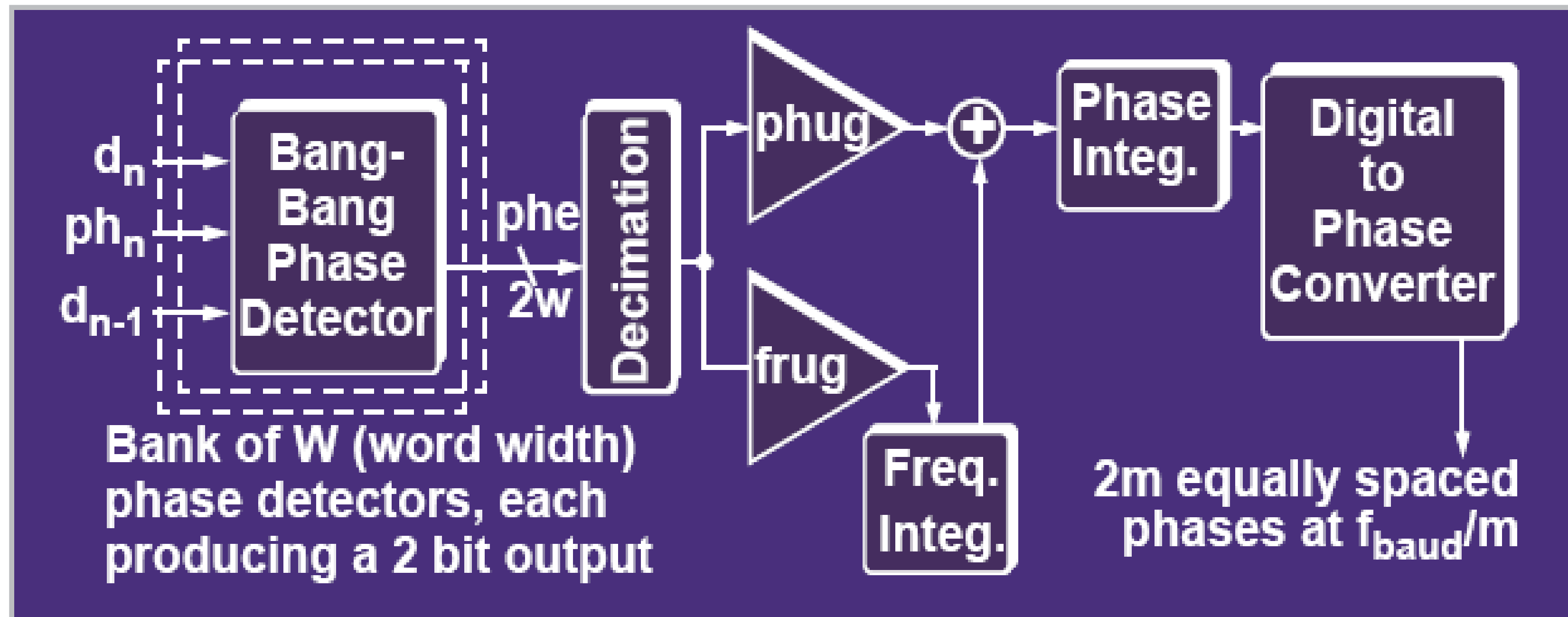
© 2006 Synopsys, Inc. (52)

# High Performance PHY @ 65 nm…

- PSRR, Jitter
- Robustness
- Power
- Testability
- PVT invariance

**→ Need *digital* CDR**

# Example PCIe PHY: Digital CDR




*"A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links"*,
**Jeff Sonntag and John Stonick Synopsys, Inc. CICC 2005**



SYNOPSYS® Predictable Success

# Advantages Of Digital CDR

- PSRR, Jitter
  - Digital components
    - No PSRR
    - Jitter controlled by design resolution
  - Only analog component is DPC
    - May include high b/w PLL, always tracking reference clock
    - Tracking reference clock allows use of linear PFD and about 10 times the b/w of the CDR
    - High b/w effective at correcting power supply injected errors and thermally generated jitter



SYNOPSYS®
Predictable Success

# Advantages Of Digital CDR, cont.

- Robustness
  - False lock impossible
  - Tolerance of low transition densities
    - CDR is not integrating any noise when there are zero transitions as opposed to an analog CDR when you are always integrating → it is a perfect zero input!
- PVT invariance
  - $K_{DPC}$ is not a function of PVT
  - Analog CDR depends on
    - $K_{VCO}$, R, C
    - Charge pump
      - Current
      - Up/down mismatch
      - leakage



SYNOPSYS®
Predictable Success

# Advantages Of Digital CDR, cont.

- Power
  - In order to achieve similar thermal jitter performance, the analog CDR would require much more power
- Testability
  - Standard digital SCAN techniques
  - Phase programmability can be used for margining purposes in vector-only ATE

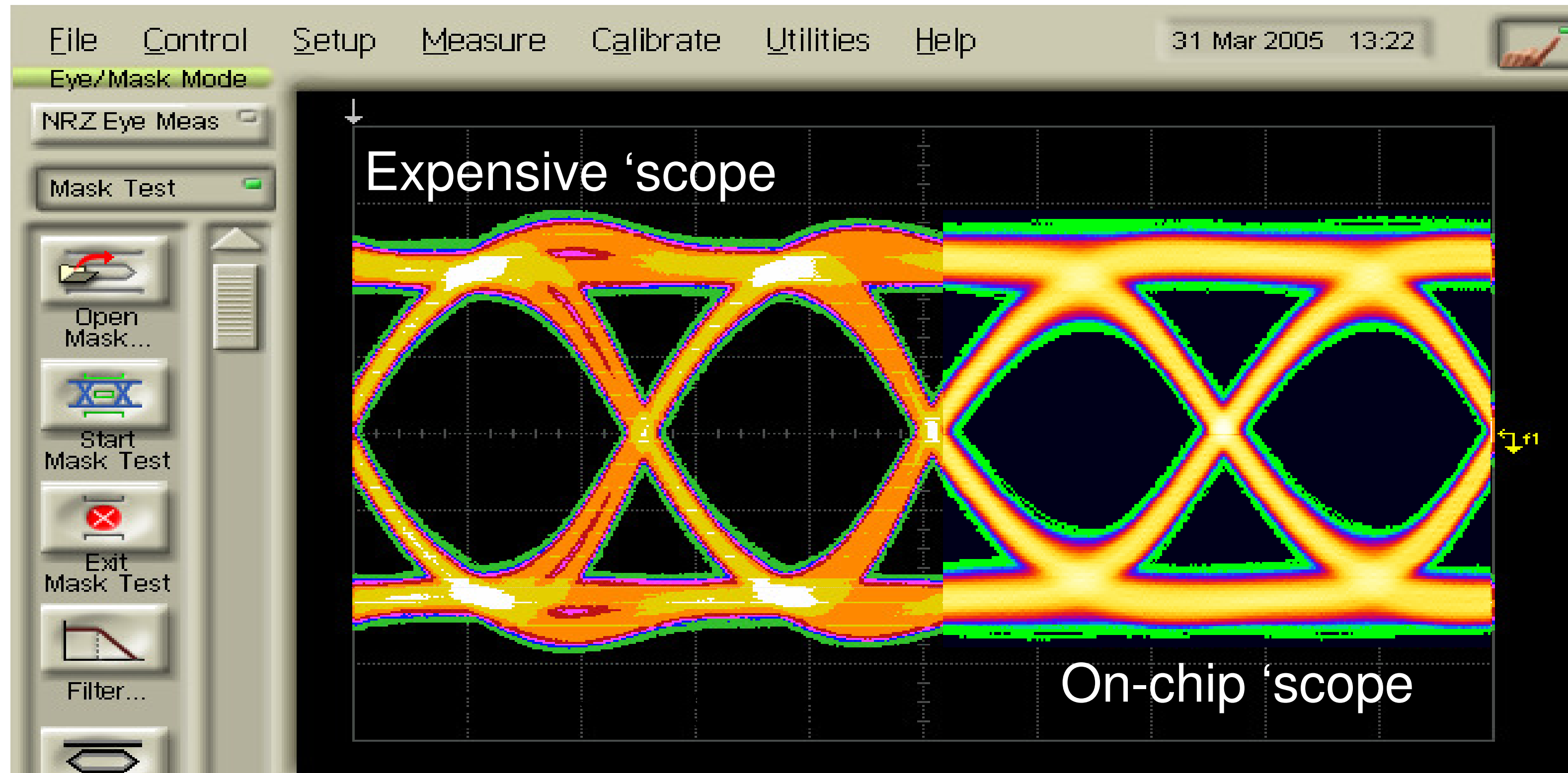


SYNOPSYS®
Predictable Success

# Precision Is Possible

- Example: On-chip, per RX, sampling scope
  - Eye diagrams available through JTAG port
  - Synchronous and asynchronous operation supported
  - Measure channel pulse response, S21 insertion loss
  - Directly measure cross-talk in connectors, layout

# On-Chip Sampling Scope per Lane




- Differences between external scope and internal diagnostics?
  - External Scope sees TX + Channel (16" FR4 + cables)
  - Internal scope sees TX + Channel + Bond Wires in the package
- Internal scope sees the high frequency filtering effects of the bond wires – and the actual RX eye!

© 2006 Synopsys, Inc. (59)

SYNOPSYS® Predictable Success

413 bond wires on 4.5mm test chip

Bond wire layout for low cross-talk
Gnd-Signal-Signal-Gnd

Short wires for Gnd

Quad PCIe PHY

© 2004 Synopsys, Inc. (5)

# Outline

- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary



SYNOPSYS® Predictable Success

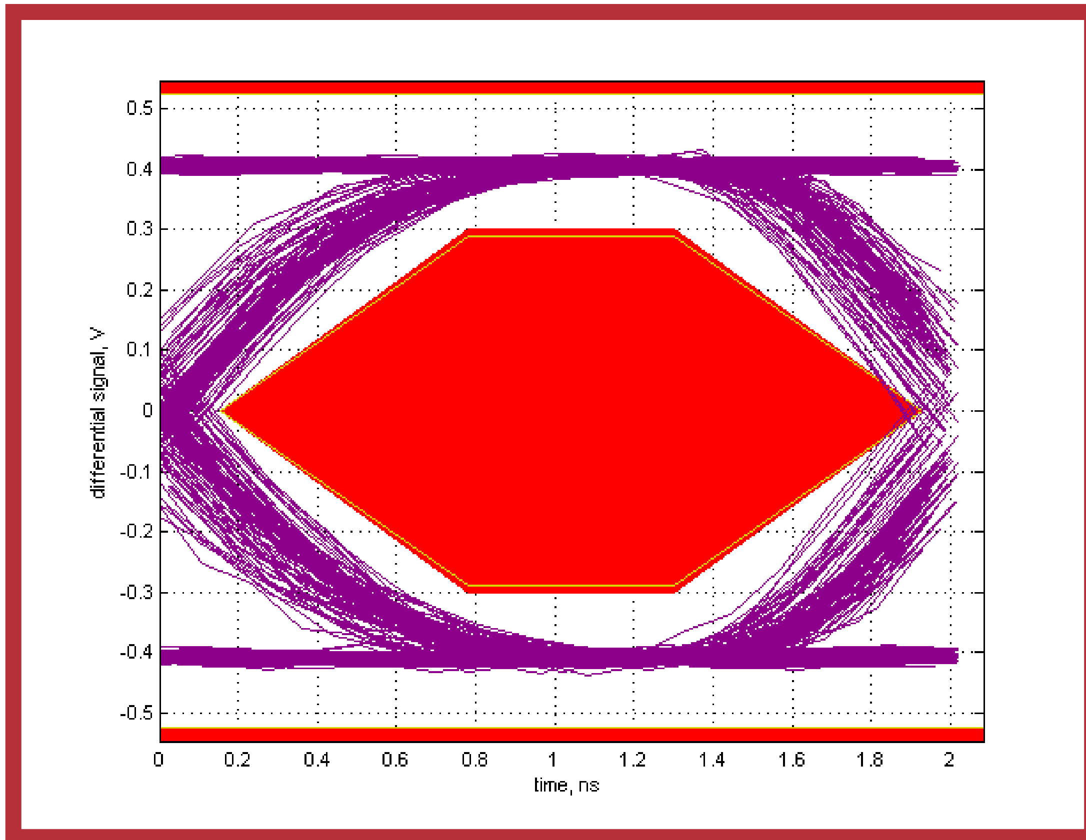
# USB 2.0 PHY "Yield By Design"

- Architecture optimizes parametric yields and minimize current consumption
- User controls many performance parameters to allow for various packages, systems and customization

© 2006 Synopsys, Inc. 

SYNOPSYS®
Predictable Success

# USB 2.0 Compliance – Eye Diagram



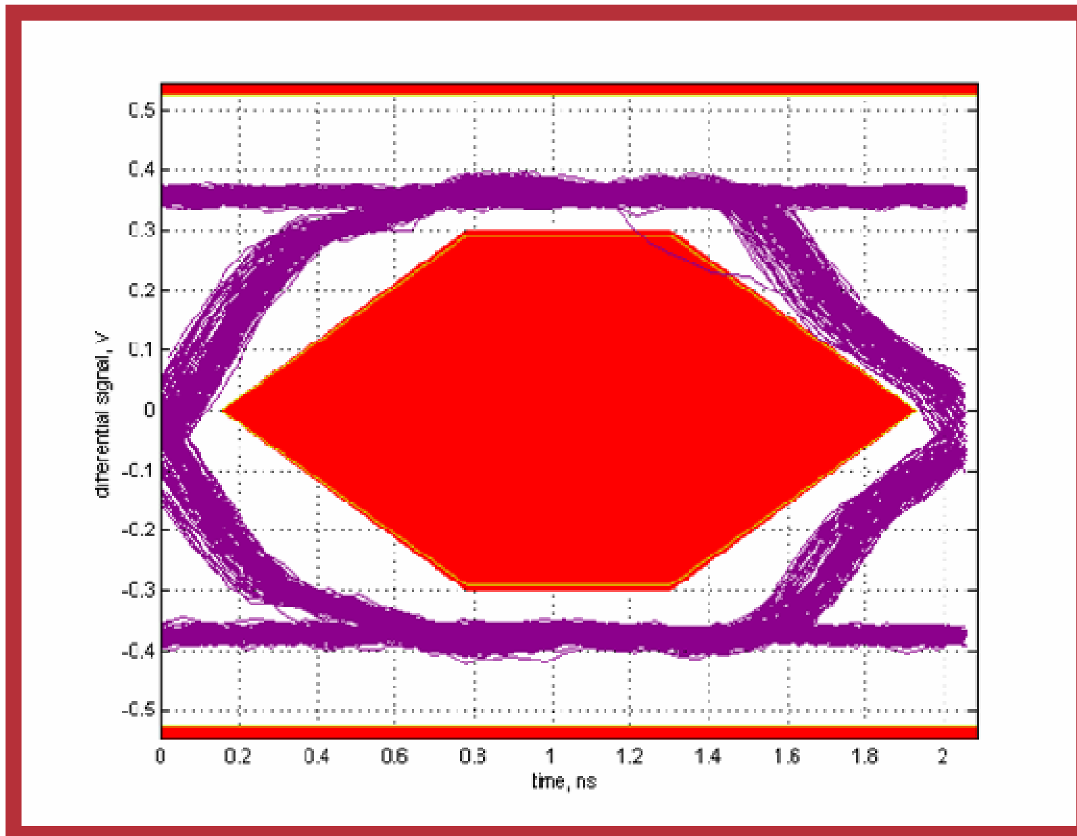

**Supply de-coupling removed**

- Noisy power supplies can affect jitter
- Power supply filtering (decoupling) recommended

© 2006 Synopsys, Inc. (63)

SYNOPSYS®
Predictable Success

# USB 2.0 Compliance – Eye Diagram



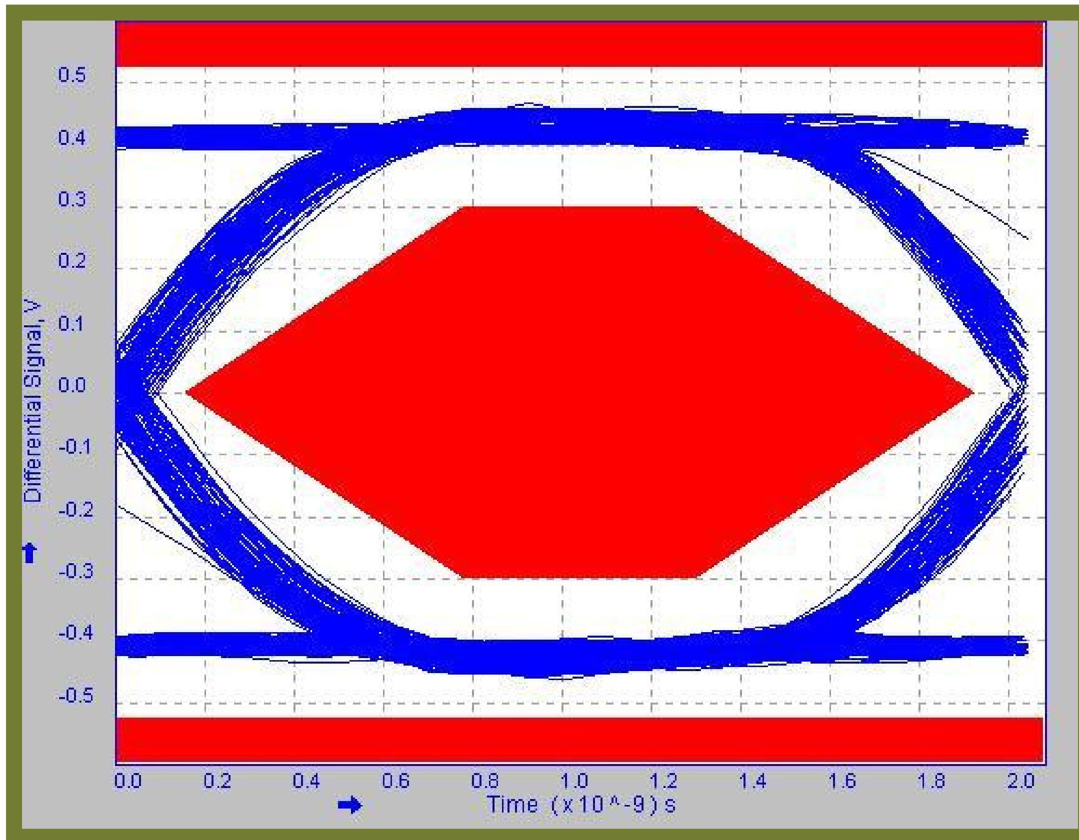

**Excess board parasitics introduced**

- Low HS DC levels
- Rise/fall shape not smooth
- High jitter
- Last bit transition violates eye



SYNOPSYS® Predictable Success

# USB 2.0 Compliance – Eye Diagram




- ✓ HS DC levels
- ✓ Rise/fall shape
- ✓ Jitter
- ✓ Crossover voltage



SYNOPSYS® Predictable Success

# Outline

- Analog versus digital design in sub-wave length technologies
- Design partitioning (Mixed-signal design)
- Mixed-signal design example: a duty cycle corrector
- Killer sources of variation in analog design
  - STI, WP, CS, OPC/PSM, NBTI, HCI
  - Current mirror example
- Analog design trends @ 65 nm
- Low jitter PCI Express® PHY
- Yield by design – USB 2.0 PHY
- Summary



SYNOPSYS®
Predictable Success

# Summary

- High performance analog/mixed-signal circuits are possible in standard deep sub-micron CMOS technologies
- A thorough understanding of the deep-submicron process effects must be made in order to produce working, robust production worthy analog/mixed-signal designs
- This requires close co-operation between the fab. process engineers, circuit designers and EDA vendor



SYNOPSYS®
Predictable Success

SYNOPSYS®

Predictable Success

© 2006 Synopsys, Inc. (68)