Chapter 2

Basing Circuits

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Version-II, 2012,09

Focus on the Contents

Biasing: Constant current/Voltage generation; $V \Leftrightarrow I$

-- Single branch, the simplest biasing

-- Multi-branches coupled biasing (Linear/Nonlinear CM);

L-CM for current transportation; NL-CM for current definition;

-- Dynamic property.

Current Mirror

-- Current Source/Sink for transfer, used in & out biasing

-- Cascode CM used for impedance boosting

Excellent or Ideal biasing

-- Better in matching when delivering current;

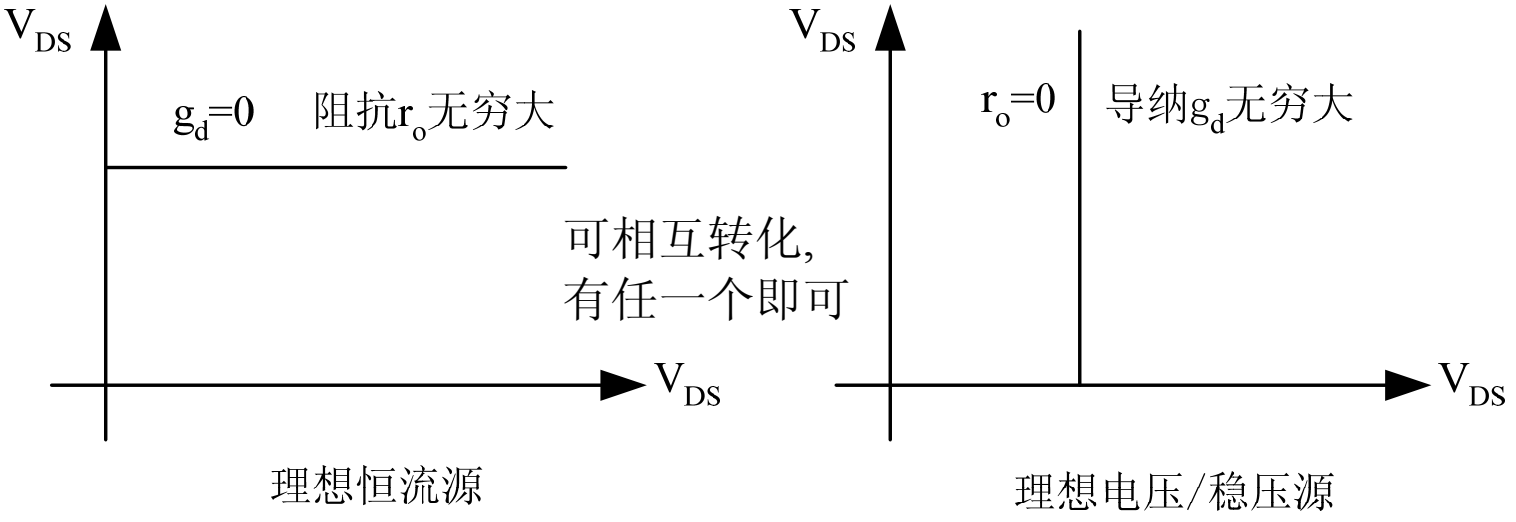
-- Stable when V_{DD}, temperatures are varied

Ideal Biasing: Voltage/Current Source

Biasing for a MOSFET: Static I_{DS} and V_{GS} provided circuit

- To generate a stable I_{DS} by a fixed V_{GS} when located at S.R. or
- To generate a stable V_{GS} by a fixed I_{DS} when located at S.R.

PVT insensitivity: Process, Voltage, Temperature; **Endless**
V/C Reference: V/C Source with zero Temperature Coefficient



How to generate stable biasing

For passive element, no operation point or biasing conditions are required, but it's necessary for active devices used in analog signal processing;

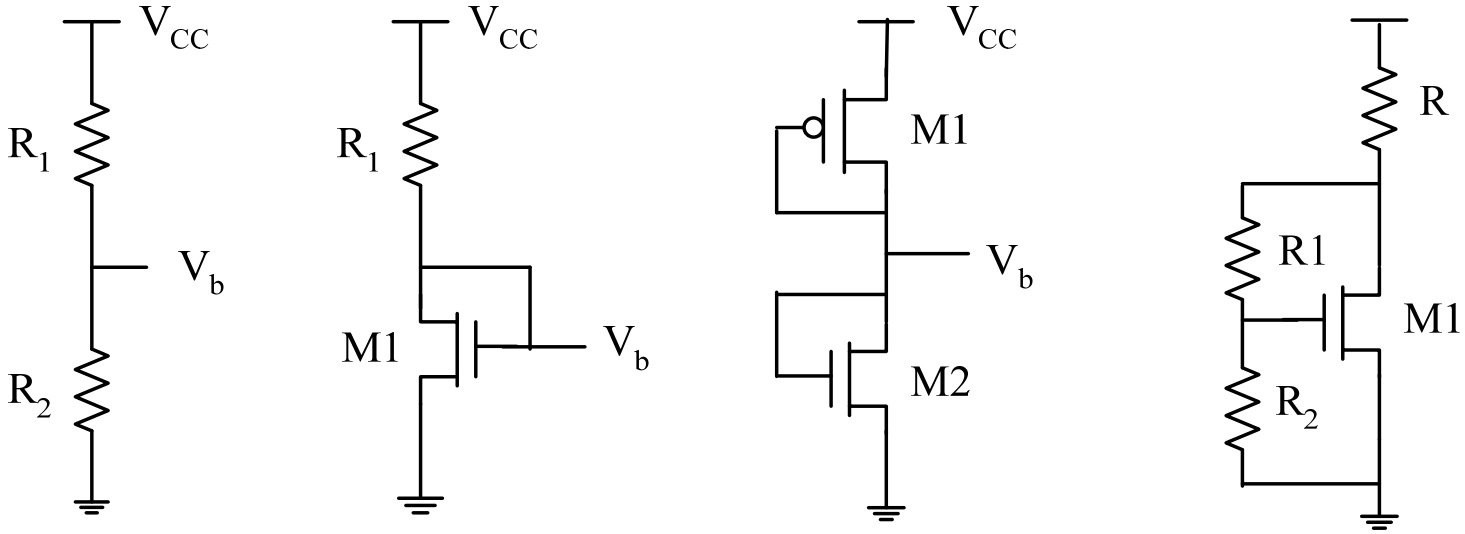
However, passive element (R) can be used for set suitable operation point for active devices, to obtain

- Current Source: high/∞ output r_d, low/zero output g_d;
- Voltage Source: low/zero output r_d, high/∞ output g_d

There is no possibility to obtained the stable static biasing for active devices purely by linear passive element, NL elements are certainly required.

Simple Biasing: Single branch type

1. R+R type 2. R+MOS Diode 3. Diode + Diode 4. Coupled



1. Simplest, both I_b & V_b are linear changed with V_{DD}, unfit for IC ;
2. NL resistance induced, V_b varied small, but I_b remain changed quickly with V_{DD}； widely used in IC for simplicity.
3. NL+NL resistance, both I_b & V_b varied with V_{DD}, seldom used;
4. V_{GS} boost, current reduction, mixed structure of single branch.

Basic Voltage divided Principle Review

Static V_b from V_{CC} for provide V_{GS} :

$$V_b = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{1}{1 + R_1 / R_2} V_{CC} \Rightarrow V_{GS}$$ Constant needed

Interrupt ΔV_b from ΔV_{DD} :

$$\Delta V_b = \frac{r_2}{r_1 + r_2} \Delta V_{CC} = \frac{1}{1 + r_1 / r_2} \Delta V_{CC}$$ Zero required

Nonlinear resistance should be introduced to separate DC R from AC r. For ΔV_b=0, $r_1 \rightarrow \infty$ (constant I) & $r_2 \rightarrow 0$ (constant V) are required, which mean that the voltage source and current source should be used together in a single branch, in this way the fixed DC V & I can be certainly established by variable R_1/R_2 with V_{CC}.

R_1+MOS Diode (r_2)

If R_2 is replaced by MOS Diode, R_2 for DC, r_2 for AC, and $R_1=r_1$

$$R_2 = \frac{V_{GS}}{(1/2)k\Delta^2} = (\frac{2V_{GS}}{\Delta})\frac{1}{g_m} \qquad r_2 = \frac{1}{g_m + g_d} \approx \frac{1}{g_m}$$

$$2V_{GS}/\Delta) >> 1 \Rightarrow R_2 >> r_2$$

DC & AC resistance for MOS Diode is well separated!

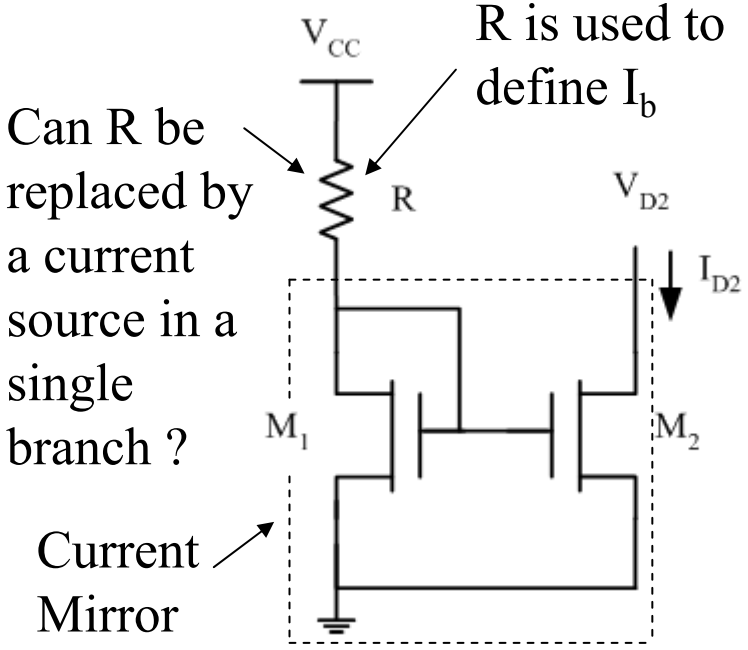
Negative FB control: $V_{CC}\uparrow \Rightarrow I_b\uparrow \Rightarrow g_m\uparrow \Rightarrow R_2, r_2\downarrow \Rightarrow$ 分压比$\downarrow \Rightarrow$ Stable.

Ques: For single branch, how to achieve Voltage & current source simultaneously, and where the current source coming from?

R+MOS Diode Biasing for Current Mirror

Deal with the output current and gate voltage translation.

Take the reason (Input) and the results (Output) relationship.



Partially requirements are satisfied!

$$\frac{1}{2}k(V_b - V_{TH})^2 = \frac{V_{CC} - V_b}{R_1}$$

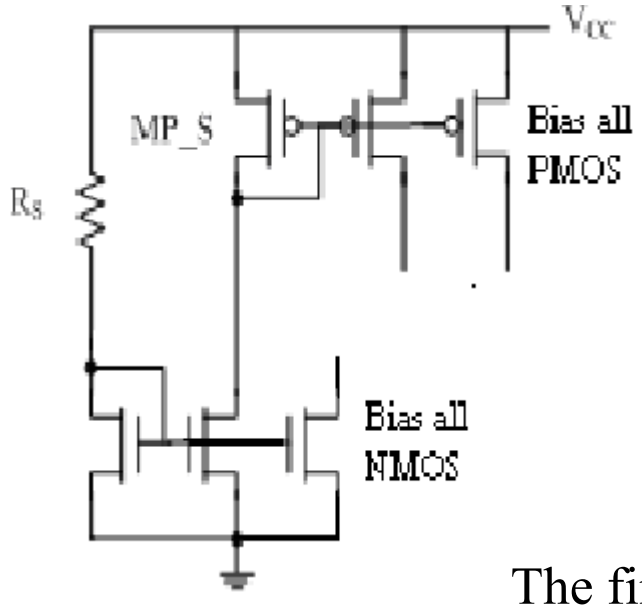
$$V_b = V_{TH} - \frac{1}{kR_1} + \sqrt{(\frac{1}{kR_1} - V_{TH})^2 + \frac{2V_{CC}}{kR_1}}$$

$$= V_{TH} + \Delta$$

Weak related with V_{CC}

Single branch biased circuit is poor at current stability!

I⇔V transform for all NMOS & PMOS Biasing



If stable biased V_{GSN} is generated, it can be used to bias all other NMOS transistors in a form of Current mirror.

I-V-I transform:

Constant I_{in} → Constant V_{GSN} →

→ Constant I_{out} → Constant V_{GSP}

The first one (reason) is generated by biasing circuit

Attention: NMOS is biased by V_{GSN}, PMOS is biased by V_{GSP}, in the form of linear current mirrors.

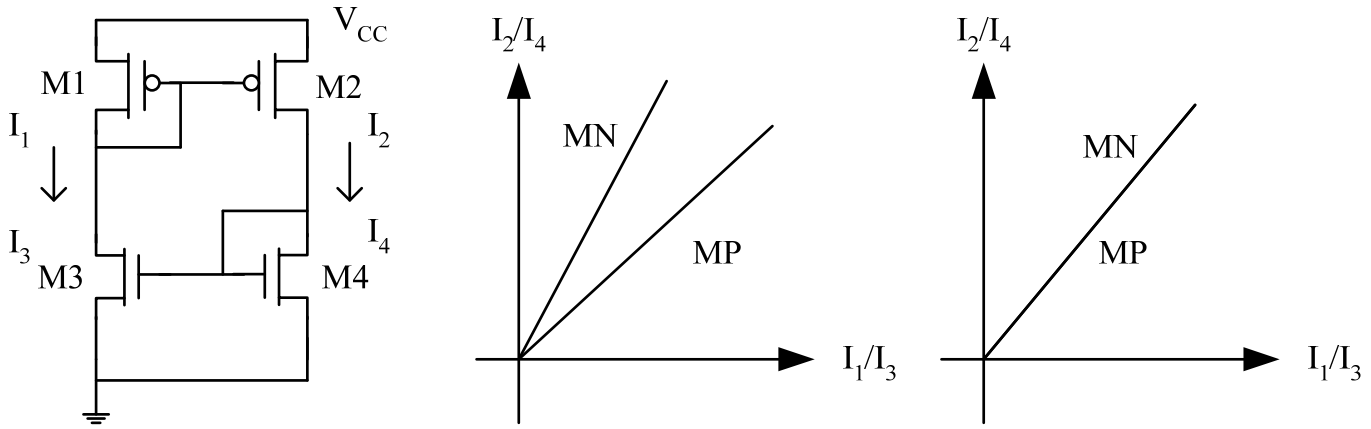
Principle: NMOS to bias NMOS, PMOS to bias PMOS, same type

Multi-Branches Biased Circuits

Two branches biased circuit:

NMOS current mirror + PMOS Current mirror coupled (biased) for each others to obtain only one intersection point other than zero (static point).

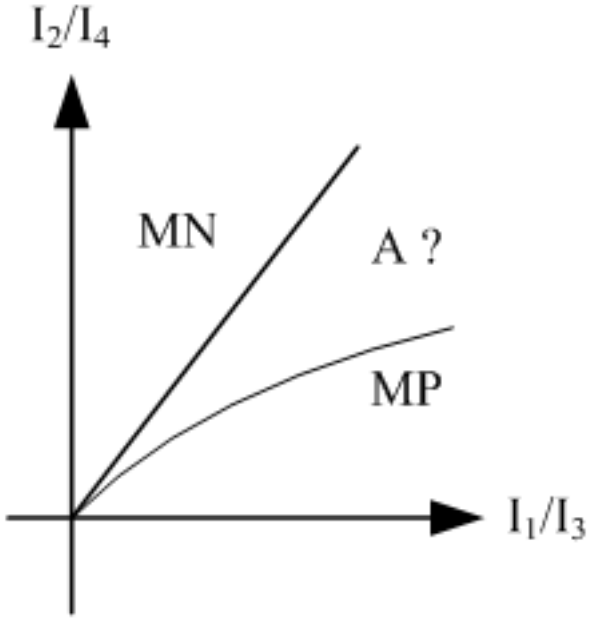
Thus, at least one of the two CM should be given as NL CM.

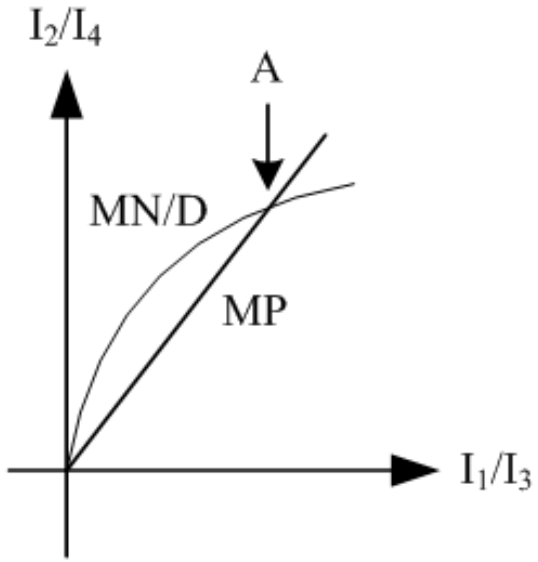


One branch: high impedance + low impedance architecture.

If both are NL CM, two situation happen: 1) no intersection point except original point; 2) infinite intersection points. Failed in biasing

Non linear CM is enough?



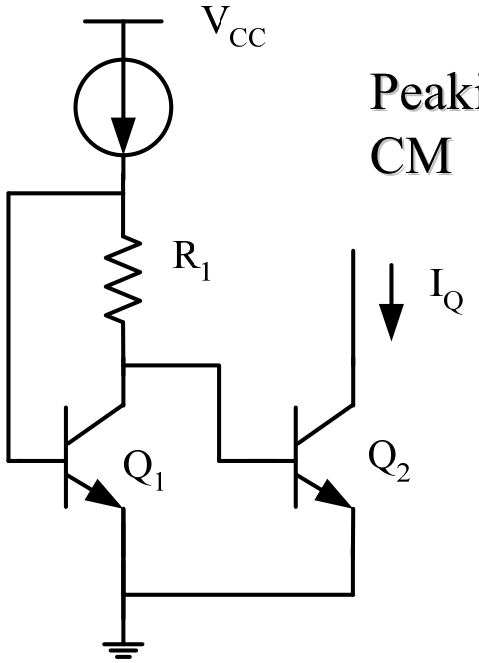


Only one intersection point A except O(0,0) is required.

It's unnecessary to introduce two NL CM (keep one L-CM)

L-CM: **current transportation**; NL-CM: **current definition**.

Nonlinear CM by different V_{BE}



Peaking CM

NL CM

- Two branch I_{Q1}, I_{Q2};
- $I_{Q1}=I_{Q2}$ defined by L-CM; $m_{1\text{-}2}=1$
- $S_{Q2}:S_{Q1}=N_{2\text{-}1}>1$
- $\Delta V_{BE}=V_{BEQ1}-V_{BEQ2}=V_{R1}$;
- $I_{Q1,2}=\Delta V_{BE}/R_1$ $N=m_{1\text{-}2}N_{2\text{-}1}$

$$V_{BE,Q} = V_T \ln(I_Q / I_{SQ})$$

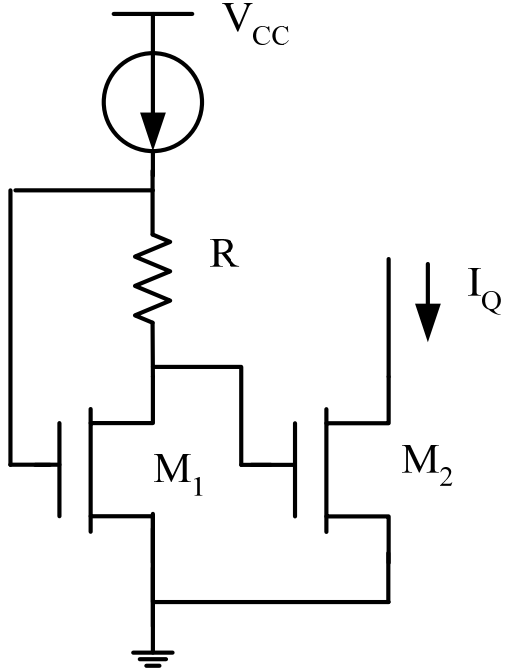
$$\Delta V_{BE,Q1\text{-}Q2} = V_T \ln(\frac{I_{Q1}}{I_{Q2}}\frac{S_{Q2}}{S_{Q1}}) = V_T \ln(m_{1-2}N_{2-1}) = V_T \ln N$$

$$I_{Q1} \approx I_{Q2} = \frac{V_R}{R_1} = \frac{\Delta V_{BE}}{R_1} = \frac{V_T}{R_1}\ln N$$

V_{CC} unrelated!

Nonlinear CM by different V_{GS}

Peaking CM, similar as BJT typed circuit.



$$I_1 = \frac{V_R}{R_1} = \frac{V_{GS1} - V_{GS2}}{R_1} \approx \frac{\Delta_{M1} - \Delta_{M2}}{R_1}$$

$$= \frac{\Delta(\Delta_{M1,2})}{R_1} = \frac{1}{R_1}\left(\sqrt{\frac{2I_{M1}}{k_1}} - \sqrt{\frac{2I_{M2}}{k_2}}\right)$$

$$If \quad I_{M1} \approx I_{M2} = I_Q; \quad k_2 / k_1 = N_{2-1}$$

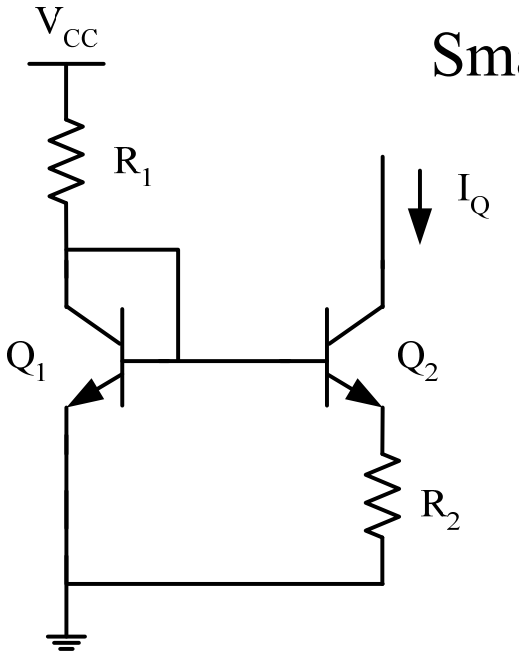
$$\sqrt{I_Q} = \frac{\sqrt{2}}{R_1}\frac{1}{\sqrt{k_1}}\left(1 - \sqrt{\frac{k_1}{k_2}}\right) = \frac{\sqrt{2}}{R_1}\frac{1}{\sqrt{k_1}}\left(1 - \sqrt{\frac{1}{N}}\right)$$

$$I_Q \approx \frac{2(\sqrt{N} - 1)^2}{k_1 \cdot N \cdot R_1^2}$$

V_{CC} unrelated.

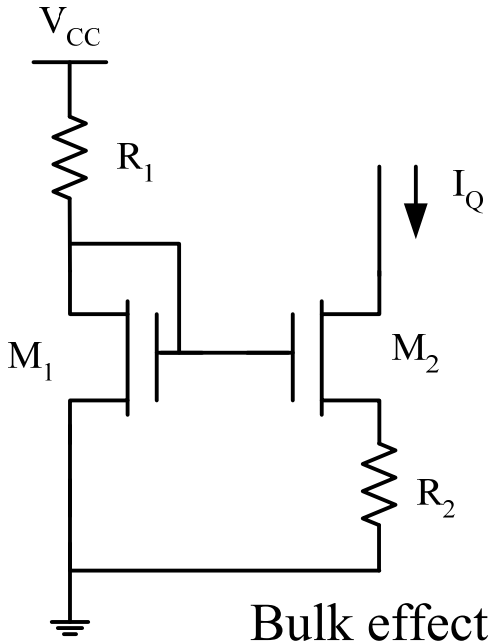
Ques: Is I_Q really **completely unrelated** with V_{CC}, why? How to improving?.

Widlar NL CM, another ΔV_{BE} or ΔV_{GS}



Small current generation

Current definition R_2 is located at emitter or source of N-typed device to configure NL CM.



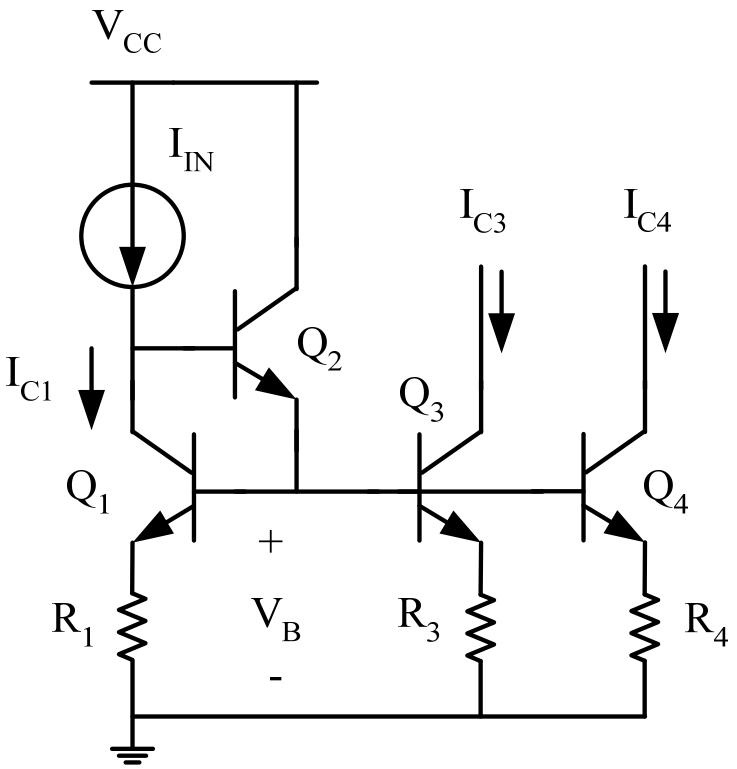
Bulk effect

$$I_Q = \frac{\Delta V_{BE,Q1-Q2}}{R_2}$$

Relation between two branches current is actually important in determining ΔV_{BE} or V_{GS}.

$$I_Q = \frac{\Delta V_{GS,M1-M2}}{R_2}$$

Nonlinear Return Back to Linear ?



Nonlinear → Linear

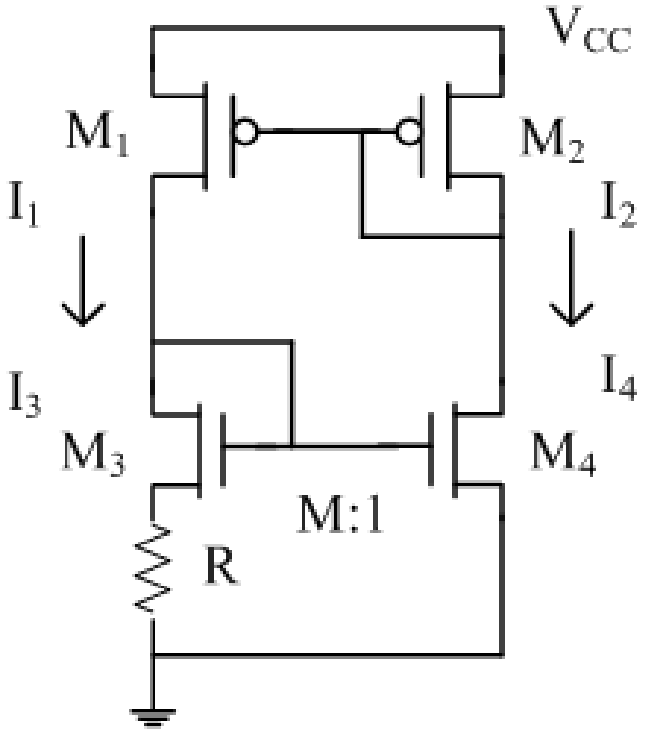
R_i at emitter is used to set equal or balanced V_{BE} for returning back as L-CM.

Ri used to define current relationship, not the current value.

Emitter areas of each Qi should be in proportion as current ratio defined.

Complicated in dimension arrangement

Location of R and dimension of NL-CM



If R located below M3 at source,

So $V_{GS3}<V_{GSM4}$;

If $I_3=I_4$ defined by PMOS L-CM;

So $(W/L)_{M3}:(W/L)_{M4}=N>1$;

Current dynamic: first (from 0) negative FB, Later positive FB.

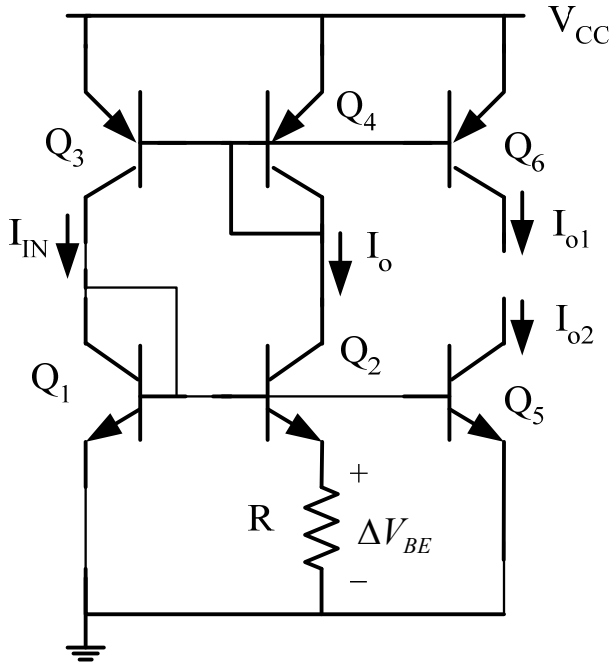
So, static current can not be setup and stable.

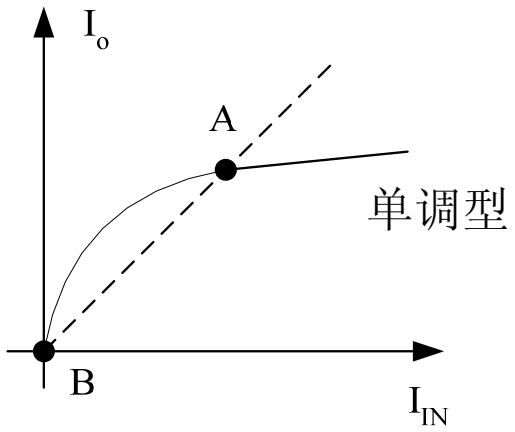
R should be located under M4 (at source), opposite with the M3 diode transistor, and $(W/L)_{M4}:(W/L)_{M3}=N>1$.

Two branch of coupled Self-Biasing: $\Delta V_{BE}/R$

NL-CM is monotonous type:

output current is increased with increasing of input current



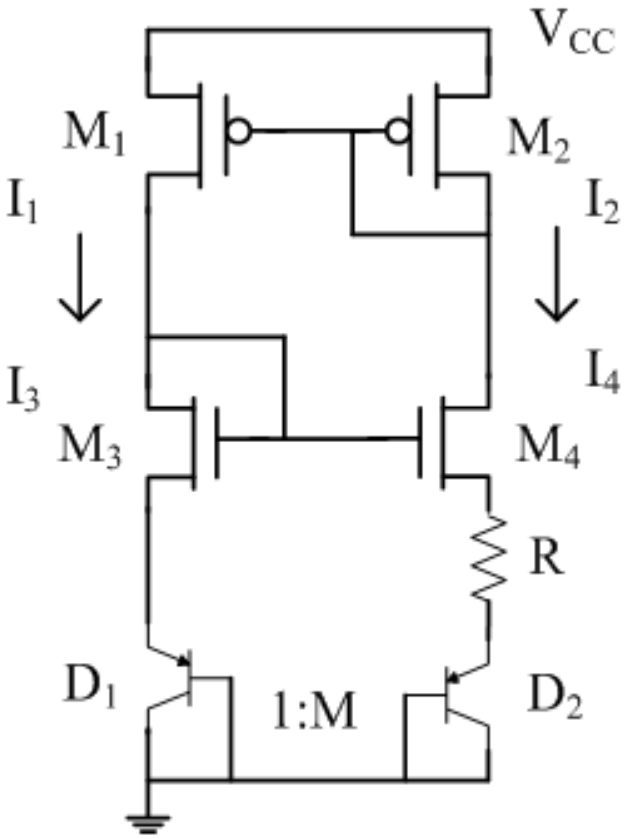


$S_{e,Q2}$: $S_{e,Q1}$ =N>1

BJT Version → CMOS Version

ΔV_{BE} → ΔV_{GS} (W.I. & S.I)

$\Delta V_{BE}/R$ provided by Parasitic PNP transistors



In N-Well CMOS, there are no lateral NPN transistors, only vertical parasitic PNP transistors existed (P+ S,D/N-well/P-sub)

I_3=I_4 defined by PMOS L-CM

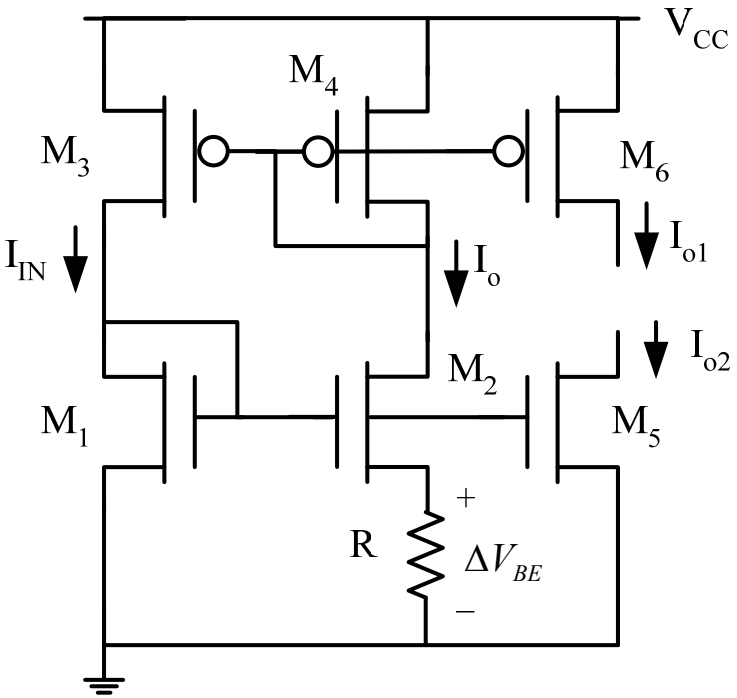
$$(\frac{W}{L})_{M3} = (\frac{W}{L})_{M4} \Rightarrow V_{S,M3} = V_{S,M4}$$

$$I_R = \frac{V_R}{R} = \frac{\Delta V_{BE,Q1-Q2}}{R} = \frac{V_T}{R}\ln M$$

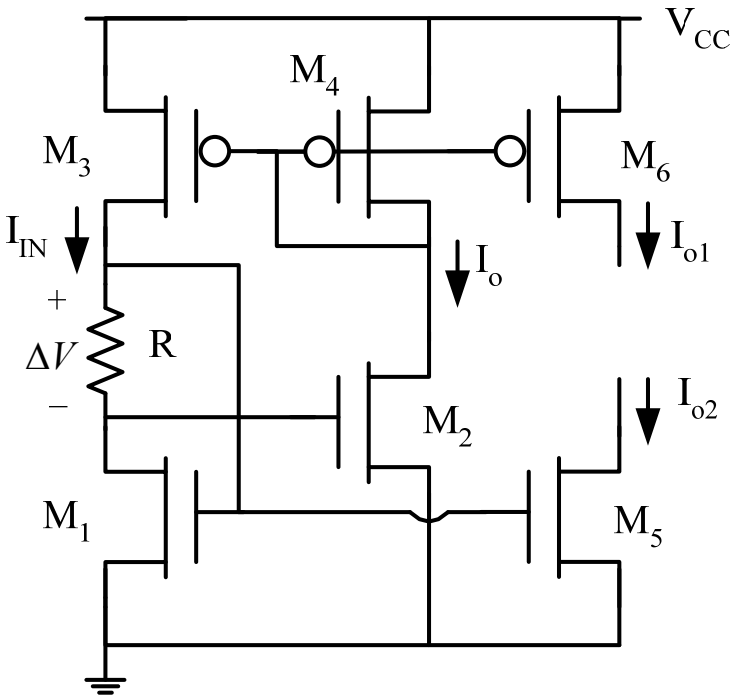
If D1 & D2 removed? Or if only D2 removed?

Two branch coupled Self-Biasing: $\Delta V_{GS}/R$

MOS monotonous NL-CM



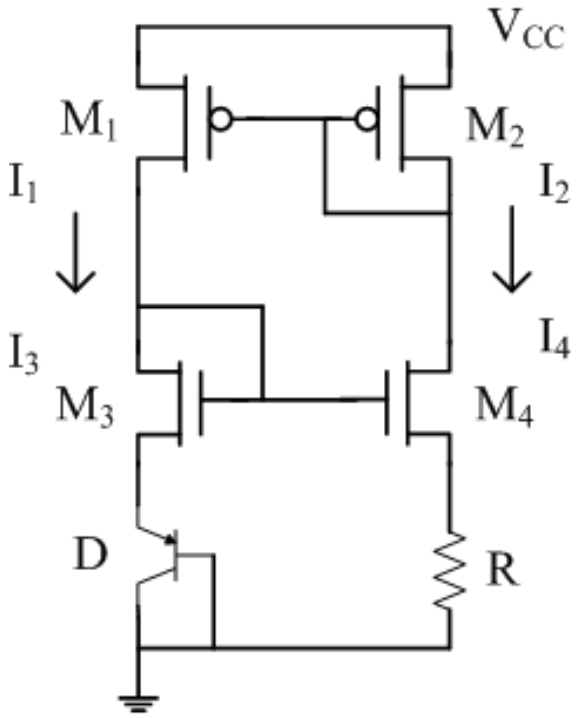
MOS Peaking NL-CM



Ques: Is the current the same when NL-CM operated under S.I. and W.I.?

Voltage positive FB Loop gain >1?

Nonlinear CM of V_{BE}/R type



Where R should be located?

Positive feedback? Why?

$V_{S,M3}$ is not always equal to $V_{S,M3}$ when I_3 and I_4 changed, so M3 and M4 service as NL-CM in general.

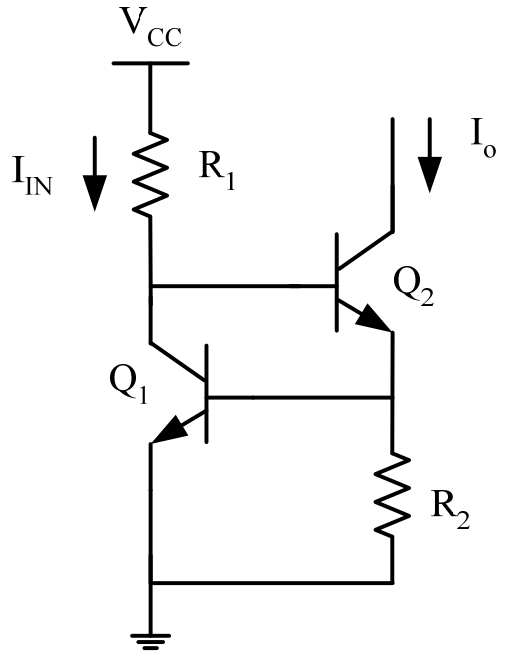
Only in equivalent statue when I_3=I_4 defined by PMOS L-CM, $V_{S,M3}$=$V_{S,M4}$ is generated by $(W/L)_{M3}$=$(W/L)_{M4}$, thus

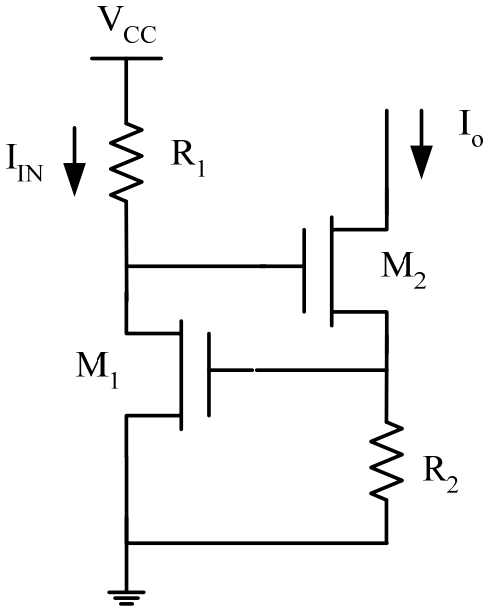
$$I_1 \approx I_2 = \frac{V_{S,M4}}{R} = \frac{V_{S,M3}}{R} = \frac{V_{BE}}{R}$$

Large current by $I = \frac{\Delta V}{R} \Rightarrow I = \frac{V}{R}$

Other Way in define V_{BE}/R or V_{GS}/R

The setting of $V_R=V_{BE}$ or $V_R=V_{GS}$ is changed from virtual short-circuit to physic direct short connection.





$$I_{in}(MOS)=\frac{V_{CC}-V_{GS1}-V_{GS2}}{R_1}$$

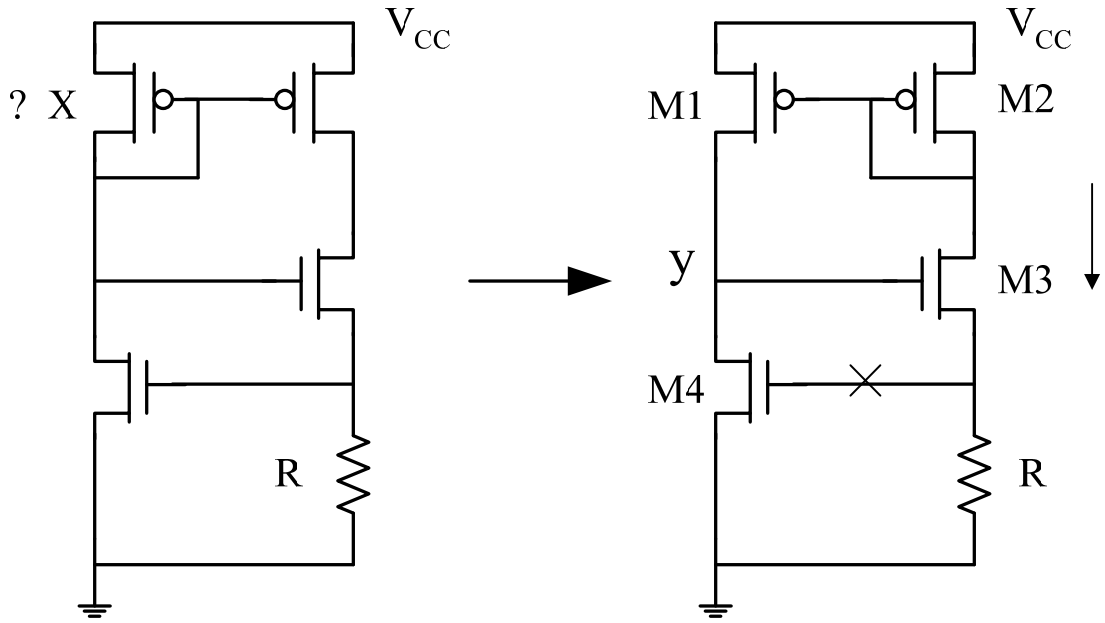
$$\approx\frac{V_{CC}-2(V_{TH}+\Delta)}{R_1}$$

$$I_o=\frac{V_{GS1}}{R_2}\approx\frac{V_{TH}+\Delta}{R_2}$$

Two resistor define two branches current

If R_1 is replaced by PMOS L-CM to set $I_{in}=I_o$ and if currents are small to give $\Delta\approx0$, then $I_o\approx V_{TH}/R_2$.

How to combined with PMOS L-CM?



$$A = -g_{m4}(r_{ds4} \,//\, r_{ds1})$$

$$r_{o3\_Down} = R(1-A)g_{m3}r_{ds3}$$

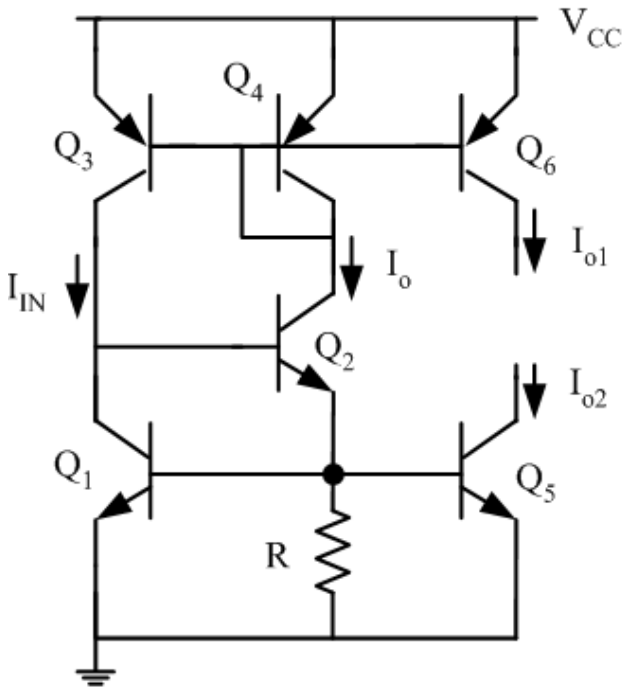
Break at x, two stage **negative FB** to make V_R stable. AC short effect to make r_y small in down direction.

Left PMOS in diode is wrong: left side all in low impedance and right all in high impedance;

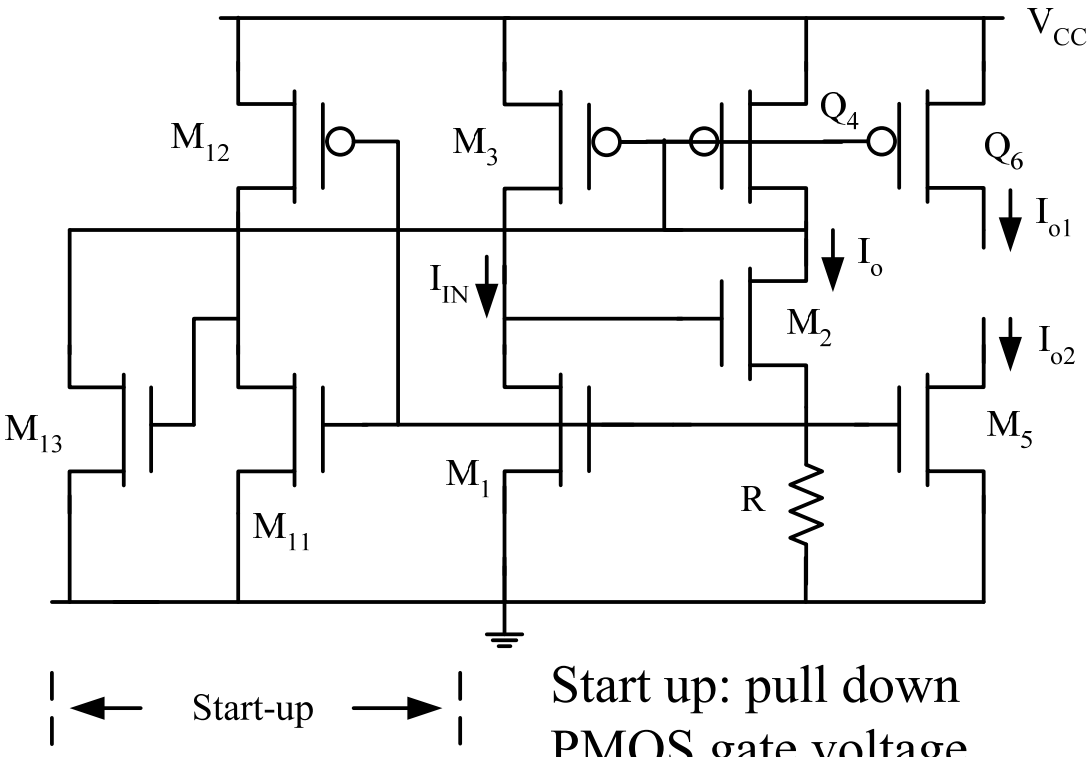
Right PMOS in diode is correct: every side or branch is coupled by low + high impedance.

Completed V_{BE}/R & V_{GS}/R Circuits

BJT V_{BE}/R

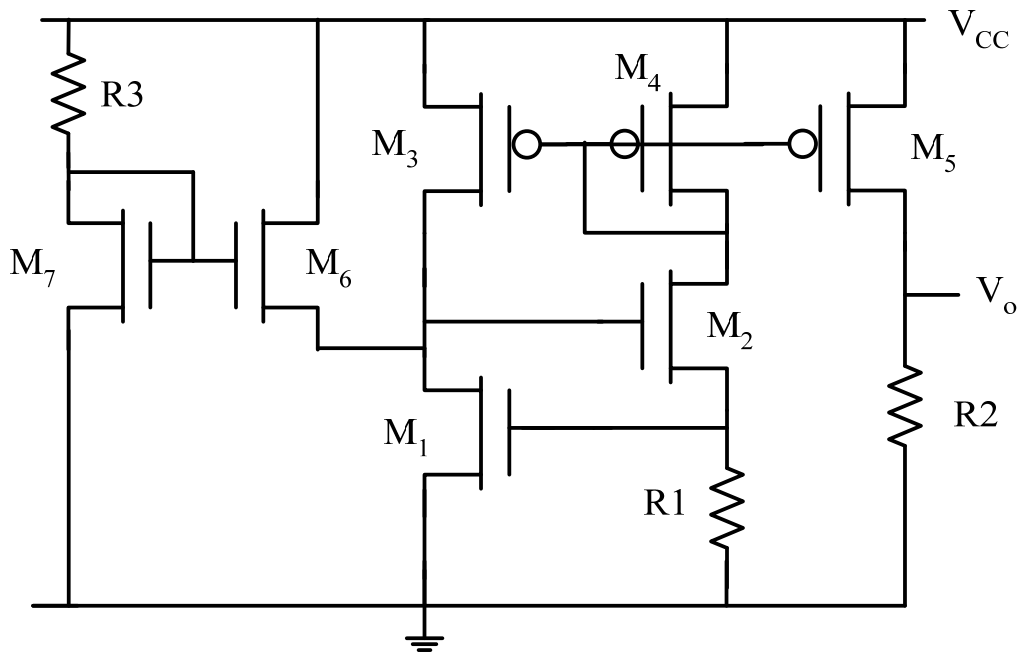


CMOS V_{GS}/R including Start up



Start up: pull down PMOS gate voltage

Start up Circuit



Start up:

1. Effective during power on transient;
2. Low power or zero static current
3. Reliability, multi-times start up needed
4. Do not interrupt biasing circuit in normal operation region.

Start-up

Start up: pull up NMOS gate voltage

I-V转换

Current consumption of start up circuit is large due to R+MOS diode biasing branch in start up circuit.

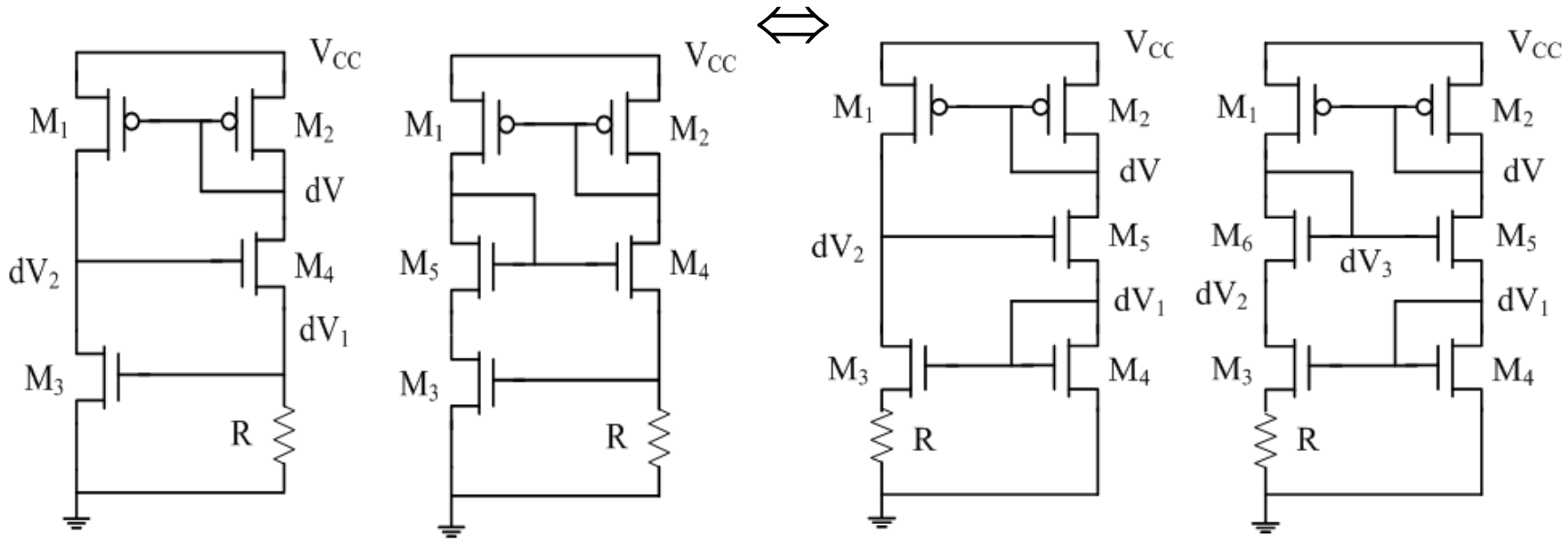
Using Capacitor start up circuit

Level Shift, Change between V/R & ΔV/R

SE
NANJING

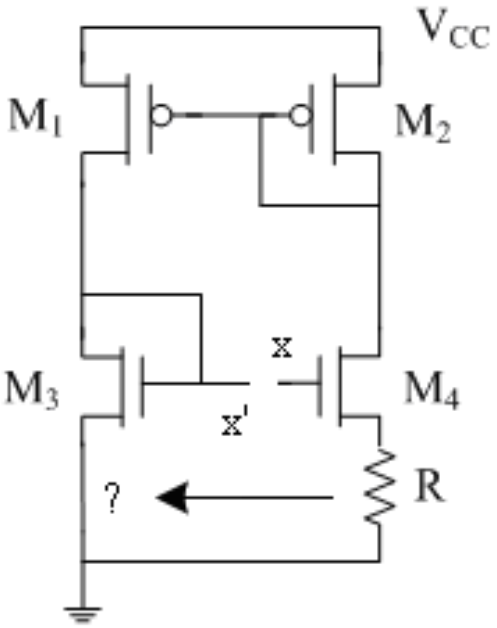
M5 Diode added to drop down the drain voltage of M3

Different in NL-CM definition
Change from V/R → ΔV/R



What happens when resistor R is replaced by a MOS diode (AC:$1/g_m$)?
Nonlinear CM in definition branch current is disappeared! Another R!

Dynamic Property in view of Voltage FB



Break at x-x', two gain stages consist of positive FB

$$A_{loop} = \frac{g_{m4,eff}}{g_{m2}}\frac{g_{m1}}{g_{m3}} = \frac{g_{m4,eff}}{g_{m3}} = \frac{1}{1+g_{m4}R}\frac{g_{m4}}{g_{m3}}$$

Initial, both g_{m3},g_{m4} are ultra small, but $g_{m4}/g_{m3}>>1$, So positive FB with loop gain $A_{loop}>1$, Start up!

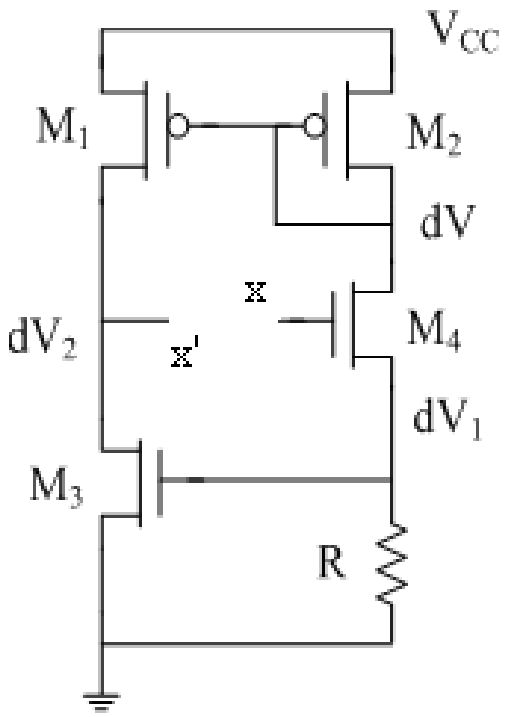
When current is larger enough, $g_{m4}R>1$ to decrease the positive loop gain, when $A_{loop}=1$ the static voltages and currents are finally established.

Latch?
2 INV!

If R located with M3 $A_{loop} = \frac{g_{m4}}{g_{m2}} g_{m1}(\frac{1}{g_{m3}} + R) = (1+g_{m3}R)\frac{g_{m4}}{g_{m3}}$

Initial: $g_{m4}/g_{m3}<<1$, $A_{loop}<1$, no possibility to start up.

Dynamic Property by multi-FB loop



Break at x-x', two FB loop forms, one is positive, (x-dV-dV_2) the other one is negative (x-dV_1-dV_2)

Loop gain and variation with the statues?

Initial, positive loop gain is stronger than that negative loop gain, net positive gain is larger than 1 to start-up.

Later, when current is larger enough, negative loop gain is larger than that of positive loop gain, to get stable static point.

Comparison of single & multi-FB Loop?

Time varying and **nonlinear** are critical in self-biased circuit start up analysis.

P-FB with gain>1 for startup; P-FB with gian=1 or N-FB for stable

Application & Improvement

Application of the Biasing circuit → Current Mirror

Improvement of Current Mirror

Improved CM returned back to improve biasing circuit.

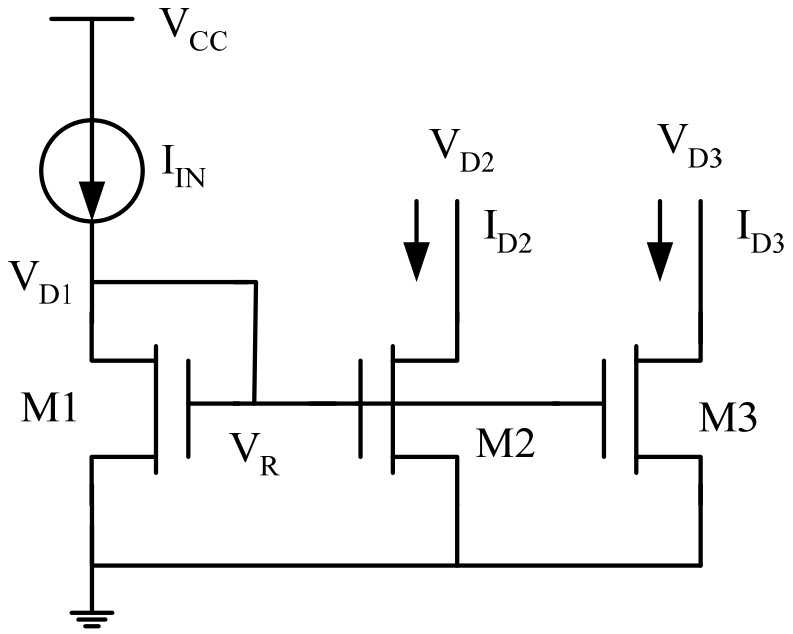
Main aspects that can be improved for CM

Matching of the different branch current: voltage match;

High PSRR of biasing current: high impedance output;

Low power, Low voltage or wide Voltage swing.

Mismatch in Conventional L-CM



Unmatched current by unmatched V_{DS}!

$$\frac{I_{DS2}}{I_{IN}} \approx \frac{(W/L)_2}{(W/L)_1} \times \frac{1+\lambda_2 V_{DS2}}{1+\lambda_1 V_{GS1}}$$

Absolute capability improve:

$r_o \to \infty$ by $\lambda_1=\lambda_2=0$;

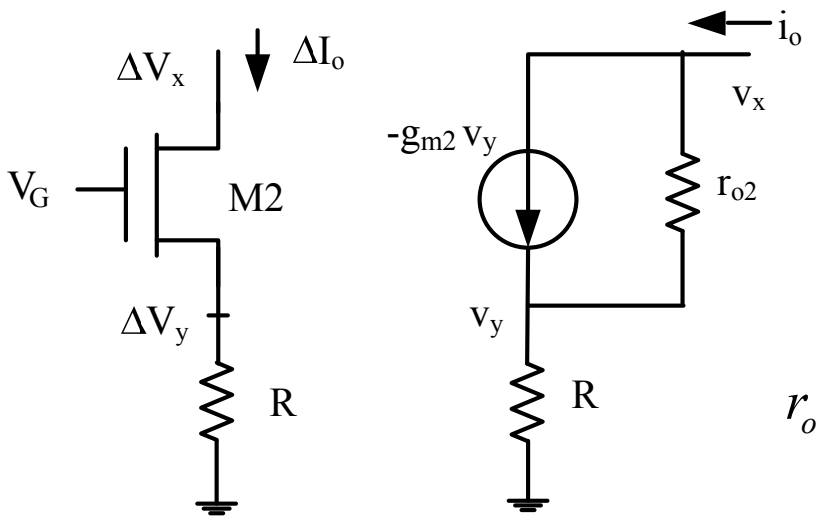
Matching improve:

limited r_o, or $\lambda_1=\lambda_2>0$

but $V_{DS1}= V_{DS2}$.

How to set the same V_{DS} in CM? Cascode! Effective r_o is improved!

Resistance improve & Gm degradation



Equivalent circuit analysis

$$\Delta V_y = \Delta I \times R = -\Delta V_{gs}$$

$$\Delta I = -g_{m2}\Delta V_y + (\Delta V_x - \Delta V_y)/r_{o2}$$

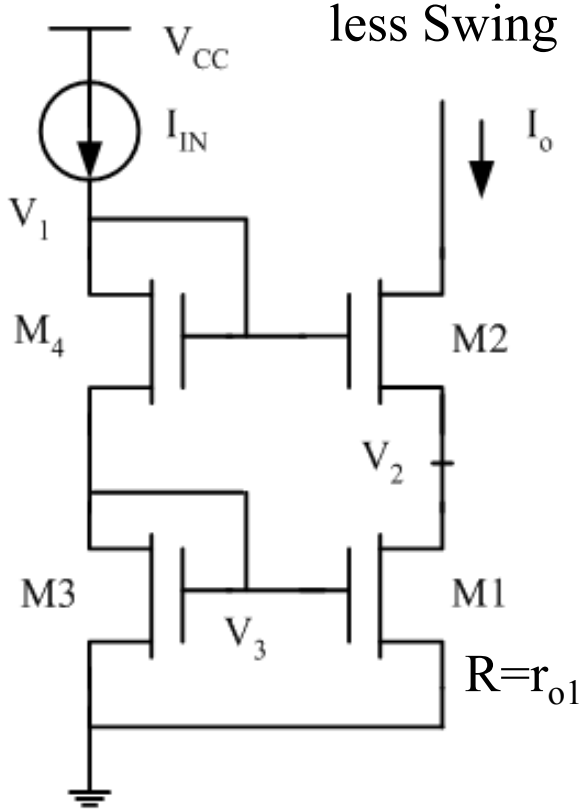
$$r_o = \frac{\Delta V_x}{\Delta V_y / R} = R\frac{\Delta V_x}{\Delta V_y} = R + r_{o2} + (g_{m2}r_{o2})R$$

CG gain effect: current remain but voltage boost

Function of source resistance R?

G_m degradation $\quad G_m = \frac{\partial I_{DS}}{\partial V_{gs}}\frac{\partial V_{gs}}{\partial V_g} = g_m \frac{1/g_m}{1/g_m + R} = \frac{g_m}{1 + g_m R}$

Simple Cascode Current Mirror



less Swing

V_{DS} matching of M1 & M3

V_2=V_3 under $I_{in}=I_o$ & $(W/L)_{M2}=(W/L)_{M4}$

Resistance boosting

$$r_o = r_{o1} + r_{o2} + g_{m2} r_{o2} r_{o1}$$

Reduction to Simple CM

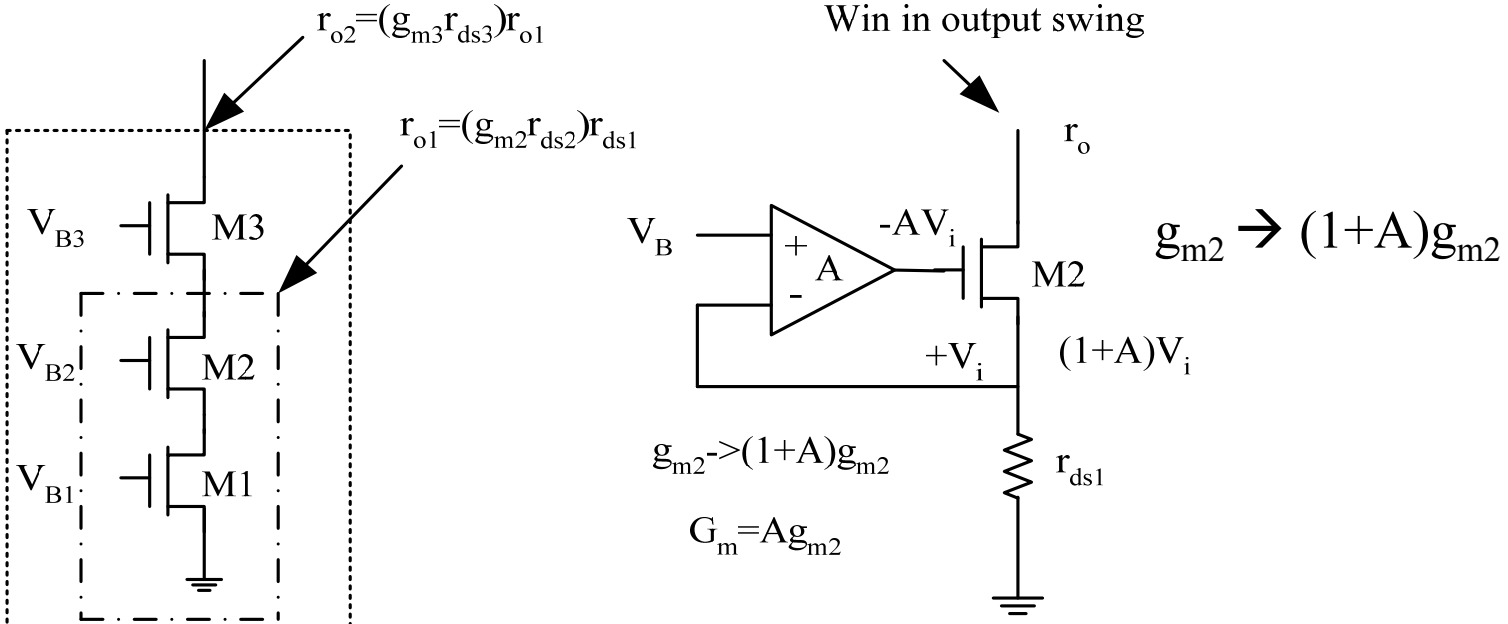
$$r_{o1} = 0 \Rightarrow r_o = r_{o2}$$

$$r_{o2} = 0 \Rightarrow r_o = r_{o1}$$

M3, M4, M1 is certainly and M2 should be stay at Saturation region.

Current transfer accurate is significantly improved!

Multi-Layer Cascode for more impedance boosting



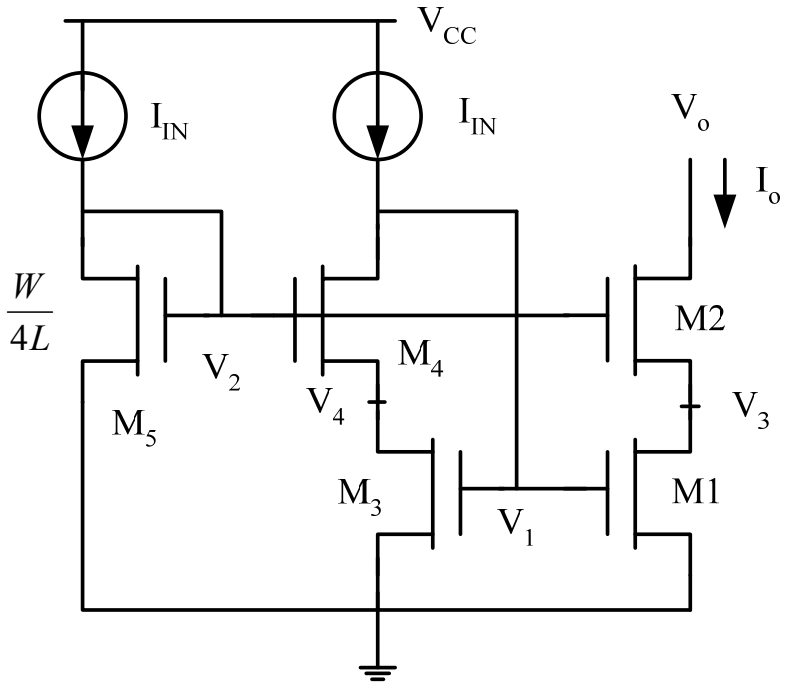
$r_o=(g_{m3}r_{ds3})(g_{m2}r_{ds2})r_{ds1}$
$=(Ag_{m2})r_{ds2}r_{ds1}=(G_mr_{ds2})r_{ds1}$

$r_o=G_mr_{ds2}r_{ds1}$
$=Ag_{m2}r_{ds2}r_{ds1}$

For multi-layer cascode output impedance boost is achieved at lost of output swing, so regulated cascode is better in saving output swing, but current consumption is significantly increased.

High-Swing Cascode CM - 1

Ignore bulk effect



W/L and overdrive relations

M1=M2; M3=M4.

$\Delta_3 \approx \Delta_4 = \Delta$; $\Delta_{5min} = 2\Delta$

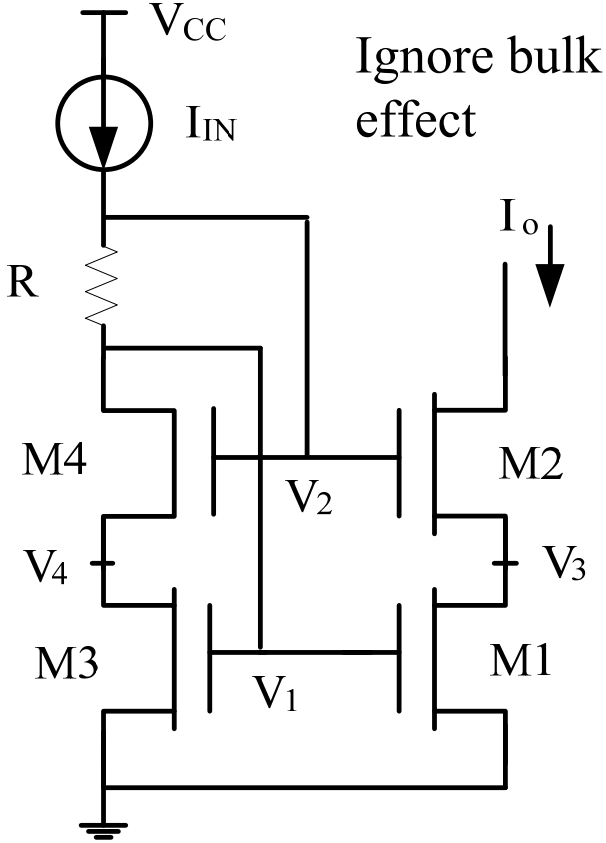
2Δ: one for M4 Δ_4, the other for $V_{DS3} = \Delta$, M3, M1 located at boundary of L/S region.

If driving currents are the same

$$\frac{(W/L)_{M5}}{(W/L)_{M4}} = \left(\frac{\Delta_4}{\Delta_{5,\min}}\right)^2 = \frac{1}{4}$$

If bulk effect of M2/M4 considered, then $(W/L)_{M5} < \frac{1}{4}(W/L)_{M4}$ for more saturation margin, but lost in output swing $V_{swing,\max} \approx V_{CC} - 2\Delta_n - 2\Delta_p$

High-Swing Cascode CM -2



Ignore bulk effect

W/L and overdrive voltage relation

M3=M1; M4=M2, M3=M4

$\Delta_3 \approx \Delta_4 = \Delta$;

V_R: $V_{R,min} \sim V_{R,max}$?

$$V_{DS3} = V_2 - V_{GS2} \approx V_2 - V_1 = V_R \geq \Delta$$

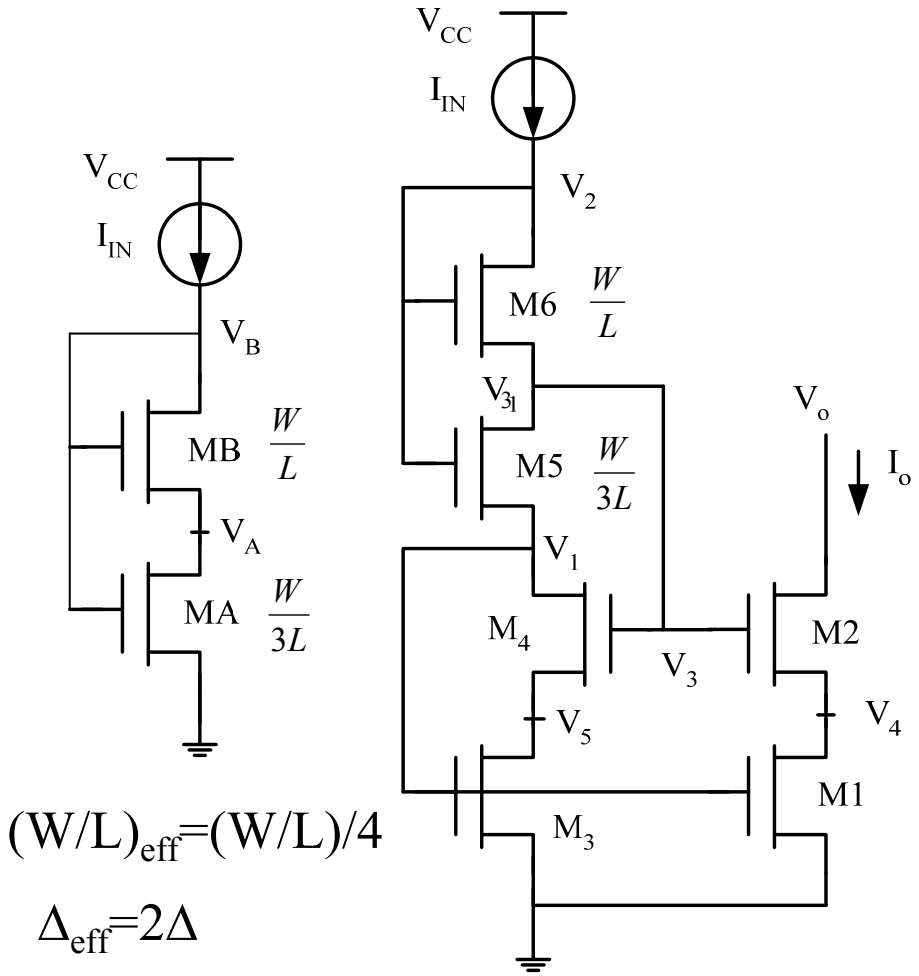
$$V_{DS4} = V_1 - V_{DS3} = V_{TH} + \Delta - V_R \geq \Delta$$

$$\Delta \leq V_R \leq V_{TH} \Rightarrow R_{\min} \leq R \leq R_{\max}$$

$$R_{\min} = \Delta / I_{in}; \quad R_{\max} = V_{TH} / R$$

Process shift will resulting in a much large variation in R, margin and Swing reduced. Less input swing.

Sooch Cascode CM: MOS Linear Transistor



$(W/L)_{eff}=(W/L)/4$

$\Delta_{eff}=2\Delta$

$I_{in}=I_{out}$; All saturated except M5

Δ under (W/L) as reference

$$\Rightarrow \quad V_B = V_{TH} + 2\Delta; \quad V_A = \Delta$$

$$V_1 = V_{TH} + \Delta$$
$$V_3 = V_{TH} + 2\Delta$$
$$V_2 = 2V_{TH} + 3\Delta$$

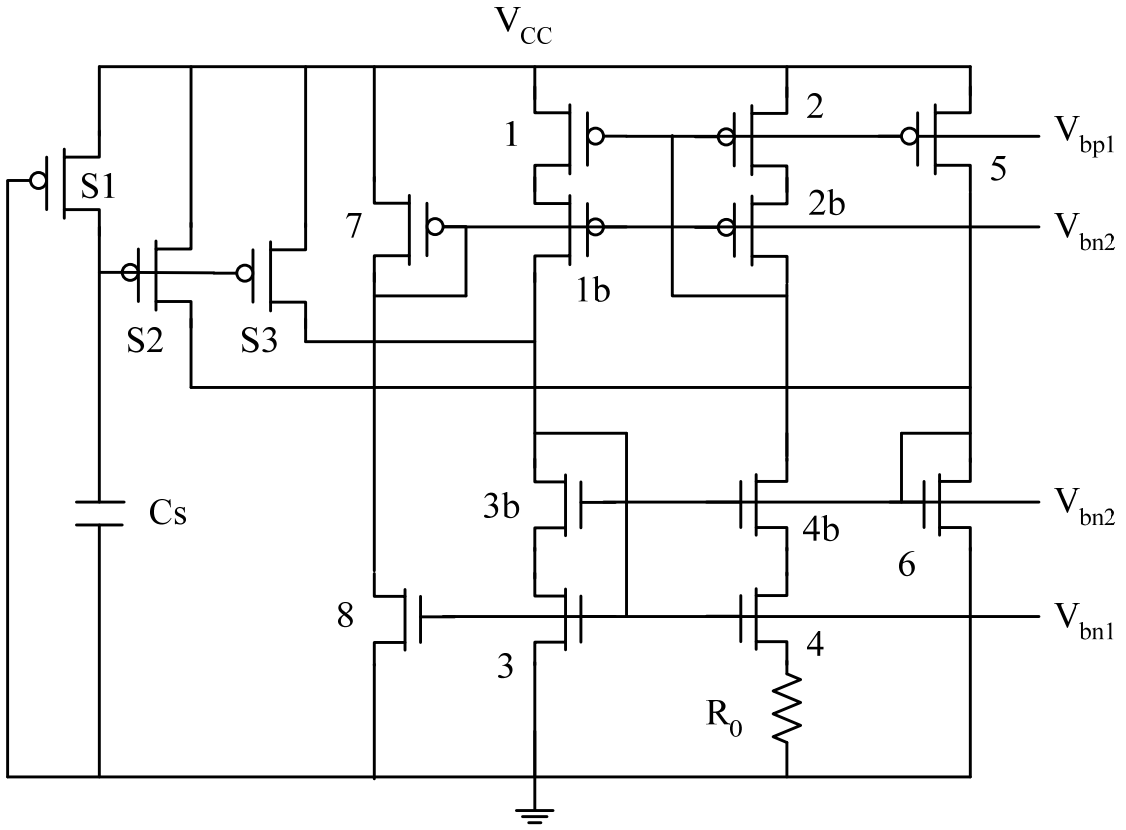
$$V_4 = V_5 = \Delta$$
$$V_3 - V_1 = \Delta$$

$$V_{o(\min)} = 2\Delta$$
$$V_{DD}(\min) = V_2 + \Delta = 2V_{TH} + 4\Delta$$

Minimal V_{DD} at least V_{GS} increased

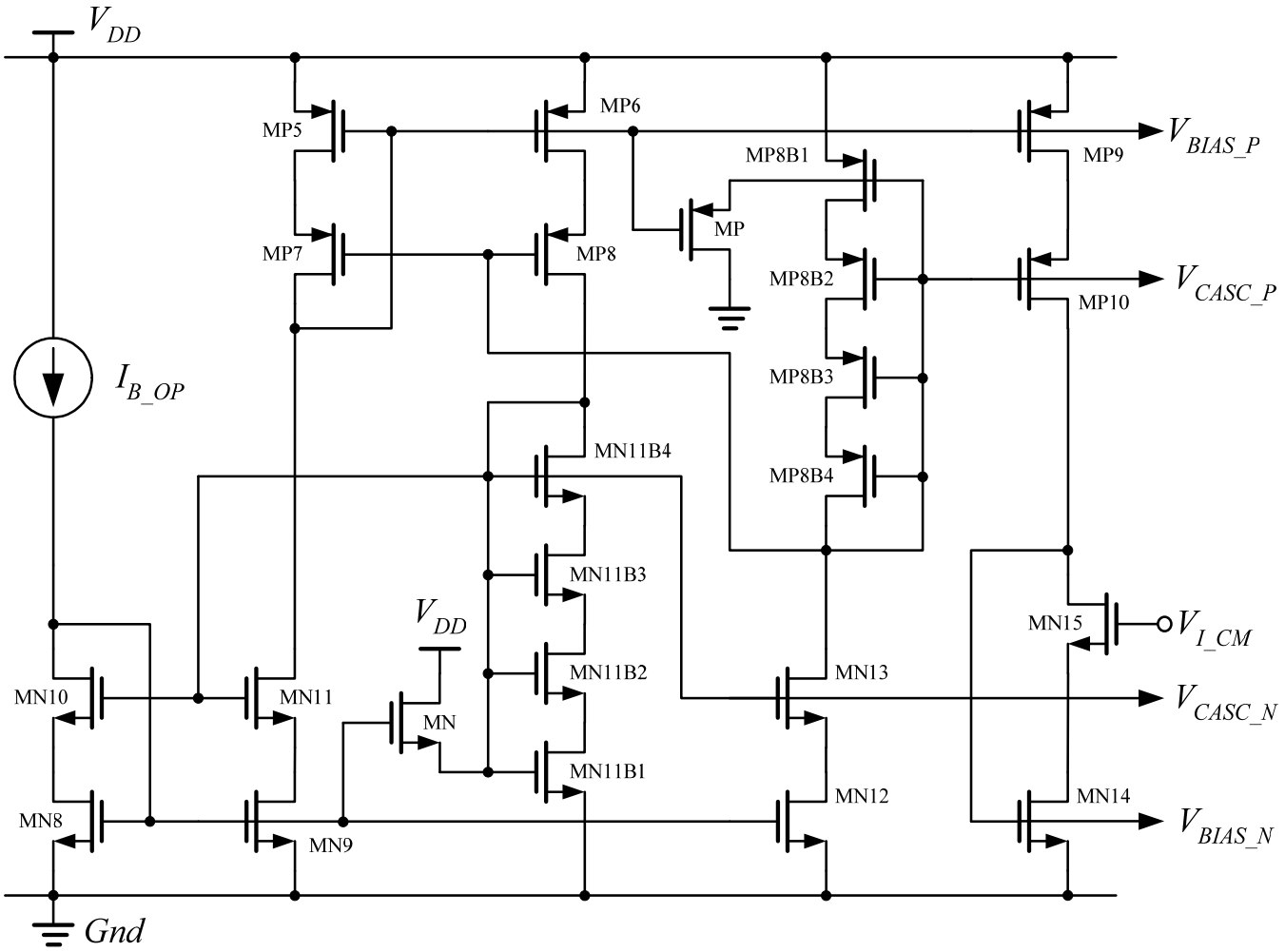
Cascode used in Self-Biasing Circuits

Start up: inject current to charge the gate voltage including cascode transistor.



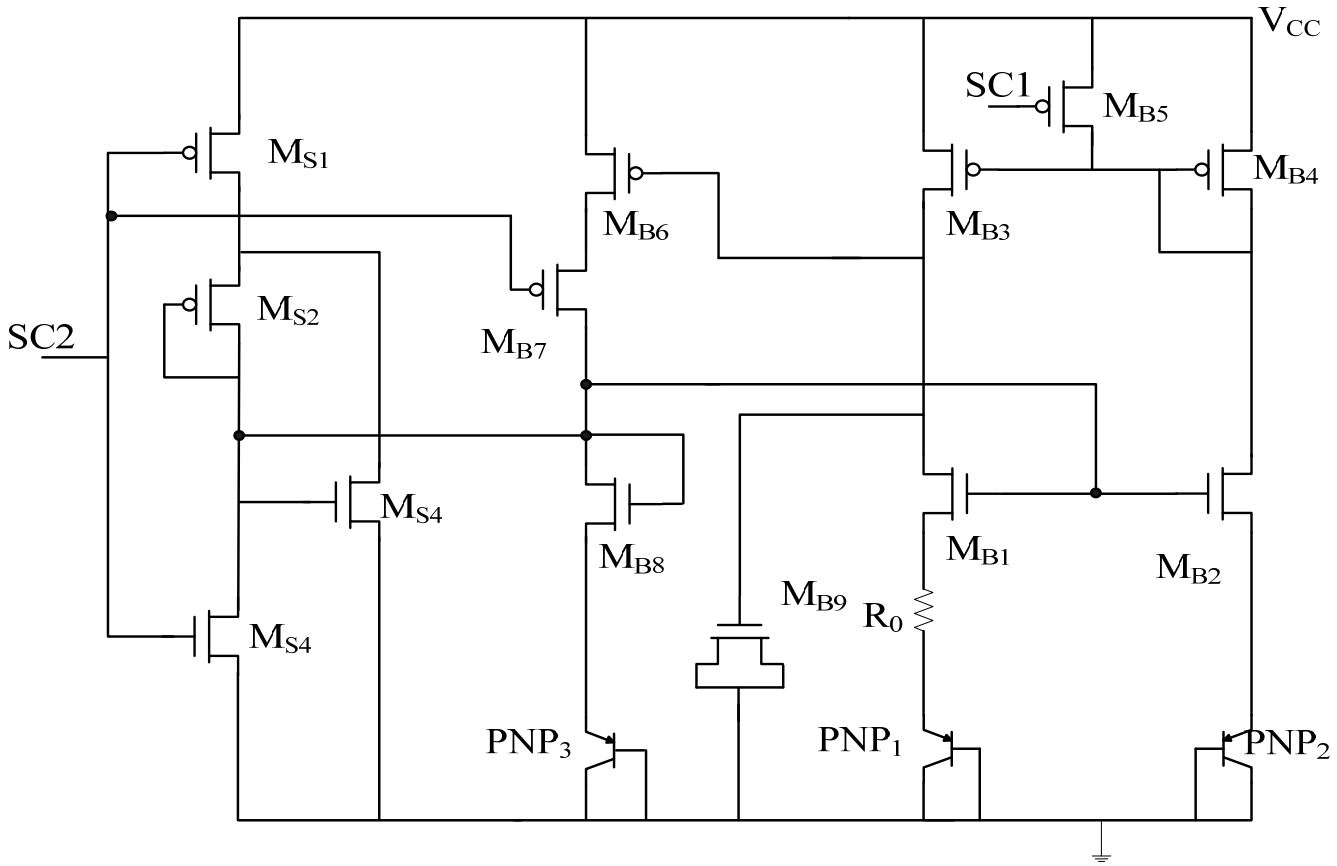
Both current generation and transportation accuracy are well improved! But more difficult in start up due to cascode structures.

Cascode Biasing Voltage Generation



Using basing current to generate Cascode voltage

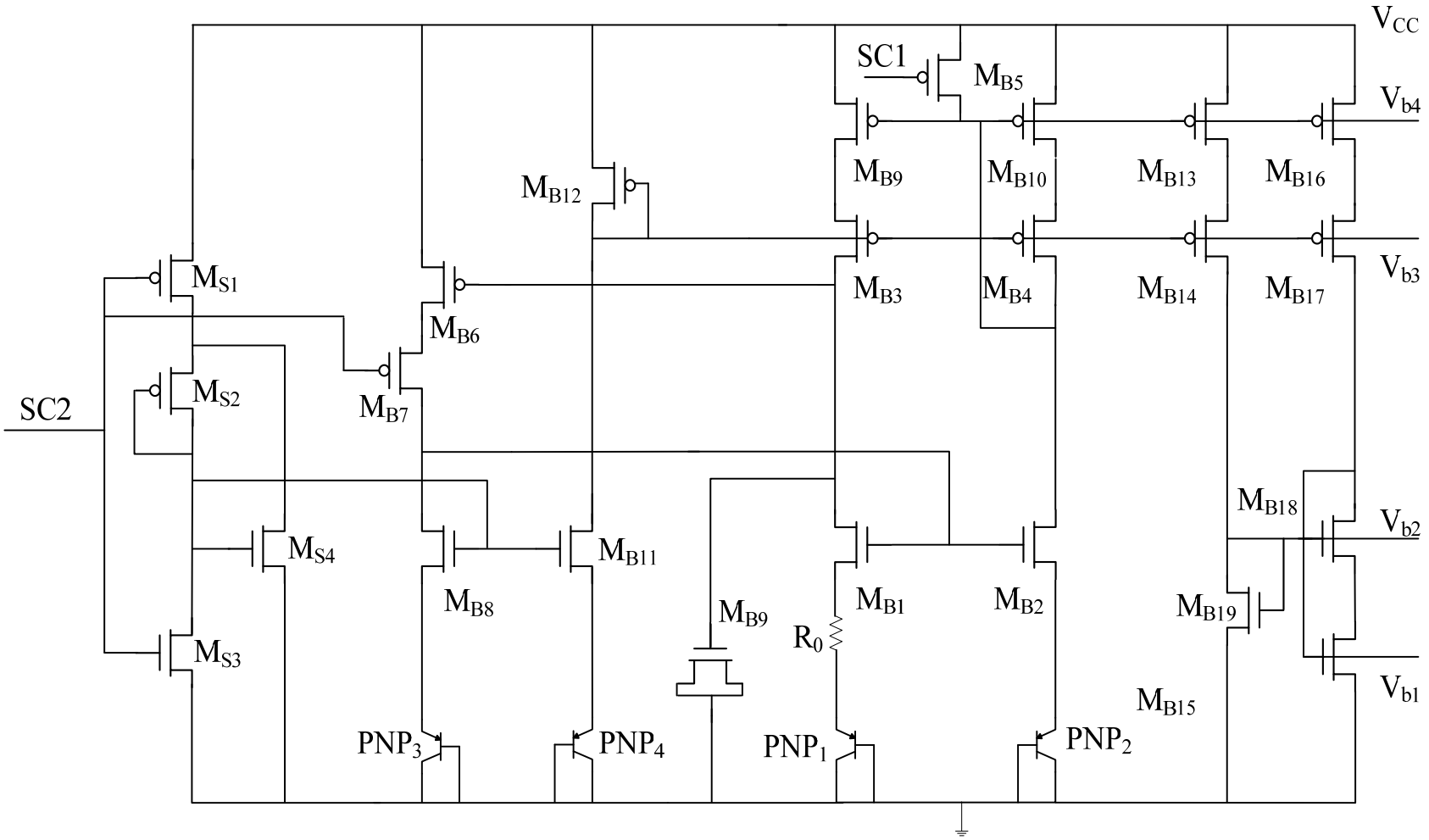
Three branch coupled biasing



Obvious change in impedance driving : Low (CM) → high (Gain)

Three branch coupled biasing with Cascode

SE
NANJING



Summary

Relation between CM & Biasing;

Single branch R+R, R+MOS diode typed biasing;

Two branches coupled Self biasing:

- NL-CM + L-CM Coupled (horizon);
- Low + High impedance coupled (Vertical)
- V/R & ΔV/R current definition and NL induced.

Multi-branched coupled, high impedance driving.

Start up problem: Time variable and NL effects.

End of Unit 2