A High-Power Packaged Four-Element X-Band Phased-Array Transmitter in 0.13-μm CMOS for Radar and Communication Systems

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***Abstract*—This paper presents a four-element X-band phased-array transmitter in 0.13-μm CMOS. The design is based on the *all-RF* architecture and contains a 5-bit phase shifter (lowest bit is used as a trim bit), 4-bit gain control (to reduce the rms gain error), and power amplifiers capable of delivering a $P_{\rm SAT}$ of 13.5 dBm per channel at 8.5–10.5 GHz. The chip can be used in the linear mode for communication systems and in the saturated mode for frequency-modulated continuous-wave radar systems, and therefore, extensive analysis is done on the phase shifter distortion versus input power. Spectral regrowth and error vector magnitude measurements indicate that the chip can support at least 20-MSym/s quadrature phase-shift keying and binary phase-shift keying modulation at an output power of +5 dBm per channel. Packaging techniques based on chip-on-board and quad flat no-lead (QFN) modules have been implemented with the four-channel chip, and both show a nearest neighbor coupling of −30 dB at 8–10 GHz, limited by bond-wire coupling. The chip dimensions are 2.9 × 3.0 mm^2 and it consumes 870 mW from 2- and 3-V power supplies.**

***Index Terms*—Beamforming, CMOS integrated circuits (ICs), IC packaging, phase shifters, phased arrays.**

I. Introduction

SILICON phased-array RF integrated circuits (RFICs), based on SiGe and CMOS technologies, have been well demonstrated at X/Ku-band using the *all-RF* beamforming approach, in the receive, transmit, and transmit/receive modes [1]–[10]. SiGe and CMOS offer multiple RF front-ends on a single chip, together with all the necessary digital control electronics, which results in a space savings per unit cell as compared to a GaAs solution [11]. This allows for the construction of compact X/Ku-band phased-arrays using standard printed-circuit board techniques at a great reduction in cost and increase in reliability, either using chip-on-board (CoB) or quad flat no-lead (QFN) packaging techniques [5], [10], [12]–[14].

This paper presents an X-band four-element phased-array chip built using 0.13-μm CMOS technology and with moderately high power levels from each channel ($\sim$ 13 dBm). The chip is intended for dual operation: A radar mode at 9–9.5 GHz for frequency-modulated continuous-wave (FMCW) perimeter detection and a communication mode at 8.2–8.7 GHz for binary phase-shift keying (BPSK) and quadrature phase-shift keying (QPSK) satellite systems. The chip is therefore characterized at saturated power levels for the radar mode and at $P_{\rm 1dB}$ and associated backoff power levels in a communications mode where attention is placed on distortion versus power levels. The four-element chip has been packaged using CoB and using QFN solutions. The mutual coupling between the bond-wires are taken into account together with the passive baluns on the CMOS integrated circuit (IC), and the resulting channel-to-channel coupling simulation is done using Ansoft HFSS [15]. A comparison is presented between the two solutions in terms of isolation between the channels and ground inductance effects. To our knowledge, this is the first demonstration of a packaged

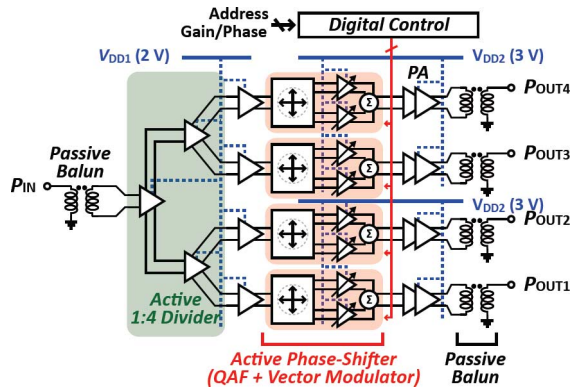

Fig. 1. Block diagram of four-element phased-array transmitter.

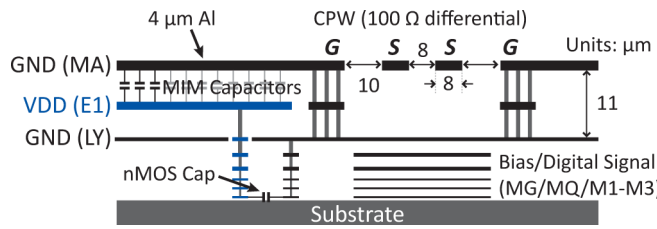

Fig. 2. Metal stack-up of IBM8RF 0.13-μm CMOS process.

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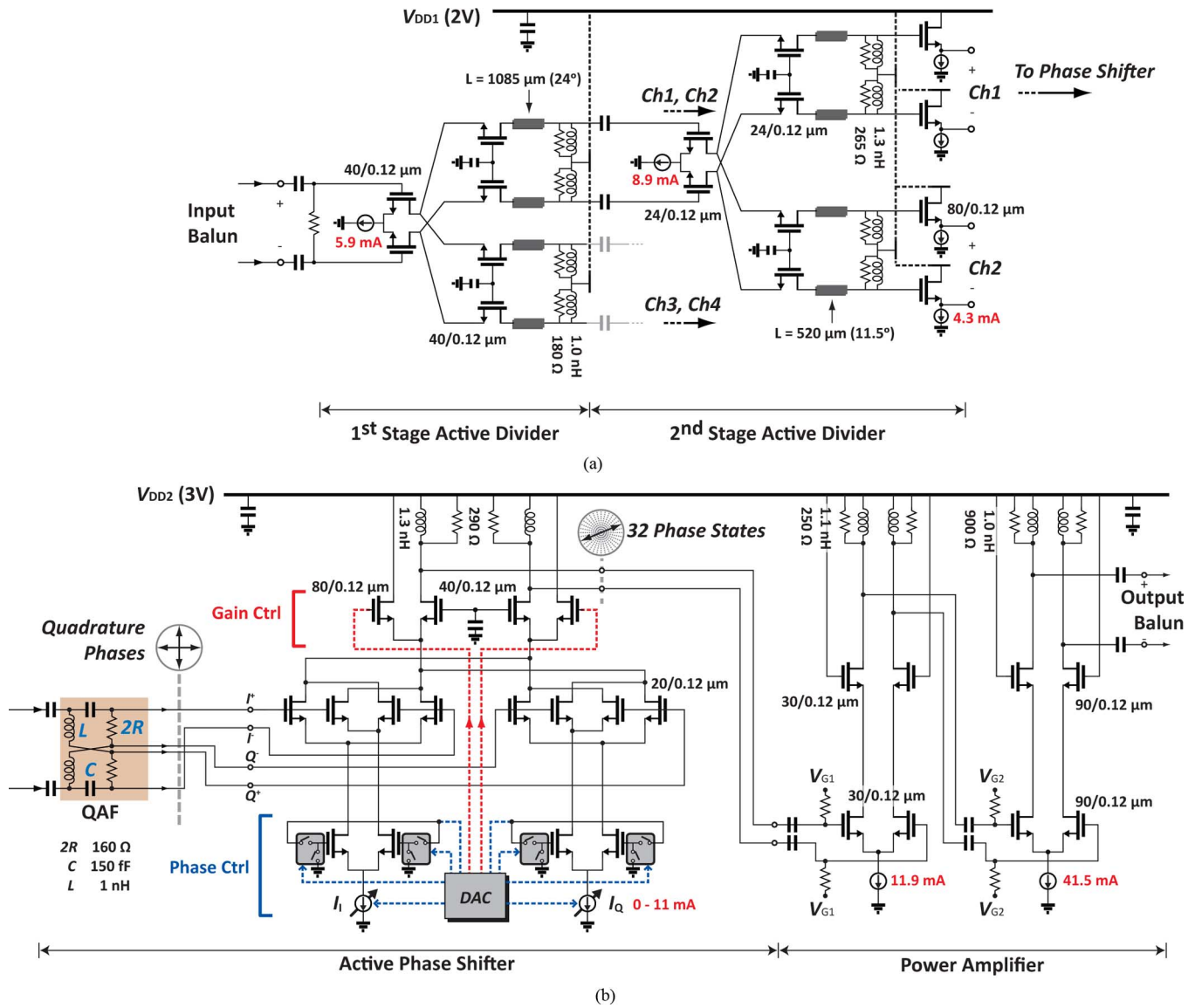

Fig. 3. Circuit schematic of a single-channel: (a) active 1:4 divider and (b) phase shifter and PA.

phased-array transmitter chip for radar and communication systems.

II. Design

A. Block Diagram and Technology

Fig. 1 presents the block diagram of the four-element transmit phased-array chip. The circuit design is differential, but baluns are used at the input and output ports since single-ended ports are compatible with microstrip or coplanar waveguide (CPW) circuits on the printed circuit board (PCB). Two independent power supplies are used on the chip. The input power divider and buffer amplifier are driven using a 2-V supply, while the active phase shifter and output power amplifier (PA) are driven using a 3-V supply. Two different 3-V power supply lines are also used, each driving a two-element subarray so as to reduce the coupling between the elements and also to reduce the current draw from the supply pins. The use of several supply pins, each with its own off-chip decoupling capacitors, isolate the different areas of chip from the large current swings encountered in the PA circuits.

The chip is built in a low-cost 0.13-μm CMOS technology with an f_T of 100 GHz and $\mathrm{NF}_{\min}$ of 0.8 dB at a bias current density of 0.1 mA/μm (IBM8RF) and with eight metal layers (Fig. 2). Differential transmission lines are implemented in a grounded coplanar waveguide (G-CPW) configuration with dimensions of 10/8/8/8/10 μm and a simulated loss of 0.22 dB/mm at 9 GHz. Note that the IBM8RF process allows for 11 μm of oxide between the MA and the LY layer, which results in relatively wide and low-loss differential lines.

All inductors and transmission-line connections are simulated using a 2.5-D electromagnetic solver (Sonnet [16]) and have Q of 12–15 at 9–10 GHz depending on the design. The capacitors are implemented using the library metal–insulator–metal (MIM) capacitors.

TABLE I
VECTOR MODULATOR I/Q DC CURRENT LEVEL

	I_I (mA)	I_Q (mA)
0 °	10.7	0
22.5 °	9.8	1.0
45 °	5.5	5.5
67.5 °	1.0	9.8
90 °	0	10.7

B. Active 1:4 Divider

An active 1:4 divider is used after the input balun and is based on a two-stage cascode divider with inductor/resistor (LR) loads for wideband operation [see Fig. 3(a)]. The input stage should be capable of handling $\sim$ 0 dBm of input power (-1.7 dBm after the balun), and is biased at 5.9 mA. The second stage feeds a source-follower amplifier with an output impedance of 54 Ω so as to drive the low-impedance quadrature all-pass filter (QAF) network [17]. The active 1:4 divider consumes 25 mA and has an electronic gain of 1.5 dB at 9 GHz, where the gain is defined as the power in the 54-Ω load (differential) at the output of a source follower divided by the available power at the single-ended port from a 50-Ω source. The simulated output power and phase versus input power is shown in Fig. 4 with an input $P_{1\mathrm{dB}}$ of -5 dBm, limited mostly by the first-stage active divider. Still, the 1:4 divider can deliver -2 dBm at the QAF $(350\ \mathrm{mV_{peak}})$ for an input power of 0 dBm, and with low phase distortion $(\sim 2^\circ)$.

C. Active Phase Shifter

The QAF is designed for a $Zo = \sqrt{L/C} = 80\ \Omega$ with $L = 1.0$ nH, $C = 150$ fF and $R = 80\ \Omega$ and provides a very wide-band quadrature with $< \pm 3^\circ$ phase variation at 6–10.5 GHz, including the effect of the capacitance loading of the vector modulator stage ($C_{\mathrm{Load}} = 30$ fF). A $Zo = 80\Omega$ is chosen as a compromise between the effect of capacitive loading in the in-phase/quadrature (I/Q) network ($Zo > 100\Omega$) and power consumption in the circuit ($Zo < 60\Omega$) [17]. The simulated QAF voltage gain is 1.5 dB including the capacitive load, and with $\leq$ 3.6-dB error between the I and Q outputs at 9 GHz (Fig. 5). A lower amplitude error can be designed using a QAF with $Z_O = 40\ \Omega$, but at the expense of lower gain (or higher current) in the active divider.

The QAF feeds a vector modulator phase shifter with integrated gain control and wideband *RL* loads [see Fig. 3(b)]. The switches at the bottom select between the I+ and I− quadrants (and Q+ and Q− quadrants), and the gain of the I and Q paths is controlled using a 5-bit DAC. The requirements are a 4-bit phase shifter, but an additional bit is used as a trim bit to improve the rms phase error (if needed). The DAC currents are optimized to take into account the interconnect parasitic effects (modeled using Sonnet) and are listed in Table I for 0°, 22.5°, 45°, 67.5°, and 90°. In addition, a 5-dB gain control stage is placed on top of the phase shifter using a current steering mode. This gain stage also uses a 3-bit control voltage from the DAC and is employed to reduce the rms gain error in the phase shifter. This is done by controlling the gain by ±2 dB in eight steps (0.5 dB/step) so as to compensate for the phase shifter gain variation. Note that this gain control method is useful for a 0–5-dB range due to current starving effect in the main RF path transistor.

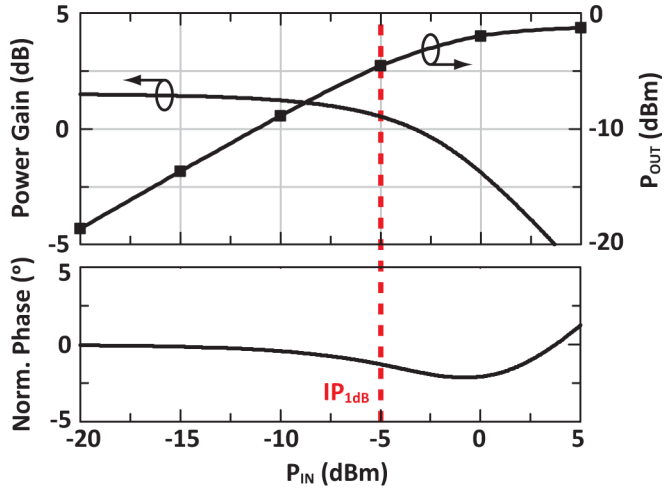

Fig. 4. Simulated power gain and output power, and normalized phase versus input power of active divider at 9.0 GHz.

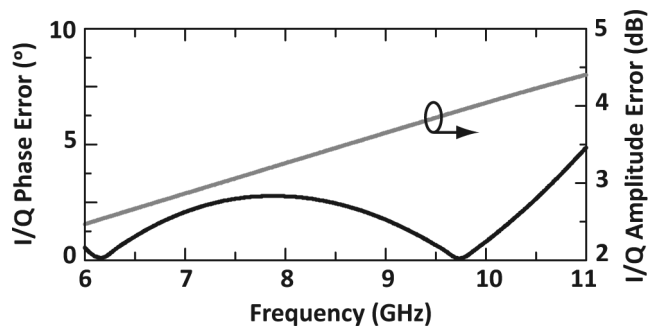

Fig. 5. Simulated I/Q phase and amplitude error of the all-pass network.

The phase shifter consumes 11.5 mA of current from a 3-V supply and has a simulated voltage gain of 5.6 dB, an input $P_{1\mathrm{dB}}$ of 6.7 dBm, and a noise figure of 12 dB (gain values can change by ±1.5 dB versus phase state). However, since this chip will be operated under high drive powers, it is important to study the gain and phase distortion versus input power. The gain follows the usual compression curve, but the phase starts to distort at an input power of > -10 dBm for 22.5°, 45°, and 67.5° phase states [see Fig. 6(b)]. This is because compression begins for different input power levels for the I- and Q-path transconductance stages. For the 22.5° *phase* state, the linearity of the Q-path transconductance stage is much smaller than the I-path due to the lower dc bias current ($I_I = 9.8$ mA, $I_Q = 1$ mA). As a result, the amplitude mismatch between the I/Q ac currents combined at the load (i_I and i_Q) increases at higher input power even though the power is less than $IP_{1\mathrm{dB}}$ [see Fig. 6(a)], and hence, an output phase error occurs.

Still, for radar operation operating at P_{SAT}, the input power of the active phase shifter is -2 dBm from the 1:4 active divider, and the resulting phase distortion at different phase states are $< 15^\circ$, which can be calibrated out using the additional trim bit in the DAC (see Section III-B).

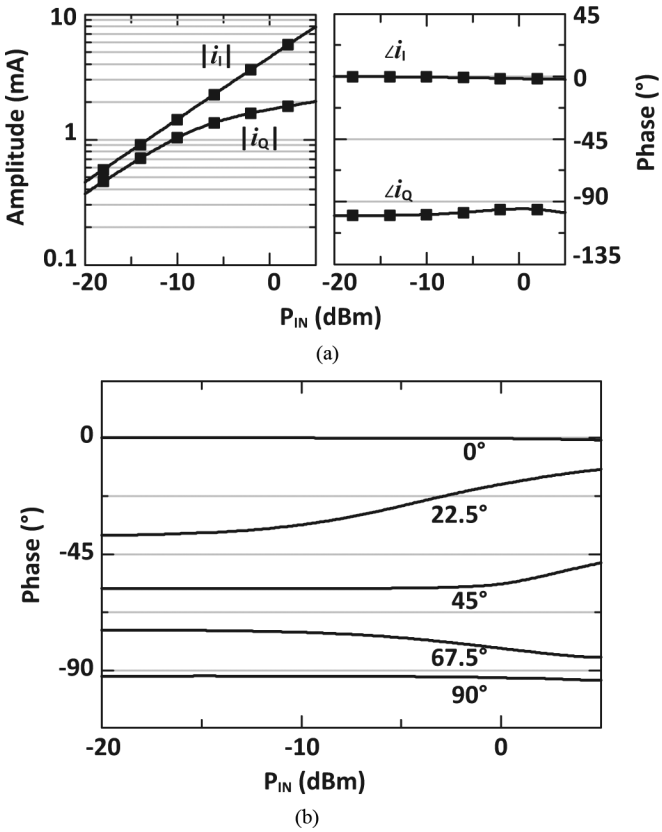

Fig. 6. Simulated: (a) i_I and i_Q at 22.5° phase state and (b) phase versus input power defined at the QAF input port.

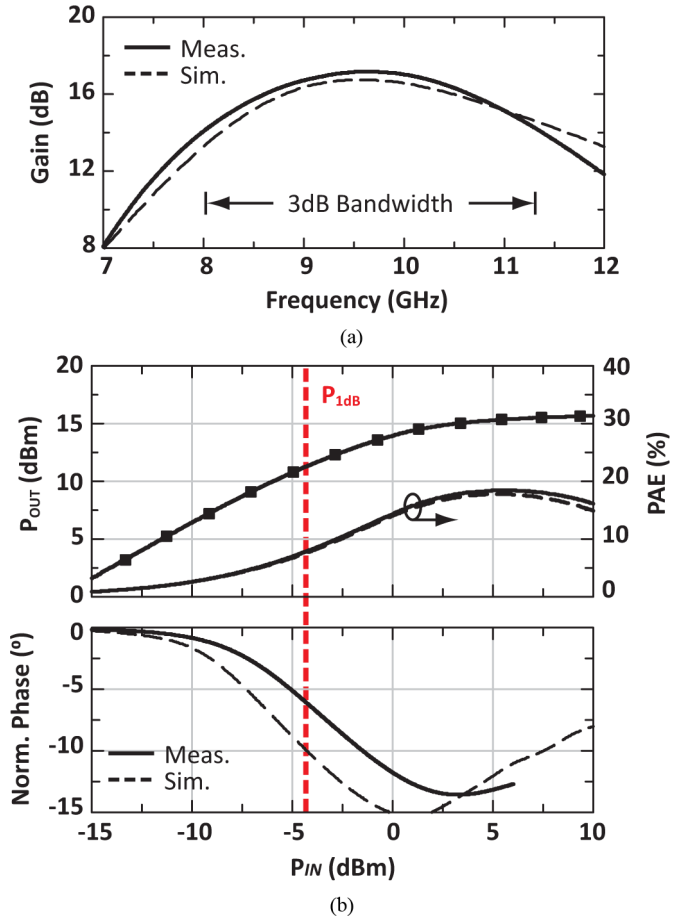

Fig. 7. Measured and simulated PA: (a) gain and (b) output power, PAE, and phase distortion versus input power.

D. Power Amplifier (PA)

The PA is a two-stage cascode design with a total bias current of 53.4 mA from a 3-V supply. The bias conditions of the first and second stages are optimized as class A and class AB, respectively. Since this is a relatively high PA with $P_{\rm SAT} = 15$ dBm, the selection of the transistors and their layout is essential for proper operation. In this design, transistors with $W/L = 30/0.12$ μm and $90/0.12$ μm for the first and second stages, and the interconnects are modeled using Sonnet. The inductors are designed with a 9-μm-wide line for improved Q ($\sim$ 14 at 9.5 GHz) and the layout is entirely symmetrical with top and bottom inductors. The edge-to-edge separation between the first and second stage inductors is > 100 μm, which also ensures a coupling of < -30 dB. Resistors with values of 250 and 900 Ω are used in parallel with 1–1.1-nH inductors for wideband operation and stability at $f > 12$ GHz. The simulated small-signal gain is 17 dB at 9.5 GHz with differential output impedance of 100 Ω.

The measurements of the PA are presented here for completeness and since they do not fit in the phased-array measurement section. The PA was tested on an individual breakout chip with the input and output balun losses de-embedded. Measurements indicate a gain of $\sim$ 17 dB with a 3-dB bandwidth of 8.1–11.3 GHz [see Fig. 7(a)]. The measured $OP_{\rm 1dB}$ and $P_{\rm SAT}$ are 11 and 15.5 dBm, respectively, at 9.5 GHz and with a peak PAE of 19% (Figs. 7(b) and 8). Note that there is an AM to PM

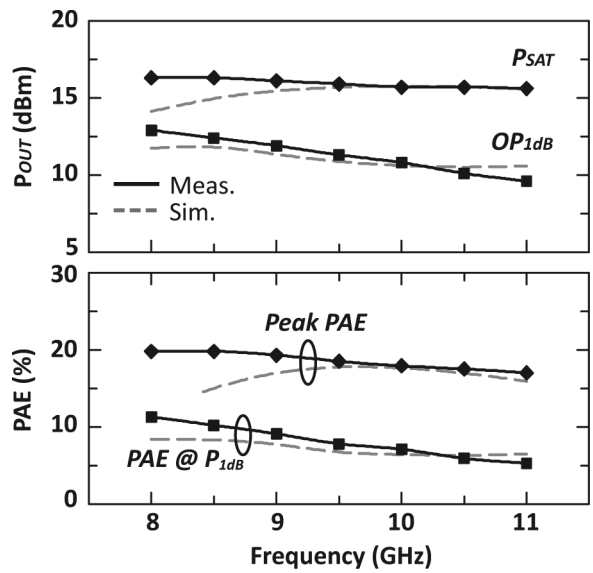

Fig. 8. Measured and simulated PA output power $P_{\rm SAT}$, $P_{\rm 1dB}$, and PAE versus frequency.

distortion of $-5°$ and $-12°$ at the $P_{\rm 1dB}$ and $P_{\rm SAT}$ powers, respectively, and again, this can be calibrated out for radar application (see Section III-B). Finally, the measured output second and third harmonic levels are at -32 and -60 dBc for $P_{\rm SAT}$

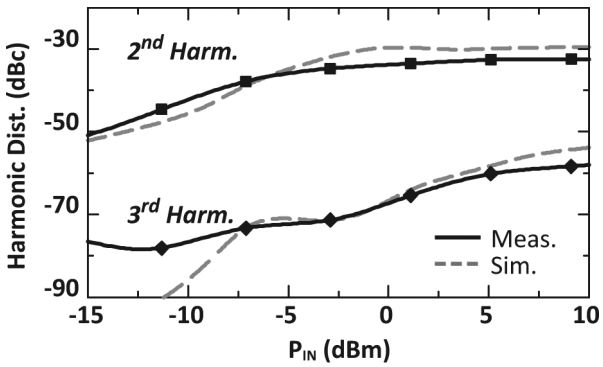

Fig. 9. Measured and simulated PA second and third harmonic components versus input power at 9.0 GHz.

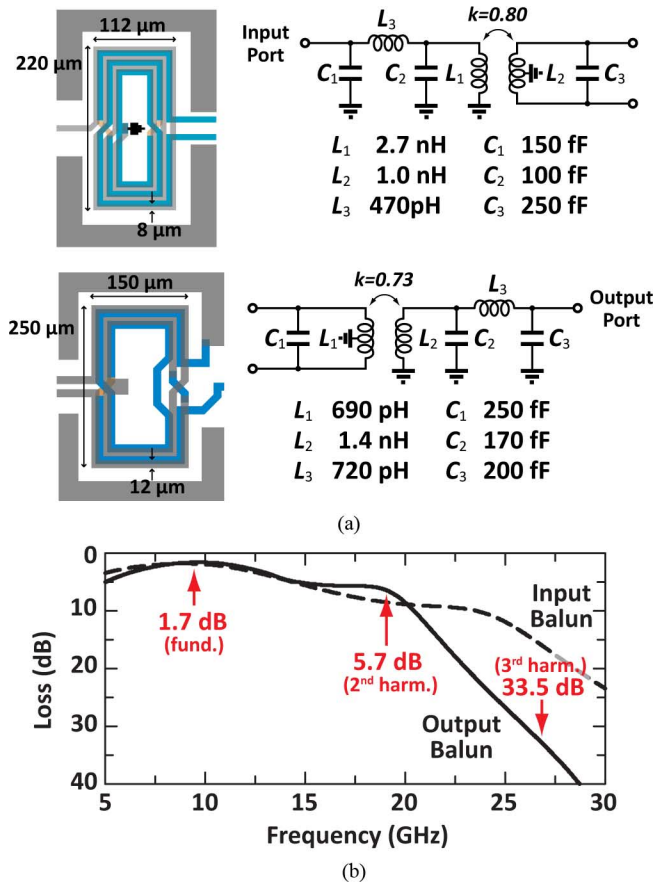

Fig. 10. (a) Input and output baluns with wideband matching network and (b) simulated frequency response.

power levels (note that this include the output balun filtering effect) (Fig. 9). All measurements are in good agreement with simulations for the PA breakout, and compete well with X-band results [18].

E. Input and Output Baluns

The input and output baluns are built using vertical magnetic coupling between the top two metal layers (MA and E1) (Fig. 10). The baluns also act as electrostatic discharge (ESD) protection circuits since they provide a wideband short circuit to ground at low frequencies. An additional LC matching network (C_1 and L_3 for the input balun, and C_3 and L_3 for the output balun) is used to provide very wideband input and output impedance matching so as to result in easy bond-wire attachment and PCB matching circuits. The simulated losses of the input and output baluns are 1.7–1.8 dB at 7–11 GHz with a differential impedance of 100 Ω. Note that the output balun also provides substantial filtering at the second $(-5.7\ \text{dB})$ and third $(-33.5\ \text{dB})$ harmonic frequencies.

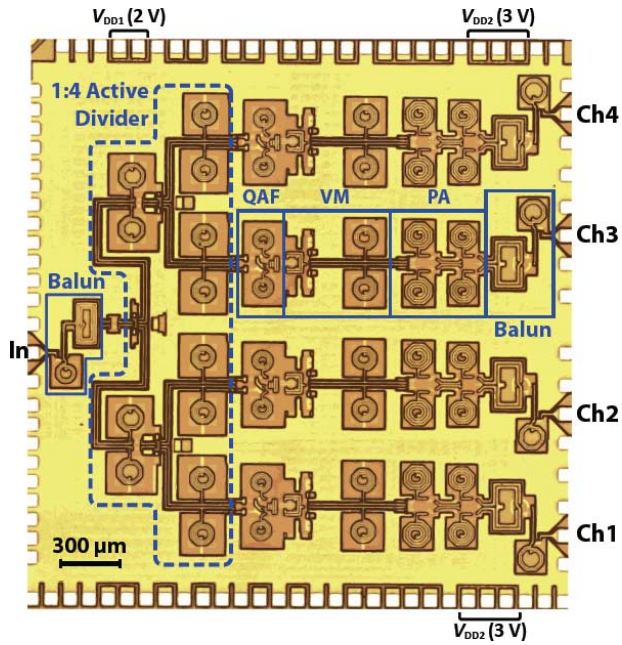

Fig. 11. Microphotograph of X-band four-element phased-array transmitter chip ($2.9 \times 3.0\ \text{mm}^2$).

F. Bias and Control

The layout is done in a symmetrical fashion and every differential stage contains a top and bottom inductor for the *RL* loads (Fig. 11). This design was preferred over differential inductors due to symmetry. The chip size is $2.9 \times 3.0\ \text{mm}^2$ and consumes 79 mA (2 V) and 237 mA (3 V) for a total power consumption of 870 mW. The 3-V supply pins are at the top and bottom of the chip to reduce the infrared (IR) drop to the PAs and for added isolation between channels 1 and 2 and 3 and 4. The V_{DD} plane covers most of the available chip area using the E1 metal layer, which is placed between MA and LY ground planes. High-density MIM capacitors $(2\ \text{fF}/\mu\text{m}^2)$ are used for supply decoupling and the total capacitance of $\sim$ 200 pF is distributed over the chip area.

The chip is controlled using a parallel interface. Each channel stores the phase and amplitude data on a 7-bit (four for phase and three for amplitude) register, and a 2-to-4 address decoder allocates the address to each register by an enabling clock signal. The digital signal routing is done using M2 or M3 and are shielded by M1 and MQ ground planes to isolate the digital switching noise from the analog path.

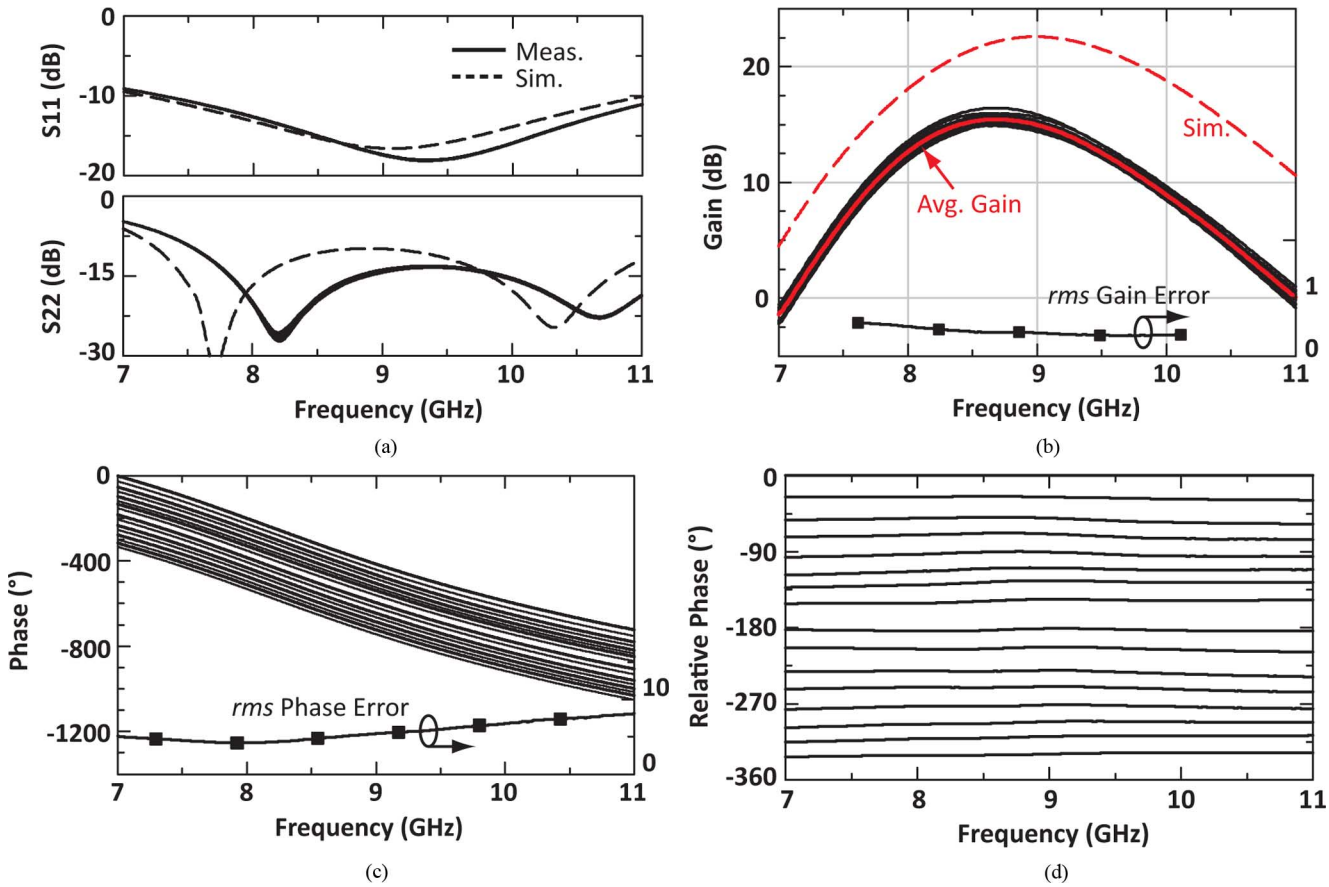

Fig. 12. Measured and simulated small-signal: (a) input and output reflection coefficient, (b) gain, (c) phase response, and (d) differential phase response (normalized to 0°) for 16 phase states for a single channel. A VGA and trim-bit were used to reduce the rms gain and phase error. Other channels had essentially the same response.

III. Measurements

A. S-Parameter Measurements: Small Signal

All measurements are done on-chip with ground–signal–ground (GSG) probes and a short-open-load-thru (SOLT) calibration to the probe tips. The bias voltages are supplied using a dc bias probe on the north and south side of the chip. No oscillations have been recorded from dc to 40 GHz, either at the RF probes or the dc probes. The chip was biased at 2 V, 79 mA, and at 3 V, 237 mA for all measurements below.

Fig. 12 presents the measured and simulated S-parameters under small-signal conditions. The measured S_{11} and S_{22} is < -10 dB from 7.5 to 11 GHz. The measured gain peak shifted from 9.0 to 8.7 GHz, and we believe that this is due to the transmission-line sections inside the 1:4 cascode divider stage (between the cascode stage and *RL* load). The 3-dB bandwidth is 7.9–9.6 GHz with a gain of 15.5 dB at 8.7 GHz, which is suitable for both communication and radar applications. The four channels showed nearly identical response ($< \pm 0.5$ dB), and therefore only one channel is shown. The amplitude and phase trim bits were used in the vector modulator in order to get a very low rms gain and phase error, as shown in Fig. 12, and with no phase cross-overs. The phase trim is a one-bit current control on the DAC, which results in an 11° phase step and can be used in addition or subtraction to the standard 4-bit setting to yield a precise 4-bit phase response. The measured gain and phase at 9.0 GHz on a polar circle is also shown (Fig. 13). Overall, except for the gain reduction, the measurements agreed well with simulations.

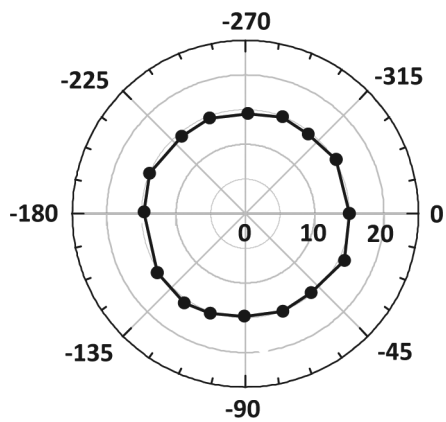

Fig. 13. Polar diagram showing measured phase and gain at 9.0 GHz.

B. S-Parameter Measurements: Large Signal

The measured output power versus input power are shown in Fig. 14(a) with a best $P_{1\mathrm{dB}}$ and P_{SAT} of 8.8 and 13.6 dBm, respectively, at 9.0 GHz. This is expected knowing that the output balun and GSG pad loss is $\sim$ 2 dB and the PA delivers a P_{SAT}

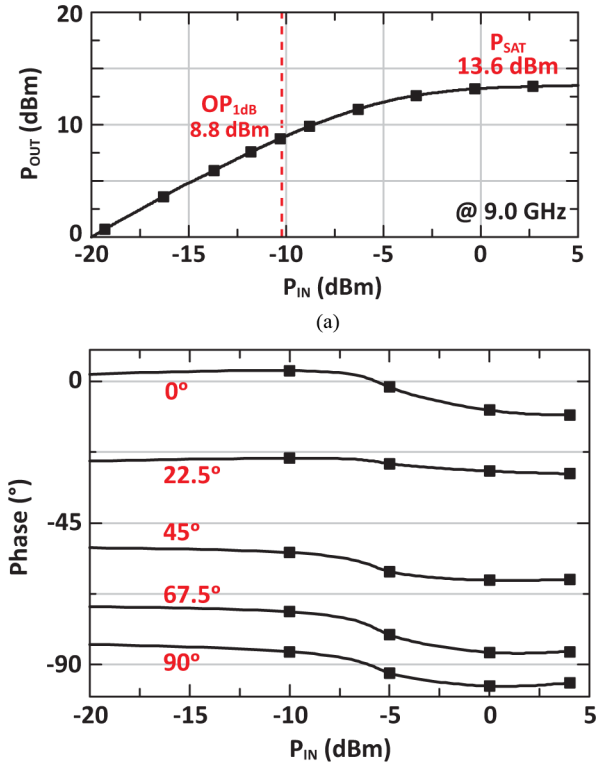

Fig. 14. Measured: (a) output $P_{1\mathrm{dB}}$ and P_{SAT} and (b) phase versus input power at 9.0 GHz. VGA set at maximum gain state.

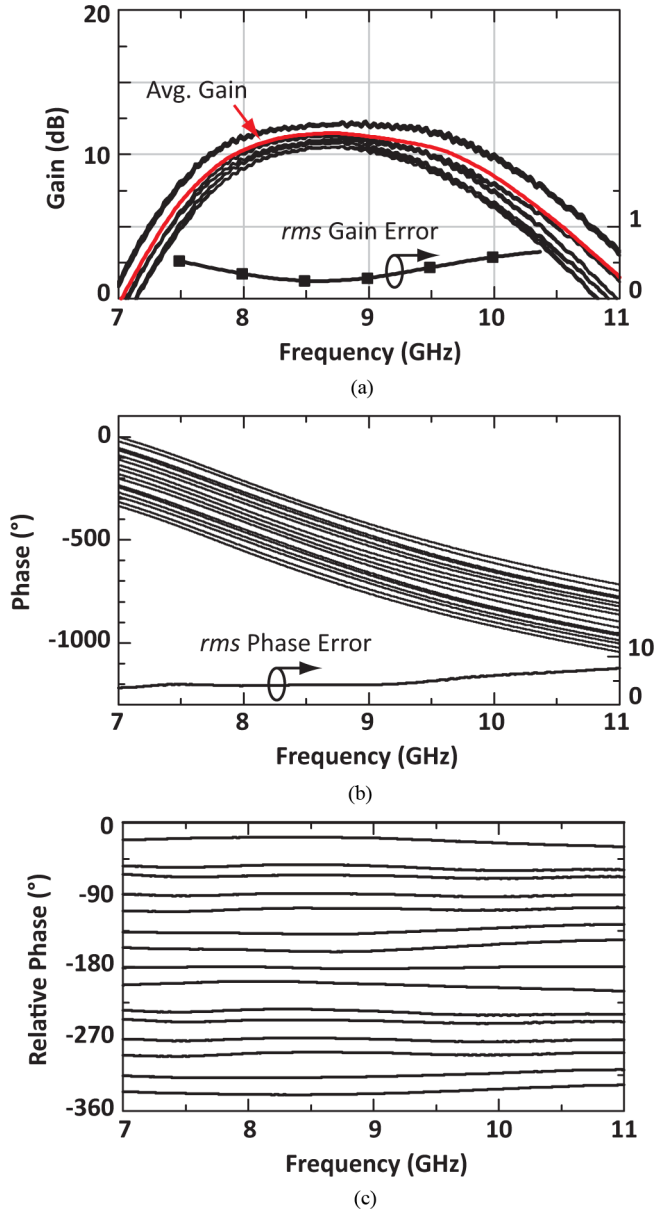

Fig. 15. Measured large-signal: (a) gain, (b) phase response, and (c) differential phase response (normalized to 0°) for 16 phase states. VGA set at maximum gain state.

of 15.5 dBm. These values are achieved at the phase state with the highest gain, and the average $P_{1\mathrm{dB}}$ and P_{SAT} over all phase states are $\sim$ 0.7–0.8 dB lower. The measured phase distortion versus power level is shown in Figs. 14(b). Note that this overall phase distortion takes into account the 1:4 active divider, phase shifter, and the PA AM-to-PM distortion components (as compared to Fig. 6, which is only for the vector modulator). This distortion can be calibrated out versus input power and has virtually no effect on the radar operation.

The measured S-parameters of a single channel at $P_{\mathrm{OUT}} =$ 12–13 dBm is shown in Fig. 15. In this case and due to the gain compression, the VGA is not used. The average gain is $\sim$ 11.5 dB (4-dB compression from the small-signal values) with a peak-to-peak variation of 1.5 dB versus all phase states and an rms gain error of 0.5 dB. The rms phase error is $\sim 4°$–$5°$ at 8.5–9.5 GHz, which is much lower than the 4-bit requirement. There are also no cross-overs in the phase shifts. The chip is therefore suitable for radar applications at 8.5–9.5 GHz with very low rms gain and phase errors, even under P_{SAT} conditions.

C. Spectral Regrowth and Error Vector Magnitude (EVM)

Fig. 16 presents the measured spectral regrowth at 8.7 GHz versus different output levels for 20-MSym/s QPSK and BPSK modulation. It is seen that an output power of up to 4–5 dBm ($OP_{1\mathrm{dB}} - 4$ dB) results in very little spectral regrowth, as expected. This is done at an input power of ~ -12 dBm, and the 1:4 active divider and the phase shifter both have virtually no phase distortion. At close to P_{SAT}, the spectral regrowth is not acceptable for communication systems. The measured EVM is 2%–2.5% up to an output power of 5 dBm, and then increases rapidly at higher P_{SAT} values, as expected (Fig. 17). The I/Q constellation for a 20 MSym/s is shown and is near ideal up to 5 dBm (Fig. 18). The EVM values are 0.5%–0.6% higher than measurements done on a PA breakout alone, indicating that the phase shifter and 1:4 active divider are contributing a small amount of additional error.

D. On-Chip Coupling

The coupling between the channels was measured according to [19] and is < -42 dB for neighboring channels at 7–11 GHz. This is due to the differential nature of the chip, and such low levels have been measured before on similar multi-channel chips [1], [2]. The coupling increases when the chip is placed

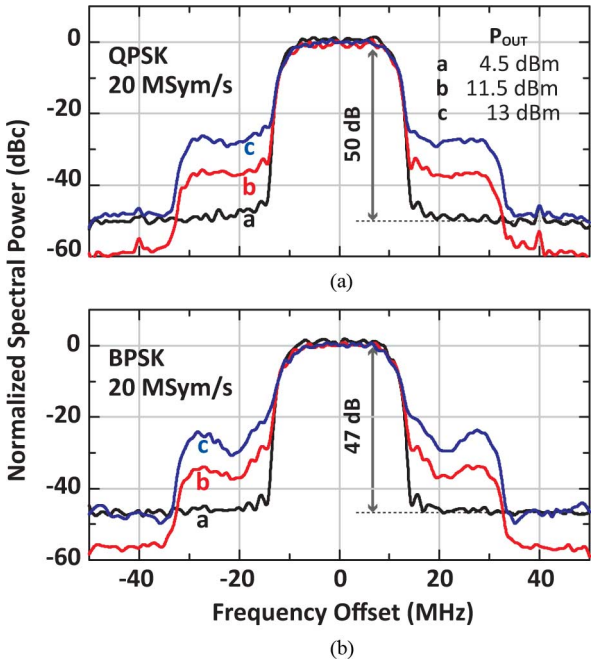

Fig. 16. Measured output spectrum for: (a) QPSK and (b) BPSK modulation at different output power levels.

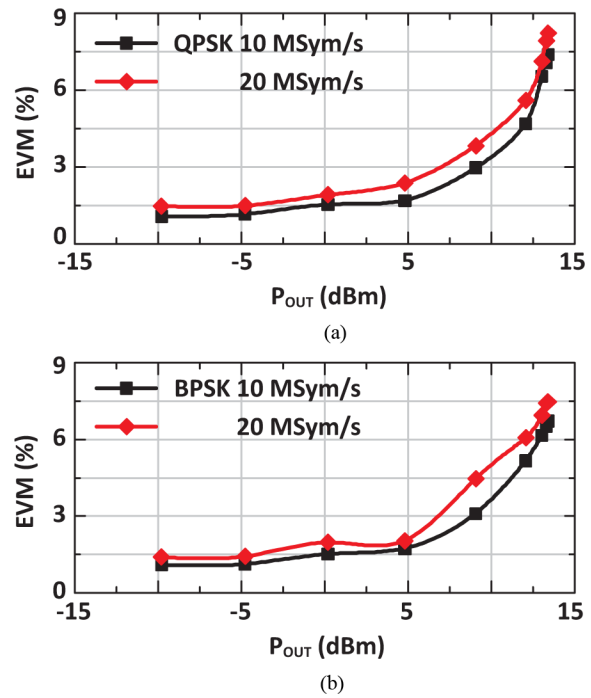

Fig. 17. Measured EVM for: (a) QPSK and (b) BPSK versus input power at 8.7 GHz.

in a package due to bond-wire and ground inductance, and this is presented in Section IV.

IV. Packaging

The four-element chip was packaged in a CoB implementation and in a 6×6 mm^2 QFN package with a standard 0.5-mm-pitch lead frame (Fig. 19) [13]. Both are assembled on a Rogers RT5880 PCB with $\epsilon_r = 2.2$ and $t = 10$ mil with a large ground

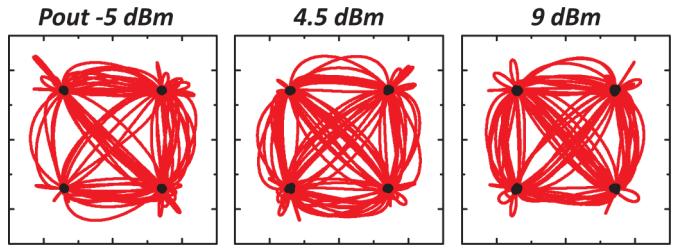

Fig. 18. Measured QPSK 20-MSym/s constellation versus output power at 8.7 GHz.

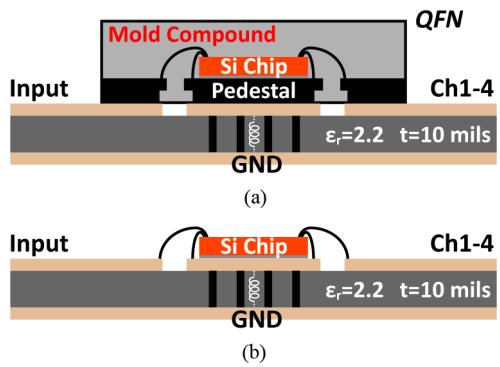

Fig. 19. Cross section of QFN package (6×6 mm^2) and CoB on a Rogers RT5880 substrate.

pad underneath the chip or QFN pedestal. A mold compound of $\epsilon_r = 4.2$, $\tan\delta = 0.015$ is used inside the QFN, but the CoB implementation does not use any glop-top material over it. Bond-wires with 1-mil diameter are used to connect the CMOS chip to the board or inside the QFN package.

The electromagnetic coupling environment between the four CMOS RFIC output ports is shown in Fig. 20 for the CoB and QFN implementations. The on-chip transformers on the silicon chip, bond-wires, QFN pedestals, transmission lines, and surrounding vias are all placed into Ansoft HFSS and modeled together. Ports 1–4 are differential on the silicon chip, while Ports 5–8 are single-ended on the PC board. Note that grounded CPW lines are used around the chip to raise the ground plane to the top PCB surface and reduce the ground-plane inductance. A maximum channel-to-channel coupling of < -34 and < -29 dB is achieved for the CoB and QFN implementations at 9 GHz [see Fig. 20(b)]. For the QFN implementation, and due to the relatively long signal and bond-wires used, two ground bond-wires are needed between the signal ports in order to get high isolation, and this is the primary reason why a 6×6 mm^2 QFN package is used (instead of a 5×5 mm^2 package). The simulated insertion loss is < -1.3 dB at 7.5–9.5 GHz due primarily to the balun loss. However, this is lower than the simulated loss of the balun itself, as shown in Fig. 10(b), due to the discretization of HFSS for such a large electromagnetic problem (finer discretization is used when simulating the balun alone).

The electromagnetic model also results in the S_{NN} at all ports and a matching network is then placed on the PC board for a 50-Ω impedance match. However, in the QFN case, the capacitance of the lead frame bond pad presents a near-perfect compensation of the bond-wire inductance at X-band ($\sim$ 0.7 nH), and a matching circuit is not needed on the PC board. For the

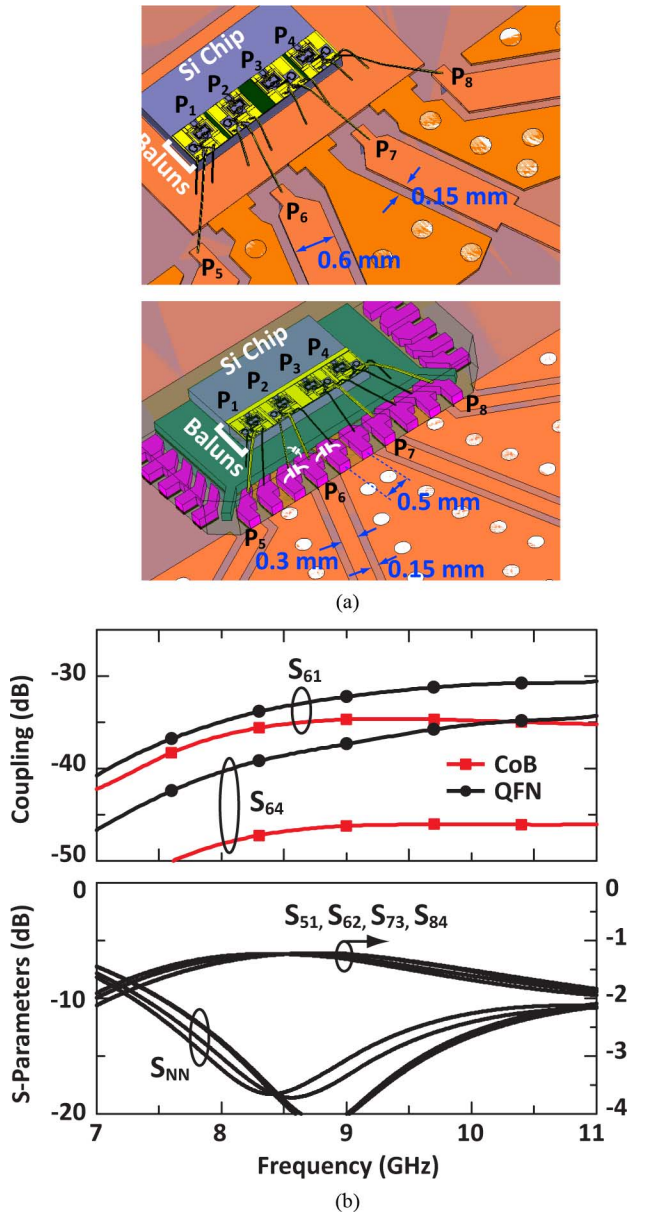

Fig. 20. (a) 3-D EM simulation setups of the silicon chip, baluns, and bond-wires in a package using HFSS. (b) Resulting S-parameters.

CoB case, a simple capacitive matching network is used. Similar impedance matching is done at the input port (not shown).

The circuit environment with a packaging effect is shown in Fig. 21. In this case, the CMOS Cadence library models are used for all circuit components, except for the input and output transformers. These are now embedded in the EM transition model, and an eight-port S-parameter matrix is used to account for the baluns and the bond-wire/package coupling effects. This model also takes into account the additional ground inductance at the balun grounds, which affects the coupling between the ports. A similar procedure is done on the input port, but in this case, it is just a two-port S-matrix for impedance matching, and no coupling is present. Additionally, power supply inductance and ground inductance are also taken due to the packaging effects. Simulations on the entire chip with ground inductance show no packaging detrimental effect (same S-parameters as

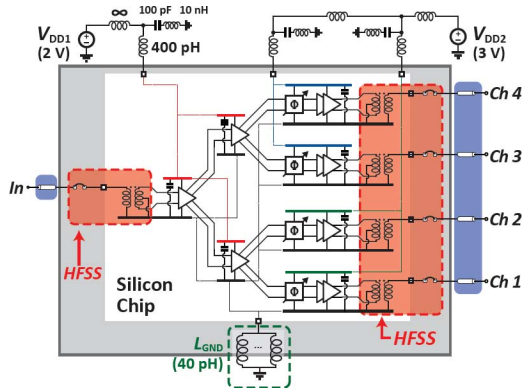

Fig. 21. Circuit environment of the packaged phased-array transmitter including silicon chip, package 3-D EM simulation, and on-board matching/distribution network with bond-wire inductances.

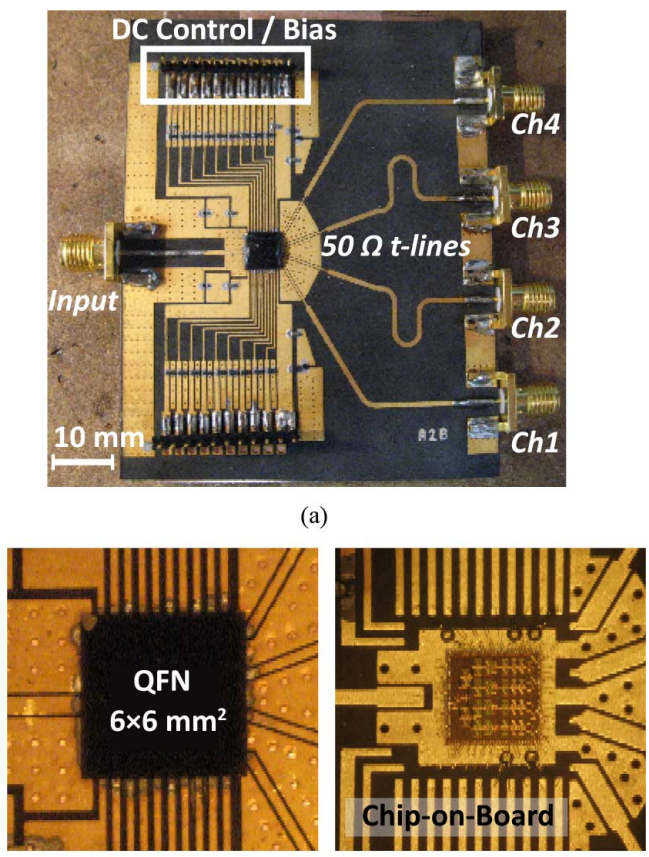

Fig. 22. Photograph of the: (a) packaged X-band phased-array transmitter on a Rogers RT5880 substrate and (b) close-in view of QFN and CoB.

Section III-A) due to the differential circuits used. Therefore, the main effect of the packaging is the electromagnetic coupling between the elements.

The CoB and QFN implementations are shown in Fig. 22 together with the entire board. Note the grounded-CPW environment around the chip with transitions to four equi-phase microstrip lines. The additional loss referenced to the SMA connectors is $\sim$ 1.4 dB at 9 GHz (2 $\times$ 0.5 dB SMA connector loss and 0.4-dB microstrip line loss). The measured S-parameters referenced to the SMA connectors are shown in Fig. 23 for the

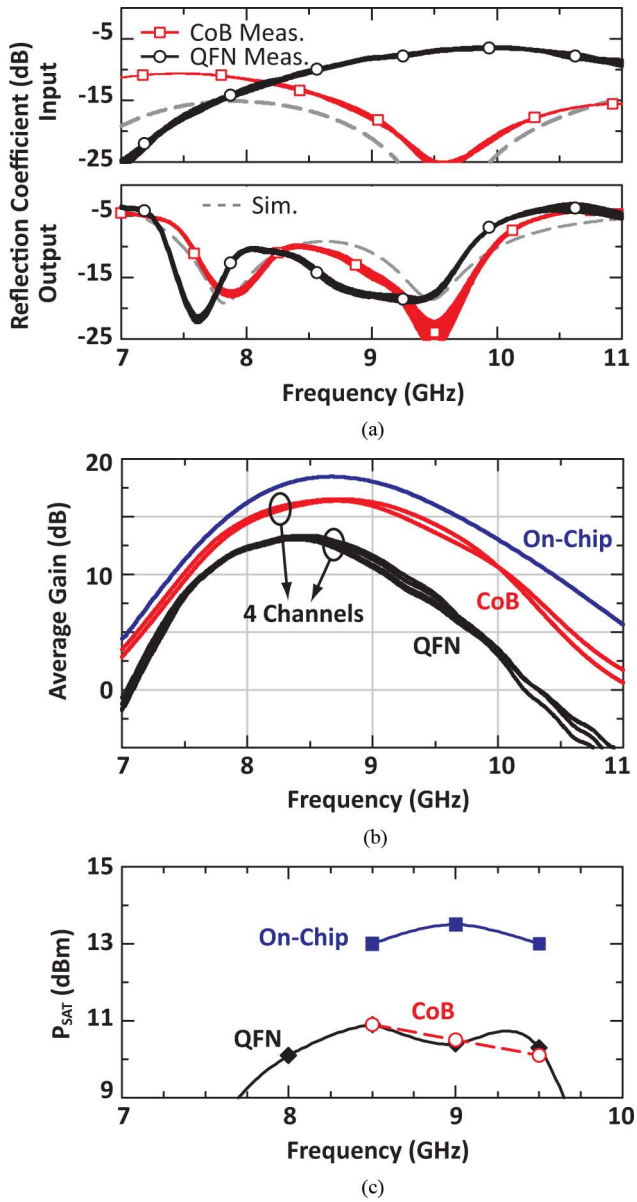

Fig. 23. Measured: (a) reflection coefficients and (b) average gain of 16 phase states and (b) P_{SAT} compared to the on-chip measurement of QFN and CoB packaged X-band phased-array transmitter.

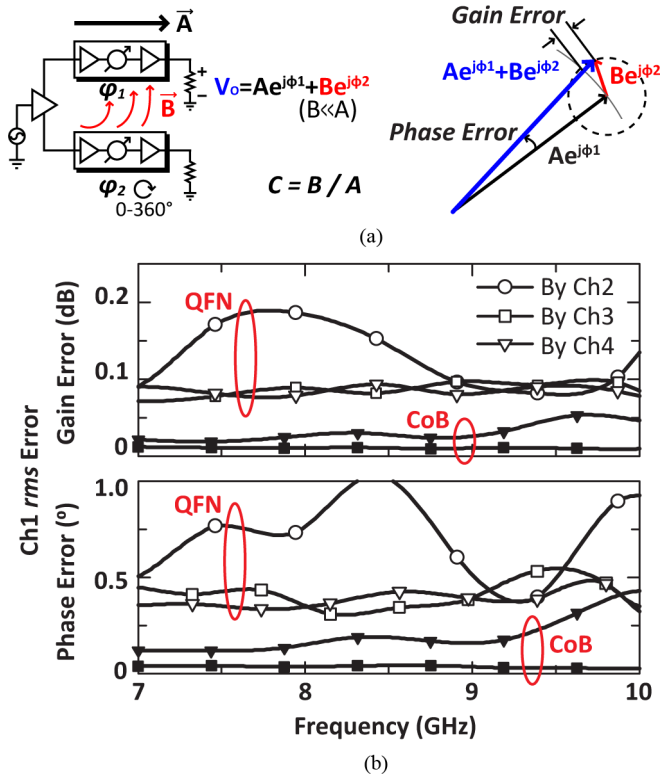

Fig. 24. (a) Vectorial representation of channel-to-channel coupling and (b) measured rms gain and phase error of channel 1 when changing the phase states of channels 2–4 in a QFN and CoB package.

TABLE II
SUMMARY OF THE PERFORMANCE

Technology	IBM8RF 0.13-μm CMOS
Frequency Band	7.9–9.6 GHz
Supply Voltage	2.0/3.0 V (analog), 1.5 V (digital)
Power Consumption	870 mW
Chip Area	2.9×3.0 mm^2
Phase Resolution	4-bit (+ trim-bit)
Gain Control	5 dB (3-bit)
Peak Average Gain	15.5 dB (Linear-mode)
	11.5 dB (Saturated-mode)
rms Gain Error	$<$ 0.5 dB (calibrated)
rms Phase Error	$<$ 6° (calibrated)
Max. Output Power (P_{SAT})	13.6 dBm (On-Chip)
	11.0 dBm (QFN, CoB)
Coupling between Channels	<-41 dB (On-Chip)
	<-29 dB (QFN, CoB)

CoB and QFN implementations. It is seen that the channels are well balanced (average gain shown for 16 phase states for each channel) and that the CoB results in slightly higher gain than the QFN implementation. There is also $\sim$ 2-dB drop in the CoB gain as compared to the average gain of a chip measured with GSG probes, which is close to the expected value of $\sim$ 1.4 dB. The QFN package showed an additional drop in gain, partly due to the high S_{11} of 8.5–10.5 GHz (from -10 to -7 dB). It is not clear why the QFN gain difference is much higher than expected at 9–11 GHz.

The measured output P_{SAT} is also shown in Fig. 23(c) and is 2.0–2.5 dB lower than the GSG probe measurements for the CoB and QFN implementations. Still, this chip delivers 11 dBm of power per channel at the output of the SMA connectors (13 dBm on-chip), which is the highest so far from a CMOS chip at X-band frequencies.

The coupling between the channels was determined by measuring the output of channel 1 at a fixed phase setting and changing the phase of channels 2–4 from 0° to 360° (one channel at a time) [19]. This results in an amplitude and phase modulation in channel 1 bounded by $(1+c)$ and $(1-c)$ in amplitude and $\pm\tan^{-1}(c)$ in phase, and can be represented as an rms gain and phase error in channel 1. For $c = 0.018 - 0.036$ (from -35 to -29 dB), the equivalent rms gain and phase error is 0.1–0.2 dB and 1°–2°, respectively [see Fig. 24(c)].

Fig. 24(b) presents the measured rms gain and phase error versus frequency for channel 1 when the phase of channels 2–4 are changed. Both the CoB and QFN resulted in nearly the same coupling for channel 2 and the QFN results are shown. As expected, the maximum coupling occurs between channels 1 and 2, with an rms gain error of < 0.2 dB and $\sim 1^\circ$ at ~ 8 GHz. This is equivalent to a peak coupling of from -29 to -30 dB, as expected from simulations. Note that QFN channels 3 and 4 show a wideband coupling characteristic of -35 dB, which may be due to V_{DD} coupling and to the silicon RFIC/package/PCB ground inductance. For the CoB, channels 3 and 4 result in a wideband coupling characteristics of -45 dB (rms gain and phase error < 0.05 dB and $< 0.5^\circ$) showing the reduced ground and V_{DD} inductance of this implementation.

V. Conclusion

This paper has presented a four-element high-power phased-array transmitter capable of operation in a communication or a radar mode and the measured performance is summarized in Table II. It has been found that the vector modulator phase shifter and the PA result in phase distortion versus power, but these can be calibrated out in radar mode operation. For communication systems, it is best to operate below the output $P_{1\mathrm{dB}}$ level for complex constellations. The chip has been packaged using CoB and QFN techniques, and the CoB results in higher ultimate isolation between the channels $(-45$ dB$)$ as opposed to the QFN $(-35$ dB$)$. However, both result in nearly the same isolation between the neighboring channels (~ -30 dB), which is primarily limited by bond-wire coupling. This work shows that complex phased arrays with multiple channels can be packaged in low-cost QFN packages for X-band applications.

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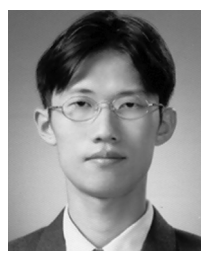

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