A Multi-Loop Low-Dropout FVF Voltage Regulator with Enhanced Load Regulation

(Invited Paper)

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***Abstract*—-This paper introduces a multi-loop fast transient response flipped voltage follower (FVF) low-dropout (LDO) voltage regulator suitable for system-on-chip (SOC) applications. While typical FVF-based LDOs exhibit fast transient response, which is critical for SOC applications, their output DC accuracy is limited due to low loop gain of the FVF. In this work, we introduce a multi-loop design aimed at improving the DC accuracy while preserving the transient performance. The LDO is implemented in a 180-nm CMOS process to provide an output voltage of 1.5V at a maximum load current of 10mA from an input line voltage of 1.8V. The designed LDO's quiescent current is 53μA at minimum load. Simulation results showcase the advantages of the multi-loop design with a transient response time of 0.73ns and a figure of merit (FOM) of 3.9ps.**

***Index Terms*—flipped voltage follower, folded flipped voltage follower, FVF, LDO, capacitor-less LDOs, SOC, low dropout, voltage regulators.**

I. Introduction

With the increase in demand for portable electronics, system-on-chip's (SOCs) with increased complexity have become widely prevalent. SOCs require several circuit blocks to implement a complete system. While incorporating different circuit blocks on a single chip, voltage regulators which require minimal area are essential for providing clean ripple-free supply rails across the integrated circuit [1], [2]. Fully-integrated low-dropout (LDO) voltage regulators are specifically used in such circumstances [3], [4]. Among many existing topologies, fully-integrated flipped voltage follower (FVF) based LDOs are an attractive topological choice due to their low output impedance, fast transient characteristic and minimal area requirements for implementing regulators for on-chip applications [5]–[7].

A single-transistor-control FVF based LDO adapted from [5] is shown in Fig. 1. The LDO consists of an error amplifier (EA), a V_{SET} generation stage and an FVF output stage. Voltage V_{MIR} is regulated by the error amplifier in order to set V_{MIR} equal to V_{REF}. The V_{SET} generation stage forms the bridge in between V_{MIR} and V_{OUT}. V_{SET} is held one V_{SG} below V_{MIR} by diode connected transistor M_7. The generated V_{SET} is used to bias transistor M_8 in the FVF stage. From Fig. 1 it can be observed that V_{MIR} and V_{OUT} are approximately equal due to the floating current mirror formed by transistors

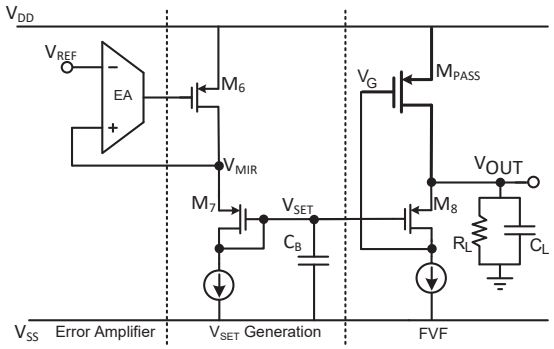

Fig. 1: Single-transistor-control FVF LDO adapted from [5].

$M_7 - M_8$. An FVF stage is used at the output of the LDO to improve transient response.

However, due to low loop gain of the FVF [8], the LDO has substandard load regulation. Poor load regulation is also because V_{OUT} is not tightly bound to V_{REF}.

Another major drawback of [5] is the limitation on minimum and maximum load current [9]. If the load is less than the minimum, the gate voltage of M_{pass} increases to reduce the overdrive voltage. This pushes M_8 out of saturation, which is undesirable for proper functioning of LDO. At high load currents the output dominant pole is in proximity with the internal non-dominant pole, leading to poor phase margin.

Another FVF implementation is done in [8], It consists of a triple-input error amplifier to improve load regulation and also employs Buffer Impedance Attenuation (BIA) technique to move the internal poles to high frequency, away from the output pole [8].

Despite the use of a triple-input error amplifier, the loop gain for the regulating loop in [8] is low, resulting in deficient load regulation. Our proposed design enhances the load regulation by introducing another loop. While the LDO in [8] has a single compensation capacitor C_B, another compensation network is introduced in the proposed design to make the LDO stable. This also results in reducing the disturbance on V_{OUT} during a load transient.

This paper is organized as follows: Section II describes implementation details of proposed multi-loop LDO. Section III presents simulated results. Conclusion and comparison with literature are discussed in Section IV.

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II. Implementation of Proposed LDO

The proposed multi-loop LDO is an enhanced version of the work presented in [8]. The LDO in [8] was implemented in a 65-nm CMOS process. However, in this work we selected a low-cost 180-nm process. In order to scale the design to a different process node, a scaling factor of the ratio of the maximum supply voltage of 180-nm core devices to those of 65-nm core devices is chosen.

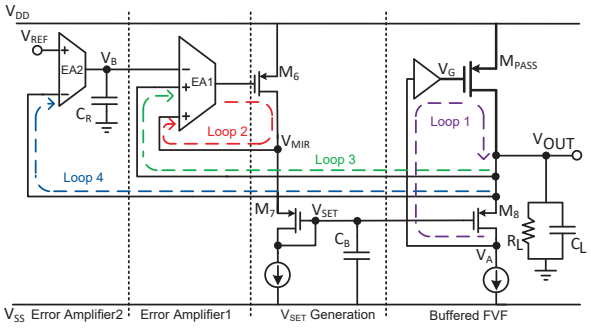

Fig. 2: Block diagram of proposed multi-loop FVF LDO.

Fig. 2 presents the block diagram of the proposed LDO. Loop 1 consists of a Folded Flipped Voltage Follower (FFVF) driving an output FVF stage. Loop 1 by itself can regulate the output voltage but exhibits poor load regulation owing to its low loop gain. The low output impedance of the FVF stage provides a high unity gain frequency (UGF) for Loop 1 [10]. This enables it to react immediately to changes in the load current. Loop 2 consists of an error amplifier (EA1) and is predominantly used to set a left-half-plane (LHP) zero which aids in the stabilization of the LDO. Another function of Loop 2 is generation of voltage V_{SET}. [8] describes that sufficient DC accuracy of the LDO is achieved through the introduction of Loop 3. Loop 3 enhances the DC accuracy through the connection of V_{OUT} to one input of the error amplifier (EA1). The proposed work introduces a second error amplifier (EA2) to enhance the load regulation through the negative feedback of Loop 4.

Fig. 3 depicts the schematic of the proposed LDO. Transistors M_1-M_5 form the triple-input NMOS differential amplifier. Transistor M_3 forms the third input for the error amplifier, allowing to feedback V_{OUT}, thereby enhancing DC accuracy. Feedback from V_{MIR} to transistor M_2 forms Loop 2, as described above. Control voltage V_{SET} required for the output FVF stage is generated using transistors M_6, M_7 and M_{15}. V_{SET} generated through the diode-connection of transistor M_7 is used to bias M_8 in the output FVF stage. A compensation capacitor C_B is required to ensure stability of the FVF LDO [8]. The BIA technique is implemented using an FFVF due to its extremely low output impedance compared to a regular voltage buffer [8], [10]. An FFVF buffer is constructed using transistors M_9-M_{13}. Introducing an FFVF reduces the resistance at the gate of M_{PASS} and the capacitance at node V_A, moving the poles at both V_G and V_A away from the output dominant pole [8].

However in the 180-nm process, higher parasitics result in an unacceptably low phase margin (PM) of Loop 1. Therefore, a compensation network Z_C formed by resistor R_C and capacitor C_C is used to improve the PM of Loop 1. To further supplement the speed of the buffered FVF stage, the parasitic capacitance associated with it is reduced by doubling the effective length of bias transistors M_{17}-M_{19}, such that size of transistors M_{11}, M_{12} and M_{14} can be halved for the same bias current. The FVF LDO's pass element is a PMOS transistor M_{PASS}.

[8] derives the relationship between its V_{REF} and V_{OUT} based on the input transistor sizing of the triple-input differential amplifier and is given by

$$\left(V_{REF} - \frac{1}{4} \cdot V_{MIR} - \frac{3}{4} \cdot V_{OUT}\right) \cdot A_{EA} = V_{OUT} \quad (1)$$

where $V_{MIR} = V_{OUT} + \Delta V$. From (1) we find that, $V_{OUT} = V_{REF} - \Delta V/4$. This states that, V_{OUT} is held close to V_{REF} than to V_{MIR}.

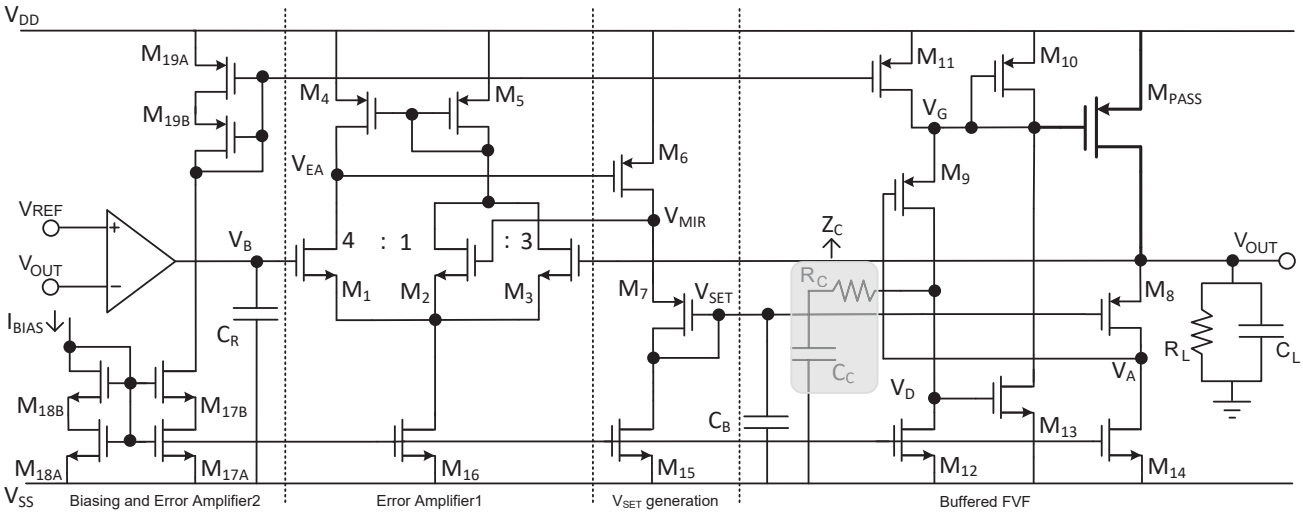

Fig. 3: Architecture of proposed multi-loop FVF LDO.

Though V_{OUT} is regulated approximately equal to V_{REF}, the low loop gain through Loop 3 limits the load regulation that can be achieved through the architecture shown in [8]. To further enhance the DC accuracy, a second error amplifier (EA2) is introduced, as shown in Fig. 3. Node V_{OUT} is fed back to the negative terminal of EA2 to form Loop 4 through the connection of node V_B to the gate of transistor M_1. An integrating capacitor C_R is required to stabilize Loop 4. The negative feedback action results in the modulation of the internal reference V_B to further improve regulation.

III. Simulation Results

The proposed multi-loop FVF LDO is designed in a 180-nm CMOS process. The supply voltage of the implemented LDO is 1.8V. The LDO is designed to provide a regulated output voltage of 1.5V across a load current range of 0μA - 10mA. The LDO consumes a total quiescent current of 93μA at maximum loading conditions. At maximum load current the simulated dropout voltage is 225mV.

A. AC Stability Analysis

AC small-signal analysis is performed on the proposed multi-loop LDO to verify its stability across the complete load range.

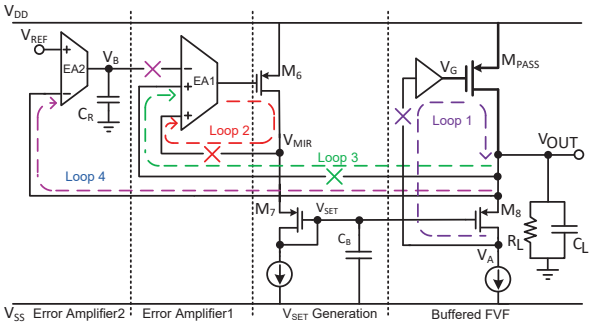

Fig. 4: Break points of individual loops for AC analysis.

In order to accurately deduce the magnitude and phase response of individual loops, each loop is broken as shown in Fig. 4. For simulating the AC response of Loop 1, it is required to break the loop at node V_A, as shown in Fig. 4. In order to accurately observe the effect of node parasitics, a parasitic loading stage is also required [5]. Another important point to note is the requirement to isolate the effects of other loops on Loop 1. Therefore to establish the DC operating point of transistor M_8, node V_{SET} is also considered as a break point for Loop 1. As such, a DC voltage source can be used to establish operating conditions for transistor M_8. Now, Loop 2 is broken at node V_{MIR} while performing AC analysis to verify the stability of Loop 2. For Loop 3, the loop's break point is at node V_{OUT}. Finally the newly-introduced Loop 4 is broken at node V_B. The magnitude and phase response of Loop 1 are shown in Fig. 5. We note that without the compensation network Z_C, Loop 1's phase margin is 6°. With the introduction of compensation network Z_C, at node V_D as shown in Fig. 3, Loop 1's phase margin improves to 26°.

The complete AC analysis summary is presented in Table I. Loop 1 exhibits the highest UGF of 180MHz, and the lowest PM of 26°. For Loop 2, a gain of approximately 52dB is achieved along with a phase margin of 82°. Loop 3's gain is reduced due to the presence of Loop 2 resulting in a low loop gain of 1.20dB, as shown in Table I. Finally, the introduced Loop 4's gain is equal to 32dB with a PM of 86°.

Loop	Loop gain (dB)	UGF (MHz)	PM (°)	Comments
1	26.5	180.5	26	DC at V_{SET}
2	51.9	31.4	82.18	Open: Loops 3, 4
3	1.20	1.24	86.4	Open: Loop 4
4	32	0.38	86.31	-

TABLE I: Summary of AC analysis of individual loops at load current of 10 mA.

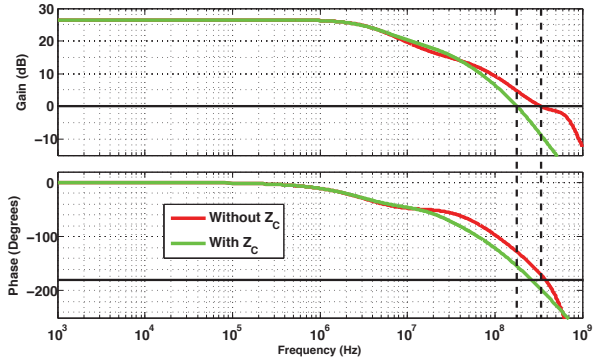

Fig. 5: Magnitude and Phase response of Loop 1 with and without compensation network Z_C.

B. Transient Analysis

The implemented LDO's transient performance is characterized through a load transient simulation. A load transient step of 0μA to 10mA is provided at the output node V_{OUT} of the LDO with a rise time of 10ns. The response of the LDO is measured in terms of ΔV_{OUT}, recovery time T_R, and load regulation. The LDO's load transient response is shown in Fig. 6. The proposed LDO achieves a transient response time (T_R) of 0.73ns, while exhibiting a DC load regulation of 0.031mV/mA.

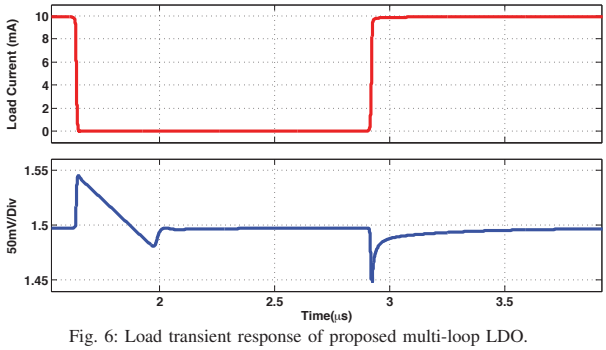

Fig. 6: Load transient response of proposed multi-loop LDO.

IV. Discussion and Conclusion

A multi-loop FVF LDO is proposed with improved load regulation. A DC regulation loop (Loop 4) is introduced to

Publication	[11] JSSC 2005	[12] JSSC 2012	[1] TCAS-I 2014	[7] TCAS-I 2014	[8] TCAS-I 2015	[13] EL. 2016	This Work
C_L	On-chip						
Technology	90-nm	45-nm SOI	0.35μm	65-nm	65-nm	28-nm	180-nm
Vout	0.9V	0.9 to 1.1V	1.2V	1V	1V	0.8V	1.5V
Drop out	300mV	85mV	600mV	200mV	150mV	200mV	225mV*
I_Q	6mA	12mA	44μA	23.7μA	50 to 90μA	100μA	53 to 93μA
I_{max}	100mA	42mA	12mA	50mA	10mA	10mA	10mA
Total Cap.	600pF	1.46nF	100pF	27pF	140pF	120pF	153pF
$\Delta\ V_{OUT}@T_{EDGE}$	90mV@100ps	N/A	105mV@500ns	40mV@100ns*	82mV@200ps	26mV@30ps	48mV@10ns
DC Line Reg.	882mV/V**	27mV/V**	0.28mV/V	8.89mV/V	37.1mV/V	NA	24mV/V*
DC Load Reg.	0.9mV/mA	0.083mV/mA	0.68mV/mA	0.034mV/mA	1.1mV/mA	NA	0.031mV/mA*
T_R	0.54ns	0.309ns*	N/A	N/A	1.15ns	312ps	0.73ns*
FOM	32ps	62.4ps*	N/A	N/A	5.74ps	3.12ps	3.9ps*

TABLE II: Summary and Comparison of simulated results with the state-of-the-art LDOs.
* Simulated Results. ** Estimated from figure.

improve steady state output regulation of the FVF LDO. The proposed LDO achieves a transient response time (T_R) of 0.73ns while exhibiting an improved DC load regulation of 0.031mV/mA. A ΔV_{OUT} of 48mV is measured through the load transient analysis.

To compare this work with other LDOs in the literature, widely used T_R and figure-of-merit (FOM) are adopted from [11]. T_R is defined as

$$T_R = \frac{C\ \cdot\ \Delta\ V_{OUT}}{I_{MAX}} \tag{2}$$

where $\Delta\ V_{OUT}$ is the maximum variation in output voltage during the load transient and C is the total on-chip capacitance. The FOM is given by

$$FOM = T_R\ \cdot\ \frac{I_Q}{I_{MAX}} \tag{3}$$

Therefore, FOM is a function of T_R, total quiescent current I_Q and maximum load current I_{MAX}. This indicates that, the lower the FOM, the better is the performance of the LDO. From Table II, it can be observed that the proposed LDO with the newly introduced Loop 4 for improving DC accuracy also aids in enhancing the transient response time and thereby achieving an ultra low FOM of 3.9ps. In comparison with other works in the literature as showcased in Table II, the proposed LDO performs comparably in terms of dropout, quiescent current consumption, transient response time, and DC load regulation.

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