An 800 mA Load Current LDO with Wide Input Voltage Range

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***Abstract*—A low-dropout regulator (LDO) with 800 mA load current with wide range input voltage is designed and proposed in this paper. The designed LDO includes two cascaded LDOs. The first one uses a p-type of DMOS power transistor to convert a wide input voltage (3.9 to 20 V) to a stable output voltage of 3 V, which provides a supply voltage for other circuits. The second LDO is designed to achieve a large load current by utilizing a high current driving capability of NPN power transistor. To achieve a high slewing rate, both PMOS and NMOS input-pair amplifiers with a push-pull output stage are adopted. Through the Kelvin connection of external resistors, the output voltage can be adjusted to a different value. The typical output voltage is 2.5 V in this study, and the simulation results show that the designed LDO has good transient response. The measurements demonstrate the output voltage of 2.5 V is stable with a 15μF output capacitor when an input voltage from 3.9 V to 20 V is applied. With a full output load range from 0 to 800 mA, the proposed LDO obtains a line regulation of 0.5093 mV/V and a load regulation of 0.046 mV/mA. The total active chip size is approximately 1.42 mm^2 with 20V/0.25μm CMOS process.**

Keywords-wide range input voltage; large load current; LDO

I. INTRODUCTION

With the rapid development of the microelectronics technology, power management family is necessary to reduce the standby power of portable applications such as PDAs and phones [1], [2]. As a common power chip, LDO has many advantages, such as: fast transient response, current output capability, high linearity and low output ripple [3]; however, part of the application of LDO is restricted because of the narrow input supply range (usually 2-5 V), when the supply voltage comes higher than 5 V, most of the LDOs with typical input range will be crashed [4]. Wide range of input voltage can expand application scope of the LDO, not only on battery-powered systems but also on industrial products [5]. At present, the low voltage device is used in the internal control circuit of the chip. Therefore, it is more and more widely used in the power management chip with a high-low voltage conversion LDO module. In addition, the output current range of a traditional LDO is very low, so it has essential to design a high performance LDO with wide input voltage range and large output load current.

In this paper, the designed circuit with two cascaded LDOs structure achieves not only a wide range of input voltage but also a large output current. In order to withstand high input voltage, the first stage of the LDO uses a P-type of DMOS power transistor as pass device to convert high input voltage to a 3 V power supply powering all other low voltage circuits. The second stage of the LDO adopts a NPN power transistor to obtain a large load current. This paper is organized as follows. Section II presents the operating principle of the traditional LDO regulator; Section III introduces the proposed LDO structure with wide range of input voltage and large load current. The simulation and measured results of the proposed LDO regulator are demonstrated in Sections IV and the conclusions are finally given in Section V.

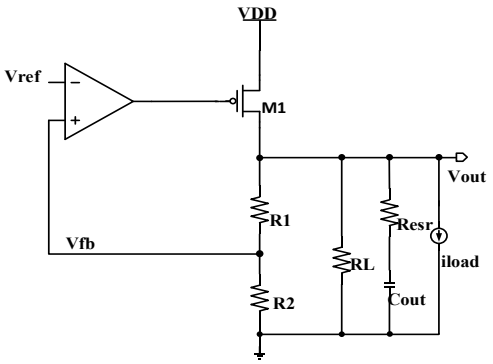

Figure 1. The circuit architecture of a traditional LDO regulator.

II. TRADITIONAL LDO REGULATOR

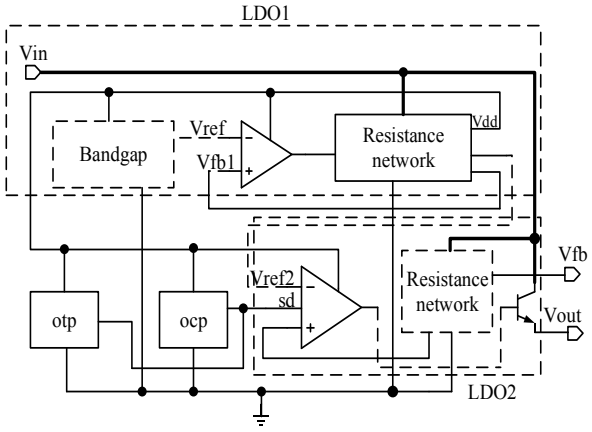

Figure 2. The full structure of the proposed LDO regulator.

Figure 1 shows a traditional LDO regulator, where a bandgap reference, an error amplifier, a power transistor, a feedback-resistor network, an off-chip Equivalent Series Resistor (ESR) R_{esr} and capacitor C_{out} are used [2]. R_L represents the equivalent load impedance. The voltage divider resistors (R1 and R2), the error amplifier and the power transistor formed a negative feedback loop. LDO regulator works as follows: if V_{out} rises, the feedback voltage V_{fb} will be increased, and then the output voltage of the error amplifier will become larger, resulting in the rise of gate voltage of M1. Because M1 is a PMOS power device, so the overdrive of M1 is decreased, leading to a reduced current flowing through it. Therefore V_{out} drops. Because of the action of the error amplifier, the feedback voltage V_{fb} is approximately equal to the reference voltage V_{ref}, so the relationship between the output voltage and the bandgap reference voltage is

$$V_{out} = \frac{(R_1 + R_2) \times V_{ref}}{R_2} \tag{1}$$

It can be clearly seen that V_{out} is independent of the power voltage VDD.

III. Circuit Design and Analysis

A. The Overall Function of the Circuit

Figure 2 shows the full structure of the designed LDO regulator, it includes two cascaded LDOs. The first stage of the LDO consists of bandgap generator, an amplifier and a resistance network module, and is used for generating voltage references, bias currents and a 3 V power supply V_{dd} which is employed for powering all low voltage control circuits. The second LDO is designed to achieve a large load current by utilizing a high current driving capability of NPN power transistor. Through the Kelvin connection of external resistors between nodes V_{fb} and V_{out}, the output voltage can be adjusted to a different value. In order to protect the chip, an over-temperature protection module and an over-current protection module are designed. When the chip temperature is higher than 160 degrees or the current is greater than 1.2A, the circuit stops working.

B. The First Stage of LDO

As shown in Figures 3, the first stage LDO consisting of a bandgap generator, an error amplifier and a resistance network module is implemented. The main function of the first stage LDO is to transfer the wide input range from 3.9 to 20 V to 3 V power supply, having the feature of low output noise. As shown in Figure 3, bias currents and voltage references are provided by the bandgap reference module. The node V3 is connected to the input V_{fb1} of the error amplifier and forms a negative feedback to obtain stable operation.

Since the adopted low-voltage Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) cannot work at a high voltage environment, the resistance network consisting of DMOS transistors M9-M13 instead of MOSFET transistors and R4 resistor working at a supply voltage as high as 20 V is employed in this study. By using DMOS transistors, the first LDO with an input voltage range from 3.9 to 20 V (V_{in}) achieves to a stable low output voltage (V_{dd}=3 V) in this study. In addition, the DMOS channel structure is formed by a diffused junction and the on-resistance R_{on} is very low, so the pole frequency generated by DMOS output stage is higher than conventional MOSFET. In other word, the use of a DMOS power transistor makes the frequency compensation much simpler; however, the DMOS device will occupy a large area, and the match quality between different devices is not accurate, so other circuits except for resistance network circuit in this study are implemented by low-voltage MOSFET devices, as shown in Figure 3.

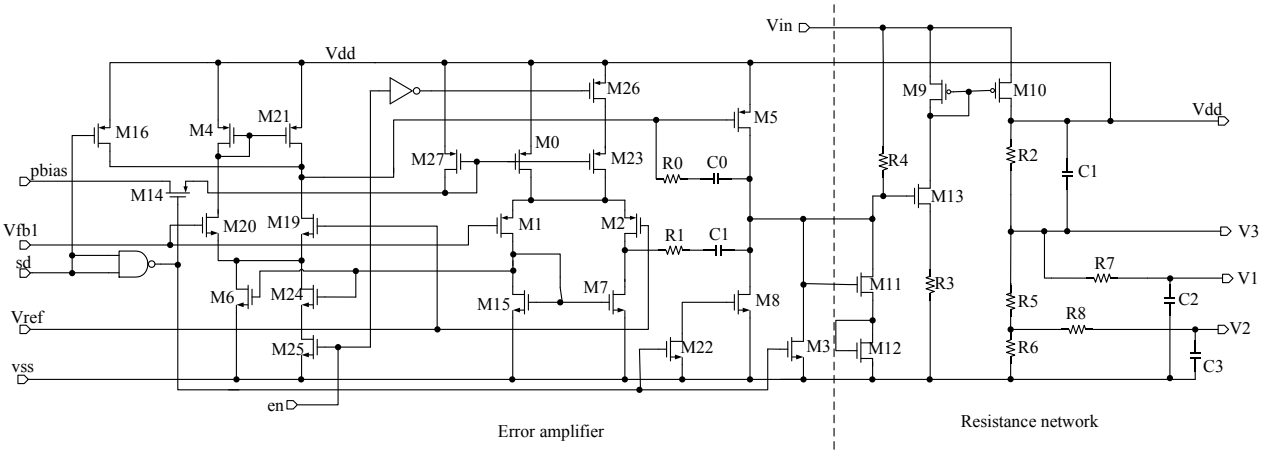

Figure 3. The first stage of LDO.

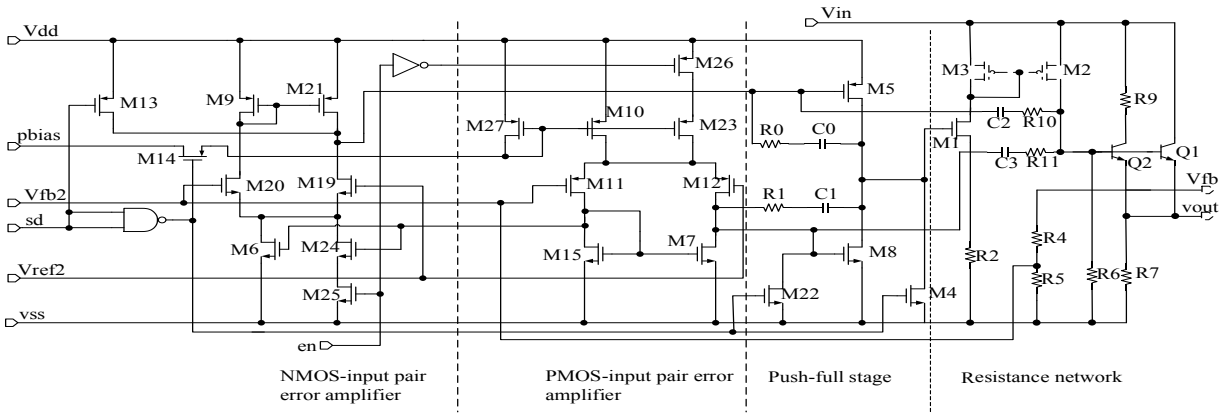

Figure 4. The second stage of LDO.

TABLE I. COMPARISON OF DIFFERENT CONDUCTIVE DEVICES IN LDO

Power transistor	NPN	PNP	NMOS	PMOS
Control method	Current control	Current control	Voltage control	Voltage control
Output current	High	High	Medium	Medium
speed	fast	Slow	Medium	Medium
Drive capability	Strong	Strong	Weak	Weak

C. *The Second Stage of LDO*

As shown in Figure 4, the second stage of the LDO in this study is mainly composed of an error amplifier, and a resistance network circuit in which a NPN power transistor Q1 is used. The error amplifier operates with a low supply voltage from LDO1, as shown in Figure 2. The resistance network circuit consisting of DMOS transistors M1-M3, a NPN power transistor and several resistors operates at a supply voltage range of 3.9 to 20 V and achieves a typical output power voltage of 2.5 V. The NPN power transistor uses an emitter follower structure to obtain features of low output impedance and higher current driving capability. As shown in Table I, NPN transistor shows a higher performance compare with other type of transistors. Due to NPN transistor's smaller parasitic capacitance, and the circuit transient response is significantly enhanced. Also, at the same driving capability, the area of NPN power transistor is much smaller than other power transistors. Consequently, a high-load current LDO is achieved by using NPN power transistor in this study.

The error amplifiers with identical structure and features are implemented in both LDO1 and LDO2, and the only difference is that the gate of M5 and M8 in LDO2 connects with C2/R10 and C3/R11, respectively, which compensates the overall frequency of the LDO. As shown in Figures 3 and 4, the amplifier is implemented by both NMOS differential input pair and PMOS differential input pair error amplifiers and a push-pull second stage. They work as class AB amplifiers, and have a high slewing rate and a very fast transient response speed [6], [7]. MOSFET M6, M24, M25 and M10, M23, M26 are the source for NMOS differential input pair and PMOS differential input pair respectively, when the LDO works in the heavy load case, they all work; when the load is a light load case such as the load current is lower than 5 mA, "en" node becomes low and turns off M24 and M25, the output of the inverter becomes low and also turns off M23 and M26, only M6 and M10 provide current. Thus the bias current of the error amplifier is significantly reduced, leading a very low quiescent current for the whole LDO circuit. By the use of this amplifier structure and a NPN power transistor, a full load current (0 to 800mA) is achieved. It enables the LDO to achieve a fast and stable operation.

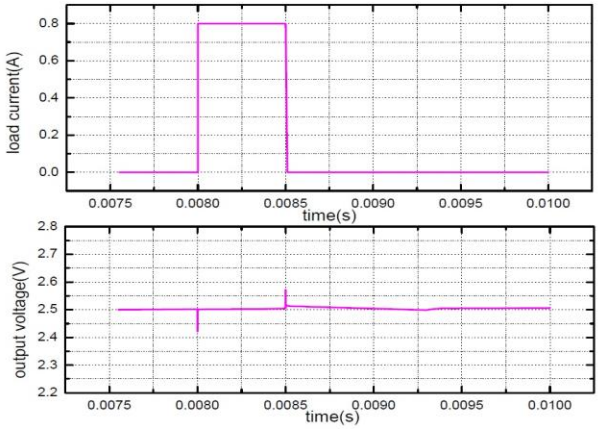

Figure 5. Simulated load transient response.

In addition, R0/C0, R1/C1 are used for phase compensation; ensuring the stability of the error amplifier circuit. The LDO has a primary pole and a zero at the output [8], this because the LDO chip requires a μF class capacitor with an equivalent series resistance. The output stage of error amplifier module produces a non-dominant pole, R10/C2, R11/C3, generate LHP zeros for the LDO regulator loop, by selecting the appropriate resistance and capacitance value, these zeroes compensate the non-dominant poles effectively [9]-[10]. Under different load current conditions, the proposed LDO regulator has a phase margins over 60 degree.

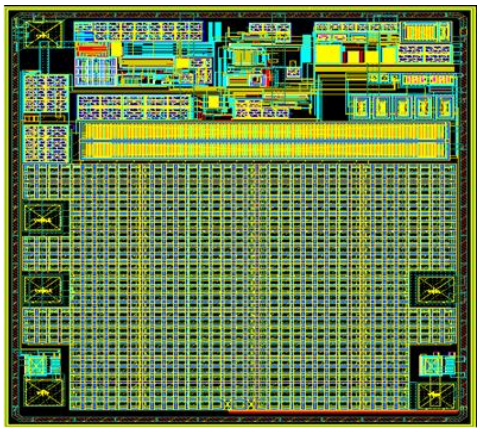

Figure 6. Layout view of LDO.

IV. Simulation and Measure/d Results

As shown in Figure 5, when the load current is increased from 0 mA to 800 mA, then from 800 mA back to 0 mA after 500 μs, load transient simulation results show that the output over-shoot voltage is 81mV with a recovery time of 9.5 μs and the under-shoot voltage is 68 mV, with a recovery time of 180 μs. From the heavy load to light load, the excess current flows to the output capacitor so the regulating capacity of the power transistor is reduced, LDO.

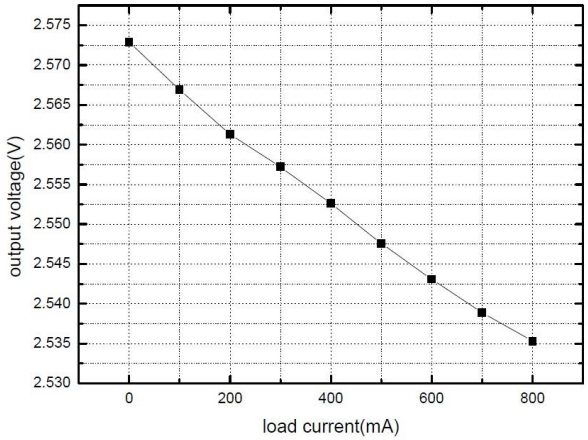

Figure 7. Measured load regulation.

The designed LDO was fabricated based on Taiwan vis25cb Technology of VIS. Layout view of the LDO can be found in Figure 6. The efficient routing minimized the area of the device to 1.42 mm^2. In the error amplifier module, in order to ensure the differential pair of tubes with good matching characteristics, using common-centroil layout technique, the poly resistance need high matching precision, they are divided into a number of small resistors in series, and then the minimum spacing is arranged alternately. Finally, dummy resistors are placed on both sides to achieve good resistance matching. Table II shows competitive results when compared with other works.

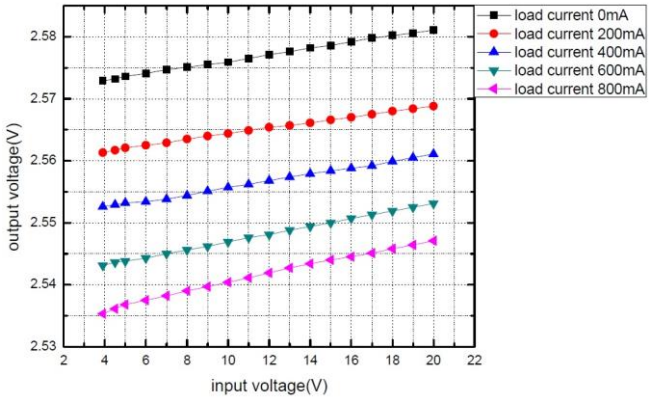

Figure 8. Measured line regulation.

Figure 7 shows the measurement results of load regulation when input voltage is 3.9 V, the load regulation of 0.0458 mV/mA is obtained. Figure 8 presents the measured result of line regulation at different load current. When load current change from 0 mA to 800 mA, we get line regulation is of 0.5093 mV/V.

TABLE II. Comparison with Other Studies

Parameter	This work	[2] 2017	[4] 2014	[8] 2010	[9] 2017
Process(μm)	0.25	0.5	0.6	0.5	0.18
Area (mm^2)	1.42	0.4	0.3	0.263	0.216
Vin (V)	3.9-20	3.5-5.5	4-40	1.4-4.2	2.9-3.3
Vout (V)	2.5	3.3	2.5-5	1.21	2.8
$I_{OUT_{MAX}}$ (mA)	800	300	30	100	150
$I_{OUT_{MIN}}$ (mA)	0	0	0.1	0.001	0.001
Line Reg. (mV/V)	0.5093	1.66	--	--	1.25
Load Reg. (mV/mA)	0.0458	0.0334	--	--	0.25

V. Conclusion

The designed LDO structure with large load current is achieved by using two-stage LDO structure, and the circuit configuration has wide input voltage from 3.9 V to 20 V. Testing shows the designed LDO is stable under various conditions with the load current ranging from 0 mA to 800 mA. The quiescent current is 800μA. The total active chip size is approximately 1.42 mm^2 with a standard 0.25-μm CMOS process.

Acknowledgment

This research was supported in part by the Tianjin Municipal Science and Technology Commission under Grant (15JCZDJC30900).

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