POLE-ZERO TRACKING FREQUENCY COMPENSATION FOR LOW DROPOUT REGULATOR

Ka Chun Kwok and Philip K. T. Mok

Department of Electrical and Electronic Engineering
The Hong Kong University of Science and Technology
Clear Water Bay, Hong Kong

Tel: (852) 2358-8517, Fax: (852) 2358-1458, E-mail: eemok@ee.ust.hk

ABSTRACT

Most of the Low Dropout Regulators (LDRs) have limited operation range of load current due to their stability problem. This paper proposes a new frequency compensation scheme for LDR to optimize the regulator performance over a wide load current range. By introducing a tracking zero to cancel out the regulator output pole, the frequency response of the feedback loop becomes load current independent. The open-loop DC gain is boosted up by a low frequency dominant pole, which increases the regulator accuracy. To demonstrate the feasibility of the proposed scheme, a LDR utilizing the new frequency compensation scheme is designed and fabricated using TSMC 0.35μm digital CMOS process. Simulation results show that with output current from 0 μA to 100 mA the bandwidth variation is only 2.3 times and the minimum DC gain is 72 dB. Measurement of the dynamic response matches well with simulation.

1. INTRODUCTION

Low Dropout Regulators (LDRs) are commonly used in high performance applications due to their low noise, fast transient response characteristics. In LDR design, frequency response is the most important issue in regulator performance. Conventional LDR uses Equivalent Series Resistance (ESR) frequency compensation [1-2]. This introduces an ESR zero in the open-loop transfer function and contributes a pole-zero cancellation to ensure closed-loop stability. This design, however, is not an optimal method to maintain stability. In general, the dominant pole is at the output node [3-4]. Since typical voltage regulator has wide loading current range, the dominant pole changes significantly with different loading conditions. Thus the frequency response is only optimized in a fixed load current. Other problems such as low open-loop DC gain, ESR variation and ESR ripple voltage also limit the performance of the regulator.

In order to maintain the regulator stability and performance over wide load current range, a novel pole-zero tracking frequency compensation scheme is proposed. Using a tracking zero to cancel the output pole, the frequency response becomes load current independent.

In this paper, the limitations of conventional LDR frequency compensation are discussed in Section 2. The proposed design is presented in Section 3. Measurement results are included in Section 4 and finally a conclusion is given in Section 5.

2. LIMITATIONS OF CONVENTIONAL LDR FREQUENCY COMPENSATION

In this section, the design and limitations of conventional LDR design is evaluated. Figure 1 shows the structure of a conventional LDR in system level [3]. The error amplifier A acts as a gain stage in the feedback loop to maintain a pre-defined output voltage. The buffer amplifier B provides a low impedance node at the gate of the power transistor. The pass element is a common source PMOS power transistor to provide the output current. The resistor string R_1, R_2 scales the output voltage and compares to the reference voltage from the error amplifier. A large capacitor C_o is connected at the output node to stabilize the output voltage and resistor R_{ESR} is in series with the output capacitor to form the compensation element.

In analyzing the frequency response of the LDR, the error amplifier and pass transistor are modeled by transconductance g_{m1} and g_{mp}, respectively. The buffer is assumed to have a unity gain. The output resistance and capacitance at node 1 and 2 are notated as $r_{1,2}$ and $c_{1,2}$, respectively. The pass transistor has output resistance r_o.

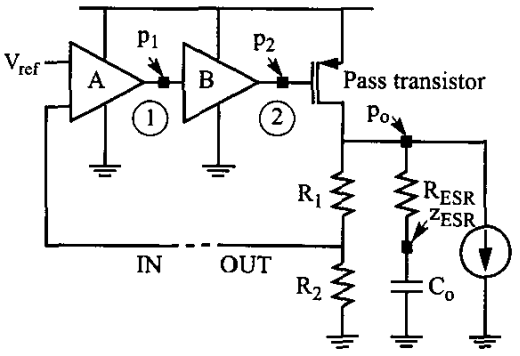


Figure 1: Conventional LDR with ESR frequency compensation

The feedback loop in Figure 1 is "*AC disconnected*" at nodes IN and OUT, i.e. assuming an infinitely large inductor connecting IN and OUT. For a stable system, the loop gain OUT/IN should have enough phase margin. The poles and zero are given by

$$p_1 = \frac{1}{r_1 \cdot c_1} \qquad (1)$$

$$p_2 = \frac{1}{r_2 \cdot c_2} \qquad (2)$$

$$p_o = \frac{1}{(R_{ESR} + r_o) \cdot C_o} \approx \frac{1}{r_o \cdot C_o} \qquad (3)$$

$$z_{ESR} = \frac{1}{R_{ESR} \cdot C_o} . \qquad (4)$$

Conventional LDR frequency compensation uses the ESR zero to cancel out the intermediate frequency pole p_1 so that the phase margin is greater than 45° before the unity-gain frequency. A typical frequency response curve is shown in Figure 2. The major drawback of the ESR frequency compensation is the bandwidth variation due to loading current. From Equation (3), the output pole is given by

$$p_o = \frac{\lambda \cdot I_{out}}{C_o} \qquad (5)$$

where λ is the channel length modulation parameter and I_{out} is the LDR output current. It shows that the dominant pole p_o is directly proportional to I_{out}. Assume that the system performance is optimum in the maximum loading current case. As I_{out} decreases, the dominant pole and so the unity-gain bandwidth of the open-loop response decreases. This severely degrades the performance of the regulator in the low loading current condition in terms of dynamic response and power supply rejection ratio. Figure 3 shows the graphical explanation of this effect in a bode plot.

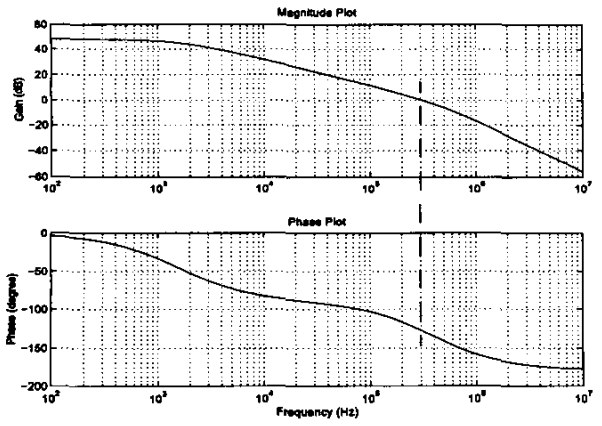


Figure 2: Loop response of an ESR compensated LDR

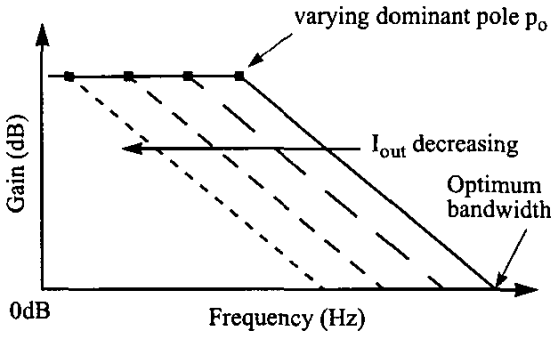


Figure 3: Loop bandwidth variation due to output current

The DC gain of the frequency response depends on the separation of the first and second pole. In conventional design, the two poles are closely spaced [4] and thus the DC gain is usually limited to less than 50dB. Low DC gain leads to poor accuracy.

The feedback loop stability depends on the accuracy of the pole-zero cancellation. Since typical ESR value is temperature, voltage, frequency and material dependent [5], the design of an ESR compensated LDR may not be reliable for all temperature and supply voltage range.

When the load current increases rapidly, there is voltage drop across the output capacitor [6]. Since conventional LDR compensation has a resistor in series with C_o, an excess of voltage ripple appears at the output and degrades the regulator performance.

3. POLE-ZERO TRACKING FREQUENCY COMPENSATION FOR LDR

The block diagram of the proposed frequency compensation scheme is shown in Figure 4. The concept of the proposed scheme is to move the series RC network used for compensation into the output node of the error amplifier. If the resistance value is a controllable parameter, the generated zero can be adjusted. In order to have pole-zero cancellation, the position of the output pole p_o and compensation zero z_c should match with each other. The compensation resistor R_c and capacitor C_c values are given by

$$\text{output pole } p_o = \frac{1}{r_o \cdot C_o}$$

$$= \frac{1}{R_c \cdot C_c} = \text{compensation zero } z_c . \qquad (6)$$

By setting the relationships

$$R_c = r_o \times K, \qquad C_c = C_o / K \qquad (7)$$

with K as a constant, the equality in Equation (6) holds. In Figure 4, the tracking zero is generated by a scaled mirror transistor M_c operating in linear region and acts as a linear

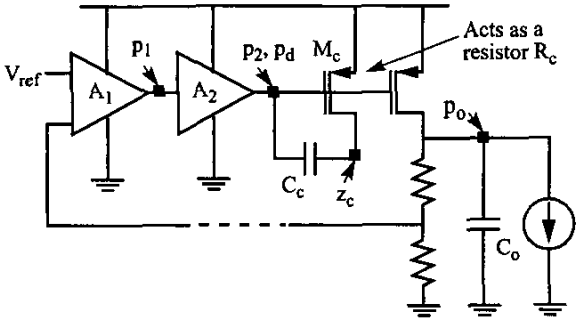


Figure 4: Structure of pole-zero tracking compensated LDR

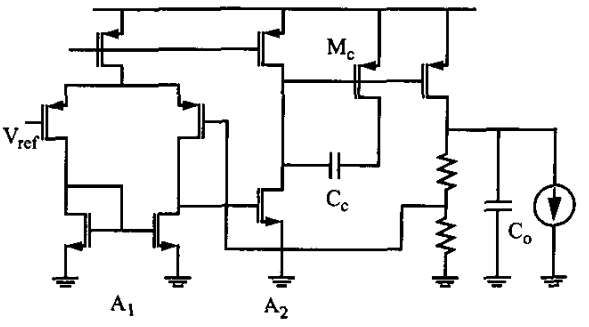


Figure 5: Schematic of the pole-zero tracking compensated LDR

resistor R_c whose resistance value is controlled by the gate terminal.

In this design, a two-stage amplifier is used as the error amplifier to provide a higher DC gain. Amplifiers A_1 and A_2 are modeled as two transconductor stages g_{m1} and g_{m2}. Their corresponding output resistance and capacitance are r_1, c_1 and r_2, c_2 respectively. The buffer amplifier appearing in conventional design is removed in order to minimize power consumption. The frequency compensation network consists of the capacitor C_c and the M_c drain-source resistance R_c. The gates of the mirror transistor M_c, and the output transistor M_o contribute a parasitic capacitance c_{par}. The poles and zero are now given by

$$p_1 = \frac{1}{r_1 \cdot c_1} \qquad (8)$$

$$z_c = \frac{1}{R_c \cdot C_c} \qquad (9)$$

$$p_o = \frac{1}{r_o \cdot C_o} . \qquad (10)$$

The r_2, c_2, R_c, C_c and C_{par} at the output of the second gain stage contribute two poles, p_d and p_2, which are the roots of the polynomial

$$1 + s(r_2 \cdot c_{par} + R_c \cdot C_c + r_2 \cdot C_c) + s^2 r_2 \cdot R_c \cdot c_{par} \cdot C_c = 0 . \qquad (11)$$

The output pole p_o is cancelled by the tracking zero z_c. Pole p_1 becomes a high frequency pole by careful design of amplifier A_1. By optimizing the parameters in Equation (11), p_d becomes the dominant pole and p_2 is a high frequency pole. The schematic of the LDR is given in Figure 5.

Figure 6 shows the bode plot of the loop gain. The bandwidth of the loop gain remains fairly constant in the order of

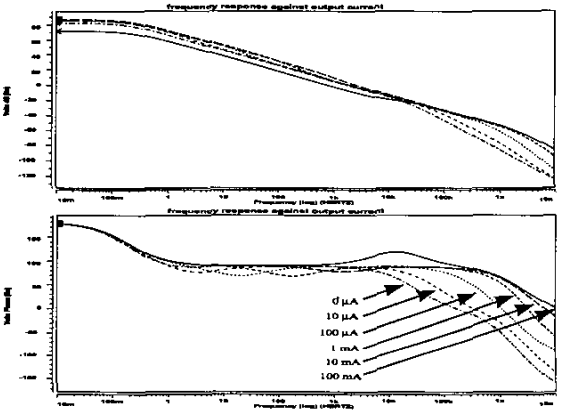


Figure 6: Loop response against different output current

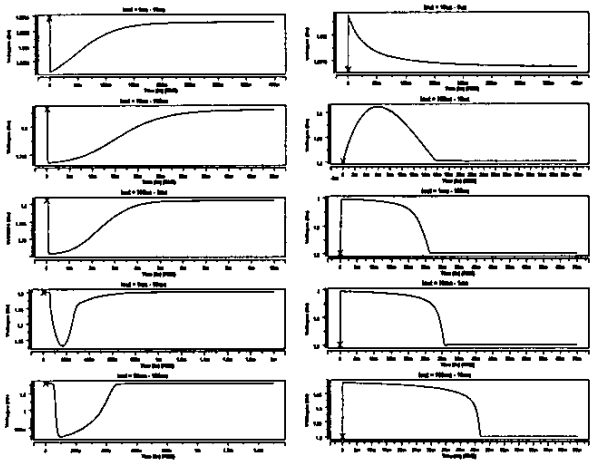
1 kHz for a wide load current range from 0 μA to 100 mA. Although there is a finite mismatch in the pole-zero cancellation of p_o and z_c, the minimum DC gain and phase margin are 72 dB and 86°, respectively.

The transient response of the regulator with different load current rising/falling steps is shown in Figure 7. As seen in the figure, the transient response is now limited by the large signal slewing of the amplifier. The response time can be speed up by using an amplifier with high slew rate capability.

4. EXPERIMENTAL RESULTS

The LDR with pole-zero tracking compensation is fabricated using TSMC[1] 0.35 μm digital CMOS process and the micrograph is shown in Figure 8. Figure 9 shows the measurement results by applying different current pulses at the output of the regulator and observing the output voltage. The

1. Taiwan Semiconductor Manufacturing Company, Taiwan



rising falling

Figure 7: Transient response with different rising and falling load current steps

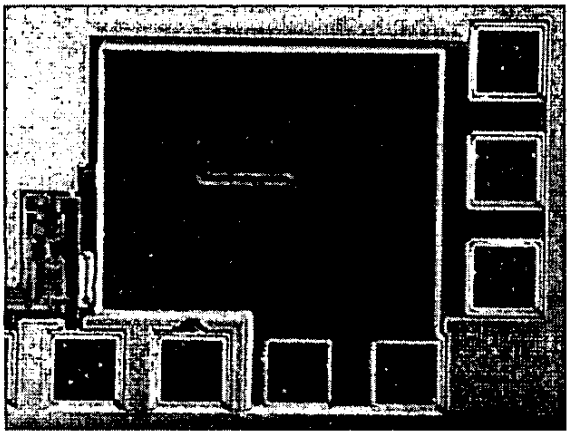


Figure 8: Micrograph of the LDR with pole-zero tracking

steps of the current pulses are 10 μA to 100 μA and 10 mA to 100 mA. It shows very similar response time and voltage spike as in the simulation.

5. CONCLUSIONS

In this paper, the design and limitations of conventional LDR frequency compensation is analyzed. A novel pole-zero tracking frequency compensated scheme is proposed to solve the problem of bandwidth variation due to output current. It also gives a reliable design by eliminating the ESR. To demonstrate the feasibility of the proposed scheme, a LDR utilizing the new frequency compensation scheme is fabricated. With output current from 0 μA to 100 mA, the

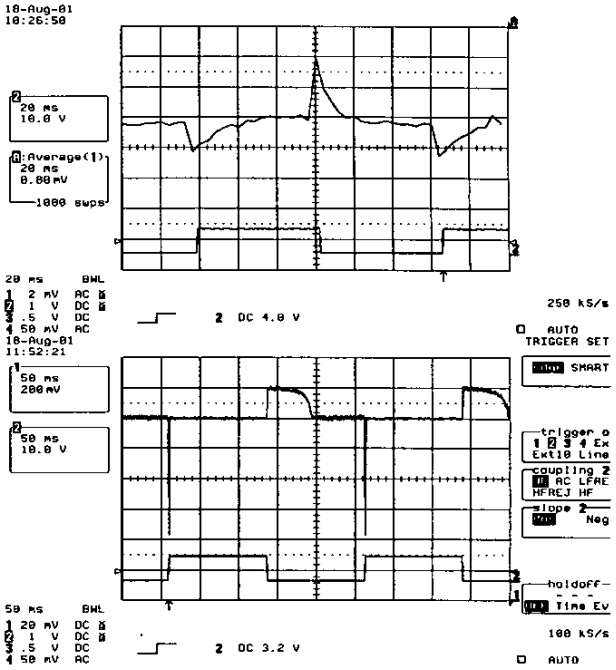


Figure 9: Current step from 10μA to 100μA and 10mA to 100mA

bandwidth variation is 2.3 times and the minimum DC gain is 72 dB. The measured transient response matches well with the simulation.

ACKNOWLEGEMENTS

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REFERENCES

[1] C. Simpson, "Linear Regulators: Theory of Operation and Compensation," Application Note 1148, *National Semiconductor*, May 2000.

[2] C. Simpson, "A User's Guide to Compensating Low-Dropout Regulators," *Wescon Conference*, Santa Clara, CA, pp. 270–275, Nov. 1997.

[3] G. A. Rincon-Mora and P. E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[4] G. A. Rincon-Mora and P. E. Allen, "Optimized Frequency-Shaping Circuit Topologies for LDO's," *IEEE Transactions on Circuits and Systems II*, vol. 45, no. 6, pp. 703–708, Jun. 1998.

[5] R. W. Franklin, "Equivalent Series Resistance of Tantalum Capacitors," Technical Information, AVX Limited.

[6] J. P. Busson, "Supply Voltage Drop on Fast Current Demand," Application Brief SLVA 076, *Texas Instruments*, Sept. 1999.