On the Choice of Optimum FET Size in Wide-Band Transimpedance Amplifiers

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***Abstract*—The main figure of merit for transimpedance amplifiers used in amplifying photocurrents in fiber-optics systems is the optical sensitivity. This sensitivity is determined by the equivalent input noise current of the amplifier. To obtain the best noise performance, most transimpedance amplifiers with FET input stages are designed using a result that prescribes making the capacitance of the input FET equal to the photodiode capacitance. It is shown here that this is not necessarily the most favorable practice when using FET's in scaled submicron technologies. For one, it may compromise the stability of the amplifier.**

INTRODUCTION

LOW NOISE fiber-optics receiver design for gigahertz links is a very active area of circuit design. This note addresses some of the considerations in optimizing the noise performance of receiver amplifiers designed in submicron FET silicon or gallium arsenide technologies.

The *sensitivity* of a receiver is its main figure of merit in long-haul fiber-optics link applications. This is defined as the minimum optical signal incident on a photodiode that, when corrupted by the noise in the amplifier following it, results in an average of one error in every 10^9 bits of the data recovered from the amplified signal by a perfect decision-making circuit. An equivalent circuit of the amplifier may be obtained by representing the photodiode as a capacitive current source, and inserting noise current sources in parallel with the channel of the input stage FET and the feedback resistor R_f [1] (Fig. 1). The stages of amplification following the input FET normally contribute a negligibly small noise. The spectral densities of the noise sources are, approximately

$$\hat{i}^2_{FET} = 4kT\gamma g_m, \qquad \hat{i}^2_{Rf} = \frac{4kT}{R_f} \tag{1}$$

where g_m is the transconductance of the FET and γ is a factor that may lie anywhere between 0.67 to 8, depending on the type of FET and the operating point [2].

This note addresses the issue of how to best choose the FET size such that the noise added by these two sources to the photocurrent is minimized in the bandwidth of interest. The consequences of using FET's with submicron gate lengths, as is common in high bandwidth applications, are considered, with emphasis on the stability of the transimpedance amplifier. The discussion is restricted to the study of a wide-band unequalized amplifier; it is well known that amplifiers with a lower input noise may be used if they are not of the transimpedance variety, but these suffer from the limitation that a trimmed equalizing filter must follow the amplifier.

Manuscript received April 21, 1987; revised July 20, 1987. This work was supported by AT&T Bell Laboratories and the State of California MICRO program.

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IEEE Log Number 8717513.

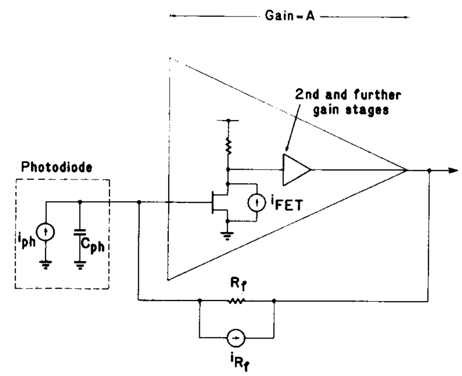

Fig. 1. Equivalent circuit of transimpedance amplifier showing noise current sources.

THE NOISE MINIMUM

A previous study [3] suggests that the best sensitivity occurs when $C_g = C_{ph}$, where $C_g = C_{gs} + C_{gd}$, the total gate capacitance of the FET, and C_{ph} is the sum of the photodiode and stray capacitances. This result may be qualitatively interpreted as follows. The carriers in the inversion layer of a submicron FET move at the *saturation drift velocity* $v_{\rm dsat}$ when the FET channel is biased well beyond pinchoff to obtain a high gain. The unity voltage gain frequency is given by $\omega_T = g_m/C_g$; for a given channel length, ω_T is constant because $g_m = C_g' W v_{\rm dsat}$, where C_g' is the gate capacitance per unit area and W is the gate width. This means that g_m is directly proportional to C_g. Choosing a small width device implies a small g_m; from (1), the noise contribution of $V_{\rm FET} = i_{\rm FET}/g_m$ will then become large. On the other hand, a large width means a large C_g, so the feedback resistor R_f must be made small to drive the increased capacitance; thus, i_{Rf} becomes large. The optimum lies where $C_g = C_{ph}$.

This result has been used to design broadband transresistance amplifiers in monolithic silicon NMOS circuits,

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for operation at 90 Mbit/s [4] and 1.4 Gbit/s [5]. Typical photodiode and stray capacitances of between 0.5 to 1 pF are matched by input device widths of about 1000 μm and channel lengths of 1 μm, where the oxide thickness is 250 Å. These large input devices, however, may substantially increase the power dissipation of the IC's, because they have to be biased with relatively large currents to obtain the maximum gain. In the case of the 1.4-Gbit/s circuit, there is an additional important consideration. Wire bonds are used to connect the amplifier terminals from the chip to the external package. In particular, this introduces a bondwire inductance L_{bond} in series with the source of the input FET. The effective FET transconductance then becomes

$$\frac{i_d}{v_{gs}} = \frac{g_m}{1 + j\omega L_{\text{bond}} g_m}.$$

This produces an additional phase lag in the circuit due to the pole at $1/(g_m L_{\text{bond}})$. When combined with the other poles that arise within the transresistance feedback loop, this may make the loop unstable. For $g_m = 100$ mS and $L = 2$ nH, typical values for an input FET with a width of 1000 μm mounted in a microwave package, the pole frequency lies at 795 MHz, and will have a significant effect on the response of an amplifier intended for gigahertz operation. As the bond wire inductance is fixed by the practical mechanical constraints, the ac performance of the circuit may only be improved if a FET of smaller width, and thus smaller g_m, is used. This very important issue has not been addressed in a recent study of noise optimization in GaAs MESFET transimpedance amplifiers [6].

When examining the tradeoffs of different values of R_f versus C_g (Fig. 1) on the noise performance, it is important to realize that only a small voltage gain is available from a single stage submicron FET amplifier, irrespective of the external load. This is because the ratio g_m/g_{ds} of submicron FET's in both MOS and GaAs technologies is between 5 and 10, so the voltage gain of a FET biased by an ideal current source (Fig. 2), the best of all possible loading conditions, is limited by its own output conductance g_{ds}. Thus, because only one or two gain stages are typically used within a feedback loop to ensure table operation, A (Fig. 1) is between 10 to 30.

If the transresistance amplifier is required to have a -3-dB bandwidth of ω_B, determined by the transmission bit rate, then, clearly

$$\omega_B = \frac{A}{R_f(C_{ph} + C_g)} \tag{2}$$

where it is assumed that a cascode-like input stage is used to prevent the effect of Miller multiplication of C_{gd}. If i_{eq} is the net noise contribution of i_{FET} and i_{Rf} that appears in parallel with the photocurrent, then

$$\frac{\hat{i}^2_{eq}}{4kT} = \frac{1}{R_f} + \frac{\gamma}{g_m}\left(\frac{1}{R_f^2} + \omega^2 (C_g + C_{ph})^2\right) \tag{3}$$

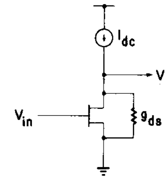

Fig. 2. Illustrating the intrinsic gain of a FET biased by current source.

which, using (2) and the definition of ω_T, may be written as

$$\frac{\hat{i}^2_{eq}}{4kT} = \frac{\omega_B}{A}(C_g + C_{ph}) + \frac{\gamma}{\omega_T C_g} \times (C_g + C_{ph})^2 \left(\frac{\omega_B^2}{A^2} + \omega^2\right). \tag{4}$$

The noise bandwidth of the amplifier is $\alpha(\omega_B/2\pi)$, where α is almost 1 for a multipole rolloff [1]. Thus, the mean-square integrated noise current is given by

$$\overline{i^2_{eq}} = \int_0^{\alpha\omega_B/2\pi} \hat{i}^2_{eq} df$$

so from (4)

$$\frac{\overline{i^2_{eq}}}{4kT\omega_B^2} = \frac{\alpha}{2\pi}\left(\frac{\gamma\alpha^2}{3} \cdot \frac{\omega_B}{\omega_T} \cdot \frac{(C_g + C_{ph})^2}{C_g} + \frac{1}{A}(C_g + C_{ph})\right). \tag{5}$$

For a given amplifier bandwidth ω_B and photodiode capacitance C_{ph}, the minimum amplifier noise results for the value of C_g that minimizes the expression within the brackets. To evaluate this expression meaningfully, note that the ratio of the amplifier bandwidth to the unity gain frequency of the FET's constituting the amplifier ω_B/ω_T will vary anywhere from $1/A$ to $0.5/A$, depending on the type of circuit used. Thus, (5) may be rewritten as

$$\overline{i^2_{eq}} \cong \frac{4kT}{2\pi} \cdot \frac{\omega_B^2 C_{ph}}{A}\left(\beta \cdot \frac{(C_g/C_{ph} + 1)^2}{C_g/C_{ph}} + (C_g/C_{ph} + 1)\right) \tag{6}$$

where we use the fact that $\alpha \cong 1$, and where

$$\beta \overset{def}{=} \frac{\gamma A \alpha^2}{3} \cdot \frac{\omega_B}{\omega_T}$$

and from the values of the several variables discussed above, it may be seen that β is a constant in the range

$$0.1 < \beta < 2. \tag{7}$$

The expression within large parentheses in (6) undergoes a minimum when

$$\frac{C_g}{C_{ph}} = \sqrt{\frac{\beta}{\beta + 1}}.$$

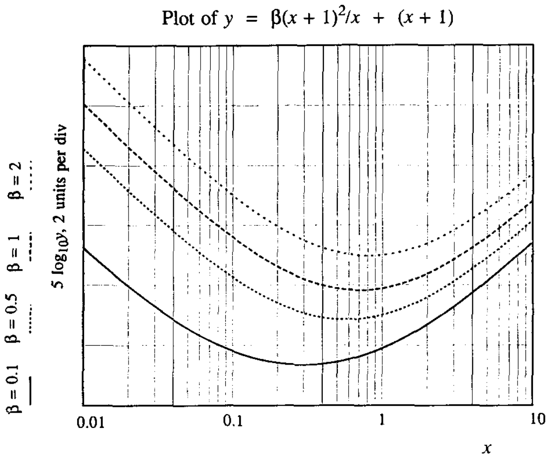

Fig. 3. Plot of normalized mean-square equivalent input current versus normalized device capacitance.

Let the minimum value of the expression be m_β. Then the smallest mean square noise current presented by the amplifier is

$$\overline{i_{eq}^2}\,(\min) \propto \frac{\omega_B^2 C_{ph}}{A} \cdot m_\beta.$$

This expression has the following interpretation. For any photodiode capacitance, the input FET capacitance may be adjusted to obtain the minimum value m_β, which only depends on the constant β. The resulting amplifier noise increases as the square of the data bandwidth (ω_B), linearly with the photodiode capacitance (C_{ph}), and inversely with the amplifier gain (A). A substantial penalty is thus paid in noise performance when submicron FET amplifiers are used to make gigabit-per-second receivers, because ω_B increases while, at the same time, A tends to be smaller for these FET's. The magnitude of C_{ph} is determined by fundamental considerations like the photodiode area, which must be large enough to gather sufficient light from the fiber, but not so large that the diode capacitance limits the speed of response.

Now consider the situation where all these three quantities are given to the circuit designer, who has only the freedom to choose the FET width. The optical sensitivity of the amplifier η is given by [3]

$$\eta = 10 \log_{10}\left(6\overline{i_{eq}} \cdot \frac{hc}{q\lambda} \cdot \frac{1}{1 \text{ mW}}\right) \text{dBm} \qquad (8)$$

where h is Planck's constant, q is electronic charge, λ is the wavelength of photons incident on the photodetector connected at the amplifier input, and c is the speed of light. We will assume that an acceptable amplifier is one that remains within 0.5 dBm of the optimal sensitivity. It is necessary, then, to examine how the quantity 10 $\log_{10}(\overline{i_{eq}}) = 5 \log_{10}(\overline{i_{eq}^2})$ varies in magnitude as C_g deviates from the optimum value. This normalized noise current is plotted with the coefficient of the first capacitive term in (5) in the range of 0.1–1 relative to that of the second capacitive term (Fig. 3). The plots indicate that the range $0.2\,C_{ph} \leq C_g < 2\,C_{ph}$ gives values of amplifier noise very close to the optimum. Noting the lower bound, this means that width of the input FET may be made up to 5 times smaller than that required to match the photodiode capacitance, without seriously degrading the noise of the transimpedance amplifier. The circuit will then dissipate less power, and excess phase shift due to the wirebond inductance will start to appear at proportionally higher frequencies. Both these advantages are highly sought by the circuit designer.

Conclusion

It is shown that optimum noise performance may be obtained in transresistance amplifier employing submicron FET input stages by choosing the width of the input device such that its gate capacitance is one-fifth of the sum of the photodiode and stray capacitance. This reduces the power dissipated in the amplifier, and the possible instability in the transimpedance feedback loop due to the excess phase lag introduced by bond wire inductance.

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