An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch

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***Abstract*—This brief analyzes the effect of load capacitor mismatch on the offset of a regenerative latch comparator. Two analytical models are presented and compared with HSpice simulations. Our results indicate that in a typical 0.18-μm CMOS latch, a capacitive imbalance of only 1 fF can lead to offsets of several tens of millivolts.**

***Index Terms*—Capacitor mismatch, dynamic offset, latch.**

I. Introduction

THE dynamic latch (Fig. 1) is a commonly used building block in a variety of applications, including memory chips and A/D converters. Design considerations for many application specific derivates of this circuit, along with associated nonidealities have been the topic of numerous publications [1]–[5].

Among the key performance metrics of a dynamic latch used in a voltage comparator is its input referred offset voltage. Relevant effects that contribute to the offset can be divided into static and dynamic components. The most commonly discussed source of static offset stems from threshold voltage mismatch [6], [7] in the constituent transistors. An example of a dynamic contributor is charge injection from switches that interface the basic latch of Fig. 1 to its surrounding circuitry [1], [2].

In this brief, we investigate the effect of load capacitance mismatch as an additional source of dynamic offset. As we shall show, any mismatch in the load capacitors C_1 and C_2 (see Fig. 1) in an otherwise perfect latch can lead to considerable offset in practice. In practice, any difference between C_1 and C_2 can be due to random mismatch in the device capacitances, as well as systematic and random imbalance in the wiring parasitics and loading of the two output nodes.

In previous work, an intentional load capacitor imbalance has been used to calibrate the total input-referred offset of a latch comparator [8]. The present work delivers a detailed analysis of the dynamic effects that determine the offset due to capacity imbalance. Reference [9] describes similar work based on a different mathematical approach..

II. Circuit Model

Fig. 1 models the circuit under consideration in regeneration mode, i.e., the state at which the nodes have been set to their initial values and the latch is about to amplify the applied voltage differential. For simplicity, we omit additional components, such as switches that are used to setup, configure and interface this circuit in its various phases of operation. C_1 and C_2 represent the total capacitance that is present at the output nodes $V_{\rm out1}$ and $V_{\rm out2}$.

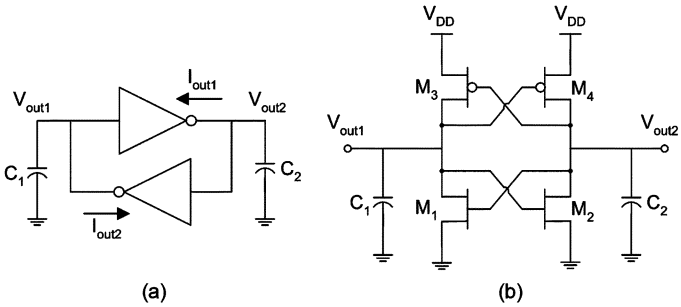

Fig. 1. (a) Dynamic latch consisting of back-to-back inverter stages. (b) Transistor-level schematic.

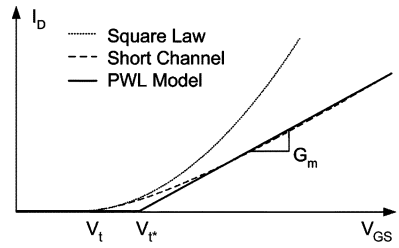

Fig. 2. PWL $I_{\rm D}-V_{\rm GS}$ model for a short-channel MOSFET.

For further analysis, we assume that transistors are forward active in the latch's initial operating point. Furthermore, we invoke the following simplified piecewise-linear (PWL) model for the drain current in a short-channel MOS device (respective signs and polarities are for nMOS)

$$\begin{cases} I_D = G_m(V_{\rm GS} - V_{t^*}), & \text{for } V_{\rm GS} > V_{t^*} \\ I_D = 0, & \text{otherwise.} \end{cases} \tag{1}$$

A graphical justification of this model and an illustration of the involved parameters (G_m, V_{t^*}) are provided in Fig. 2. While the $I_D-V_{\rm GS}$ curve of any MOSFET is nearly quadratic at moderate $V_{\rm GS} - V_t$, the characteristic becomes nearly linear for higher values in modern short channel devices [10]. In our simplified model, G_m represents the slope of a linear fit to the "on" region of the transistor, and V_{t^*} is given by the intercept of this segment with the $V_{\rm GS}$ axis. Note that V_{t^*} is slightly larger than the actual threshold voltage (V_t) of the device.

Applying the above-discussed PWL model to the nMOS and pMOS devices of the inverters in Fig. 1, we find

$$I_{\rm out1} = G_{m1}(V_{\rm out1} - V_{S1}) \tag{2}$$

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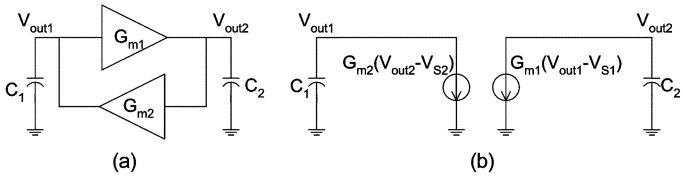

Fig. 3. Model 1. (a) Linearized back-to-back inverter stages. (b) Circuit model.

$$I_{\text{out2}} = G_{m2}(V_{\text{out2}} - V_{S2}). \tag{3}$$

In these equations, $G_{m1,2}$ are the sum of the pMOS and nMOS transconductance terms, and $V_{S1,2}$ are the "switching voltages" of each inverter, i.e., the voltage at which pMOS and nMOS currents are equal. The values of $V_{S1,2}$ depend on V_{DD} and also on G_m and V_{t^*} of the constituent devices.

III. Analysis

A. Model 1

For simplicity, we first consider an idealized latch circuit that contains only capacitances from each output node to ground (see Fig. 3). Using KCL for nodes V_{out1} and V_{out2}, we obtain the following coupled first-order differential equations:

$$C_1\frac{dV_{\text{out1}}}{dt} = -G_{m2}(V_{\text{out2}} - V_{S2}) \tag{4}$$

$$C_2\frac{dV_{\text{out2}}}{dt} = -G_{m1}(V_{\text{out1}} - V_{S1}). \tag{5}$$

The above expressions can be simplified to a single differential equation for one of the outputs

$$\frac{d^2V_{\text{out1}}}{dt^2} - \frac{1}{\tau^2}V_{\text{out1}} + \frac{V_{s1}}{\tau^2} = 0 \tag{6}$$

with

$$\tau^2 \equiv \frac{C_1C_2}{G_{m1}G_{m2}}. \tag{7}$$

Note that by symmetry, solving for one output suffices as the other one can be simply obtained by appropriately swapping the indexes. The two initial conditions required for solving (6) are the initial value of V_{out1} and its first derivative

$$V_{\text{out1}}(0) = V_{\text{out1,0}} \tag{8}$$

$$\frac{dV_{\text{out1}}}{dt}(0) = -\frac{G_{m2}}{C_1}(V_{\text{out2,0}} - V_{S2}) \tag{9}$$

where $V_{\text{out1,0}}$ and $V_{\text{out2,0}}$ denote the initial voltage values of V_{out1} and V_{out2}, respectively. Note that (9) is obtained by evaluating (4) at time zero. Using (8) and (9), we obtain

$$\begin{aligned}V_{\text{out1}}(t) = {}& \frac{1}{2}[\alpha(V_{\text{out2,0}} - V_{S2}) + (V_{\text{out1,0}} - V_{S1})]\exp\left(-\frac{t}{\tau}\right)\\ & - \frac{1}{2}[\alpha(V_{\text{out2,0}} - V_{S2}) - (V_{\text{out1,0}} - V_{S1})]\\ & \times \exp\left(+\frac{t}{\tau}\right) + V_{S1}\end{aligned} \tag{10}$$

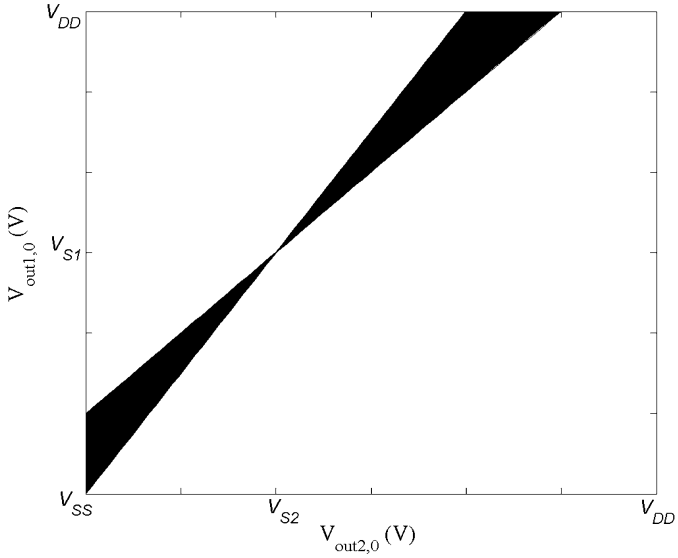

Fig. 4. Decision map for $\alpha = 1.5$. The latch makes a wrong decision in the shaded region.

$$\begin{aligned}V_{\text{out2}}(t) = {}& \frac{1}{2\alpha}[\alpha(V_{\text{out2,0}} - V_{S2}) + (V_{\text{out1,0}} - V_{S1})]\exp\left(-\frac{t}{\tau}\right)\\ & + \frac{1}{2\alpha}[\alpha(V_{\text{out2,0}} - V_{S2}) - (V_{\text{out1,0}} - V_{S1})]\\ & \times \exp\left(+\frac{t}{\tau}\right) + V_{S2}\end{aligned} \tag{11}$$

where

$$\alpha \equiv \sqrt{\frac{G_{m2}C_2}{G_{m1}C_1}}. \tag{12}$$

The above equations contain exponentials with positive exponents that are given by the time constant τ, defined in (7). Furthermore, the opposite signs in (10) and (11) confirm that a decision of the latch will entail the transition of the two outputs toward opposite rails.

Since the exponential terms with negative exponents eventually vanish, only the terms with the positive exponents are important in determining the final state of the outputs. Mathematically, this leads to the following association:

$$\begin{cases} V_{\text{out1}}(\infty) = V_{\text{DD}} \\ V_{\text{out2}}(\infty) = V_{\text{SS}} \end{cases} \Leftrightarrow (V_{\text{out1,0}} - V_{S1}) > \alpha(V_{\text{out2,0}} - V_{S2}) \tag{13}$$

$$\begin{cases} V_{\text{out1}}(\infty) = V_{\text{SS}} \\ V_{\text{out2}}(\infty) = V_{\text{DD}} \end{cases} \Leftrightarrow (V_{\text{out1,0}} - V_{S1}) < \alpha(V_{\text{out2,0}} - V_{S2}) \tag{14}$$

where V_{DD} and V_{SS} denote the positive and negative rails, respectively. Equations (13) and (14) are sufficient to characterize and predict the behavior of the latch for a set of initial voltages. From these expressions, $\alpha = 1$ and $V_{S1} = V_{S2}$ correspond to an ideal, offset-free latch. However, if $\alpha \neq 1$, it is possible for an otherwise ideal latch to make a wrong decision. As an example, Fig. 4 shows a decision map for $\alpha = 1.5$. In this diagram, the shaded region is where the latch fails to make a correct decision, in the sense that the output node with the smaller initial voltage value will transition to the positive rail.

Assuming that $V_{S1} = V_{S2}$, further investigation of (13) and (14) reveals that the latch can make a wrong decision if and only if

$$(V_{\text{out1},0} - V_{S1})(V_{\text{out2},0} - V_{S2}) > 0. \tag{15}$$

This assertion can be verified by further analyzing the behavior of the latch in Fig. 1. For the cases where the initial voltages on two output nodes lie on both sides of the switching voltages, (i.e., one of them is larger than the switching voltage and the other one is smaller) the latch will always make the correct decision, regardless of the amount of mismatch at the output nodes.

To proceed, we define the differential output voltage as

$$V_{\text{out}} = V_{\text{out1}} - V_{\text{out2}}. \tag{16}$$

Noting that the initial differential input to the latch is the output at $t = 0$, we can now express (13) and (14) as

$$\begin{cases} V_{\text{out}}(\infty) = V_{\text{DD}} - V_{\text{SS}}, & \text{iff} \quad V_{\text{out0}} > V_{\text{off}} \\ V_{\text{out}}(\infty) = -(V_{\text{DD}} - V_{\text{SS}}), & \text{iff} \quad V_{\text{out0}} < V_{\text{off}}. \end{cases} \tag{17}$$

with

$$V_{\text{off}} \equiv \alpha(V_{\text{out2},0} - V_{S2}) - V_{\text{out2},0} + V_{S1}. \tag{18}$$

Note that (17) describes the general behavior of a latch, and V_{off} denotes the offset voltage ($V_{\text{off}} = 0$ for an ideal latch). In a non-ideal latch, the mismatch between G_{m1} and G_{m2}, V_{S1} and V_{S2} or C_1 and C_2 will yield non-zero V_{off}, which can be calculated using (18). In practice, the main contributor to the mismatch between V_{S1} and V_{S2} is typically the mismatch in the device threshold voltages. It is understood from (18) that this component directly adds to the total latch offset.

In this brief, we are primarily interested in the influence of output capacitor mismatch (i.e., the mismatch between C_1 and C_2). Assuming that capacitor mismatch is the only source of mismatch between the two inverters stages, the offset voltage becomes

$$V_{\text{off}} = \left(\sqrt{\frac{C_2}{C_1}} - 1\right)(V_{\text{out2},0} - V_{S2}). \tag{19}$$

We further simplify (19) using two more definitions

$$C_1 \equiv C \tag{20}$$

$$C_2 \equiv C + \Delta C. \tag{21}$$

This yields

$$V_{\text{off}} = \left(\sqrt{1 + \frac{\Delta C}{C}} - 1\right)(V_{\text{out2},0} - V_{S2}). \tag{22}$$

Now assuming that $\Delta C/C$, is small, we arrive at the following simple formula that concludes the theoretical model 1

$$V_{\text{off}} = \frac{1}{2}\frac{\Delta C}{C}(V_{\text{out2},0} - V_{S2}). \tag{23}$$

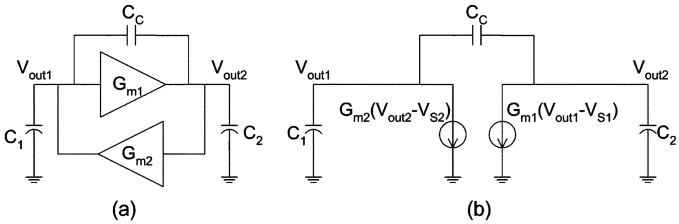

Fig. 5. Model 2. (a) Linearized back-to-back inverter stages with coupling capacitance C_C. (b) Circuit model.

B. Model 2

In a more realistic latch, the two outputs are capacitively coupled. Model 2 takes this into account (see Fig. 5). Similar to model 1, a set of two first-order differential equations is obtained using KCL for the output nodes, V_{out1} and V_{out2}, in Fig. 5(b)

$$(C_1 + C_C)\frac{dV_{\text{out1}}}{dt} = -G_{m2}(V_{\text{out2}} - V_{S2}) + C_C\frac{dV_{\text{out2}}}{dt} \tag{24}$$

$$(C_2 + C_C)\frac{dV_{\text{out2}}}{dt} = -G_{m1}(V_{\text{out1}} - V_{S1}) + C_C\frac{dV_{\text{out1}}}{dt} \tag{25}$$

Again, from these equations, we obtain a second-order differential equation for V_{out1}

$$\frac{d^2V_{\text{out1}}}{dt^2} + \frac{C_C(G_{m1} + G_{m2})}{C_1C_2 + C_CC_1 + C_CC_2}\frac{dV_{\text{out1}}}{dt} - \frac{G_{m1}G_{m2}}{C_1C_2 + C_CC_1 + C_CC_2}(V_{\text{out1}} - V_{S1}) = 0. \tag{26}$$

The two required initial conditions are given in (27) and (28). Equation (28) is obtained by evaluating both (24) and (25) at time zero and then solving for the first derivative of V_{out1}

$$V_{\text{out1}}(0) = V_{\text{out1},0} \tag{27}$$

$$\frac{dV_{\text{out1}}}{dt}(0) = -\frac{1}{C_1C_2 + C_CC_1 + C_CC_2} \times [G_{m2}(C_2 + C_C)(V_{\text{out2},0} - V_{S2}) + G_{m1}C_C(V_{\text{out1},0} - V_{S1})]. \tag{28}$$

The following equations (29)–(33) are definitions for algebraic convenience. α is defined as in (10):

$$\kappa \equiv (G_{m1} + G_{m2})^2C_C^2 + 4G_{m1}G_{m2}(C_1C_2 + C_CC_1 + C_CC_2) \tag{29}$$

$$\beta \equiv \alpha\sqrt{\frac{(C_2 + C_C)C_1}{(C_1 + C_C)C_2}\frac{\sqrt{\kappa} + (G_{m1} - G_{m2})C_C}{\sqrt{\kappa} - (G_{m1} - G_{m2})C_C}} \tag{30}$$

$$\gamma \equiv \alpha\sqrt{\frac{(C_2 + C_C)C_1}{(C_1 + C_C)C_2}\frac{\sqrt{\kappa} - (G_{m1} - G_{m2})C_C}{\sqrt{\kappa} + (G_{m1} - G_{m2})C_C}} \tag{31}$$

$$\tau_- \equiv \frac{\sqrt{\kappa} - (G_{m1} + G_{m2})C_C}{2G_{m1}G_{m2}} \tag{32}$$

$$\tau_+ \equiv \frac{\sqrt{\kappa} + (G_{m1} + G_{m2})C_C}{2G_{m1}G_{m2}}. \tag{33}$$

We now arrive at the following transient solution:

$$V_{\text{out1}}(t) = \frac{G_{m1}(C_1+C_C)\beta}{\sqrt{\kappa}} \times [\gamma(V_{\text{out2,0}}-V_{S2})+(V_{\text{out1,0}}-V_{S1})] \times \exp\left(-\frac{t}{\tau_-}\right) - \frac{G_{m1}(C_1+C_C)\gamma}{\sqrt{\kappa}} \times [\beta(V_{\text{out2,0}}-V_{S2})-(V_{\text{out1,0}}-V_{S1})] \times \exp\left(+\frac{t}{\tau_+}\right)+V_{S1} \quad (34)$$

$$V_{\text{out2}}(t) = \frac{G_{m1}(C_1+C_C)}{\sqrt{\kappa}} \times [\gamma(V_{\text{out2,0}}-V_{S2})+(V_{\text{out1,0}}-V_{S1})] \times \exp\left(-\frac{t}{\tau_-}\right) + \frac{G_{m1}(C_1+C_C)}{\sqrt{\kappa}} \times [\beta(V_{\text{out2,0}}-V_{S2})-(V_{\text{out1,0}}-V_{S1})] \times \exp\left(+\frac{t}{\tau_+}\right)+V_{S2}. \quad (35)$$

Note that when $C_C = 0$, these equations reduce to those obtained with model 1. Again, noting the fact that only the exponential terms with positive exponents are important in determining the final outputs and using the same definition of V_{out} in (16), we find

$$V_{\text{off}} \equiv \beta(V_{\text{out2,0}}-V_{S2}) - V_{\text{out2,0}} + V_{S1}. \quad (36)$$

Note that the only difference between (18) and (36) is that α in (17) has been replaced by β in (36). Since the focus of our study is the mismatch between the output capacitors, we again assume that the two inverter stages are matched except for $C_{1,2}$. Therefore, (36) reduces to

$$V_{\text{off}} = \left(\sqrt{\frac{C_2+C_C}{C_1+C_C}}-1\right)(V_{\text{out2,0}}-V_{S2}). \quad (37)$$

Combining (20), (21) and (37) now yields

$$V_{\text{off}} = \left(\sqrt{1+\frac{\Delta C}{C+C_C}}-1\right)(V_{\text{out2,0}}-V_{S2}). \quad (38)$$

To simplify further, we assume

$$\frac{\Delta C}{C+C_C} \ll 1. \quad (39)$$

We now arrive at the following simple offset voltage formula for model 2:

$$V_{\text{off}} = \frac{1}{2}\frac{\Delta C}{C+C_C}(V_{\text{out2,0}}-V_{S2}). \quad (40)$$

IV. Simulation Results

In order to validate the above-derived analytical models, we performed circuit level HSpice simulations. Our results are based on generic 0.18-μm BSIM3v3 CMOS models and

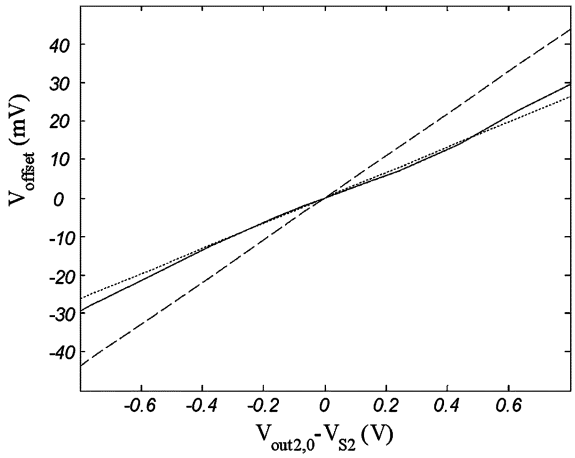

Fig. 6. Offset voltage for $\Delta C = 1$ fF. Dashed line: model 1; dotted line: model 2; solid line: HSpice simulation result.

$V_{\text{DD}} = 1.8\ V$ for the circuit in Fig. 1(b). In addition to the transistors' capacitances that are contained in C_1 and C_2 a capacitor ΔC was added to node V_{out2} to emulate mismatch. Fig. 6 shows simulation results using the following parameters:

$$(W/L)_{\text{nMOS}} = 1.8\ \mu\text{m}/0.18\ \mu\text{m} \quad (41)$$

$$(W/L)_{\text{pMOS}} = 3.6\ \mu\text{m}/0.18\ \mu\text{m} \quad (42)$$

$$\Delta C = 1\ \text{fF} \quad (43)$$

It is seen from Fig. 6 that both models follow the trend predicted by simulation correctly. Overall, model 2 matches the simulations more accurately, since it does not neglect the impact of coupling capacitance (C_C) between the output nodes. In practice, C_C stems mostly from gate-drain capacitance of the four transistors and can usually be estimated with sufficient accuracy from technology data.

The residual mismatch between simulation and model 2 mostly stems from voltage dependence of the involved capacitors. For simplicity, we used gate-source capacitance values that were extracted at the switching point of the inverters, regardless of the actual initial operating point. Toward the boundaries of the plot in Fig. 6, the devices approach the triode and/or cutoff regions, which leads to reduced capacitance C. From (40), we see that this leads to an increase in V_{off}, and this is also signified in the solid curve in Fig. 6. If desired, actual operating point data for the capacitances can be used to achieve better agreement of (40) with simulation data.

We have done similar simulations and comparisons for other mismatch values ranging from 1 fF to 20 fF and for various different device geometries. In all cases, model 2 was found to predict the offset with sufficient accuracy.

An important observation that follows from (40) and was confirmed through simulation is that the input-referred offset voltage due to capacitor mismatch is zero when $V_{\text{out2,0}} = V_{S2}$, and grows in magnitude when moving away from this condition. This suggests that in order to minimize dynamic offset, the latch should be initialized to operate as close as possible to the switching voltage of the inverters.

V. Conclusion

We have analyzed the effect of load capacitor mismatch on the offset voltage of a dynamic latch. Two simple equations for predicting the offset were derived and compared against simulation data. The presented example shows that a mismatch as small as 1 fF can lead to an offset of several tens of millivolts for a typical latch in 0.18-μm technology, where parasitic wiring capacitances are on the order of 0.2 fF/μm [10]. Hence, an imbalance in wiring of only 5 μm can lead to significant offset contributions. In order to cope with this effect, it is critical to ensure a well-balanced routing. Furthermore, as we have shown, operating the latch as close as possible to its inverters' thresholds can also help minimize the dynamic offset. As done in [8], one can deliberately introduce capacitance mismatch at the two output nodes to cancel the offset due to other sources that might be more difficult to control, like threshold voltage mismatches.

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