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Broadband and Energy-Efficient Power Amplifier Architectures

by

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Abstract

In this dissertation, power amplifier circuits and architectures are proposed that provide high efficiency for spectral-efficient high peak-to-average power ratio signals that are being used in modern communications systems. Using the proposed amplifier architectures and circuits high efficiency can be achieved in large frequency bandwidth.

The TLLM (Transformer-Less Load-Modulated) amplifier proposed in this dissertation is an amplifier that has similar efficiency performance to the Doherty amplifier, while it does not utilize any power combiner at the output. In the proposed TLLM amplifier, the two amplifier branches are connected directly together and provide high efficiency for high PAPR (Peak-to-Average Power Ratio) signals. A complete analysis is given for designing the two amplifier branches in the TLLM amplifier and a complete and comprehensive design procedure is provided for designing broadband TLLM amplifiers. Three different amplifier prototypes are also implemented using the TLLM architecture showing its performance and capability.

The second architecture proposed in this dissertation is a Doherty amplifier that utilizes three-port input and output networks. The analysis and flexible design procedure for designing a Doherty amplifier with three-port input/output networks is provided. The proposed analysis and design procedure can be used to design a Doherty amplifier with any output power ratio from the branches, and power division between the branch inputs. The proposed amplifier eliminates the need for any impedance inverter and offset lines at the input or output of the amplifier.

In the next part, a new biasing technique is proposed for transistors. It is shown that using this new biasing, transistors exhibit completely different behaviors from the conventionally biased transistors that can be used for different purposes. Two of the applications are studied in this dissertation. First, a multi-branch amplifier is presented which can provide

Doherty-like efficiency in a very large bandwidth. The second application is a linearizing driver amplifier. It is shown that using the proposed biasing scheme, a controlled amount of gain expansion can be achieved. The gain expansion can be used to compensate for the gain compression of the conventional power amplifiers to improve the amplifier's linearity without the need for additional linearizing circuitry or digital pre-distortion.

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To Zahra and Parsa

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List of Symbols, Abbreviations and Nomenclature

Symbol	Definition
2G	Second Generation
3G	Third Generation
4G	Fourth Generation
5G	Fifth Generation
AC	Alternating Current
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
ATC	American Technical Ceramics
BJT	Bipolar Junction Transistor
BO	Back-Off
bps	bits per second
CMOS	Complementary Metal Oxide Semiconductor
CW	Continuous Wave
dB	Decibel
dBc	Decibel relative to the carrier
dBm	Decibel-Milliwatts
DC	Direct Current
DE	Drain Efficiency
DPD	Digital Pre-Distortion
EDGE	Enhanced Data Rates for GSM Evolution
EER	Envelope Elimination and Restoration
EM	Electromagnetic
FET	Field-Effect Transistor

GaAs	Gallium Arsenide
GaN	Gallium Nitride
GHz	Gigahertz
GPRS	General Packet Radio Services
GSG	Ground-Signal-Ground
GSM	Global System for Mobile Communications
HBT	Heterojunction Bipolar Transistor
IBM	International Business Machines Corporation
IMD3	Third Order Intermodulation
IMDN	Input Matching/Dividing Network
IS-95	Interim Standard 95
ISS	Impedance Standard Substrate
ITU	International Telecommunication Union
I-V	Current-Voltage
LED	Light-Emitting Diode
LSSP	Large-Signal S-Parameters
LTE	Long-Term Evolution
mA	Milliamperes
MHz	Megahertz
mm	Millimetre
mmW	Millimetre Wave
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
mV	Millivolts
NMOS	N-channel MOSFET
OFDM	Orthogonal Frequency Division Multiplexing
OMCN	Output Matching/Combining Network

OPBO	Output Power Back-Off
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PDF	Probability Density Function
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RFPA	Radio Frequency Power Amplifier
SDR	Software Defined Radio
SiGe	Silicon-Germanium
SMS	Short Message Service
SOLT	Short-Open-Load-Thru
TLLM	Transformer-Less Load Modulated
TSMC	Taiwan Semiconductor Manufacturing Company
V	Volts
VNA	Vector Network Analyzer
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
Re	Real Part
∞	Infinity
λ	Wavelength
μm	Micrometre
Ω	Ohms
$\approx$	Approximately Equal to

Chapter 1

Introduction

1.1 Motivation

Modern wireless communication technologies experienced a large amount of growth in the last few decades. Wireless mobile networks experienced continuous increasing of data rate and service quality. As shown in Fig. 1.1, almost in every decade, a new generation of data communication standards is being introduced to the wireless communication world.

In 1980s the first generation of mobile communication systems were introduced to the world providing voice service using analog communications technology. The second generation (2G) was introduced in 1990s adding the data service capabilities starting with SMS (Short Message Service) text messages. The second generation cellular networks, such as GSM (Global System for Mobile Communications) and IS-95 (Interim Standard 95), was an evolution from the analog communications to digital and provided voice and low rate data services [1]. The GPRS (General Packet Radio Services) known also as 2.5G, made internet connections possible with the personal mobile communications and was a major evolution from 2G towards 3G. GPRS provided maximum theoretical data rate (downlink) of around 170 kbps and average data rates of around 40-50 kbps [2, 3]. With EDGE (Enhanced Data Rates for GSM Evolution) standard, the maximum theoretical data rate was increased to

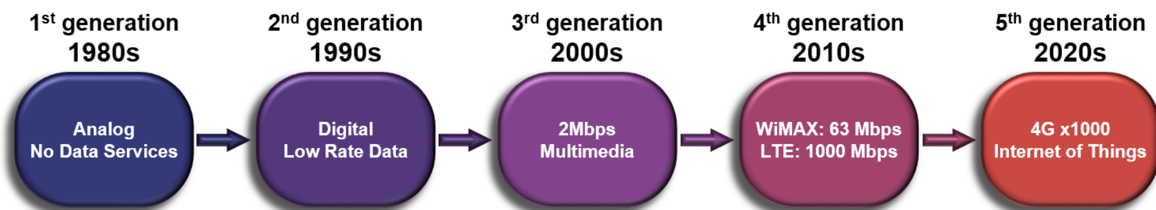


Figure 1.1: Mobile communication history and future.

250 kbps. The third generation (3G) was deployed in 2000s providing higher data rates (Maximum of 2 Mbps for stationary users) and numerous multimedia data communication services. In the recent years, the advent of 4G provides even higher data rates. WiMAX (Worldwide Interoperability for Microwave Access) which is considered to be a part of 4G can provide up to 63 Mbps data rate [4]. Newer 4G standard, LTE (Long Term Evolution), can provide maximum theoretical data rates of up to 1000 Mbps [5–7], but the realistic average data rate in an LTE network is on the order of 0.5-10 Mbps [7].

It is anticipated [8–11] that the fifth generation (5G) will begin to be deployed around 2020. 5G is anticipated to provide around 1000 times more data compared to the 4G standards. The main features of 5G communication standards are expected to be [8]:

1- Higher data rate: The total amount of data expected from 5G communication systems are expected to be around 1000 times higher than 4G systems. The cell edge rate or 5% data rate per user is expected to increase from current 1 Mbps in 4G to 100 Mbps in 5G (The peak rate expected from 5G networks is in the range of tens of Gbps). On the other hand, the number of users is expected to increase. The advent of "Internet of Things" will increase the number of connected devices to tens or even hundreds of times with a network of sensors [12]. These changes will lead to the need for the dramatic increase of around 1000 times in the network capacity.

2- Reasonable energy consumption and cost: For 5G to be viable, the energy consumption and costs per user has to remain almost unchanged from the previous generations. Considering the increase in the bit rate, this means that the energy per bit needs to be decreased by around 1000 times to keep the energy consumption in the same level. This means that the mobile stations can work at the new high data rates while consuming the same amount of energy as 4G networks and hence can operate with existing battery technologies. Keeping the energy costs constant, the service providers can provide their services with almost the same cost to the users.

Considering the radical expansion of data in the next generation and the obvious need for profitability of the forthcoming systems, *"Energy efficiency will be a major research theme for 5G"* [8](©2014 IEEE).

On the other hand, the continuous advancement of wireless standards forces the service providers to change their infrastructure to upgrade to new standards. Upgrading the hardware, imposes very large amounts of expense to service providers and also has many environmental drawbacks since the old hardware needs to be recycled or disposed.

In recent years, there is a large tendency toward software defined radios (SDRs) that can operate in different standards and frequency bands with the same hardware [13, 14]. SDRs can decrease the costs for further developments and upgrades in systems. Therefore, the hardware implemented in these systems should be capable of working with different standards. To meet these criteria, the wireless transceivers need wideband analog circuitry that cover a large frequency band. It makes the system flexible to work in different frequency bands specified for different standards. The wireless transceiver should also be able to work with a variety of communication signals, while maintaining signal's quality and high energy efficiency.

Although sophisticated modulation techniques are being used to increase the spectral efficiency of communication signals, covering the need for the data rate in the next wireless generations still demands a very large frequency bandwidth. One of the solutions is to use the mmW frequency range especially the unlicensed band around 60 GHz [8, 15, 16]. There is a large amount of research on the 60 GHz analog circuits to improve their performance. The energy efficiency of the 60 GHz circuits is one of the main research areas since the semiconductor technologies have lower efficiency in the mmW frequencies.

The mmW frequencies and especially the 60 GHz band have high attenuation in the free space which limits the transmission range to a few meters. The limited range adds the advantage of frequency re-use in short range, but it makes mmW frequencies unusable for

larger cells. For larger cells, underutilized licensed bands in the lower portion of frequency spectrum can be used as a shared bandwidth using cognitive radios [17,18]. Cognitive radios also should be able to work in a large frequency bandwidth so they can utilize any available frequency band that is not being used by other services.

1.2 The Role of RF Power Amplifier

The RF power amplifier is considered to be the most power dissipating component in a wireless transceiver [19–22]. This means that any attempt for the efficiency enhancement in a wireless transceiver has to start from the power amplifier.

In a base station, improving the efficiency of the RF power amplifier results in considerable energy savings not only in the amplifier itself, but also in the peripheral facilities. As an example, consider a wireless transmitter transmitting an average of 10 watts RF output power. If the power amplifier has an efficiency of 20%, then the DC power delivered to the amplifier is 50 watts. 10 watts of the DC power is delivered to the load as the output RF power, and 40 watts is dissipated as heat in the power amplifier. If the efficiency of the amplifier improves to 30%, then the dissipated power in the power amplifier will decrease to 23 watts which is almost half of the previous case. It means that by improving efficiency from 20% to 30%, the amount of heat generated in the power amplifier will decrease almost by half, consequently the amplifier needs much less cooling power. On the other hand, due to decreased heat generation, the equipment room needs less cooling power or even the need for cooling system might be completely eliminated. In mobile stations, a high efficiency power amplifier means longer battery life when connected to the network.

1.2.1 Efficiency, Linearity and Bandwidth

The performance of a power amplifier is mainly evaluated by its frequency of operation, output power, energy efficiency and linearity. There is a trade-off between the energy efficiency

and linearity of a power amplifier. A power amplifier's efficiency usually increases when its output power is close to its maximum rated output power, but the power amplifiers usually show nonlinear effects when working close to saturation.

Frequency of operation and frequency bandwidth also affect the efficiency of a power amplifier. The performance of the solid-state transistors used in power amplifiers usually degrade by increasing the frequency of operation. This results in the degradation of gain and energy efficiency. The amplifier's bandwidth also affects the performance of the amplifier since realizing the matching networks in a large bandwidth cannot be easily done for any type of impedance trajectories required by the transistor.

1.2.2 Power Amplifiers and High PAPR Signals

Modern wireless communication systems use complicated modulation schemes to exploit the frequency spectrum in the most efficient way. The high order modulation schemes such as 64 QAM and 256 QAM are proposed for wireless communication systems [23, 24]. These modulation schemes provide higher data rates by increasing the number of bits per symbol in the same frequency bandwidth. Also multiplexing schemes such as OFDM (Orthogonal Frequency-Division Multiplexing) result in system robustness against the effects of the environment on the signals such as multi-path fading.

These modulations and multiplexing schemes present high crest factors or high Peak-to-Average Power Ratios (PAPR). With a high PAPR signal, the peak transmitted power is much higher than the average RF output power.

For a power amplifier fed by a high PAPR signal, the average output power is much lower than the maximum output power. In other words, the power amplifier has to work in large power back-off. The classical power amplifier's efficiency decreases at power back-off. Fig. 1.2 shows the probability density function (PDF) of a high PAPR signal along with the efficiency of a conventional power amplifier. As can be seen from the figure, the PDF is concentrated in the low power range which means most of the times, signal's amplitude is

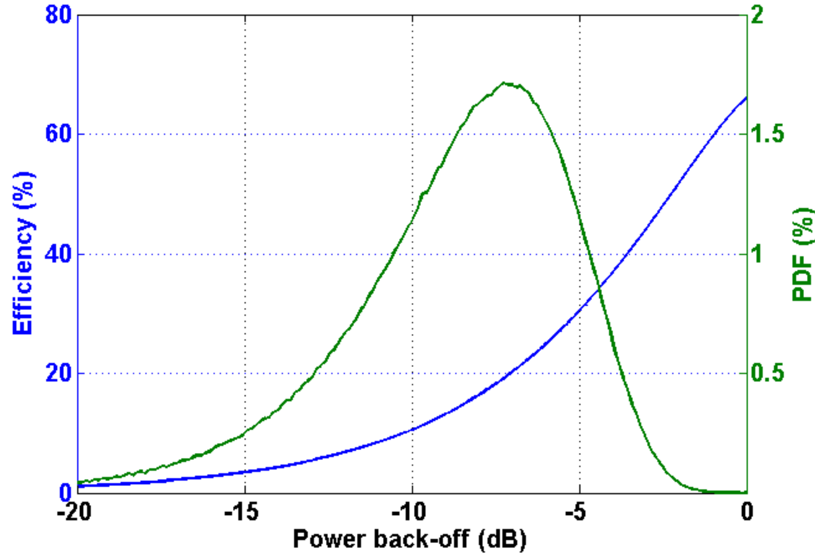


Figure 1.2: Probability density function of a high PAPR signal and amplifier's efficiency.

much lower than the the signal's peak amplitude. This means that most of the times, the amplifier is working in the low efficiency range. Consequently, in this case, the amplifier's average efficiency is in the range of 15-20% while the amplifier's peak efficiency is higher than 60%.

There are different solutions for achieving high efficiency at power back-off, such as envelope elimination and restoration (EER) [25], the Chireix outphasing method [26], envelope tracking [27], and the Doherty amplifier [28].

The Doherty amplifier's structure is one of the most widely used methods for improving the efficiency at power back-off. It employs load modulation to have amplifiers working in high-efficiency regions for a certain range of output power. A large number of research papers are recently published on the Doherty amplifiers aiming at improvement in the efficiency and increasing its operational frequency bandwidth [29–38].

1.3 Objectives of This Work

As discussed in the previous sections, two of the challenges in the forthcoming wireless technologies are the energy efficiency and frequency bandwidth. Some solutions are proposed

in the literature to address these challenges, but there is still a need for improvement to meet the requirements of the future wireless standards.

The main objective of this work is to find new power amplifier structures and design procedures to achieve high efficiency, large bandwidth and design flexibility. Obtaining high energy efficiency over a wide frequency band is challenging and currently there is a lot of research going on to address this need. In this work, the existing amplifier structures and their limitations will be studied and the objective is to either modify the structures to remove the limitations or to propose new structures and design procedures that do not have those limitations in terms of energy efficiency and frequency bandwidth.

On the other hand, current amplifier structures may be suitable for a specific technology or a specific frequency range. Some structures have restrictions on the active devices or the technology and are limited to the specific conditions. In this work the objective is to provide generic amplifier structures and design procedures suitable for implementation in different technologies and frequency bands.

1.4 Contributions of This Work

The use of spectral efficient high PAPR communication signals in modern wireless communication systems results in considerable degradation of power amplifier's energy efficiency. There are solutions to improve the efficiency of a power amplifier working in power back-off. The Doherty amplifier is one possible solution to improve amplifier's average efficiency with high PAPR signals.

The need for broadband transmitters require broadband power amplifiers. The classical Doherty amplifier suffers from bandwidth limitation mainly due to frequency dependent Doherty output power combiner. There are solutions for increasing the Doherty amplifier's operational bandwidth by optimizing the Doherty combiner for bandwidth enhancement [32–38].

On the other hand, the main source of nonlinearity on a transmitter system is the power amplifier. To compensate for the nonlinearities, different forms of linearization techniques are used. Analog pre-distorters produce controlled nonlinear behaviors to compensate for the power amplifier nonlinearities. Analog pre-distorters usually utilize diode or transistor-based circuits to generate the desired nonlinear behavior for power amplifier nonlinearity compensation [39–47]. Digital pre-distorters generate the desired nonlinearity through digital signal processing [48–55] which consume power from the power supply, leading to degradation of energy efficiency.

In this dissertation, the load modulation technique which is the fundamental idea behind the Doherty amplifier is used to propose new amplifier structures which do not use the Doherty amplifier's output combiner. Different amplifier structures introduced in this dissertation, provide different features and design flexibilities for the intended application and technology. The main contributions in this dissertation can be summarized as follows:

- The Transformer-Less Load Modulated (TLLM) amplifier structure. The full analysis and a complete design procedure is provided for designing broadband TLLM amplifiers providing high efficiency at large output power back-off (**P1, P7**).

- Extending the TLLM concept to mm-wave integrated circuit design and validating it by designing and implementing a TLLM amplifier in 60 GHz frequency using 65nm bulk CMOS technology, showing the suitability of the TLLM amplifier for millimetre-wave applications (**P2, P4, P5, P6, P9**).

- A generic topology for Doherty power amplifier employing three-port input and output networks. This amplifier provides flexible design for complex source/load impedances. A complete analysis and design procedure is provided for this amplifier's topology (**P3**).

- Proposing a new biasing scheme for power amplifiers using a constant current source rather than a voltage source. Using the new biasing scheme, the transistor's behaviour is completely different from the conventional biasing which opens the doors towards new classes of amplifiers and applications (**P8**).

- A new broadband power amplifier providing high efficiency at power back-off employing a current biased amplifier branch and one or more voltage biased amplifier branch(es). This structure can operate in very large frequency bandwidth of a few octaves (**P8**).

- An amplifier circuit presenting a predefined amount of gain expansion. This amplifier can be used as a driver amplifier to compensate for the gain compression of the conventional power amplifiers. A complete analysis and design procedure is given to design these types of amplifiers in CMOS technology.

1.4.1 List of Publications

The following is a list of publications resulted from the work carried out for this thesis:

Journal Papers

P1: M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "A Transformer-Less Load-Modulated (TLLM) Architecture for Efficient Wideband Power Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2863-2874, Sep. 2012.

P2: M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "A 60 GHz CMOS Power Amplifier with High Efficiency for High PAPR Signals", Submitted to *Wiley International Journal of RF and Microwave Computer-Aided Engineering.*

P3: M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "Analytical Design Methodology for Generic Doherty Amplifier Architecture Using Three-Port Input/

Output Networks", Submitted to *IEEE Transactions on Microwave Theory and Techniques.*

Conference Papers and Workshops

P4: M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "A 60 GHz Dual-Mode Amplifier in 65nm CMOS Technology", in *54th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2011)*, Seoul, Korea, pp. 1-4, 7-10 August 2011.

P5: F. M. Ghannouchi, M. Akbarpour and M. Helaoui, "CMOS mmW Doherty Power Amplifiers", in *RF and mmW PAs: Linearization and Power Challenges Workshop, 2012 International Microwave Symposium (IMS2012)*, Montreal, QC, Canada, 17-22 June 2012.

P6: M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "A 60GHz CMOS Class C Amplifier Intended for Use in Doherty Architecture", in *2012 IEEE International Conference on Wireless Information Technology and Systems (ICWITS 2012)*, Maui, HI, USA, pp. 1-4, 11-16 November 2012.

P7: M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "Broadband Doherty Power Amplifiers", in *2013 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR 2013)*, Austin, TX, USA, pp. 1-3, 20-23 January 2013.

Patent

P8: M. Akbarpour, F. M. Ghannouchi and M. Helaoui, "High Efficiency Ultra-Wideband Amplifier", PCT patent application, filed February 2014.

Book Chapter

P9: M. Akbarpour, F. M. Ghannouchi and M. Helaoui, “mmW Doherty” in *Linearization and Efficiency Enhancement Techniques for Silicon Power Amplifiers, From RF to mmW*, Academic Press, on press, Feb. 2015.

1.5 Thesis Outline

The dissertation is organized as follows:

A major part of this thesis is based on the load modulation similar to the Doherty amplifier. For this reason, in Chapter 2, an overview of the Doherty amplifier, its working principles and the practical design challenges is presented.

In Chapter 3, the Transformer-Less Load-Modulated (TLLM) amplifier is presented. The TLLM amplifier provides high efficiency at power back-off similar to Doherty amplifier. Contrary to the Doherty amplifier, the TLLM amplifier does not utilize an output power combiner. In TLLM amplifier, the two amplifier branches are connected directly together without the need for an output power combiner. In Chapter 3, it is shown that the amplifier can be designed to operate as a broadband high efficiency power amplifier. A detailed analysis and design procedure is provided for designing broadband TLLM power amplifiers.

In Chapter 4, another amplifier structure is proposed for designing power amplifiers with high efficiency at large output power back-off. The proposed amplifier utilizes one three-port input network and one three-port output network. Contrary to the Doherty amplifier, the proposed amplifier can be designed for any arbitrary complex source and load impedances. A complete analysis and detailed design procedure is given for designing three-port input and output networks. The proposed analysis and design procedure is also very flexible because it can be applied to any dual branch amplifiers with any combination of transistors, output powers, input power division and any required phase shift at the input. One possible implementation of the three-port networks is also provided in Chapter 4 which gives very compact amplifier footprint suitable for integrated designs.

Chapter 5 introduces a new high efficiency broadband amplifier capable of providing high efficiency at large output power back-off in multiple octaves of frequency bandwidth. This amplifier utilizes a current-biased amplifier and one or more voltage biased class C amplifiers. First, feasibility of implementing current-biased amplifiers is discussed, then the power amplifier design and test results are provided.

In Chapter 6, another application of current-biased transistors is introduced. It is shown that the current biased amplifiers can provide a controlled gain expansion. A complete analysis and design procedure is provided for designing a driver amplifier that compensates for the gain compression of a power amplifier in CMOS technology.

Chapter 7 concludes the dissertation with a summary of this work, the key points and main contributions of the dissertation.

Chapter 2

The Doherty Amplifier

Modern communication systems use spectrum efficient modulation schemes to maximize the data transmission rate. The spectrum efficient signals usually have large peak-to-average power ratios (PAPR) . As discussed in Chapter 1, high PAPR signals lead to low efficiency in the RF power amplifier. The amplifier structure proposed by W. H. Doherty [28] provides high efficiency in power back-off leading to high efficiency for high PAPR communication signals.

Most of the work done in this research is based on the load modulation similar to the Doherty structure. In this chapter, the Doherty structure, its working principles and design considerations are presented.

2.1 Load Modulation Concept and the Doherty Amplifier Structure

In classical (class A, AB, B or C) power amplifiers, the efficiency depends on the class of amplifier and the output power. The DC component (I_{DC}) and fundamental component (I_1) of the drain current of an amplifier can be obtained respectively as [56]:

$$I_{DC} = \frac{I_{max}}{2\pi} \frac{2\sin(\theta_c/2) - \theta_c \cos(\theta_c/2)}{1 - \cos(\theta_c/2)} \tag{2.1}$$

$$I_1 = \frac{I_{max}}{2\pi} \frac{\theta_c - \sin\theta_c}{1 - \cos(\theta_c/2)} \tag{2.2}$$

In (2.1) and (2.2), θ_c is the conduction angle and I_{max} is the maximum drain current. Assuming ideal transistor (zero knee voltage) and having the load impedance of R_L at fundamental frequency, the amplifier's drain efficiency can be calculated as:

$$\eta = \frac{I_1^2 R_L/2}{I_{DC} V_{DC}} = \frac{I_{max} R_L}{4\pi V_{DC}} \frac{(\theta_c - \sin\theta_c)^2}{(1 - \cos(\theta_c/2))\,(2\sin(\theta_c/2) - \theta_c \cos(\theta_c/2))} \tag{2.3}$$

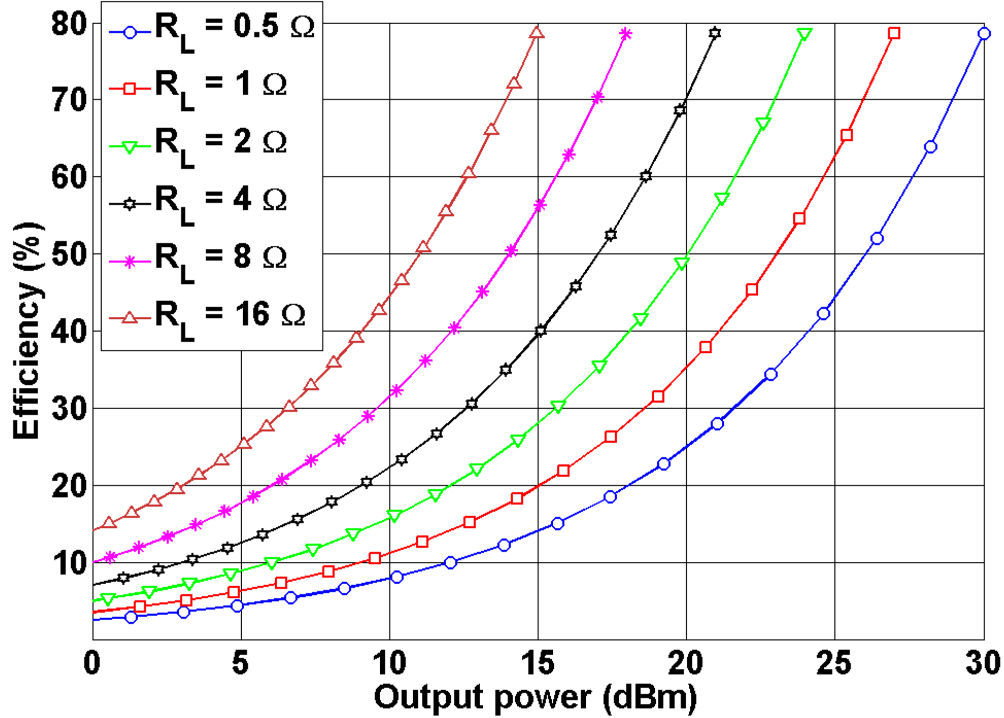


Figure 2.1: Efficiency of a class B amplifier for different load impedances

Fig. 2.1 shows the value of efficiency versus output power for class B amplifier ($\theta_c = \pi$) for normalized case of $V_{DC} = 1$. The maximum efficiency occurs when $R_L I_1 = V_{DC}$ which is met when the amplifier works at maximum output voltage swing. Having maximum output voltage swing means that the amplifier delivers its maximum output power or in other words it works in saturation. As can be seen from Fig. 2.1, for a class B amplifier, maximum output power is inversely proportional to the load impedance and the maximum efficiency is the same for all load impedances. The relation between the load impedance and maximum output power can also be seen from the transistor's load line. In Fig. 2.2, the load lines are shown for an amplifier at different load impedances. For lower load impedances, the maximum current swing increases which means that the transistor can inject more current into the load and hence delivering more output power to the load impedance.

The Doherty amplifier utilizes this behaviour to provide high efficiency at power back-off. The Doherty amplifier's structure is shown in Fig. 2.3. It is composed of two amplifier

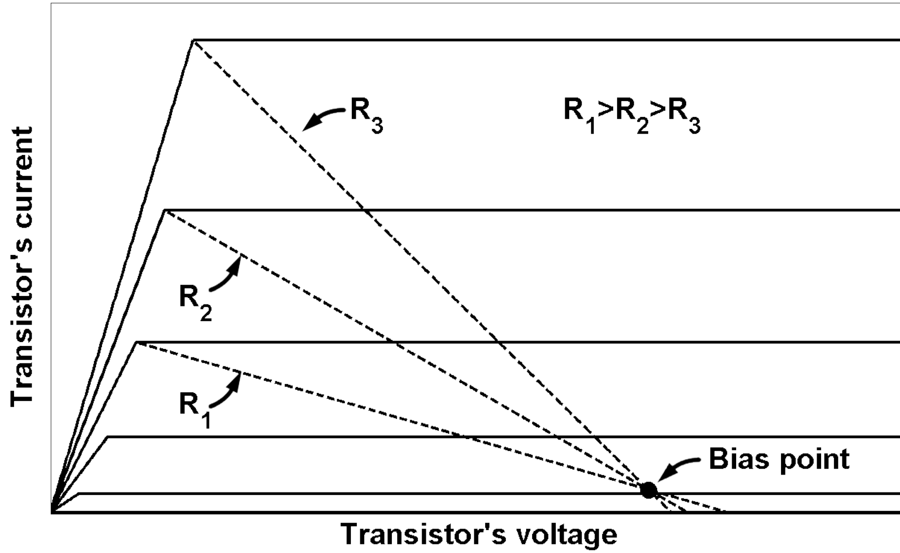


Figure 2.2: Typical transistor's load lines.

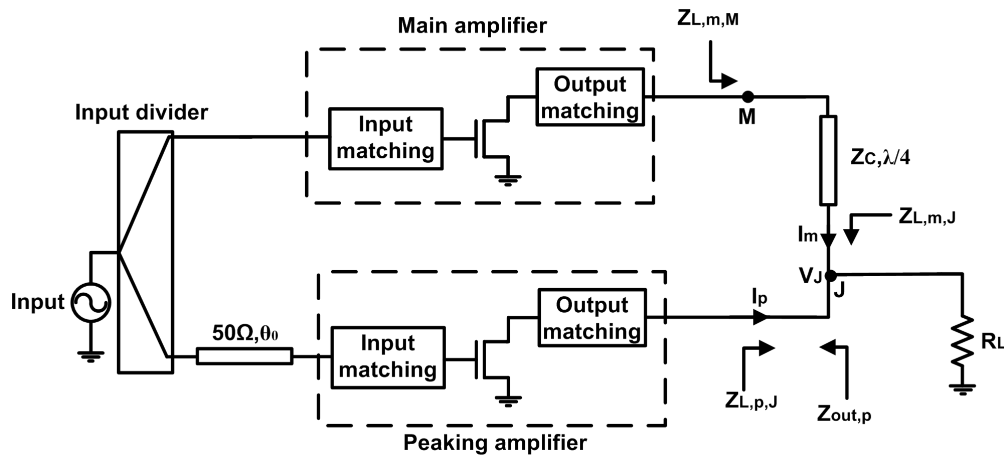


Figure 2.3: The Doherty amplifier's structure

branches. One amplifier branch is called the main (or the carrier) amplifier and the second amplifier branch is called peaking (or auxiliary) amplifier. The main amplifier is usually a class AB or class B amplifier and the peaking amplifier is a class C amplifier. At low input power, the peaking amplifier is turned off and only the main amplifier delivers power to the load impedance. When the main amplifier reaches saturation, the peaking amplifier turns on and changes the load impedance seen by the main amplifier to keep it in saturation and hence provide high efficiency at a large range of output powers.

The load impedance seen by the main amplifier branch at point J can be expressed as:

$$Z_{L,m,J} = \frac{V_J}{I_m} = \frac{R_L(I_m + I_p)}{I_m} = R_L\left(1 + \frac{I_p}{I_m}\right) \tag{2.4}$$

and the load impedance seen by the peaking amplifier branch at point J can be expressed as:

$$Z_{L,p,J} = \frac{V_J}{I_p} = \frac{R_L(I_m + I_p)}{I_p} = R_L\left(1 + \frac{I_m}{I_p}\right) \tag{2.5}$$

It means that the load impedance seen by the two amplifier branches change after the peaking amplifier starts to deliver current to the load. At power back-off, assuming that the peaking amplifier presents a very high output impedance compared to the load impedance ($Z_{out,p} >> R_L$), the peaking amplifier's output current is zero because the peaking amplifier is in the *off* state and it does not generate or draw any output current. Then, from (2.4), the main amplifier's back-off load impedance is equal to $Z_{L,m,J,BO} = R_L$ and from (2.5) the peaking amplifier's back-off load impedance is equal to $Z_{L,p,J,BO} = \infty$.

At maximum output power, the load impedances for the main branch is $Z_{L,m,J,PK} = R_L(1 + I_{p,max}/I_{m,max})$ and the load impedance for the peaking branch is $Z_{L,p,J,PK} = R_L(1 + I_{m,max}/I_{p,max})$ where $I_{m,max}$ and $I_{p,max}$ are the main and peaking amplifier's currents at peak output power respectively. We can say that after the peaking amplifier turns on, it changes the load impedance seen by the main branch from R_L at power back-off to $R_L(1 + I_{p,max}/I_{m,max})$ at peak output power. The load impedance seen by the peaking branch changes from ∞ at power back-off to $R_L(1 + I_{m,max}/I_{p,max})$ at peak output power.

It should be noted that $I_{m,max}$ and $I_{p,max}$ can be complex-valued quantities since each amplifier branch may have a different phase shift compared to the input signal. For efficient power combining, the output currents from the two amplifier branches have to be in-phase which means that $I_{p,max}/I_{m,max}$ should be a real and positive quantity. This means that the load impedance seen by the main amplifier branch increases by a factor of $1 + I_{p,max}/I_{m,max}$. This effect is called the load modulation which is the main working principle of the Doherty amplifier.

From Fig. 2.1 and Fig. 2.2, for the main amplifier to remain in saturation in a range of output powers beyond the turn-on point of the peaking amplifier, its load impedance has to decrease, but the load impedance seen by the main branch increases with the output power. The Doherty structure utilizes an impedance inverter in the main branch to reverse the load modulation at the main amplifier's output. The impedance inverter is usually a quarter-wave (or $\lambda/4$) transmission line at the frequency of operation. From the transmission line theory, the main amplifier's load impedance $Z_{L,m,M}$ can be expressed versus $Z_{L,m,J}$ as:

$$Z_{L,m,M} = \frac{Z_C^2}{Z_{L,m,J}} \tag{2.6}$$

which means that the load impedance seen by the main amplifier decreases by a factor of $1 + I_{p,max}/I_{m,max}$ from back-off to peak power.

The peaking amplifier in the Doherty structure is a class C amplifier. The bias point for the peaking amplifier is usually selected such that the peaking amplifier turns on when the main amplifier reaches saturation. It means that the main amplifier reaches its maximum efficiency and then by increasing the input power, the peaking amplifier decreases the load seen by the main amplifier, causing its output power to increase while it remains in saturation and hence provides high efficiency. For a symmetrical Doherty amplifier having $I_{p,max}/I_{m,max} = 1$, the back-off range that the main amplifier is in saturation is equal to 6 dB. After the main amplifier saturates, the peaking amplifier turns on and the main amplifier's load impedance decreases by a factor of 2, hence the maximum output power increases by 3 dB. The peaking amplifier also adds another 3 dB to the output power since in theory, it delivers the same amount of power as the main amplifier, resulting in 6 dB power back-off range.

Efficiency of a Doherty amplifier can be calculated for two regions based on the peaking amplifier's state. At power back-off, the peaking amplifier is turned off and the efficiency of the Doherty amplifier is that of the main amplifier. In this region, the efficiency of a

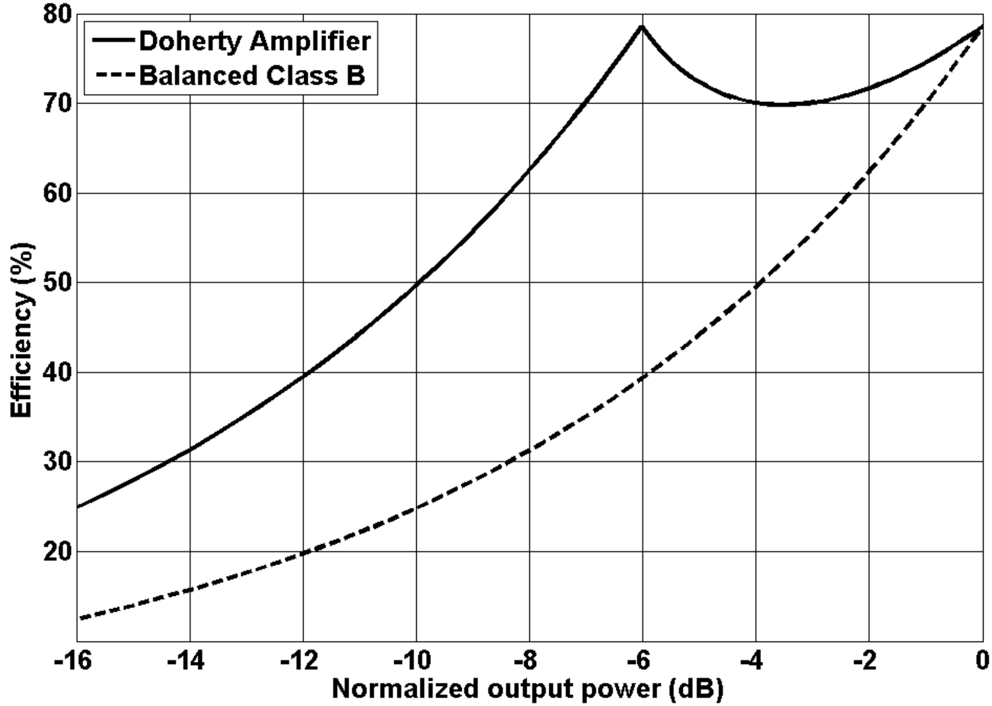


Figure 2.4: Symmetrical Doherty amplifier's efficiency versus output power

symmetrical Doherty amplifier can be expressed as [56]:

$$\eta = \frac{\pi v_{in}}{2V_{max}}, \quad 0 \leq v_{in} \leq V_{max}/2 \tag{2.7}$$

In (2.7), v_{in} is the input signal's magnitude and V_{max} is the input signal's magnitude at maximum input power. After the main amplifier saturates, the overall efficiency of the symmetrical Doherty amplifier as a function of input drive is given by [56]:

$$\eta = \frac{\pi}{2} \frac{(v_{in}/V_{max})^2}{3v_{in}/V_{max} - 1}, \quad V_{max}/2 < v_{in} \leq V_{max} \tag{2.8}$$

The efficiency of a symmetrical Doherty amplifier is plotted versus normalized output power in Fig. 2.4 along with the efficiency of a balanced amplifier having two identical class B power amplifiers in both branches. The efficiency of a Doherty amplifier is twice the efficiency of a balanced class B amplifier for the low power region (before the peaking amplifier turns on). After the peaking amplifier turns on, the Doherty amplifier's efficiency

remains higher than 70% which is higher than the efficiency of the balanced class B amplifier.

2.2 Doherty Amplifier Design, Practical Design Considerations

The Doherty amplifier's theory is based on the load-line analysis at the output terminal of transistor. The load lines shown in Fig. 2.2, are obtained for an ideal transistor and usually the optimum load impedances considered are a resistive load obtained from the load lines.

In practice however, the transistor has parasitic elements that change the optimum load impedance compared to the ideal case. Most of the transistors have an output capacitance which changes the optimum load to a complex-valued impedance. The complex-valued optimum impedance can be obtained using the transistor model or from load-pull simulation or measurements.

To convert the load impedance to the complex-valued optimum load impedance, a matching network is used to convert R_{opt} to the complex-valued optimum load impedance. The matching network can be designed using different circuit topologies and using different circuit elements. Different circuits may convert the back-off load impedance to different load impedances at the transistor drain. Due to the effects of the parasitics and the matching network, the load impedance at power back-off may be converted to a set of load impedances. To obtain the best performance at power back-off, usually offset lines are used at the output of the main and peaking branches [31, 57, 58]. The offset lines are segments of transmission lines. The offset line's length is selected to give the best performance at power back-off. The main and peaking branch offset lines are shown in Fig. 2.5.

An important parameter in the Doherty structure is the peaking amplifier's output impedance ($Z_{out,p}$ in Fig. 2.3). At power back-off, the load impedance seen by the main branch is equal to the parallel combination of the load impedance and the peaking amplifier's output impedance. To minimize the dissipation of the RF output power in the peaking amplifier's output impedance, usually the output impedance of the peaking ampli-

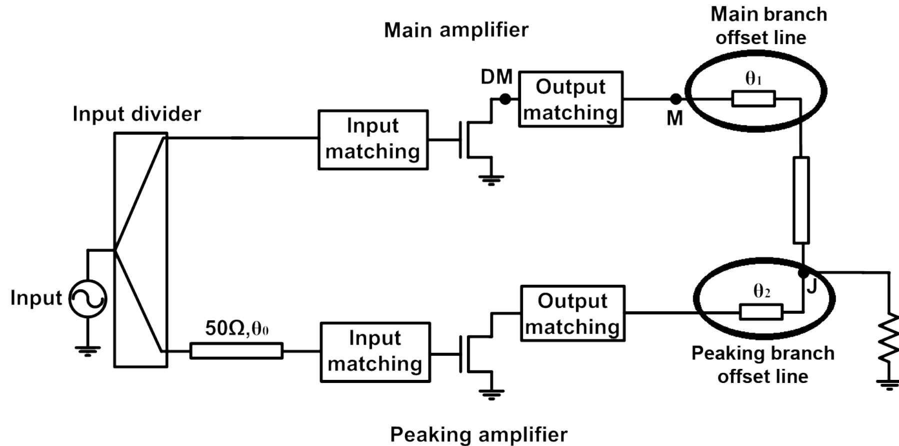


Figure 2.5: The Doherty amplifier employing offset lines at the output.

fier is transformed to a high impedance using an offset line at the output of the peaking branch [31, 57, 58]. For the peaking offset line to have no effect at the peak output power, the characteristic impedance of the peaking offset line is selected to be $R_L(1+I_{m,max}/I_{p,max})$ (from (2.5)). The peaking branch offset line is shown in Fig. 2.5.

In some cases, the output impedance of the peaking amplifier may have low reflection coefficient. This may happen when the output impedance of the class C biased transistor is not on the edge of the Smith chart or the elements used as the peaking amplifier's matching network are lossy elements. Both of these conditions usually exist at very high frequencies such as mmW frequencies. This means that the real part of the peaking amplifier's output impedance may cause some degree of power loss at the power back-off, leading to lower efficiency at power back-off.

Another factor that can affect the Doherty amplifier's performance, is the different behaviour of the main and the peaking amplifier. Due to the difference between the bias points in the two branches, the AM/PM characteristics of the transistors may be different [59]. The difference between the AM/PM characteristics may cause the output powers from the two branches not to combine efficiently in some input power levels leading to performance degradation in some power levels.

2.3 Broadband Doherty Amplifiers

The classical Doherty amplifier utilizes a quarter-wave impedance transformer and offset lines at the output of the amplifier branches. The quarter-wave transformer and the offset lines are frequency-dependent elements. This means that the required performance from each of these elements are only met in a limited frequency bandwidth which means that the Doherty amplifier's operational bandwidth is limited.

Due to the need for high efficiency and broadband power amplifiers, numerous works are done to increase the operational bandwidth of the Doherty amplifier [32–38]. In [32], the frequency response of the impedance inverter is studied and guidelines are given for the selection of the characteristic impedance for the impedance inverter in the Doherty structure and a Doherty amplifier having 42% fractional bandwidth is implemented. In [33], an additional circuit is added to the output of the peaking amplifier to reduce the quality factor of the matching circuit to the final load and hence increase the bandwidth. In [34], a low quality factor quarter-wave transformer, a phase compensation circuit and an additional offset line is implemented in the matching networks to obtain larger operational bandwidth for the Doherty amplifier. In [35], broadband amplifiers were designed for the main and peaking amplifiers and the conditions for connecting them in a Doherty structure which give broadband operation are studied and a Doherty amplifier with 26% fractional bandwidth is designed.

In this dissertation, two other structures are proposed to obtain high efficiency at power back-off in a large frequency bandwidth. The Transformer-Less Load-Modulated (TLLM) amplifier completely eliminates the need for a power combining network by giving guidelines on how to design the two amplifier branches such that they can be connected directly together and obtain wideband Doherty performance. Also a new multi-branch amplifier is proposed which utilizes a current-biased amplifier as the main amplifier branch which is capable of operating in a very large frequency bandwidth.

Chapter 3

The Transformer-Less Load-Modulated (TLLM) Amplifier

As discussed in the previous chapter, the Doherty amplifier utilizes an impedance inverter to provide the proper load modulation for the main amplifier. The Doherty power combiner is a non-isolated power combiner, hence allowing the load modulation to take place. This chapter presents the Transformer-Less Load-Modulated (TLLM) amplifier (©2012 IEEE) [1]. In terms of efficiency, the TLLM amplifier provides the same performance as the Doherty amplifier, but it is capable of operating in a larger bandwidth. It is shown that by proper design of the two output matching networks in the two branches there will be no need for a combiner circuit. In TLLM amplifier, the two amplifier branches can be connected directly together. Since there is no power combiner in the TLLM amplifier, the combining losses are minimized and there are less limitations on bandwidth and consequently it can provide high efficiency at large frequency bandwidth. In Section 3.1, the structure and the design goals of the TLLM amplifier are introduced. The design of the main branch is presented in Section 3.2 and the design of the peaking amplifier branch is given in Section 3.3. The synthesis techniques of the output matching networks are discussed in Section 3.4 for narrowband and wideband design cases. In Section 3.5, a systematic design procedure for the TLLM amplifier is given . Some implementations of the TLLM amplifier and the amplifier performances are presented in Section 3.6.

[1] M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "A Transformer-Less Load-Modulated (TLLM) Architecture for Efficient Wideband Power Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2863-2874, Sep. 2012.

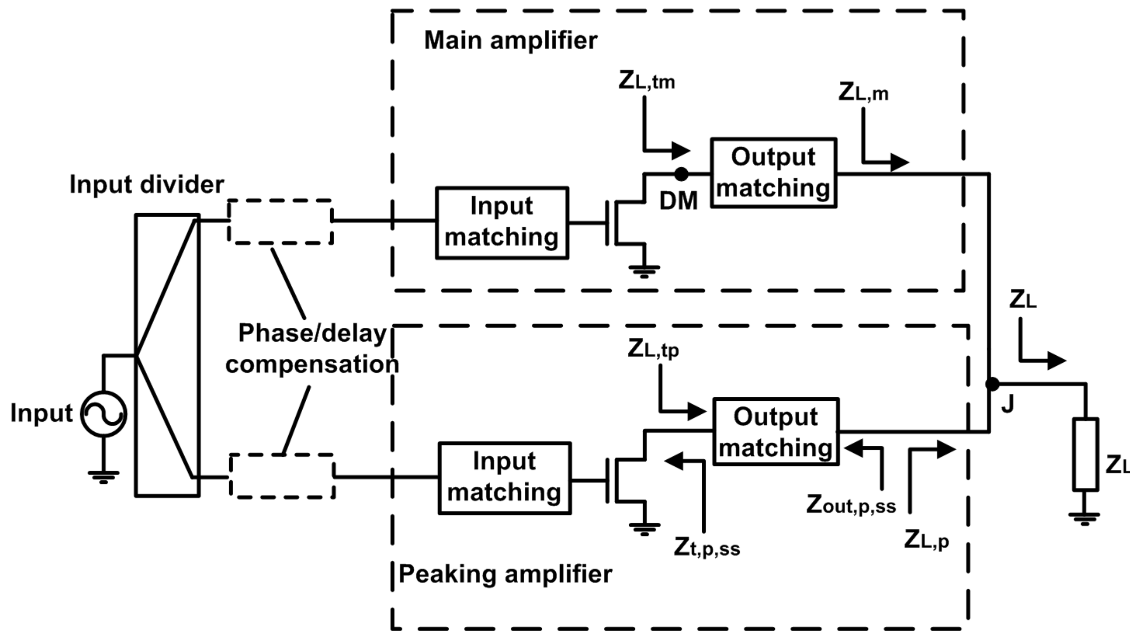


Figure 3.1: The Transformer-Less Load Modulated (TLLM) amplifier's structure

3.1 The TLLM Amplifier's Structure and Design Goals

The structure of the TLLM amplifier is shown in Fig. 3.1. Similar to the Doherty amplifier, the TLLM amplifier utilizes two amplifier branches. The main amplifier is a class AB or class B biased amplifier and the peaking amplifier is a class C biased amplifier. At low input power range, only the main amplifier amplifies the signal and the peaking amplifier is turned off. At higher input power range, both amplifiers contribute in delivering RF power to the load. Similar to Doherty amplifier, the number of peaking amplifier branches can be increased to boost the efficiency at higher output power range.

In the TLLM architecture, the transformer used in the Doherty structure is avoided. As a result, the load modulation at the output of the main amplifier is different from the Doherty amplifier. To show the difference, consider the two architectures shown in Fig. 2.3 and Fig. 3.1 with the same load impedance of 50 Ω. For comparison consider that the two branches have the same amount of output powers at peak input power and the peaking amplifier has high output impedance (these conditions are not necessary in TLLM amplifier).

In this case, for the Doherty amplifier, the main amplifier has 100 Ω load impedance at

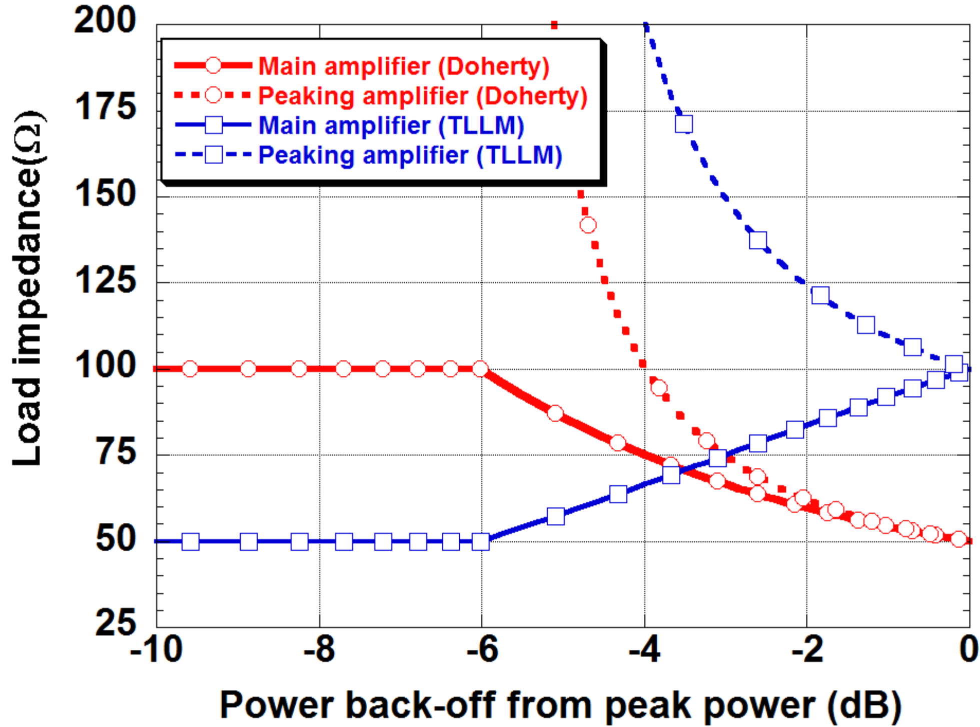


Figure 3.2: Load modulation in symmetrical Doherty and TLLM architectures.

power back-off and in the last 6 dB output power range; the load impedance will be decreased to 50 Ω. In the TLLM architecture, the main amplifier will have 50 Ω load impedance at power back-off. In the last 6 dB power range, the load impedance will increase to 100 Ω. The difference between these two load variations is because of the impedance inverter used in the Doherty architecture. Despite the completely different load modulation, the TLLM architecture will have similar performance compared to the Doherty architecture. Actually, the load impedance seen by the transistor is important in obtaining high efficiency at power back-off as well as high output power at peak power. In the TLLM architecture, the proper load modulation at the drain level is guaranteed by the output matching network.

In both cases, the peaking amplifier has infinite load impedance at power back-off since it does not draw current at back-off level. When the peaking amplifier starts to deliver current to the load, its load impedance begin to decrease. In TLLM architecture, the peaking amplifier's load impedance at peak power will be 100 Ω while in Doherty amplifier it is 50

Ω due to the difference in the load seen at the junction (point J in Fig. 2.3 and Fig. 3.1). The load changes for both architectures are shown in Fig. 3.2.

For TLLM architecture, when peaking amplifier has reactive output impedance (not quasi-open output impedance), there will be some current going into the output terminal of the peaking amplifier. As a result, the load impedance seen by the peaking amplifier will not be infinite. In this case, the peaking amplifier's load impedance starts from a finite reactive impedance at power back-off and it will reach to the impedance of $Z_{L,pk} = Z_L(I_m + I_p)/I_p$ at peak output power. I_m and I_p are the output currents from the main and peaking amplifier at peak power respectively.

The appropriate impedance transformations at the transistor drain levels are realized using impedance matching networks. At the input of one or both amplifiers, a delay and phase compensation network is needed to ensure the in-phase combination of the main and peaking amplifier output currents at peak power. According to the output powers and bias conditions, different transistors can be used for the two branches. This means that the input and output matching networks can be different. Even with the same transistors, the matching networks may be different, since the two branches are working in different bias conditions and may have different input and optimum load impedances.

At first glance, references [34] and [35] seem to propose topologies for the Doherty PA similar to the one illustrated in Fig. 3.1. In [34], the impedance transformer is implemented using lumped elements and embedded in the output matching network of the main amplifier. In [35], the real frequency technique is used; however, it still uses the impedance inverter as a part of the output combining network. In addition, the methodology proposed here to design the TLLM amplifier illustrated in Fig. 3.1 is original and different from the ones proposed in [34] and [35].

In our approach, the design of the output matching networks are done so that the requirements at power back-off and at peak power are fulfilled. We provide a systematic approach

to obtain the output matching network parameters. For the main amplifier, our approach ensures the best possible performances at both back-off and peak power. Also a very important part of the design is the prevention of power leakage into the peaking amplifier at power back-off. While the other references use optimization to fulfill this requirement, we provide a systematic approach for the design of the wideband peaking amplifier to prevent power leakage in the back-off region and to ensure the best performance at the peak power.

In Doherty amplifier, the bandwidth is limited by the intrinsic frequency bandwidth of the individual PAs and by the frequency response of the quarter wave impedance transformer. In our approach, we do not have the impedance transformer, so the bandwidth of the whole structure is only limited by the bandwidth of the main and peaking PAs.

The most important parts of this architecture are the two output matching networks. Their characteristics are defined based on the design goals. In our approach, these matching networks are designed based on two goals. The main goal is high efficiency at power back-off, and the second goal is the highest possible maximum output power at peak input power. The efficiency at peak output power is considered herein to be less important, because with high PAPR signals, the probability density function (PDF) of the signal is usually concentrated in the back-off region and the efficiency at peak power has little effect on the average amplifier's efficiency. To meet our design goals, the following requirements should be met:

Design requirement 1: To obtain the high efficiency at power back-off, the main transistor should see its optimum load impedance for efficiency at power back-off. To reach the second goal, it should have the load impedance as close as possible to its optimum load impedance for peak output power.

Design requirement 2: For high efficiency at back-off, the peaking amplifier should have no RF power leakage in power back-off. If the peaking amplifier has a small-signal output admittance of $Y_{out,p,ss} = 1/Z_{out,p,ss}$ at back-off (Fig. 3.1), the ratio of the power delivered to

the load (P_L) over the main amplifier's output power (P_m) can be calculated as:

$$\frac{P_L}{P_m} = \frac{1/R_L}{1/R_L + \mathrm{Re}(Y_{out,p,ss})} \tag{3.1}$$

where $\mathrm{Re}(Y_{out,p,ss})$ is the real part of the $Y_{out,p,ss}$.

In this case, a part of the power generated by the main amplifier is delivered to the load. The rest of the output power generated by the main amplifier is dissipated in resistive part of the peaking amplifier's output impedance. Equation (3.1) shows that $\mathrm{Re}(Y_{out,p,ss})$ should be as low as possible to reduce the power leakage toward the peaking amplifier in the back-off power range. The peaking amplifier may include a reactive susceptance component at its output. In such a case, this susceptance should be considered in the design of the main amplifier's output matching network, since it changes the main amplifier's load impedance at back-off.

<u>Design requirement 3</u>: The peaking transistor should see a load impedance close to its optimum load impedance at peak power to meet the second goal.

<u>Design requirement 4</u>: The peaking amplifier should have low, or in the best case, zero DC power consumption in the power back-off region, when it is turned off. Therefore, it should be biased at a proper gate bias for class C to turn on at the correct input power level.

<u>Design requirement 5</u>: At peak power, the output currents from the two amplifiers should be in-phase to have the best combining efficiency. This condition can be assured by the insertion of delay and phase alignment circuits at the inputs of the amplifiers.

The last two criteria should be met by proper biasing and a delay/phase compensation circuit. The first three criteria should be satisfied by proper design of the output matching networks. As can be seen from these conditions, there are two limitations for each matching network. For the main amplifier's output matching network, two load impedances at back-off and peak powers should be transformed to two optimum impedances for the main transistor. For the peaking amplifier's design, the output impedance of the amplifier at back-off and

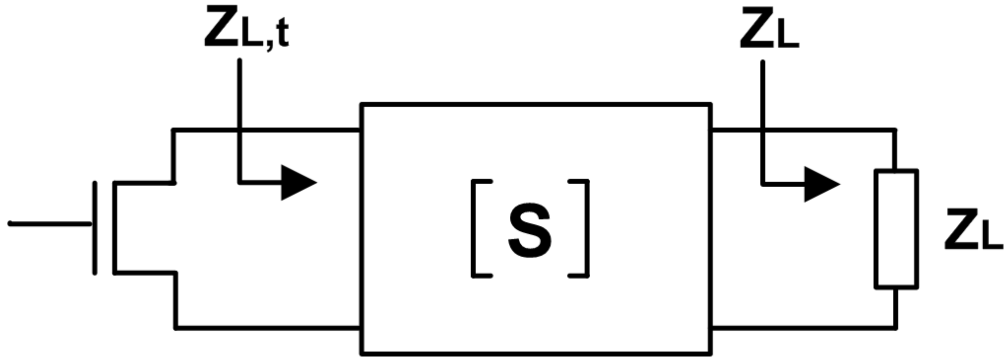


Figure 3.3: A two-port matching network for main amplifier

the transistor's load impedance at peak power are of prime importance.

At the input, the TLLM amplifier uses the same components as the Doherty amplifier. A power divider splits the input power between the two amplifier branches. Two input matching networks match the power divider port impedances to the optimum source impedances for the transistors and an offset line adjusts the delay and phase of the input signals between the two amplifier branches for proper power combining at the output.

3.2 Main Amplifier: Two-Point Matching

Fig. 3.3 shows an output matching network. In the design of impedance matching networks, an impedance Z_L is transformed to another impedance $Z_{L,t}$ by the matching network. In power amplifier design, the output matching network transforms the load impedance Z_L to the optimum impedance that is dictated by the transistor, $Z_{L,t} = Z_{opt}$. If the value of load impedance changes to Z'_L, then the load impedance seen by the transistor will be different than Z_{opt}. In conventional matching network design, the load impedance Z_L is fixed and consequently the matching network is only designed to transform the fixed load impedance to the desired impedance at the transistor's output terminal.

The design criteria for the main amplifier's output matching network are given in Section 3.1. In TLLM amplifier, there are two conditions to be met, one in power back-off and one in peak output power. The load impedance at peak power is different than the load

impedance at power back-off due to the load-modulation effect. On the other hand, the optimum impedance at power back-off is different than the optimum impedance at peak output power due to the nonlinear behaviour of the transistor and the criteria for optimum impedance (at peak power, the optimum impedance is defined for maximum output power and at power back-off maximum efficiency is desired). This section presents the theory for designing the matching network that provides optimum performance at both peak and power back-off levels. There are two load impedances that should be transformed to two optimum impedances at peak power and at power back-off. For this reason, the design procedure is designated as the *two-point matching* technique.

Consider the output matching network of the main amplifier shown in Fig. 3.3 as a lossless reciprocal two-port network. The S-parameter matrix of a lossless and reciprocal two-port network can be written as:

$$\begin{bmatrix} S_{11} & \sqrt{1-|S_{11}|^2}e^{j\theta_{21}} \\ \sqrt{1-|S_{11}|^2}e^{j\theta_{21}} & -S_{11}^{*}e^{j2\theta_{21}} \end{bmatrix} \tag{3.2}$$

In this equation, θ_{21} is the phase of S_{21}. We consider the main amplifier's load impedances at back-off and peak powers to be $Z_{L,m,BO}$ and $Z_{L,m,P}$, respectively. Assume that the main transistor's optimum load at back-off is $Z_{L,tm,BO}$, and the optimum load at peak power is $Z_{L,tm,P}$. The main goal is high efficiency at back-off; therefore, the matching network has to convert $Z_{L,m,BO}$ to the desired $Z_{L,tm,BO}$. We select $Z_{L,m,BO}$ as the reference impedance for the matching network's S-parameters [60–64]. By selecting a complex-valued impedance as the reference impedance for a port, the values of reflection coefficients at the port should be calculated considering the direction we are looking at (Appendix A).

At power back-off, the output port is terminated to its reference impedance $Z_{L,m,BO}$; hence, we write:

$$\Gamma_{L,tm,BO} = S_{11} \tag{3.3}$$

At peak power, the transistor's load reflection coefficient can be expressed as:

$$\Gamma_{L,tm,P} = S_{11} + \frac{S_{12}S_{21}\Gamma_{L,m,P}}{1 - S_{22}\Gamma_{L,m,P}} \tag{3.4}$$

The value of $\Gamma_{L,tm,BO}$ can be obtained from the transistor model or load-pull measurement. $\Gamma_{L,tm,BO}$ should guarantee optimum efficiency at output power back-off. Knowing $\Gamma_{L,tm,BO}$, means that the value of S_{11} for the matching network is known (from (3.3)). From (3.2) and (3.3), we can re-write (3.4) as:

$$\Gamma_{L,tm,P} = \Gamma_{L,tm,BO} + \frac{\Gamma_{L,m,P}(1 - |\Gamma_{L,tm,BO}|^2)e^{j2\theta_{21}}}{1 + \Gamma_{L,m,P}\Gamma^*_{L,tm,BO}e^{j2\theta_{21}}} \tag{3.5}$$

Equation (3.5) can be expressed as:

$$(\Gamma_{L,tm,P} - \Gamma_{L,tm,BO})(1 + \Gamma_{L,m,P}\Gamma^*_{L,tm,BO}e^{j2\theta_{21}}) = \Gamma_{L,m,P}(1 - |\Gamma_{L,tm,BO}|^2)e^{j2\theta_{21}}$$

$$e^{j2\theta_{21}}\left(\Gamma_{L,tm,P}\Gamma^*_{L,tm,BO}\Gamma_{L,m,P} - \Gamma_{L,m,P}|\Gamma_{L,tm,BO}|^2 + \Gamma_{L,m,P}|\Gamma_{L,tm,BO}|^2 - \Gamma_{L,m,P}\right) = \Gamma_{L,tm,BO} - \Gamma_{L,tm,P}$$

$$\frac{\Gamma_{L,tm,P} - \Gamma_{L,tm,BO}}{\Gamma_{L,tm,P} - 1/\Gamma^*_{L,tm,BO}} = -\Gamma_{L,m,P}\Gamma^*_{L,tm,BO}e^{j2\theta_{21}} \tag{3.6}$$

Equation (3.6) can be written as:

$$\left|\frac{\Gamma_{L,tm,P} - \Gamma_{L,tm,BO}}{\Gamma_{L,tm,P} - 1/\Gamma^*_{L,tm,BO}}\right| = \left|\Gamma_{L,m,P}\Gamma^*_{L,tm,BO}\right| \tag{3.7}$$

Equation (3.7) shows that the locus of the possible $\Gamma_{L,tm,P}$ values are located on a circle with centre and radius respectively of (Appendix B):

$$C_{L,tm,P} = \frac{(1/\Gamma^*_{L,tm,BO} - \Gamma_{L,tm,BO})|\Gamma_{L,m,P}\Gamma_{L,tm,BO}|^2}{|\Gamma_{L,m,P}\Gamma_{L,tm,BO}|^2 - 1} + \Gamma_{L,tm,BO} \tag{3.8}$$

$$r_{L,tm,P} = \frac{(1 - |\Gamma_{L,tm,BO}|^2)|\Gamma_{L,m,P}|}{1 - |\Gamma_{L,m,P}\Gamma_{L,tm,BO}|^2} \tag{3.9}$$

Equations (3.7) shows that when the matching network of Fig. 3.3 converts $Z_{L,1}$ to $Z_{L,t,1}$, then any other load impedance $Z_{L,2}$ will be transformed on a circle. The location of the $Z_{L,t,2}$ on the circle is determined by the value of θ_{21} which is the transmission phase of the matching network.

In designing the TLLM amplifier, the load impedance at power back-off is transformed to the optimum load impedance for maximum efficiency, $Z_{opt,tm,BO}$. The load impedance at peak output power will be transformed on a circle defined by (3.8) and (3.9). To find the optimum value of θ_{21}, this circle can be plotted along with the power contours obtained from load-pull simulation or measurement. The intersection of the circle with the highest output power contour is the best possible choice and should be selected as $Z_{L,tm,P}$. Having $Z_{L,tm,P}$ and using (3.6), the value of θ_{21} can be determined directly. If the contours are not available, the phase of S_{21} can be set such that the load impedance becomes as close as possible to the optimum load at the peak power. It should be noted that the analysis was done with $Z_{L,m,BO}$ selected as the reference impedance. The contours should be plotted in a reflection coefficient plane with this reference impedance or the locus should be transformed to the standard impedance of 50 Ω (Appendix A).

The two-point matching technique is shown graphically in Fig. 3.4 with a reference impedance of 50 Ω. As shown in this figure, $Z_{L,m,BO}$ should be converted to the optimum impedance for efficiency at back-off power. The locus of the possible transistor's load impedances at peak input power can then be plotted along with the contours of output power at peak input power. The transistor's load impedance at peak input power is selected to give the highest possible output power.

Having S_{11} and θ_{21}, the S-parameter matrix of the matching network (given in (3.2)) is fully determined. The matching network should then be synthesized using circuit elements in a later circuit synthesis phase.

The equations for the two-point matching design can be simplified for the case of wide-

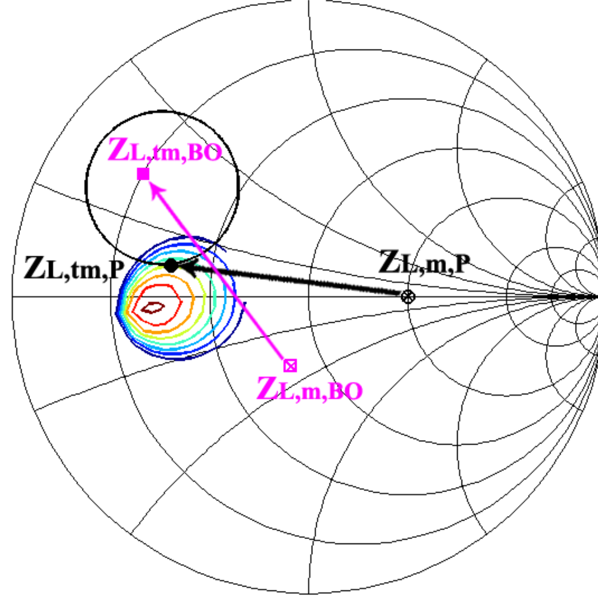


Figure 3.4: Graphical illustration of the two-point matching network performance.

band TLLM amplifier. We can choose $Z_{L,m,BO}$ as the reference impedance of the output port (port 2) and $Z^*_{L,tm,BO}$ as the reference impedance for the input port (port 1) of the matching network. Since the matching network converts $Z_{L,m,BO}$ to $Z_{L,tm,BO}$, we can say $S_{11} = 0$, and the S-parameter matrix of (3.2) can be written in the form of:

$$\begin{bmatrix} 0 & e^{j\theta_{21}} \\ e^{j\theta_{21}} & 0 \end{bmatrix} \tag{3.10}$$

In this case $\Gamma_{L,tm,BO} = 0$, and (3.5) can be written as:

$$\Gamma_{L,tm,P} = \Gamma_{L,m,P} e^{j2\theta_{21}} \tag{3.11}$$

It should be noted that the reference impedances used for the calculation of $\Gamma_{L,tm,P}$ and $\Gamma_{L,m,P}$ are different. Equation (3.10) shows that with these reference impedances, the matching network has no loss and only a phase shift, which can be obtained using (3.11) and the output power contours or optimum load impedance of the transistor at peak power.

In fact, it can be seen that the Doherty amplifier is a special case of the TLLM amplifier. The impedance inverter and the offset line in the main branch can be considered as a part

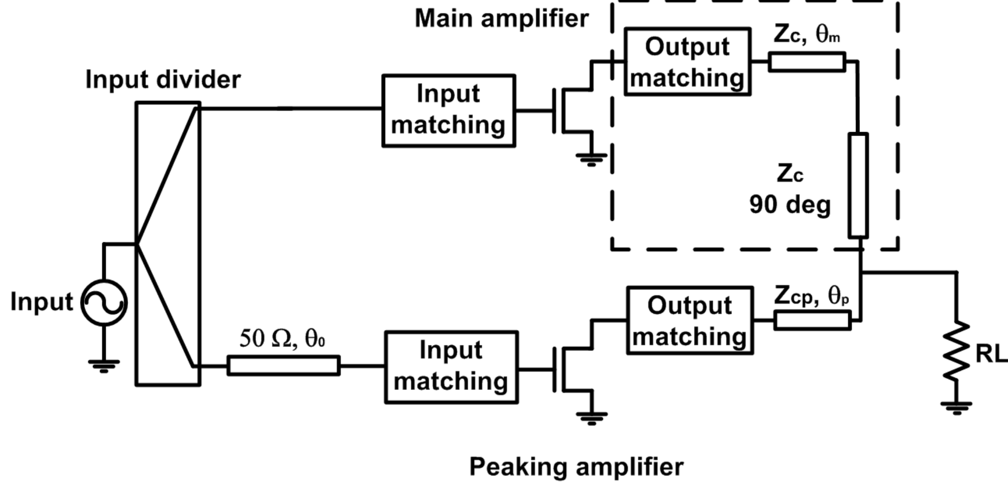


Figure 3.5: The Doherty amplifier as a special case of the TLLM amplifier

of the matching network shown in Fig. 3.5. The offset line actually adjusts the value of θ_{21} (equation (3.10)) in the Doherty amplifier to get the desired performance.

3.3 Peaking Amplifier: Two-Sided and Reversed Two sided Matching

The design criteria for the peaking amplifier is given in Section 3.1. There are two criterion to be met, one at peak power and one at the power back-off. At peak power, the peaking amplifier has to provide enough output power to provide proper load modulation for the main amplifier. At power back-off, the peaking amplifier should not dissipate the RF power generated by the main amplifier to prevent performance degradation at power back-off (low power leakage into the peaking branch).

The output matching network for peaking amplifier in TLLM amplifier is shown in Fig. 3.6 and considered to be a lossless and reciprocal network. The output matching network transforms the load impedance $Z_{L,p,P}$ to the optimum impedance that is dictated by the transistor, $Z_{L,tp,P} = Z_{opt}$. For the peaking amplifier in the TLLM structure, the design criterion at power back-off introduces another limitation to the matching network. Referring to Fig. 3.6, to have low power leakage at power back-off, the output impedance seen from the peaking amplifier branch, $Z_{out,p,ss}$ should cause low power dissipation. In the design of

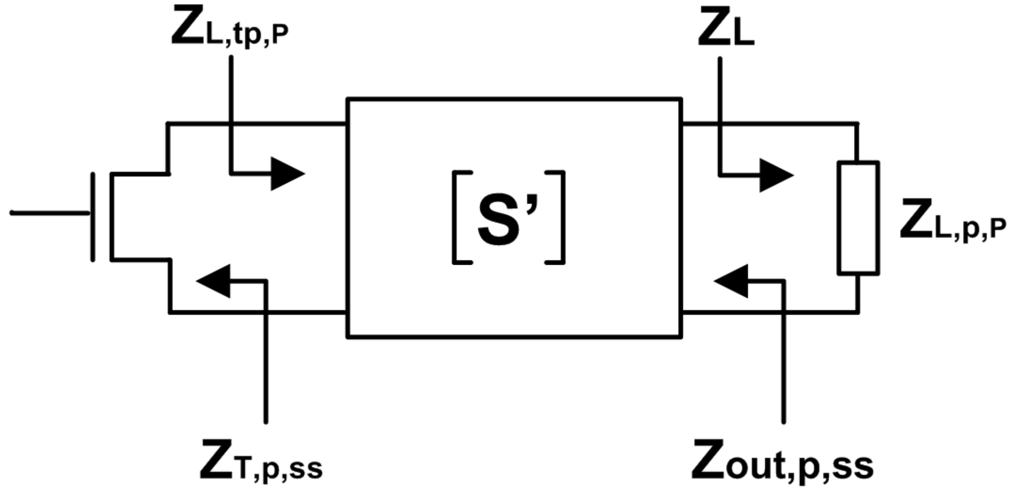


Figure 3.6: A two-port matching network for peaking amplifier

the peaking amplifier matching network, the impedance seen from both ports are important due to the requirements defined by the TLLM amplifier's design goals. For this reason, the design procedures provided in this section is designated as the *two-sided matching* and *reversed two-sided matching* techniques. The selection of two-sided or reversed two-sided matching depends on the small-signal output impedance of the peaking transistor according to the following two cases:

Case 1: If the transistor's small-signal output impedance $Z_{T,p,ss}$ corresponds to a low magnitude reflection coefficient, the matching network is designed to convert it to a nearly reactive output impedance. Its parameters are then selected so that the peaking amplifier has the highest possible peak output power. In this case, the matching technique is termed *two-sided matching.*

Case 2: If the transistor's small-signal output impedance $Z_{T,p,ss}$ corresponds to a high magnitude reflection coefficient (nearly reactive impedance), the matching network usually converts it to a high magnitude output reflection coefficient that can fulfill the output impedance requirement at power back-off for the peaking amplifier. In this case, the matching network is primarily designed to convert $Z_{L,p,P}$ to the transistor's optimum load at peak power $Z_{opt,tp,P}$. The parameters of this matching network are then selected so that the

peaking amplifier does not have RF power leakage before it is turned on. This matching procedure is termed *reversed two-sided matching*.

In the following, both design techniques will be addressed in detail. In the analysis provided in the following sections, the primed notation is used for the S-parameters of the peaking amplifier's output matching network (i.e. S'_{11}, S'_{12}, S'_{21} and S'_{22}) to differentiate them from the main amplifier's output matching network given in the previous section.

3.3.1 Two-Sided Matching

If the peaking transistor has a low magnitude output reflection coefficient, the primary criterion in the design is the output impedance at power back-off, in order to minimize the power leakage. This condition usually happens at very high frequencies, such as millimetre-wave frequencies, in which conductive losses are dominant in the transistor terminal interconnections. In this case, by selecting $Z_{L,p,P}$ to be the reference impedance, we have:

$$\Gamma_{L,tp,P} = S'_{11} \tag{3.12}$$

$$\Gamma_{out,p,ss} = S'_{22} + \frac{S'_{12}S'_{21}\Gamma_{T,p,ss}}{1 - S'_{11}\Gamma_{T,p,ss}} \tag{3.13}$$

Since the peaking amplifier's output matching network is lossless and reciprocal, its S-parameter matrix can be written (similar to (3.2)) as :

$$\begin{bmatrix} -S'^{*}_{22}e^{j2\theta'_{21}} & \sqrt{1-|S'_{22}|^2}e^{j\theta'_{21}} \\ \sqrt{1-|S'_{22}|^2}e^{j\theta'_{21}} & S'_{22} \end{bmatrix} \tag{3.14}$$

Herein, θ'_{21} is the phase of S'_{21}. Using (3.14) and (3.12), (3.13) can be written as:

$$\Gamma_{L,tp,P}\Gamma_{out,p,ss}e^{-j2\theta'_{21}} - \frac{\Gamma^{*}_{L,tp,P} + \Gamma_{out,p,ss}e^{-j2\theta'_{21}}}{\Gamma_{T,p,ss}} + 1 = 0 \tag{3.15}$$

Here, we define $\theta_{T,p,ss}$ as the phase of $\Gamma_{T,p,ss}$ and $\theta_{out,p,ss}$ as the phase of $\Gamma_{out,p,ss}$. Then by

multiplying both sides of (3.15) by $\sqrt{|\frac{\Gamma_{T,p,ss}}{\Gamma_{out,p,ss}}|}e^{j(\theta'_{21}+\frac{\theta_{T,p,ss}-\theta_{out,p,ss}}{2})}$, one can write:

$$\begin{aligned}\Gamma_{L,tp,P}\sqrt{|\Gamma_{T,p,ss}\Gamma_{out,p,ss}|}e^{j\left(-\theta'_{21}+\frac{\theta_{T,p,ss}+\theta_{out,p,ss}}{2}\right)} - \frac{\Gamma^*_{L,tp,P}e^{j\left(\theta'_{21}-\frac{\theta_{T,p,ss}+\theta_{out,p,ss}}{2}\right)}}{\sqrt{|\Gamma_{T,p,ss}\Gamma_{out,p,ss}|}} \\ -\sqrt{\left|\frac{\Gamma_{out,p,ss}}{\Gamma_{T,p,ss}}\right|}e^{j\left(-\theta'_{21}+\frac{\theta_{out,p,ss}-\theta_{T,p,ss}}{2}\right)} + \sqrt{\left|\frac{\Gamma_{T,p,ss}}{\Gamma_{out,p,ss}}\right|}e^{j\left(-\theta'_{21}+\frac{\theta_{T,p,ss}-\theta_{out,p,ss}}{2}\right)} = 0\end{aligned} \tag{3.16}$$

By letting $X = \sqrt{|\Gamma_{T,p,ss}\Gamma_{out,p,ss}|}e^{j(-\theta'_{21}+\frac{\theta_{T,p,ss}+\theta_{out,p,ss}}{2})}$, (3.16) becomes:

$$\Gamma_{L,tp,P}X - \frac{\Gamma^*_{L,tp,P}}{X} - \frac{X}{\Gamma_{T,p,ss}} + \frac{\Gamma_{T,p,ss}}{X} = 0 \tag{3.17}$$

$$X\left(\Gamma_{L,tp,P} - \frac{1}{\Gamma_{T,p,ss}}\right) = \frac{1}{X}(\Gamma^*_{L,tp,P} - \Gamma_{T,p,ss}) \tag{3.18}$$

$$X^2 = \frac{\Gamma^*_{L,tp,P} - \Gamma_{T,p,ss}}{\Gamma_{L,tp,P} - 1/\Gamma_{T,p,ss}} \tag{3.19}$$

From definition of X, we can write:

$$\frac{\Gamma^*_{L,tp,P} - \Gamma_{T,p,ss}}{\Gamma_{L,tp,P} - 1/\Gamma_{T,p,ss}} = |\Gamma_{T,p,ss}\Gamma_{out,p,ss}|e^{j(-2\theta'_{21}+\theta_{T,p,ss}+\theta_{out,p,ss})} = \Gamma_{T,p,ss}\Gamma_{out,p,ss}e^{-j2\theta'_{21}} \tag{3.20}$$

which can be written as:

$$\left|\frac{\Gamma^*_{L,tp,P} - \Gamma_{T,p,ss}}{\Gamma_{L,tp,P} - 1/\Gamma_{T,p,ss}}\right| = |\Gamma_{T,p,ss}\Gamma_{out,p,ss}| \tag{3.21}$$

Equation (3.21) shows that the locus for the possible $\Gamma_{L,tp,P}$ values are located on a circle with centre and radius respectively of (Appendix B):

$$C_{L,tp,P} = \frac{\left(1/\Gamma_{T,p,ss} - \Gamma^*_{T,p,ss}\right)|\Gamma_{T,p,ss}\Gamma_{out,p,ss}|^2}{|\Gamma_{T,p,ss}\Gamma_{out,p,ss}|^2 - 1} + \Gamma^*_{T,p,ss} \tag{3.22}$$

$$r_{L,tp,P} = \frac{(1 - |\Gamma_{T,p,ss}|^2)\,|\Gamma_{out,p,ss}|}{1 - |\Gamma_{T,p,ss}\Gamma_{out,p,ss}|^2} \tag{3.23}$$

This circle is the locus of the possible values for $Z_{L,tp,P}$. To find the parameters for the matching network, a value should first be selected for $Y_{out,p,ss}$ (or $\Gamma_{out,p,ss}$). For example, by

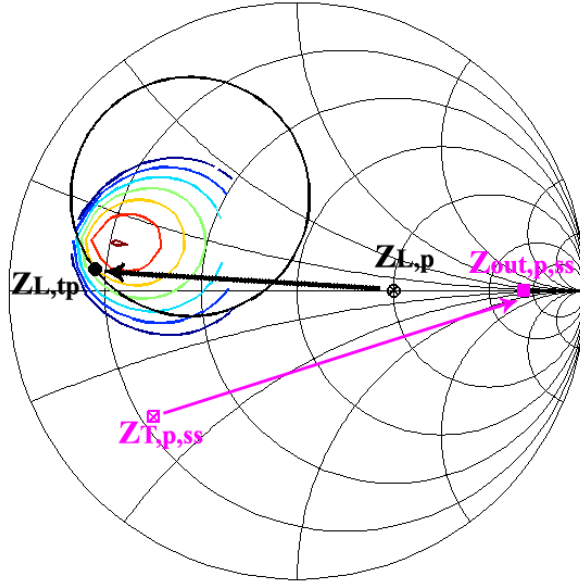


Figure 3.7: Graphical illustration of the two-sided matching network performance.

selecting $\mathrm{Re}(Y_{out,p,ss}) = \mathrm{Re}(Y_{L,BO})/10$, according to (3.1), the total power loss percentage due to power leakage into the peaking amplifier is nearly 9%. By plotting the circular locus for the possible $\Gamma_{L,tp,P}$ values along with the output power contours of the peaking transistor and using (3.20), the value of θ'_{21} can then be found. By finding this parameter, the S-parameter matrix of the peaking amplifier's output matching network is fully determined.

Fig. 3.7 illustrates the two-sided matching technique graphically with the reference impedance of 50 Ω. As can be seen from this figure, the output impedance of the peaking transistor should be converted to the desired output impedance. The locus of the possible $Z_{L,tp,P}$ values can then be plotted along with the output power contours. $Z_{L,tp,P}$ is selected to give the highest possible output power. Having $Z_{L,tp,P}$, one can find using θ'_{21} (3.20).

3.3.2 Reversed Two-Sided Matching

When $Z_{T,p,ss}$ is nearly reactive, a different design procedure can be adopted. Usually class-C biased transistors in low RF frequencies meet such a condition. In this case, the magnitude of the output reflection coefficient de-embedded to the output access port of the matching

network remains high; therefore, there is very low power leakage into the peaking amplifier at power back-off. In these cases, it is better to design the matching network to have the optimum impedance at peak power and then select the parameters to have the desired output impedance at power back-off.

The analysis in this case is similar to the two-sided matching case. By selecting the reference impedance to be $Z_{T,p,ss}$, we have:

$$\Gamma_{out,p,ss} = S'_{22} \tag{3.24}$$

$$\Gamma_{opt,tp,P} = S'_{11} + \frac{S'_{12}S'_{21}\Gamma_{L,p}}{1 - S'_{22}\Gamma_{L,p}} \tag{3.25}$$

Using the same procedure as the two-sided matching case, we have:

$$\frac{\Gamma^*_{out,p,ss} - \Gamma_{L,p,P}}{\Gamma_{out,p,ss} - 1/\Gamma_{L,p,P}} = \Gamma_{L,p,P}\Gamma_{opt,tp,P}e^{-j2\theta'_{21}} \tag{3.26}$$

which is a circle with a center and radius, respectively, of:

$$C_{out,p,ss} = \frac{(1/\Gamma_{L,p,P} - \Gamma^*_{L,p,P})|\Gamma_{L,p,P}\Gamma_{opt,tp,P}|^2}{|\Gamma_{L,p,P}\Gamma_{opt,tp,P}|^2 - 1} + \Gamma^*_{L,p,P} \tag{3.27}$$

$$r_{opt,p,ss} = \frac{(1 - |\Gamma_{L,p,P}|^2)|\Gamma_{opt,tp,P}|}{1 - |\Gamma_{L,p,P}\Gamma_{opt,tp,P}|^2} \tag{3.28}$$

The small-signal output impedance of the peaking amplifier lies on this circle. In this case,we have optimum load impedance for the transistor at peak power; and by selecting a proper value for θ'_{21}, the output impedance power back-off can be set to a desired value.

Fig. 3.8 illustrates the reversed two-sided matching graphically with reference impedance of 50 Ω. In this figure, $Z_{L,p,P}$ is converted to $Z_{opt,tp,P}$ to get the maximum output power. By selecting the proper output impedance, θ'_{21} can be found using (3.26).

3.4 Synthesis of the Matching Networks

In the previous sections, the S-parameters of the matching networks are obtained using the design criteria. As we have seen, all the cases lead to the same condition in which the

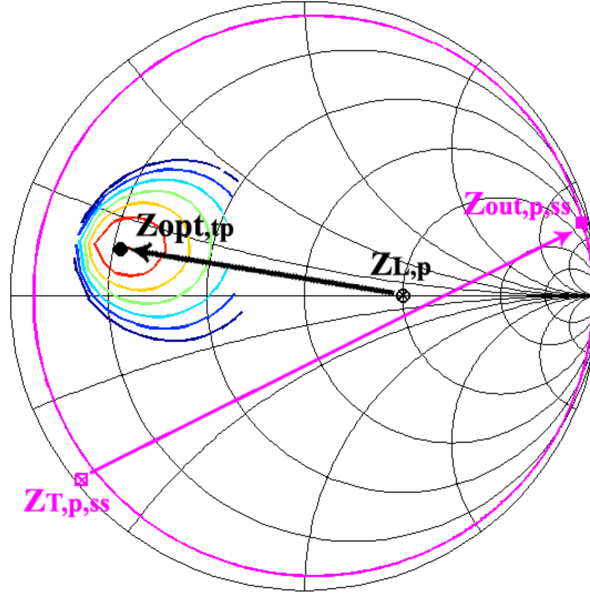


Figure 3.8: Graphical illustration of the reversed two-sided matching network performance.

S-parameter matrix is fully determined. The next step is the synthesis of the matching networks using circuit elements in the given technology. In the following, a single-frequency synthesis method based on Π and T networks is presented; and then, the wideband design procedure is described.

3.4.1 Narrowband Matching Network Synthesis

The problem is the synthesis of a two-port network with predetermined S-parameters. One of the simplest ways of designing the matching network is the utilization of T or Π networks, as shown in Fig. 3.9. Having the S-parameters of a two-port network, its ABCD parameters can be obtained at the design frequency, and with the ABCD parameters, the network elements for the networks of Fig. 3.9 can be obtained as described in [65].

With the element values, the S-parameters necessary for proper load modulation at drain are ensured, and there is no need for the impedance transformer, as used in conventional Doherty architecture.

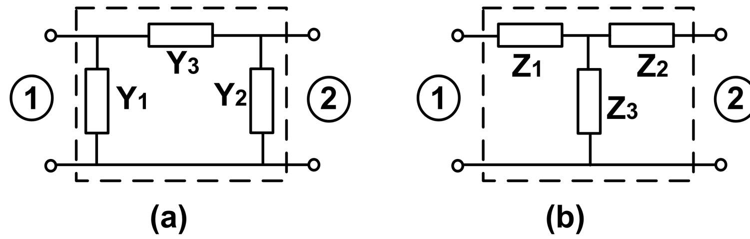


Figure 3.9: Three-element networks for narrowband matching network synthesis, a) Π network, b) T network.

3.4.2 Wideband Matching Network Synthesis

In wideband matching network design, the only important response is usually the amplitude response. The phase response is important only in terms of group delay flatness. However, in our design case, the S-parameters are fully determined, so the matching network has to be synthesized so that both the amplitude and phase responses are simultaneously satisfied. In general, it is not possible to synthesize both amplitude and arbitrary phase responses; nonetheless, the design should be done to follow the amplitude and phase requirements as closely as possible.

For the output matching networks, after characterizing the transistors in the desired bandwidth, the S-parameters of the matching networks can be obtained using the two-sided (or reversed two-sided) and two-point matching techniques. Then, by selecting a proper response type, such as Butterworth or Chebychev, the matching networks can be designed. When selecting the response type, one should note that both amplitude and phase responses in the frequency range of interest should be satisfied as much as possible; therefore, there may be a need to select a wider bandwidth response than the PA design bandwidth, in order to have a phase response close to the analytically required one. After selection of the response type, the synthesis of the matching network can be done using broadband matching network design techniques [60, 64].

The design of the main amplifier's output matching network can be simplified by controlling the output impedance of the peaking amplifier. Referring to Fig. 3.1, the load

impedance seen by the main amplifier before turning on the peaking amplifier ($Z_{L,m,BO}$) is equal to $Z_L||Z_{out,p,ss}$. Usually, the optimum impedances of the transistors for maximum output power are confined to a small region of the Smith chart at different frequencies. The optimum impedances of the transistors for maximum efficiency are also confined to a small region of the Smith chart at different frequencies. One can approximate these impedances with a constant impedance value. Using (3.11), we have:

$$\begin{aligned} e^{j2\theta_{21}} &= \Gamma_{L,tm,P}/\Gamma_{L,m,P} = e^{j(\theta_{L,tm,P}-\theta_{L,m,P})} \\ &= \frac{Z_{L,tm,P} - Z_{L,tm,BO}}{Z_{L,tm,P} + Z^*_{L,tm,BO}} \times \frac{Z_{L,m,P} + Z^*_{L,m,BO}}{Z_{L,m,P} - Z_{L,m,BO}} \end{aligned} \tag{3.29}$$

The value of $Z_{L,m,P}$ is fixed versus frequency since the load impedance and the load modulation is the same for all frequencies. Assuming that the optimum impedances for the peak power and peak efficiency do not change significantly with frequency, the values of $Z_{L,tm,BO}$ and $Z_{L,tm,P}$ are almost constant over the frequency range. If the output impedance of the peaking amplifier is nearly open ($\Gamma_{out,p,ss} \approx 1$) over the frequency bandwidth, then $Z_{L,m,BO} \approx Z_L$ will be a constant quantity over frequency. Consequently, the right-hand side of (3.29) is a constant value over the frequency band, because all the impedances are nearly constant. This means that the transmission phase to be realized for the main amplifier's matching network ($\theta_{21}(\omega)$) should be nearly constant in the desired bandwidth, i.e. the matching network should have nearly zero group delay. Such a matching network may not be feasible.

To have more realizable conditions, the output admittance of the peaking amplifier can be set to be a frequency dependent susceptance of $B_{out,p,ss}(\omega)$. Using (3.29), the graph of $\theta_{21} - \theta_{L,tm,P}/2$ versus normalized $B_{out,p,ss}$ is plotted in Fig. 3.10 for the normalized case of $Y_L = 1$ and $Y_{L,m,P} = 1/2$ (equal output powers from two amplifiers). From (3.29), it can be seen that $\theta_{L,tm,P}$ is almost constant; therefore, the slope of the θ_{21} is negative versus $B_{out,p,ss}$ in the $-1/2 < B_{out,p,ss} < 1/2$ range. Hence, if we have an increasing $B_{out,p,ss}$ versus frequency in the range of $-1/2$ to $1/2$, we have a negative θ_{21} slope versus frequency (positive group

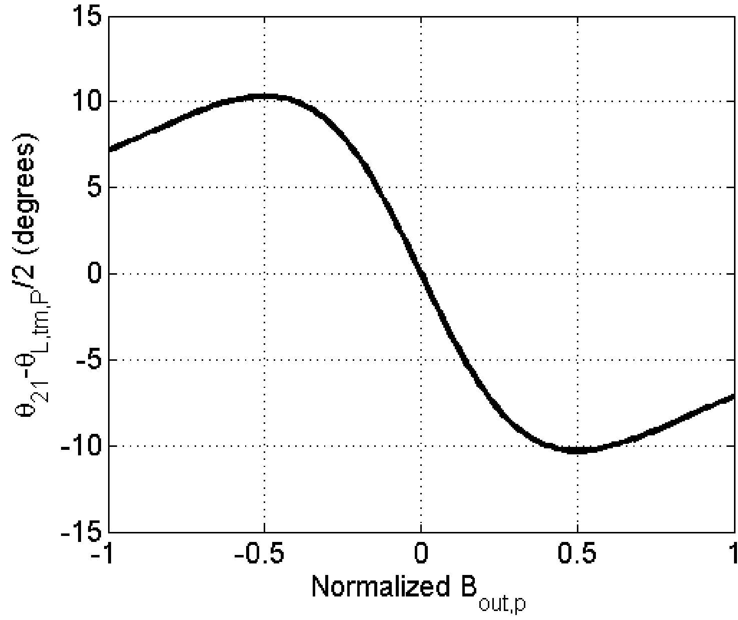


Figure 3.10: $\theta_{21} - \theta_{L,tm,P}/2$ versus normalized $B_{out,p}$.

delay), resulting in a more realizable matching network for the main amplifier.

The input matching networks can be designed using the conventional wideband matching network design method [60, 64]. By having the appropriate source impedances, the input matching networks can be designed to convert the standard 50 Ω impedance to the desired source impedance for the transistors.

3.5 TLLM Amplifier Systematic Design Procedure

In the proposed architecture, the design of the main and peaking amplifiers are not independent from each other. Therefore, the design should be done considering the effects of the amplifiers on each other. The design procedure is proposed as the following:

Step 1: At the design frequency, the ratios of the output powers from two amplifiers should be specified at peak power. Having the ratios of the output powers, the load impedances of each amplifier at peak power can be determined as follows:

$$Z_{L,m,P} = \left(1 + \frac{I_p}{I_m}\right) R_L \tag{3.30}$$

$$Z_{L,p,P} = \left(1 + \frac{I_m}{I_p}\right) R_L \tag{3.31}$$

where I_m and I_p are the main amplifier and the peaking amplifier's peak output currents, respectively. These currents can be obtained from the peak power values.

Step 2: The value of $Z_{T,p,ss}$ should be obtained at small signal condition, and $Z_{opt,tp,P}$ (or load-pull contours) should be determined using the peaking transistor's model or from load-pull measurements. Using the main transistor's model or load-pull measurements, $Z_{L,tm,BO}$ and $Z_{L,tm,P}$ (or load pull contours at peak power) should be determined.

Step 3 : The selection of the peaking amplifier's output matching design procedure is based on the output return loss of the peaking transistor. If the output of the peaking transistor has a high reflection coefficient, the design can be done using the reversed two-sided matching technique, and if the peaking transistor's output return loss is not very high, the two-sided matching technique should be used.

Step 4 : If two-sided matching is being used, $Z_{out,p,ss}$ should be selected to have low power leakage in power back-off. Having $Z_{L,p,P}$, $Z_{T,p,ss}$, $Z_{opt,tp,P}$ and $Z_{out,p,ss}$, the S-parameters of the peaking amplifier's output matching network can be found using the two-sided matching technique. Using (3.20), one can find θ'_{21}, so that the peaking transistor's load impedance ($Z_{L,tp,P}$) gives the highest possible output power at peak power. If reversed two-sided matching is being used, the S-parameters of the peaking amplifier's output matching network can be found by $Z_{L,p,P}$, $Z_{T,p,ss}$ and $Z_{opt,tp,P}$ and using (3.26) to select θ'_{21} to have the proper $Z_{out,p,ss}$ (as discussed in Section 3.4).

Step 5 : Having $Z_{out,p,ss}$, the load impedance of the main amplifier at back-off ($Z_{L,m,BO}$) can be determined. Using the two-point matching technique, the S-parameters of the main amplifier's matching network can be found.

Step 6 : For wideband design, steps 1 to 5 can be repeated at different frequency points in the desired bandwidth, in order to have enough information about the required frequency

response of the matching networks.

Step 7 : After obtaining enough data points in the frequency bandwidth, the matching networks can be designed using broadband matching network design techniques [60, 64]. To utilize the broadband matching network design procedure of [60, 64], the measured optimum impedances should be fitted with proper impedance models over the design frequency range. By selecting proper port reference impedances, the insertion loss shape should be selected to fulfill both amplitude and phase requirements. The matching networks then can be implemented by finding the corresponding circuit element values.

Step 8 : The input matching networks for the desired frequency band is designed using the broadband matching network design technique.

The design procedure for this architecture is summarized as a flow chart in Fig. 3.11.

3.6 Experimental Validation

To verify the design procedure given in the last sections, two wideband TLLM amplifiers were designed using discrete transistors in Gallium Nitride (GaN) technology. Since the TLLM amplifier does not utilize the Doherty combiner, the losses at the output are minimal and higher efficiency can be obtained compared to the Doherty amplifier in millimetre-wave (mmW) frequencies where the passive component losses are a main reason for performance degradation. A TLLM amplifier is implemented in Complementary Metal-Oxide Semiconductor (CMOS) technology for operation at 60 GHz frequency to show its suitability at mmW frequency range.

3.6.1 Wideband TLLM Amplifier Fabricated in GaN Technology

An amplifier was designed using the TLLM architecture and design procedure at the frequency range of 1.8-2.4 GHz. The device used for this prototype was the CGH40010F GaN transistor from Cree. The device was characterized in terms of the optimum load and source

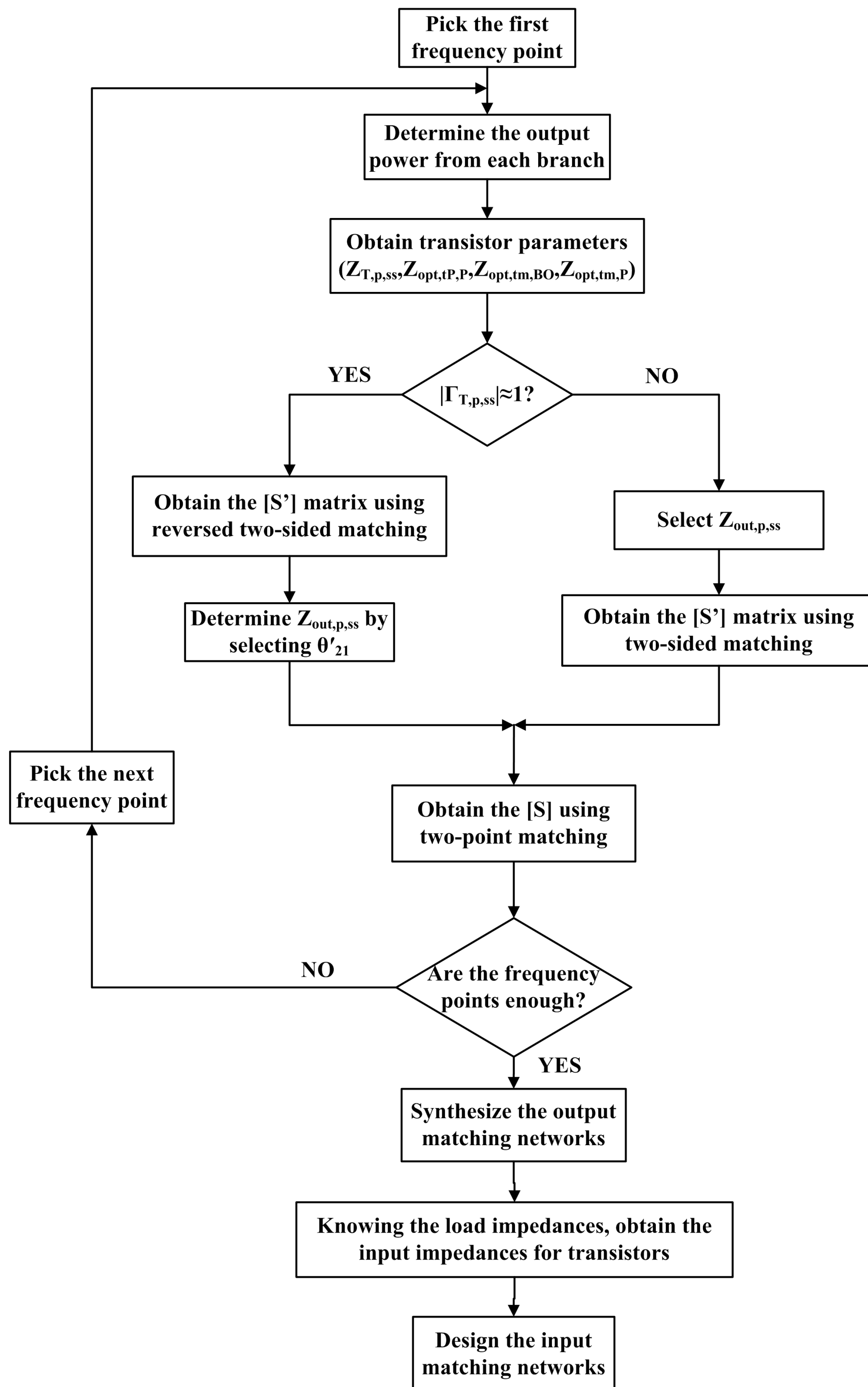


Figure 3.11: Flow chart of the TLLM amplifier's design procedure.

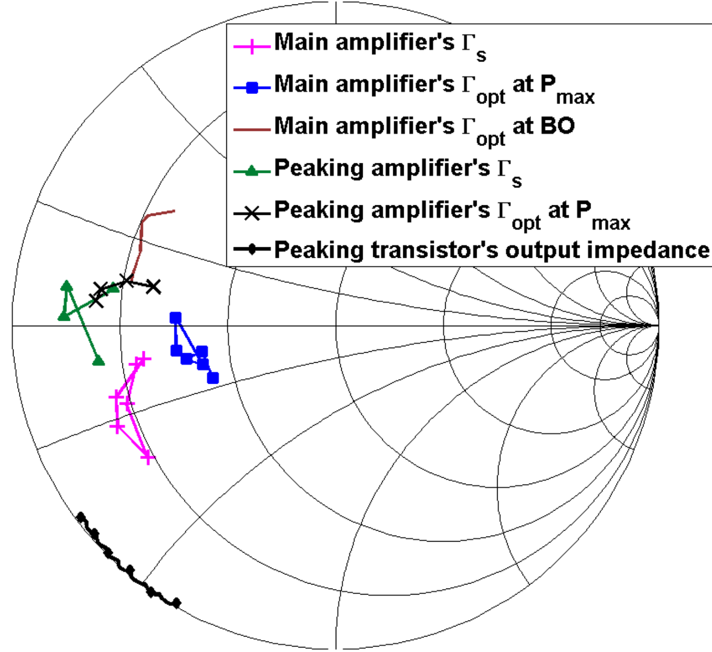


Figure 3.12: Measured impedances for main and peaking transistors.

impedances at six frequency points in the design bandwidth. The class-C small-signal output impedance was also measured at the design band using a vector network analyzer. These impedances for the frequency range of 1.8-2.4 GHz are shown in Fig. 3.12.

As can be seen in Fig. 3.12, the output reflection coefficient of the peaking transistor has a magnitude close to unity; therefore, reversed two-sided matching can be used for the peaking amplifier's output matching design. The source impedances shown in Fig. 3.12 were measured including bias and stabilization circuit.

Although it is not necessary, we designed the main and peaking amplifiers to have the same output power at full drive. The drain biases of the main and peaking amplifiers were selected to be 25 V and 30 V, respectively, so that both amplifiers have the same output power at saturation.

To design the matching networks, a series *RLC* (resistor-inductor-capacitor) network model was fitted to the measurement data for each measured impedance. Using this model, the analytical approach presented in [60] can be used to design the matching networks.

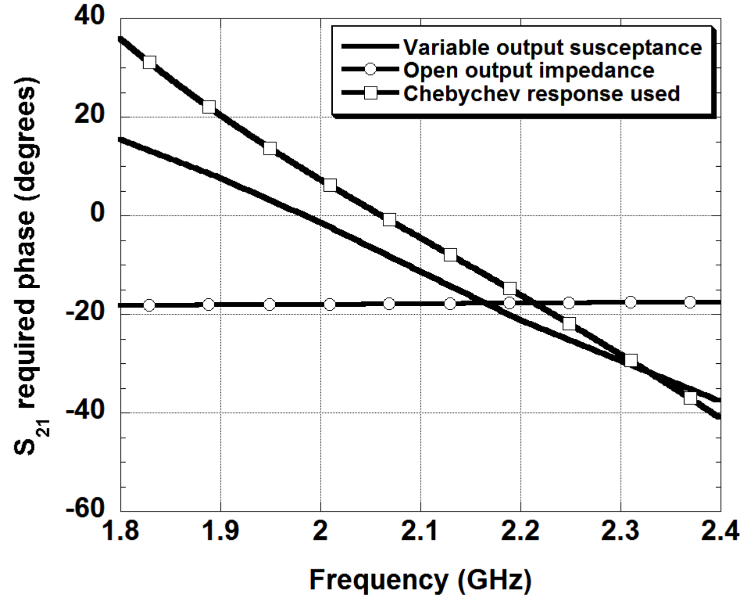


Figure 3.13: Transmission phase required for the main amplifier's output matching network.

For the output matching networks, the design was started by the peaking amplifier's output matching network. As can be seen from the main amplifier's optimum impedances (Fig. 3.12), they do not change significantly in the desired bandwidth; therefore, it is better to use the procedure mentioned in Section 3.4.2. By considering $-1/2 < B_{out,p,ss} < 1/2$, and selecting the second-order Chebychev response with a 0.2 dB ripple, the peaking amplifier's output matching network can be designed using the reversed two-sided matching procedure. The bandwidth of the Chebychev response was selected to be between 1.8 and 2.8 GHz, because of the transmission phase requirement on the matching network. The wider bandwidth was selected to follow the desired transmission phase response in the design bandwidth (1.8-2.4 GHz), as well as the amplitude response.

After designing the peaking amplifier, the main amplifier's load impedance at back-off was determined. Using this load impedance, the transmission phase needed for the main amplifier is shown in Fig. 3.13. The required phase when the peaking amplifier presents open impedance at its output is also shown in this figure. As can be seen, if the peaking amplifier has open output impedance, it is almost impossible to implement the matching

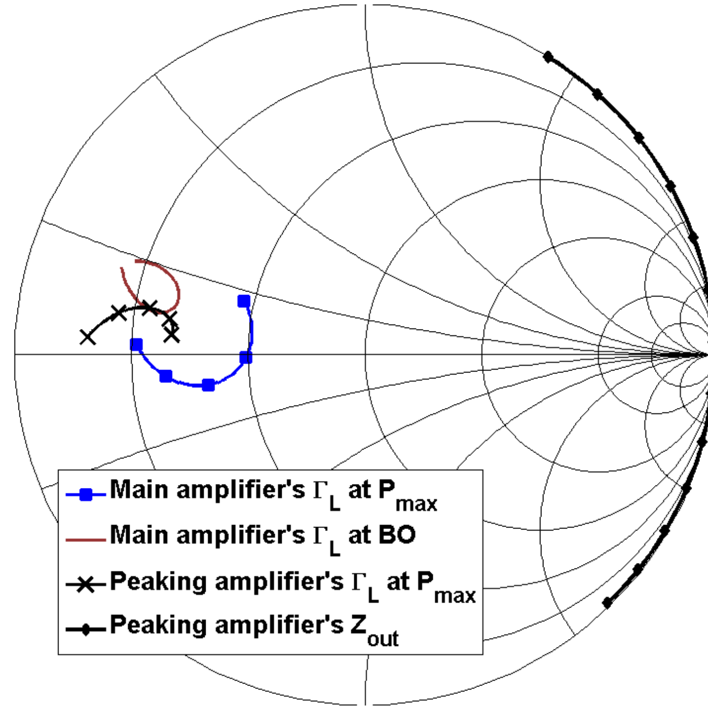


Figure 3.14: Synthesized load impedances for main and peaking transistors.

network, since it needs nearly zero group delay. The change in slope shown in Fig. 3.13 is a little bit higher than the one shown in Fig. 3.10, because the optimum impedances are not fixed points in the design frequency band, as was assumed in obtaining Fig. 3.10.

To realize the required phase response, the second-order Chebychev response with a ripple of 0.2 dB was used at the band of 1.7-2.5 GHz for the main amplifier to nearly meet both amplitude and phase requirements. The phase of this response is also shown in Fig. 3.13. There is a difference between the phase selected and the required phase range, which comes from the Bode-Fano limitation on the matching network, since it limits the bandwidth. In the Doherty architecture, the impedance transformer and the offset lines used for compensation, add a large group delay to the matching network's response. It is obvious that adding more delay to the output matching network will cause more deviation from the desired phase response, which will result in degradation of the bandwidth.

The input matching networks were designed for the main and peaking amplifiers using the

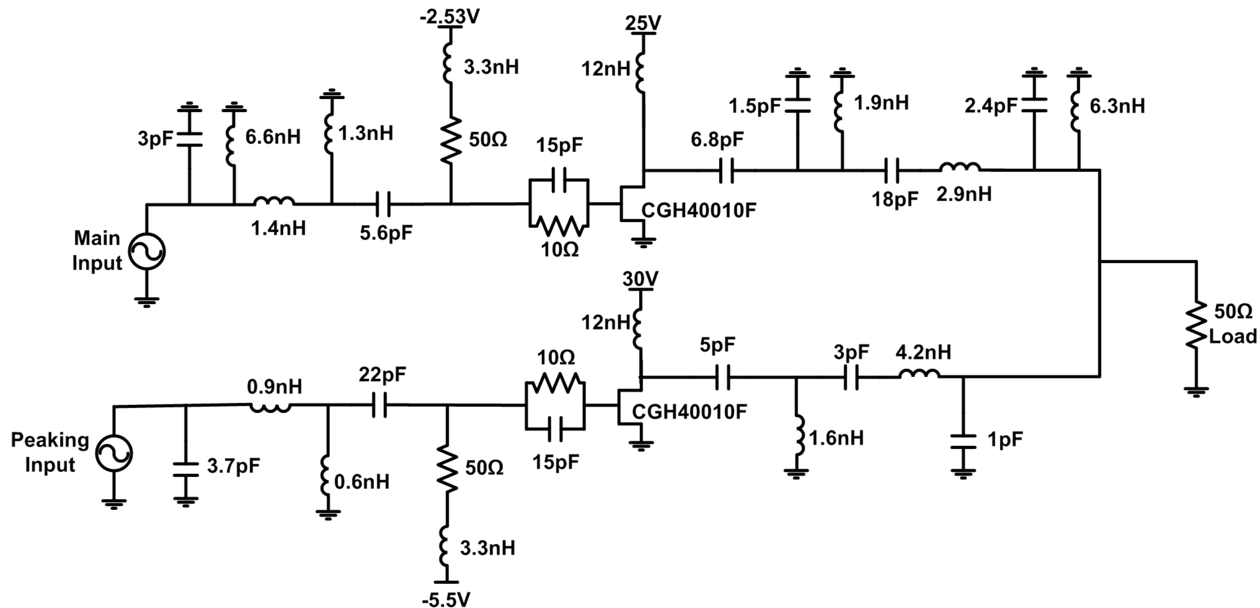


Figure 3.15: Schematic of the PA with component values.

second-order Chebychev responses of 0.1 and 0.2 dB ripples for the 1.8-2.4 GHz bandwidth, respectively.

The matching network synthesis was done using lumped elements [60]. The simulated load impedances at back-off and peak power for the main transistor and the load impedance at peak power for the peaking transistor are shown in Fig. 3.14. As can be seen from Figs. 3.12 and 3.14, the matching networks have the proper matching function in both back-off and peak power for both amplifiers over the frequency band. The output impedance of the peaking amplifier is also shown in Fig. 3.14, which lay in the desired range of $-1/2 < B_{out,p,ss} < 1/2$. The complete circuit schematic utilizing the ideal component matching networks is shown in Fig. 3.15.

In realizing the matching networks, the inductors were replaced with high-impedance short transmission lines in the printed circuit board (PCB) of the amplifier, because the physical lumped inductors have large parasitics. Coilcraft 0603CS inductors were used for the bias circuits. The capacitors used in the circuit were ATC 100A series with a voltage rating of 150 V. To match the delay and the phase of the main and peaking amplifier

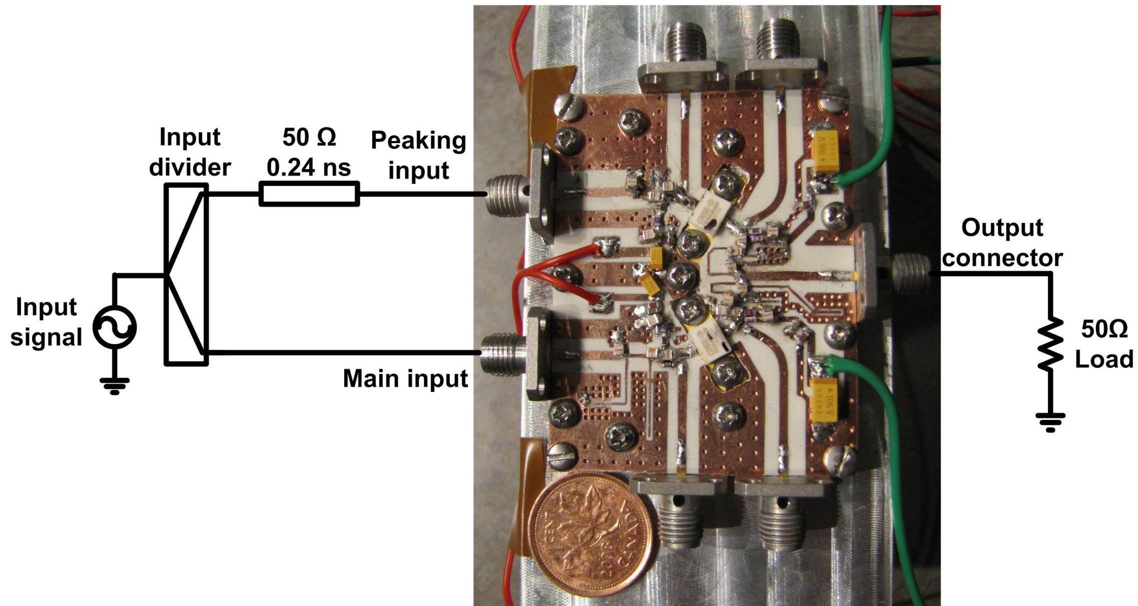


Figure 3.16: PCB of the fabricated PA and the test setup .

branches, a delay line was inserted at the peaking amplifier's input. The fabricated PA's PCB is shown in Fig. 3.16.

The designed amplifier was tested in 1.8-2.5 GHz frequency band. The two transistors were biased at the same condition used in the characterization procedure. The main transistor was biased at the bias current of 200 mA, and the peaking transistor's gate bias was -5.5 V.

The maximum input power to the amplifier was 31 dBm, and the power was split equally between the two amplifier branches. The measured small-signal gain versus frequency is shown in Fig. 3.17, and the measured power gain versus output power is shown in Fig. 3.18 at different test frequencies. The maximum output power versus frequency is shown in Fig. 3.19. The maximum output powers were measured at the point where the gain compression was less than 5 dB.

The small signal gain and maximum output power show a drop around 1.9-2.0 GHz frequency. This drop is caused by the 6.8 pF capacitor connected to the drain of the main transistor (Fig. 3.15). The 6.8 pF capacitor in the ATC 100A series has its resonant frequency

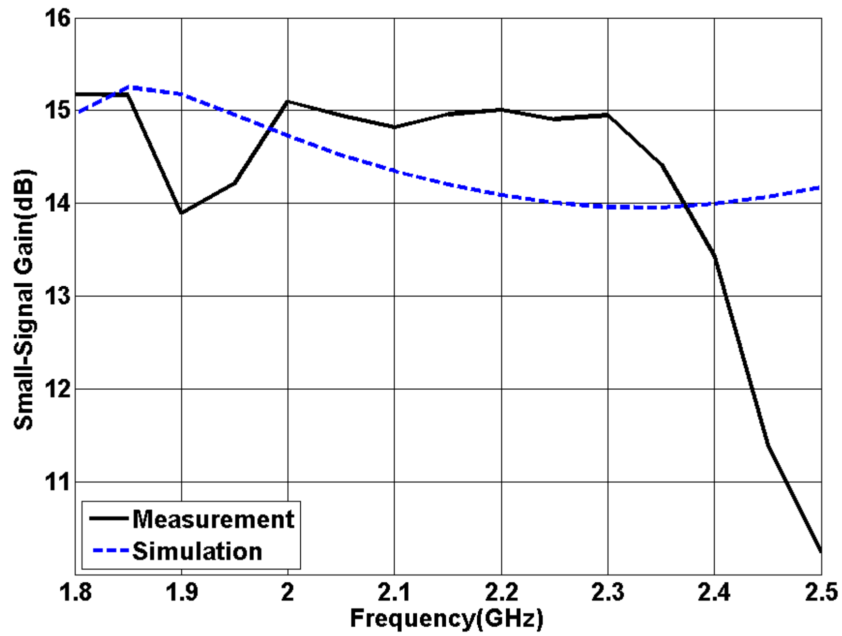


Figure 3.17: Measured and simulated amplifier's small-signal gain versus frequency.

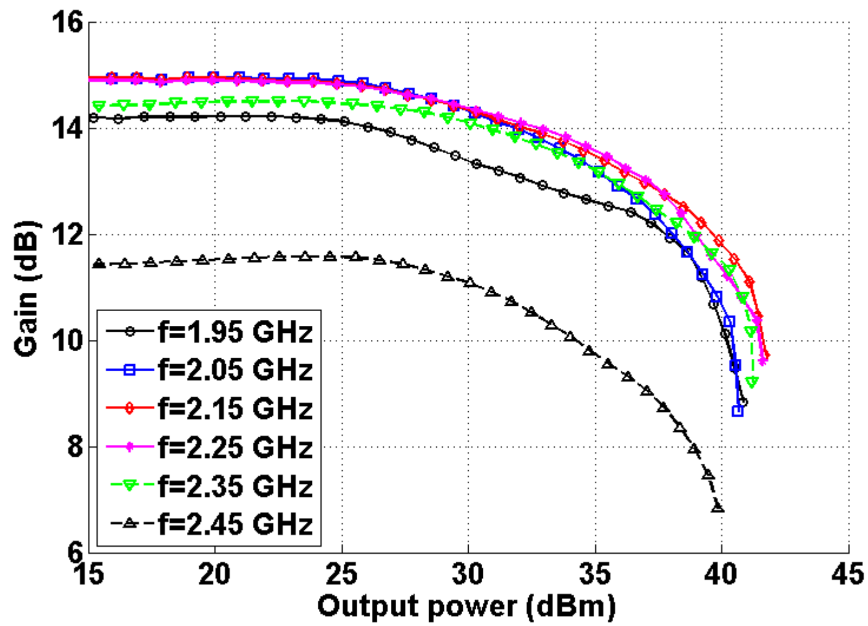


Figure 3.18: Measured power gain versus output power at different frequencies.

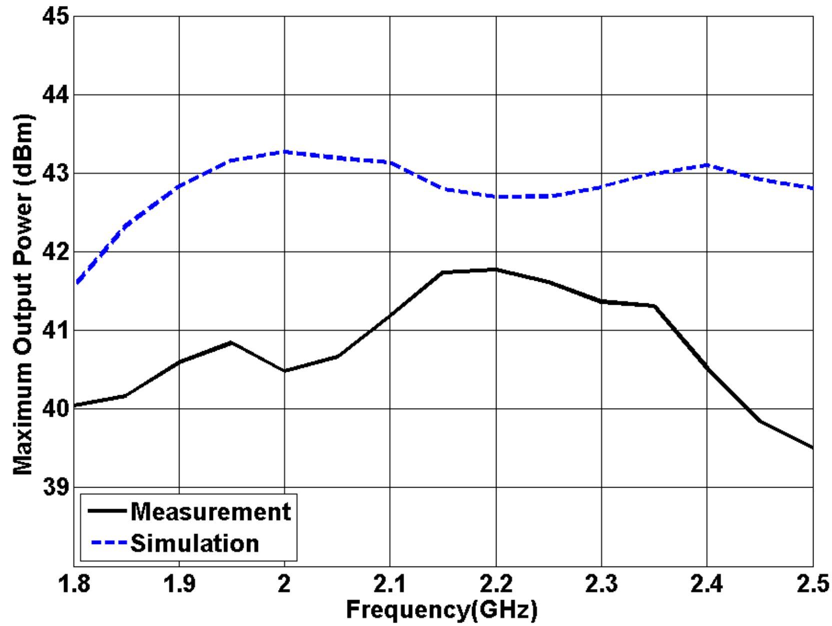


Figure 3.19: Measured and simulated maximum output power versus frequency.

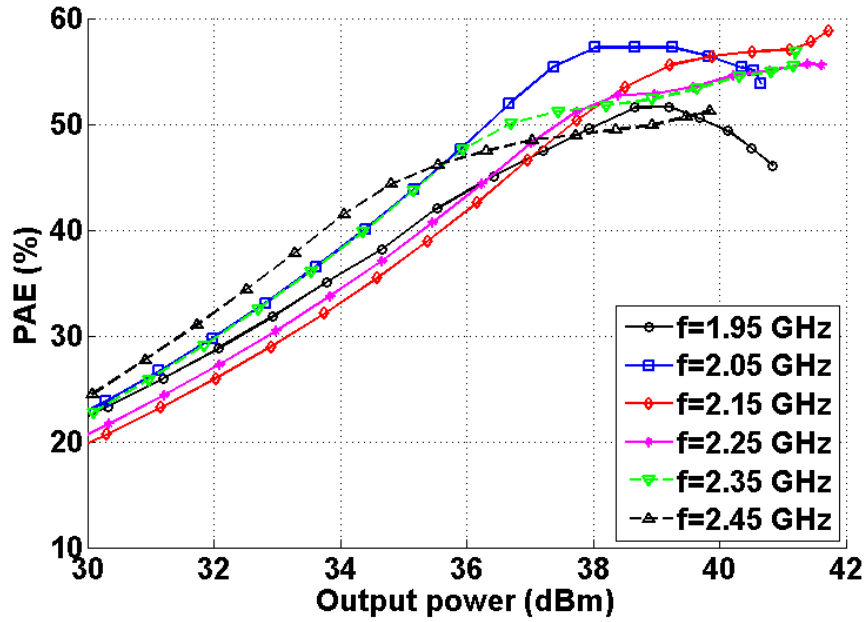


Figure 3.20: Measured PAE versus output power at different frequencies.

around 3.9 GHz which is the second harmonic of 1.95 GHz where the gain and output power show a drop.

The measured power-added efficiency (PAE) versus output power is shown for different

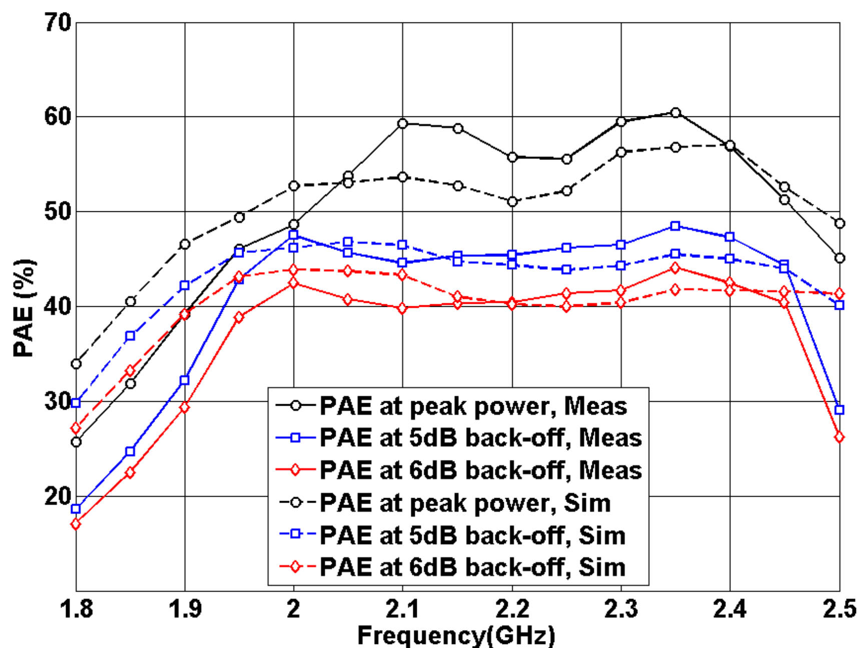


Figure 3.21: Measured and simulated PAE at peak power and 5- and 6-dB power back-off versus frequency.

frequencies in Fig. 3.20, and the PAEs at peak power, 5 dB and 6 dB back-off powers are shown in Fig. 3.21. As can be seen from these graphs, the PAE remains higher than 40% at a 6dB power back-off for a nearly 500 MHz bandwidth. There was a shift and also bandwidth shrinkage in the measurement results, which was caused by the parasitics in the matching networks.

The two-tone test was done to measure the linearity properties of this PA. Third-order inter-modulation (IMD3) products were measured by applying a two-tone signal with a 1 MHz frequency separation. By sweeping the power of the two-tone signal at different frequencies, the IMD3 products were measured versus output power. Fig. 3.22 shows the measured IMD3 products versus output power.

The PA was also tested with a WiMAX (Worldwide Interoperability for Microwave Access) input signal with a 7.3 dB PAPR in a center frequency of 2.15 GHz . The values of the adjacent channel power ratio (ACPR) and PAE were measured with the WiMAX input signal. The measured ACPR level and PAE versus output power are shown in Fig. 3.23. As

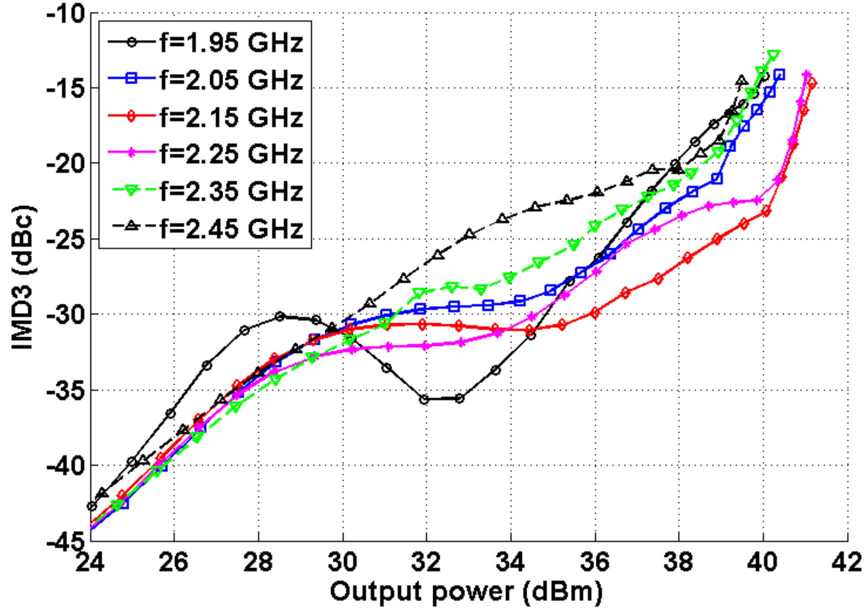


Figure 3.22: Measured IMD3 products versus output power at different frequencies.

Architecture	Frequency Range	Fractional Bandwidth	Min PAE at 6 dB BO
Conventional Doherty [31]	2.04-2.22 GHz	8%	40%
TLLM amplifier	1.96-2.46 GHz	23%	40%

Table 3.1: Comparing the TLLM amplifier with a conventional Doherty amplifier.

can be seen from this figure, the PAE at a 7.3 dB output power back-off from the maximum output power of 41.7 dBm is 40%. This is due to the combination of the probability density function (PDF) of the signal and the continuous wave PAE of the PA.

To assess the performance of the proposed architecture, a conventional Doherty PA was used to benchmark the results. The conventional Doherty PA was designed using a quarter wave impedance transformer and offset lines as reported in Section I of [31] and implemented using identical GaN devices to those used in the proposed TLLM PA. The performance of

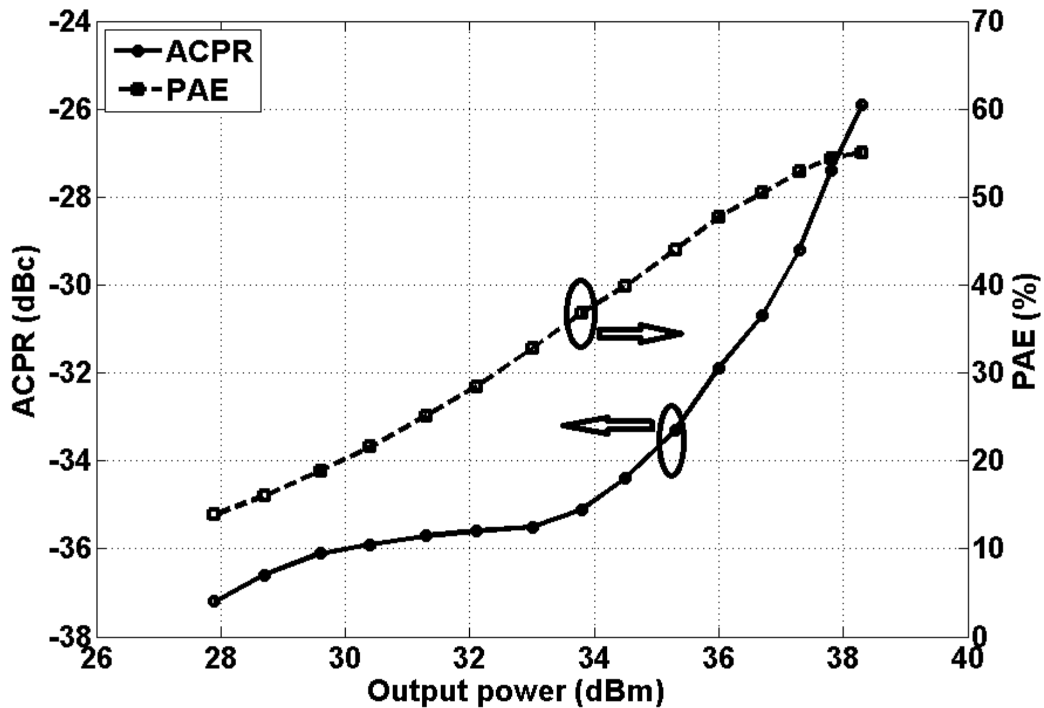


Figure 3.23: Measured PAE and ACPR versus output power for a WiMAX input signal.

the proposed architecture is compared with the conventional Doherty PA in Table 3.1. As can be seen from this table, the fractional bandwidth of the proposed architecture has a significant improvement (250%) over the conventional Doherty amplifier.

3.6.2 Wideband TLLM Amplifier Simulation

The TLLM amplifier implemented in the previous section as a proof of concept provided 23% fractional bandwidth. It should be noted that the TLLM amplifier can provide much larger bandwidth through proper utilization of transistors and biases. In this section, a simulated design example is presented in this chapter providing 50% fractional bandwidth (©2013 IEEE) [1]. For the design of the second TLLM amplifier, the devices and working conditions selected to be the same as the conditions reported in [32] for easier comparison.

[1]M. Akbarpour, M. Helaoui and F. M. Ghannouchi, "Broadband Doherty Power Amplifiers", in *2013 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR 2013)*, Austin, TX, USA, pp. 1-3, 20-23 January 2013.

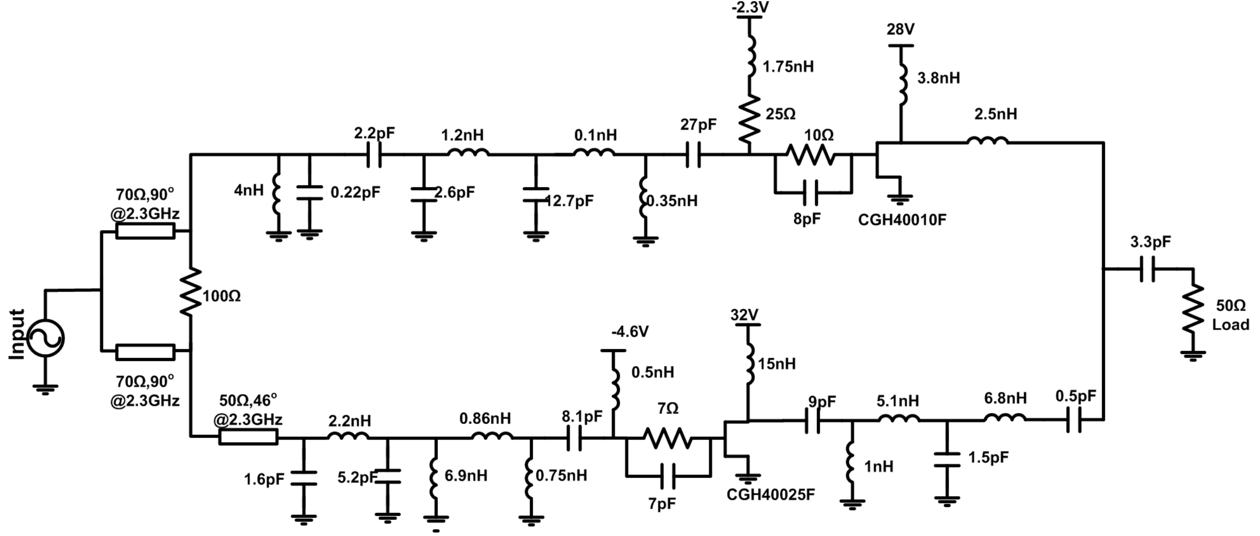


Figure 3.24: Schematic of the simulated TLLM power amplifier.

The 10 Watt GaN CGH40010F device was used as the main transistor and the 25 Watt GaN CGH40025F device was used as the peaking transistor. Both transistors are from Cree. The nonlinear models provided by the manufacturer were used for the simulation in Agilent ADS. The bias points were selected to be the same as what is used in [32] for comparison reason.

Using the design procedure provided in the previous sections and implementing the matching networks by the lumped elements, the amplifier's schematic shown in Fig. 3.24 is obtained. As can be seen from this figure, the output matching network of the main amplifier is very compact and simple. The simulated small-signal gain, the maximum output power and the drain efficiency at 6 dB power back-off of the amplifier are shown in Fig. 3.25. The gain roll-off seen in the small signal gain can be avoided by modifying the main amplifier's input matching network if needed. The maximum output power of the amplifier is higher than 42 dBm or 16 Watts and the drain efficiency is higher than 47% in the 1.7-2.8 GHz frequency band. Comparing the drain efficiency with the simulation results shown in Fig. 17 of [32] shows that using TLLM architecture, similar fractional bandwidth is obtained.

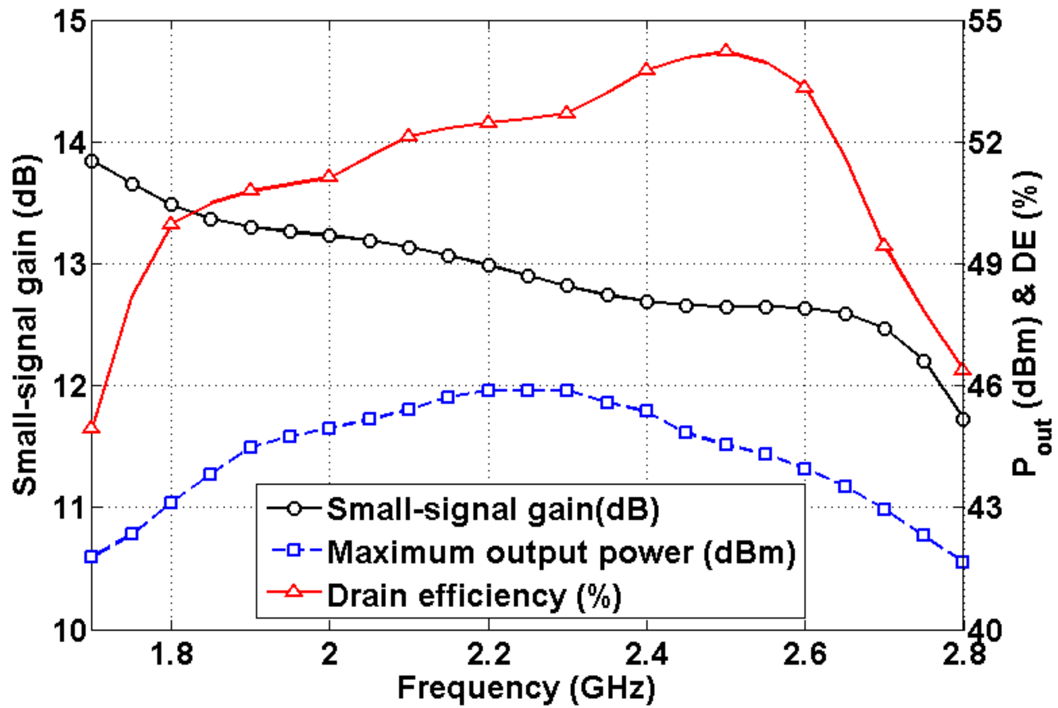


Figure 3.25: Simulated performance of the TLLM amplifier shown in Fig. 3.24.

3.6.3 60 GHz CMOS TLLM Amplifier

Since the TLLM amplifier does not need the power combiner, the two amplifier branches are directly connected together. This means that the losses at the output of the amplifier are minimal. This property makes the TLLM amplifier suitable for the mmW amplifiers because the conductive losses are dominant at those frequencies and the losses result in low amplifier efficiency.

To study the capability of TLLM amplifier, a prototype is implemented in 65nm CMOS technology by Taiwan Semiconductor Manufacturing Company (TSMC). The amplifier is designed to operate at 60 GHz centre frequency. The targeted maximum output power is selected to be 11 dBm. The source and load impedance are selected to be 50 Ω to facilitate measurement process using standard 50 Ω equipment.

The main amplifier branch is designed as a two stage cascode class AB amplifier. The peaking amplifier is designed as a three-stage cascode class C amplifier. Cascode stages

were used to improve stability and gain performance of each stage. Cascode stages also allow using higher bias voltages with proper design considerations. The number of stages in peaking branch is higher than the main amplifier because peaking amplifier is biased in class C and the amplifier stages have lower gain compared to class AB biased amplifier stages. Using this configuration allows equal gain for the two branches at peak output power.

The transistor models provided by the factory was used to simulate the performance of the amplifier. These models are valid up to 35 GHz, but we used the same models for designing the amplifier at 60 GHz frequency. Measurements from a previously fabricated amplifier showed that simulation results are accurate in terms of gain and efficiency, but they are not accurate in terms of voltage and current phase in the amplifier circuit. As a result, to have better control over the phase of output currents from two amplifier branches, the amplifier was implemented with separate inputs for each amplifier. Using two inputs, the inaccuracies in simulation of output current phases is ruled out.

Transistor Biasing

The bias voltage for the CMOS transistors is limited by their low breakdown voltages. Low breakdown voltage of CMOS transistors necessitates use of large transistors to increase current swing in order to obtain required output power. On the other hand, increasing transistor's size decreases its optimum load impedance for output power and efficiency which makes design of matching networks more difficult.

Due to stacking of transistors, cascode structure allows the use of higher voltages for biasing amplifier stages. By proper selection of gate voltages, one can use bias voltage that is higher than each transistor's breakdown voltage and guarantee that the voltage on each transistor would not exceed its breakdown voltage. A bias voltage of 1.6 V is selected for biasing amplifier stages in the design while maximum allowed voltage for the transistors is 1.2 V. Fig. 3.26 shows the bias schemes used for the main and peaking amplifier stages respectively. Fig. 3.27 shows the drain-source and gate-source voltages on each transistor

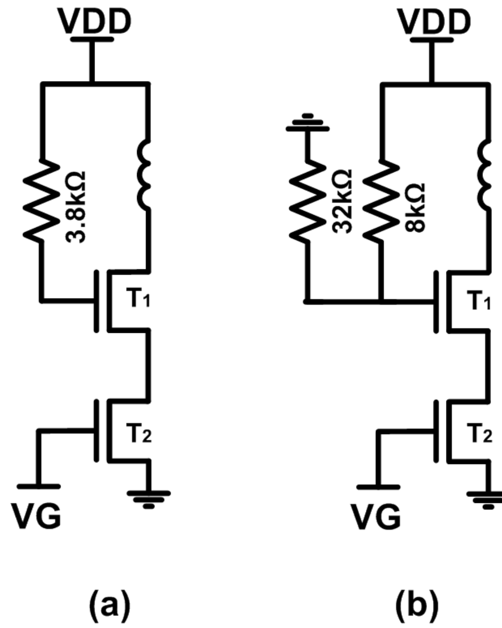


Figure 3.26: Bias scheme for (a) main amplifier (b) peaking amplifier.

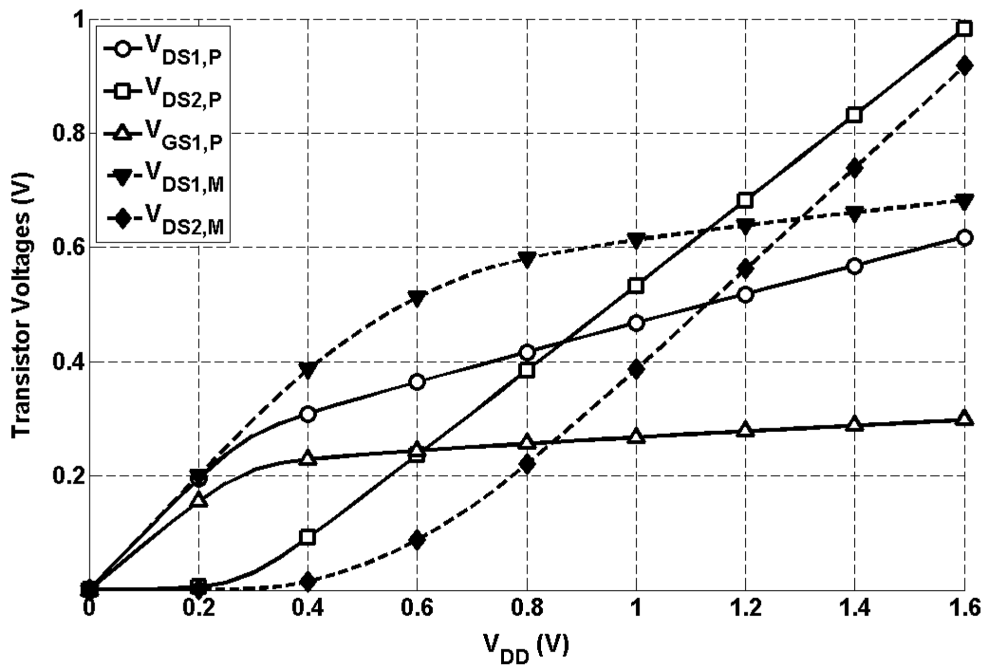


Figure 3.27: Bias voltages on main and peaking transistors.

for main and peaking amplifier cascode stages versus supply voltage. As can be seen from Fig. 3.27, the transistor voltages do not exceed 1 V for supply voltages up to 1.6 V.

Gate voltage of 650 mV used for common source transistors of main amplifier stages to

maximize the cascode stage gains while maintaining stability of the stages around the design frequency. To ensure stable operation of the amplifier stages in low frequencies, resistors were used at gate bias path. For peaking amplifier stages, slightly different gate voltages were used. The last stage was biased close to class B to let this stage provide more gain and enough output power required for load modulation at maximum input power. The first two stages were biased in class C so that the peaking amplifier turns on at the required input power. The gate voltages for peaking amplifier stages were selected to be 230 mV, 230 mV and 250 mV respectively. Using these gate voltages, the voltages across the transistors does not exceed the maximum allowed voltage.

The sizes of transistors were selected using the procedure given in [66]. The amplifier is designed for the output power of 11 dBm which means each branch has to provide 8 dBm of output power. By using bias voltage of 1.6 V and saturation voltage of 0.4 V for the cascode amplifier, the size of the transistors used in the last stage of the main amplifier can be obtained as [66]:

$$W = \frac{4P_{max}}{0.4(V_{DD} - V_{DS,sat})} = \frac{4 \times 6}{0.4 \times 1.2} = 50 \tag{3.32}$$

The size of the driver stage for the main amplifier branch is obtained using the same procedure. The total width of transistors used for main amplifier's driver stage is 19.2 μm. The transistor size for the peaking amplifier was obtained experimentally such that it turns on when the main amplifier reaches the output power of 5-6 dBm and it can provide enough output power for proper load modulation. The transistor sizes used for peaking amplifier stages are 19.2 μm, 57.6 μm and 128 μm respectively.

Designing Output Matching Networks

Using small signal S-parameter simulation, the output impedance for the peaking transistor was obtained. By load-pull simulations, the output power contours for output power were obtained for both main and peaking amplifier stages at maximum input power. Also the

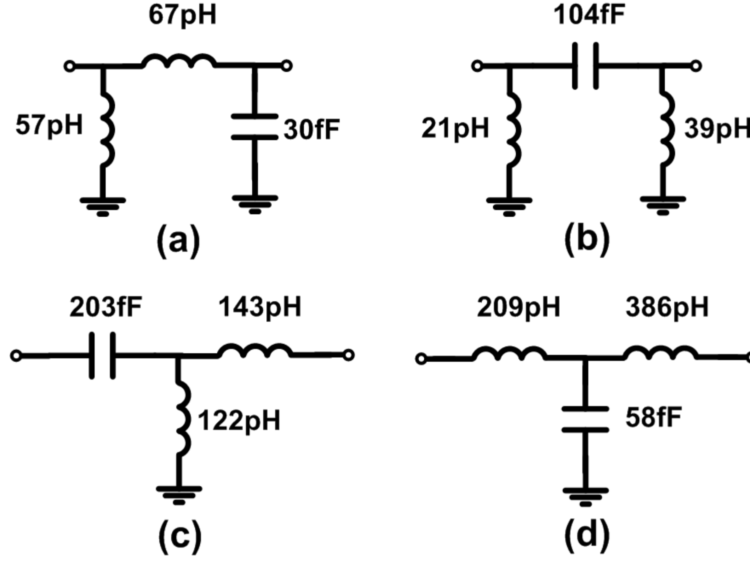


Figure 3.28: Possible network realizations for peaking amplifier's output matching network.

optimum impedance for efficiency was obtained for the main transistor at power back-off.

The peaking amplifier output matching network is designed using the two-sided matching technique. The output impedance of the peaking amplifier was selected to be 500 Ω to have high output power while maintaining the power leakage less than 10%. The S parameters obtained for the peaking amplifier's output matching network in 50 Ω reference impedance are:

$$\mathbf{S} = \begin{bmatrix} -0.59 + j0.43 & \pm(0.67 + j0.13) \\ \pm(0.67 + j0.13) & 0.38 + j0.63 \end{bmatrix} \tag{3.33}$$

As can be seen from (3.33), there are two solutions for the S-parameters. Fig. 3.28 shows the synthesized Π and T networks based on the obtained S-parameters. The network shown in Fig. 3.28-a is selected as the output matching network. Using the network of Fig. 3.28-a, the losses are minimal and the bias can be applied to the transistor through the matching network and there will be no need for additional biasing components.

The main amplifier's output matching network is designed using the two-point matching technique. Fig. 3.29 shows the output matching network impedance transformations along

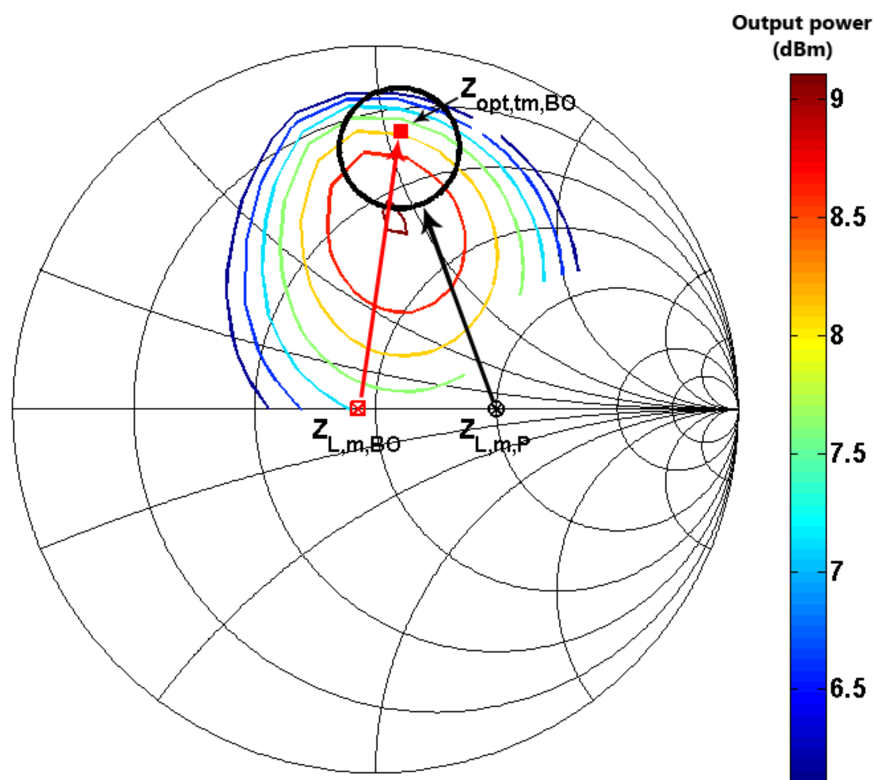


Figure 3.29: Graphical illustration of two-point matching for the circuit of Fig. 3.26-a in 50 Ω Smith chart.

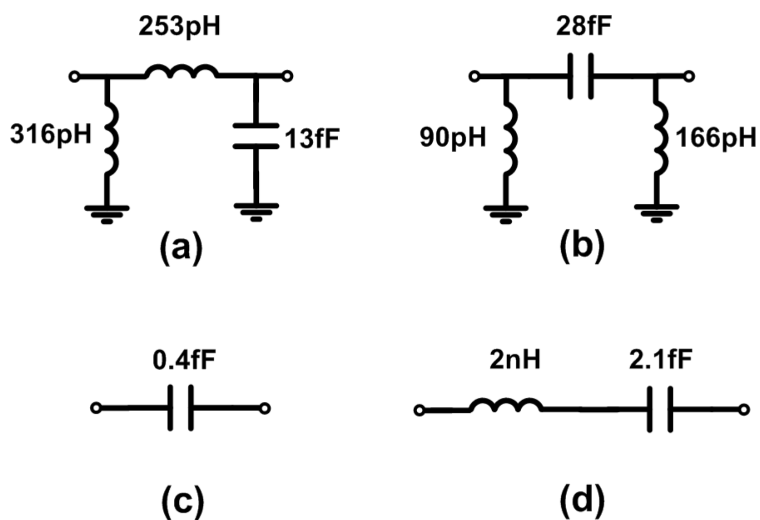


Figure 3.30: Possible simple network realizations for main amplifier's output matching network.

with the output power contours at peak input power. The S-parameters obtained for the main amplifier's output matching network in 50 Ω reference impedance are:

$$\mathbf{S} = \begin{bmatrix} 0.07 + j0.75 & \pm(0.51 - j0.42) \\ \pm(0.51 - j0.42) & 0.72 + j0.20 \end{bmatrix} \tag{3.34}$$

Fig. 3.30 shows the synthesized Π and T networks based on the obtained S-parameters. The network shown in Fig. 3.30-a is selected as the realizable output matching network to minimize the losses.

Designing Interstage and Input Matching Networks

To design the inter-stage and input matching networks, load pull analysis was done to obtain each stage's optimum load impedances at peak input power. Also large-signal S-parameter (LSSP) simulations were done to obtain large signal input impedance of each stage then using three to four elements the matching networks were designed. The input matching networks were designed for 50 Ω source impedance. The complete amplifier's schematic after compensating for the layout parasitic is shown in Fig. 3.31. Due to layout design rules, the input and inter-stage matching networks were implemented using shielded coplanar transmission lines presented in [67]. The transmission lines used in the matching networks were simulated using CST Microwave Studio full-wave electromagnetic simulator. The EM (Electromagnetic) simulation results were used for simulation of amplifier performance.

Measurement Results

The layout of the fabricated amplifier is shown in Fig. 3.32. Total chip dimensions used for the amplifier including bias and input/output pads are 0.6 mm$\times$1.13 mm and the amplifier dimensions excluding pads are 0.43 mm$\times$0.85 mm. During measurements, the chip was glued to the printed circuit board and the bias pads were wire-bonded to the PCB.

For S-parameter test, an Anritsu ME7808B vector network analyzer (VNA) was used. The input and output pads of the chip were connected to the VNA ports using GSG (Ground-

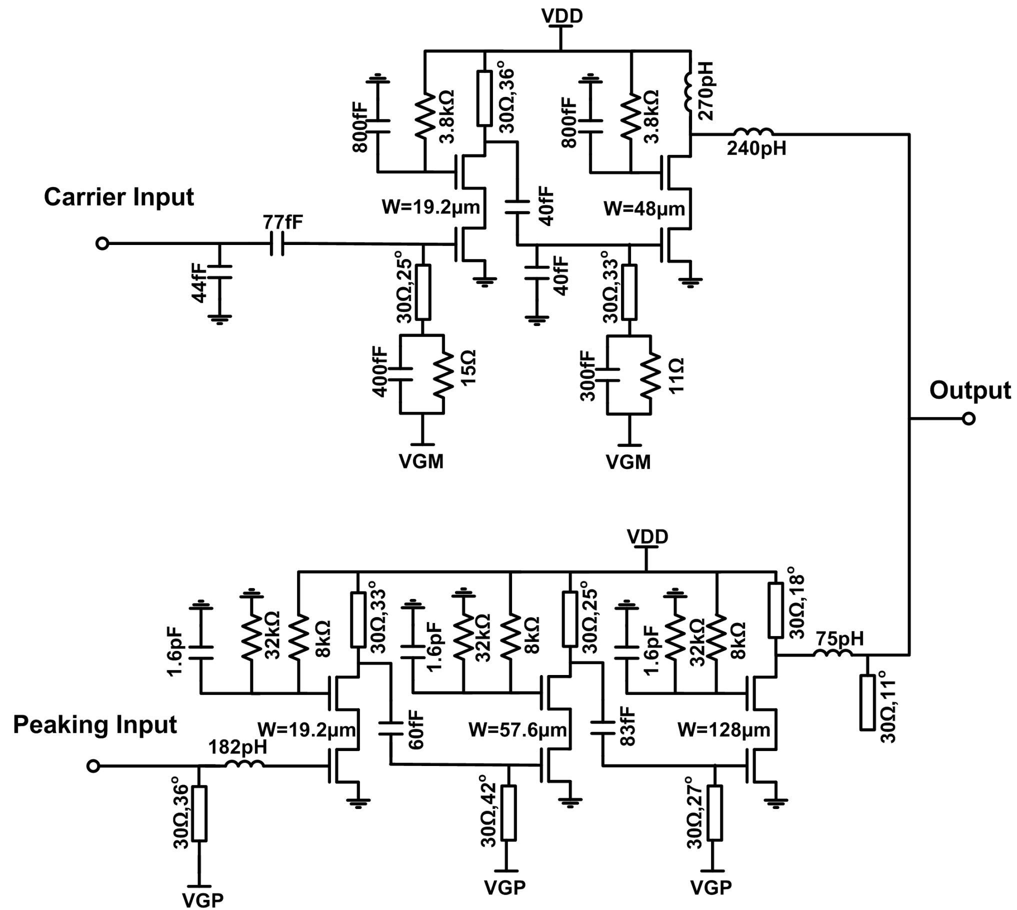


Figure 3.31: Implemented 60GHz TLLM amplifier's schematic.

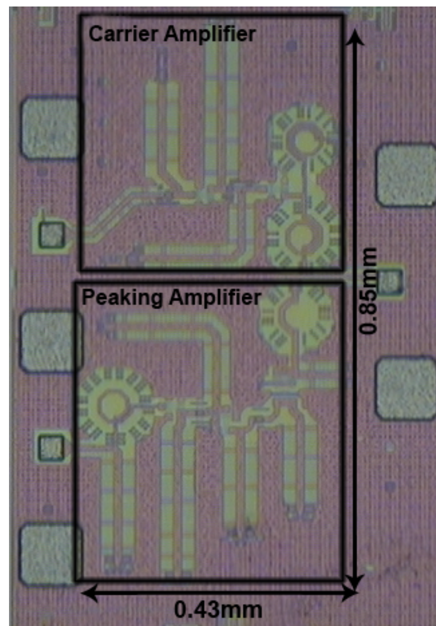


Figure 3.32: Chip micrograph of fabricated 60GHz TLLM power amplifier.

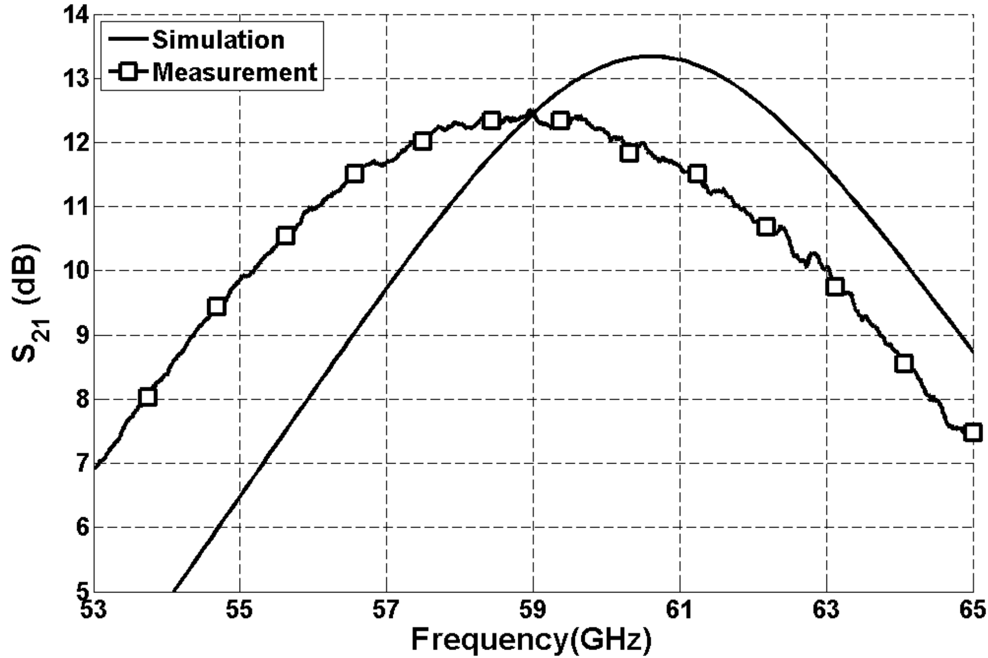


Figure 3.33: Simulated and measured small-signal gain.

Signal-Ground) probes. At low input power the peaking amplifier is in off state, and the input signal was applied only to the main amplifier's input. In order to have proper output impedance from the peaking amplifier, its bias was connected during S-parameter test. VNA calibration was done using SOLT (Short-Open-Load-Thru) calibration standards on an impedance standard substrate (ISS). Fig. 3.33 shows the simulated and measured gain of the amplifier in 55-65 GHz frequency range. Maximum measured small signal gain is 12.5 dB at 59 GHz. In simulation results, maximum gain is obtained at 60.6 GHz because the amplifier is designed based on large signal transistor parameters. Measurement results show around 1.5 GHz shift towards lower frequencies which is resulted by inaccuracies in the element models.

Fig. 3.34 shows the simulated and measured gain and output power of the whole amplifier versus input power at 59 GHz frequency. Maximum output power obtained is 11.5 dBm. Simulated and measured drain efficiency and power-added efficiency are shown versus output power in Fig. 3.35. Maximum measured drain efficiency obtained from the amplifier is 12.7%.

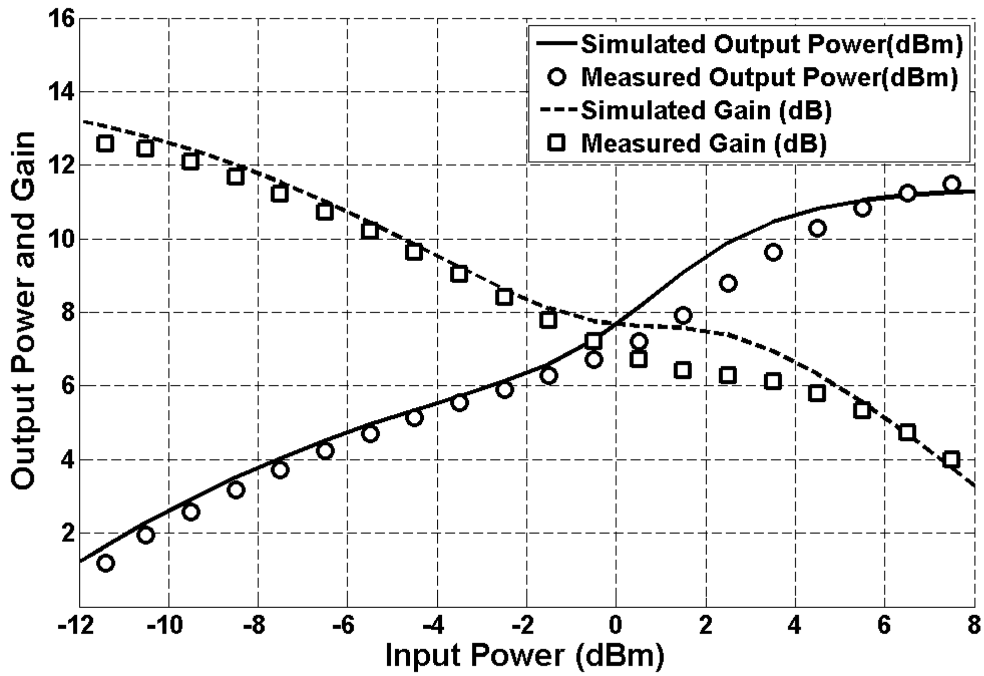


Figure 3.34: Gain and Output power vs. input power.

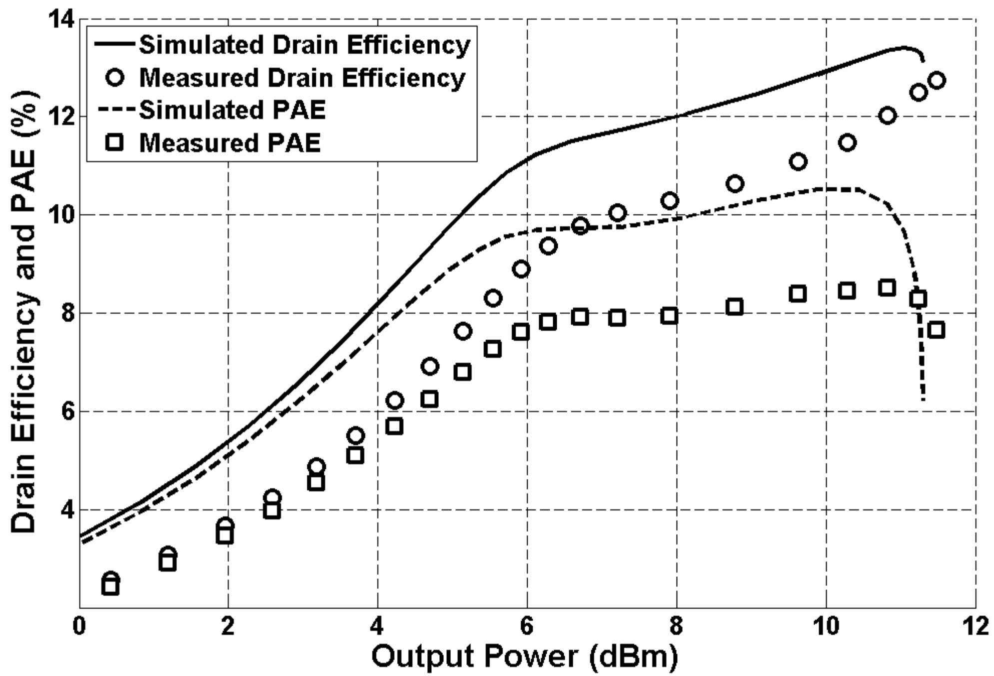


Figure 3.35: Drain and power-added efficiency vs. output power.

Reference	Frequency (GHz)	Technology	Gain (dB)	P_{sat} (dBm)	Gain Compression at P_{sat} (dB)	DE_{6dB} (%)	PAE_{6dB} (%)
[68]	60	90 nm	5.5	12.3	3	8	5.5
[69]	60	90 nm	20.6	19.9	8.5	7.7	7.6
[70]	60	65 nm	19.2	18	12	3	3
[71]	55-67	65 nm	18.2	9.6	9.5	3.8	3.7
[72]	60	65 nm	24	18	15	3	3
[73]	60	65 nm	15.8	11.5	13	7.3	6.9
[74]	60	65 nm	20	15.6	15	2	2
[75]	57-64	90 nm	12	11.4	15.5	8	7.5
[76]	60	130 nm	13.5	7.8	8	1.3	1.2
This work	60	65 nm	12.5	11.5	8.5	8.3	7.2

Table 3.2: Performance Summary and Comparison for the TLLM 60 GHz CMOS amplifier.

The value of power-added efficiency remains higher than 7% in the last 6 dB output power range which means that the amplifier has higher than 7% efficiency for a modulated signal with 6 dB peak-to-average power ratio.

Table 3.2 shows the results obtained from the implemented TLLM amplifier along with a comparison to the state-of the art CMOS power amplifiers. Power added efficiency values obtained by the references at 6 dB power back-off are in the range of 1-7%. Another parameter that should be considered in the performance of amplifier is the gain compression which is important in terms of amplifier's linearity. In the two references which obtained highest efficiency at power back-off, the gain compression values at maximum output power are 15.5 and 13 dB. With these amounts of compression, the amplifier introduces severe distortions to the communication signal and the amplifier could not be linearized. In our work, the amount of gain compression is around 8.5 dB which can be linearized using the conventional linearization techniques.

Chapter 4

Three-Port Input/Output networks in Doherty Amplifier

As discussed in Chapter 3, the output matching networks in the Doherty structure can be designed to perform the impedance matching in both peak power and power back-off without the need for Doherty impedance transformer or the offset lines. In this chapter, a Doherty amplifier is presented with three-port input and output networks. The proposed amplifier results in a flexible and compact design suitable for all cases and specially for the integrated power amplifiers.

This chapter is organized as follows: In Section 4.1, the structure of the proposed Doherty amplifier having three-port input and output networks is given. Sections 4.2 and 4.3 provide the theory for designing output and input networks respectively. One possible way for the synthesis of three-port networks is provided in Section 4.4 and finally some design examples along with measurement results are provided in Section 4.5.

4.1 Doherty Amplifier with Three-Port Input/Output Networks

The structure of the proposed amplifier is shown in Fig. 4.1. The amplifier consists of two-transistors. The two transistors can have different output powers to obtain the desired back-off performance. Similar to the Doherty amplifier, the main transistor is biased at class AB or class B and the peaking transistor is biased at class C. The turn-on point of class C biased amplifier can be selected by the designer to obtain the desired back-off performance. The output matching/combining network (OMCN) and the input matching/divider network (IMDN) are three-port networks used at the output and input of the amplifier respectively.

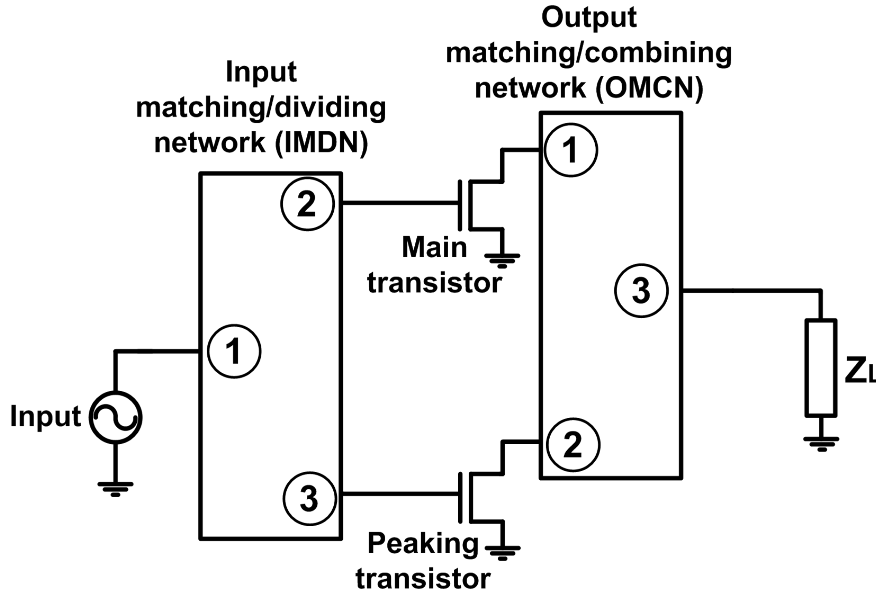


Figure 4.1: The Doherty amplifier with three-port input and output network

The input and output networks can be designed for complex source and load impedances. The ability to design the amplifier for complex load impedances is important when the amplifier is directly connected to the antenna, especially in the cases where an electrically small antenna is used [77, 78]. The power amplifier can be directly connected to the antenna when the antenna does not need a balun at its input and it is integrated with the power amplifier. In this case, the amplifier can be designed to be matched directly to the antenna's input impedance without the need for additional circuit elements. For input, the ability of designing for complex source impedance is important when the amplifier is to be connected to a driver amplifier at the input. In this case, the Doherty power amplifier can be designed to be connected directly to the transistor in previous stage.

4.2 Three-Port Output Network Design

The three-port output matching/combining network (OMCN) proposed here is a non-isolated, non-symmetrical power combiner that also performs the impedance matching at peak power for both transistors and guarantees optimum performance at output power back-off. The

output powers from the two transistors can have any arbitrary ratio and the amplifier's load impedance can be any arbitrary real or complex-valued impedance. The ability of designing for any arbitrary complex load impedance is important when the power amplifier is directly connected to the antenna with complex input impedance.

The OMCN is a non-symmetrical and non-isolated power combiner network that combines the output powers from the two transistors. It also matches the arbitrary real-valued or complex-valued load impedance to the optimum impedance needed by the two transistors at peak output power and has optimal performance at output power back-off. We define the design goals for the OMCN as follows:

1- OMCN is a lossless, passive and reciprocal network.

2- At peak power, the output powers from the two transistors can have any arbitrary ratio.

3- OMCN should present optimum load impedance for maximum output power to both transistors. The two optimum load impedances can be any complex-valued impedances inside the Smith chart.

4- The amplifier's load can have any arbitrary real-valued or complex-valued impedance inside Smith chart.

5- OMCN should guarantee maximum possible efficiency at the desired output power back-off.

To obtain the S-parameters for the OMCN, a set of reference impedances should be selected. Fig. 4.2 shows the OMCN with its ports numbered from 1 to 3 and the reference impedance for each port. Port 1 is the port that connects to the main (class AB or class B biased) transistor. The reference impedance for port 1 is $Z^*_{opt,m,P}$ that is the complex conjugate of the main transistor's optimum impedance for maximum output power at peak input power [60,64]. Port 2 connects to the peaking (class C biased) transistor. The reference impedance for port 2 is $Z^*_{opt,p,P}$ that is the complex conjugate of the peaking transistor's

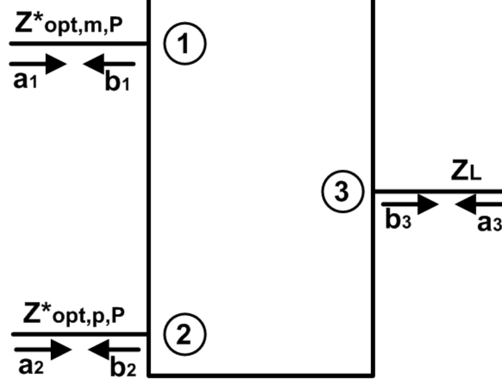


Figure 4.2: Three-port output matching/combining network and port reference impedances.

optimum impedance for maximum output power at peak input power. Port 3 connects to the load impedance. The reference impedance for port 3 is Z_L that is the arbitrary real-valued or complex-valued load impedance. The values of $Z_{opt,m,P}$ and $Z_{opt,p,P}$ can be obtained from load-pull simulation or measurement of the transistors or from load-line theory.

From design goal 2, the output powers from the two transistors can be different. To have proper power combining, the output power waves from both amplifiers have to be in-phase at port 3, but their amplitude can be different. We define parameter α as follows:

$$\frac{b_{3,2}}{b_{3,1}} = \alpha \tag{4.1}$$

In (4.1), $b_{i,j}$ is the normalized reflected power wave at port i caused solely by the normalized incident power wave to port j under matched condition. Equation (4.1) means that the ratio of the peaking amplifier's output power to the main amplifier's output power is equal to α^2. Due to superposition principle, the total b power wave at port i will be:

$$\sum_j b_{i,j} \tag{4.2}$$

To satisfy design goal 3, at peak power the normalized reflected powers b_1 and b_2 must vanish and satisfy the condition $b_1 = b_2 = 0$. This ensures that both transistors will see optimum load impedances at peak power. From (4.1) we can write:

$$\frac{b_{3,2}}{b_{3,1}} = \frac{S_{32}a_2}{S_{31}a_1} = \alpha \tag{4.3}$$

On the other hand, at peak power $b_1 = b_2 = 0$. Using this condition and (4.3), we can write:

$$b_1 = S_{11}a_1 + S_{21}a_2 = \left(S_{11} + \alpha S_{21}\frac{S_{31}}{S_{32}} \right) a_1 = 0 \tag{4.4}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 = \left(S_{21} + \alpha S_{22}\frac{S_{31}}{S_{32}} \right) a_1 = 0 \tag{4.5}$$

From (4.4) and (4.5), the S-parameters of the matching/combining network can be written as:

$$\begin{bmatrix} tS_{21} & S_{21} & S_{31} \\ S_{21} & \dfrac{S_{21}}{t} & S_{32} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{4.6}$$

$$t = -\frac{\alpha S_{31}}{S_{32}} \tag{4.7}$$

From passivity and losslessness of matching/combining network (design goal 1) we have:

$$|S_{11}|^2 + |S_{21}|^2 + |S_{31}|^2 = |S_{21}|^2 \left(1 + |t|^2\right) + |S_{31}|^2 = 1 \tag{4.8}$$

$$|S_{21}|^2 + |S_{22}|^2 + |S_{32}|^2 = |S_{21}|^2 \left(1 + \frac{1}{|t|^2}\right) + |S_{32}|^2 = 1 \tag{4.9}$$

$$S_{11}S_{21}^* + S_{21}S_{22}^* + S_{31}S_{32}^* = |S_{21}|^2 \left(t + \frac{1}{t^*}\right) + S_{31}S_{32}^* = 0 \tag{4.10}$$

From (4.8) and (4.10) it can be deduced that:

$$|S_{31}| = \sqrt{\frac{1}{1+\alpha}} \tag{4.11}$$

From (4.9) and (4.10) it can be deduced that:

$$|S_{32}| = \sqrt{\frac{\alpha}{1+\alpha}} \tag{4.12}$$

On the other hand:

$$|S_{33}|^2 = 1 - |S_{31}|^2 - |S_{32}|^2 = 0 \tag{4.13}$$

$$|t|^2 = \alpha^2 \left| \frac{S_{31}}{S_{32}} \right|^2 = \alpha \tag{4.14}$$

From (4.8), (4.11) and (4.14) we can write:

$$|S_{21}| = \frac{\sqrt{\alpha}}{1+\alpha} \tag{4.15}$$

As can be seen from (4.11)-(4.15), the amplitudes of the S-parameters are determined by the design goals. If we denote the phase of S_{ij} parameter by θ_{ij}, then we can write the S-parameter matrix as:

$$\begin{bmatrix} -\frac{\alpha}{1+\alpha} e^{j(\theta_{21}+\theta_{31}-\theta_{32})} & \frac{\sqrt{\alpha}}{1+\alpha} e^{j\theta_{21}} & \frac{1}{\sqrt{1+\alpha}} e^{j\theta_{31}} \\ \frac{\sqrt{\alpha}}{1+\alpha} e^{j\theta_{21}} & \frac{-1}{1+\alpha} e^{j(\theta_{21}-\theta_{31}+\theta_{32})} & \sqrt{\frac{\alpha}{1+\alpha}} e^{j\theta_{32}} \\ \frac{1}{\sqrt{1+\alpha}} e^{j\theta_{31}} & \sqrt{\frac{\alpha}{1+\alpha}} e^{j\theta_{32}} & 0 \end{bmatrix} \tag{4.16}$$

In the S-parameter matrix, there are three parameters (θ_{21}, θ_{31} and θ_{32}) which can be used to optimize the amplifier's performance at power back-off. At power back-off, there are two criteria which affect the amplifier's performance. One is the load impedance seen by the main transistor and the other one is the power leakage into the peaking transistor.

At power back-off, port 3 is terminated to its reference impedance, so the load reflection coefficient seen by the main transistor can be calculated as [60, 65]:

$$\Gamma_{in,1,BO} = S_{11} + \frac{S_{21}^2 \Gamma_{t,p,BO}}{1 - \Gamma_{t,p,BO} S_{22}} = \frac{S_{11}}{1 - \Gamma_{t,p,BO} S_{22}} \tag{4.17}$$

In (4.17), $\Gamma_{t,p,BO}$ is the peaking transistor's output reflection coefficient at power back-off where the peaking transistor is turned off. The value of $\Gamma_{t,p,BO}$ is calculated with the reference impedance of port 2. Using (4.16), we can re-write (4.17) as:

$$\Gamma_{in,1,BO} = \frac{-\alpha e^{j(\theta_{21}+\theta_{31}-\theta_{32})}}{(1+\alpha) + |\Gamma_{t,p,BO}| e^{j(\theta_{t,p,BO}+\theta_{21}+\theta_{32}-\theta_{31})}} \tag{4.18}$$

The magnitude of the $\Gamma_{in,1,BO}$ can be calculated as:

$$|\Gamma_{in,1,BO}|^2 = \frac{\alpha^2}{(1+\alpha)^2 + |\Gamma_{t,p,BO}|^2 + 2(1+\alpha)|\Gamma_{t,p,BO}| \cos(\theta_{t,p,BO}+\theta_{21}+\theta_{32}-\theta_{31})} \tag{4.19}$$

From (4.19) it can be seen that $|\Gamma_{in,1,BO}|$ is a function of $\theta_{21} + \theta_{32} - \theta_{31}$. The upper and lower bounds of $|\Gamma_{in,1,BO}|$ can be calculated as:

$$\frac{\alpha}{1 + \alpha + |\Gamma_{t,p,BO}|} \leq |\Gamma_{in,1,BO}| \leq \frac{\alpha}{1 + \alpha - |\Gamma_{t,p,BO}|} \tag{4.20}$$

From (4.19) one can define and calculate ϕ_0 as:

$$\phi_0 = \theta_{t,p,BO} + \theta_{21} + \theta_{32} - \theta_{31} \pm \cos^{-1}\left(\frac{\frac{\alpha^2}{|\Gamma_{in,1,BO}|^2} - (1+\alpha)^2 - |\Gamma_{t,p,BO}|^2}{2(1+\alpha)|\Gamma_{t,p,BO}|}\right) \tag{4.21}$$

From (4.18) we have:

$$\angle\Gamma_{in,1,BO} = \pm\pi + (\theta_{21} + \theta_{31} - \theta_{32}) - \phi_D \tag{4.22}$$

$$\phi_D = \tan^{-1}\left(\frac{|\Gamma_{t,p,BO}|\sin\phi_0}{1 + \alpha + |\Gamma_{t,p,BO}|\cos\phi_0}\right) \tag{4.23}$$

From (4.21) and (4.22), one can deduce:

$$\theta_{21} = \frac{\angle\Gamma_{in,1,BO} + \phi_D + \phi_0 - \theta_{t,p,BO} \pm \pi}{2} \tag{4.24}$$

$$\theta_{31} - \theta_{32} = \frac{\angle\Gamma_{in,1,BO} + \phi_D - \phi_0 - \theta_{t,p,BO} \pm \pi}{2} \tag{4.25}$$

Equation (4.24) shows that to have the desired $\Gamma_{in,1,BO}$, the phase value of θ_{21} should be fixed to a set of specific values based on the signs selected in (4.21) and (4.24). Equation (4.25) shows that the phase difference of $\theta_{31} - \theta_{32}$ should have a set of specific values based on the signs selected in (4.21) and (4.25). The selection of the signs in (4.21) and (4.24) are arbitrary and independent of each-other, but the signs in (4.24) and (4.25) should match with each-other, as a result, generally there are four sets of solutions for the phase values. The desired value of $\Gamma_{in,1,BO}$ should be obtained considering transistor's behavior (load-pull analysis or measurement) and the power leakage into the peaking transistor at power back-off. The procedure of determining optimum $\Gamma_{in,1,BO}$ is presented in the following.

To quantify the power leakage into the peaking transistor, we define the leakage factor, ϵ as the ratio of the power leakage into the peaking transistor to the power delivered to the load:

$$\epsilon = \frac{P_{leak,BO}}{P_{load,BO}} = \frac{|b_2|^2 - |a_2|^2}{|b_3|^3} \tag{4.26}$$

In (4.26), the power waves are considered at back-off power level where the peaking transistor is in off state. Also port 3 is matched to its reference impedance, so there will be no reflection at that port ($a_3 = 0$) and $P_{load,BO} = |b_3|^2$. To calculate power leakage factor from circuit parameters, we can write:

$$b_2 = \frac{S_{21}}{1 - S_{22}\Gamma_{t,p,BO}} a_1 \tag{4.27}$$

$$b_3 = \left(S_{31} + \frac{S_{32}S_{21}\Gamma_{t,p,BO}}{1 - S_{22}\Gamma_{t,p,BO}} \right) a_1 \tag{4.28}$$

Using (4.27) and (4.28), we can re-write (4.26) as:

$$\epsilon = \frac{|S_{21}|^2 \left(1 - |\Gamma_{t,p,BO}|^2\right)}{|S_{31} + \Gamma_{t,p,BO}(S_{32}S_{21} - S_{31}S_{22})|^2} \tag{4.29}$$

Using (4.16) and (4.29), the power leakage factor can be calculated as:

$$\begin{aligned} \epsilon &= \frac{\alpha \left(1 - |\Gamma_{t,p,BO}|^2\right)}{(1+\alpha) \left| e^{j\theta_{31}} + |\Gamma_{t,p,BO}| e^{j(\theta_{t,p,BO} + \theta_{32} + \theta_{21})} \right|^2} \\ &= \frac{\alpha \left(1 - |\Gamma_{t,p,BO}|^2\right)}{(1+\alpha) \left(1 + |\Gamma_{t,p,BO}|^2 + 2|\Gamma_{t,p,BO}| \cos(\phi_0)\right)} \end{aligned} \tag{4.30}$$

Equation (4.30) shows that the value of leakage factor is also a function of ϕ_0. Using (4.30), one can obtain the upper and lower limits of the leakage factor as follows:

$$\frac{\alpha(1 - |\Gamma_{t,p,BO}|)}{(1+\alpha)(1 + |\Gamma_{t,p,BO}|)} \leq \epsilon \leq \frac{\alpha(1 + |\Gamma_{t,p,BO}|)}{(1+\alpha)(1 - |\Gamma_{t,p,BO}|)} \tag{4.31}$$

The procedure of obtaining optimum $\Gamma_{in,1,BO}$ for certain back-off power is as follows:

1- The main transistor's DC power consumption and output power can be obtained in $\Gamma_{in,1,BO}$ plane by load pull simulation or measurement of the main transistor at the desired power back-off level.

2- The leakage factor values can also be obtained in $\Gamma_{in,1,BO}$ plane using (4.30) and (4.21).

3- Using (4.26), the power delivered to the load can be calculated as:

$$P_{load,BO} = P_{out,main,BO} - P_{leak,BO} = \frac{P_{out,main,BO}}{1+\epsilon} \tag{4.32}$$

By using the values obtained in step 1 and 2, the values of the power delivered to the load can be obtained in $\Gamma_{in,1,BO}$ plane using (4.32).

4- From the load power values obtained in step 3 and the DC power consumption obtained in step 1, the values of efficiency can be obtained in $\Gamma_{in,1,BO}$ plane.

5- By plotting the efficiency contours obtained in step 4, and the limits of $|\Gamma_{in,1,BO}|$ given in (4.20), one can find the optimum load impedance for the main transistor.

Using the optimum $\Gamma_{in,1,BO}$ found in this procedure, one can calculate the values of θ_{21} and $\theta_{31} - \theta_{32}$ using (4.24) and (4.25). There are still two degrees of freedom in the design (there are maximum of 4 possible values for θ_{21} and also there is no limitation on the value of θ_{31}) which can be used by the designer to obtain a realizable network, minimize the losses or reduce the network's sensitivity to element tolerances in the final network. In step 5 of the characterization process, the limits of the $|\Gamma_{in,1,BO}|$ should be plotted along with the efficiency contours on Smith chart. The value of $\Gamma_{in,1,BO}$ is calculated with $Z^*_{opt,m,P}$ as the reference impedance, but the Smith chart is defined only for real valued reference impedances [65]. The limits of (4.20) should be transformed to the $\Gamma_{in,1,BO}$ plane with a real-valued reference impedance. We denote $\Gamma_{in,1,BO,50}$ as the input reflection coefficient from port 1 with the standard 50 Ω reference impedance.

The transformation from Γ_1 plane with reference impedance of Z_{r1} to Γ_2 plane with reference impedance of Z_{r2} is possible through the following equation [60]:

$$\Gamma_2 = \frac{(Z_{r1} + Z^*_{r2})\Gamma_1 + (Z^*_{r1} - Z^*_{r2})}{(Z_{r1} - Z_{r2})\Gamma_1 + (Z^*_{r1} + Z_{r2})} \tag{4.33}$$

Equation (4.33) is a bilinear transformation from Γ_1 to Γ_2 plane. Equation (4.20) shows that $\Gamma_{in,1,BO}$ can be located between two circles centered at the origin of $\Gamma_{in,1,BO}$ plane.

These circles will be transformed to two circles in $\Gamma_{in,1,BO,50}$ plane. The center and radius of the limit circles in $\Gamma_{in,1,BO,50}$ plane can be obtained using the procedure given in Appendix B. By drawing these two circles in $\Gamma_{in,1,BO,50}$ plane along with the efficiency contours, the optimum load impedance for the main transistor at power back-off can be found.

4.3 Three-Port Input Network Design

The three-port input matching/divider network (IMDN) proposed here is a non-isolated, non-symmetrical power divider that also matches any arbitrary complex-valued source impedance to the input impedances of the two transistors. The IMDN also provides an arbitrary phase difference between the two transistors; As a result there is no need to use offset lines at the input of the amplifiers. In the analysis it is shown that by proper selection of the IMDN parameters, the amplifier's performance can be optimized by utilizing the nonlinear behavior of the transistor input impedances. The ability of designing for any arbitrary complex source impedance is important when the amplifier is fed by a driver stage. In this case there is no need to match both power amplifier and the driver to intermediate common impedance, minimizing circuit size and the number of circuit elements.

In Doherty amplifier, an isolated power divider is used to divide the input power between the two branches. To adjust the signal phase between the two branches, usually an offset line is used at the input of the peaking branch. In addition to the power divider and offset line, input matching networks are used at the input of each amplifier branch.

In the proposed amplifier, the three-port IMDN is a non-symmetrical, non-isolated power divider with arbitrary power division ratio. It also converts the arbitrary, real or complex valued source impedance to the optimum source impedances needed by the two transistors. We define the design goals for the IMDN as follows:

1- IMDN is a lossless, passive and reciprocal network.

2- At peak power, the input power to the two transistors can have any predefined arbitrary

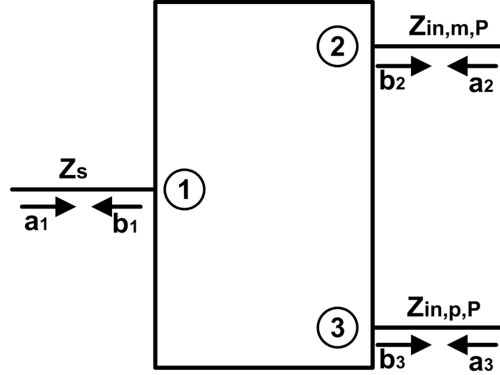


Figure 4.3: Three-port input matching/dividing network and the port reference impedances.

ratio.

3- IMDN should present optimum source impedance for maximum power transfer to both transistors. The two optimum source impedances can be any complex-valued impedances inside the Smith chart. Also at peak power all the input power should be delivered to the transistors without reflection.

4- The amplifier's source impedance can be any arbitrary real-valued or complex-valued impedance inside Smith chart.

5- At peak power, the phase difference between the two input signals to the two transistors should have a predefined (arbitrary) value for proper combining at the output.

To obtain the S-parameters for the IMDN, a set of reference impedances should be selected. Fig. 4.3 shows the IMDN with its ports numbered from 1 to 3 and the reference impedance for each port. Port 1 is the port that connects to the source impedance. The reference impedance for port 1 is Z_S that is the arbitrary real-valued or complex-valued source impedance. Port 2 connects to the input port of the main (class AB or class B biased) transistor. The reference impedance for port 2 is $Z_{in,m,P}$ that is the main transistor's large signal input impedance at peak input power. Port 3 connects to the peaking (class C biased) transistor's input port. The reference impedance for port 3 is $Z_{in,p,P}$ that is the peaking transistor's large signal input impedance at peak input power. From design goals 2 and 5, at peak input power the input signals to the two transistors may have different

amplitudes and phases. As a result we can define S_0, γ and θ_0 as follows:

$$\frac{b_3}{b_2} = S_0 = \gamma e^{j\theta_0} \tag{4.34}$$

Equation (4.34) means the input signals to the two transistors have a phase difference of θ_0 and the ratio of the input powers is γ^2.

At peak power, the large signal input impedances of the two transistors are equal to the reference impedances at ports 2 and 3. This means that the loads at ports 2 and 3 have no reflection and we will have:

$$b_2 = S_{21} a_1 \qquad , \qquad b_3 = S_{31} a_1 \tag{4.35}$$

From (4.34) and (4.35) we have:

$$\frac{b_3}{b_2} = \frac{S_{31}}{S_{21}} = S_0 \tag{4.36}$$

From (4.36) and the no reflection condition for port 1, the S-parameter matrix can be written as:

$$\begin{bmatrix} 0 & S_{21} & S_0 S_{21} \\ S_{21} & S_{22} & S_{32} \\ S_0 S_{21} & S_{32} & S_{33} \end{bmatrix} \tag{4.37}$$

The losslessness condition gives:

$$|S_{21}|^2 + |S_0 S_{21}|^2 = 1 \qquad \rightarrow \qquad |S_{21}| = \frac{1}{\sqrt{1+\gamma^2}} \tag{4.38}$$

We can also write:

$$S_{22} S_{21}^* + S_{32} S_0^* S_{21}^* = 0 \qquad \rightarrow \qquad S_{22} = -S_{32} S_0^* \tag{4.39}$$

$$S_{32} S_{21}^* + S_{33} S_0^* S_{21}^* = 0 \qquad \rightarrow \qquad S_{32} = -S_{33} S_0^* \tag{4.40}$$

$$|S_{32}|^2 + |S_{33}|^2 + \frac{\gamma^2}{1+\gamma^2} = 1 \qquad \rightarrow \qquad |S_{33}| = \frac{1}{1+\gamma^2} \tag{4.41}$$

Using (4.34) and (4.37)-(4.39), we can re-write (4.36) as:

$$\begin{bmatrix} 0 & \dfrac{e^{j\theta_{21}}}{\sqrt{1+\gamma^2}} & \dfrac{\gamma e^{j(\theta_{21}+\theta_0)}}{\sqrt{1+\gamma^2}} \\ \dfrac{e^{j\theta_{21}}}{\sqrt{1+\gamma^2}} & \dfrac{\gamma^2 e^{j(\theta_{33}-2\theta_0)}}{1+\gamma^2} & \dfrac{-\gamma e^{j(\theta_{33}-\theta_0)}}{1+\gamma^2} \\ \dfrac{\gamma e^{j(\theta_{21}+\theta_0)}}{\sqrt{1+\gamma^2}} & \dfrac{-\gamma e^{j(\theta_{33}-\theta_0)}}{1+\gamma^2} & \dfrac{e^{j\theta_{33}}}{1+\gamma^2} \end{bmatrix} \tag{4.42}$$

In (4.42), θ_{21} and θ_{33} are phases of S_{21} and S_{31} respectively. These two parameters are the degrees of freedom that can be used to adjust the performance of the IMDN at power back-off for linearity or higher gain at power back-off. The input impedances of the transistors are usually dependent on the input power [29, 30]. This nonlinear input impedance can be used to adjust the amplifier's performance at power back-off. Suppose that the input reflection coefficients of the main and peaking transistors at power back-off are $\Gamma_{in,m,BO}$ and $\Gamma_{in,p,BO}$ respectively (with reference impedances given in Fig. 4.3). Then at power back-off we will have:

$$a_2 = b_2\Gamma_{in,m,BO} \quad , \quad a_3 = b_3\Gamma_{in,p,BO} \tag{4.43}$$

$$\begin{bmatrix} S_{22}\Gamma_{in,m,BO} - 1 & S_{32}\Gamma_{in,p,BO} \\ S_{32}\Gamma_{in,m,BO} & S_{33}\Gamma_{in,p,BO} - 1 \end{bmatrix} \begin{bmatrix} b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} -S_{21} \\ -S_{31} \end{bmatrix} a_1 \tag{4.44}$$

Equation (4.44) can be re-written as:

$$\begin{bmatrix} b_2 \\ b_3 \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} 1 - S_{33}\Gamma_{in,p,BO} & S_{32}\Gamma_{in,p,BO} \\ S_{32}\Gamma_{in,m,BO} & 1 - S_{22}\Gamma_{in,m,BO} \end{bmatrix} \begin{bmatrix} S_{21} \\ S_{31} \end{bmatrix} a_1 \tag{4.45}$$

$$\Delta = 1 - S_{33}\Gamma_{in,p,BO} - S_{22}\Gamma_{in,m,BO}$$

Using (4.45) and (4.42), the ratio of powers delivered to the two transistors at power back-off can be calculated as:

$$\left|\frac{b_2}{b_3}\right|^2 = \frac{1}{\gamma^2}\left|\frac{e^{-j\theta_{33}} - \Gamma_{in,p,BO}}{e^{-j\theta_{33}} - \Gamma_{in,m,BO}e^{-j2\theta_0}}\right|^2 \tag{4.46}$$

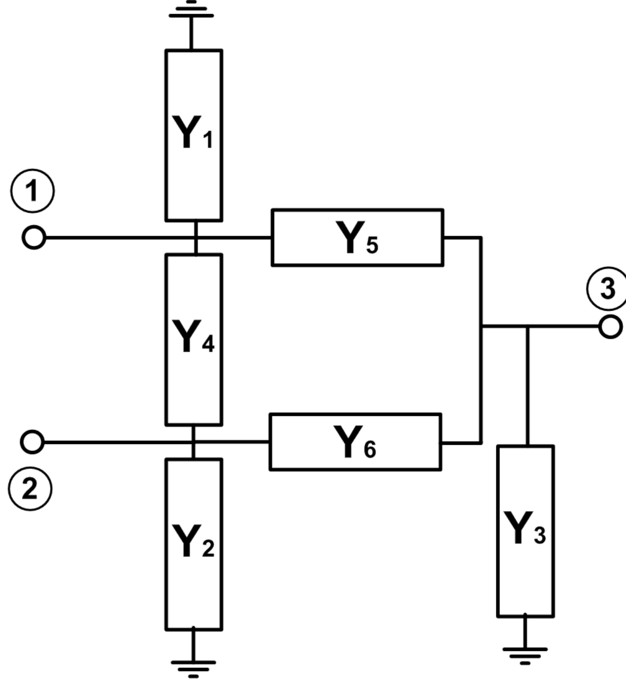


Figure 4.4: Six-element three-port network.

Equation (4.46) shows that the division ratio can be controlled by the parameter θ_{33}. The range of division ratios in back-off is determined by the transistor's nonlinear input behavior (the values of $\Gamma_{in,m,BO}$ and $\Gamma_{in,p,BO}$). From (4.42) it can be seen that there is no constraints on the value of θ_{21}. The parameter θ_{21} can be used by the designer as a degree of freedom for realizability, decreased loss, lower sensitivity to element tolerances or other purposes.

4.4 Three-Port Network Synthesis

In the previous subsections, the OMCN and IMDN were characterized by their three-port S-parameter matrices. After finding the parameters of the three-port networks, they should be realized using circuit elements. The three-port networks can be realized using different circuit structures. Here we present one possible implementation of the three-port networks. This network utilizes maximum of 6 circuit elements which results in compact layout for the final amplifier. This three-port network is shown in Fig. 4.4. In this circuit, the elements Y_4, Y_5 and Y_6 are considered to be lumped elements whereas the Y_1, Y_2 and Y_3 elements can

be either lumped or distributed elements. The admittance matrix of this network can be written as:

$$\mathbf{Y} = \begin{bmatrix} Y_1 + Y_4 + Y_5 & -Y_4 & -Y_5 \\ -Y_4 & Y_2 + Y_4 + Y_6 & -Y_6 \\ -Y_5 & -Y_6 & Y_3 + Y_5 + Y_6 \end{bmatrix} \tag{4.47}$$

The elements of the matching network can be obtained using the Y parameters as:

$$\begin{gathered} Y_1 = y_{11} + y_{12} + y_{13} \quad , \quad Y_2 = y_{21} + y_{22} + y_{32} \quad , \quad Y_3 = y_{31} + y_{32} + y_{33} \\ Y_4 = -y_{11} \quad , \quad Y_5 = -y_{31} \quad , \quad Y_6 = -y_{32} \end{gathered} \tag{4.48}$$

The S-parameter matrices (4.16) and (4.42) can be converted to the Y-parameter matrix [60] and the values of circuit elements can be calculated accordingly. As stated above, there is no limitation on the value of θ_{31} for OMCN and the value of θ_{21} for IMDN. These values can be swept and for each value of these parameters, the elements of the matching network can be obtained. Among the obtained networks, the designer can select the most desired network considering realizability, loss, lower sensitivity to element tolerances or other design criteria.

4.5 Experimental Validation

To verify the analysis shown above, two Doherty amplifiers are designed using the proposed amplifier structure. The first amplifier is designed for 50 Ω source and load impedance and the second amplifier is designed for complex source and load impedances to show the applicability of the proposed amplifier for complex terminations. The transistor used for both amplifiers is the CGH4006P, 6 watt GaN transistor from Cree. The design frequency for both amplifiers was 1 GHz. In both designs, the main transistor was biased at the drain voltage of 28 V and the drain current of 100 mA and the peaking transistor was biased at drain voltage of 28 V and gate voltage of -5.6 V.

Using load-pull and source-pull simulations, the optimum load and source impedances

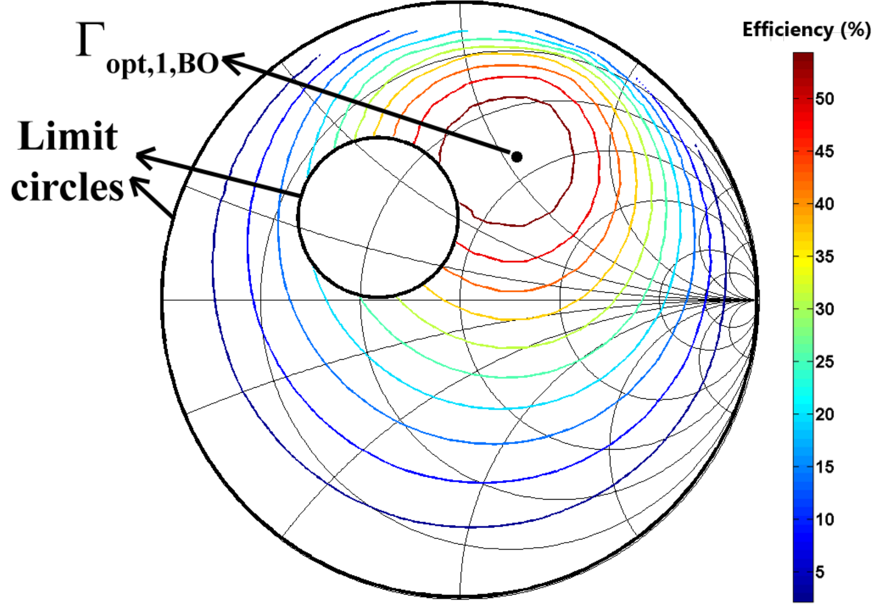


Figure 4.5: Back-off efficiency contours and limit circles in $\Gamma_{in,1,BO,50}$ plane.

for each transistor was obtained. At peak input power, the optimum load impedances for maximum output power were $Z_{opt,m,P} = 23 + j17\ \Omega$ and $Z_{opt,p,P} = 19 + j25\ \Omega$ for main and peaking transistor respectively. The maximum output powers were 40.3 dBm and 39.8 dBm from the main and peaking transistor respectively which means $\alpha = 0.94$ for both designs. The peaking transistor's small signal output impedance was $Z_{t.p.BO} = 1 - j130\ \Omega$. At peak power, equal power splitting ($\gamma = 1$) was selected at the input. The main transistor's large signal input impedances at peak power and power back-off was found as: $Z_{in,m,P} = 12 - j19\ \Omega$, and $Z_{in,m,BO} = 7.7 - j14\ \Omega$ respectively. For the peaking transistor, the large signal input impedances was found as: $Z_{in,p,P} = 6 - j32\ \Omega$, and $Z_{in,p,BO} = 11 - j43\ \Omega$ at peak power and power back-off respectively.

4.5.1 Amplifier 1, 50 Ω Source/Load Impedances

The first amplifier was designed for 50 Ω source and load impedances. Using the 5-step procedure given in Section 4.2, the back-off efficiency contours are plotted in Fig. 4.5 along with the limits of $|\Gamma_{in,1,BO,50}|$. Using the value of obtained optimum impedance at power

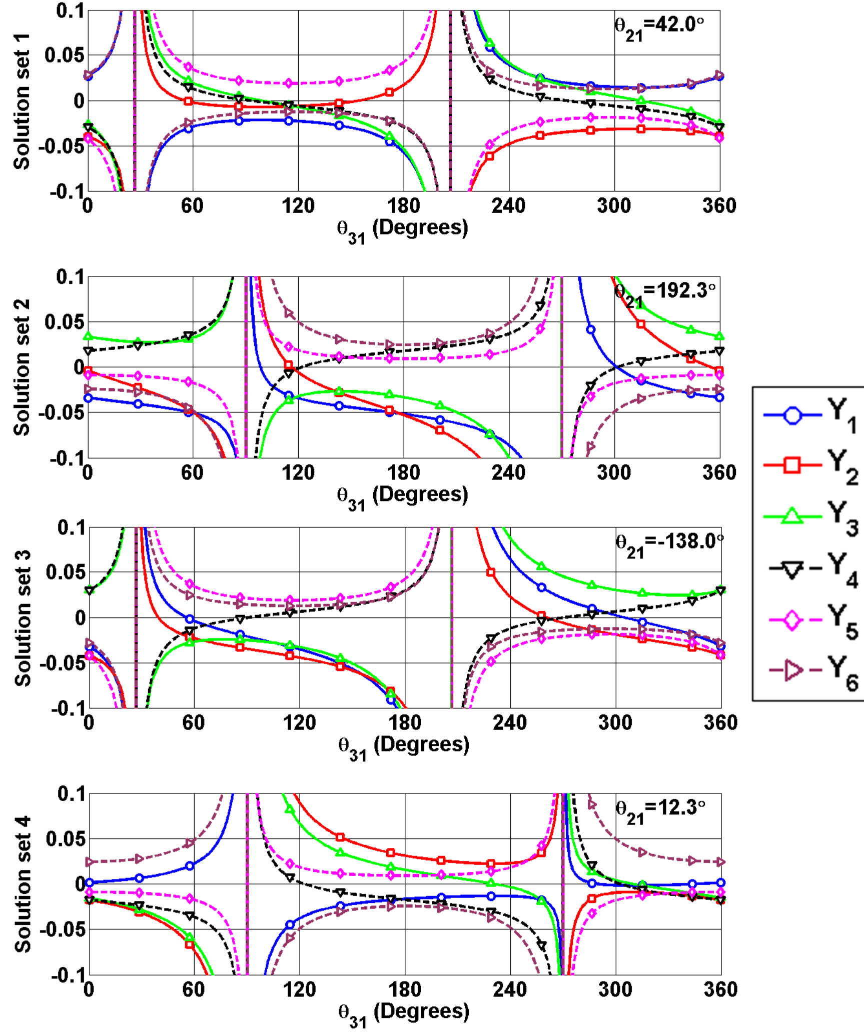


Figure 4.6: Possible solutions for designing amplifier1 OMCN using the circuit of Fig. 4.4.

back-off, the values of θ_{21} and $\theta_{31} - \theta_{32}$ can be obtained using (4.24) and (4.25). There are four values obtained for θ_{21}. Using these four values and by sweeping θ_{31} we can obtain the admittance values Y_1 to Y_6 shown in Fig. 4.4. These sets of solutions are plotted in Fig. 4.6. In our design, we select $\theta_{21} = 192.3°$ and $\theta_{31} = 320°$. Using these values, the drain bias for both amplifiers can be supplied through the OMCN, the values of elements are reasonable, and the OMCN has low sensitivity to the element value tolerances.

To design the IMDN, the required phase difference was simulated to be $\theta_0 = 89°$ using the obtained OMCN. To obtain the value of θ_{33}, the value of power splitting factor at power back-off is plotted in Fig. 4.7. The value of $\theta_{33} = 200°$ is selected for better linearity

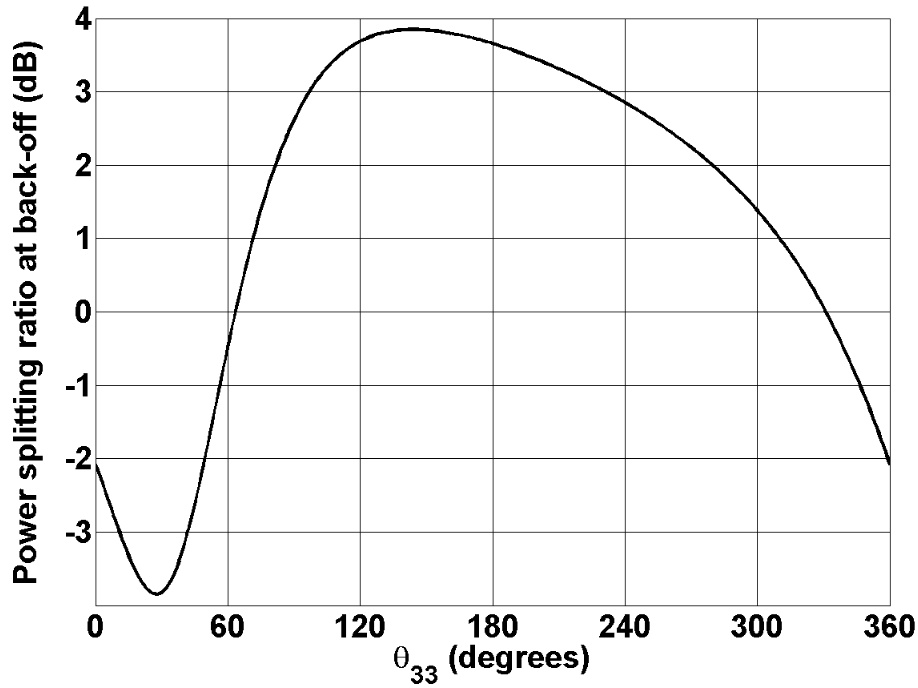


Figure 4.7: The ratio of the main transistor's input power to the peaking transistor's input power at power back-off versus θ_{33} in IMDN.

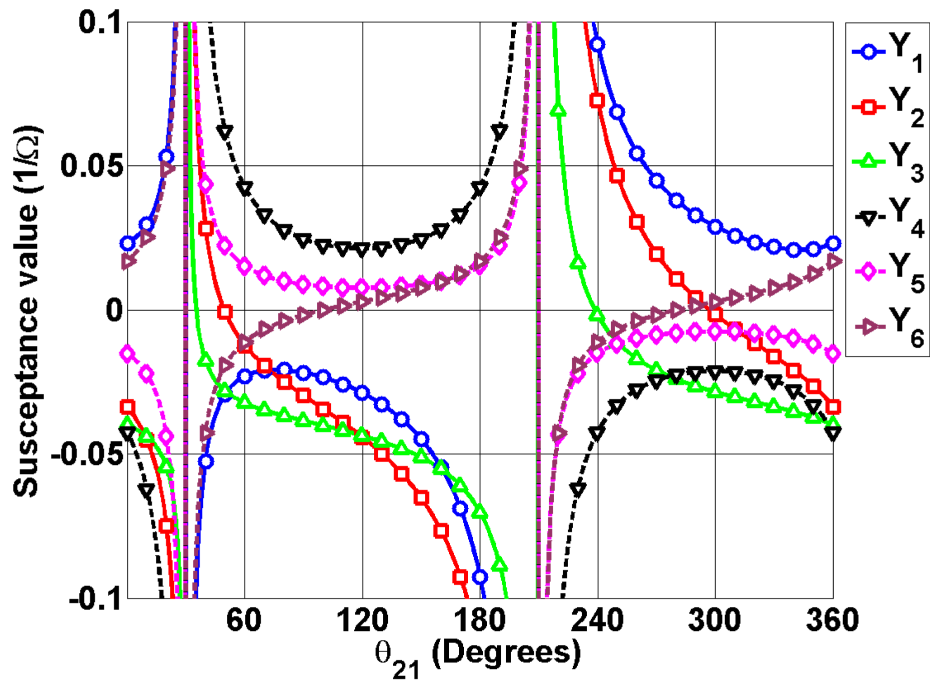


Figure 4.8: Possible solutions for designing amplifier1 IMDN using the circuit of Fig. 4.4.

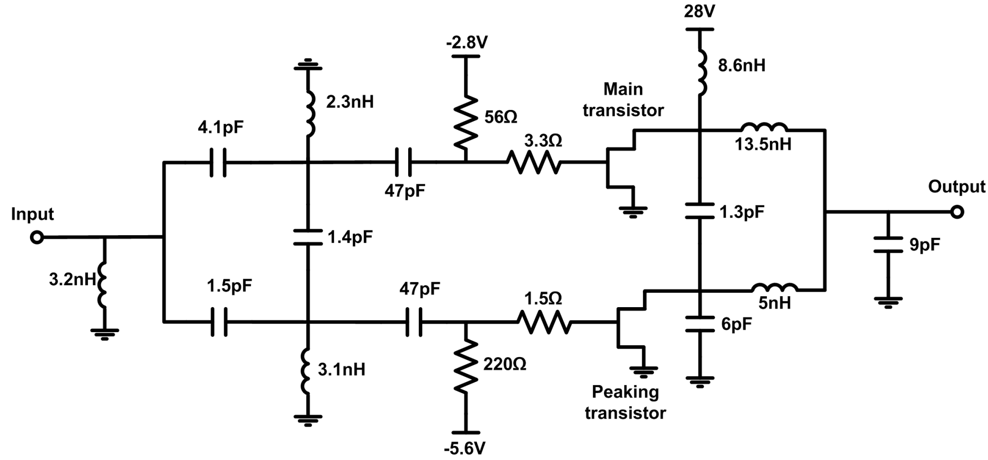


Figure 4.9: Schematic of the Amplifier 1 designed for 50 Ω source and load impedances.

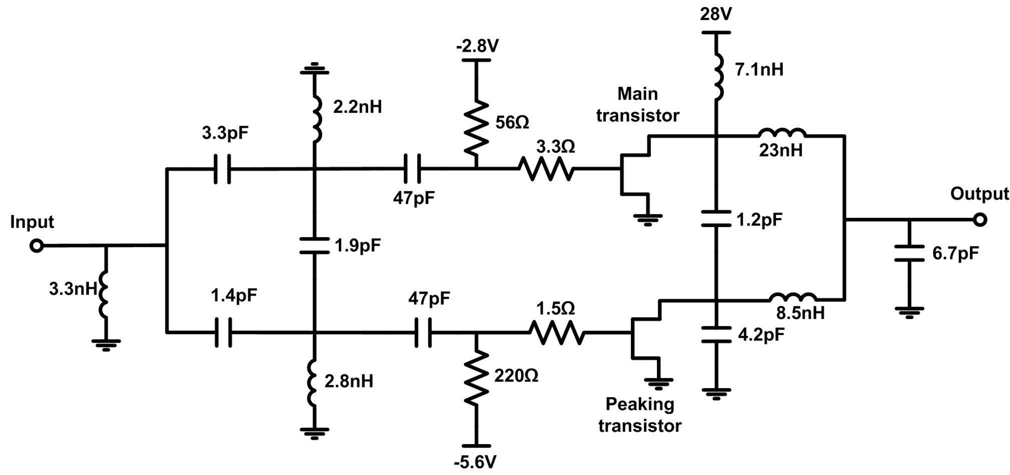
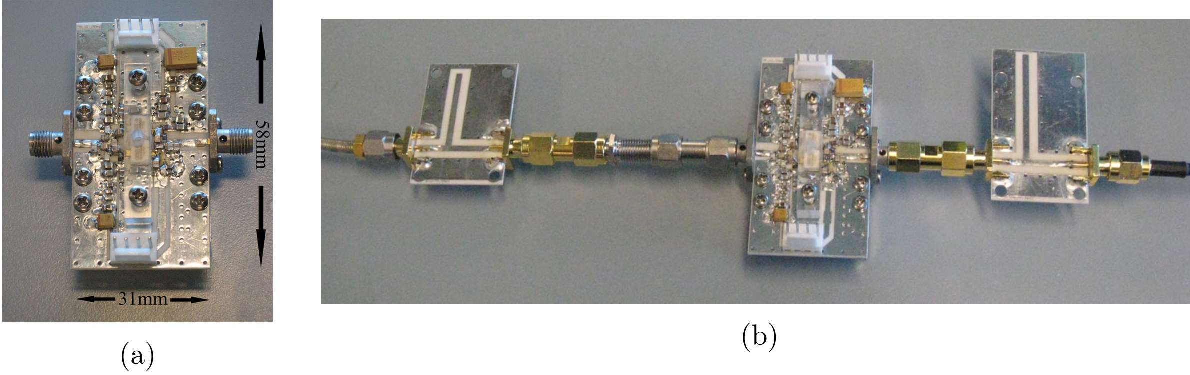


Figure 4.10: Schematic of the Amplifier 2 designed for source impedance of $Z_S = 48.2 - j44\ \Omega$ and load impedance of $Z_L = 35.7 + j66.9\ \Omega$.

performance and higher gain at power back-off. After selecting θ_{33}, the values of admittance values Y_1 to Y_6 are plotted versus θ_{21} in Fig. 4.8. To obtain a network with reasonable element values, $\theta_{21} = 155°$ was selected for the amplifier. The final amplifier's schematic is shown in Fig. 4.9.

4.5.2 Amplifier 2, Complex Source/Load Impedances

To show the applicability of the designed amplifier for complex source/load impedances, another amplifier was designed for arbitrary source impedance of $Z_S = 48.2 - j44\ \Omega$ and



(a) (b)

Figure 4.11: Photos of the tested amplifiers (a) Amplifier 1, (b) Amplifier 2 with the stubs used for generating the complex source/load impedances.

load impedance of $Z_L = 35.7 + j66.9\ \Omega$. This amplifier was designed using the same procedure as the first amplifier. The final schematic for this amplifier is shown in Fig. 4.10.

4.5.3 Simulation and Measurement Results

The two amplifiers were built and measured using the obtained lumped-element IMDNs and OMCNs. A small change in the element values was necessary to obtain the commercially available and standard element values. For the complex load/source amplifier, the load and source impedances were implemented using detuning stubs and proper transmission line lengths to convert the 50 Ω standard impedance to the complex source and load impedances. The two fabricated amplifiers are shown in Fig. 4.11. Same PCB layout was used for both amplifiers since the IMDN and OMCN for each design have the same topology. The circuit size for both amplifiers was 31 mm × 58 mm. In Fig. 4.11b, the input/output stubs used to generate the complex source/load impedances are also shown.

Due to transistor model inaccuracies, board parasitics and element tolerances, the operating frequency of both amplifiers were shifted to lower frequencies. The operating frequency of amplifier 1 and amplifier 2 were shifted to 950 MHz and 940 MHz respectively.

The power sweep simulation and measurement results using continuous-wave (CW) input signal are shown in Fig. 4.12. There is a small discrepancy between the measurement results of the two amplifiers which comes from the element tolerances and difference between the

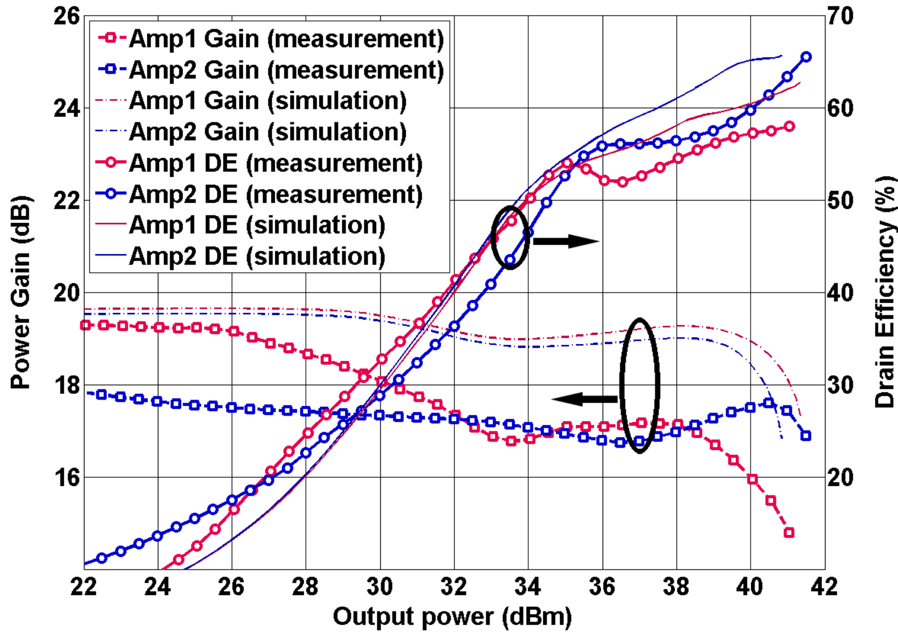


Figure 4.12: Measured gain and efficiency for CW signal.

load impedances at harmonic frequencies presented to the transistors in the two amplifiers. As can be seen from the measurement results, both amplifiers provide higher than 50% efficiency over 7 dB power back-off range.

Both amplifiers were also tested with a modulated LTE signal having 7.2 dB of PAPR and 5 MHz of bandwidth. The power of LTE signal was swept and the values of efficiency and ACPR for both amplifiers were obtained and plotted versus output power in Fig. 4.13. Both amplifiers were linearized using digital pre-distortion (DPD). A memory-polynomial DPD technique with nonlinearity order of 8 and memory depth of 5 was used to linearize the amplifiers [48]. Fig. 4.14 shows the spectrum of the LTE signal before and after linearization. After linearization, amplifier 1 has 33.8 dBm output power, 48% drain efficiency and lower than -50 dBc ACPR. After applying DPD, amplifier 2 has 34.8 dBm output power, 49.4% drain efficiency with lower than -49 dBc ACPR.

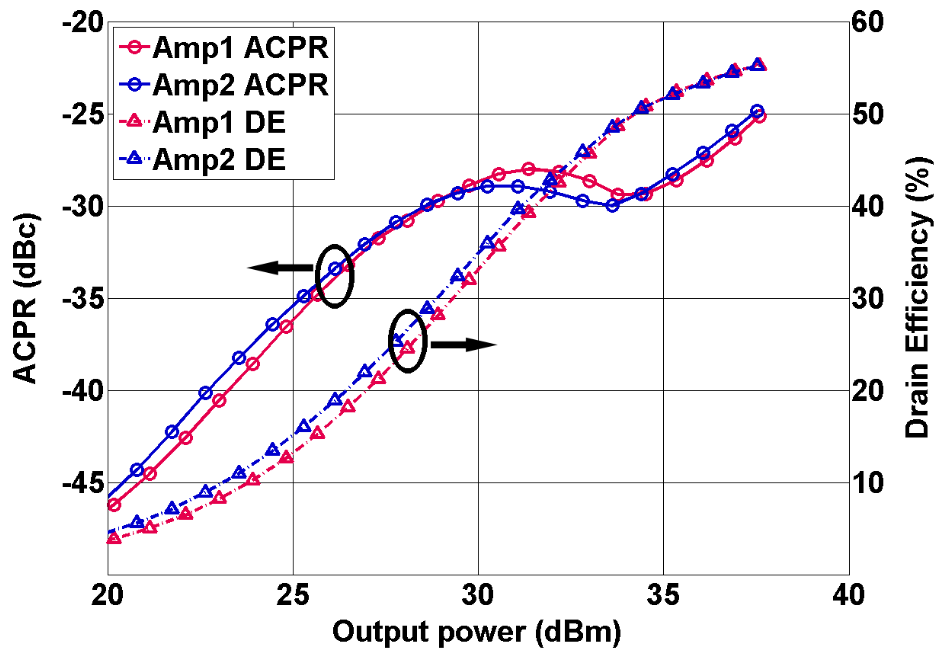


Figure 4.13: Measured efficiency and ACPR versus output power for LTE signal.

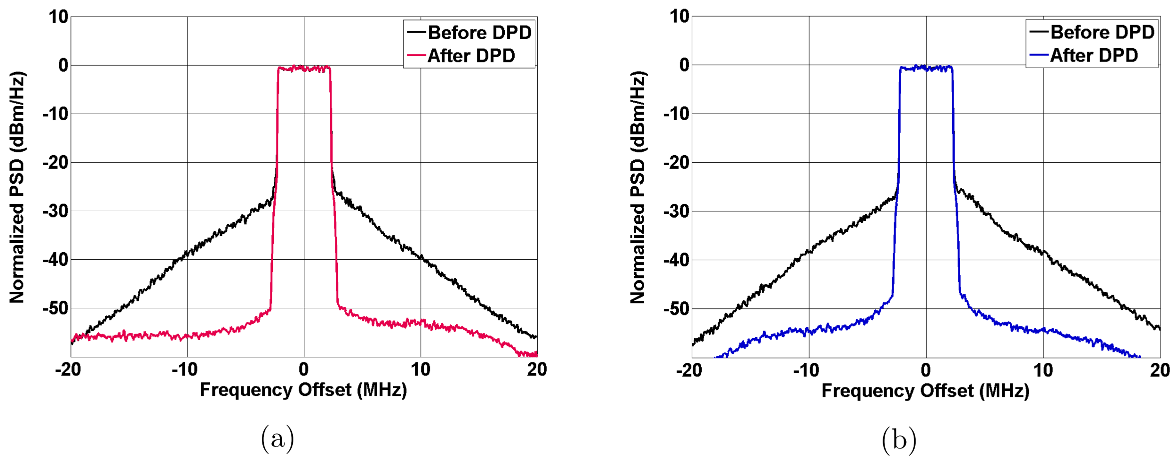


Figure 4.14: Measured output spectra for LTE signal before and after DPD (a) Amplifier 1, (b) Amplifier 2

Chapter 5

Doherty-Like Amplifiers Employing A Current-Biased Amplifier

In Chapter 3 an amplifier structure was proposed that provides high efficiency over large bandwidth. The two-point matching and two-sided/reversed two-sided matching techniques proposed in Chapter 3 can be used to design high efficiency and broadband amplifiers. As it was shown, the S-parameters of output matching networks were fully determined in two-point and two-sided/reversed two-sided matching technique. It means that the matching networks should be designed to provide both amplitude and phase requirements. This puts restrictions on the output matching networks. In this chapter, a new architecture is proposed that has less constraints on the output matching networks. The structure proposed in this chapter has two branches similar to Doherty and TLLM structures, but the main branch utilizes an amplifier that is biased by a constant current source. A current-biased transistor presents completely different behavior compared to a voltage biased transistor, allowing implementation of Doherty-like performance in very large bandwidth (in multiple octaves).

This chapter is organized as follows: In Section 5.1, the idea of biasing a transistor with a constant current source and feasibility of high efficiency current sources is presented. In Section 5.2, a wideband high efficiency amplifier is introduced that uses a current biased transistor and finally in Section 5.3, the measurement results for an amplifier prototype designed based on the proposed architecture are presented.

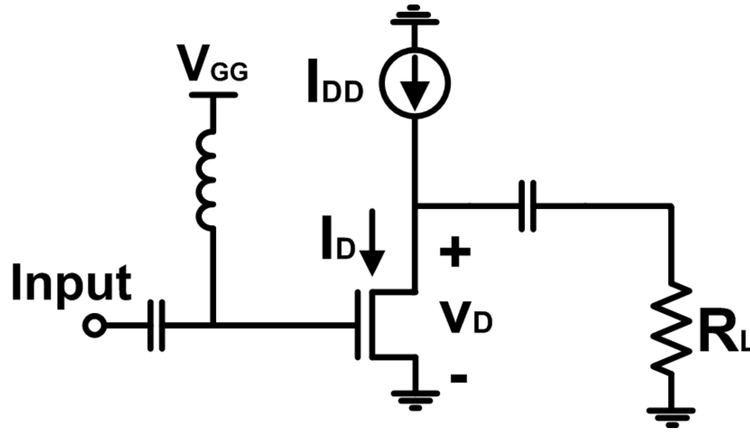


Figure 5.1: Current-biased transistor schematic.

5.1 Current-Biased Transistors

A generic transistor biased by a current source is shown in Fig. 5.1. This type of bias can be used for any type of transistor such as BJT, HBT, FET and other types of transistors. The current biasing can also be used for any semiconductor technology such as GaAs, CMOS, GaN, SiGe, and other technologies. It can also be used for different circuit topologies such as common source (or common emitter), common gate (or common base), cascode and other topologies.

In this type of bias, a constant current DC power supply is connected to the output terminal of the transistor. The input terminal is biased by a constant voltage supply to control the voltage on the output terminal. The I-V characteristics of a typical transistor are shown in Fig. 5.2 along with the characteristic line of the current source. In Fig. 5.2, the blue curves show the transistor's output current versus the transistor's output voltage for different input voltage levels. The horizontal black line is the characteristic current-voltage for the constant current source. It shows that the output current of the current source is fixed, but its voltage can have any values depending on the load connected to it. Depending on the input terminal's DC voltage, the bias point of the transistor falls on the horizontal line shown in he figure. The red dots shown in this figure are some examples of the bias points.

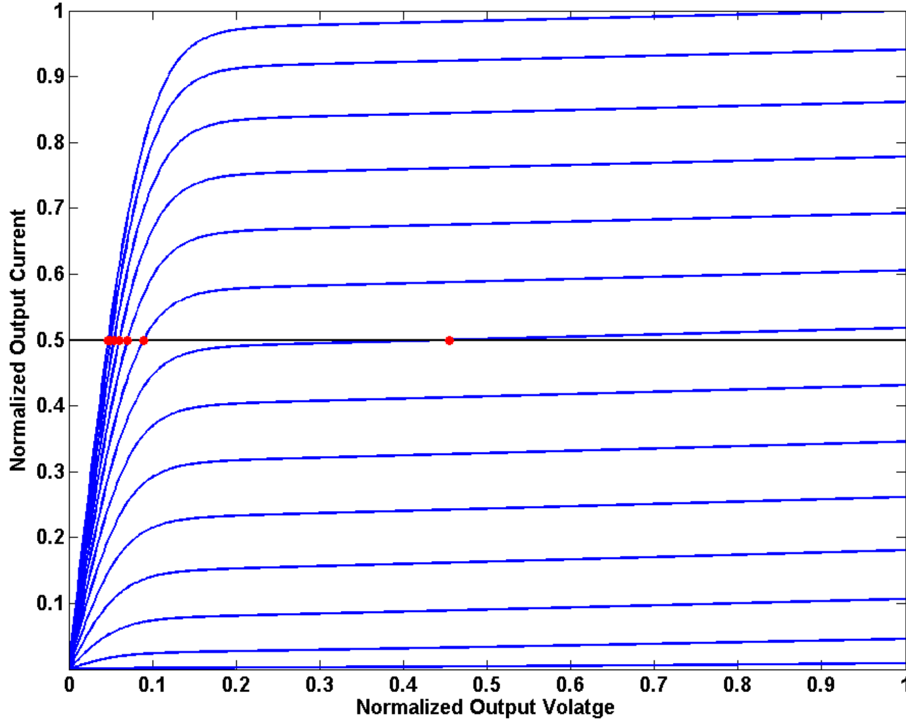


Figure 5.2: Current biased transistor bias points.

A current biased transistor can be biased in different points. Similar to the voltage biased transistors, we can denote the classes of operation for a current-biased transistor based on the transistor's voltage. In Fig. 5.3, the bias points for conventional voltage biased transistors are shown along with the bias points and the classes of operation for a current biased transistor. The classes of operation for the voltage-biased and current biased transistors shown in the figure. Classes A, AB and B are the classes of operation for a voltage biased transistors. The starred notation is used for naming the classes of operation for the current-biased transistors. The naming here is chosen to maintain the similarity between the conventional voltage biasing and the current biasing case. For a current biased transistor, the conduction angle for different classes of operation can be defined in the same way as the voltage biased transistor based on the transistor's current waveform.

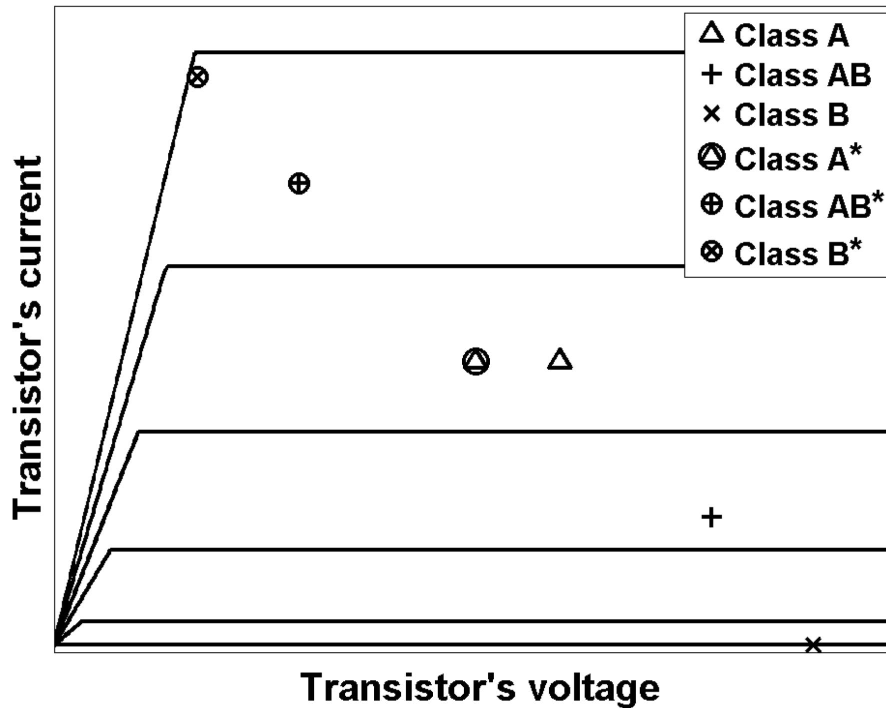


Figure 5.3: Bias points for different classes of operation for voltage and current biasing.

5.1.1 Constant Current Power Supply

For voltage biased transistors, supply circuitry provide the required bias voltage for the transistors. In portable devices where the power is supplied by a battery, there would be no need for DC/DC conversion if the battery voltage is used directly to bias the transistors. However the battery voltage can vary depending on the battery charge status. To avoid the voltage variations due to battery drainage, voltage regulation is needed in most cases which needs DC/DC conversion or voltage regulating circuits. In some cases, the required bias voltage is different from the battery voltage which necessitates the use of DC/DC conversion. In base stations, the required energy is usually supplied by AC power supplies. In this case, AC/DC converters are needed to provide the required bias voltage for the transistors. In most cases DC/DC converters are also needed in base stations to provide different DC voltages needed in different parts of the circuits.

The first question about the current biased transistor is whether implementing a high

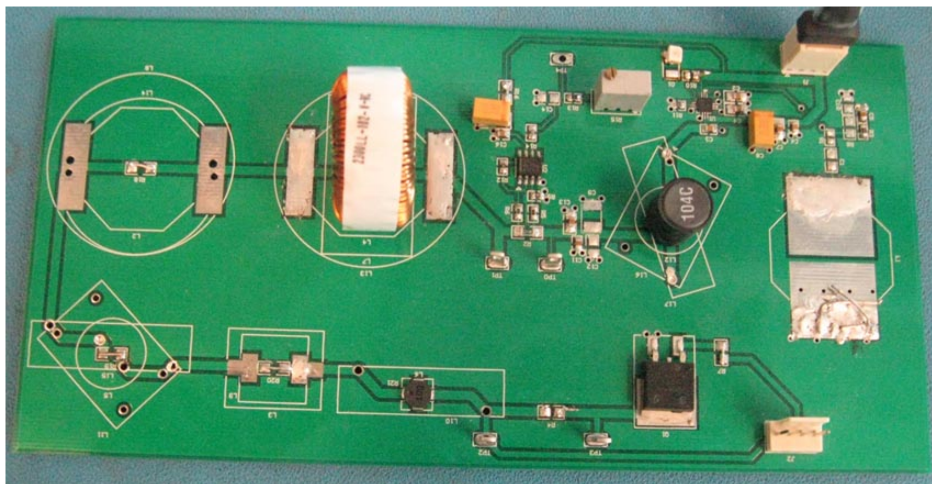


Figure 5.4: PCB photo of the designed constant current source.

efficiency constant current supply is possible. The overall efficiency of the power amplifier depends on both efficiency of the amplifier itself and the efficiency of the supply circuitry. If the supply circuitry has a low energy efficiency, then the overall transmitter system will have low efficiency because of the losses in the power supply.

There are a large number of commercially available parts providing constant current biasing for the lighting systems. Solid-state high brightness LEDs provide high efficiency and have long lifetime and low maintenance costs [79]. LEDs require constant current flow for optimal operation and as a result there are a class of power electronics devices named LED drivers. LED drivers provide constant current needed for the LEDs to operate properly. LED drivers are available in a variety of forms. Some LED drivers convert the AC input voltage to a constant current output and some products convert a DC voltage to the constant output current. The LED driver's efficiency has to be high to avoid degradation of the overall efficiency in lighting systems. Consequently there are a large number of high efficiency constant current LED drivers in the market with efficiencies in the order of 90% and higher. These LED drivers can be used as a constant current source for biasing RF transistors.

To show the feasibility of high efficiency constant current DC sources, a current source was designed as a part of this research. The constant current source was designed using a

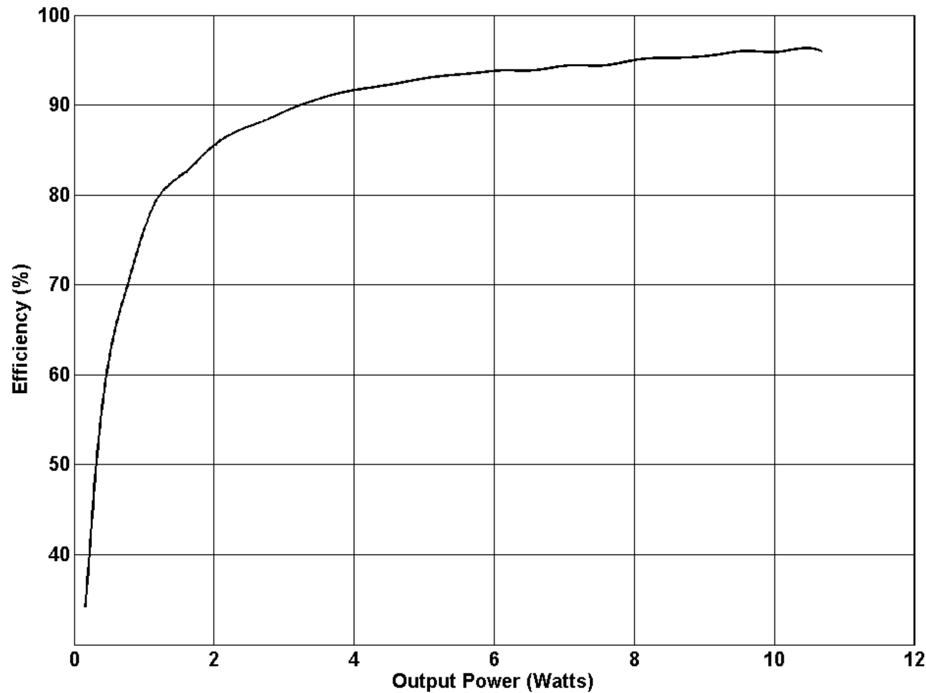


Figure 5.5: Measured efficiency of the designed current source.

high efficiency switching voltage regulator. The switching voltage regulator was configured to work as a constant current source. The designed PCB is shown in Fig. 5.4. The PCB was tested with input voltage of 30 V and output current of 400 mA. The efficiency plot versus output power is shown in Fig. 5.5 for output current of 400 mA. Efficiency of the designed current source is higher than 90 % for voltages higher than 8.1 V which is equivalent to the output power of 3.25 Watts.

5.1.2 Bias Point Stability and Robustness

When biasing the transistors with a current source, unwanted effects may be seen due to tolerances in transistor size and transistor's thermal behavior. Referring to Fig. 5.6a, if the transistor's size is W_1, the voltage across the transistor will be V_{DS1}. If due to manufacturing tolerances and process variations transistor's size decrease, the current handling of transistor decreases. Decreasing the current handling leads to higher voltage on the transistor. Referring to Fig. 5.6a, if the transistor size decreases from W_1 to $0.9W_1$, then the I-V curve for a

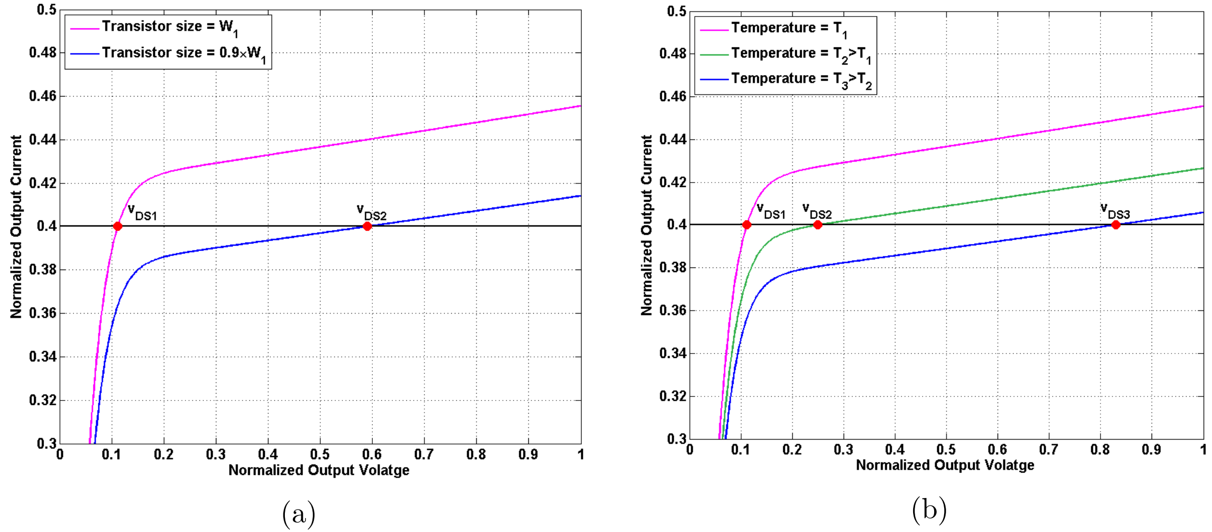


Figure 5.6: Dependence of bias point to (a) transistor size variations, (b) temperature.

constant gate-source voltage will move towards lower currents. In this case, the bias voltage changes from V_{DS1} to V_{DS2}. The change of transistor size may lead to very high bias voltage on the transistor and consequently it may lead to permanent damage to the transistor.

Another phenomenon that may lead to instability of the bias point is the transistor's thermal behavior. When biasing transistors, the DC power consumption on the transistor causes heat generation. Changing transistor's temperature leads to a change in its characteristics. As an example, in GaN transistors, for a fixed gate voltage the drain current decreases by temperature. Referring to Fig. 5.6b, for a fixed gate voltage and fixed drain current, increasing temperature causes an increase in the drain voltage, and consequently higher power dissipation in the transistor. It causes more heat generation and this cycle continues until the drain voltage reaches maximum voltage allowed by the current source. In short, current biasing for a GaN transistor leads to thermal runaway.

In current-biased transistors, the sensitivity of bias point to temperature and transistor size can be decreased by using a feedback in the bias circuit. In a current biased transistor, the drain voltage is controlled by the gate voltage. The variable drain voltage can be used to stabilize the bias point. Fig. 5.7 shows a very simple feedback circuit using two resistors to

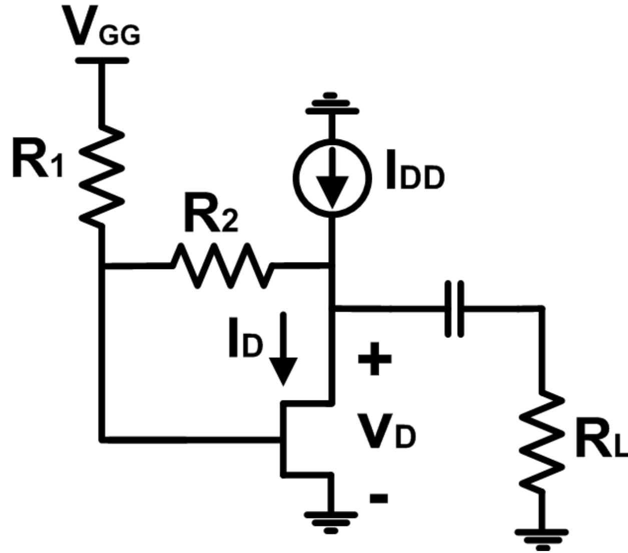


Figure 5.7: Bias feedback for a current-biased transistor.

stabilize the bias point for the current biased transistor. In circuit of Fig. 5.7, when the drain voltage increases, it raises the gate voltage and consequently prevents further increasing of the drain voltage, leading to stabilization of the transistor's bias point.

5.2 Ultra-Wideband High Efficiency Amplifier

As explained in Chapter 2, the Doherty amplifier operates based on load-modulation effect. Referring to Fig. 2.3, for a symmetrical Doherty amplifier the amplifier's load impedance at junction point J changes from R_L at power back-off to $2R_L$ at peak output power. On the other hand, referring to the transistor's load-line (Fig 2.2) at the drain of the main transistor, the load has to change from $2R_{opt}$ at power back-off to R_{opt} at peak output power to keep the transistor in saturation and obtain high efficiency. This means that the load variation required at the transistor's drain is the opposite of the load variations in the junction point. In the junction point, the load increases after the peaking amplifier tuns on, but the required load at drain needs to be decreased for normal operation. The impedance inverter in Doherty structure is used to overcome the difference in the impedance trajectories. The impedance inverter, converts the increasing load impedance at the junction point to a

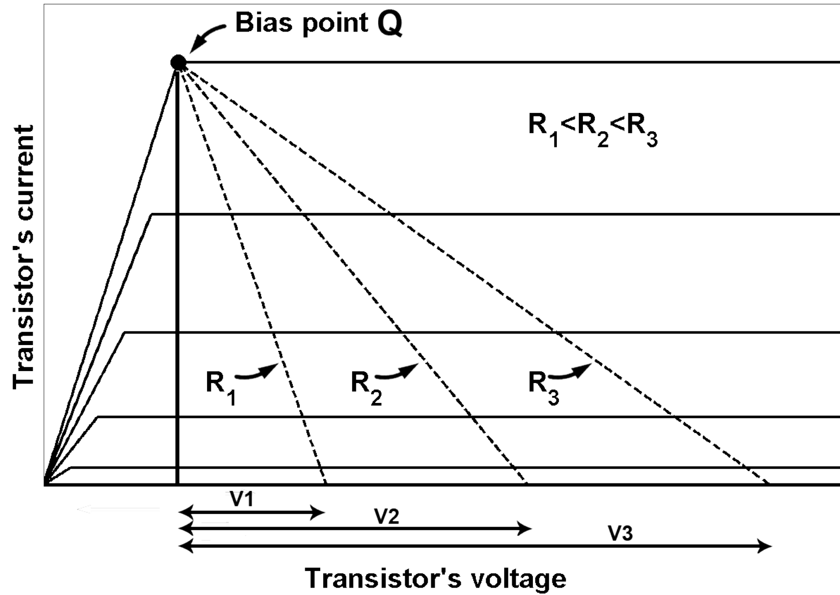


Figure 5.8: Current-biased transistor's load lines.

decreasing impedance at the drain level.

The transistor's bias point can be selected such that it remains in saturation when its load impedance increases. Consider the I-V curves of Fig. 5.8. If the transistor is biased at point Q, then the load-lines of the transistor will be as shown in the figure. For the load impedance of R_k, the maximum voltage swing on the transistor will be V_k. As can be seen from Fig. 5.8, higher load impedances result in larger maximum voltage swing across the transistor, leading to higher output power.

The bias point Q shown in Fig. 5.8 is a point with high bias current and low bias voltage. If a voltage source is used to bias the transistor, then the DC voltage is fixed at the bias voltage. Having a low DC bias voltage means that the transistor cannot provide the maximum voltage swing expected for the load impedance. Current biasing however can be used to bias the transistor at point Q. The DC voltage on a transistor biased with a current source can vary depending on the output voltage waveform.

Similar to the voltage biased transistors, the current biased transistors provide maximum efficiency at maximum output power. Referring to Fig. 5.8, if the load impedance seen by the transistor increases after saturation, the transistor can provide higher output power while

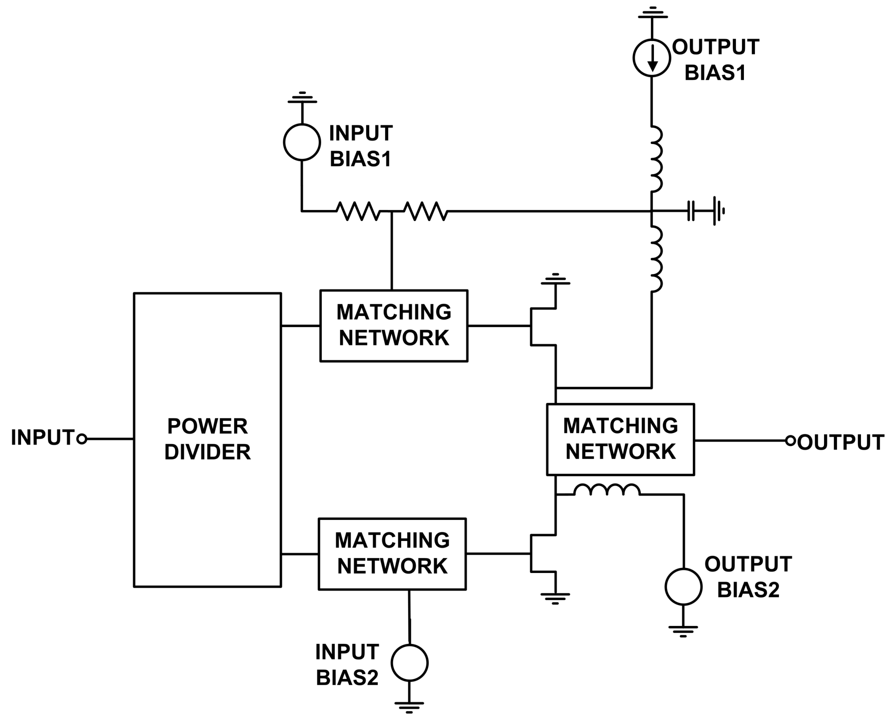


Figure 5.9: Block diagram of the broadband current biased Doherty amplifier.

providing high efficiency. The transistor's load impedance can be changed in the same way as the Doherty amplifier. The current biased class B* amplifier can be used as a main amplifier and a class C biased peaking amplifier can be used to modulate the load impedance seen by the main amplifier. The structure of the current-biased Doherty amplifier is shown in Fig. 5.9. The peaking amplifier turns on after the main amplifier saturates and increases the load impedance seen by the main amplifier, causing it to remain in saturation and provide high efficiency. Since there is no need for impedance inverter, the two amplifier branches can be connected directly together and the amplifier can operate in a large bandwidth. In the next section, a current biased Doherty amplifier and the measurement results are presented providing high efficiency at power back-off and a large frequency bandwidth.

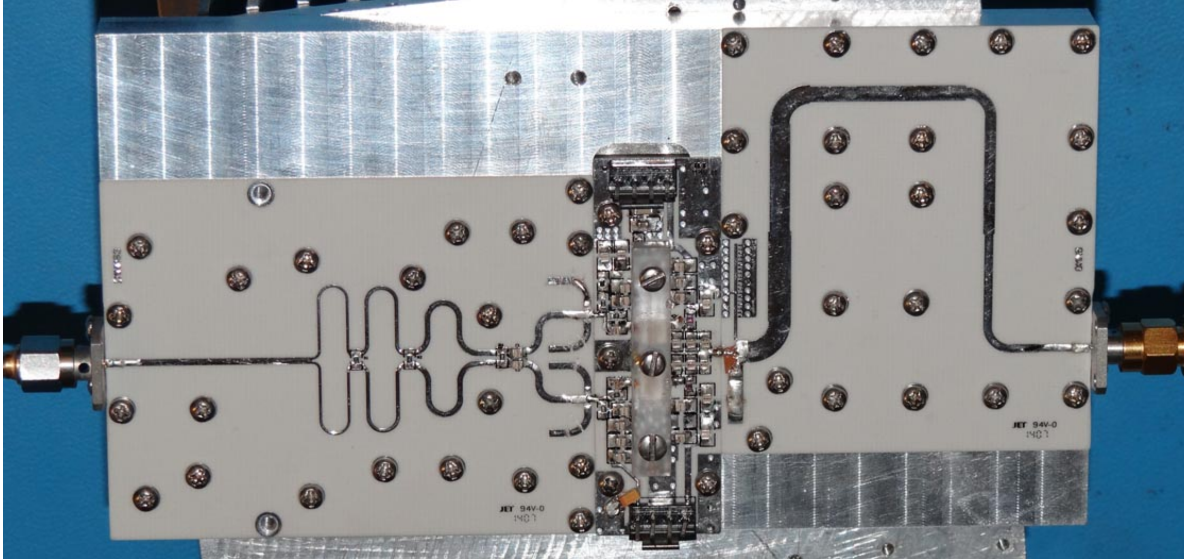
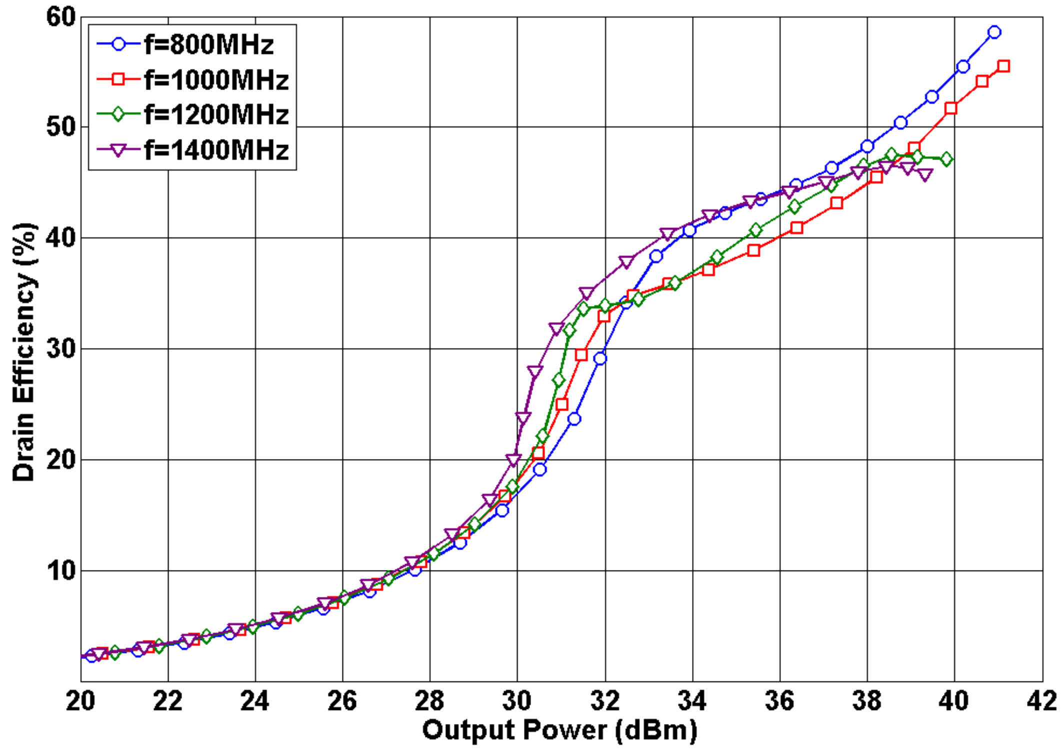


Figure 5.10: Fabricated broadband current biased Doherty amplifier.

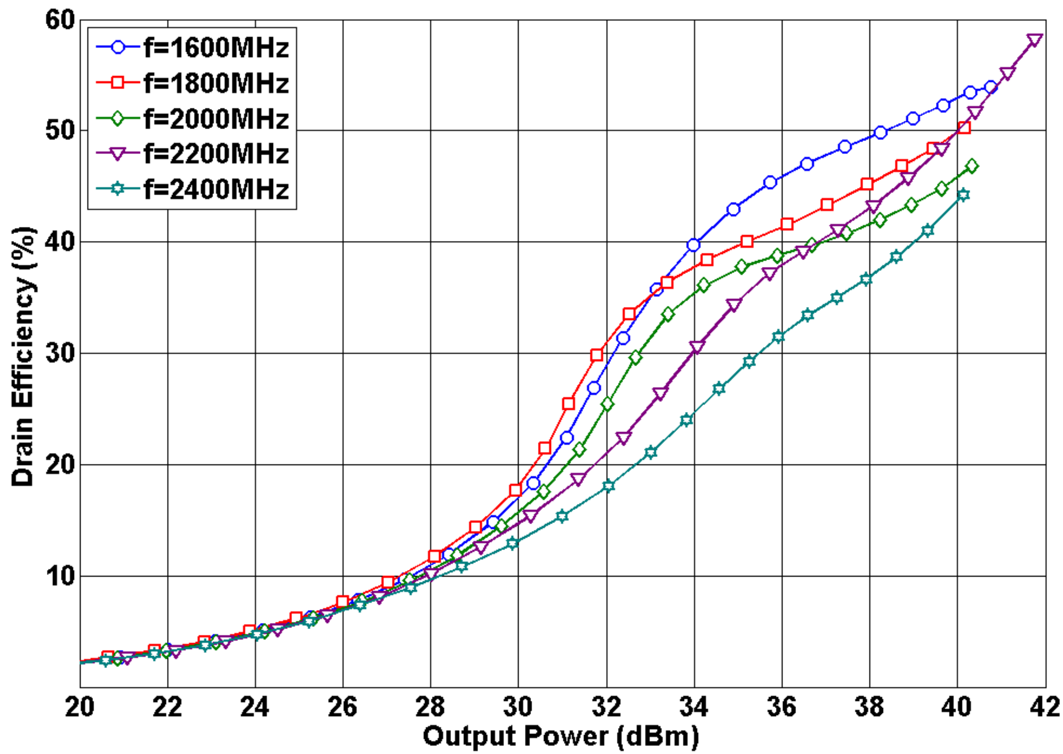
5.3 Experimental Validation

To verify the applicability of the current biased Doherty amplifier, a prototype dual branch amplifier is designed and tested. The main amplifier is designed as a current biased class AB* amplifier and the peaking amplifier is a class C voltage biased amplifier. The transistor used for both amplifiers is the CGH40006P GaN transistor from Cree Inc. The main amplifier is biased in a bias current of 400 mA. The peaking amplifier is biased in drain voltage of 30 V. The amplifier is designed to operate in 0.8-2.5 GHz frequency band. The input power is divided equally between the two branches with a multi-section wideband Wilkinson power divider. The photo of the fabricated amplifier is shown in Fig. 5.10

The results of the CW test are shown in Fig. 5.11 to 5.13. In CW test, the input power to the amplifier is swept and the gain and efficiency are plotted versus output power. In Fig. 5.11, the drain efficiency is shown versus output power for the CW test at different frequencies. As can be seen from this figure, the efficiency remains higher than 35 % for the last 6-8 dB output power back-off range. Fig. 5.12 shows the gain versus output power for the CW test versus output power. The gain has the same behaviour as the Doherty amplifier. At frequencies around 1.2-1.4 GHz, the amplifier presents a drop of around 3 dB

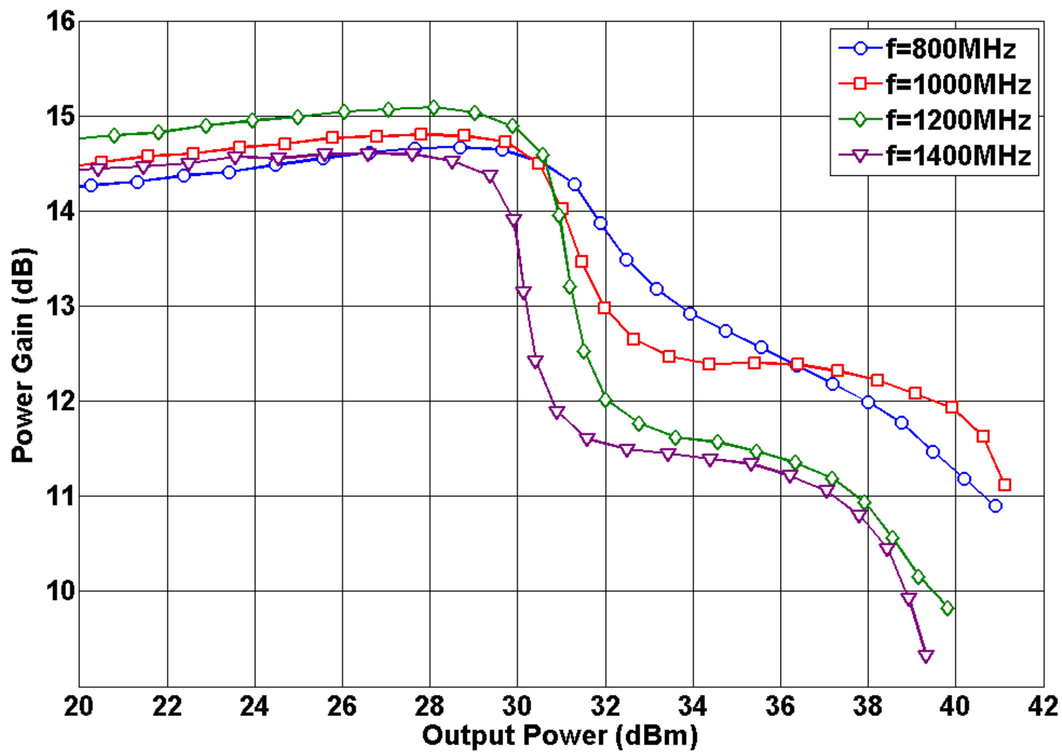


(a)

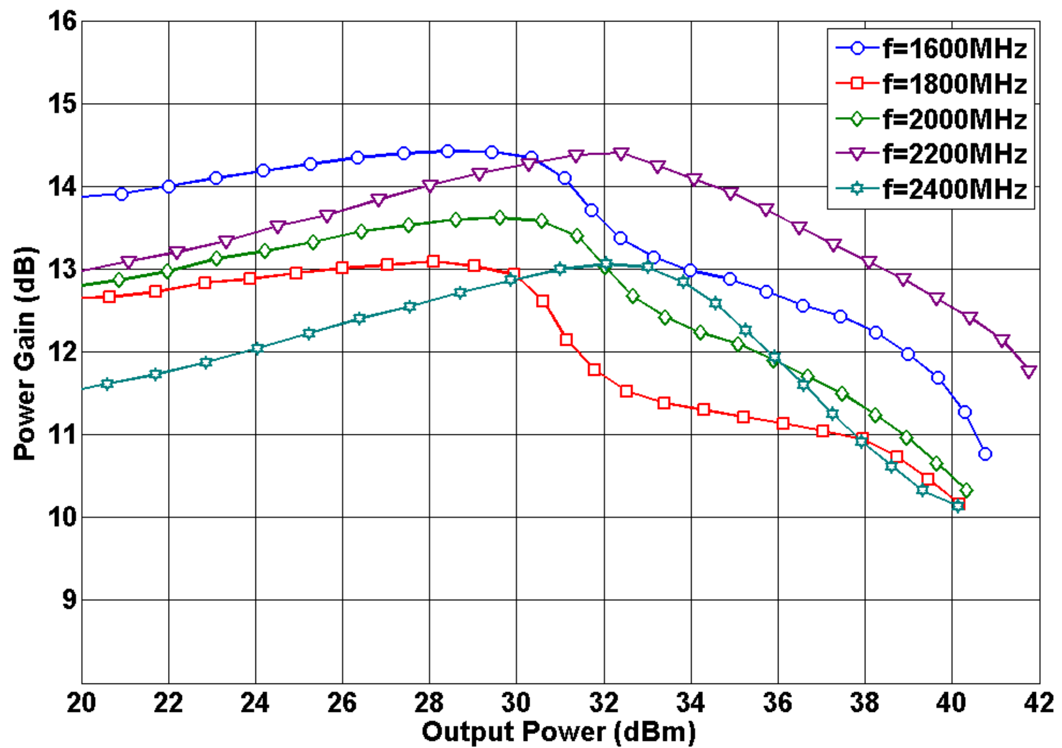


(b)

Figure 5.11: Drain efficiency of the broadband power amplifier (a) lower band (b) upper band.



(a)



(b)

Figure 5.12: Power gain of the broadband power amplifier (a) lower band (b) upper band.

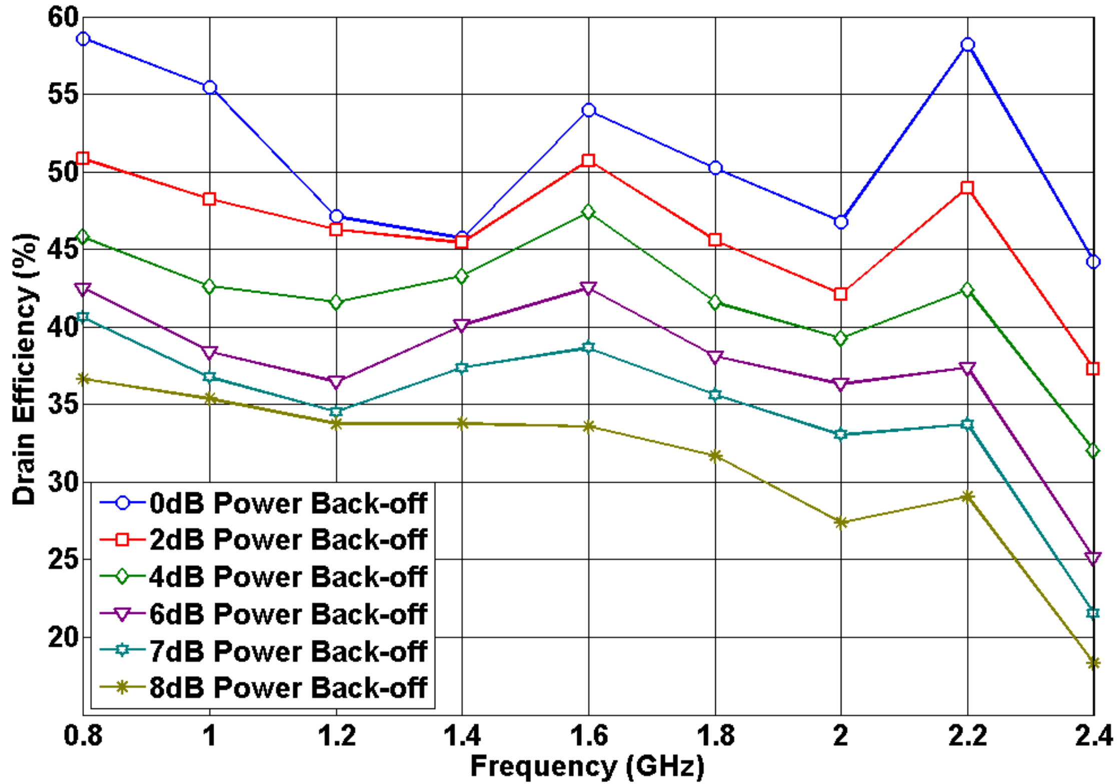


Figure 5.13: Broadband power amplifier's drain efficiency at different power back-off levels.

when the main amplifier saturates before the peaking amplifier turns on. Efficiency of the amplifier is plotted versus frequency for different power back-off values in Fig. 5.13. As can be seen from this graph, the drain efficiency is higher than 35% at 6 dB power back-off for the frequency range of 0.8-2.2 GHz.

To assess the performance and linearity of the power amplifier, it was tested with a WCDMA (Wideband Code Division Multiple Access) input signal having 7 dB PAPR. The amplifier was tested at different frequencies. Digital pre-distortion (DPD) was also applied on the amplifier to linearize the amplifier. A memory-polynomial DPD technique with nonlinearity order of 8 and memory depth of 5 was used to linearize the amplifiers [48]. The spectrum of the output WCDMA signal are plotted at different frequencies before and after applying DPD in Fig. 5.14. The values of ACPR at the two closest adjacent channels are given in this figure along with the output power and the drain efficiency after applying DPD. The drain efficiency after applying DPD is between 33% to 36% in the frequency band of

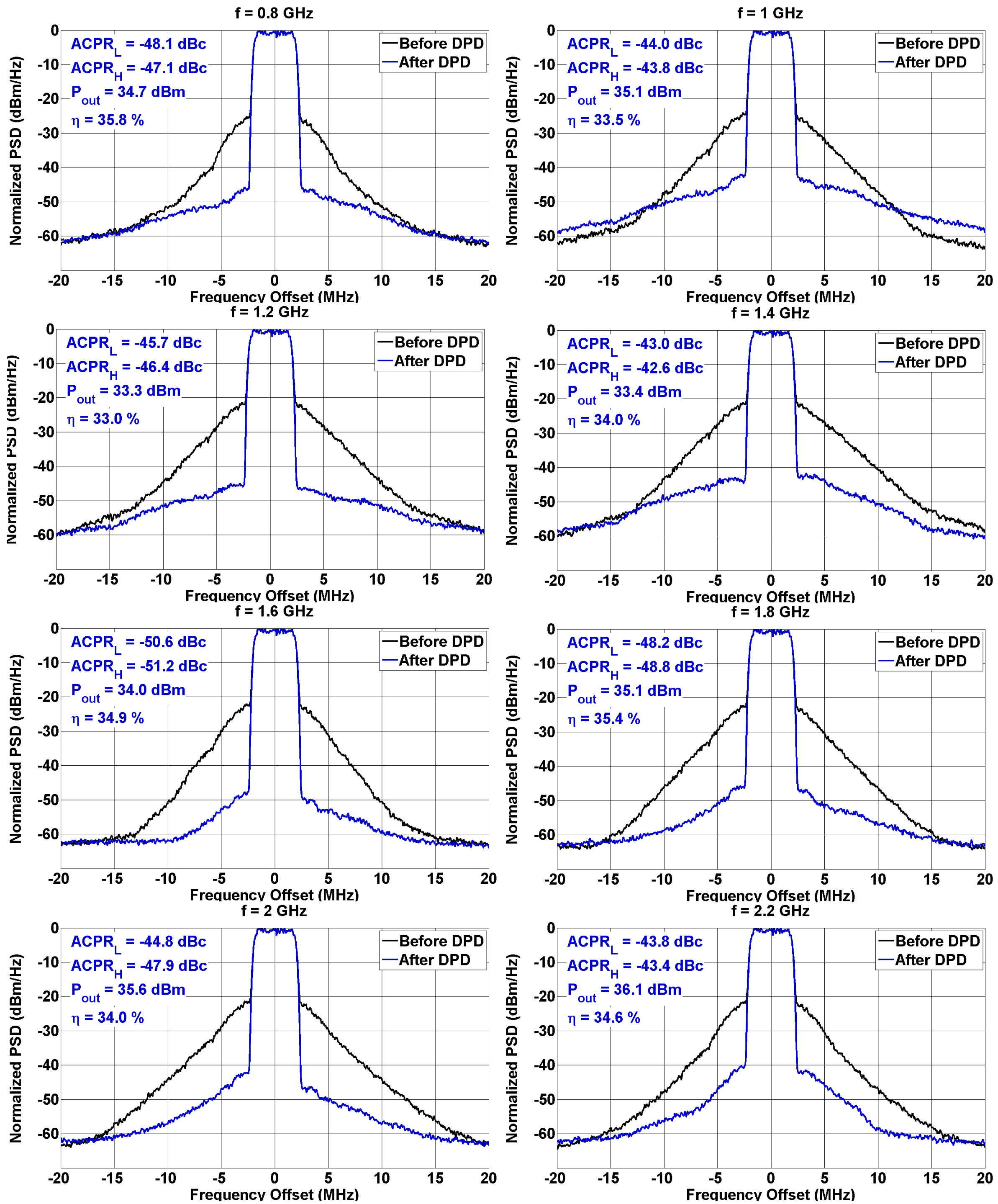


Figure 5.14: Measured spectrum before and after applying DPD for WCDMA input signal at different frequencies.

Reference	Frequency (GHz)	Fractional bandwidth (%)	P_{sat} (dBm)	DE_{6dBBO} (%)
[32]	1.7 - 2.6	42.8	42.1 - 45.3	41 - 55
[35]	2.2 - 2.96	29.8	40.2-41.7	40 - 47
[36]	0.7 - 1.0	35.9	49 - 50.8	52 - 68
[37]	1.7 - 2.4	34.7	39.5 - 41	43 - 59
[38]	1.05 - 2.55	91.7	40 - 41	35 - 58
This work	0.8 - 2.2	105.5	39.3 - 41.9	37 - 43

Table 5.1: Performance summary and comparison for the broadband dual branch current-biased amplifier.

operation and the ACPR level is lower than -43 dBc over the bandwidth.

The measurement results show that the proposed amplifier architecture can provide high efficiency at large power back-off levels in a very large frequency bandwidth. The load modulation for the current-biased main amplifier in this amplifier architecture is the opposite of the load modulation for the conventional voltage-biased amplifiers. This different behaviour completely eliminates the need for use of the impedance inverters in the proposed amplifier and allows operation in very large frequency bandwidth. On the other hand, the test with modulated communication signal shows that the amplifier can be linearized and used for real communication signals.

Table 5.1 shows a comparison of the fabricated power amplifier with the other broadband amplifiers. Compared to the other published results, the fabricated amplifier presents the largest bandwidth with comparable back-off efficiency.

Chapter 6

Current-Biased Linearizing Driver Amplifier

In Chapter 5, the current biased transistor was introduced. It was shown that a current-biased transistor can be used in a multi-branch amplifier to achieve Doherty-like performance in a very large frequency band due to the different behaviour of the current-biased transistor compared to the conventional voltage biasing.

In this chapter, another behaviour of the current biased transistor is introduced and used for designing a new class of analog linearizers. It is shown that a transistor biased in the low voltage-high current region (triode region) can provide controlled gain expansions. The gain expansion behaviour can be used to compensate for the gain compression in the conventional voltage-biased amplifiers.

Referring to Fig. 5.2, in the triode region the I-V curves are closer to each other. In the area where the curves are closer to each other, applying an input signal creates a small change in output current and voltage, leading to a low gain. The amplifier's gain depends on the bias point and the load impedance. As the input signal's amplitude increases, the current-voltage enters the saturation region, leading to larger variation in output current and voltage and hence larger gain for higher input power. It should be noted that this behaviour is not limited to a specific type of transistor.

In this chapter, the analysis of gain expansion is given for MOSFET transistors because due to the advances in CMOS technology, there are very well-established and accurate equations for MOSFET characteristics. In the analysis, the I-V characteristics of the MOSFET is used to study the gain expansion in MOSFETs. As a proof of concept, a very simple current-biased amplifier is designed as the driver amplifier to linearize a CMOS power amplifier. In fact the example given here may be sensitive to process variations and consequently, addi-

tional circuitry may required to stabilize the amplifier regarding process and temperature variations. The same concept is used to design a broadband GaN amplifier presenting gain expansion to linearize a GaN power amplifier.

This chapter is organized as follows: In Section 6.1, the analysis for gain expansion in MOSFET transistors is given. In Section 6.2, the analysis is validated by simulation of an NMOS transistor. In Section 6.3, a design procedure is given to design a driver amplifier with a predefined output power and gain expansion. In Section 6.4, a driver amplifier is designed to linearize a power amplifier and it is shown that the driver amplifier decreases the gain compression and the intermodulation levels. Finally, in Section 6.5 a broadband current-biased GaN amplifier is designed for linearizing a GaN power amplifier and it is shown that using the current-biased amplifier as the driver, the power amplifier's gain compression can be greatly reduced in a very large bandwidth.

6.1 Analysis of Gain Expansion in MOSFET Transistors

In this section, the current-voltage waveform analysis is given for an N-channel MOSFET providing gain expansion. Using analytical I-V characteristics, the amount of gain expansion, output power and the current and voltage waveforms are obtained. The analysis is given for resistive loading in fundamental frequency and all harmonic frequencies. Using the same approach the analysis can be done for other harmonic loading cases.

According to the current-voltage characteristics, MOSFETs have three regions of operation [80]. In cut-off region ($V_{GS} < V_{TH}$), no current flows into the drain and the transistor is considered to be in the off state. The saturation region ($V_{GS} > V_{TH}$ and $V_{DS} > V_{GS} - V_{TH}$) is the region where the drain current is almost constant versus drain-source voltage V_{DS}. The saturation region is usually used as the bias region for power amplifiers. The triode region ($V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$) is the region where the drain current has large dependency on the drain-source voltage V_{DS}.

The N-channel MOSFET's current-voltage relationship in saturation and triode regions can be expressed as:

$$I_D = \begin{cases} \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_{TH})\, \beta V_{DS} - \frac{(\beta V_{DS})^2}{2} \right] & \beta V_{DS} \leq V_{GS} - V_{TH} \\ \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{TH})^2 & \beta V_{DS} > V_{GS} - V_{TH} \end{cases} \tag{6.1}$$

The parameter β is introduced in the equations to obtain a better fit to the actual simulated or measured I-V data. Letting $\beta = 1$, results in the conventional I-V equations [80]. (6.1) can be re-written as:

$$I_D = \begin{cases} 2\alpha \left[V_E \beta V_{DS} - \frac{(\beta V_{DS})^2}{2} \right] & \beta V_{DS} \leq V_E \\ \alpha V_E^2 & \beta V_{DS} > V_E \end{cases} \tag{6.2}$$

where:

$$\alpha = \frac{\mu_n C_{ox} W}{2L} \tag{6.3}$$

$$V_E = V_{GS} - V_{TH} \tag{6.4}$$

6.1.1 Small-Signal Gain in Triode Region

Consider the circuit shown in Fig. 6.1 consisting of a transistor biased through a current source in the triode region and a resistive load R_L. It should be noted that the current source shown in this circuit cannot be a current mirror since current mirrors do not provide high efficiency. The current source should be implemented using high efficiency switching circuits.

Due to presence of the DC blocking capacitor, the load current does not have a DC component. Under small-signal condition, the drain current, drain-source voltage and the gate overdrive voltage V_E can be decomposed to a DC and an AC component as:

$$I_D = I_{DQ} + i_d \tag{6.5}$$

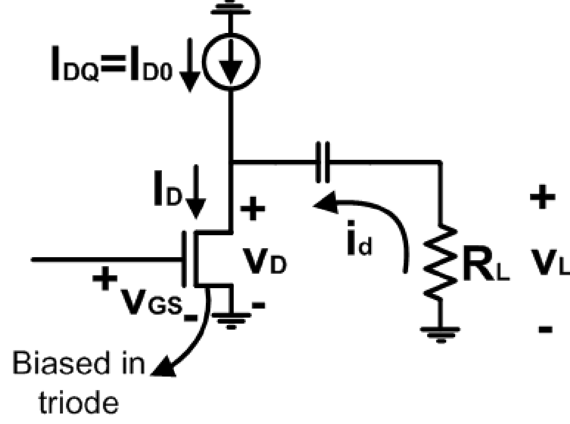


Figure 6.1: Current biased N-channel MOSFET with resistive load.

$$V_{DS} = V_{DSQ} - v_{ds} \tag{6.6}$$

$$V_E = V_{EQ} - v_e = V_{EQ} - v_{gs} \tag{6.7}$$

On the other hand, we can write:

$$v_{ds} = -R_L i_d \tag{6.8}$$

Since the transistor is biased in triode region, using (6.2) we can be write:

$$I_{DQ} + i_d = 2\alpha \left[(v_{gs} + V_{EQ})\beta(v_{ds} + V_{DSQ}) - \frac{\beta^2 (V_{DSQ} + v_{ds})^2}{2} \right]$$

or:

$$I_{DQ} + i_d = 2\alpha\beta \left[v_{gs}v_{ds} + V_{EQ}V_{DSQ} + v_{gs}V_{DSQ} + v_{ds}V_{EQ} - \beta \frac{v_{ds}^2 + V_{DSQ}^2 + 2v_{ds}V_{DSQ}}{2} \right] \tag{6.9}$$

If $v_e << V_{EQ}$ and $v_{ds} << V_{DSQ}$, then the small signal part can be written as:

$$i_d \approx 2\alpha\beta \left[v_{gs}V_{DSQ} + v_{ds}V_{EQ} - \beta v_{ds}V_{DSQ} \right]$$

or:

$$\frac{i_d}{v_{gs}} \approx \frac{V_{DSQ}}{\frac{1}{2\alpha\beta} + R_L(V_{EQ} - \beta V_{DSQ})} \tag{6.10}$$

From (6.2) we can write:

$$\beta V_{DSQ} = V_{EQ}\left(1-\sqrt{1-\frac{I_{DQ}}{\alpha V_{EQ}^2}}\right) = V_{EQ}\left(1-\sqrt{1-I_{DQ,norm}}\right) \tag{6.11}$$

$$I_{DQ,norm} = \frac{I_{DQ}}{I_{DQ,sat}} = \frac{I_{DQ}}{\alpha V_{EQ}^2} \tag{6.12}$$

$I_{DQ,norm}$ is the normalized drain bias current I_{DQ} to the maximum achievable drain current at the bias gate voltage. The value of I_{DQ} can vary between 0 and 1. Using (6.11), (6.13) can be written as:

$$g_{m,ss} = \frac{i_d}{v_{gs}} \approx \frac{2\left(1-\sqrt{1-I_{DQ,norm}}\right)}{1/\alpha V_{EQ} + 2\beta R_L\sqrt{1-I_{DQ,norm}}} \tag{6.13}$$

$g_{m,ss}$ obtained in (6.13) is the small-signal transconductance from gate voltage to drain current. Having the transconductance, the input impedance of the transistor R_G and the load impedance R_L, the small-signal power gain of the amplifier can be obtained as:

$$G_{ss} = \frac{P_{out}}{P_{in}} = \frac{i_d^2 R_L}{v_{gs}^2/R_G} = g_{m,ss} R_L R_G \tag{6.14}$$

6.1.2 Large-Signal Load Line

In the circuit of Fig. 6.1, the load voltage and current do not have DC components while the transistor's voltage and current are composed of both DC and AC components. We denote the DC component of drain current as I_{D0} and the DC component of the drain-source voltage as V_{DS0}. The drain voltage and current can be decomposed to AC and DC components as follows:

$$I_D = I_{D0} + i_d \tag{6.15}$$

$$v_L = -R_L i_d \tag{6.16}$$

$$V_{DS} = v_L + V_{DS0} = -R_L i_d + V_{DS0} \tag{6.17}$$

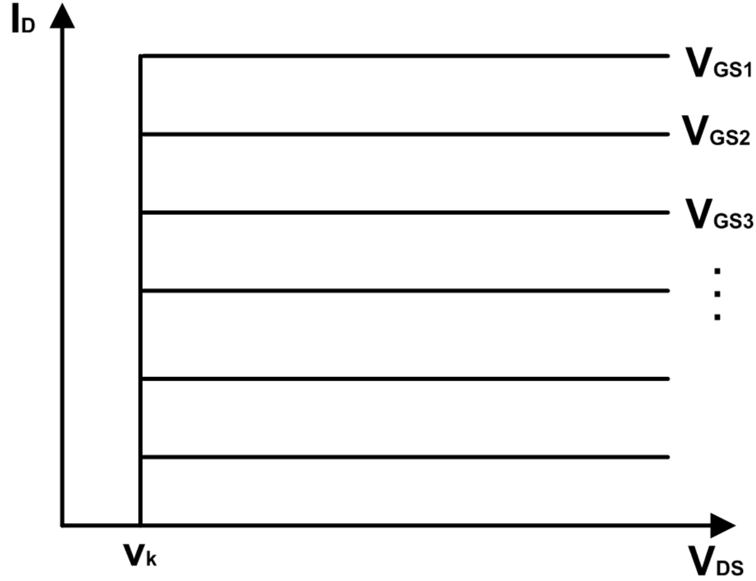


Figure 6.2: Simplified transistor's I-V characteristics.

From (6.15) and (6.17), we can write:

$$V_{DS} = -R_L(I_D - I_{D0}) + V_{DS0} \tag{6.18}$$

Equation (6.18) is the load line equation for the amplifier and it means that the load line always passes from the transistor's DC operating point for any current and voltage waveforms. It should be noted that the DC operating point may be different from the bias point since the DC component of drain-source voltage V_{DS0} can be different from the drain-source bias voltage V_{DSQ}.

6.1.3 Large-Signal Current Waveform

To quantify the amplifier's gain expansion, the value of large signal gain should be determined. A large signal analysis is presented in this section that can be used to calculate the large signal gain, maximum output power and the transistor's current/voltage waveforms in the large signal condition.

To obtain the large signal behaviour of the amplifier, the simplified I-V characteristics shown in Fig. 6.2 is used. This form of I-V characteristics can be used when the transistor's

drain voltage swing is larger than the knee voltage. The value of the knee voltage v_k can be selected based on the bias point and the transistor characteristics.

For the amplifier circuit of Fig. 6.1, we consider the gate voltage to have a DC bias component and a sinusoidal AC part (input signal). Using (6.4), we can express the input voltage as:

$$V_E = V_{EQ} + A\cos\omega t = V_{EQ} + A\cos\theta \tag{6.19}$$

In (6.19), the condition $A < V_{EQ}$ should be met to avoid entering the cut-off region. The drain current I_D and the drain source voltage V_{DS} have to stay on the load line given in (6.18). It means that they are continuous functions of time. Using the simplified I-V characteristics shown in Fig. 6.2 and the second part of (6.2), the time-domain drain current can be written as:

$$I_D = \begin{cases} \alpha V_E^2(\theta_t) & \theta \leq \theta_t \\ \alpha V_E^2(\theta) & \theta > \theta_t \end{cases} \tag{6.20}$$

In (6.20), θ_t is the transition angle in which the transistor enters saturation region. Using (6.19), (6.20) can be written as:

$$I_D = \begin{cases} \alpha(V_{EQ} + A\cos\theta_t)^2 & \theta \leq \theta_t \\ \alpha(V_{EQ} + A\cos\theta)^2 & \theta > \theta_t \end{cases} \tag{6.21}$$

The value of θ_t can be found from DC component of the transistor's current. The transistor current's DC component is the same as the bias current. The DC component of the drain current can be found as:

$$I_{D0} = I_{DQ} = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_D(\theta)\,\mathrm{d}\theta = \frac{1}{\pi}\int_{0}^{\pi} I_D(\theta)\,\mathrm{d}\theta \tag{6.22}$$

Using (6.21), (6.22) can be written as:

$$
\begin{aligned}
\frac{\pi I_{DQ}}{\alpha} =& \int_0^{\theta_t} \left(V_{EQ} + A\cos\theta_t\right)^2 \, \mathrm{d}\theta + \int_{\theta_t}^{\pi} \left(V_{EQ} + A\cos\theta\right)^2 \, \mathrm{d}\theta \\
=&\theta_t V_{EQ}^2 + 2AV_{EQ}\theta_t\cos\theta_t + \frac{\theta_t A^2}{2}(1+\cos 2\theta_t) + (\pi - \theta_t)V_{EQ}^2 \\
&- 2AV_{EQ}\sin\theta_t + (\pi-\theta_t)\frac{A^2}{2} - \frac{A^2}{4}\sin 2\theta_t \\
=&\pi V_{EQ}^2 + \frac{\pi A^2}{2} + \frac{\theta_t A^2}{2}\cos 2\theta_t + 2AV_{EQ}\theta_t\cos\theta_t - \frac{A^2}{4}\sin 2\theta_t - 2AV_{EQ}\sin\theta_t
\end{aligned}
\tag{6.23}
$$

Equation (6.23) can be re-written as:

$$
\frac{A}{4}\left(2\theta_t\cos 2\theta_t - sin2\theta_t\right) + 2V_{EQ}(\theta_t\cos\theta_t - \sin\theta_t) = \frac{\pi}{A}\left(\frac{I_{DQ}}{\alpha} - V_{EQ}^2 - \frac{A^2}{2}\right) \tag{6.24}
$$

We define $A_{norm} = A/V_{EQ}$ as the normalized input signal's amplitude. The value of A_{norm} has to be between 0 and 1 to prevent the transistor from entering cut-off region. Using the definition of A_{norm}, (6.24) can be written as:

$$
A_{norm}\left(2\theta_t\cos 2\theta_t - sin2\theta_t\right) + 8(\theta_t\cos\theta_t - \sin\theta_t) = \frac{4\pi}{A_{norm}}\left(I_{DQ,norm} - \frac{A_{norm}^2}{2} - 1\right) \tag{6.25}
$$

Equation (6.25), can be solved for θ_t to find the transition angle versus the values of A_{norm} and $I_{DQ,norm}$. Fig. 6.3 shows the values of θ_t versus normalized input signal's amplitude A_{norm} for different values of normalized bias current $I_{DQ,norm}$.

6.1.4 Large-Signal Voltage Waveform

Having current waveforms is enough for the calculation of large signal gain (and consequently the value of gain expansion) and output power, but it is worthwhile to obtain the drain-source voltage waveforms in case efficiency of the amplifier is of interest.

According to the load-line given in (6.18), the transistor's I-V curves given in Fig. 6.2 and the current waveform obtained in (6.21), the voltage waveform can be found as:

$$
V_{DS} = \begin{cases} v_k & \theta \le \theta_t \\ V_{DS0} + R_L(I_{DQ} - I_D) & \theta > \theta_t \end{cases} \tag{6.26}
$$

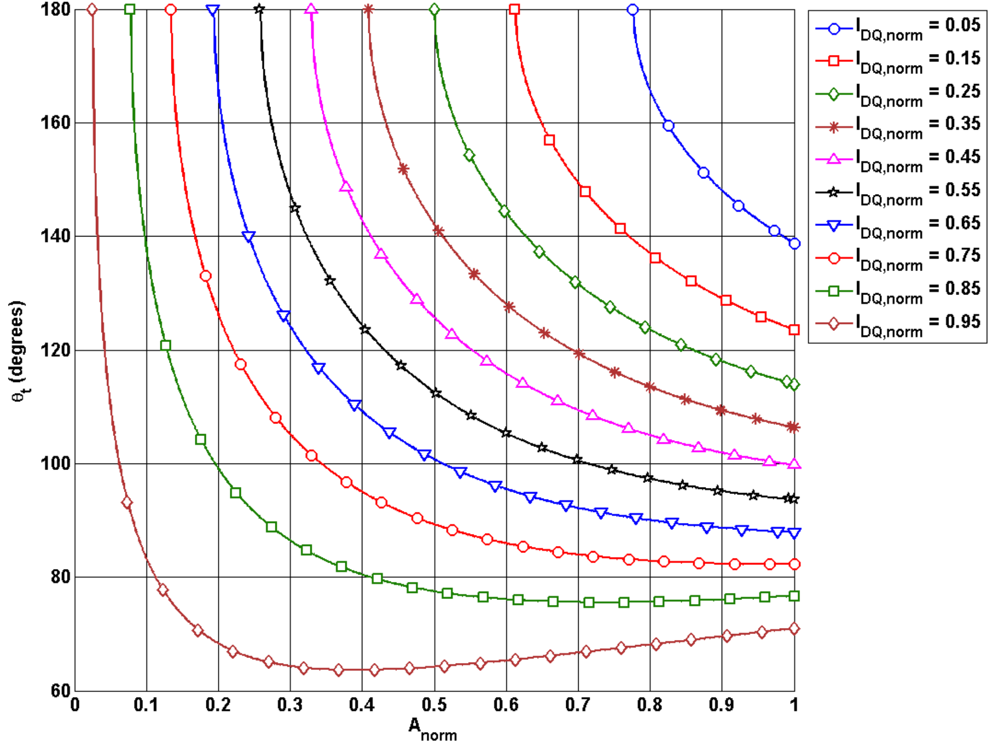


Figure 6.3: Values of θ_t for different bias points and input amplitudes.

The DC component of drain voltage V_{DS0} needs to be determined. Using the definition of the DC component, we have:

$$\pi V_{DS0} = \int_0^{\pi} V_{DS}(\theta)\,\mathrm{d}\theta = \theta_t v_k + \int_{\theta_t}^{\pi} V_{DS0} + R_L(I_{DQ} - I_D)\,\mathrm{d}\theta \tag{6.27}$$

Using (6.21), (6.27) can be written as:

$$\begin{aligned}\theta_t V_{DS0} =& \theta_t v_k + R_L(\pi - \theta_t) I_{DQ} \\ &+ R_L \alpha \left[(\theta_t - \pi) \left(V_{EQ}^2 + \frac{A^2}{2} \right) + 2 A V_{EQ} \sin\theta_t + \frac{A^2}{4} \sin 2\theta_t \right]\end{aligned} \tag{6.28}$$

and the value of V_{DS0} can be calculated as:

$$V_{DS0} = v_k + \frac{R_L \alpha V_{EQ}^2}{\theta_t} \left((\pi - \theta_t) \left(I_{DQ,norm} - \frac{A_{norm}^2}{2} - 1 \right) + 2 A_{norm} \sin\theta_t + \frac{A_{norm}^2}{4} \sin 2\theta_t \right) \tag{6.29}$$

In Fig. 6.4, the value of $(V_{DS0} - v_k)/(R_L \alpha V_{EQ}^2)$ is plotted versus input signal's normalized amplitude A_{norm} for different values of normalized bias current $I_{DQ,norm}$.

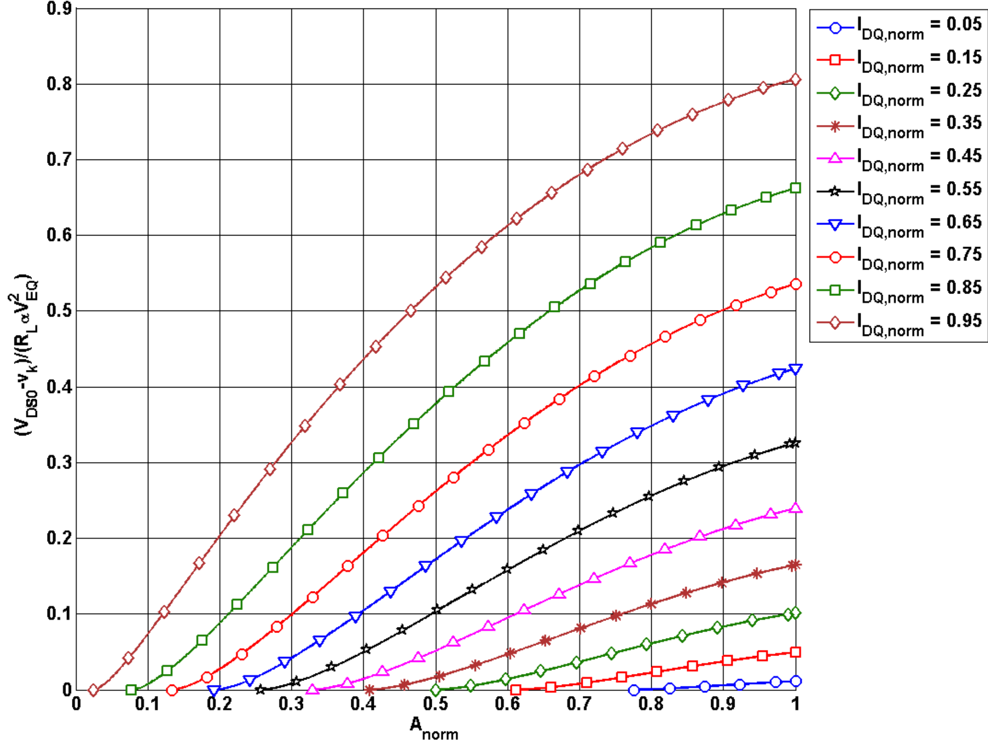


Figure 6.4: The value of $(V_{DS0} - vk)/(R_L \alpha V_{EQ}^2)$ for different biases and input amplitudes

6.1.5 Large-Signal Gain

To calculate the large signal gain, the harmonic content of the current waveform has to be determined. The cosine Fourier series of the current waveform can be written as:

$$\begin{aligned} I_D &= \frac{I_0}{2} + \sum_{n=1}^{\infty} I_n \cos n\theta = I_{DQ} + \sum_{n=1}^{\infty} I_n \cos n\theta \\ I_n &= \frac{2}{\pi} \int_0^{\pi} I(\theta) \cos n\theta \, \mathrm{d}\theta \end{aligned} \tag{6.30}$$

for $n \geq 1$, we can write:

$$\begin{aligned} \frac{\pi}{2\alpha} I_n =& \int_0^{\theta_t} (V_{EQ} + A\cos\theta_t)^2 \cos n\theta \, \mathrm{d}\theta + \int_{\theta_t}^{\pi} (V_{EQ} + A\cos\theta)^2 \cos n\theta \, \mathrm{d}\theta \\ =& (V_{EQ} + A\cos\theta_t)^2 \frac{\sin n\theta_t}{n} + \int_{\theta_t}^{\pi} V_{EQ}^2 \cos n\theta \, \mathrm{d}\theta \\ &+ \int_{\theta_t}^{\pi} 2AV_{EQ} \cos\theta \cos n\theta \, \mathrm{d}\theta + \int_{\theta_t}^{\pi} A^2 \cos^2\theta \cos n\theta \, \mathrm{d}\theta \end{aligned} \tag{6.31}$$

Calculation of integrals in (6.31), results in:

$$\frac{\pi}{2\alpha} I_n = \begin{cases} \sin\theta_t\left(2AV_{EQ}\cos\theta_t + \frac{A^2}{2}\cos 2\theta_t\right) - AV_{EQ}\left(\frac{\sin 2\theta_t}{2} + \theta_t - \pi\right) - \frac{A^2}{2}\left(\frac{\sin 3\theta_t}{6} + \frac{\sin\theta_t}{2}\right) & n=1 \\ \frac{\sin 2\theta_t}{2}\left(2AV_{EQ}\cos\theta_t + \frac{A^2}{2}\cos 2\theta_t\right) - AV_{EQ}\left(\frac{\sin 3\theta_t}{3} + \sin\theta_t\right) - \frac{A^2}{2}\left(\frac{\sin 4\theta_t}{8} + \frac{\theta_t - \pi}{2}\right) & n=2 \\ \frac{\sin n\theta_t}{n}\left(2AV_{EQ}\cos\theta_t + \frac{A^2}{2}\cos 2\theta_t\right) - AV_{EQ}\left(\frac{\sin(n+1)\theta_t}{n+1} + \frac{\sin(n-1)\theta_t}{n-1}\right) - \frac{A^2}{2}\left(\frac{\sin(n+2)\theta_t}{2(n+2)} + \frac{\sin(n-2)\theta_t}{2(n-2)}\right) & n>2 \end{cases} \tag{6.32}$$

Using the definition of A_{norm}, the normalized harmonic coefficients can be written as:

$$I_{n,norm} = \frac{I_n}{\alpha V_{EQ}^2} = \frac{2}{\pi} \begin{cases} \sin\theta_t\left(2A_{norm}\cos\theta_t + \frac{A_{norm}^2}{2}\cos 2\theta_t\right) - A_{norm}\left(\frac{\sin 2\theta_t}{2} + \theta_t - \pi\right) - \frac{A_{norm}^2}{2}\left(\frac{\sin 3\theta_t}{6} + \frac{\sin\theta_t}{2}\right) & n=1 \\ \frac{\sin 2\theta_t}{2}\left(2A_{norm}\cos\theta_t + \frac{A_{norm}^2}{2}\cos 2\theta_t\right) - A_{norm}\left(\frac{\sin 3\theta_t}{3} + \sin\theta_t\right) - \frac{A_{norm}^2}{2}\left(\frac{\sin 4\theta_t}{8} + \frac{\theta_t - \pi}{2}\right) & n=2 \\ \frac{\sin n\theta_t}{n}\left(2A_{norm}\cos\theta_t + \frac{A_{norm}^2}{2}\cos 2\theta_t\right) - A_{norm}\left(\frac{\sin(n+1)\theta_t}{n+1} + \frac{\sin(n-1)\theta_t}{n-1}\right) - \frac{A_{norm}^2}{2}\left(\frac{\sin(n+2)\theta_t}{2(n+2)} + \frac{\sin(n-2)\theta_t}{2(n-2)}\right) & n>2 \end{cases} \tag{6.33}$$

The normalized transconductance plot for the fundamental component is shown in Fig. 6.5. As can be seen, the transconductance is increasing with the input signal's amplitude for some bias conditions which means that the amplifier has an expanding gain. In fact the graphs shown in Fig. 6.5 are valid for high input drive values (higher values of A_{norm}) due to the idealization of the I-V curves in Fig. 6.2. The actual amount of gain expansion can be obtained from the small signal analysis given in the previous subsection.

6.2 Validation of the Analysis

To validate the analysis given above, a thick-oxide N-channel MOSFET having gate length of L=1 μm and width of W=100 μ m (20 fingers of 5 μm)was used. In the first step the I-V characteristic of the transistor was obtained using DC sweep simulations. The I-V characteristics were fitted to the analytical equations of (6.2). The parameters of the model were obtained as: α=6.6 mA/V^2, β=1.4 and V_{TH}=350 mV. The I-V curves obtained from simulation is plotted along with the I-V curves obtained from analytical equations in Fig. 6.6. As can be seen from Fig. 6.6, the analytical equations model the I-V curves with relatively low error for gate voltages of up to 2.2 V.

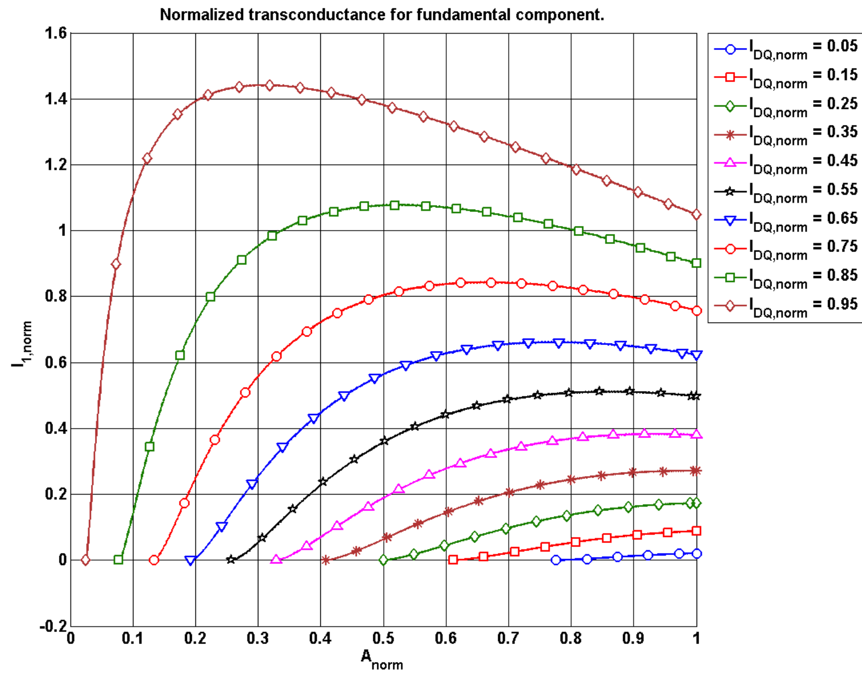


Figure 6.5: Normalized fundamental transconductance for different bias points and input amplitudes.

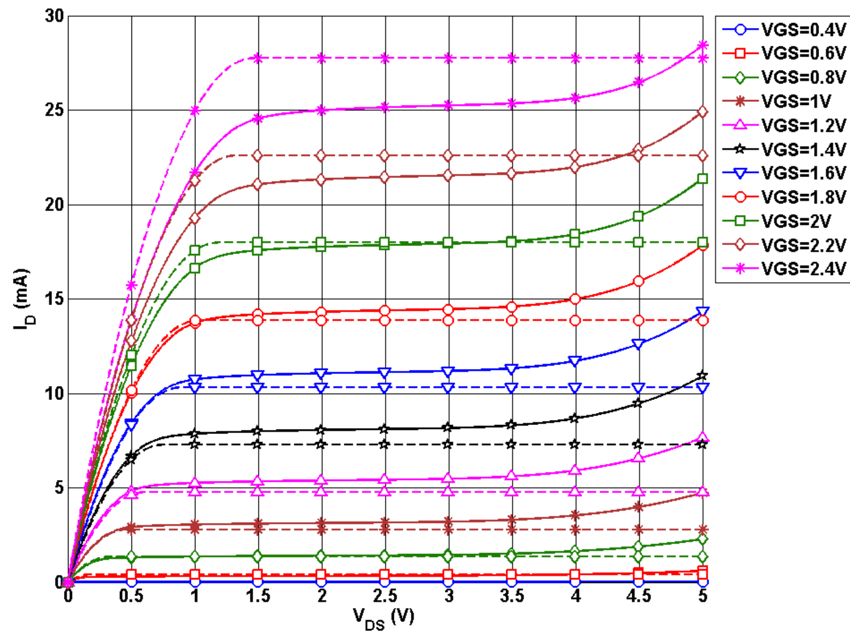


Figure 6.6: The simulated (solid) and analytically modeled (dashed) I-V curves for an NMOS transistor having L=1 μm and W=100 μm.

The transistor was biased in different bias points in triode region and simulated with different load impedances. The simulated and analytically obtained current waveforms are plotted in Fig. 6.7 for the different biases, input amplitudes and load impedances. As can be seen, the current waveforms match well for the higher input amplitudes. The output power obtained from simulation and analytical equations are plotted in Fig. 6.8. As can be seen from this figure, the output powers match at least for the last 10-15 dB of higher output power range. In lower input powers, the analytical equations are not accurate due to the idealized I-V curves used (Fig. 6.2).

6.3 Design Procedure

In this section, a design procedure is provided for designing an amplifier with NMOS having predetermined maximum output power and gain expansion. The amplifier is considered as the driver stage to provide the required input power to the PA input and to provide the required amount of gain expansion to compensate for the gain compression of the power amplifier. The design procedure provides guidelines to select the driver transistor's size, the bias conditions and the loading requirements.

In a given technology, the maximum transistor's voltage is fixed. The transistor cannot exceed the maximum drain-source voltage specified by the breakdown voltage. Having the maximum voltage fixed and using the load-line characteristics and the I-V characteristics given in Fig. 6.2, one can write:

$$R_L I_{max} = V_{max} - v_k \tag{6.34}$$

In (6.34), I_{max} is the maximum drain current and V_{max} is the maximum drain-source voltage. Maximum output power at fundamental frequency can be obtained as:

$$P_{out,max} = \frac{R_L I_{1,max}^2}{2} \tag{6.35}$$

In (6.35), $I_{1,max}$ is the fundamental component of the output current at maximum input

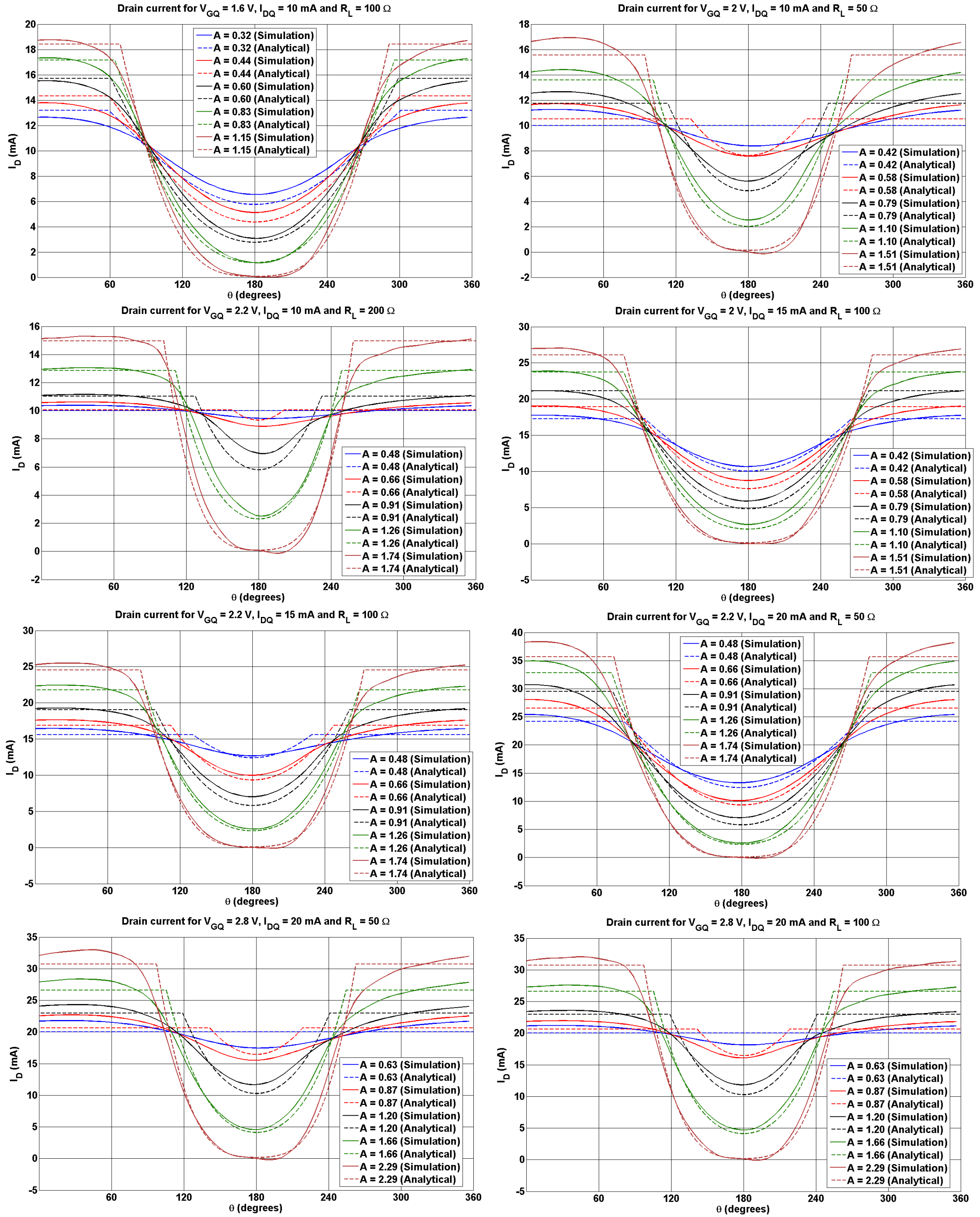


Figure 6.7: Time domain drain current for different biases, load impedances and input amplitudes.

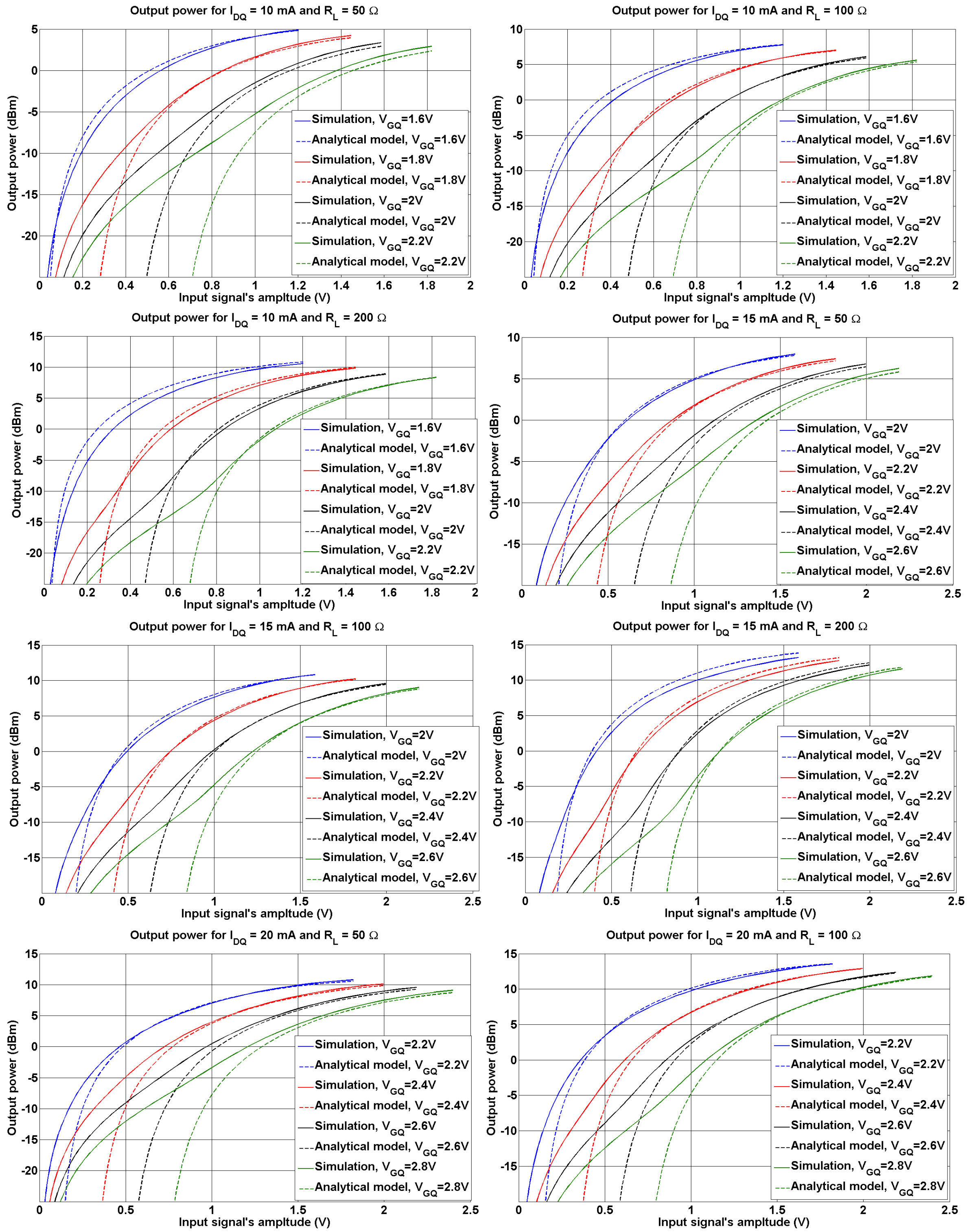


Figure 6.8: Simulated and analytically obtained output power.

power. To avoid signal clipping, the transistor should not enter cut-off region which means that the maximum input signal's amplitude without clipping the signal is when $A = A_{max} = V_{EQ}$ (equation (6.19)). We define $\theta_{t,max}$ as the transition angle at maximum input power ($A = V_{EQ}$); Then from (6.33), one can write:

$$\begin{aligned} I_{1max} &= \alpha V_{EQ}^2 \frac{2}{\pi} \left(\sin\theta_{t,max} \left(2\cos\theta_{t,max} + \frac{\cos 2\theta_{t,max}}{2} \right) - \left(\frac{\sin 2\theta_{t,max}}{2} + \theta_{t,max} - \pi \right) - \left(\frac{\sin 3\theta_{t,max}}{12} + \frac{\sin\theta_{t,max}}{4} \right) \right) \\ &= \frac{\alpha V_{EQ}^2}{\pi} \left(2\pi - 2\theta_{t,max} - \sin\theta_{t,max} + \sin 2\theta_{t,max} + \frac{\sin 3\theta_{t,max}}{3} \right) = \alpha V_{EQ}^2 f(\theta_{t,max}) \end{aligned} \tag{6.36}$$

On the other hand, from (6.21) we have:

$$I_{max} = \alpha (V_{EQ} + A_{max} \cos\theta_{t,max})^2 = \alpha V_{EQ}^2 (1 + \cos\theta_{t,max})^2 \tag{6.37}$$

From (6.36) and (6.37) we have:

$$\frac{I_{max}}{I_{1,max}} = \frac{(1 + \cos\theta_{t,max})^2}{f(\theta_{t,max})} \tag{6.38}$$

From (6.34), (6.35) and (6.38) we have:

$$\begin{aligned} P_{out,max} &= \frac{R_L I_{1,max}^2}{2} = \frac{R_L}{2} \frac{I_{max}^2 \left[f(\theta_{t,max}) \right]^2}{(1 + \cos\theta_{t,max})^4} \\ &= \frac{V_{max} - v_k}{2} \frac{\left[f(\theta_{t,max}) \right]^2}{(1 + \cos\theta_{t,max})^4} I_{max} = \frac{V_{max} - v_k}{2} \frac{\left[f(\theta_{t,max}) \right]^2}{(1 + \cos\theta_{t,max})^2} \alpha V_{EQ}^2 \end{aligned} \tag{6.39}$$

which can be re-written as:

$$\alpha V_{EQ}^2 = \frac{2 P_{out,max} (1 + \cos\theta_{t,max})^2}{(V_{max} - v_k) \left[f(\theta_{t,max}) \right]^2} \tag{6.40}$$

From (6.40) and (6.34), αV_{EQ}^2 and R_L can be obtained versus $\theta_{t,max}$. On the other hand, solving (6.25), $\theta_{t,max}$ can be obtained as a function of $I_{DQ,norm}$. It means that αV_{EQ}^2 and R_L can be stated as a function of $I_{DQ,norm}$.

So far we applied the required maximum output power and the maximum voltage limitations on the transistor. The other design criterion is the required amount of gain expansion. Assuming that the input impedance of the transistor is constant over the input power range, the amount of gain expansion can be obtained as:

$$\Delta G = G_{Pmax} - G_{ss} = 20 \log \frac{g_{m,LS}}{g_{m,ss}} \tag{6.41}$$

In (6.41), ΔG is the amount of gain expansion in dB. $G_{p,max}$ is the large signal power gain in dB and G_{ss} is the small-signal power gain in dB. $G_{m,LS}$ is the transistor's transconductance (gate voltage to drain's fundamental current component) in maximum output power and $g_{m,ss}$ is the small-signal transconductance. From (6.36) and (6.13), we have:

$$10^{\Delta G/20} = \frac{g_{m,LS}}{g_{m,ss}} = \frac{\dfrac{\alpha V_{EQ} f(\theta_{t,max})}{2\left(1-\sqrt{1-I_{DQ,norm}}\right)}}{1/\alpha V_{EQ} + 2\beta R_L \sqrt{1-I_{DQ,norm}}}$$

which gives:

$$\alpha V_{EQ} = \frac{10^{\Delta G/20} 2\left(1-\sqrt{1-I_{DQ,norm}}\right) - f(\theta_{t,max})}{2\beta R_L f(\theta_{t,max})\sqrt{1-I_{DQ,norm}}} \tag{6.42}$$

From (6.40) to (6.42), the value of V_{EQ} can be obtained versus $I_{DQ,norm}$ and using (6.42), the value of α can be obtained versus $I_{DQ,norm}$. The designer can select the proper size of transistor based on maximum current density in transistor or other design criteria. In the following a design example is presented showing the design procedure.

6.4 CMOS Design Example

As it was shown in the previous section, a transistor biased in triode region can be used to design an amplifier having an arbitrary amount of gain expansion and a desired output power. The gain expansion can be used for linearizing the power amplifiers having gain compression. To demonstrate this capability, a power amplifier is designed for optimum efficiency using thick-oxide NMOS transistors from IBM in cascode configuration.

The power amplifier's schematic is shown in Fig. 6.9. The power amplifier is designed for 50 Ω source and load impedances. The bias voltage selected for this amplifier is selected to be 4.5 V. If the amplifier turns on with the turn-on procedure described in Section 3.6.3 (first applying the gate voltage of the common-source transistor and then increasing the drain voltage gradually to its final value), then maximum drain-source voltage on each transistor will be 2.5 V which is lower than maximum bias voltage allowed for each transistor (i.e. 3.6 V). Two transistors having gate length of L=400 nm and width of W=500 μm are used in

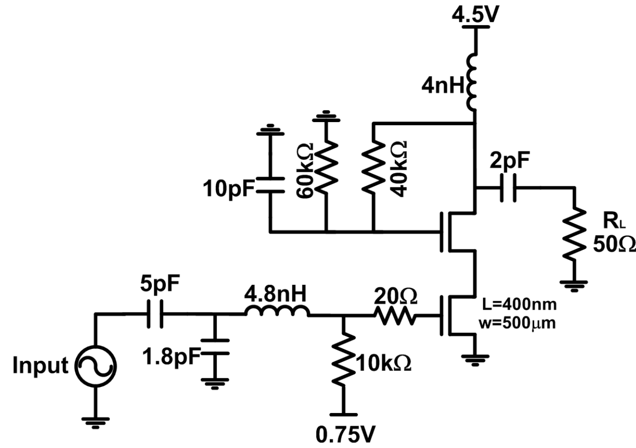


Figure 6.9: The CMOS power amplifier's schematic.

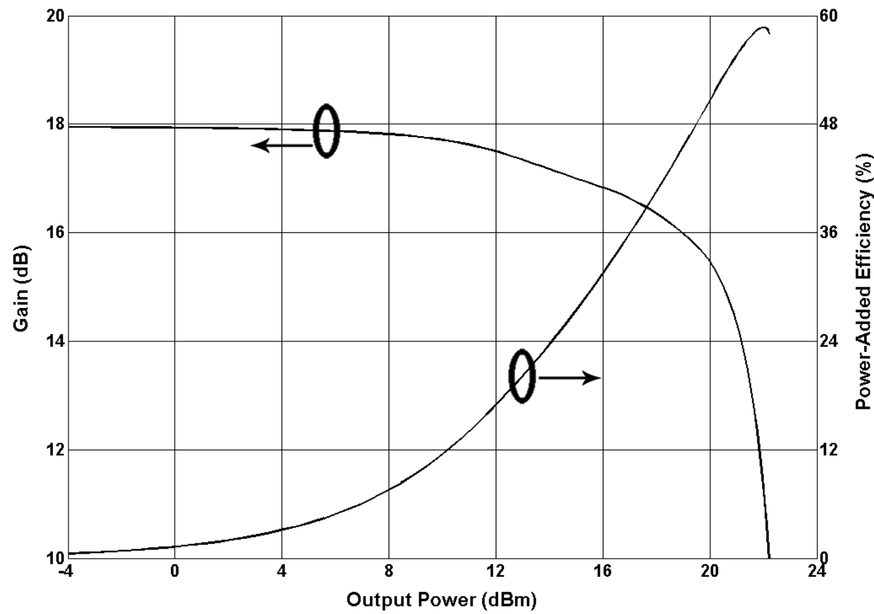


Figure 6.10: Power amplifier's gain and efficiency versus output power.

this amplifier. The design frequency is 2.4 GHz and the amplifier is designed to provide 20 dBm of output power.

The gain and efficiency versus output power are shown in Fig. 6.10. As it can be seen from the gain plot, the output power at 1 dB compression point is 15 dBm and the amplifier has 2.6 dB of gain compression in maximum output power of 20 dBm. To compensate for the gain compression, a current biased amplifier is designed as a driver for this power amplifier. The gain expansion from the driver compensates for the gain compression of the

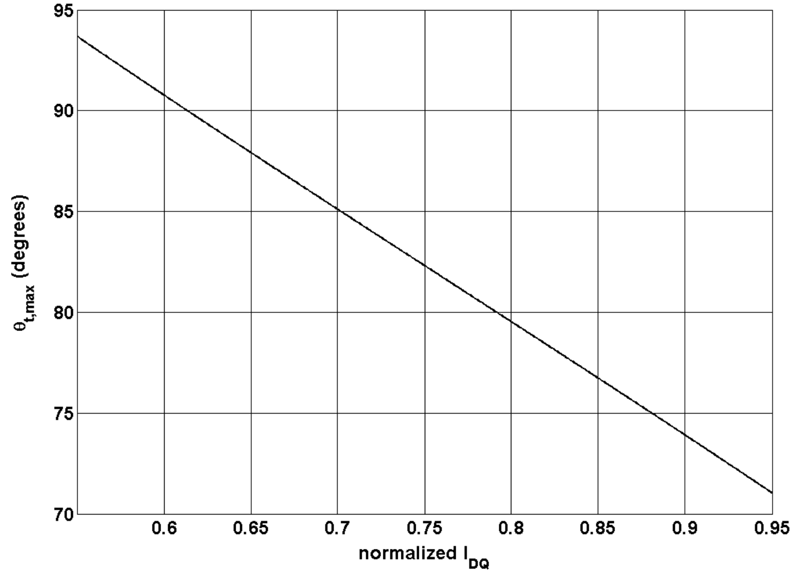


Figure 6.11: The value of $\theta_{t,max}$ versus $I_{DQ,norm}$.

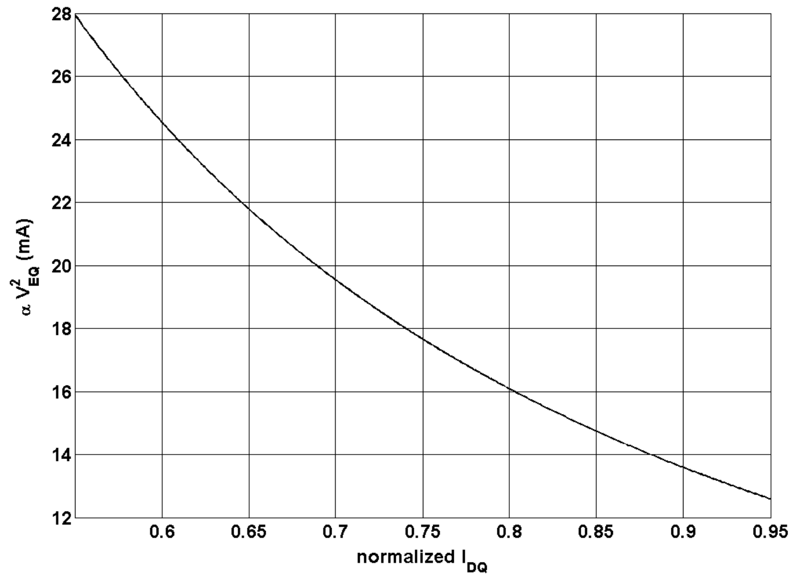


Figure 6.12: The value of αV_{EQ}^2 versus $I_{DQ,norm}$.

power amplifier. For the driver amplifier, a thick-oxide transistor having gate length of 1 μm is used.

Using the design procedure presented in the previous section, the transistor's size, its bias point and loading condition can be obtained. The maximum output power from the driver amplifier is considered to be 11 dBm to have the gain expansion and gain compression

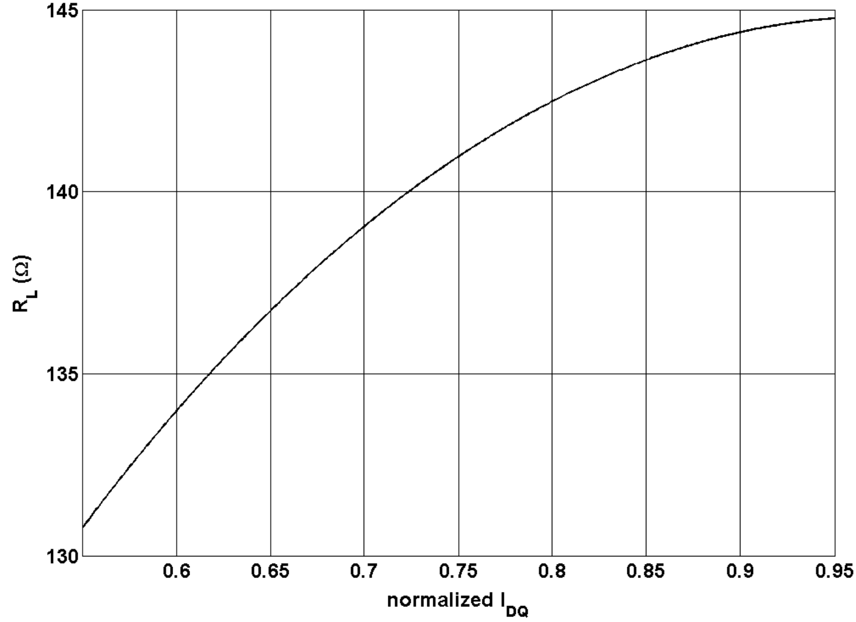


Figure 6.13: The value of R_L versus $I_{DQ,norm}$.

cancelling out each other. The maximum voltage swing on the transistor is selected to be 3.2 V. The amount of gain expansion for the driver amplifier is selected to be 3 dB to compensate for the gain compression of the power amplifier.

The value of $\theta_{t,max}$ can be obtained by replacing $A/V_{EQ} = 1$ in (6.25) and solving for $\theta_{t,max}$. The value of $\theta_{t,max}$ is plotted versus $I_{DQ,norm}$ in Fig. 6.11. From (6.40) and the graph of Fig. 6.11 (equation (6.25)), αV_{EQ}^2 can be obtained versus $I_{DQ,norm}$, and from (6.34), R_L can be obtained versus $I_{DQ,norm}$. Using the design goals, the values of αV_{EQ}^2 and R_L are plotted versus $I_{DQ,norm}$ in Figs. 6.12 and 6.13 respectively. Using (6.42) and the values R_L, the value of αV_{EQ} can be obtained versus $I_{DQ,norm}$. By dividing the values of αV_{EQ}^2 to αV_{EQ}, the value of V_{EQ} and consequently V_{GSQ} can be obtained versus $I_{DQ,norm}$. The value of V_{GSQ} is plotted versus $I_{DQ,norm}$ in Fig. 6.14.

The bias current can be obtained from αV_{EQ}^2 and $I_{DQ,norm}$. To obtain the transistor's size, the value of α can be obtained from the values of αV_{EQ}^2 and V_{GSQ}. The value of α is plotted versus $I_{DQ,norm}$ in Fig. 6.15. The value of α can be used to find the transistor width from scaling the transistor we used to fit the I-V curves to the analytical equations. The

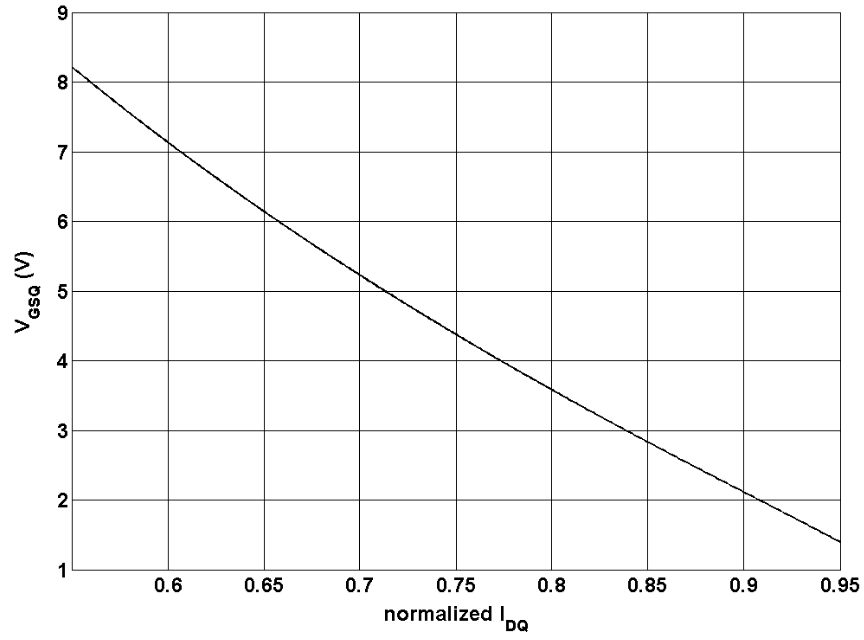


Figure 6.14: The value of V_{GSQ} versus $I_{DQ,norm}$.

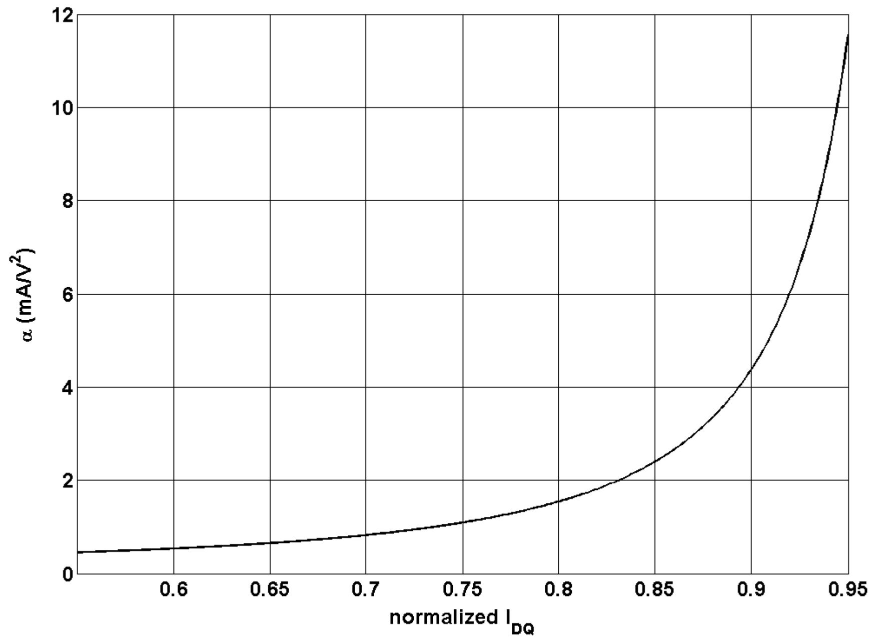


Figure 6.15: The value of α versus $I_{DQ,norm}$.

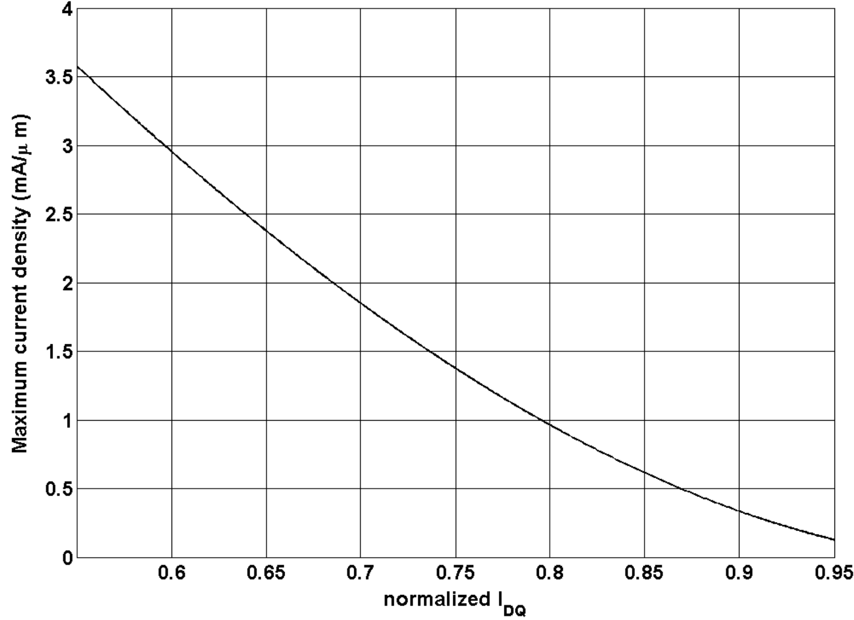


Figure 6.16: Maximum current density versus $I_{DQ,norm}$.

maximum current density can help in selection of the transistor's size. The values of I_{max} can be found versus $I_{DQ,norm}$ using (6.37). Using I_{max} and the values of α, the maximum current density can be calculated versus $I_{DQ,norm}$. The values of the transistor's maximum current density is plotted versus $I_{DQ,norm}$ in Fig. 6.16.

Using the graphs obtained, $I_{DQ,norm} = 0.915$ was selected since this value results in reasonable gate voltage and maximum current density. Using this value and using Fig. 6.15 gives α=5.5 mA/V^2 which means transistor's width should be W=83.3 μm. From Fig. 6.14, the transistor's gate bias voltage is obtained to be V_{GSQ}=1.9 V and from Fig. 6.12, the transistor's drain bias current obtained to be I_{DQ}=12.1 mA. From Fig. 6.13, the load impedance is obtained as R_L=144.5 Ω. The transducer power gain versus output power for the driver amplifier is shown in Fig. 6.17. The final amplifier's schematic consisting of the driver amplifier and the power amplifier is shown in Fig. 6.18. The amplifier is designed for 50 Ω source and load impedances. The gate bias voltage and the drain bias current were slightly changed to obtain the desired overall gain for the amplifier. The final gain versus output power for the amplifier chain is shown in Fig. 6.19. To compare the gain profile for

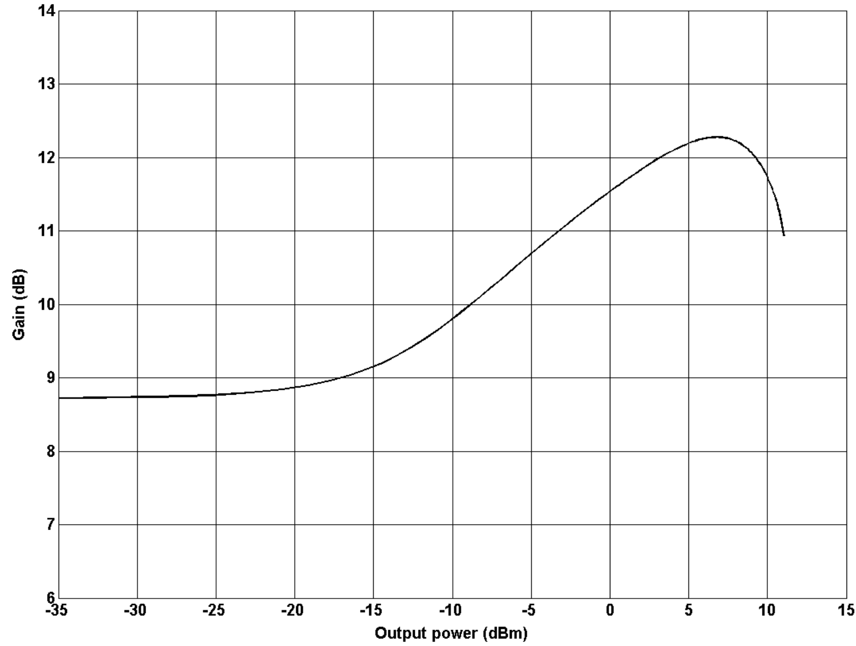


Figure 6.17: Driver amplifier's gain versus output power.

the PA before and after adding the current biased driver amplifier, normalized gain is plotted for both cases in Fig. 6.20. As can be seen from this figure, using the current-biased driver amplifier, the amount of gain compression decreased to 1 dB at the maximum output power of 20 dBm. A two-tone simulation was also done on the amplifier. The values of third-order intermodulation components are plotted for the power amplifier and the amplifier chain in Fig. 6.21. By using the current biased driver amplifier, the level of power amplifier's intermodulation is improved by up to 11 dB.

It should be noted that as stated at the beginning of this chapter, the amplifier circuit shown in Fig. 6.18 may be sensitive to fabrication tolerances and process variations. Bias stabilization feedback proposed in Section 5.1.2 can be used to stabilize the bias point and make the amplifier performance robust to process variations.

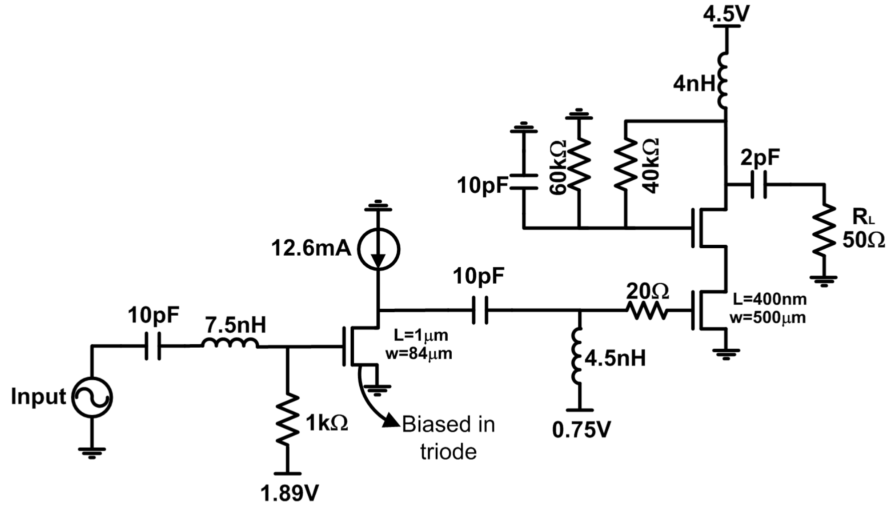


Figure 6.18: Final amplifier's schematic.

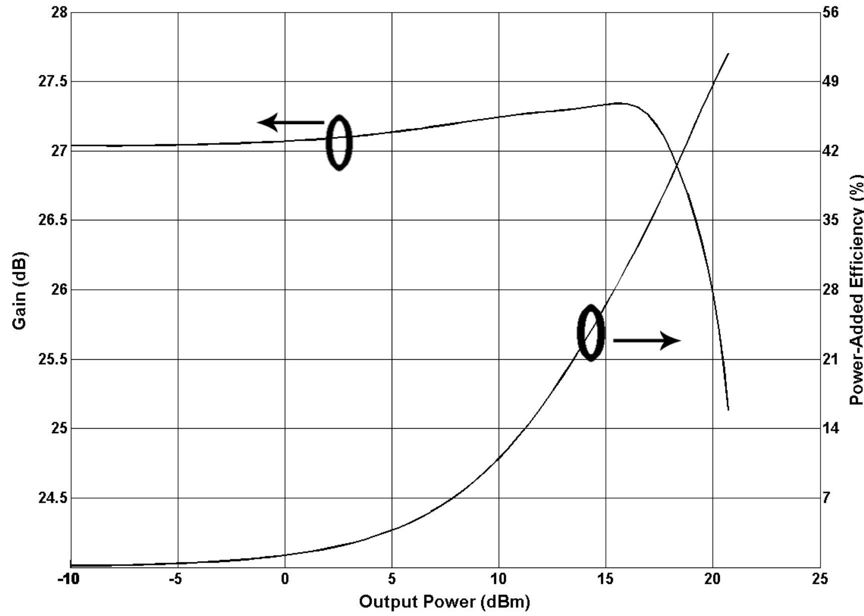


Figure 6.19: Final amplifier's gain and efficiency.

6.5 Broadband Linearizing GaN Amplifier

The gain expansion behavior can be used for designing linearizing driver amplifiers for broadband applications. To verify applicability of the proposed linearizer, a broadband current-biased amplifier was designed as a linearizer for a broadband power amplifier. The broadband voltage-biased power amplifier was designed using a 25-Watts GaN transistor from Cree Inc.,

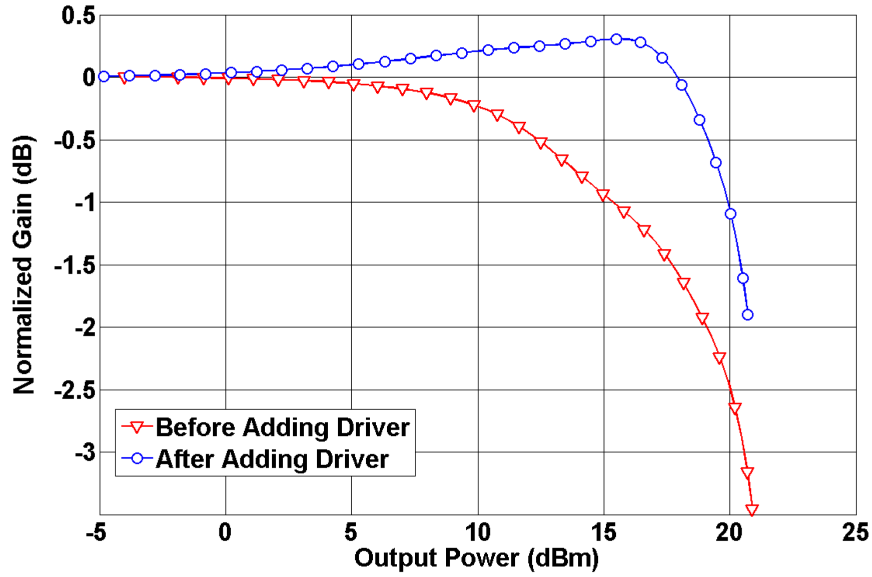


Figure 6.20: Gain profile before and after adding the driver amplifier.

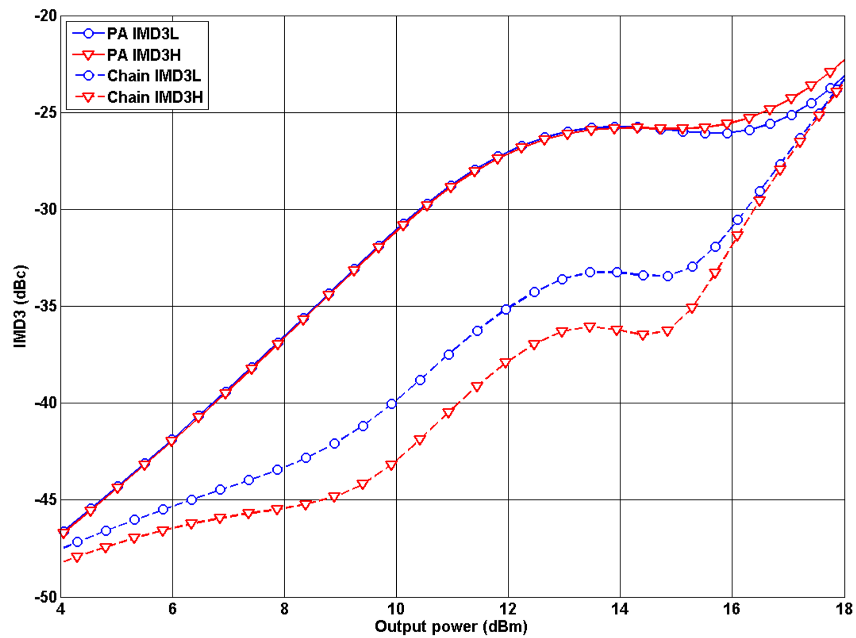
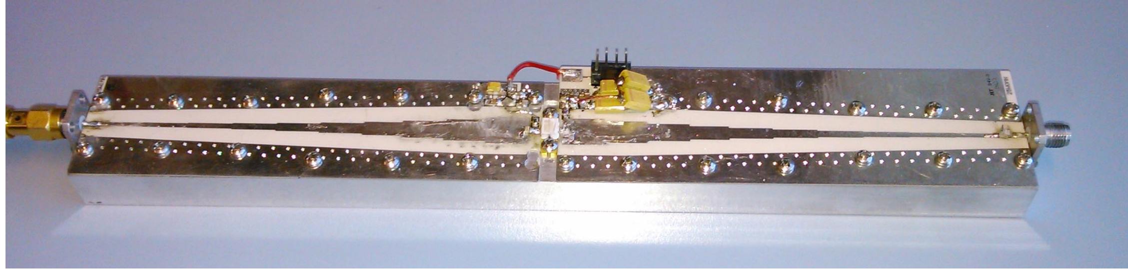
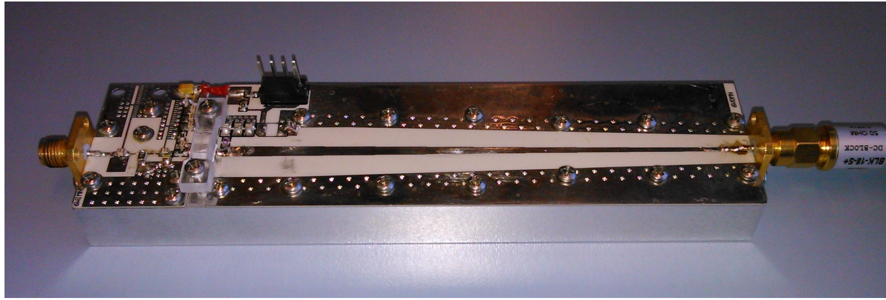


Figure 6.21: Power amplifier and chain third order intermodulation levels.



(a)



(b)

Figure 6.22: Photograph of (a) Broadband, 20 watt GaN power amplifier, (b) Broadband current-biased GaN linearizing driver

having part number of CGH40025F. The amplifier was designed in the frequency band of 1-2 GHz. The power amplifier's photograph is shown in Fig. 6.22a. The power amplifier was biased in drain voltage of 32 V and drain bias current of 200 mA. As can be seen from the measurement results shown in Fig. 6.23 (red traces), the power amplifier presents around 2-3 dB of gain compression at the output power of 43 dBm (20 watts). For this power amplifier, the output power at 1 dB compression point varies from 26 dBm to 38 dBm over the operating frequency band.

A current-biased amplifier was designed to decrease the amount of gain compression of the power amplifier. The driver amplifier was designed for the frequency band of 1-2 GHz using a 6-watt GaN transistor from Cree Inc., having part number of CGH40006P. The driver amplifier was biased at the drain current of 350 mA and drain voltage of 4.5 V. The photograph of the driver amplifier is shown in Fig. 6.22b.

The gain versus output power is shown for the cascaded amplifiers in Fig. 6.23 (blue traces). As can be seen from Fig. 6.23, after adding the current-biased driver amplifier, the

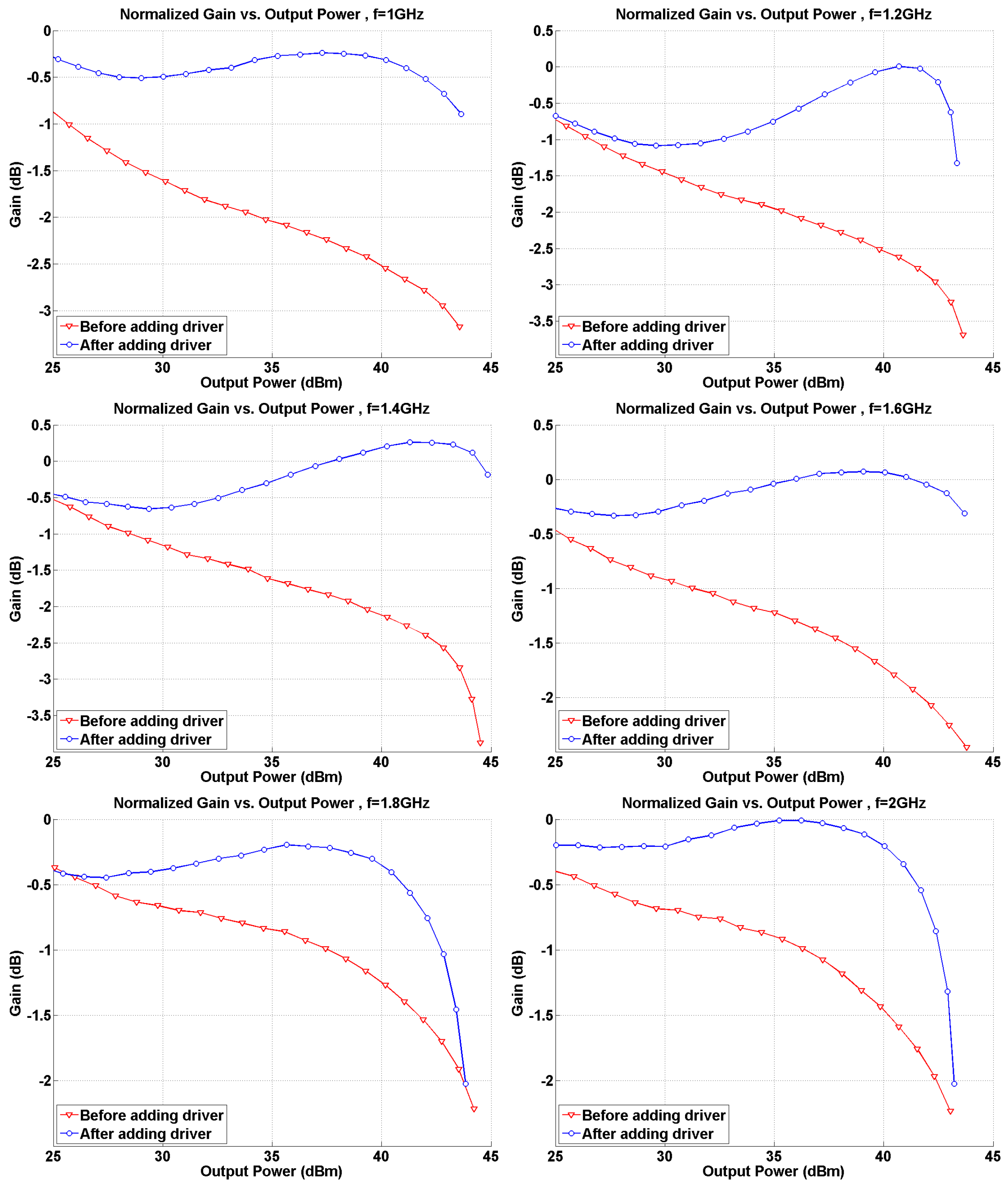


Figure 6.23: Gain versus output power before and after adding the current-biased driver amplifier.

output power at 1 dB compression is higher than 42.5 dBm over the entire frequency band of 1-2 GHz. The measurement results confirm that the gain expansion in current-biased transistors can be used to compensate for the gain compression of power amplifiers in a large frequency bandwidth.

6.6 Comparison of the Proposed Linearizer with Other Analog Pre-Distorters

There are different types of analog pre-distorters in the literature [39–47]. There are mainly two families of analog pre-distorters. The first type of analog pre-distorters use a feedforward loop and inject a distortion signal to cancel out the distortion generated by the nonlinear power amplifier. Another type of pre-distorters generate the opposite characteristics of the PA such that the combined performance of the pre-distorter and power amplifier represent a linear system. The proposed linearizer in this chapter can be classified as the second type of analog pre-distorters.

In [39–41], a feedforward loop is used to compensate for the intermodulation products. In the feedforward loop, the original signal is subtracted from the output of the power amplifier to obtain the pre-distorted signal. Then the distortions are added to the output of the power amplifier with proper phase to cancel the distortions generated by the power amplifier. In these types of analog pre-distorters, a feedforward loop, error amplifiers, attenuators, delay lines and phase-shifters are required. Also the system has to be calibrated for proper operation. The use of error amplifier causes efficiency degradation for the whole system [40].

In [42], a diode based circuit is used to generate the inverse AM-AM characteristics of the power amplifier It can compensate for the small gain expansion that is observed in some power amplifiers as well as the gain compression of the power amplifiers. The pre-distorter presents a high value of loss added to the amplifier chain, which means that the driver stage has to provide higher output power to be able to drive the power amplifier to its maximum input power.

In [43], another diode-based pre-distorter is proposed for linearization of Doherty amplifiers. It consists of a nonlinear diode circuit, an amplifier, a phase shifter and an attenuator to compensate for the nonlinearities of the power amplifier. This pre-distorter also needs tuning for optimal performance. In [44], the idea of [43] is used in a multi-branch linearizer to compensate for memory effects generated by the power amplifier. Adding more branches adds more complexity in the implementation and performance optimization of the pre-distorter. In [45], the nonlinear diode circuit of [44] is replaced by transistor-based circuits in each branch which makes the optimization process even more complex.

In [46], a diode-based analog pre-distorter is used to linearize a broadband power amplifier, however the pre-distorter can operate in a narrow bandwidth due to the difference between the characteristics of the diode and the power amplifier.

In [47], a CMOS pre-distorter is proposed using a transistor with zero DC bias on the transistor's drain. The transistoris biased at gate and the nonlinear behavior of the drain-source resistance and capacitance generate the nonlinearity required at the input of the power amplifier. The nonlinear behavior can be optimized using the gate-source bias.

The proposed linearizer in this dissertation is an amplifier that can be used as the driver amplifier. It means that the linearizer can be used both as the pre-distorter as well as the driver amplifier which means by using the proposed amplifier, no additional circuit is added to the system. The only additional circuit needed for the proposed circuit is the constant current source for biasing the linearizing driver amplifier. As it was shown in previous section, the proposed pre-distorting amplifier can be implemented in very large bandwidth while feedforward and diode/transistor-based pre-distorters can be usually designed for narrow bandwidth. Finally, since the proposed linearizer acts like the driver amplifier, additional DC power consumption is not imposed to the system while in feedforward or transistor pre-distorters which need DC power, the DC power consumed by the pre-distorter degrades the efficiency performance of the transmitter system. Table 6.1 provides a comparison of the

Reference	Technique	Complexity	RF loss	Memory effect	Bandwidth
[39–41]	Feedforward loop	Very high	Low	No	Very narrow
[42]	Diode-based	Moderate	High	No	Narrow
[43]	Diode-based	High	None	No	Narrow
[44]	Diode-based multi-branch	Very High	None	Yes	Very Narrow
[45]	Transistor-based multi-branch	Very high	None	Yes	Very narrow
[46]	Diode-based	Low	N/A	No	Narrow
[47]	Transistor-based circuit	Low	N/A	No	N/A
Proposed pre-distorter	Current-biased amplifier	Low/ Moderate	None	No	Very wide

Table 6.1: Comparison of the proposed pre-distorter with other analog pre-distorters.

proposed linearizing amplifier with other pre-distortion techniques.

Chapter 7

Conclusion and Future Work

In this chapter, the conclusion pf the dissertation is presented in Section 7.1 and the future works and final remarks are given in Section 7.2.

7.1 Conclusion

Energy efficiency is one of the most important parameters for an RF power amplifier. In portable devices, higher efficiency means longer battery life. For base stations, higher efficiency means lower energy cost and more importantly, lower greenhouse gas generation and greener environment. To have more flexible transmitter systems, broadband RF power amplifiers are needed. Having broadband power amplifiers allows the wireless transmitter to work in different frequency bands and different standards. In this dissertation, different amplifier architectures are proposed for designing broadband and energy efficient power amplifiers.

In Chapter 3, the Transformer-Less Load-Modulated (TLLM) amplifier is introduced. The TLLM amplifier uses the load modulation similar to the Doherty amplifier, but it does not need an output power combiner. A complete analysis and design procedure was introduced in Chapter 3 for designing the output matching networks for the main and peaking amplifiers. Two-sided matching technique was introduced to design the peaking amplifier's output matching network. Two-point matching was also introduced design the main amplifier's output matching network. By applying the two-sided and two-point matching techniques, the two amplifiers can be connected directly together without the need for any power combiner. A complete design procedure for designing broadband TLLM amplifiers was also given in Chapter 3.

Three implementations of the TLLM amplifier were presented in Chapter 3. The measurement results for a wideband TLLM amplifier was presented using the same transistors in both branches. Using different transistor sizes, it was shown that the TLLM amplifier can be implemented in very large bandwidth. Due to minimal number of elements used in the TLLM amplifier, it is suitable for designing high efficiency amplifiers in mmW frequency range. This was verified by another TLLM design in 60 GHz frequency band in CMOS technology.

In Chapter 4, a Doherty amplifier was proposed utilizing three-port input/output networks. The proposed amplifier is a generalization of the TLLM and Doherty amplifiers which provides more flexibility in the design and can be applied easily to many design cases. In fact the Doherty and TLLM amplifiers can be considered as a special case of the proposed amplifier. The proposed three-port output network is a power combining and matching network simultaneously. It can be designed for any output power ratio from the two branches and any arbitrary complex load impedance. The proposed input network is a power dividing and matching network that can be designed for any arbitrary complex source impedance, any arbitrary power division ratio and any arbitrary phase difference between the transistor input ports.

A complete analysis and design procedure is given in Chapter 4 for designing three-port input and output networks. Using the proposed three-port networks, there is no need for any offset lines at the input or the output of the amplifier since the input and output networks guarantee optimal operation.

In Chapter 5 a new biasing technique is proposed for RF transistors that utilizes a constant current source instead of the conventional constant voltage sources. Using this type of bias, new classes of operation are introduced. In Chapter 5, first the feasibility of high efficiency current sources is discussed, then one important application of the current biased transistors is introduced. It was shown that using a current-biased transistor in a

multi-branch amplifier Doherty-like efficiency performance can be obtained in a very large frequency bandwidth. To verify the idea, the measurement results for a broadband amplifier prototype based on the proposed architecture is presented.

In Chapter 6 another application of the current biased transistors is introduced. Since there are very well-established relations for CMOS technology, a complete analysis for a current biased MOSFET transistor was given utilizing the MOSFET I-V characteristics. It was shown that if the transistor is biased in triode region using a current source, depending on the bias point and loading condition it shows a certain amount of gain expansion. The amount of gain expansion can be as high as 15 dB and it can be controlled by the bias point and loading condition. A complete design procedure for designing an amplifier with predefined maximum output power and gain expansion is provided. As a proof of concept for the analysis and design procedure, the simulation results for a CMOS amplifier is presented. The designed amplifier is a two-stage amplifier. The driver amplifier is a current-biased amplifier providing gain expansion that compensates for the gain compression of the power amplifier. Finally, the measurement results for a broadband amplifier chain consisting of a current-biased GaN driver amplifier and a voltage biased GaN power amplifier was presented to show its applicability in other technologies.

Table 7.1 summarizes the performance of each proposed structure compared to the Doherty amplifier. The TLLM amplifier provides the same efficiency performance as the Doherty amplifier. It also provides the same degree of flexibility as the Doherty amplifier, but it can be be implemented in a much larger bandwidth compared to the Doherty amplifier. The Doherty amplifier with three-port input and output networks has the same performance as the Doherty amplifier in terms of efficiency and frequency bandwidth, but it provides a lot of flexibility for designing high efficiency amplifiers. The Doherty-like amplifier with current-biased main branch can provide the same efficiency performance compared to the Doherty amplifier in a very large frequency band due to the behavior of the current-biased transistor.

Amplifier structure	Flexibility	Efficiency improvement	Frequency bandwidth
Conventional Doherty	Moderate	High	Low/Moderate
TLLM	Moderate	High	High
Three-port I/O Doherty	Very high	High	Low/Moderate
Current-biased Doherty	Moderate	High	Very high
Current-biased linearizer	Moderate/High	Moderate	Very high

Table 7.1: Comparison of the proposed structures in this dissertation.

Finally, the gain expansion of the current-biased amplifiers can be used to compensate for the gain compression of the conventional power amplifiers. This will allow to drive the power amplifiers in more saturation and obtain higher efficiency from the power amplifier.

In summary, in this dissertation different amplifier architectures are proposed for broadband and high efficiency power amplifiers. The contributions made in this thesis are as follows:

- The TLLM amplifier structure is proposed for designing broadband high efficiency power amplifiers. Different power amplifiers were designed and fabricated in the RF and mmW frequency range to show the applicability of the proposed TLLM architecture in different frequencies and applications. Similar to the Doherty amplifier, the TLLM amplifier works based on load modulation and provides high efficiency at power back-off, but It does not utilize a power combiner at the output. In TLLM amplifier, the two amplifiers are connected directly together at the output without any power combiner network. It also does not utilize an impedance inverter nor the offset lines that is used in the Doherty amplifier and consequently can provide Doherty-like performance in a large frequency band.

- A generic topology and design procedure for Doherty amplifier with three-port input and output networks is proposed in the dissertation. The proposed

topology and design procedure can be used to design Doherty amplifiers with any transistors in the branches having any combination of power ratios and any arbitrary complex source and load impedances. Using the proposed architecture, the amplifier can be designed for any complex-valued source or load impedances. At the input port of the proposed amplifier, the power divider, the phase compensation elements and the matching networks are all integrated in one three-port input matching/dividing network. At the output port of the proposed amplifier, the power combiner, the offset lines and the matching networks are all integrated in the three-port output matching/combining network which minimizes the losses associated to the matching elements.

Two Doherty amplifiers were designed and fabricated based on the proposed topology and design procedure and the measurement results verified the performance of the proposed architecture and design procedure.

- A new biasing is proposed for the RF transistors that introduces new classes of operations and new features from RF transistors. The new biasing utilizes a current source power supply instead of the conventional voltage source. It is shown that by using this new biasing scheme, the transistors present new behaviours that can be used for new applications.

- By utilizing the new biasing technique, an amplifier architecture was proposed that provides high efficiency over very large frequency bandwidth. Based on the proposed architecture, a broadband amplifier was designed, fabricated and tested which verified the applicability of the proposed architecture for high efficiency broadband amplifiers. To the best of our knowledge, the fabricated prototype has the largest bandwidth compared to the reported amplifiers having high efficiency at power back-off so far.

- When the transistors are biased with conventional voltage source biasing, the amplifier gain decreases by increasing output power. In this dissertation it was shown that by using the proposed current biasing for the transistors, the amplifiers exhibit gain expansion by increasing the output power which is the opposite of the conventionally biased amplifiers. A complete analysis is provided in the dissertation for the MOSFET transistors and an amplifier chain was designed and simulated to show the linearization capability of the current biased amplifiers.

7.2 Future Work

The proposed structures in this dissertation can be extended or improved as follows:

The proposed characterization procedure for the Doherty amplifier with three-port input and output networks is generic and can be repeated at different frequency points for a device. By repeating the procedure, the S-parameters of the input and output networks can be obtained over a frequency bandwidth. However, synthesizing a broadband three-port network can be challenging. As a future work, study of broadband synthesis of three-port networks can be done for broadband and flexible Doherty amplifiers with three-port input and output networks. One circuit topology was proposed in Chapter 4 for synthesis of three-port networks, but other topologies and configurations can be studied for broadband implementation.

In Chapter 4, it was also shown that there are multiple solutions for the S-parameter matrix that meet the design goals. There are some parameters that can be selected by the designer to achieve additional design goals. As a future work, study of these parameters and their effects on other design criteria can be done. For example, these parameters can be used for harmonic tuning, bandwidth enhancement, gain improvement and realizability of the networks.

In Chapter 5, the idea of biasing transistor with constant current power supplies is proposed and in Chapter 6 an analysis of the current-biased transistor's current and voltage waveforms was presented for resistive loads. As the future work, the analysis can be extended for other working conditions such as different harmonic loading and different bias points. On the other hand, it was shown that bias feedback may be needed when biasing transistors with a current source. The bias feedback may change the transistor's behavior since the output DC voltage is dependent on the input power to the amplifier. The analysis of transistor's behavior can be done in presence of bias feedback as a future work.

In Chapter 6, the gain expansion of the current-biased transistor is used for compensating the gain compression of the conventional power amplifiers. As a future work, the gain expansion can be used to design other types of linearizers by using other circuit structures and topologies. Also the gain expansion behavior can be used for designing other types of load-modulated amplifiers. Study of these new structures can be done as the future work.

Appendix A

S-parameters with Complex Reference Impedances

DEFINITION

Consider the general n-port network N, shown in Fig. A.1 having complex valued reference impedance of Z_k for its k_{th} port. The incident and reflected wave vectors are defined as [60, 63]:

$$\mathbf{a} = \mathbf{R}(\mathbf{V} + \mathbf{ZI}) \tag{A.1}$$

$$\mathbf{b} = \mathbf{R}(\mathbf{V} - \mathbf{Z^{T*}I}) \tag{A.2}$$

In (A.1) and (A.2), $\mathbf{a}$,$\mathbf{b}$,$\mathbf{V}$ and $\mathbf{I}$ are $n \times 1$ vectors representing the incident and reflected waves and voltage and currents at the ports of the network respectively. $\mathbf{R}$ and $\mathbf{Z}$ are diagonal matrices whose k_{th} diagonal components are given by $1/\left(2\sqrt{Re(Z_k)}\right)$ and Z_k respectively.

Using these definitions, the incident and reflected waves at the k_{th} port of the network

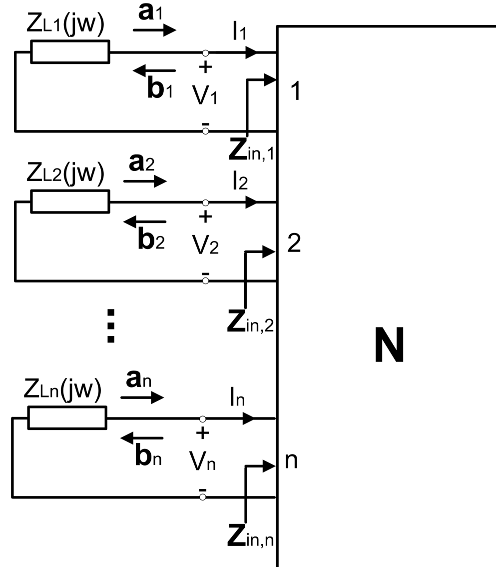


Figure A.1: General n-port network

can be written as [60–64]:

$$a_k = \frac{V_k + Z_k I_k}{2\sqrt{Re(Z_k)}} \tag{A.3}$$

$$b_k = \frac{V_k - Z_k^* I_k}{2\sqrt{Re(Z_k)}} \tag{A.4}$$

The $n \times n$ generalized scattering matrix $\mathbf{S}$ of N normalized to the impedances $Z_1, Z_2, \ldots, Z_n$ is defined as [60]:

$$\mathbf{b} = \mathbf{S}\mathbf{a} \tag{A.5}$$

DEPENDENCE ON THE DIRECTION

The selection of complex reference impedances is based on power waves [63]. Extra caution should be taken when using the complex reference impedances otherwise unwanted and inaccurate results may be observed [81].

As an example, the reflection coefficient of the loads connected to the network ports are calculated as:

$$\Gamma_{L,k} = \frac{a_k}{b_k} = \frac{V_k + Z_k I_k}{V_k - Z_k^* I_k} = \frac{V_k/I_k + Z_k}{V_k/I_k - Z_k^*} = \frac{Z_{L,k} - Z_k}{Z_{L,k} + Z_k^*}, \qquad k = 1, 2, \ldots, n \tag{A.6}$$

The reflection coefficient looking into the k_{th} port will be calculated as:

$$\Gamma_{in,k} = \frac{b_k}{a_k} = \frac{V_k - Z_k^* I_k}{V_k + Z_k I_k} = \frac{V_k/I_k - Z_k^*}{V_k/I_k + Z_k} = \frac{Z_{in,k} - Z_k^*}{Z_{in,k} + Z_k}, \qquad k = 1, 2, \ldots, n \tag{A.7}$$

As can be seen from (A.6) and (A.7), the equation used to calculate the reflection coefficient depends on the direction we need to calculate the reflection coefficient for. The reference impedance used to calculate the reflection coefficient of the load is Z_k and the reflection coefficient used to calculate the reflection coefficient of the network is Z_k^*. In fact an interconnection is transparent (an interconnection that does not cause any reflection) to a power wave when the impedance seen from the two directions of the interconnection are complex conjugate of each other; otherwise a part of the power wave will bw reflected from the interconnection.

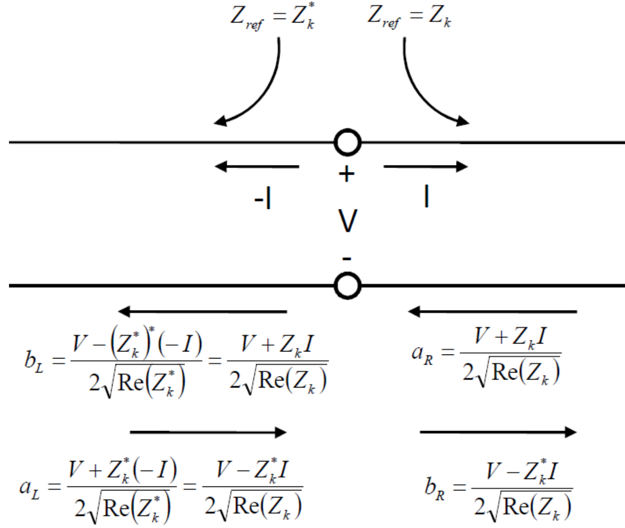


Figure A.2: Continuity of power waves in a transparent junction

Equation (A.6) shows that if the load connected to the port k is Z_k then its reflection coefficient will be zero. On the other hand the reflection coefficient seen from the network is zero when the output impedance at port k is equal to Z_k^*.

In [81] it is stated that in a transparent interconnection, the power waves are not continuous. This conclusion is based on using the same reference impedance for calculation of power waves for both directions. It is known [82] that the continuity holds when the reference impedances for the two directions are complex conjugate of each other. A transparent interconnection is shown in Fig. A.2. Using (A.3) and (A.4), the power waves at the interconnection are calculated with proper reference impedances and shown in Fig. A.2. As can be seen from the calculated power waves, $a_L = b_R$ and $b_L = a_R$ which confirms continuity of the power waves in a transparent interconnection.

CONVERSION TO IMPEDANCE AND ADMITTANCE MATRICES

Referring to Fig. A.1, the impedance matrix $\mathbf{Z_N}$, and admittance matrix $\mathbf{Y_N}$ of the n-port network N are defined as:

$$\mathbf{V} = \mathbf{Z_N}\mathbf{I} \tag{A.8}$$

$$\mathbf{I} = \mathbf{Y_N V} \tag{A.9}$$

For an n-port network, the S-parameter matrix depends on the set of reference impedances chosen for the ports, but the impedance and admittance matrices are unique. The relation between generalized scattering matrix and the impedance matrix is given in the following equations [60]:

$$\mathbf{S} = \mathbf{R}(\mathbf{Z_N} - \mathbf{Z^{T*}})(\mathbf{Z_N} + \mathbf{Z})^{-\mathbf{1}}\mathbf{R}^{-\mathbf{1}} \tag{A.10}$$

$$\mathbf{Z_N} = \mathbf{R}^{-\mathbf{1}}(\mathbf{I_n} - \mathbf{S})^{-\mathbf{1}}(\mathbf{SZ} + \mathbf{Z^{T*}})\mathbf{R} \tag{A.11}$$

In (A.10) and (A.11), $\mathbf{Z^{T*}}$ is the conjugate transpose of $\mathbf{Z}$ and $\mathbf{I_n}$ is the identity matrix of size n.

CHANGE OF REFERENCE IMPEDANCES

The scattering parameters can be defined by selecting a set of reference impedances. In some occasions it is necessary to change the set of reference impedances. By changing the set of reference impedances, the elements of the scattering matrix will change. It should be noted that even changing the reference impedance for one port may affect all of the elements in the $\mathbf{S}$ matrix.

Suppose the initial reference impedances $Z_1, Z_2, \ldots, Z_n$ are selected to calculate $\mathbf{S}$. If the reference impedances are changed to $Z'_1, Z'_2, \ldots, Z'_n$, then the new scattering matrix $\mathbf{S}'$ will be different than $\mathbf{S}$. The new scattering matrix $\mathbf{S}'$ can be calculated from $\mathbf{S}$ as [60]:

$$\mathbf{S}' = \mathbf{A}^{-\mathbf{1}}(\mathbf{S} - \mathbf{\Gamma^{T*}})(\mathbf{I_n} - \mathbf{\Gamma S})^{-\mathbf{1}}\mathbf{A^{T*}} \tag{A.12}$$

Where $\mathbf{A}$ is a diagonal matrix defined by:

$$\mathbf{A} = \mathbf{R}'^{-\mathbf{1}}\mathbf{R}(\mathbf{I_n} - \mathbf{\Gamma^{T*}}) \tag{A.13}$$

and:

$$\mathbf{\Gamma} = (\mathbf{Z}' - \mathbf{Z})(\mathbf{Z}' + \mathbf{Z^{T*}})^{-\mathbf{1}} \tag{A.14}$$

The i_{th} diagonal element of **A** is given by:

$$A_{ii} = |1 - \Gamma_i|^{-1}(1 - \Gamma_i^*)(1 - |\Gamma_i|^2)^{1/2} \tag{A.15}$$

where:

$$\Gamma_i = \frac{Z_i' - Z_i}{Z_i' + Z_i^*} \tag{A.16}$$

Appendix B

Apollonius Representation of Circles in Complex Plane

DEFINITION

The Apollonius representation of a circle is shown in Fig. B.1.

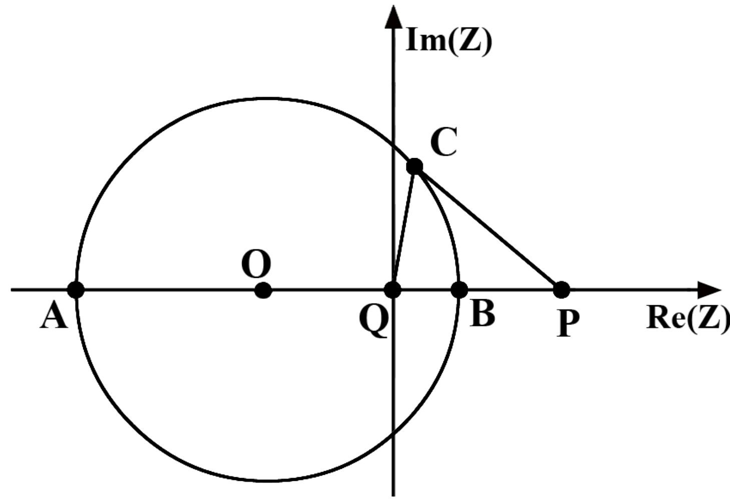


Figure B.1: Apollonius circle

Referring to B.1, in Apollonius definition, a circle is the set of points **C** that have a given ratio of distances from two fixed points **P** and **Q**. In other words, for any point **C** on the circle one can write:

$$\left|\frac{CQ}{CP}\right| = \alpha \tag{B.1}$$

P and **Q** are two fixed points called the foci of the circle.

CENTER AND RADIUS

To find the center and radius of the circle, by selecting the coordinate system shown in Fig. B.1, $Q = 0$ and one can write:

$$\left|\frac{A-Q}{A-P}\right| = \left|\frac{B-Q}{B-P}\right| = \alpha < 1 \rightarrow \frac{-A}{P-A} = \frac{B}{P-B} = \alpha \rightarrow \begin{cases} A = \dfrac{P\alpha}{\alpha-1} \\ \\ B = \dfrac{P\alpha}{\alpha+1} \end{cases}$$

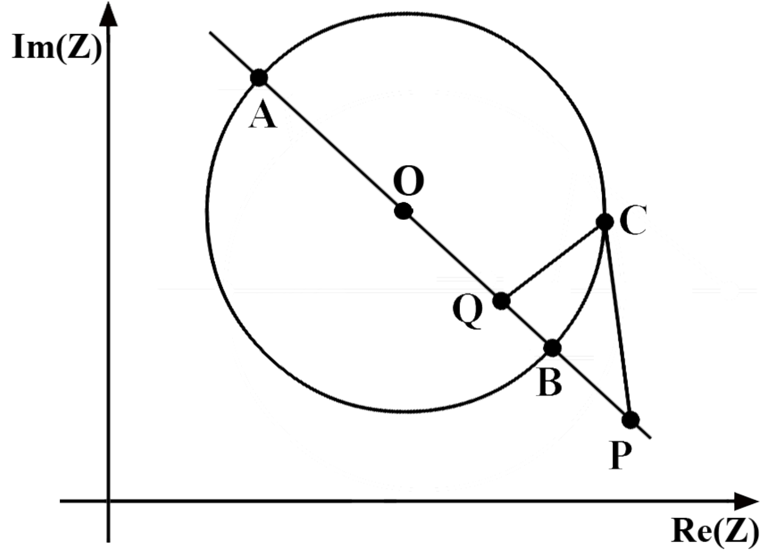


Figure B.2: General Apollonius circle

$$O = \frac{A + B}{2} = \frac{P\alpha^2}{\alpha^2 - 1} \tag{B.2}$$

$$r = \left| \frac{A - B}{2} \right| = \frac{P\alpha}{1 - \alpha^2} \tag{B.3}$$

In a more general case which $Q \neq 0$ (Fig. B.2), equations (B.2) and (B.3) can be expressed as:

$$O = \frac{(P - Q)\alpha^2}{\alpha^2 - 1} + Q \tag{B.4}$$

$$r = \frac{|P - Q|\alpha}{1 - \alpha^2} \tag{B.5}$$

CIRCLES UNDER BILINEAR TRANSFORMATION

Consider a circle defined in complex Z plane by:

$$|Z - Z_0| = r_z \tag{B.6}$$

The Z plane is transformed into the S plane with the bilinear transformation:

$$S = \frac{aZ + b}{cZ + d} \tag{B.7}$$

In (B.7), the parameters a, b, c and d are constant complex numbers. To find the transformation of circle defined in (B.6), we can write:

$$Z = \frac{dS - b}{a - cS} \tag{B.8}$$

$$|Z - Z_0| = \left| \frac{S(d + cZ_0) - (b + aZ_0)}{a - cS} \right| = r_z \tag{B.9}$$

$$\left| S - \frac{b + aZ_0}{d + cZ_0} \right| = \frac{r_z |c|}{|d + cZ_0|} \left| S - \frac{a}{c} \right| \tag{B.10}$$

Equation (B.10) can be written as:

$$|S - X| = Y|S - W| \tag{B.11}$$

$$W = \frac{a}{c}, \qquad X = \frac{aZ_0 + b}{cZ_0 + d} \qquad Y = \frac{r_z |c|}{|cZ_0 + d|} \tag{B.12}$$

Equation (B.12) is the Apollonius representation of a circle with center and radius of:

$$S_0 = \frac{(W - X)Y^2}{Y^2 - 1} + X \tag{B.13}$$

$$r_s = \frac{|W - X|Y}{1 - Y^2} \tag{B.14}$$

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