A 10–Bit 1.6-GS/s 27-mW Current-Steering D/A Converter With 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS

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***Abstract*—This paper presents a 10-bit 5-5 segmented current-steering digital-to-analog converter implemented in a standard 130-nm CMOS technology. It achieves full-Nyquist performance up to 1 GS/s and maintains 54-dB SFDR over a 550-MHz output bandwidth up to 1.6 GS/s. The power consumption for a near-Nyquist output signal sampled at 1.6 GS/s equals 27 mW. To enable the presented performance a design strategy is proposed that introduces a switch-driver power consumption aware analysis of the switched current cell. The analysis of the major distortion mechanisms in the switched current cell allows the derivation of a design strategy for maximum linearity. This strategy is extended to include the power consumption of the switch drivers in function of the switched current cell design. To minimize the digital power consumption, low-power implementations of the thermometer decoder and switch driver circuits are introduced.**

***Index Terms*—ACS320, digital to analog converters.**

I. Introduction

THE continuous evolution towards higher levels of integration in communication systems drives the need for high-performance data converters implemented in low-cost nanometer CMOS technologies. As increasing number of applications are powered through batteries or low-power links such as power-over-Ethernet, the energy efficiency of the components in such systems becomes ever more important. This efficiency is a second driver for the use of downscaled technologies as it has a dramatic impact on the power consumption of the digital section of the system.

For current-steering digital-to-analog converters (DACs), however, technology scaling introduces some challenges. The reduction of the gate oxide thickness limits the maximum voltage that can be applied to a device, while the threshold voltage scales only marginally. The design freedom with respect to voltage margin is therefore significantly reduced. This makes the design of high accuracy converters more difficult, even though scaled technologies provide better matching for equal area [1]–[3]. As the available overdrive voltage is reduced, the impact of V_T mismatch becomes more important. A second issue in nanometer CMOS technologies is the reduced voltage gain of the available transistors, impacting numerous distortion effects in current-steering converters.

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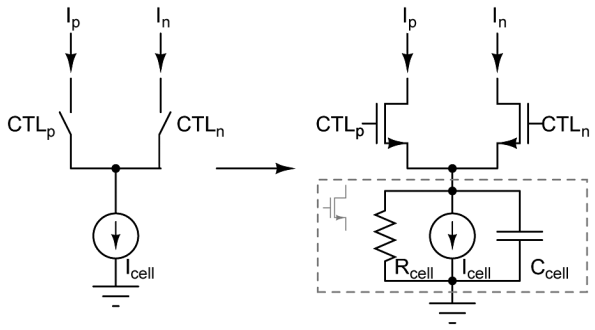

Fig. 1. Ideal switched current cell and the simple model employed for analysis. The nominal current I_{cell} is switched to the positive or negative output using a switch transistor, depending on the value of the control signals CTL_p and CTL_n. The major nonideal effects of the current source are lumped into resistor R_{cell} and capacitor C_{cell}.

The switched current cell, being the core of any current-steering D/A converter, has a significant impact on the distortion behavior of the converter. Therefore, the major distortion mechanisms caused by nonideal behavior of the current cell are analyzed in Section II. Section III will derive two strategies for the design of the current cell used. The first strategy focuses on maximizing high-frequency linearity, while the second one introduces power consumption into the equation. Section IV discusses the implementation of a high-speed 10-bit DAC for maximum power efficiency. The design of the low power thermometer encoder, the clock routing, and the switch drivers enabling the target dynamic linearity is described. The measurement results are summarized in Section V, along with a comparison to the state-of-the art to illustrate the effectiveness of the design strategy. Finally some conclusions are formulated.

II. Current Cell Induced Nonlinearity

A fundamental source of nonlinearity originates in the current cell: any deviation from ideal current cell behavior will result in spectral impurity. This section analyzes the current cell for spectral performance at both low and high output frequencies. The high target bandwidth prevents the use of an active output stage; therefore, the analysis is constrained to the current cell shown in Fig. 1.

In this simple model, the switched current cell consists of an ideal current source that is switched to either the positive or negative output by a switch transistor. The major nonideal effects of the current source are modeled by a finite frequency dependent impedance composed of resistor R_{cell} and capacitor C_{cell}.

Based upon this simple model the major linearity limitations of a current-steering DAC are discussed.

A. Low-Frequency Linearity and Static Matching

An upper limit to the distortion performance of the D/A converter is set by the phenomena that occur at low frequencies. In this paper all current-cell effects that are not caused by capacitances are considered low-frequency effects. These effects are usually described by their influence on the integral nonlinearity (INL). The static matching of the current sources sets an upper limit to the achievable INL and therefore also to the distortion performance of the D/A converter [4]. The matching error between the current cells consists of a random and a systematic component that both have to be tackled. The systematic mismatch component originates from, e.g., gradients in process parameters like doping or oxide thickness, temperature gradients, and supply wire resistance induced voltage drops [5], [6]. It can be overcome by employing appropriate switching schemes as described in [6]–[8] and/or by using calibration [9] or randomization [10].

The random component of the drain current error between two nominally equal transistors can, to first order, be described using the Pelgrom model [1], [6]

$$\sigma^2\left(\frac{\Delta I}{I}\right) = \frac{1}{WL}\left(A_\beta^2 + \frac{4A_{V_T}^2}{(V_{GS}-V_T)^2}\right) \tag{1}$$

in which A_β and A_{V_T} are technology-dependent matching constants; WL represents the area of the matched transistors, and $V_{GS}-V_T$ is their gate overdrive voltage. For a 10-bit converter a 99.7% yield specification at INL < 0.5 LSB requires a current error standard deviation of less than 0.5% [11].

As shown by (1) the mismatch error is mainly determined by the area used to implement the current source transistor. It also indicates that to ensure that threshold voltage mismatch does not dominate the total mismatch, the gate-source overdrive voltage of the current source transistor should be large. If a small overdrive voltage is used, for example, due to a small voltage headroom enforced by the technology, the area penalty due to matching requirements can become very high. As the area required for one current source determines the parasitic capacitance C_{cell} this can have a significant impact on high-frequency performance, even when cascoding is employed.

As the output resistance of the switched current cell is finite, the total output resistance of the DAC is dependent on the number of current cells connected to the output. Therefore, it is dependent on the input code. The code-dependent output current of the DAC is hence converted to a voltage over the parallel combination of the linear load resistor and the code-dependent DAC output resistance, resulting in distortion. The influence of cell impedance on the INL of the converter can be described using the following relation [12]:

$$INL \approx \frac{R_{load}N^2}{4R_{cell}}. \tag{2}$$

B. High-Frequency Linearity

Additional performance limiting effects start to occur when converting higher output frequencies. Already at modest frequencies these start to dominate the low frequency phenomena discussed in Section II-A.

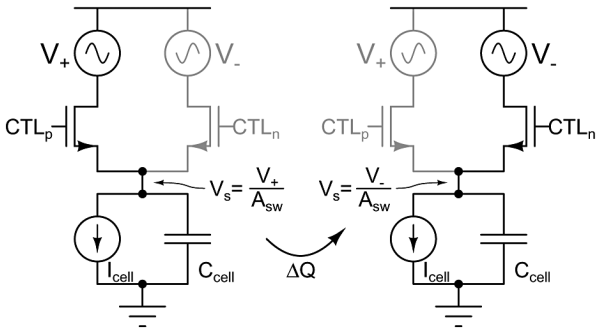

Fig. 2. Differential switching of the source node capacitance results in charge being transferred at every switch event. This results in a net current injected into the target output for which no corresponding current flows through the complementary output.

1) Nonlinear Capacitive Loading: A first high-frequency effect is strongly related to the output resistance effect leading up to (2). As frequencies increase, the capacitive portion of the cell impedance starts to dominate over the resistive part. The code-dependent DAC output impedance therefore drops for increasing frequencies, and hence the distortion increases. This effect has been analyzed extensively in [13] and [14], resulting in the following relation for the n^{th} harmonic:

$$HD_n = \left(\frac{N\,Z_L}{4Z_{cell}}\right)^{n-1} \tag{3}$$

in which the frequency-dependent unit cell impedance is represented by Z_{cell}. N equals the number of unit cells, and Z_L is the load impedance. For the model presented in Fig. 1 and assuming that R_{cell} is sufficiently big the output impedance of the cell can be approximated by

$$Z_{cell} \approx \frac{A_{sw}}{2\pi f\, C_{cell}}. \tag{4}$$

In this equation A_{sw} signifies the voltage gain of the current switch transistor. If this transistor operates in saturation its voltage gain is $A_{sw} = 1 + gm_{sw}ro_{sw}$. Using (4), (3) can be rewritten as [15]

$$HD_n = \left(\frac{\pi f Z_L C_{cell} N}{2A_{sw}}\right)^{n-1}. \tag{5}$$

Equations (3) and (5) indicate that the nth-order harmonic distortion component due to nonlinear capacitive loading increases $20(n-1)$ dB per decade.

2) Differential Capacitive Charge Transfer: Aside from its impact on the cell output impedance, the current source parasitic capacitance also impacts linearity through a second mechanism [15]. Fig. 2 illustrates the two possible states of the simplified current cell (neglecting R_{cell}): either the cell is connected to the positive output node, or it is connected to the negative output node. The output node voltages are defined to be at V_+ and V_-, respectively.

As the switches are operating in saturation, the voltage at the source node of the switches changes from $V_{s,DC}+(V_+/A_{sw})$ to $V_{s,DC}+(V_-/A_{sw})$ when switching the cell from output V_+ to

the complementary output V_-. The resulting charge difference on capacitor C_{cell} is

$$\Delta Q = \frac{V_+ - V_-}{A_{sw}} C_{cell}. \tag{6}$$

This charge difference can only be established by a corresponding current ΔI, which is superimposed on the current flowing through the target output. The current through the complementary output, however, is not affected by this charge difference as the cell is detached from it. The resulting imbalance introduces significant distortion in both single-ended and differential converters. The influence of this effect on the linearity of the total converter can be calculated using differential calculus [15]. When a single-tone sine wave is applied the following second- and third-order distortion components appear:

$$HD_2 = \frac{\pi f Z_L C_{cell} N}{2A_{sw}} \tag{7}$$

$$HD_3 = \frac{\pi f Z_L C_{cell} N}{4A_{sw}}. \tag{8}$$

C. A Combined Distortion Model for a Simple Current Cell

Comparison of (5) and (7) shows that the second-order distortion caused by the switched capacitor effect is exactly as large as the distortion caused by the output impedance alone. Since both nonlinear currents are in phase, the total second-order distortion magnitude becomes

$$HD_2 = \frac{\pi f Z_L C_{cell} N}{A_{sw}}. \tag{9}$$

The total third-order distortion is obtained by combining (5) and (8)

$$HD_3 = \frac{1}{4} \frac{\pi f Z_L C_{cell} N}{A_{sw}} \left(1 + \frac{\pi f Z_L C_{cell} N}{A_{sw}}\right). \tag{10}$$

It can be seen that for frequencies below

$$f = \frac{A_{sw}}{\pi Z_L C_{cell} N} \tag{11}$$

the source node capacitance switching effect (8) dominates the third-order distortion, while for higher frequencies the output impedance induced distortion is dominant. For practical designs the output frequency lies significantly below this transition frequency and (8) can be used to approximate HD_3.

D. The Cascoded Current-Source Cell

The preceding analysis has been performed for the simplified current cell model shown in Fig. 1. In most cases however it is not possible to design a sufficiently good current cell using only one transistor. First of all the output impedance of one single transistor is not high enough to meet the static output impedance requirements set by (2). Furthermore the large transistor area dictated by matching requirements results in very large parasitic capacitance, significantly deteriorating high-frequency linearity. To mitigate these effects cascoding is usually employed as it increases the output impedance both at dc and at high frequencies [13].

The question that arises when using one or more cascode transistors is whether the simple single-capacitor model is still valid, and what the relevant capacitances are. In general, (9) and (10) derived in Section II-C can be rewritten as [neglecting the second term in (10)]

$$HD_2 = \frac{Z_L N}{2Z_{cell}} \tag{12}$$

$$HD_3 = \frac{Z_L N}{8Z_{cell}}. \tag{13}$$

Fig. 3 illustrates the impedance plot of a single-cascode current cell. Five zones can be identified: zones 1, 3, and 5 are zones that can be described using a purely resistive cell impedance. As a result, the distortion performance of the DAC is not frequency-dependent in these zones. Zones 2 and 4 on the other hand exhibit capacitive behavior, and therefore, the DAC performance shows frequency dependence. The behavior in zone 2 is equivalent to the simple model from Fig. 1 with $R_{cell} = A_{casc} r o_{cs}$ and $C_{cell} = C_0/A_{casc}$. In zone 4 capacitor C_0 acts as a short circuit and completely dominates transistor M_{cs}. This zone can be modeled by using $R_{cell} = ro_{casc}$, $C_{cell} = C_1$ and $A_{eff} = A_{sw}$.

III. Design Strategy

The derivation of a design plan requires that the behavioral parameters of the different devices in the circuit are mapped on their physical implementation. Hence, a transistor model is required. For this section the simple square-law model given by (14) and (15) is used [16], [17]. The gate overdrive voltage $V_{GS} - V_T$ is denoted by V_{gst} and V_E is the Early voltage. While this model is not very accurate for deep-submicrometer technologies, it is still sufficient to derive the general design guidance as presented in this section.

$$I_{DS} = \frac{\mu C_{ox}}{2n} \frac{W}{L} V_{gst}^2 \tag{14}$$

$$gm = \frac{2I_{DS}}{V_{gst}}, \quad ro = \frac{V_E L}{I_{DS}}. \tag{15}$$

A. Design for Dynamic Performance

Based upon the analysis presented in Section II, a design plan for maximum dynamic linearity can be derived. First it should be ensured that the static mismatch of the current sources does not impose an upper bound on the achievable linearity [4]. Equation (1) indicates that the area of the current source array (CSA) can be traded off with transistor overdrive voltage for a given mismatch specification. Nevertheless even when using large overdrive voltage for the current source, the total device and parasitic wiring capacitance (C_0 in Fig. 3) will be large. A large C_0 means that zone 2 shifts to low frequencies. Therefore, the output linearity is mainly determined by the impedance in zone 3, while the output bandwidth is limited by the transition between zone 3 and zone 4.

Evaluating (13) in zone 3 results in

$$SFDR_{req} \approx \frac{1}{HD_3} = 4\frac{ro_{casc} A_{sw}}{Z_L N} = 4\frac{ro_{casc} gm_{sw} ro_{sw}}{Z_L N}.$$

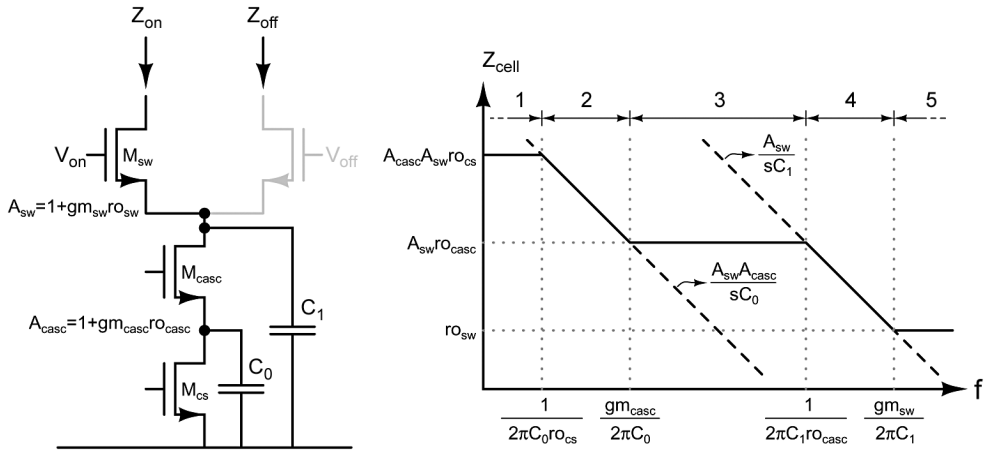

Fig. 3. Switched impedance $(Z_{on} - Z_{off})$ of a cascoded current cell with saturated switches. C_0 is assumed significantly larger than C_1 as it contains the wiring capacitance and the drain capacitance of the matched transistor M_{cs}.

As the peak-peak output voltage swing V_{out} is equal to $2NI_{cell}Z_L$, the SFDR in zone 3 becomes

$$SFDR_{req} \approx 4\frac{\frac{V_E L_{casc}}{I_{cell}}\frac{2V_E L_{sw}}{V_{gst,sw}}}{Z_L N} = 4\frac{V_E^2 L_{casc} L_{sw}}{V_{out} V_{gst,sw}}. \quad (16)$$

This equation indicates that the harmonic distortion decreases when increasing channel length of the cascode and the switch, or when the overdrive voltage of the switch is reduced. The $SFDR_{req}$-bandwidth is the transition between zone 3 and 4, and can be calculated to be

$$BW = \frac{1}{2\pi ro_{casc} C_1} = \frac{I_{cell}}{2\pi V_E L_{casc} C_1}. \quad (17)$$

When neglecting overlap capacitances, the source node capacitance is determined by the gate-source capacitance of the switch transistor and can be approximated by [16]

$$C_1 \approx \frac{2}{3} W_{sw} L_{sw} C_{ox}. \quad (18)$$

Considering the fact that the current switched is constant and given by I_{cell}, and using (14), the cell capacitance can be written as

$$C_1 \approx \frac{2}{3}\frac{2n}{\mu}\frac{I_{cell} L_{sw}^2}{V_{gst,sw}^2}. \quad (19)$$

Combining this with (17) yields

$$BW = \frac{1}{2\pi V_E}\frac{3}{2}\frac{\mu}{2n}\frac{V_{gst,sw}^2}{L_{casc} L_{sw}^2}. \quad (20)$$

This indicates that the maximum frequency is achieved when using large gate overdrive for the switch transistors, and by using minimum length for both the switch and the cascode. Combining (16) and (20) yields the relation between achievable SFDR-bandwidth and transistor parameters

$$BW = \frac{6\mu V_E^3}{\pi n}\frac{1}{V_{out}^2}\frac{1}{SFDR^2} L_{casc}. \quad (21)$$

This result indicates that the maximal SFDR bandwidth mainly depends on the technology parameters and the swing at the drain of the switches. If cascode parasitics can be neglected,

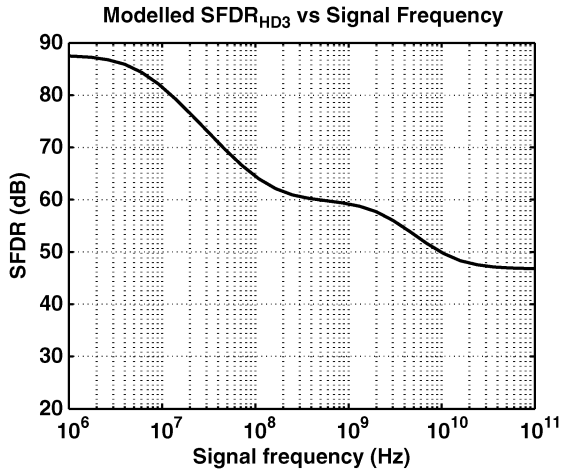

Fig. 4. SFDR according to (13) when using the switched Z_{cell} extracted from circuit simulations. The impedance in zone 3 determines the SFDR for most of the output bandwidth.

the only design parameter that affects the SFDR bandwidth of the converter is the length of the cascode transistor.

When considering the cascode gate-drain overlap capacitance the source node cell capacitance becomes

$$C_1 \approx \frac{2}{3} W_{sw} L_{sw} C_{ox} + W_{casc} C_{gdo} \quad (22)$$

in which C_{gdo} is the overlap capacitance per unit width.

This means that as long as $(2/3)W_{sw}L_{sw}C_{ox} \gg W_{casc}C_{gdo}$ the assumption that the oxide capacitance dominates holds. Using (14) this can be written as

$$L_{casc} \ll \frac{V_{gst,casc}^2}{V_{gst,sw}^2} L_{sw}^2 \frac{C_{ox}}{C_{gdo}}. \quad (23)$$

If L_{sw} is equal to the technology minimum-length L_{min} the gate-drain overlap capacitance C_{gdo} can be approximated by $(1/4)L_{min}C_{ox}$ [17], and (23) can be approximated by

$$L_{casc} \ll 4\frac{V_{gst,casc}^2}{V_{gst,sw}^2} L_{min}. \quad (24)$$

Note that wiring capacitance at the switch source node is neglected since it can be made very small through proper layout as shown in Section IV-A.

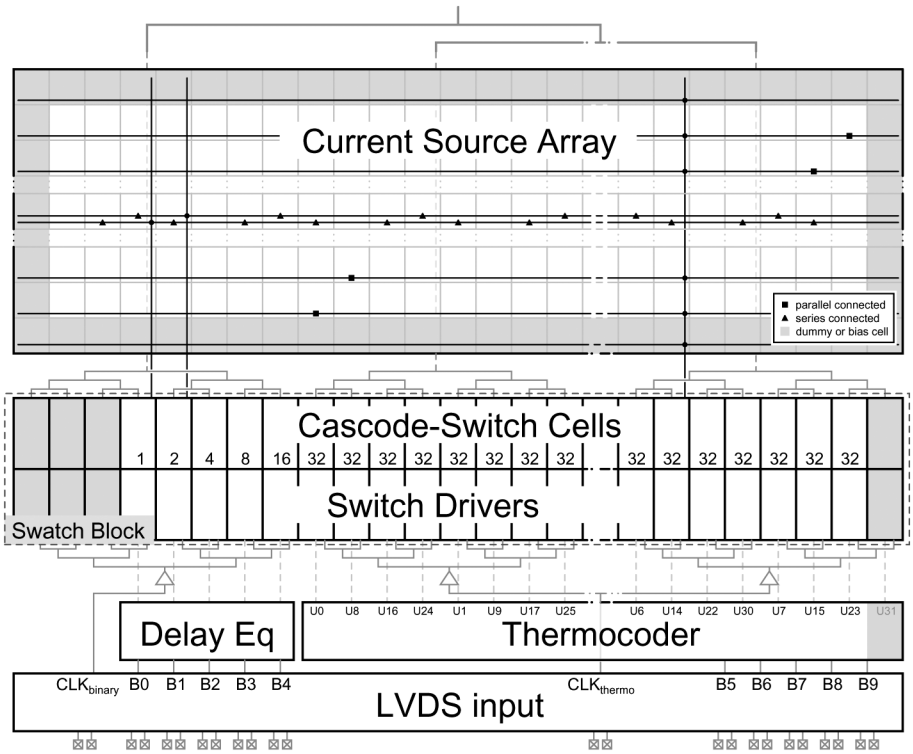

Fig. 5. Architecture of the current-steering DAC.

B. Design for Maximum Energy Efficiency

When designing a current-steering D/A converter for maximum energy efficiency, it is important to consider the impact of the current cell sizing on the power consumption of the entire system.

To simplify the calculations, the load presented by the current switch transistor is approximated by a linear capacitance proportional to the total oxide capacitance $W_{sw}L_{sw}C_{ox}$. As one switching operation encompasses turning one switch on and turning the complementary transistor off, the energy required for a switching operation is

$$E_{sw} \sim W_{sw}L_{sw}C_{ox}V_{drv}^2 \tag{25}$$

in which V_{drv} represents the output swing of the driver. Combined with (14) and the observation that $I_{cell} = I_{total}/2^B$ the switching energy becomes

$$E_{sw} \sim 2\frac{n}{\mu}\frac{I_{total}}{2^B}\left(L_{sw}\frac{V_{drv}}{V_{gst}}\right)^2. \tag{26}$$

For a near-Nyquist signal all cells are switching at a rate $F_{clk}/2$; therefore, the total power consumption can be approximated by $P = 2^B E_{sw}(F_{clk}/2)$, hence

$$P \sim 2\frac{n}{\mu}I_{total}\frac{F_{clk}}{2}\left(L_{sw}\frac{V_{drv}}{V_{gst}}\right)^2. \tag{27}$$

Equation (27) shows that the power consumption of the switch drivers is dependent on the total load current and independent of the number of cells. The design parameters that influence power consumption are the length of the current switch and the ratio between driver swing and switch overdrive voltage. For maximum energy efficiency of the driver section at a given load current, the switch transistors should have minimum length and maximum gate overdrive voltage. Aside from the reduction of intrinsic energy per transition, the reduced load also enables the use of smaller switch driver circuits, further reducing power.

C. Applied Design Strategy

The target specification for this design was to achieve a 54-dB differential SFDR bandwidth of 500 MHz for an output swing of 250 mV with minimal power consumption. The design was to be implemented in a 1.2-V, 130-nm technology and nonstandard devices (thick-oxide, triple-well) were not available.

To achieve low power consumption, the switches have minimum length as indicated by (27). Full-swing (1.2 V) drivers have been used as the design of low-swing drivers is far from trivial and can come at a large power cost [18]. When using full-swing drivers, the V_{gst} of the switches should be maximized for lowest power consumption.

According to (21) the cascode length should be maximized for maximum SFDR-bandwidth. On the other hand, (24) constrains the cascode length for (21) to be valid. It indicates that smaller cascode length will result in more headroom for the switches, allowing higher V_{gst} and therefore reducing lower power consumption. As power consumption should be minimized, minimum-length cascode transistors have been used. After both the switch and cascode length are chosen, their gate overdrive voltages can be set for minimum power consumption. This strategy yields a design that satisfies the specifications set forth while minimizing the power consumption of the DAC.

Fig. 4 shows the modeled SFDR when Z_{cell} extracted from circuit simulations of the current cell is plugged in to (13). It

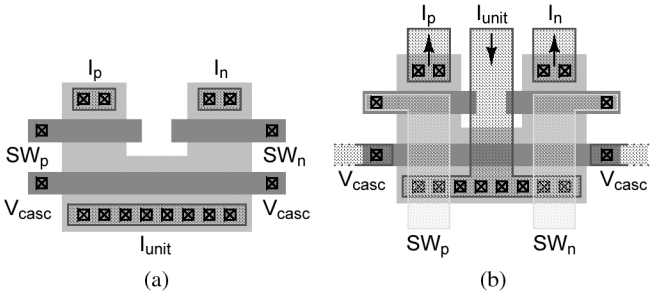

Fig. 6. Layout of the unit switched current cell for minimum source node capacitance. The switches and cascode are laid out such that no metal interconnect is used to connect the sources of the switches to the drain of the cascode. The elimination of diffusion contacts not only removes their intrinsic capacitance but also eliminates the associated clearance rules. This enables a very compact layout that makes the wiring capacitance neglectable. (a) Without metal interconnect. (b) With metal interconnect.

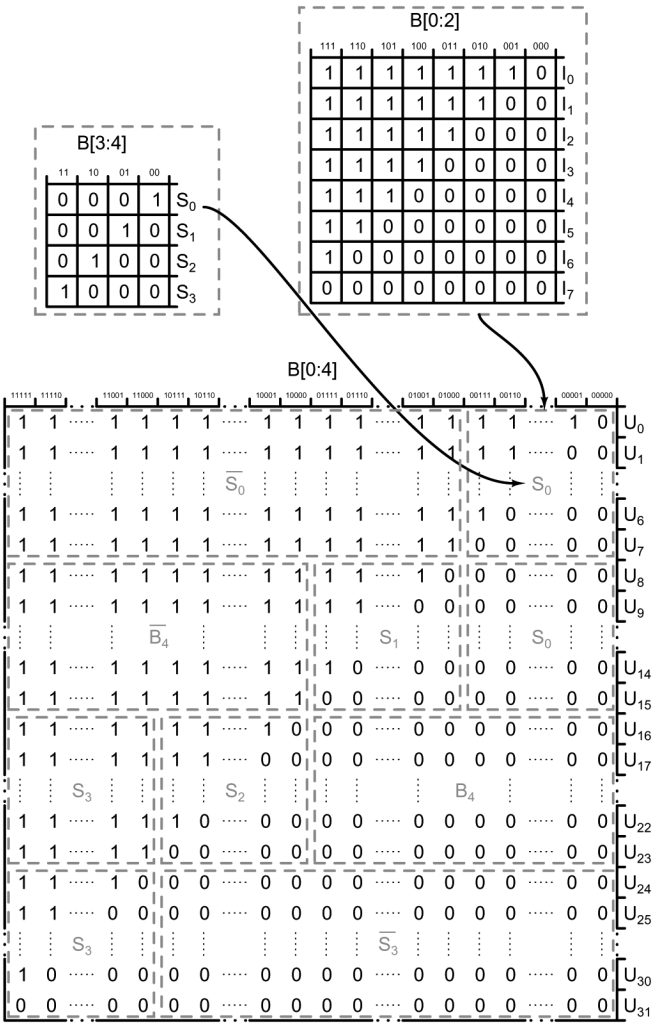

Fig. 7. Truth table for a 5-31 thermometer decoder illustrating the employed decomposition. The mux selection signals for each zone are indicated in gray.

shows that the SFDR-bandwidth will not be limited by the cell impedance.

The use of minimum-length cascodes has the additional advantage that the wire capacitance-free layout as will be introduced in Section IV-A works best, as the physical width of the cascode is approximately twice the width of the switch.

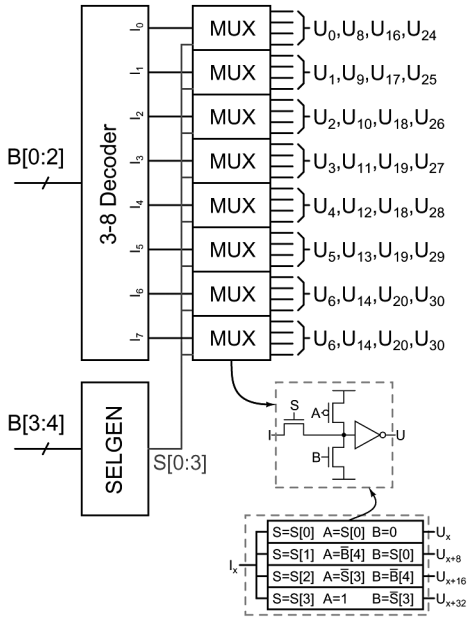

Fig. 8. Multilevel 5-31 decoder architecture.

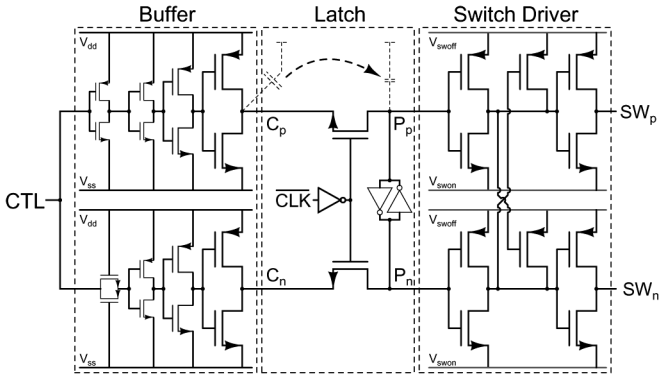

Fig. 9. Buffer, latch, and switch driver circuit schematic.

IV. Implementation

The global architecture is shown in Fig. 5. The input data is provided by a reduced specification low-voltage differential signaling (LVDS) interface at full sample rate. The DAC uses a 5-5 segmented architecture. A 5-31 thermocoder block provides the 31 thermometer coded control signals for the unary weighted section. The thermocoder delay is compensated by a delay equalization block for the binary coded bits. The design of the thermocoder is discussed in Section IV-B. The latches, switch drivers, switches, and current source cascodes are located together in the swatch block. The latch and switch driver are discussed in Section IV-C. The implementation of the switched current cell and the layout of the current source array are discussed in Section IV-A. To obtain good dynamic performance, it is imperative to ensure very good timing between the different sections of the converter. The measures taken to ensure proper timing by-construction are explained in Section IV-D.

A. Switched Current Cell and Current Source Array

As the current source nominal current is determined by the system specifications, (1) fixes the dimensions of the current source transistors for a given technology and overdrive voltage

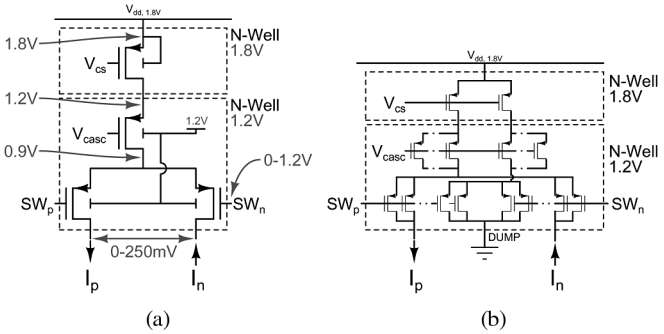

Fig. 10. Overview of the switched current cell implementation. The current source transistor is implemented in a separate well. This enables the use of a higher power supply voltage for the current source array, increasing the voltage margin available for the cascode and switch. The implementation of the binary current cells employs dummy transistors to equalize the load presented to the switch drivers. (a) Unary cell. (b) Binary cell.

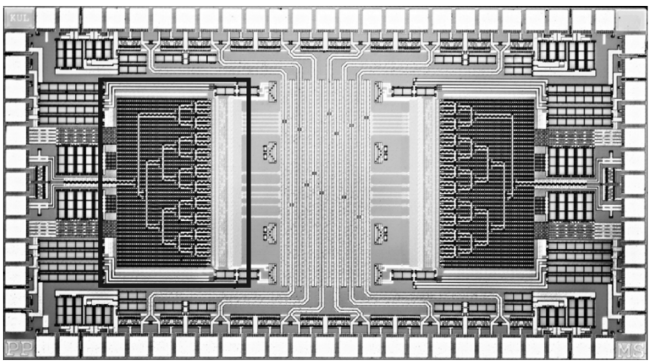

Fig. 11. Photograph of the test chip showing the described design on the left.

$(V_{gs}-V_T)$. To minimize the area penalty of the random V_T mismatch the current cell overdrive voltage was chosen to be 500 mV. Doing so makes the contribution of β mismatch dominant.

Using these relationships, the current source array (CSA) transistor width and length are calculated to be 16.1 μm and 8.3 μm. This sizing achieves a 99.7% yield specification for 10-bit accuracy. Gradient-induced mismatch errors in the unary section are compensated through the use of a switching scheme based upon the double centroid scheme introduced in [8]. To reduce the influence of edge effects the bias diodes and some dummies have been placed around the current-source array [6].

The layout of the switch and cascode combination is very important for the dynamic performance of the converter. In general, all wiring capacitances should be as small as possible. Section II-B, however, shows that the capacitance at the source node of the switches in particular should be minimized. Therefore, the switches and cascodes are laid out as shown in Fig. 6. By eliminating the metal interconnect between switch source nodes and cascode drain, the layout can be made very compact and hence wiring capacitance is minimized.

B. Thermocoder

For this design, a mux-based decoder as introduced in [19] was employed as it allows balancing the speed of a combinatorial approach with the reduced complexity of a row-column decoder. The mux based decoder is based upon the structure proposed in [6] and starts from the observation that the truth

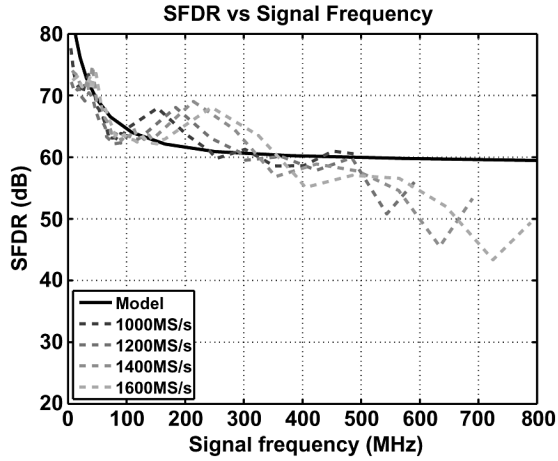

Fig. 12. Spurious-free dynamic range measured at different sample rates. The modeled SFDR according to (13) is also plotted.

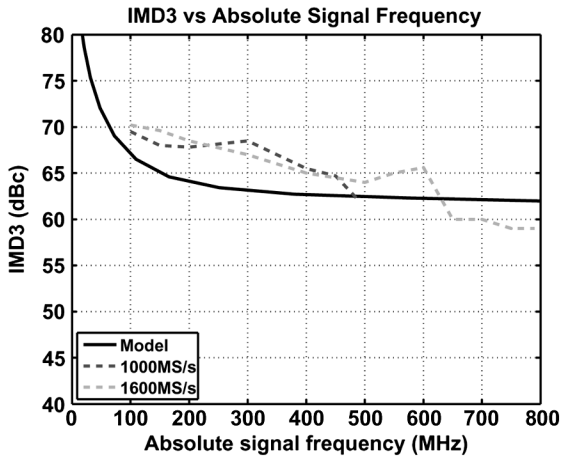

Fig. 13. Measured third-order intermodulation spurious free dynamic range at 1 Gs/s and 1.6 GS/s.

table of any thermometer decoder can be decomposed into a decoder of lower order combined with constant 1 and 0 sections as shown in Fig. 7. It is therefore possible to select the appropriate value for each decoder output using a multiplexer: either a constant 0, a constant 1, or the output of the lower order decoder.

Fig. 8 shows the 5-31 thermometer decoder architecture. In a first stage, the lower 3 bits are converted by a 3-to-8 decoder. Such a decoder can be built using logic functions that consist of either one-level NAND3 gates or two-level NAND2 gates. By restricting the decoder functions to these two logic functions the transition speed through the decoder can be fast and well equalized. The second stage consists of a set of equal mux blocks that select among three levels: logic 0, logic 1, or first-stage output. This selection is based upon the S[0:3] select signals that are generated by the SELGEN block which also consists of single-layer logic functions.

As the physical location of the thermometer decoded outputs does not affect the functional behavior of the circuit, the multiplexers selecting the same lower order output are grouped together and are physically located close to the logic function generating this lower order output. This simplifies the signal routing and reduces the number of long lines as only the SELGEN signals have to be routed over long distances, reducing overall power consumption of the decoder.

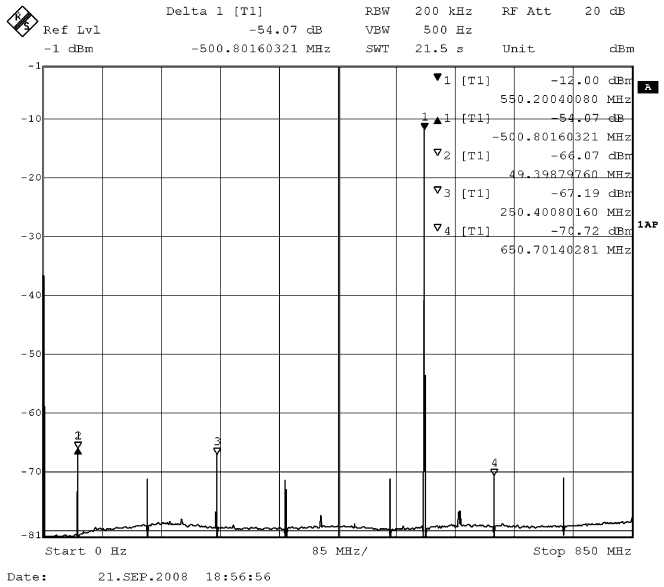

Fig. 14. Measured spectrum for a 550-MHz full-scale output signal at 1.6 GS/s.

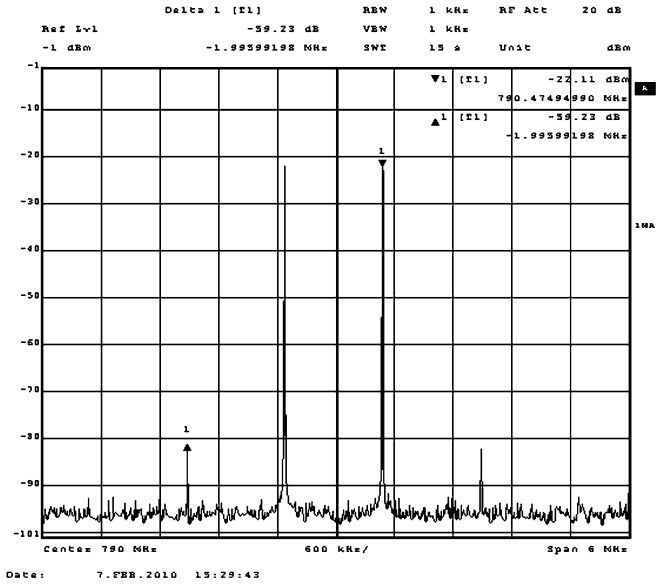

Fig. 15. Measured two-tone spectrum with two 1 MHz spaced tones around 790 MHz, sampled at 1.6 GS/s.

C. Latch and Switch Driver

The latch and switch driver employed in this design are shown in Fig. 9. The switch driver is inspired by the circuits proposed in [11], [20], and [21]. A basic pass-transistor latch is used to implement the synchronization of the switch control signals [20]. To reduce the sensitivity of the driver to data-dependent clock loading the clock signal is locally buffered, avoiding the need for clock load compensation circuitry [22].

To achieve good distortion performance it is important to minimize the intersymbol interference between successive input codes. Therefore, the input data is locally converted into a differential equivalent and buffered using an excessively scaled buffer. This improves switching speed by reducing the effect of the capacitive division between nodes Cp/Cn and Pp/Pn and by providing a low source impedance to the latch [21].

The outputs of the latch are conditioned using a switch driver lowering the crossing point [11] to ensure make-before-break operation of the current switch. Instead of directly driving the switch from the cross-coupled transistors, however, an intermediate buffer is used to reduce power consumption. The conditioning circuit lowers the crossing point by introducing cross coupling between the complementary signals; therefore, it generates short-circuit current during transitions. To drive the switches directly from the cross-coupled nodes, large transistors have to be used; hence, the short-circuit current becomes large. By adding an extra buffer between signal conditioning and switches, this current is reduced significantly. Additional advantages of this buffer are reducing the effect of clock feed-through and reverse signal coupling induced timing errors and improving switching speed.

D. Solid Timing By-Construction

To maintain high linearity at high frequencies and sample rates, the timing of the control and output signals should be tightly controlled [23], [24]. Therefore, the clock routing is performed using a partially balanced tree that ensures accurate timing between the segments. The output routing is done using two balanced trees, one for the binary section and one for the unary section.

Identical switch drivers are used for all cascode-switch cells, both for unary as binary weighted cells. This guarantees that all control signals have identical delays. The load presented by the binary scaled current switches, however, is dependent on the bit weight. When using identical switch drivers, this introduces systematic timing skew between the binary sections. To avoid this, load balancing dummy transistors have been used as illustrated in Fig. 10. To ensure maximum similarity by-construction, the dummy transistors carry current and operate in saturation. This makes that they have identical operating conditions and nonlinear capacitance behavior as the actual switches.

V. Measurement Results

Fig. 11 shows the photograph of the test chip containing the presented design. It was implemented in a standard 130-nm CMOS technology without any special processing options. The input data is provided using a full sample rate parallel LVDS, necessitating the use of on-chip terminated transmission lines. The core circuit excluding LVDS interface occupies 0.8 mm by 0.6 mm.

All measurements shown are performed differentially with a full scale load current of 10 mA. The output signals are combined using a transformer coupled double-terminated 50-Ω line and measured using a spectrum analyzer. Fig. 12 shows the differential SFDR over the entire Nyquist band for sample rates ranging from 1 GS/s to the maximum clock frequency of 1.6 GS/s. At low frequencies the converter achieves 74-dB SFDR, while it retains the desired 54-dB SFDR bandwidth of 550 MHz up to a sample rate of 1.6 GS/s. The measured two-tone intermodulation distortion at 1 GS/s and 1.6 GS/s is shown in Fig. 13. Figs. 14 and 15 show spectrum analyzer screenshots of a 550-MHz single-tone sine wave and a 790-MHz two-tone spectrum, both converted at 1.6 GS/s. Table I summarizes the performance of the implemented design. The reported power numbers do not include the power

TABLE I
MEASURED PERFORMANCE SUMMARY

Resolution	10-bit			
Technology	Standard 130nm 1P9M CMOS (UMC)			
Area	$0.5mm^2$			
INL/DNL	0.34 / 0.29			
Nominal Supply	$1.2V$/ $1.8V$			
Output Current	10mA in 25Ω			
Sample rate	1000MHz	1200MHz	1400MHz	1600MHz
Analog Power	18mW	18mW	18mW	18mW
Digital Power	5.6mW	6.8mW	7.9mW	9.0mW
Total Power	23.6mW	24.8mW	25.9mW	27.0mW
72dB SFDR BW	65MHz	65MHz	65MHz	65MHz
60dB SFDR BW	325MHz	325MHz	325MHz	325MHz
54dB SFDR BW	500MHz	550MHz	550MHz	550MHz

TABLE II
COMPARISON WITH OTHER CMOS D/A CONVERTERS IN OPEN LITERATURE MAINTAINING 60-dB SINGLE-TONE SFDR OVER AN OUTPUT BANDWIDTH OF AT LEAST 250 MHz

	This	[25]	[18]	[26]	[11]
Tech. (nm)	130	65	180	180	350
Area (mm^2)	0.5	0.31	1.13	2.5	0.35
Supply (V)	1.2/1.8	1.1/2.5	1.8	1.8/3.3	1.9/3.3
Resolution	10	12	12	14 (12)	10
$f_{clk,nom}$ (MHz)	1000	1600	500	1400	1000
$f_{clk,max}$(MHz)	1600	2900	600	/	/
Swing (mV)	250	2500	750	1500	400
Power (mW)	23.6	188	216	200	110
SFDR@LF (dB)	74	74	80	?	74
BW_{60db} (MHz)	325	430	250	260 (?)	500
FOM_1	11%	66%	5%	23%	12%
FOM_2	21695	4357	1185	/	1422
FOM_3	6886	5718	1736	/	3636
FOM_4	150	21	15	/	29

TABLE III
COMPARISON OF DIFFERENT FIGS OF MERIT FOR NYQUIST D/A CONVERTERS

	FOM_1	FOM_2	FOM_3	FOM_4
Origin	[25]	[28]	[27]	[9]
Definition	$\frac{I_{load}^2 R_{load}}{P_{total}}$	$\frac{2^N BW_N}{P_{total}}$	$\frac{V_{swing}}{P_{total}} BW\ 10^{\frac{SFDR}{20}}$	$\frac{2^{SFDR_{DC}} \cdot 2^{SFDR_{Nyquist}} \cdot f_{clk}}{P_{total} - \frac{1}{2} I_{load}^2 R_{load}}$
Dimension	none	1/Energy	1/Charge	1/Energy
Performances included in FOM				
Delivered Power	yes	no	indirect	yes
Supply Power	yes	yes	yes	yes
Output Swing	indirect	no	yes	indirect
SFDR@LF	no	no	no	yes
SFDR@Nyquist	no	yes	yes	yes
Clock frequency	no	indirect	indirect	yes

consumed by the LVDS interface, as it is considered part of the measurement infrastructure. As all bias voltages and currents were generated off-chip, the power consumption of biasing circuits is also not included.

A. Comparison With Other D/A Converters in Open Literature

In order to evaluate the effectiveness of the applied design strategy the presented DAC's performance is compared to the state of the art in Table II. The comparison includes the CMOS designs published in the JSSC and the ISSCC digest that are capable of generating an output signal with 250-MHz signal frequency with a linearity of at least 60 dB. The comparison shows that the presented design consumes significantly less power than its competitors. Absolute power numbers, however, do not provide a fair comparison as they do not account for linearity, sample rate nor output swing. Especially the latter can distort the comparison in favor of the presented design, as it has a fairly low output swing.

To assist comparison, the table also includes the according to four figures of merit (FOMs). It is difficult to capture the multitude of performance metrics into one number, and as a result FOM definitions are the source of endless debate. In a attempt to avoid this, we chose to include the most common applicable FOM figures proposed in open literature. Table III enumerates

them along with their origin and definition. The DAC performance metrics included in each FOM are also indicated in the table.

VI. Conclusions

A 10-bit current steering D/A converter implemented in a 1.2-V 130-nm CMOS process has been described. It achieves a 550-MHz 54-dB SFDR bandwidth up to 1.6 GS/s, and maintains full-Nyquist performance up to 1 GS/s. When converting a near-Nyquist signal at 1.6 GS/s the power consumption is only 27 mW. This low power consumption has been achieved by applying a switch-driver power-aware design strategy for the current cells and by using a power optimized switch-driver implementation. Furthermore a thermometer decoder has been introduced that minimizes power consumption by reducing routing related wiring capacitance. The presented DAC matches the performance of state-of-the-art designs, revealing the effectiveness of the applied design methodology and proposed circuits.

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