A/D Converter Fundamentals and Trends

(IEEE CICC 2017 Tutorial)

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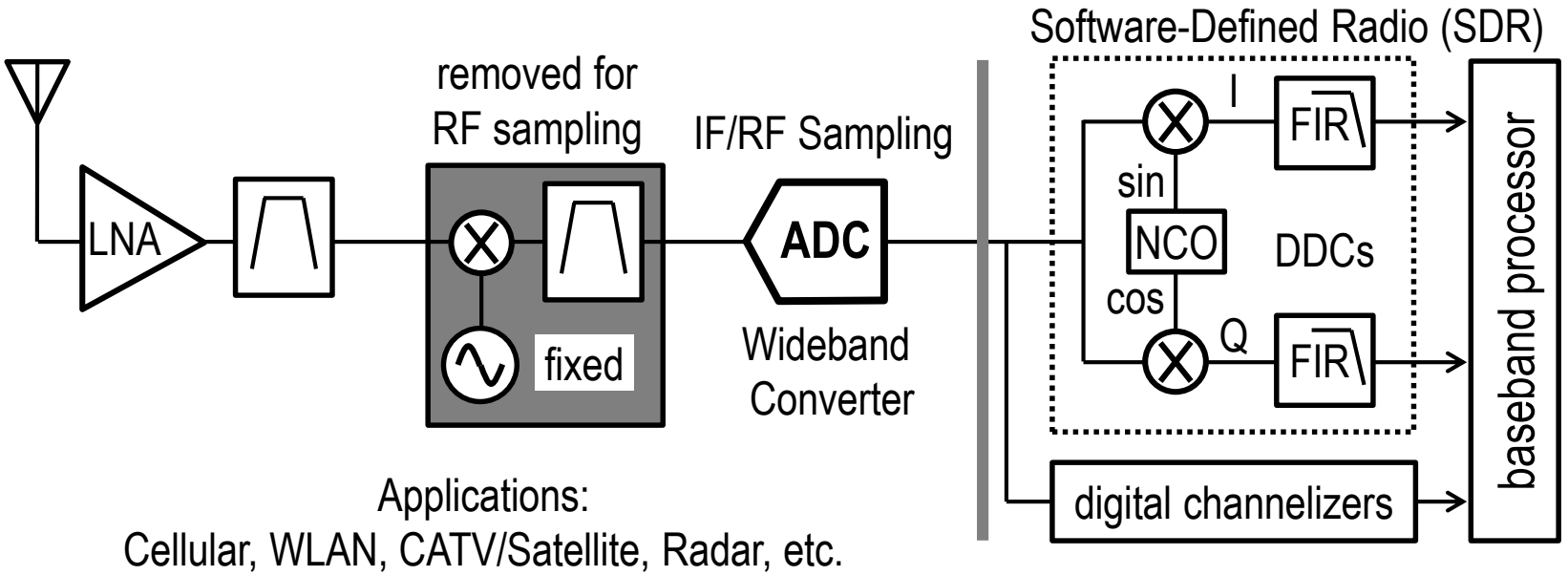
Agenda

- Applications and Systems
- Algorithms and Architectures
- Circuit Implementations
- Imperfections and Corrections
- Metrics and Measurements
- Evolutions and Trends
- Closing Remarks

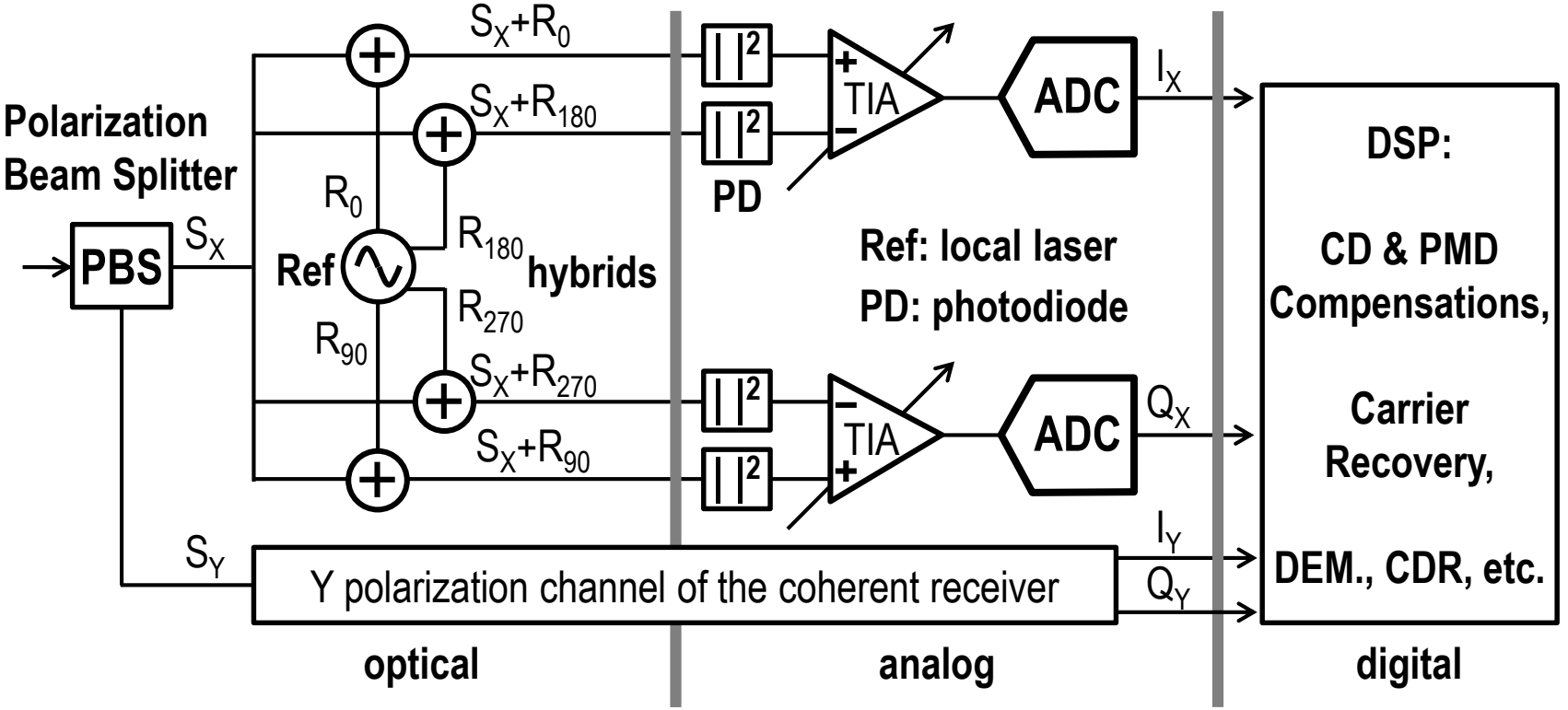
Applications and Systems

Full Band Capture and Software-Defined Radio



- Multi-GS/s ADCs for IF/RF full-band/multi-band capture of hundreds of channels
- High ADC dynamic range for DSP to sort out weak signals from in-band blockers
  - SFDR ~ 80dB & SNR ~ 60dB for GSM base station applications [*Pan, JSSC 2000*]
- High power, but gap closing with heterodyne for $f_t >> f_{nyquist}$ [*Gomez, TCAS 2016*]
  - Direct sampling (DS) more efficient than heterodyne with carrier aggregation

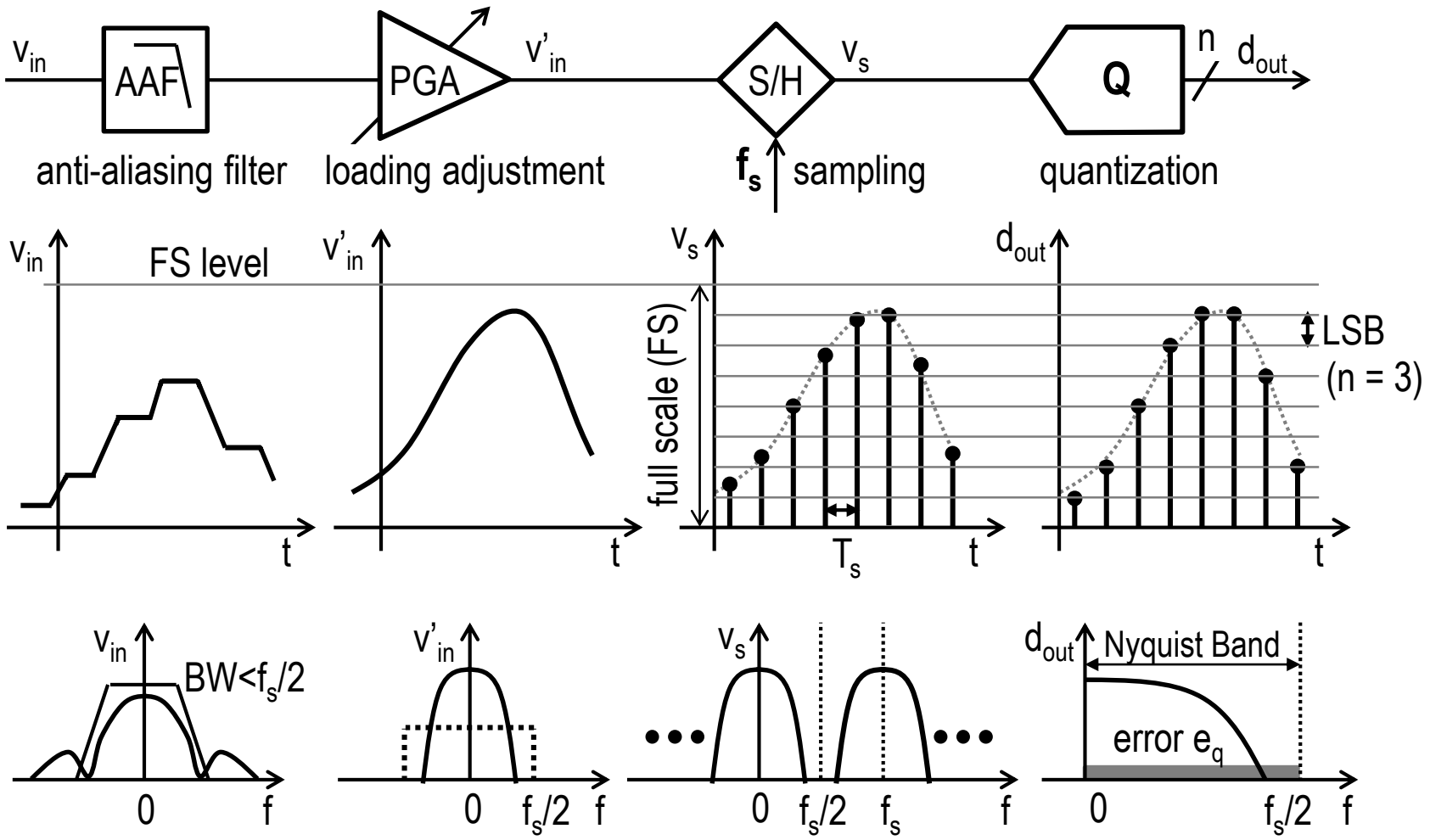
DSP Based Wireline Receivers



Applications: coherent optical communications (100G and higher)

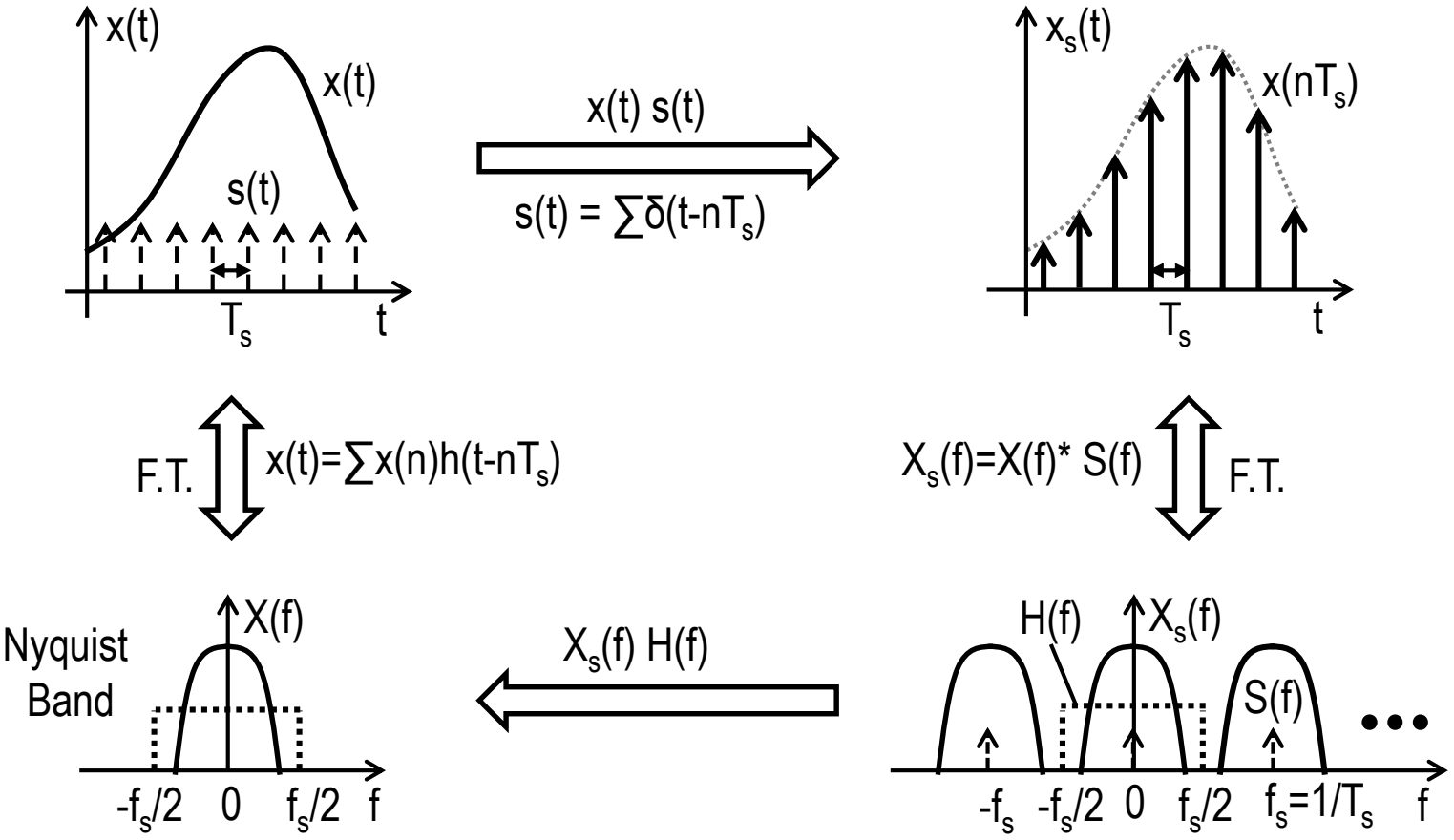
- Ultra high-speed (>10GS/s) 5~8b ADCs and DSPs enable long-haul optical transmission beyond 10Gb/s per lambda *[Crivelli, TCAS-I 2014]*.

A/D Conversion: A System Perspective

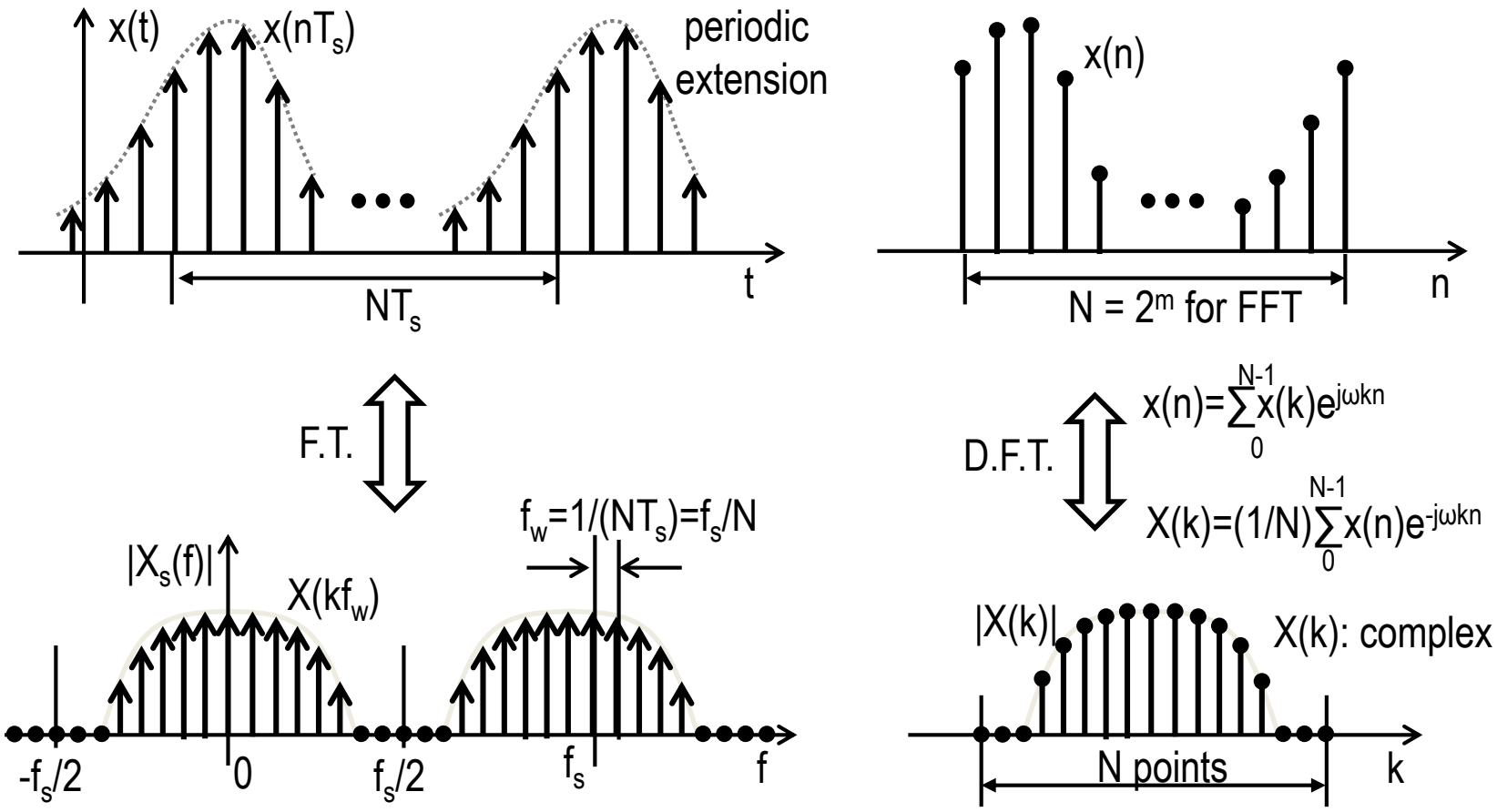


- Sampling and quantization operations are permutable with each other.

Sampling Theorem

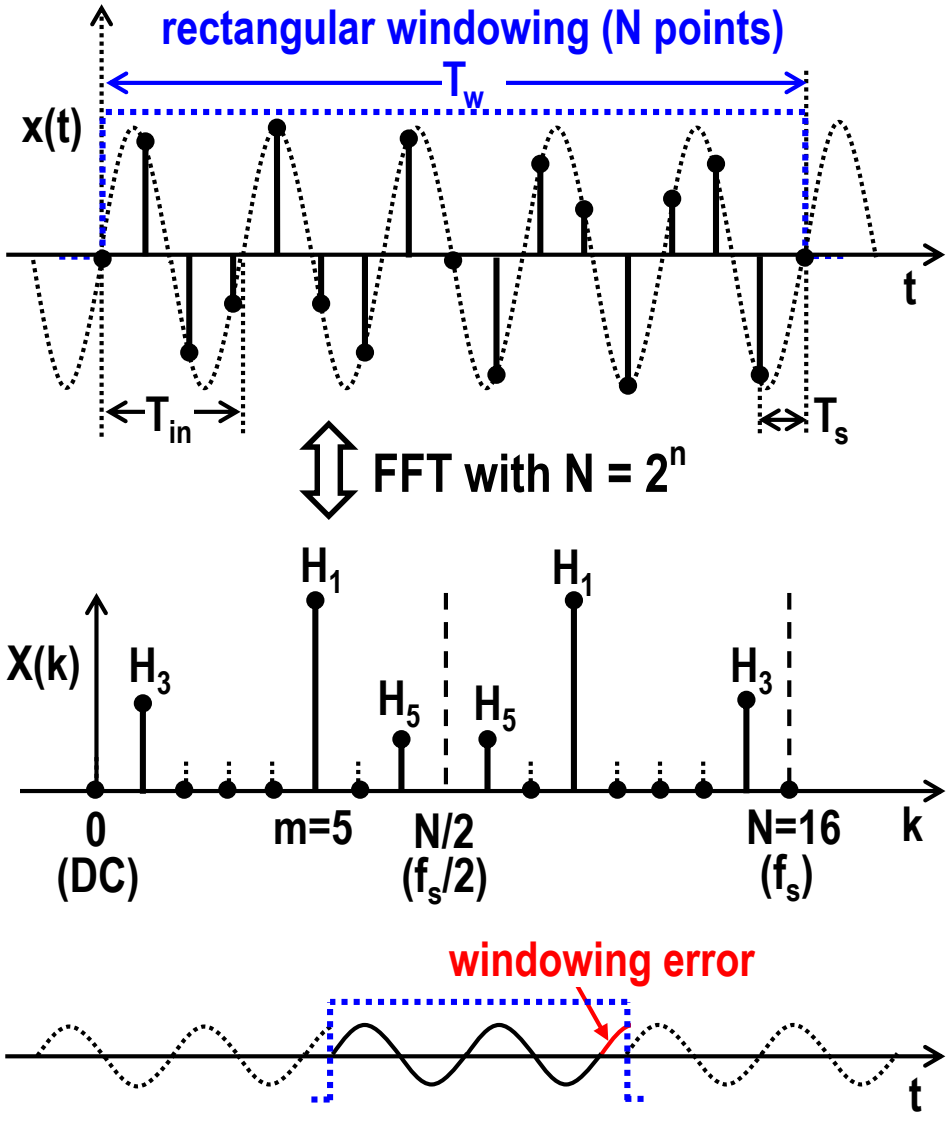


Discrete Fourier Transformation (DFT)



- Important tool for spectrum analysis of finite signal samples
- Fast Fourier Transformation (FFT) algorithms for $N = 2^m$

Coherent Sampling of Periodical Signals



N-Point Coherent Sampling:

$$T_w = N\,T_s = m\,T_{in}$$

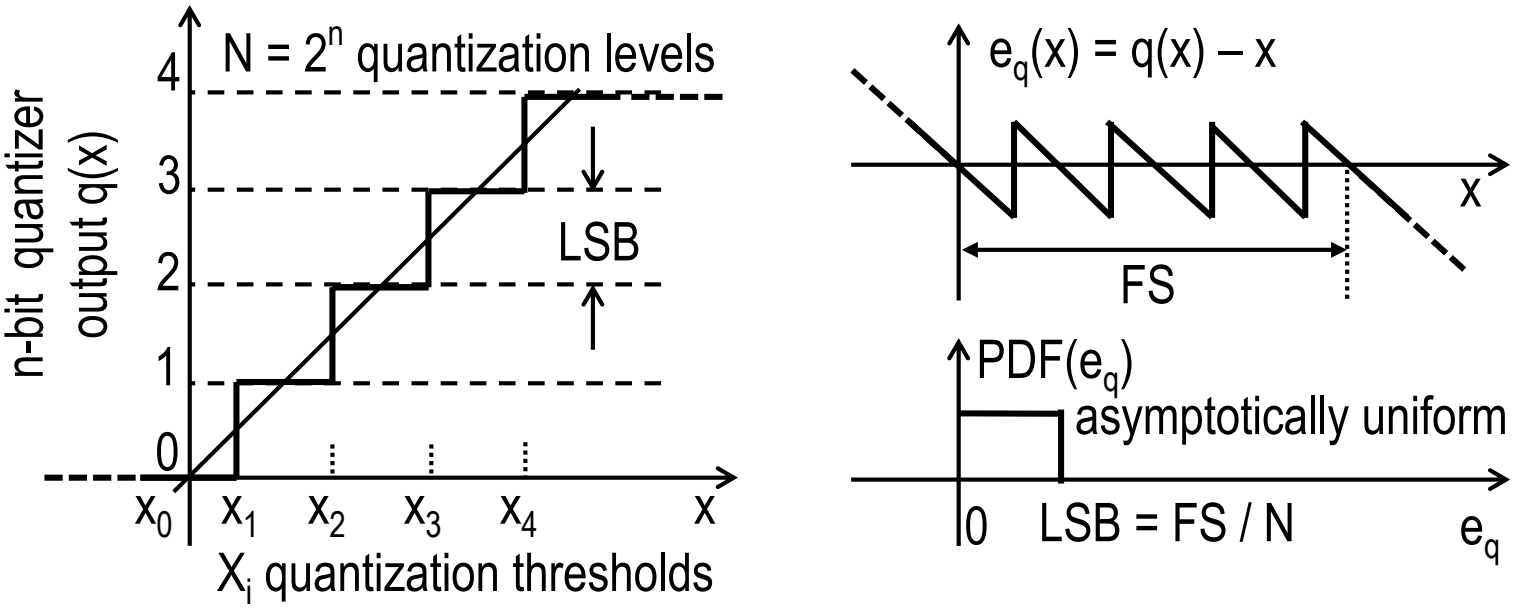
$$\Downarrow$$

$$f_{in} = (m/N)\,f_s = m\,f_{bin}$$

$$(f_{bin} = 1/T_w)$$

- Each H_i falls in one bin with coherent sampling.
- Less H_i's fall in same bin with prime ratio $m = f_{in}/f_{bin}$.
- Windowing error causes spectral leakage to all bins.

Quantization and Error Characteristics

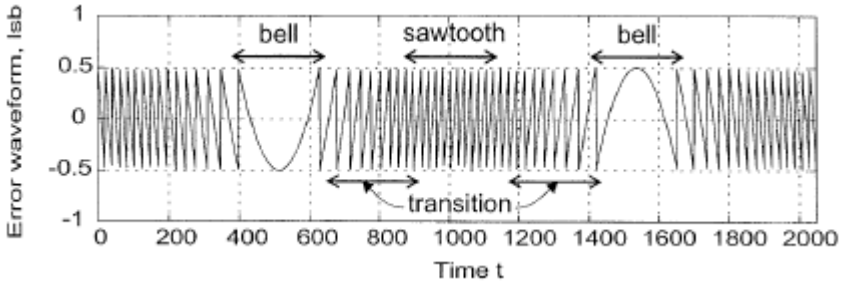


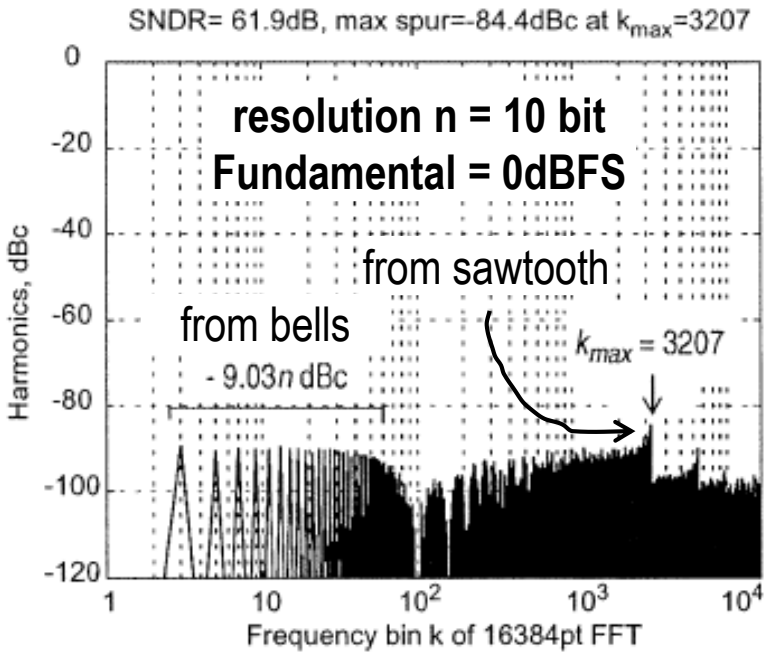
Error Power $P_e(x) = \int (e_q)^2 \, PDF(e_q) \, de_q = LSB^2 / 12$

- Quantization error is usually approximated as additive noise
  - Asymptotically uniform PDF, independent of x for x(rms) >> LSB
  - Converted to noise n_q by dithering of similar or higher magnitude

Error Waveform & Spectrum of Quantized Sinewave

$e_q(t) = q(A\sin(2\pi f_{in}t)) - A\sin(2\pi f_{in}t)$



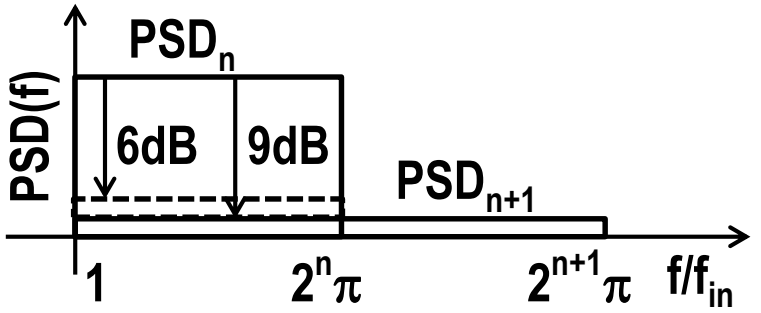


Sawtooth period ~ LSB / $(2\pi f_{in}A) = 1 / (2^n \pi f_{in})$

Max harmonic freq. ~ $(2^n \pi) f_{in}$

Max harmonic order $k_{max} \sim 2^n \pi$

Max harmonic level ~ –9n+c (dBFS)



- Quantization causes very high-order distortion (spurs).
- **Spur level actually rises as signal amplitude decreases**.
- All spurs fold within Nyquist band as a result of sampling.

[*Pan, TCAS-I 2004*]

Ideal ADC SNR & SFDR, and Real ADC ENOB

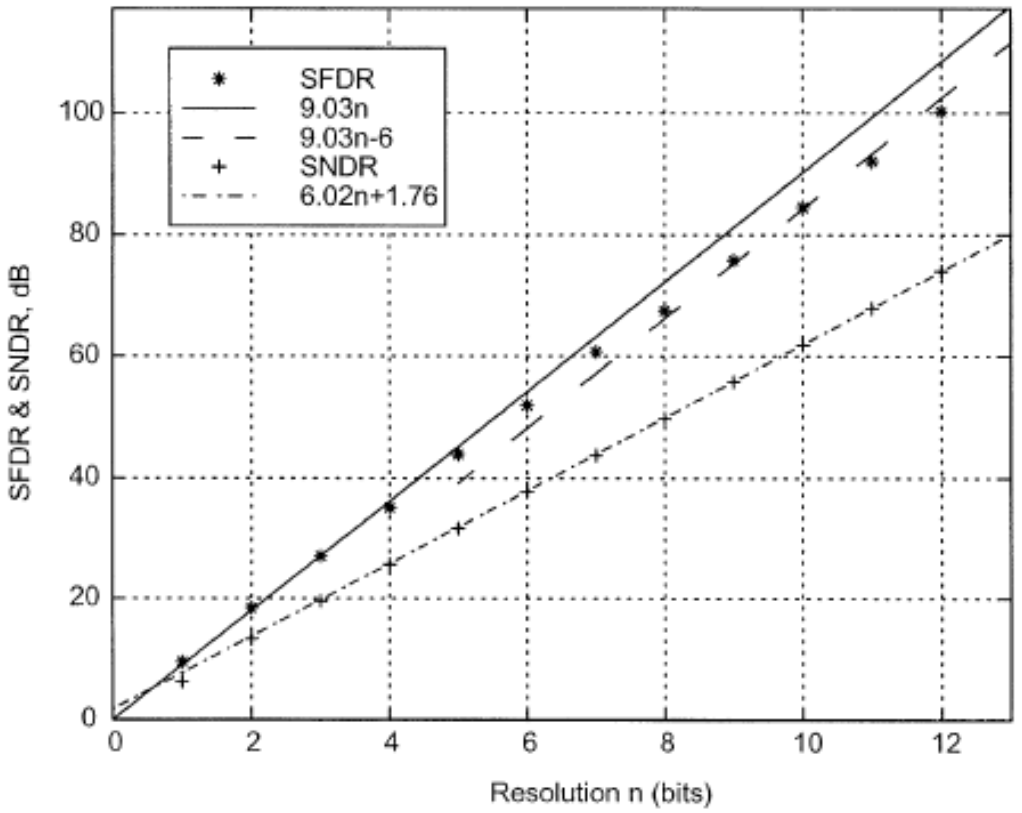
Single-tone Signal Power P_s
$= FS^2 / 8$

Noise & Distortion Power P_e
$= LSB^2 / 12$

Single-tone Spur Level P_d
$\approx -9n$ dBFS

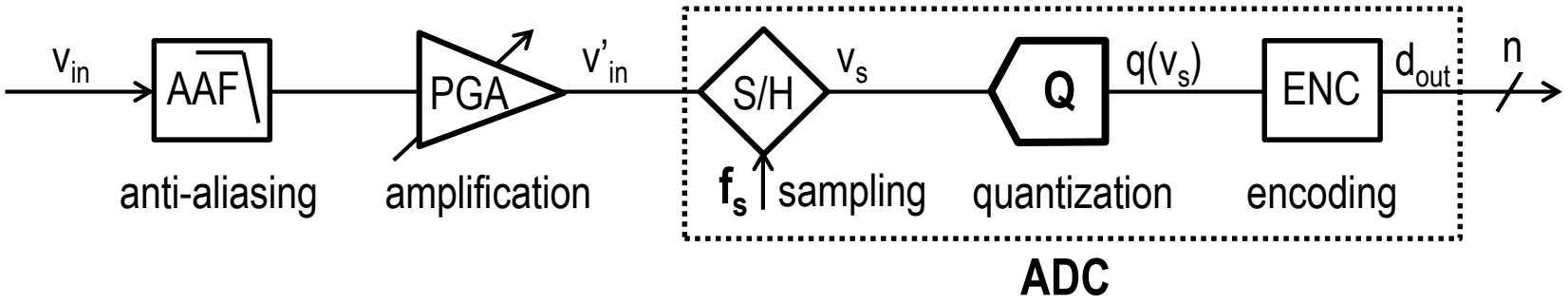
SNDR $\equiv P_s / P_e$
$= 6.02n + 1.76$ (dB)

SFDR $\equiv P_s$ / max. P_d
$= 9.03n + c$ (dBFS)
($c \approx -6$)



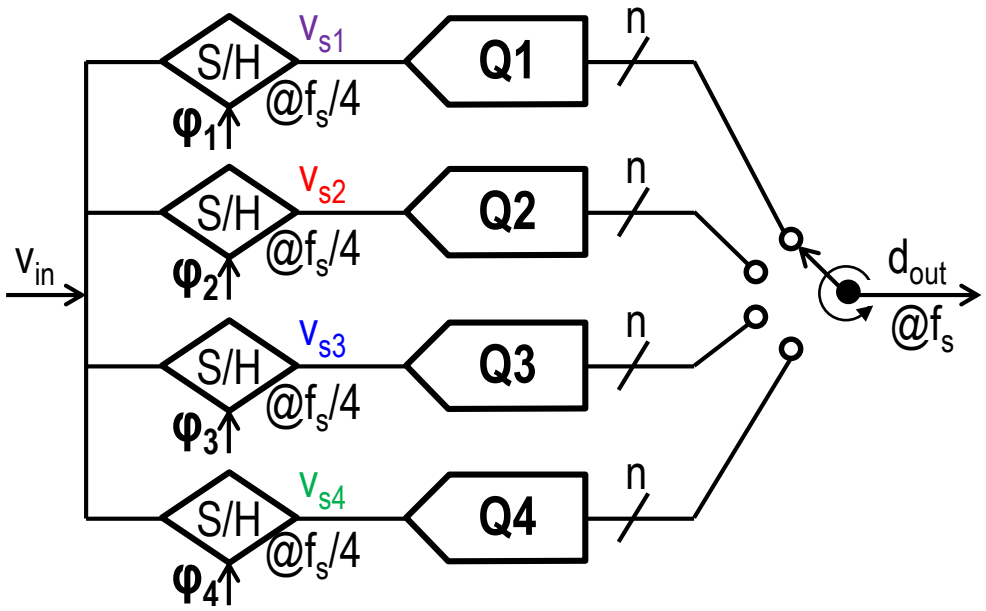
For real quantizers,
Effective Number of Bit (ENOB) = (SNDR – 1.76) / 6.02

A/D Converters and Systems

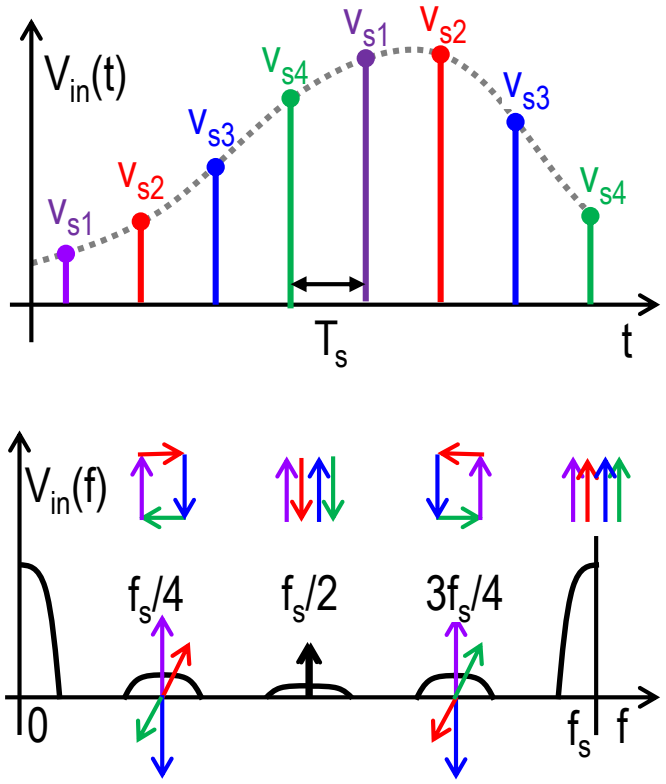


- An ADC consists of sampling, quantization, and encoding
  - AAF & PGA in different design categories or merged with S/H
  - Operation sequence permutable, but usually same as shown
- In a narrow sense, an ADC consists of only quantization.
  - S/H merged with Q or eliminated for clockless ADCs
  - Encoder merged with Q or included in succeeding DSP
- In a wide sense, an ADC is a compound system that consists of one or more quantizer cores and some auxiliary functionalities for enhancing conversion speed, resolution, efficiency, etc.

Sampling Rate Multiplication by Time-Interleaving

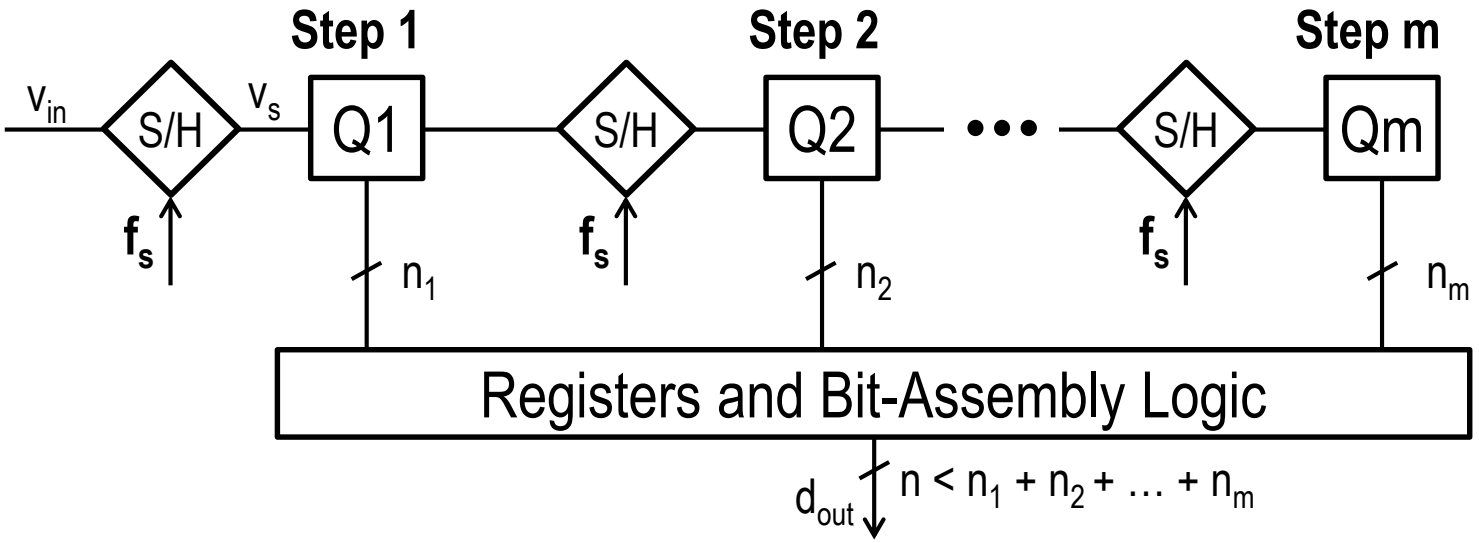


[*Black, JSSC 1980*]



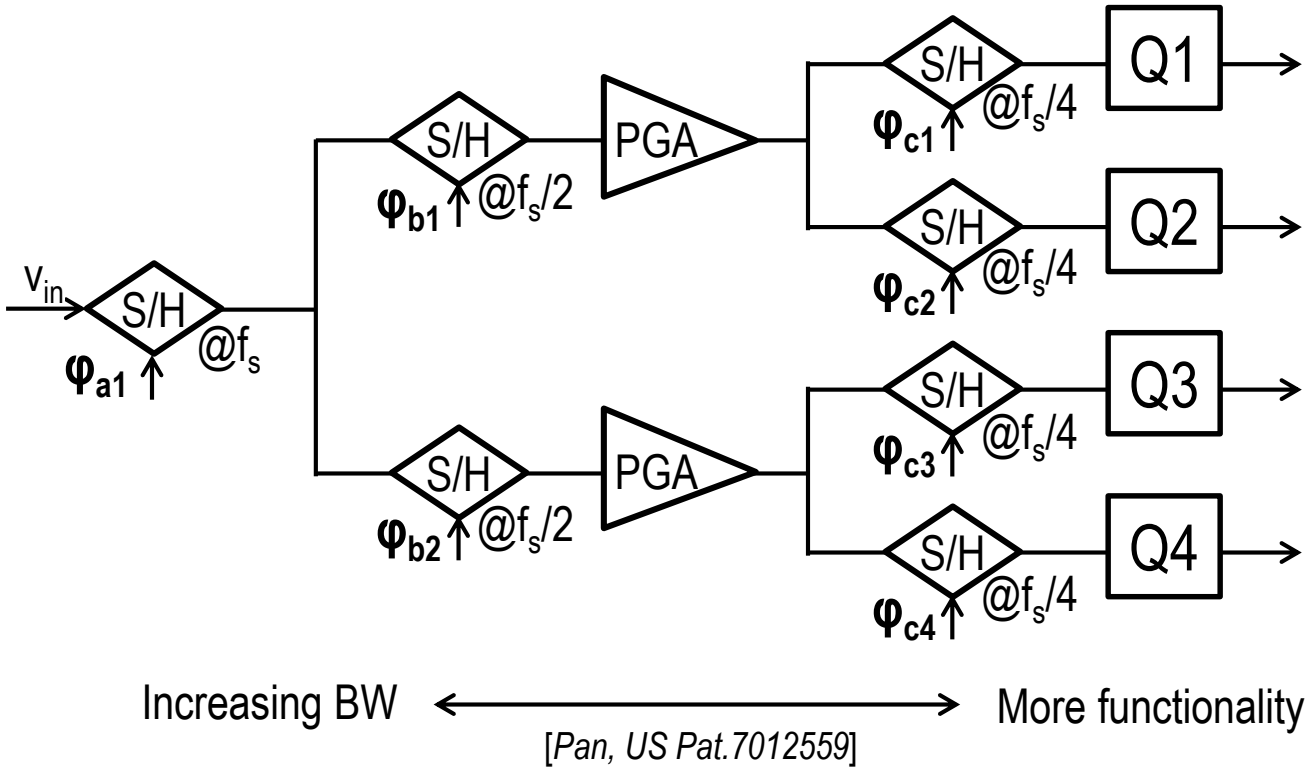
- Conversion rate linearly increases with *m* = number of time-interleaved ADCs.
- S/Hs are bottleneck for Nyquist operation as the tracking BW must scale with *m*.
- Errors arise from kickback and channel mismatch in offset, gain, BW, timing, etc.
- Error correction can be merged with succeeding digital signal processing.

Conversion Rate Multiplication using Pipelining



- Conversion rate linearly increases with *m* = number of pipeline stages, which decouple quantization throughput from latency.
- Sample-and-holds for pipeline storage must settle to full accuracy at full speed, best suited for implementation with switched capacitor circuits in CMOS technology [*Lewis, JSSC 1987*].
- Accurate settling is challenging esp. in deep submicron CMOS.

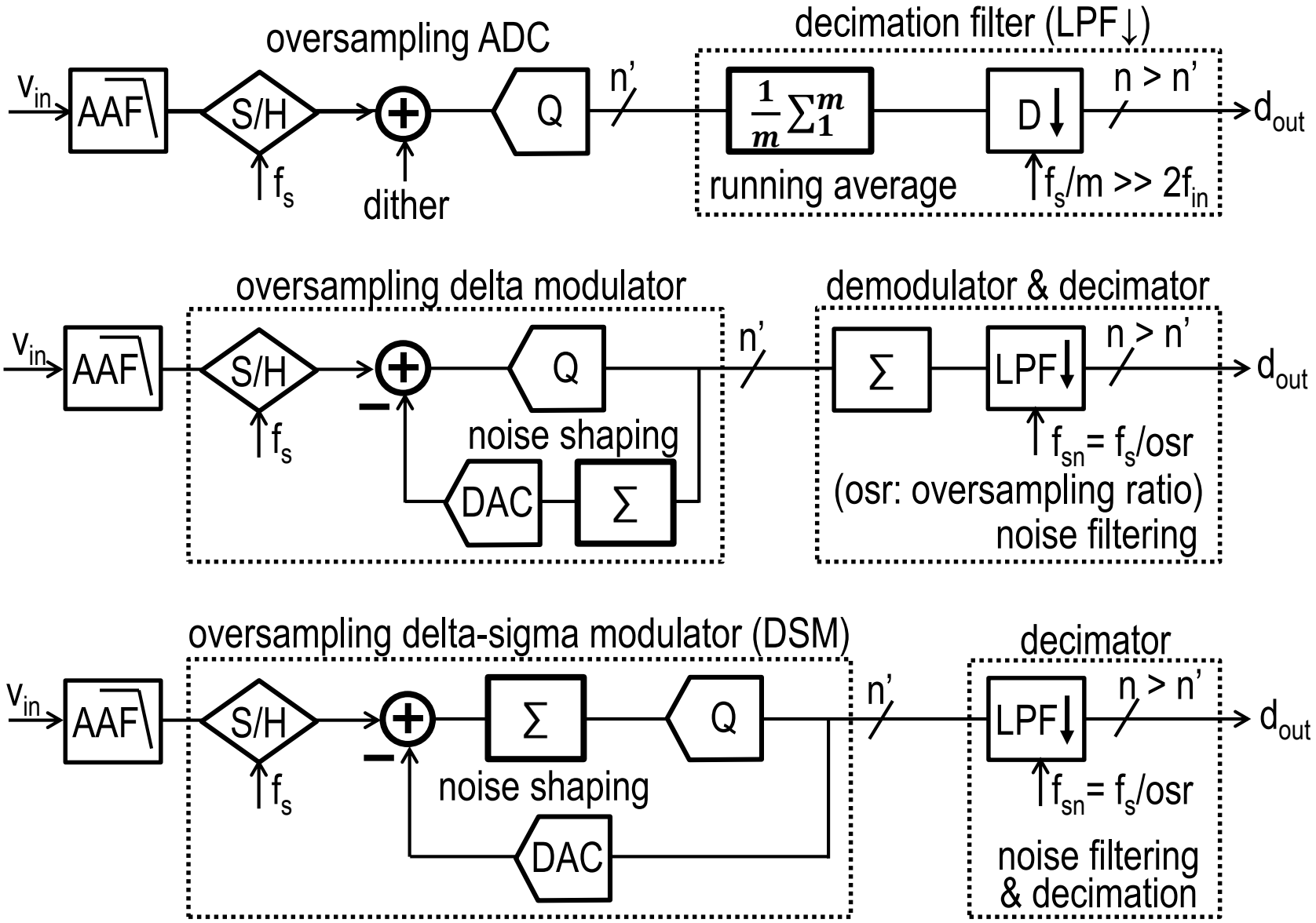
Hierarchical Parallel and Pipelined A/D Conversion



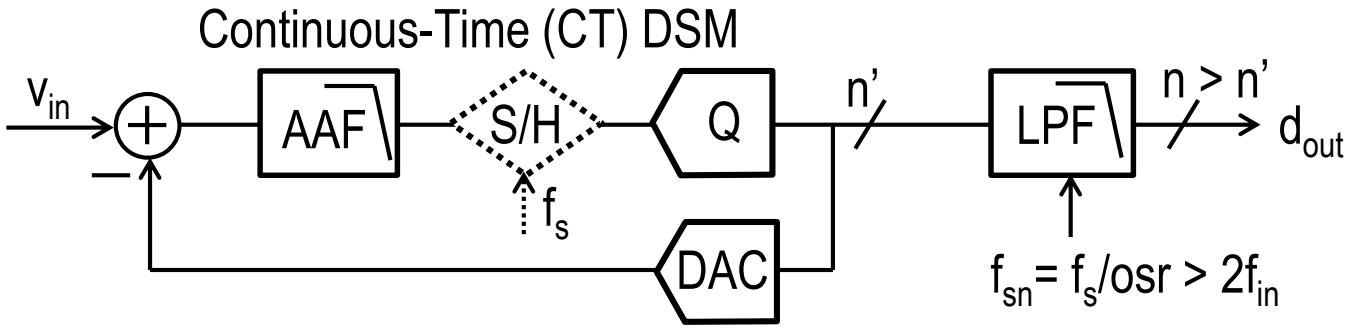
[*Pan, US Pat.7012559*]

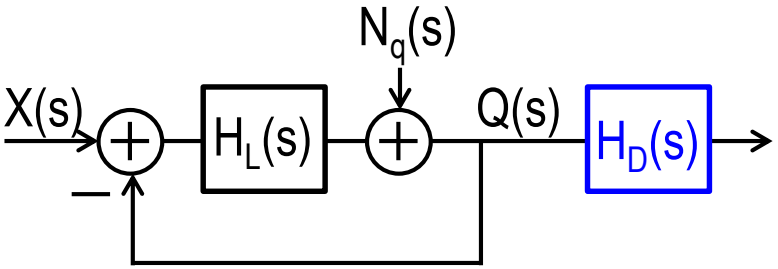
- BW and functionality grow in opposite directions in the hierarchy.
- Number of head-end channels is minimized for max. BW.
- Phase alignment necessary among multi-rate multi-phase clocks.
- Clock jitter and skew cause little error after first stage S/H(s).

Resolution Boost by Oversampling & Noise Shaping



Noise and Signal Transfer Functions (NTF & STF)

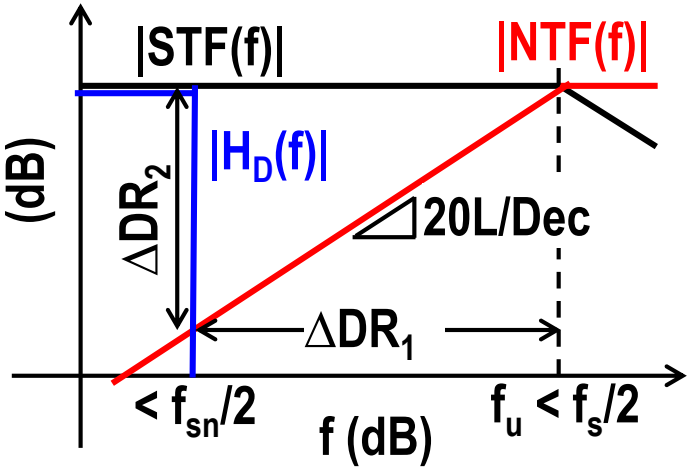




For $H_L(s) = s_u/s$

$STF(s) = Q(s) / X(s) = 1/(1+s/s_u)$

$NTF(s) = Q(s) / N_q(s) = (s/s_u)/(1+s/s_u)$



$\Delta DR_1 \sim 10 \log(OSR)$

$\Delta DR_2 \sim 20L \log(OSR)$

$\Delta DR(dB) \approx \Delta DR_1 + \Delta DR_2 \approx (6L+3) \log_2(OSR)$

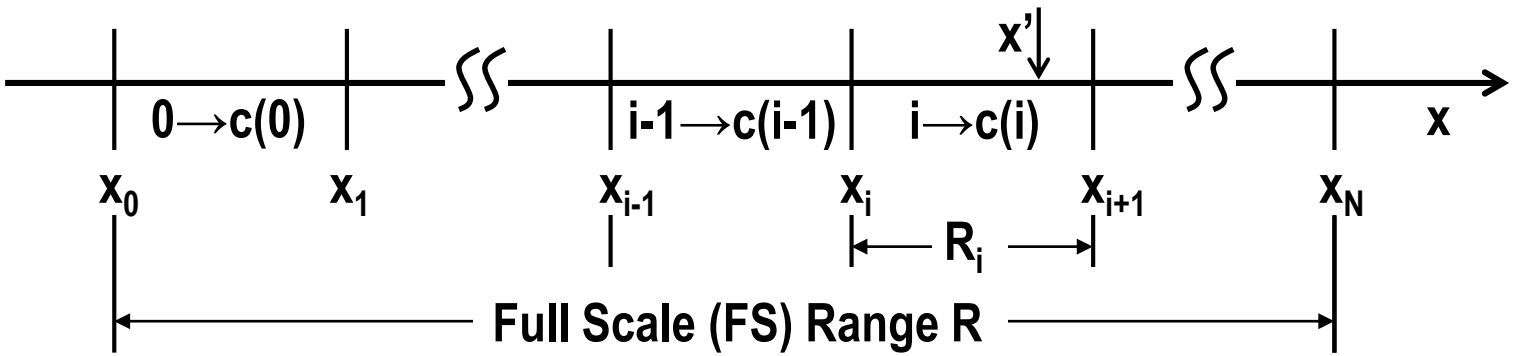
L= $H_L(s)$ order; OSR = f_s / f_{sn}

Algorithms and Architectures

Quantization Q(x) as a Search Process

$Q(x) = i \rightarrow$ codeword $C(i) = \{s_1 s_2 \ldots s_m\}$

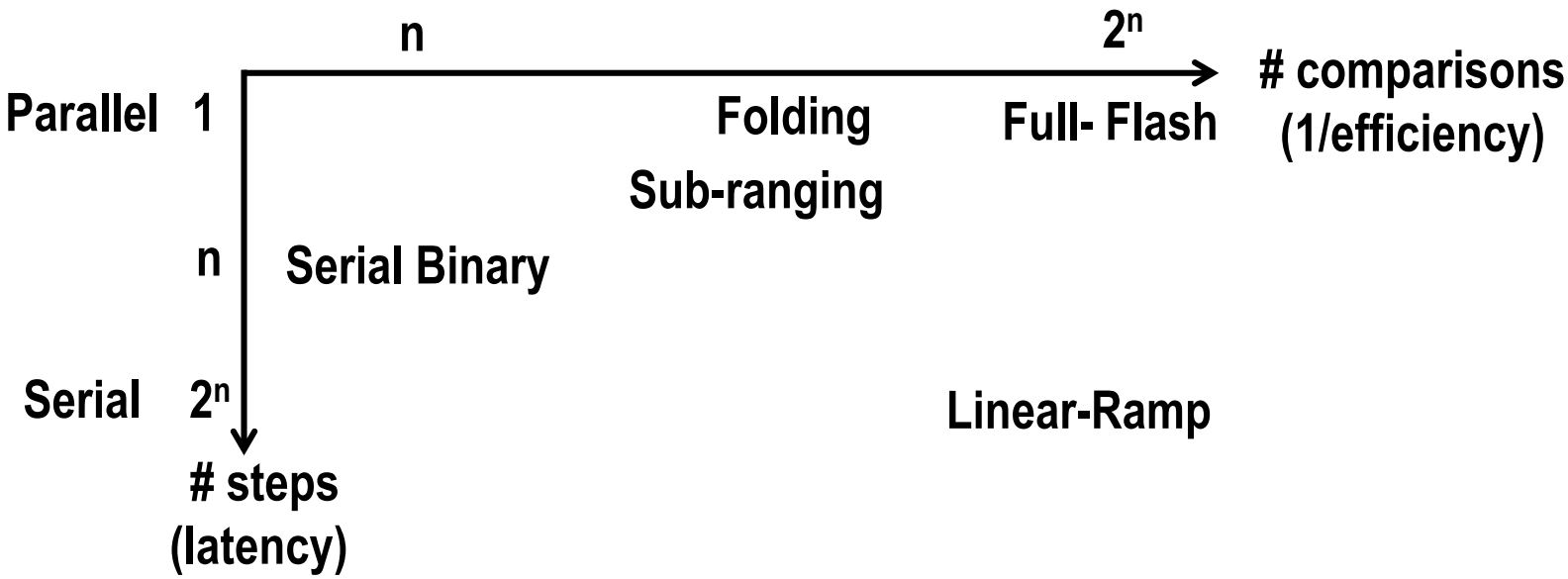
(e.g. {C(0), C(1), …, C(7)} = {000, 001, …, 111})



(x_i: quantization thresholds)

- $Q(x) = i$ for $x \in R_i$, $i = 0, 1, \ldots, N-1$; $N = 2^n$ for n-bit quantizer.
- Sub-range $R_i = x_{i+1} - x_i = R/N = LSB$ for uniform quantization.
- A quantizer searches for the R_i in which a given x falls.
- An algorithm drives the search based on (x, x_i) comparison.
- An optional encoder C maps $Q(x) = i$ to a codeword C(i).
- Q and C can be merged to resolve each code symbol s_k directly.

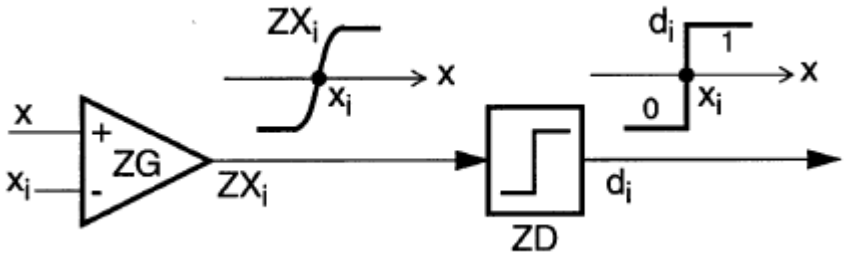
Search Algorithms for Quantization



- Parallel brute-force (full-flash) : one step, ~2^n comparisons
- Serial brute-force (linear ramp up/down): ~2^n steps and comparisons
- Serial binary search (1b/step): n steps and comparisons
- Coarse-fine search (sub-ranging): 1< steps <n, n< comparisons <2^n
- Search efficiency (# comparisons) dominates power efficiency

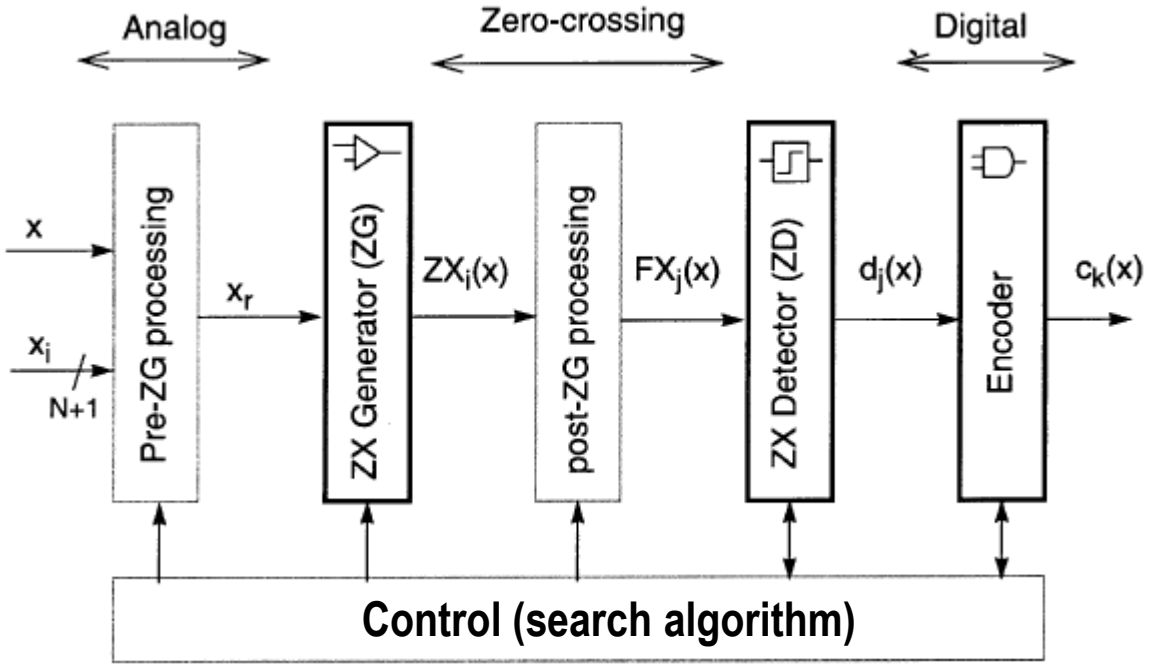
Quantization Elements and Generic Architecture

1b quantizer (comparator)



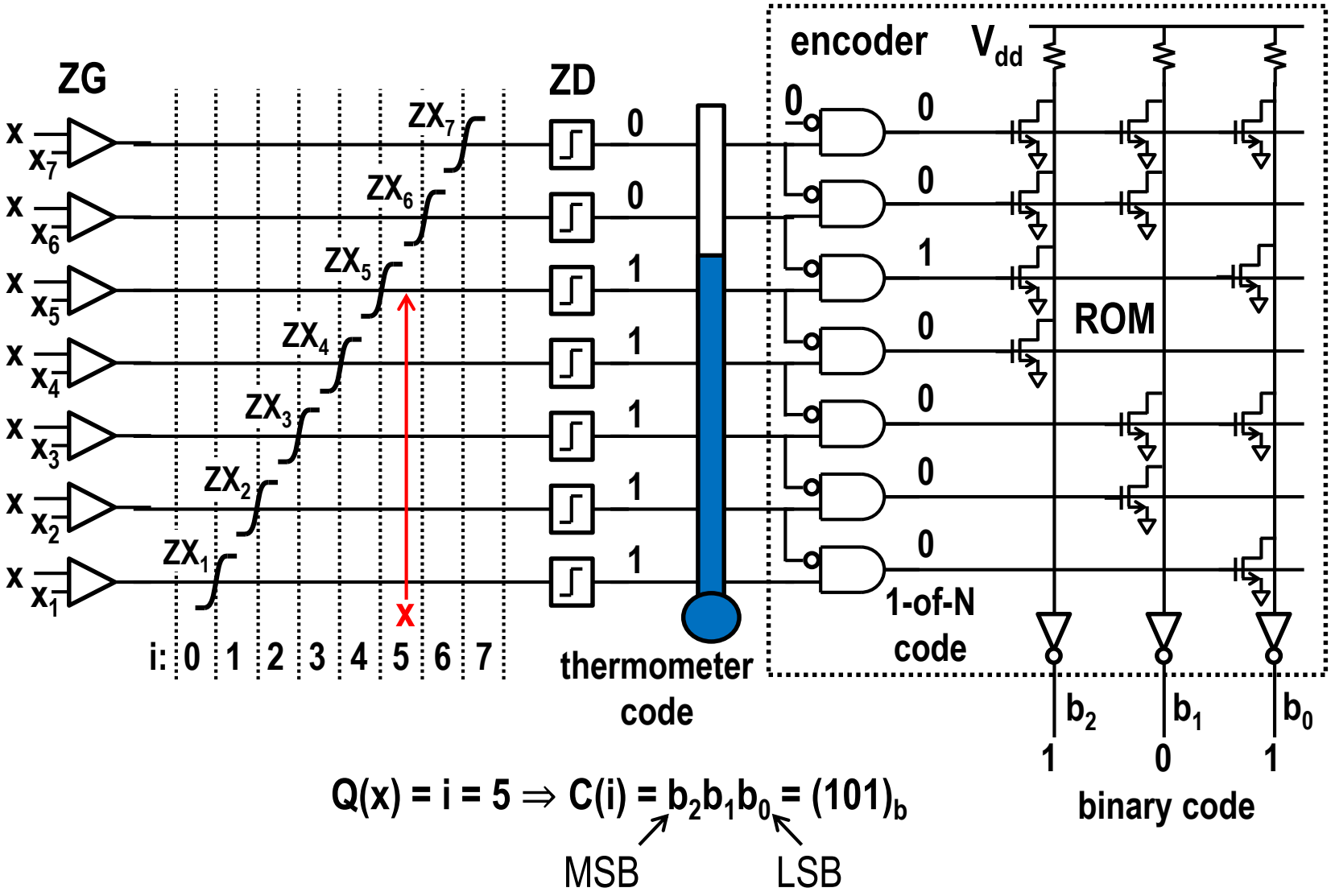
generic quantizer

[*Pan, TCAS-I 2004*]

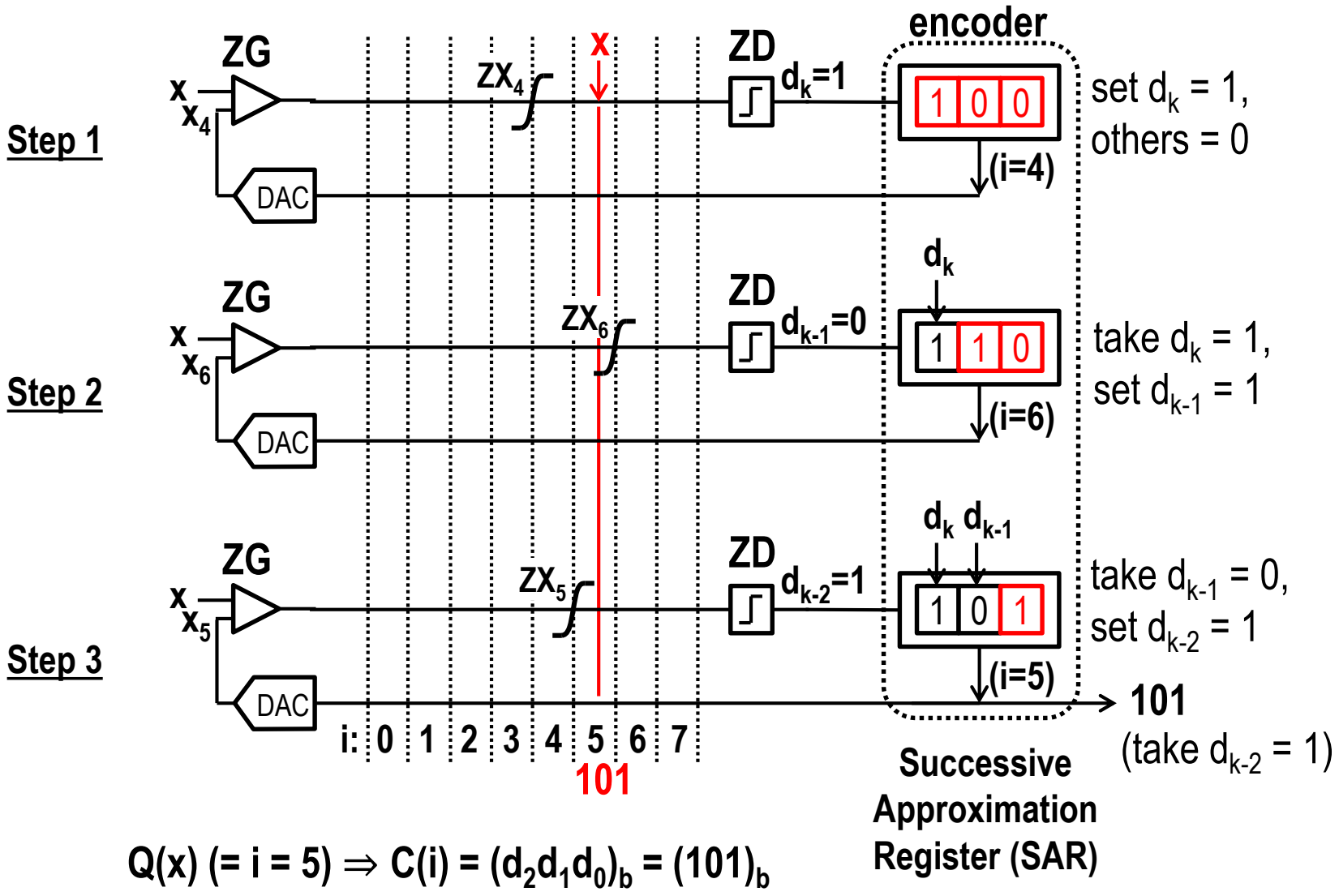


- Quantizer core elements: ZX generation (ZG) and ZX detection (ZD)

Parallel Brute-Force Search: Full-Flash



Serial Binary Search: Successive Approximation

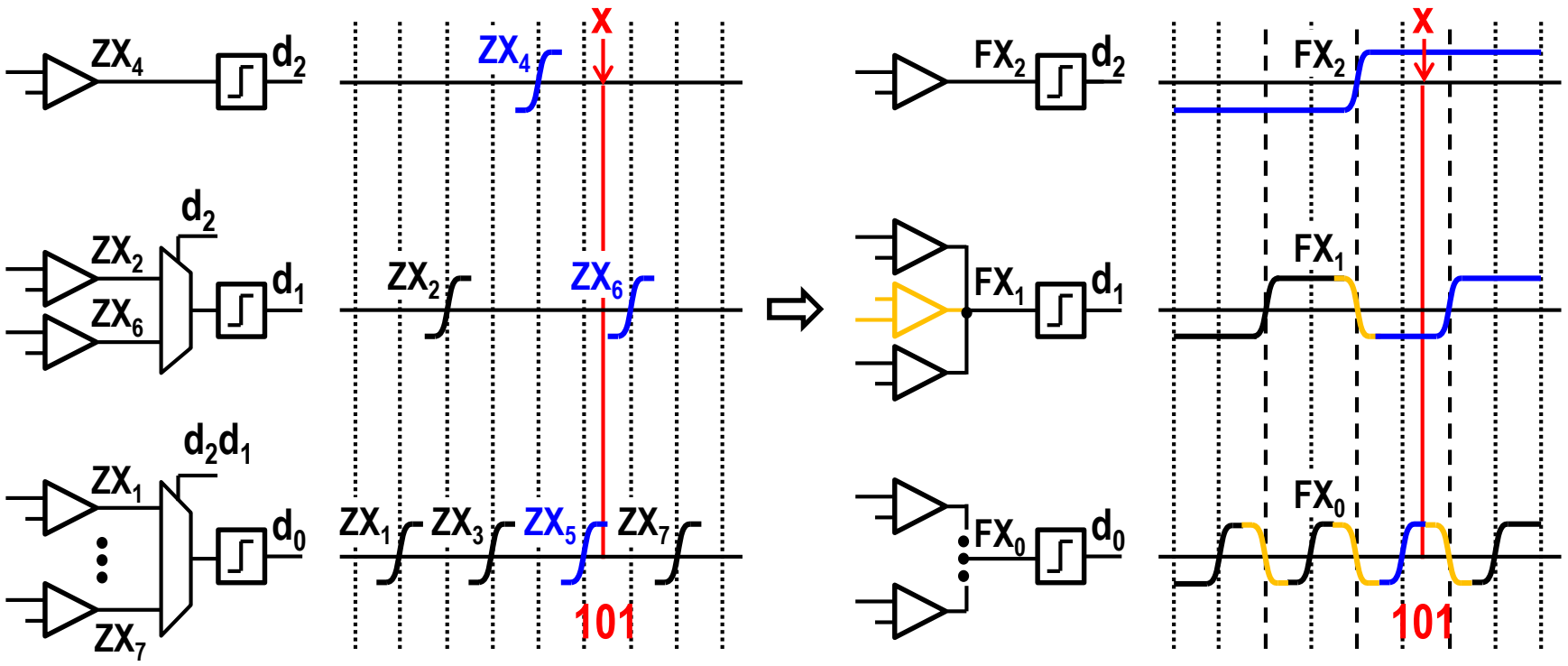


$Q(x)\ (= i = 5) \Rightarrow C(i) = (d_2 d_1 d_0)_b = (101)_b$

Parallel Binary Search: Analog Encoding

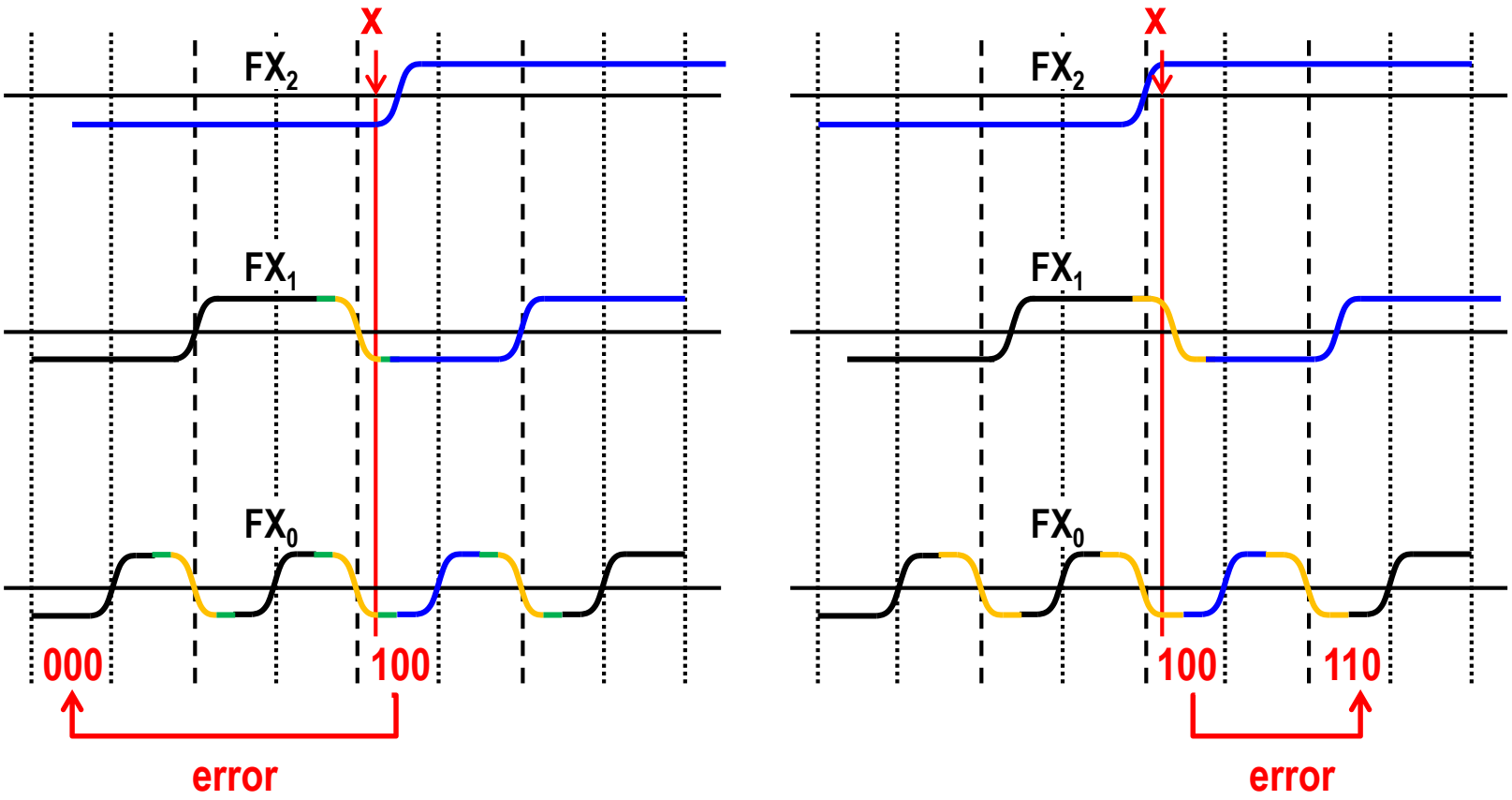
n-step serial binary search
by multiplexing ZXs

One-step parallel binary search
by signal folding



- Signal folding merges ZG and encoding ➔ analog encoding.
- Signal folding is equivalent to automatic multiplexing of ZXs.
- However, there is algorithmic conflict among redefined ZXs.

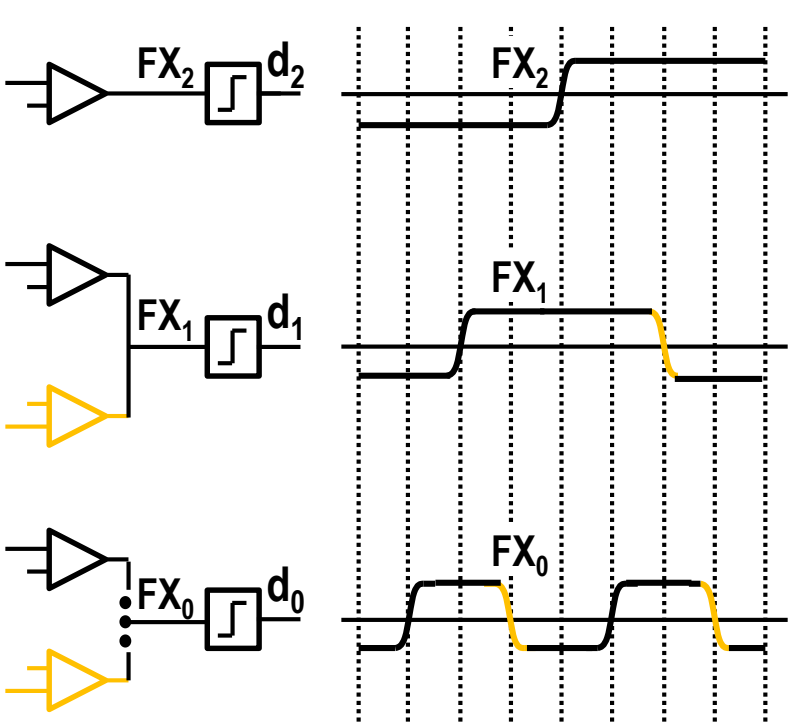
Potential Algorithmic Conflict in Binary Search



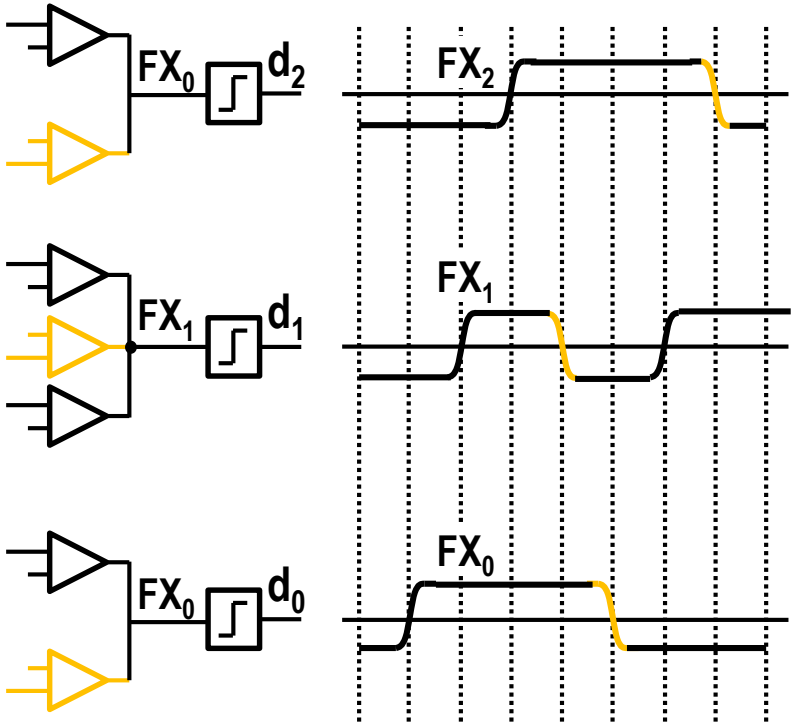
- Midpoint ZX is redefined in each parallel channel causing alignment issue, potential algorithmic conflict and large quantization error.

Binary Search Without Algorithmic Conflicts

One-step parallel binary search without redefining ZXs ➔ Gray code

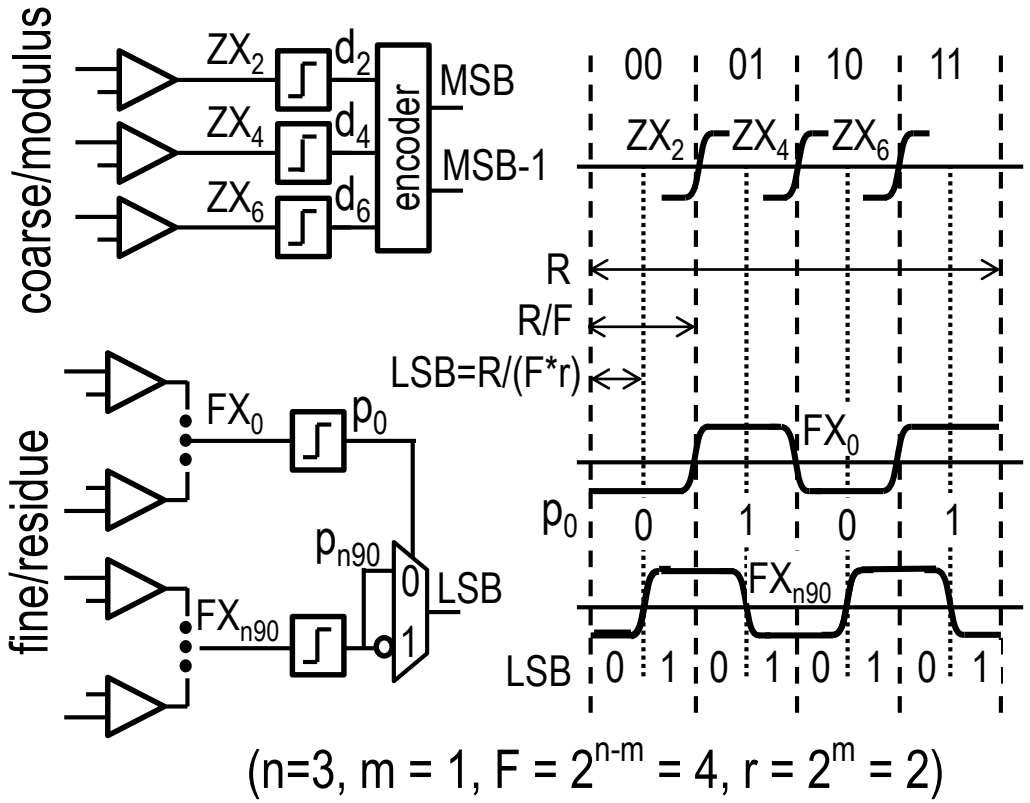


An arbitrary Gray code variant (one bit flip between adjacent R_i's)



- Gray codes are robust without redefining ZXs.
- One step, total 2^n ZGs but n instead of 2^n ZDs.

Parallel Coarse-Fine Search: Modulus-Residue Code



Bit-Sync (align redefined ZXs):

$\text{MSB-1} \overset{s=1}{\Longrightarrow} (\text{MSB-1})_s$

$\text{MSB} \overset{s=1}{\Longrightarrow} (\text{MSB})_s$

where $s = (\text{MSB-1}) \oplus p_0$

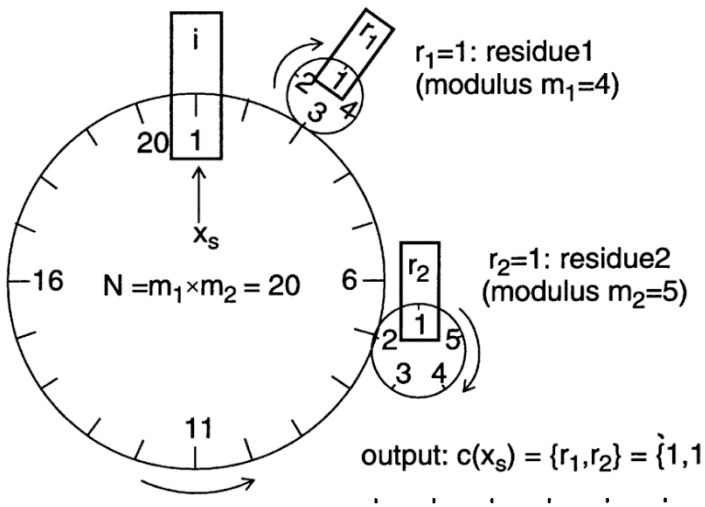
(see next page)

Output Binary Code:

$C = (\text{MSB})_s(\text{MSB-1})_s(\text{LSBs})$

- (F-1) ZXs (e.g. $ZX_{2,4,6}$) in coarse channels divide R into F folds.
- Fine foldings (e.g. FX_0, FX_{90}) divide each fold (R/F) into r LSBs.
- Bit-sync aligns coarse ZXs to fine channels. [*van de Grift, JSSC 1987*]

Parallel Residue Search: Residue Encoding



- Based on Chinese remainder theorem
- Enable carry-free addition
- Optical implementation
- Overwhelming bit-sync

output: $c(x_s) = \{r_1, r_2\} = \{1,1\}$

x' Q(x') = 14 ⇒ (2,4)

i: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

modulo 4 channel
(r_1 = i mod 4)

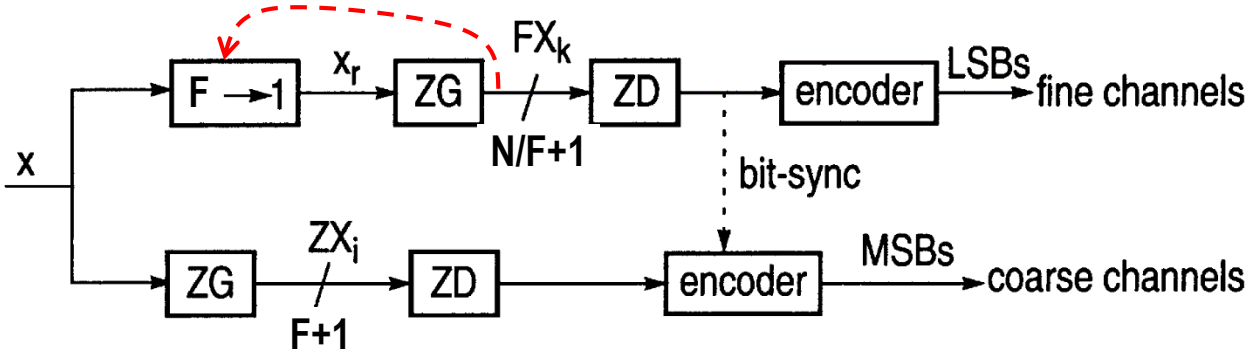
r_1: 1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4 x

modulo 5 channel
(r_2 = i mod 5)

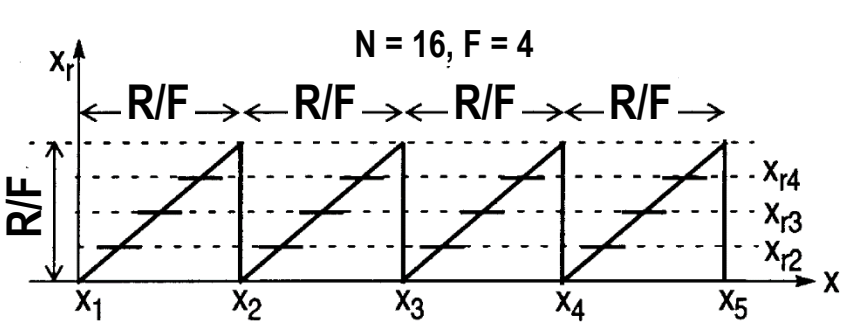
r_2: 1 2 3 4 5 1 2 3 4 5 1 2 3 4 5 1 2 3 4 5 x

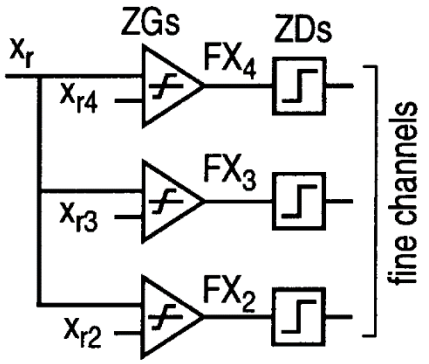
- Each symbol represents an independent partial search/quantization.
- Each encoding system represents a partition and search algorithm.

Pre-ZG Folding Reduces ZG Complexity



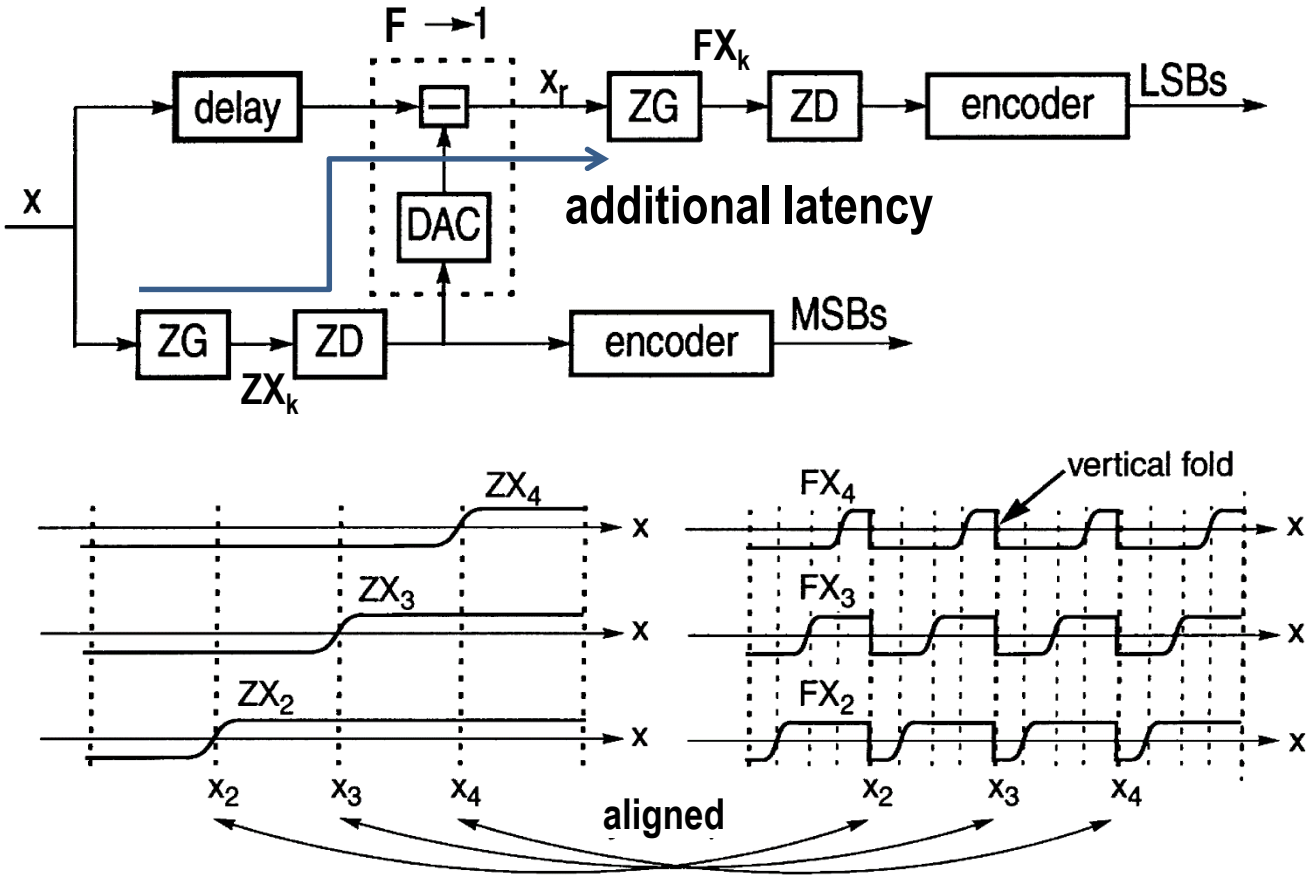
F-fold signal folding





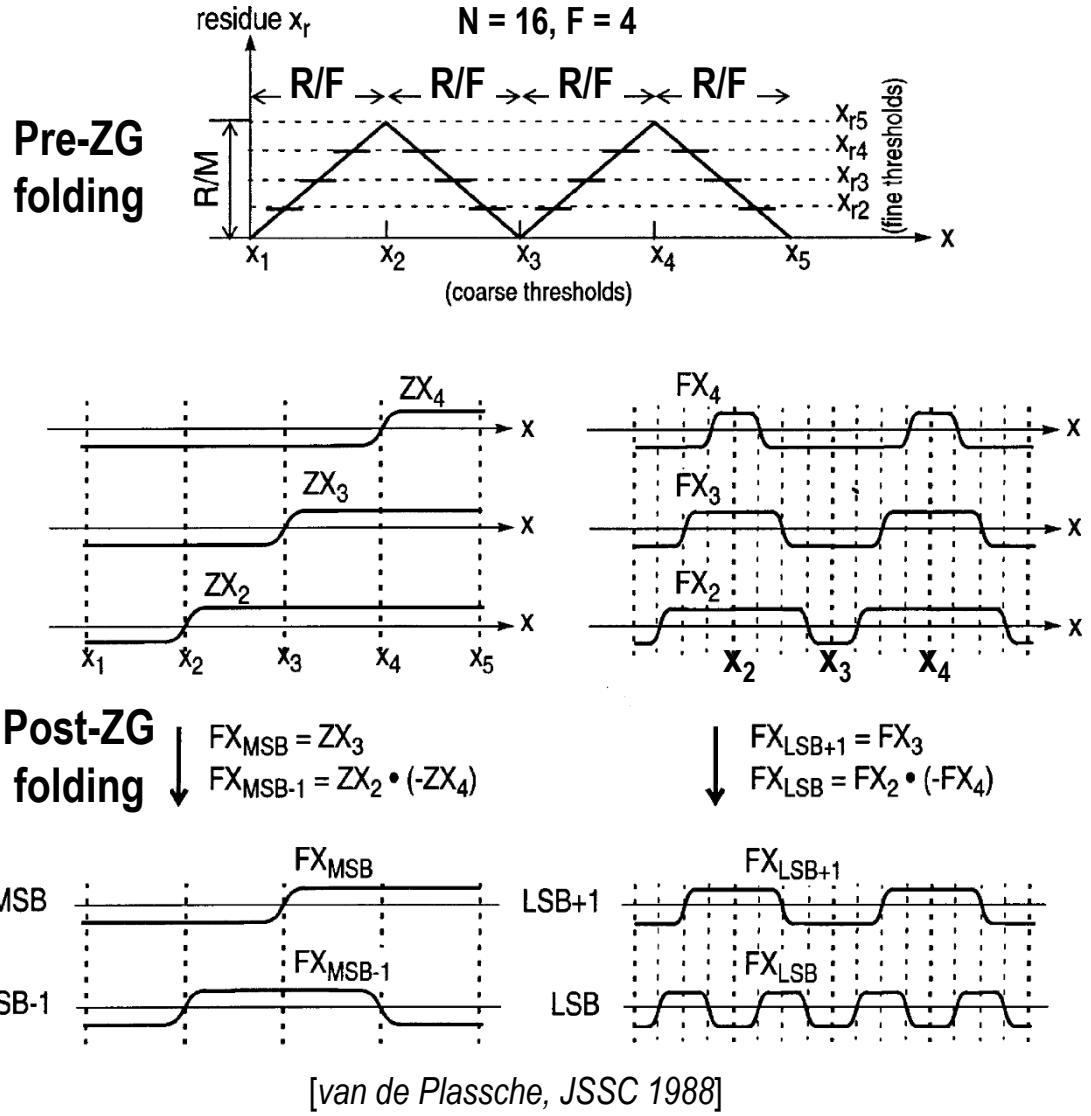
- F ➔ 1 mux(folding) moved before ZG to reduce both ZGs and ZDs by F
- Overhead: folding linearity, coarse quantizer to resolve 1 ➔ F ambiguity

Serial Folding without Bit-Sync Issue



- Serial folding operation ensures bit sync at the cost of latency and matching.
- Analog delay can be avoided with a S/H driving both coarse and fine channels.
- Coarse threshold error does not matter if folding signal falls in fine quantizer FS.

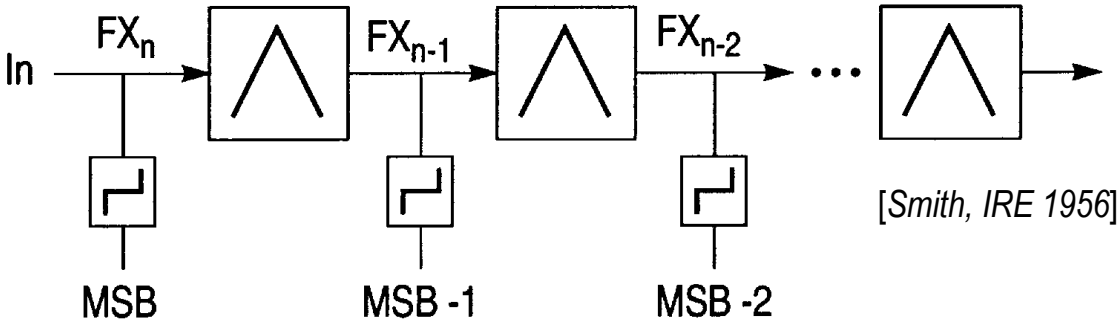
Parallel Folding without Bit-Sync Issue



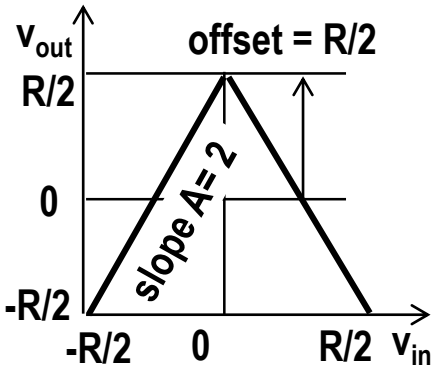
[*van de Plassche, JSSC 1988*]

- Parallel coarse-fine channels: low latency
- No vertical folding: robust quantization
- Gray code: no bit-sync and low complexity
- Rounded folding tip: linearity bottleneck

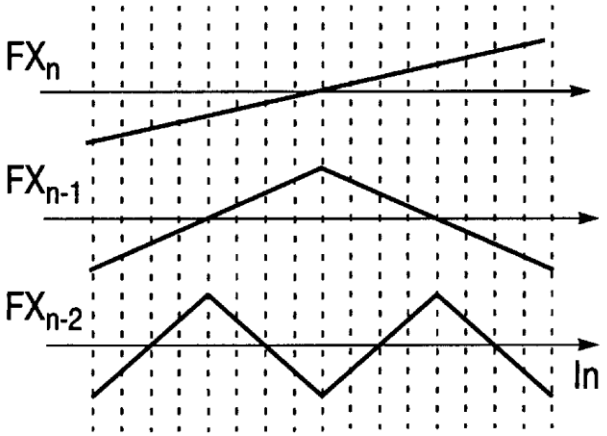
Ripple Through Folding for Gray Coding

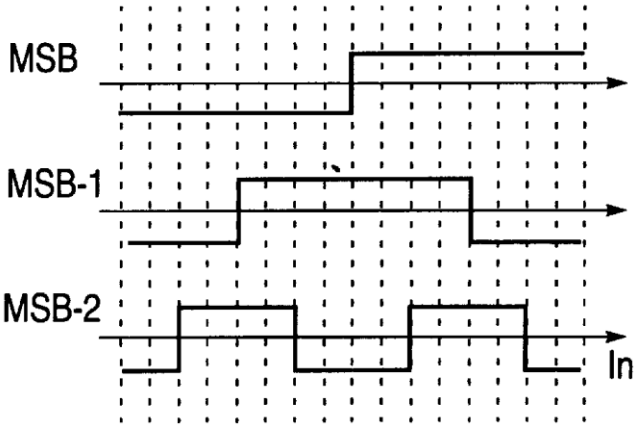


[*Smith, IRE 1956*]



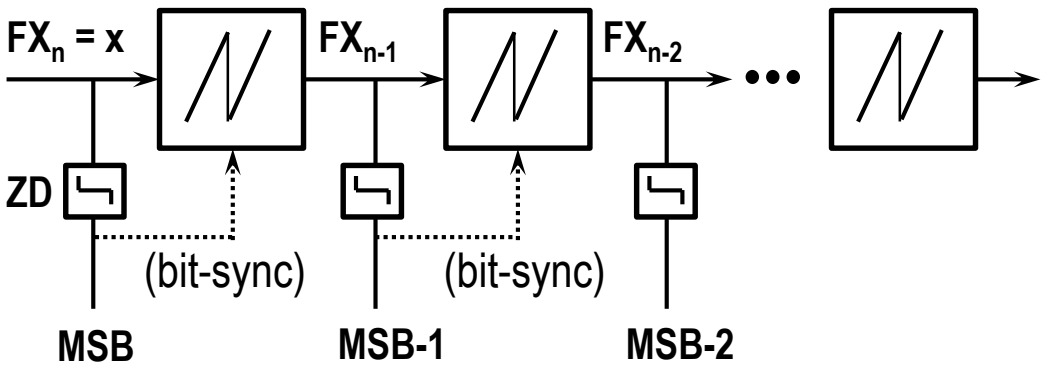
$v_{out} = offset - A|v_{in}|$

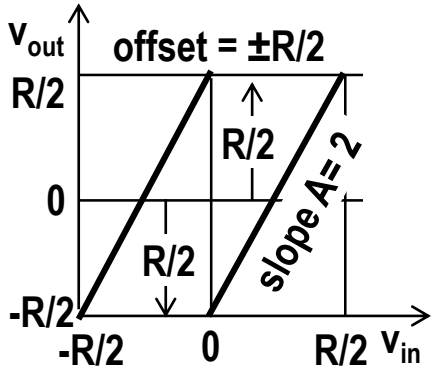




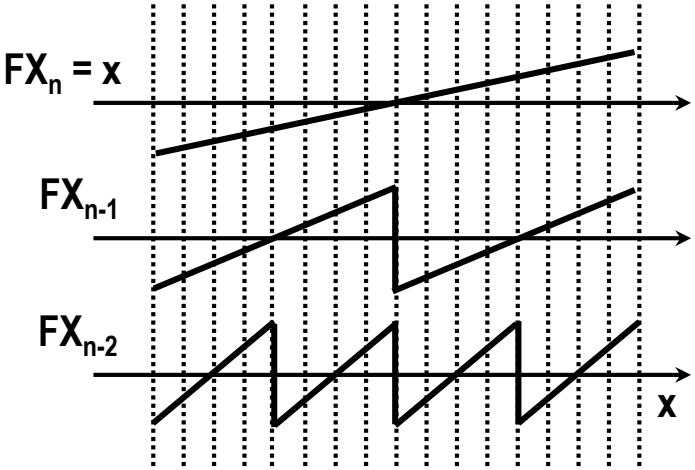
- Efficient discrete (rectifier based) ADCs for PCM, video and radar.
- $FS_{out}(i) = 2 * offset(i)$ should match $FS_{in}(i+1) = 4 * (offset(i+1) / A(i+1))$.
- A = 2 is not required as long as $offset(i+1) = (A(i+1) / 2) * offset(i)$.

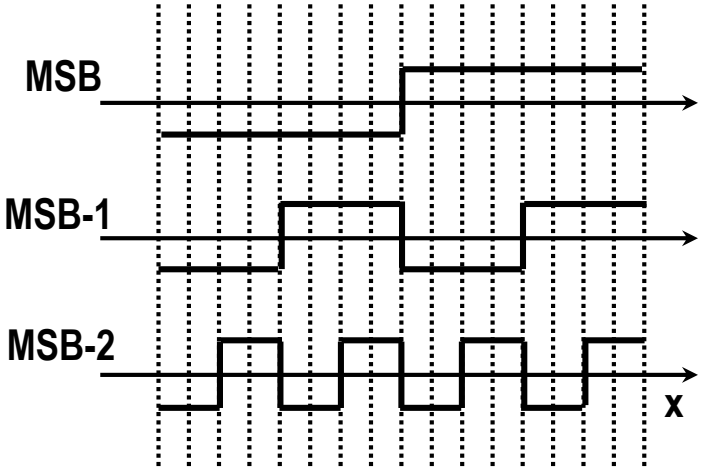
Serial Folding for Binary Coding





$v_{out} = Av_{in} + (R/2)\text{sign}(v_{in})$

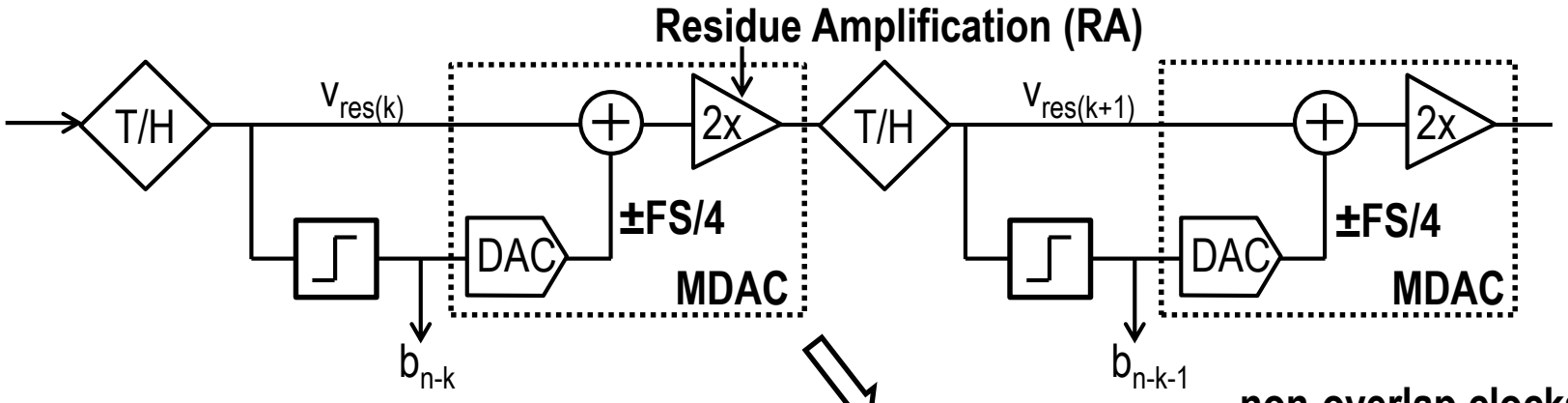


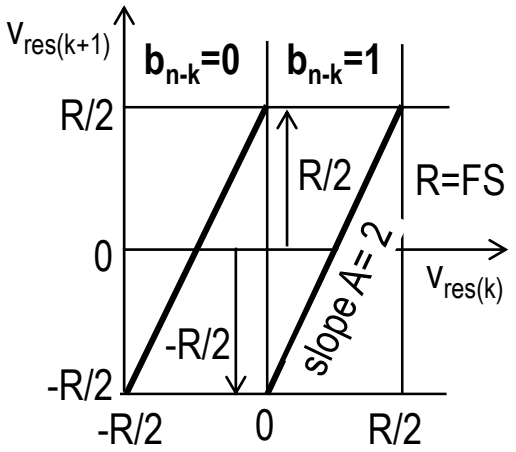


- Vertical folds requires the ZD-like decision and serial operation.

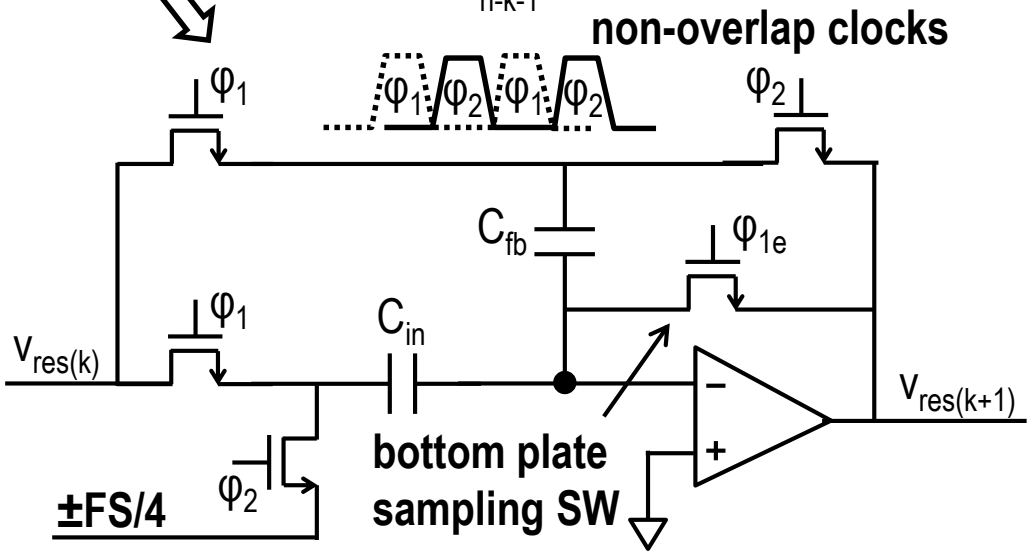
Pipelined Folding Using MDAC Summation

A 1b/stage Pipeline ADC using Multiplying D/A Converters (MDACs)





$v_{out} = 2(v_{in} \pm FS/4)$

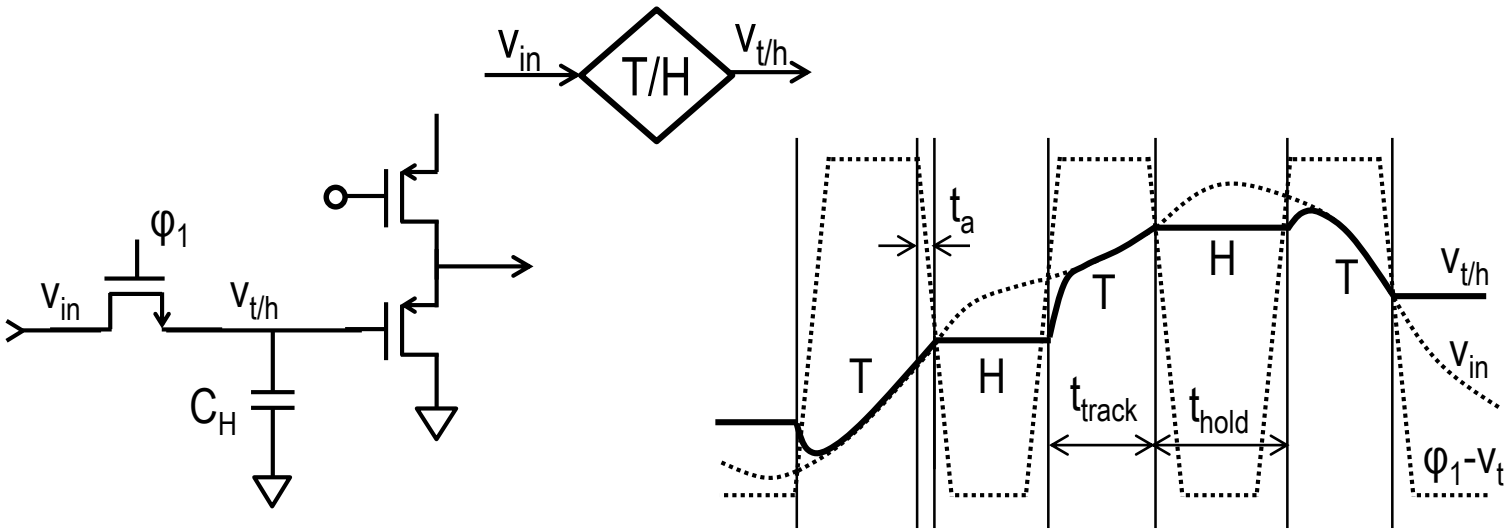


Discussions on Signal Folding

- Signal folding reduces quantizer complexity using F=>1 operation on the analog signal (analog folding) or the ZX signals (ZX folding),
- The F=>1 runs automatically involving no regeneration in parallel search based quantizers, preserving low latency and high speed.
- Automatic folding is popular in bipolar process where rectifiers are readily available to fold signals independent of any serial detection.
- Ripple-through cascaded V-shape folding was the only practical option for high speed A/D converters before the advent of IC.
- Folding involving serial regeneration is popular in CMOS where switch cap circuits are readily available to pipeline the serial folding.
- However, analog folding suffers nonlinearity at the folding tips; ZX folding suffers mutual loading & interference among the ZX signals.

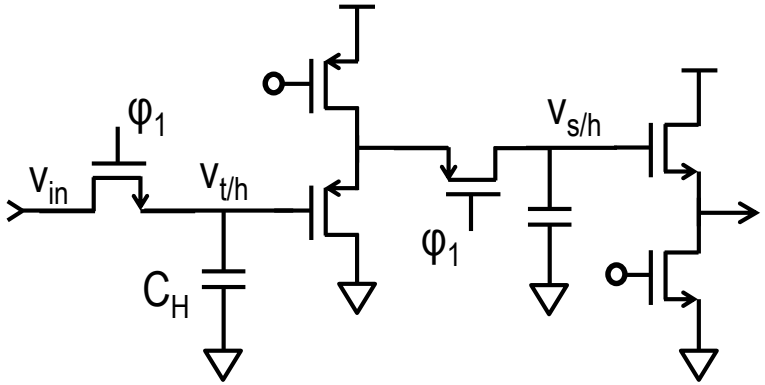
Circuit Implementations

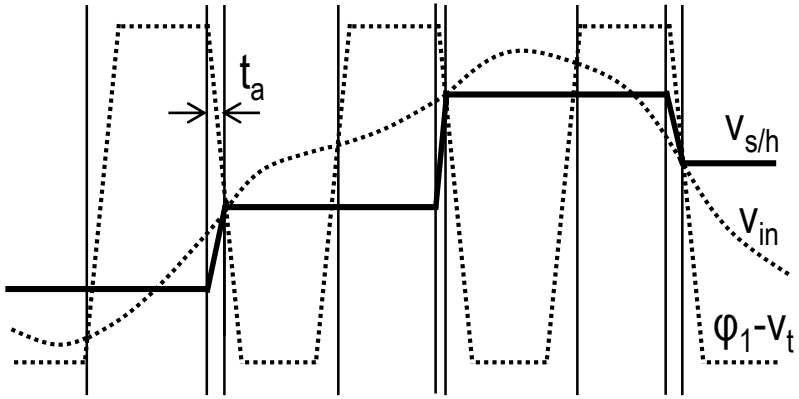
Open-Loop Track/Hold (T/H)



- Sampling aperture time t_a << $1/f_{in}$ limited by clock edge.
- Tracking BW_{track} > f_{in} limited by MOSFET f_T, power, etc.
- Very high speed but resolution limited by errors from charge injection, aperture time/jitter, switch and source follower nonlinearity, etc.

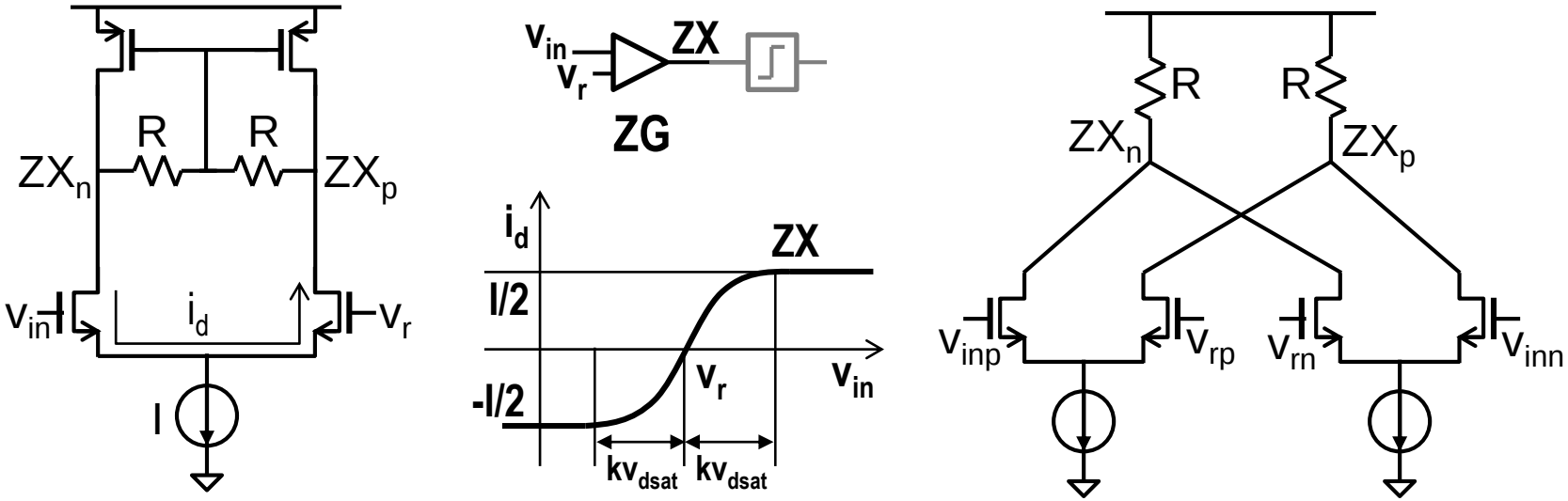
Open-Loop Sample/Hold (S/H)





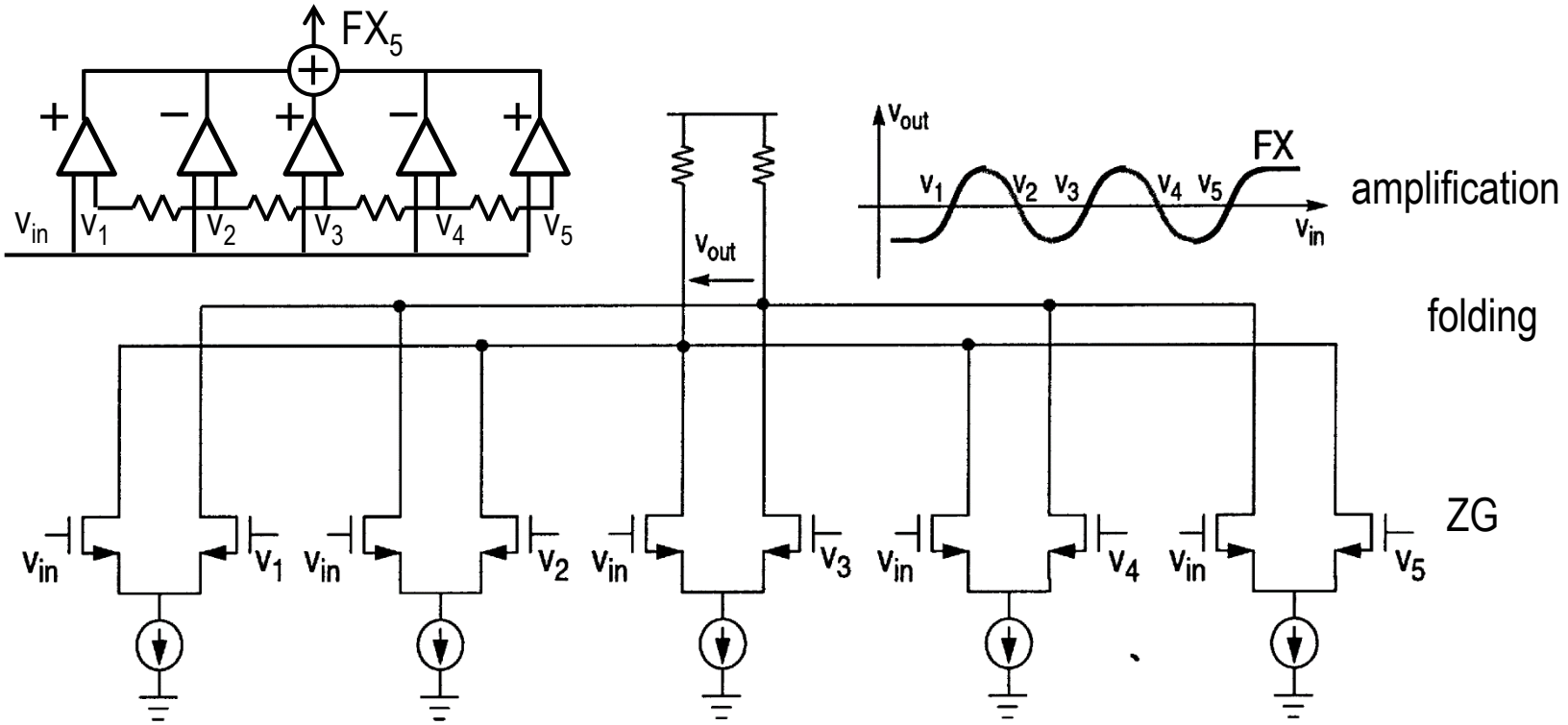
- Doubled settling time for succeeding quantizer
- Doubled power and noise from double T/Hs

Difference Amplifier (Preamp) for ZX Generation (ZG)



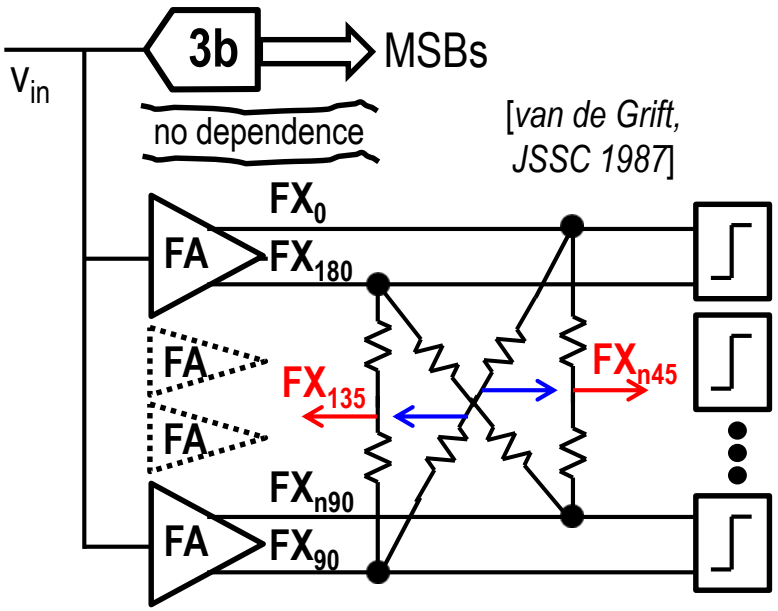
- Diff. output current i_d clips to $\pm I/2$ for $|v_{in} - v_r| > kV_{dsat}$, $k \sim \sqrt{2}$.
- Diff. input and reference are applied to input diffpairs in p-p and n-n combinations to avoid ZX error from the current clipping.
- Preamp merges amplification with ZG to mitigate ZD errors by buffering ZD kickback and reducing input referred ZD offset.

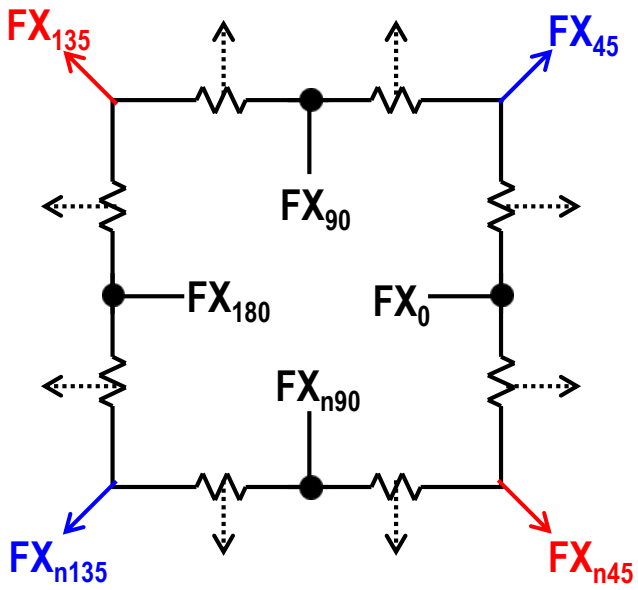
Post-ZG Folding by Summation

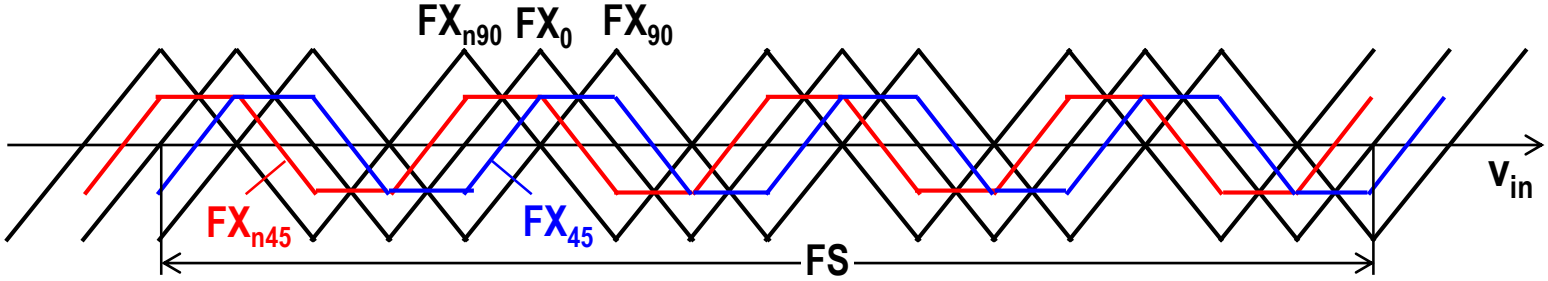


- Merged ZX generation, amplification, and folding
- Ideally, no interaction among odd number of folds (ZXs)
- Subject to all error sources and mutual loading

Additional Folding Signals from Interpolation

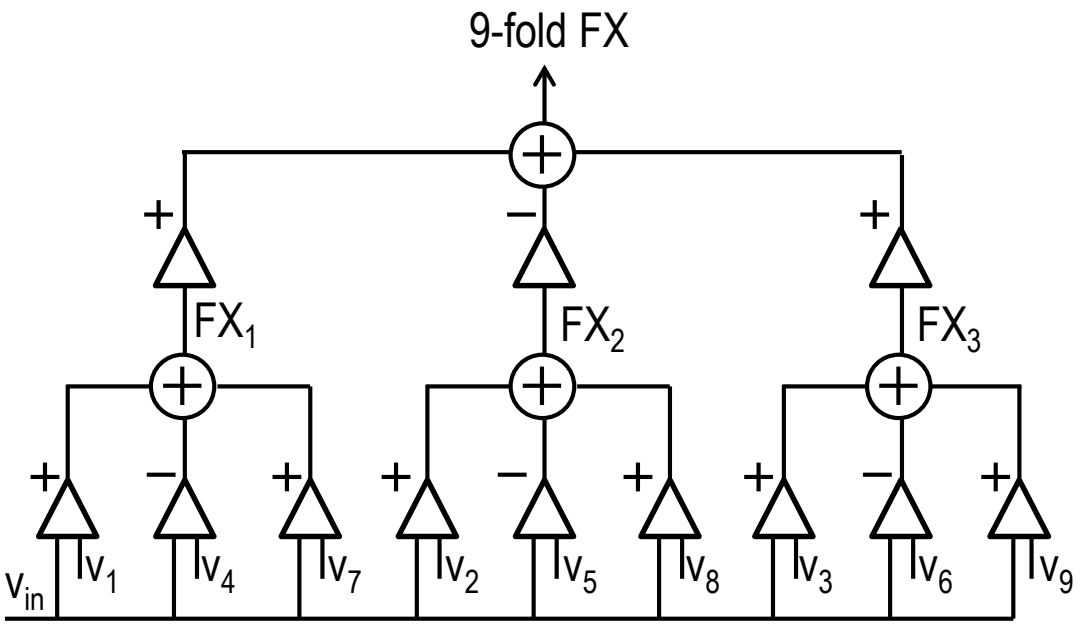




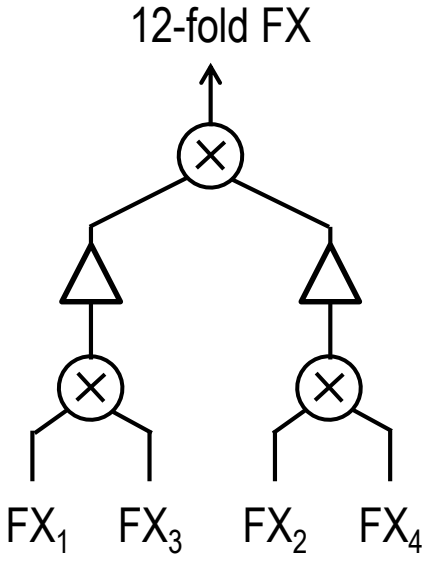


- No interaction between the folding signals
- No linearity requirement for 2x interpolation

Multi-Step Folding



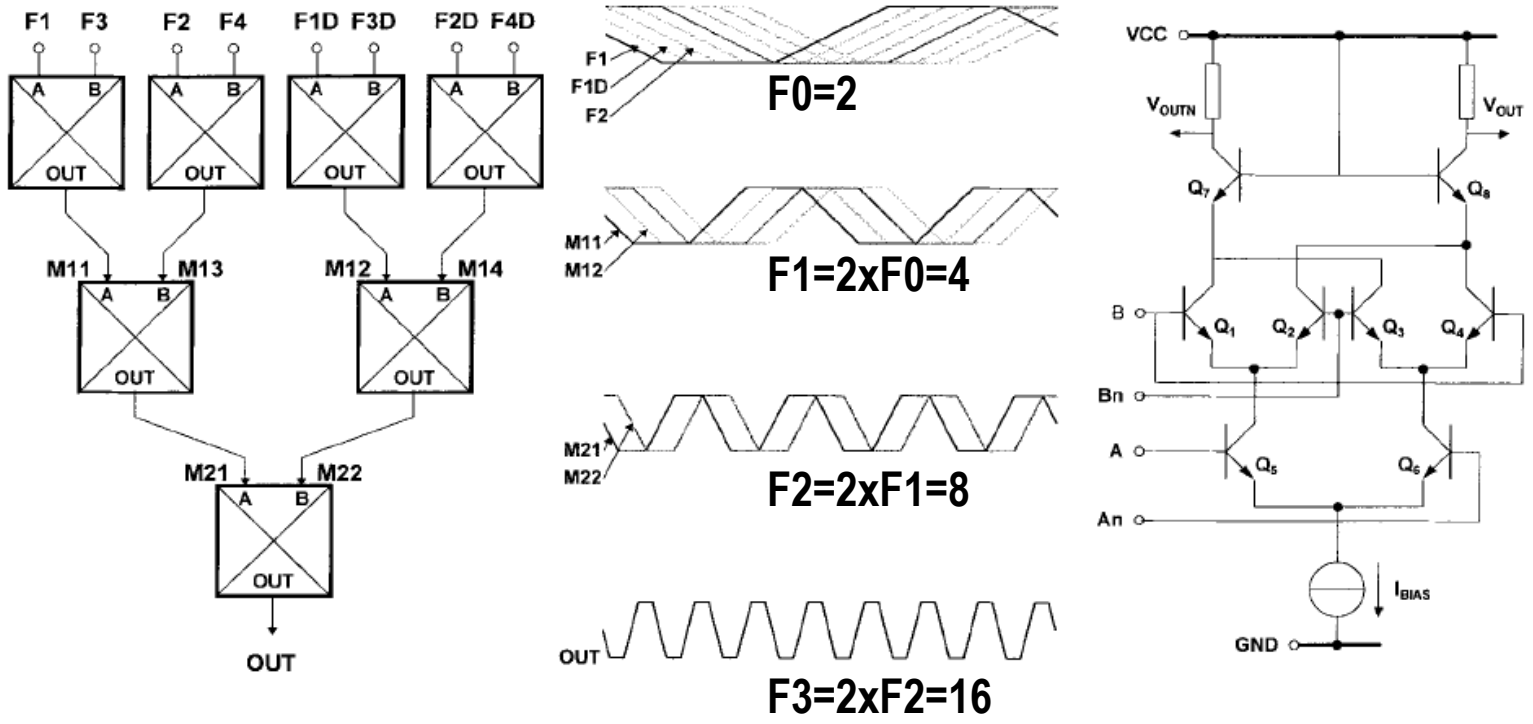
[*Bult, JSSC 1997*]



[*Vorenkamp, JSSC 1997*]

- ZXs are combined in multiple steps to avoid excessive output loading.
- Multistep folding is merged with multistep amplification for better BW.
- Pipelining is possible but is against the purpose of “flash” operation.

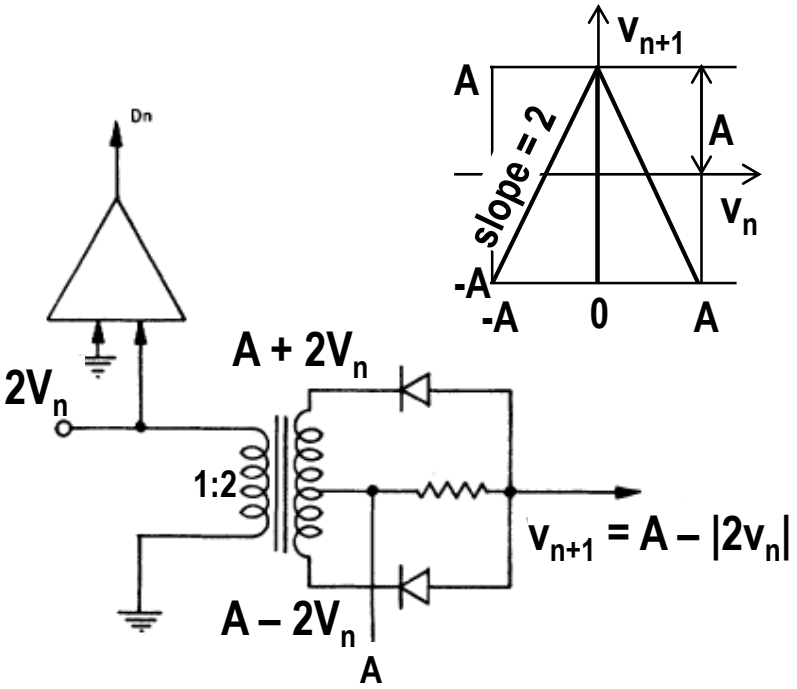
Post-ZG Folding by Multiplication



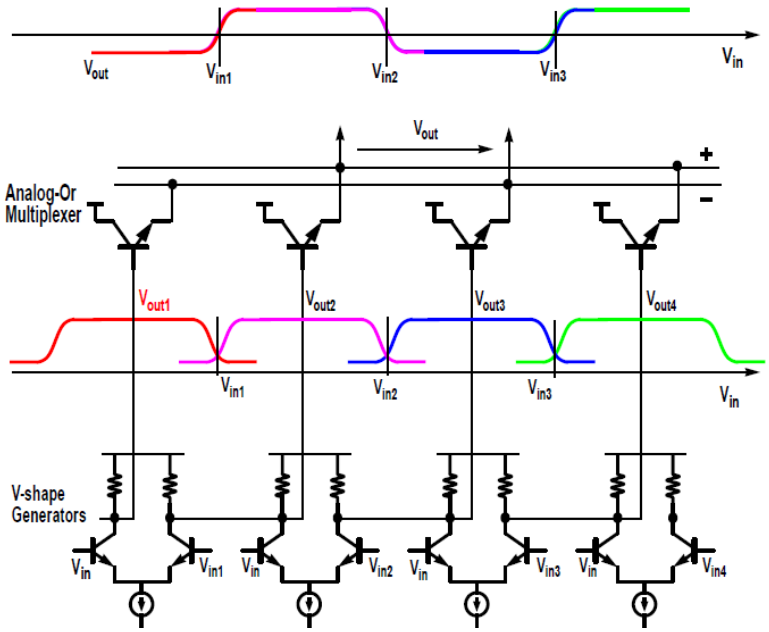
[*Vorenkamp, JSSC 1997*]

- Multiplier (e.g. Gilbert Cell) output preserves all input ZXs.
- Cascaded multiplications combine folding signals into one.

Folding with Min/Max Follower(s)



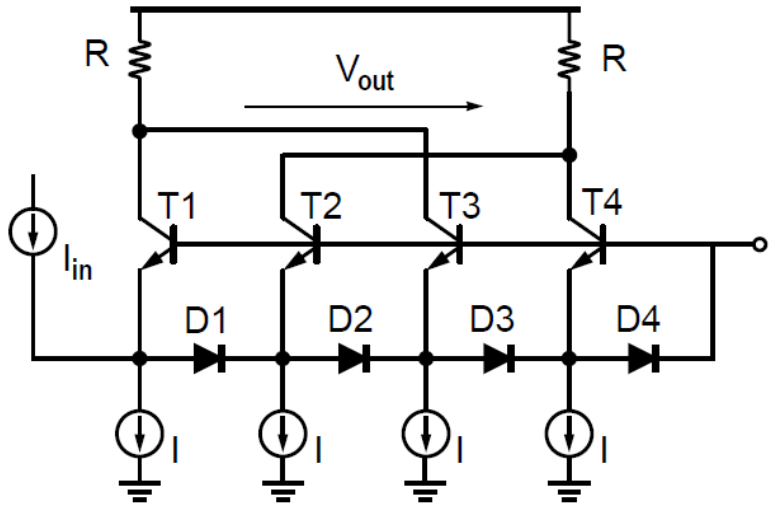
(a) [*Smith, IRE 1956*]



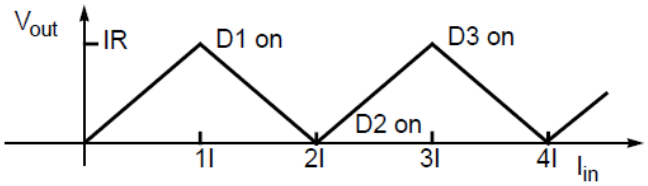
(a) [*van de Grift, JSSC 1987*]

- In (a), the diodes selects the *min* of the two voltages $A \pm 2v_n$ to realize a V-shape folding output: $v_{n+1} = A - |2v_n|$.
- In (b), the output emitter followers select the *max* among the input V-shape foldings and stitch them by alternating their polarity.

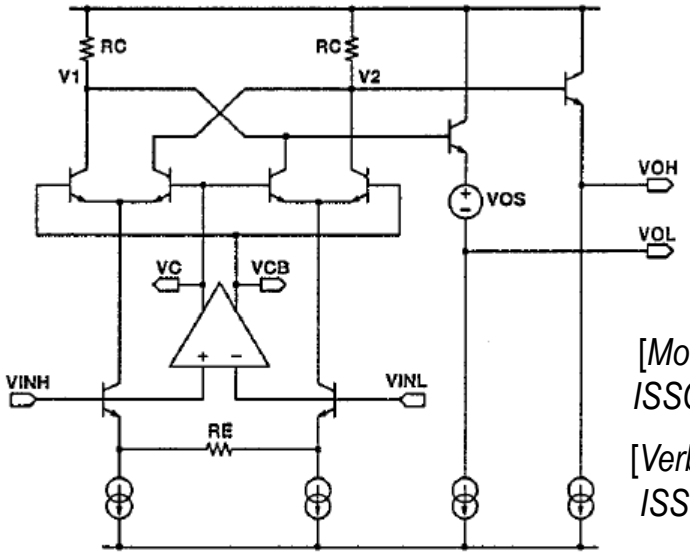
Folding by Rectifier Self-Switching



[*van de Plassche, JSSC 1979*]

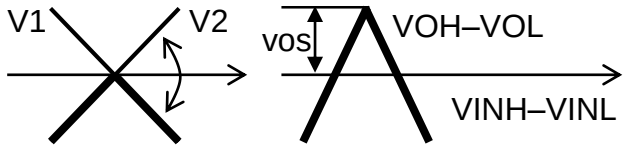


(a)



[*Moreland, ISSC 1995*]

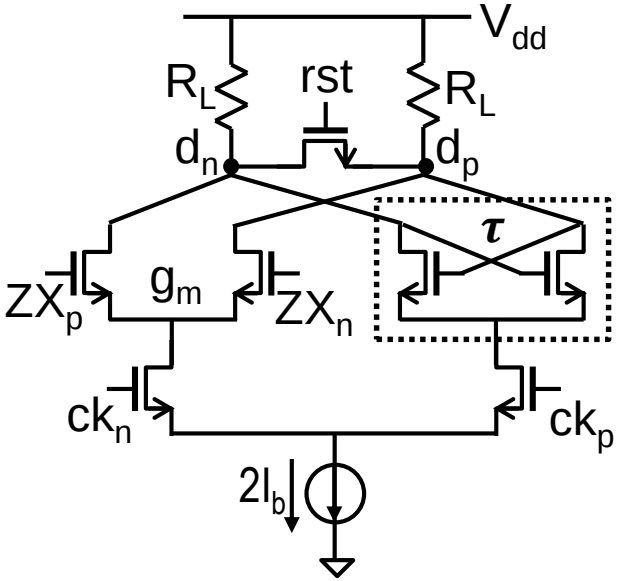
[*Verbruggen, ISSC 2008*]

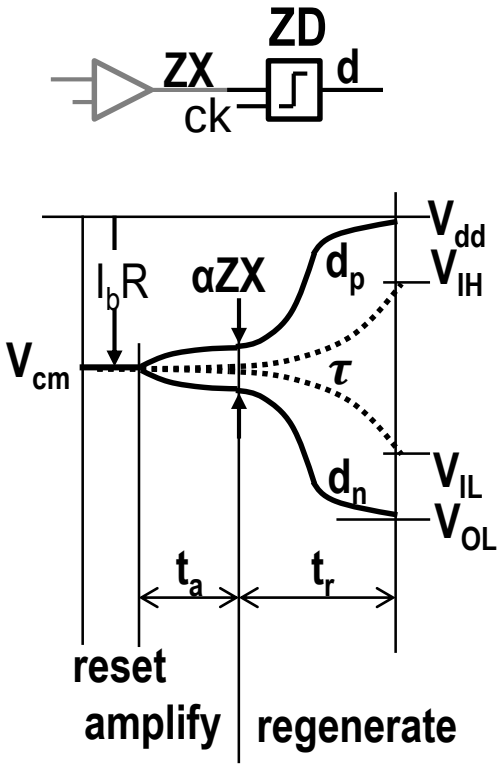


(b)

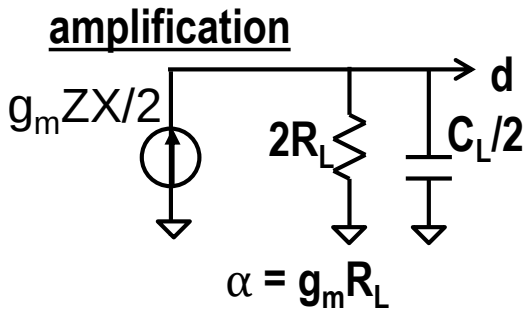
- At $I_{in} \geq kI$, Tk shuts off, Dk turns on, I_{in}–kI switches side by T(k+1).
- At (b) output, input signal multiplies its polarity by self-switching.
- ZX is detected by an op-amp instead of a regenerative latch (ZD).

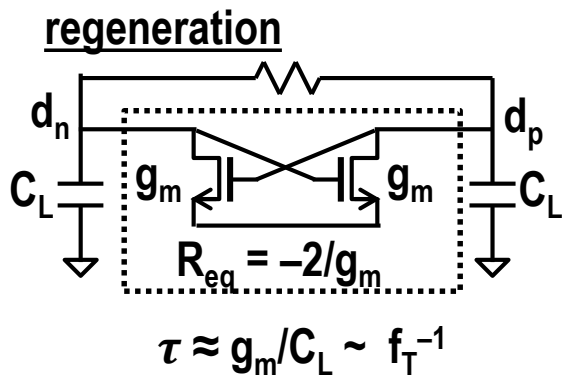
Static CML Latches for ZX Detection





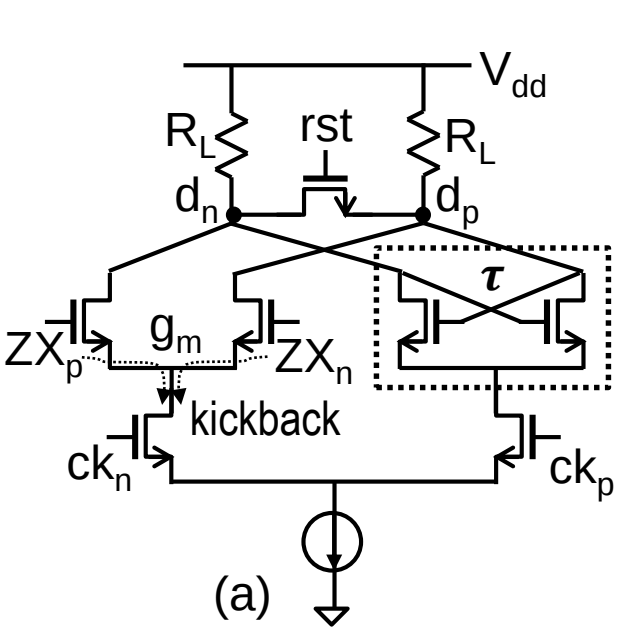
$$A \equiv d/ZX \approx \alpha e^{t_r/\tau}$$



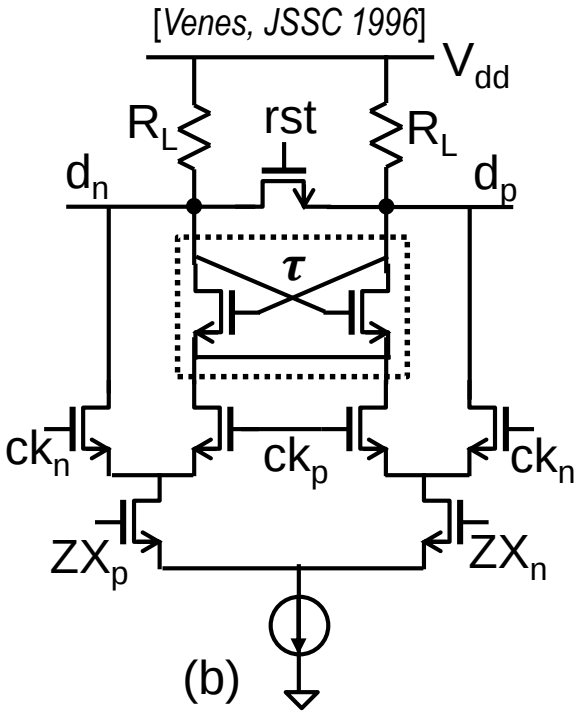


- ZD uses latch regeneration (positive feedback) to maximize the gain.
- Two-phase operation: tracking/amplification & sampling/regeneration.
- Regeneration speed or time constant (τ) is limited by technology (f_T).

Static CML Latch Improvements



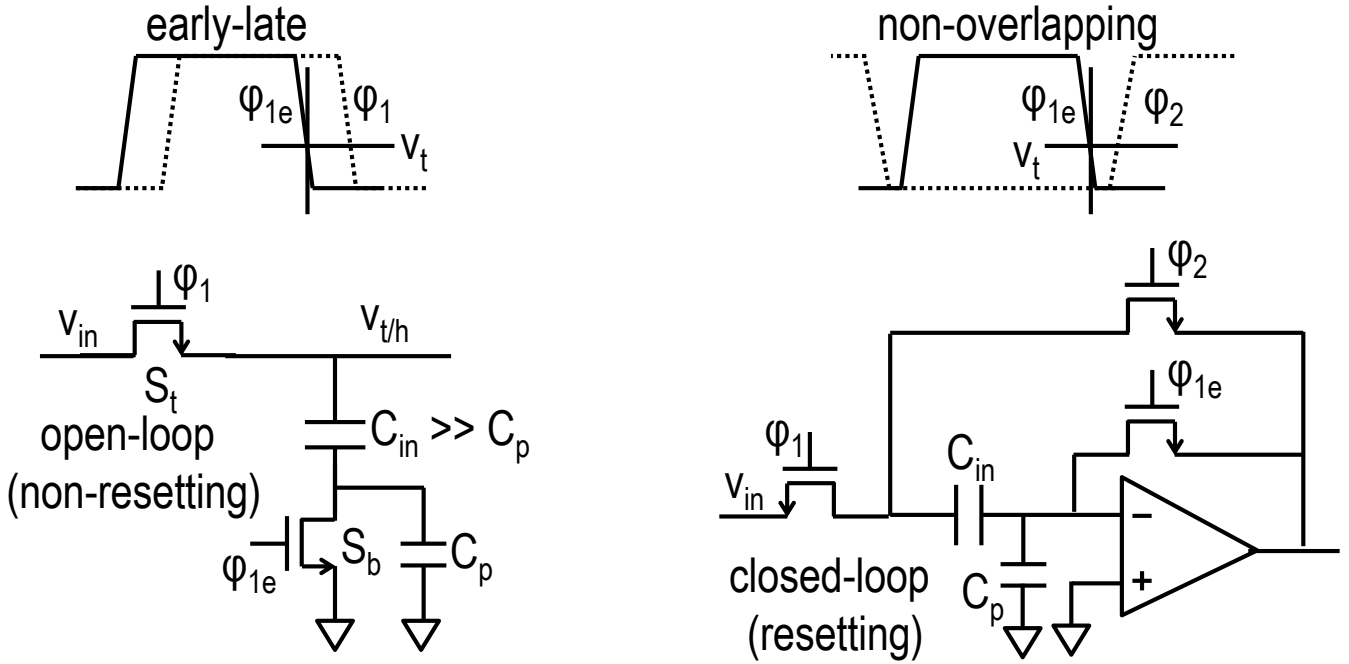
[*Venes, JSSC 1996*]



- Steady bias current and output CM avoids dynamic offset.
- Kickback is in (a) but not in (b) with balanced clocks isolating output.
- Input feedthrough is also blocked by the stacked clock diffpairs in (b).
- A reset pulse (rst) before amplification helps to erase the hysteresis.

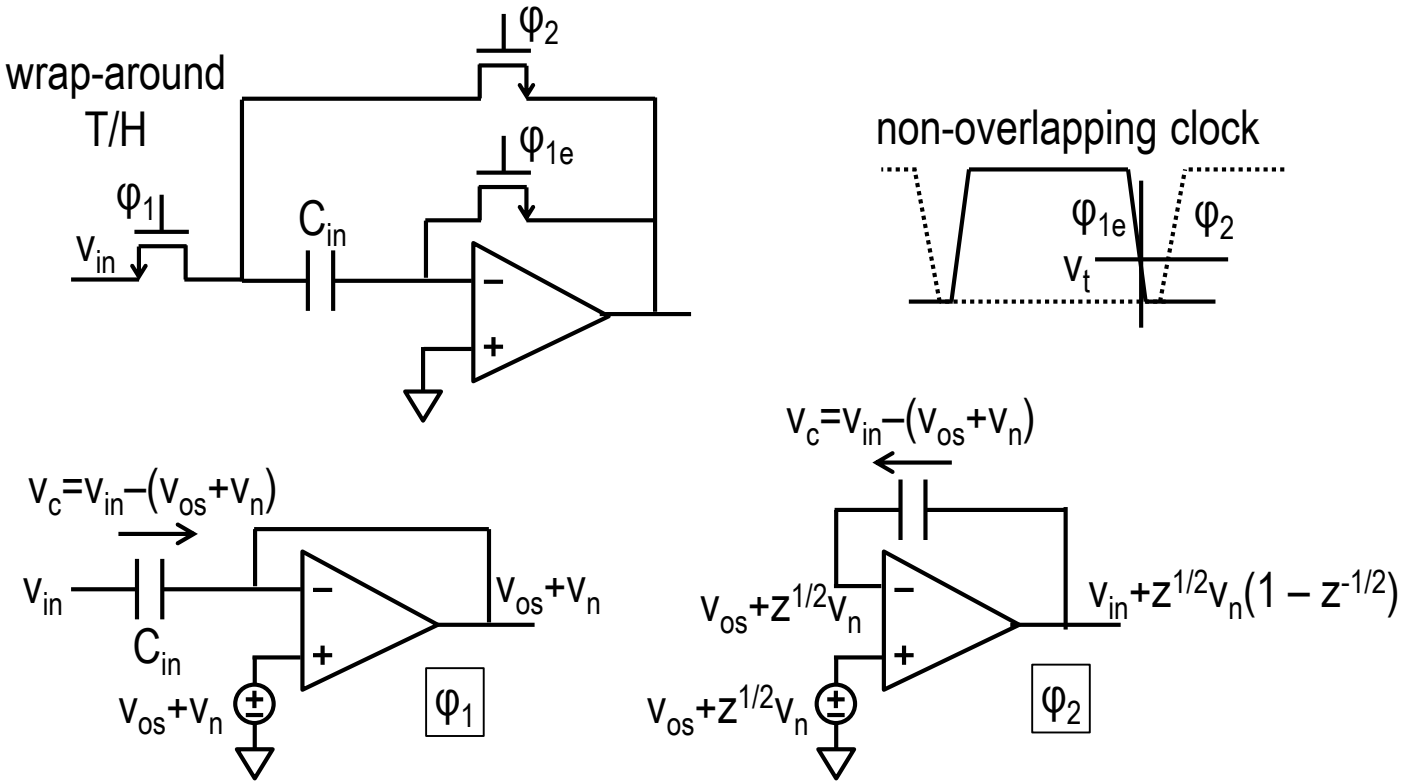
Imperfections and Corrections

T/H Bottom-Plate Sampling



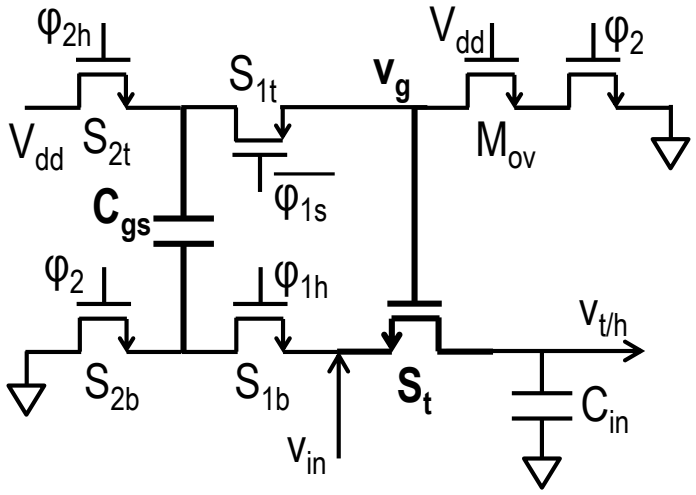
- Bottom plate switch S_b opens before top-plate switch S_t.
- Switch S_b determines the sampling time and aperture.
  - Imperfections are signal independent.
- Closed-loop virtual ground removes parasitic (C_p) effect.
  - Eliminate error from charge injection/feedthrough.

Offset Auto-Zeroing and Correlated Double Sampling

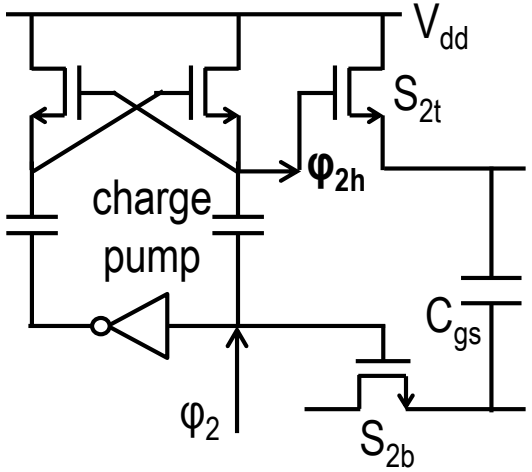


- Offset is sampled on C_{in} and cancelled in next phase.
- Op-amp input referred noise is filtered by $(1-z^{-1})$.
- Auto-zeroing is based on correlated double sampling (CDS) as slow varying op-amp offset is sampled twice in each cycle.

Input Switch Gate Bootstrapping

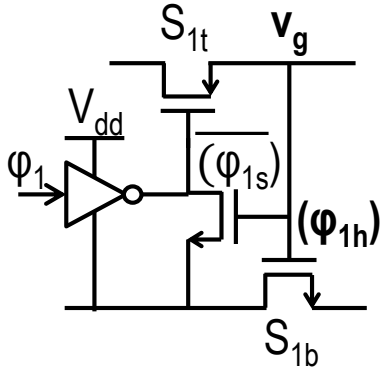


(a) S_t bootstrapped with C_{gs}



(b) high-V clock φ_{2h}

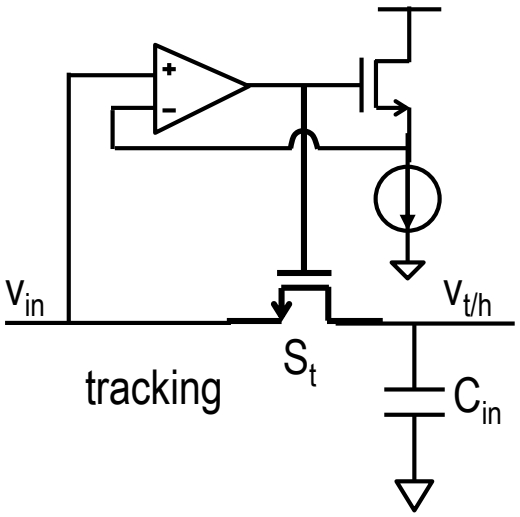
[*Abo, JSSC 1999*]



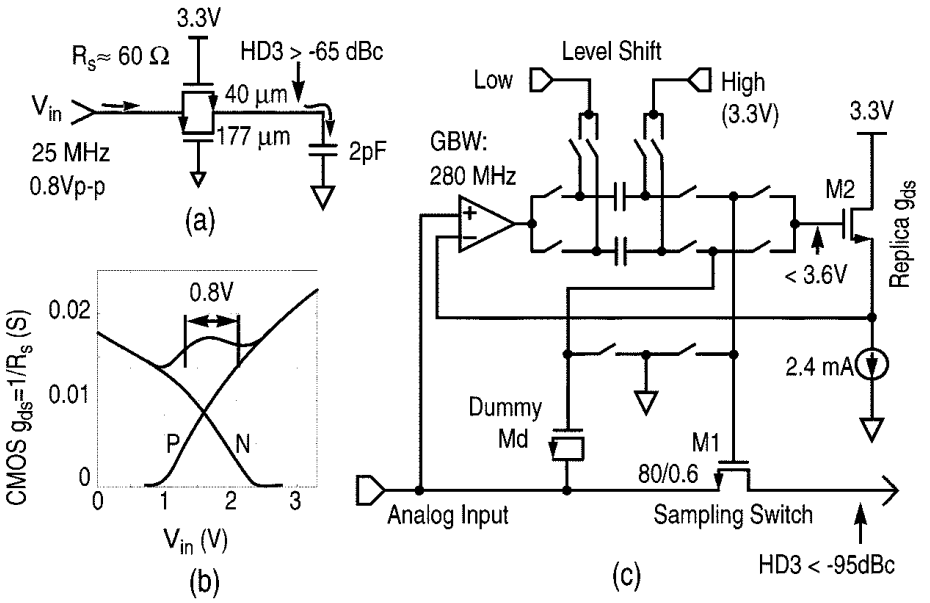
(c) high-V clock φ_{1h}

- Input switch gate is bootstrapped with $v_{gs} = V_{dd}$ free of OV.
- S_t on-resistance R_{sw} is linearized except for body effect.
- Potential reliability issue with node voltage $\mathbf{v_g}$, $\boldsymbol{\varphi_{2h}} > V_{dd}$.

Closed-Loop Switch Gate Bootstrapping



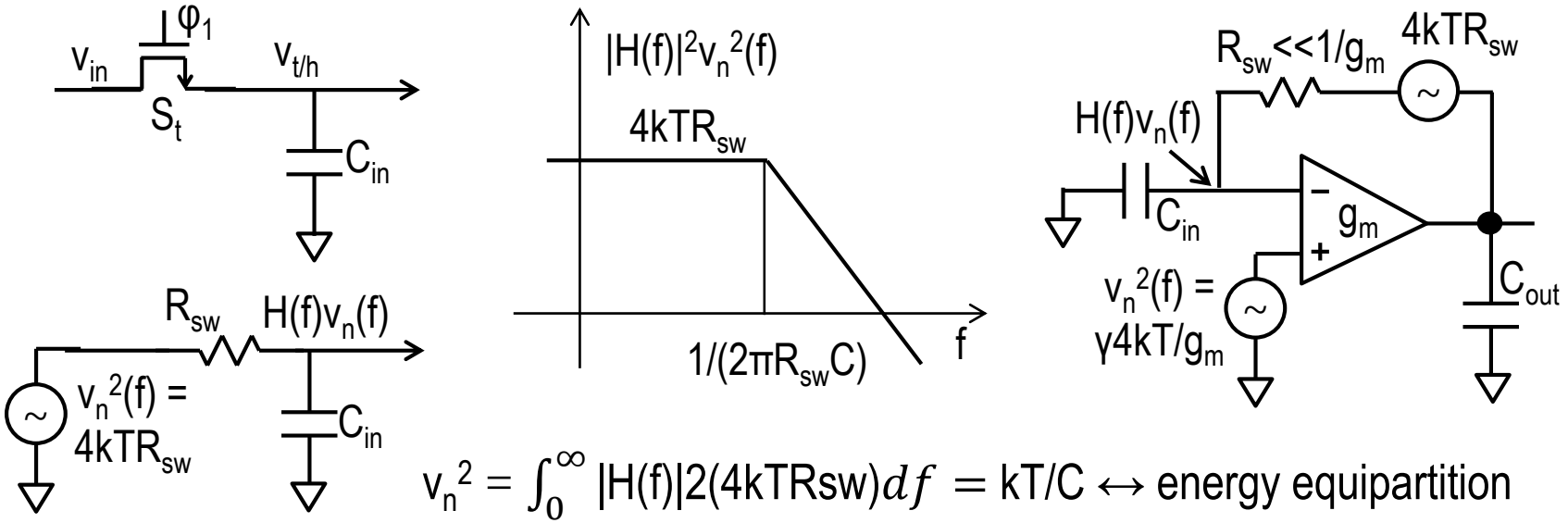
(a) closed-loop bootstrapping



[*Pan, JSSC 2000*]

- Super-linear switch with body effect compensated
- Less reliability concern with lower overvoltage
- Too much power for the op-amp driving the gate

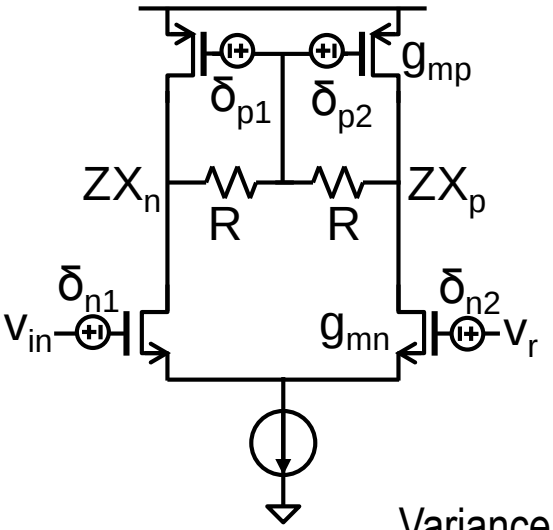
KT/C Noise from Switch and Op-amp

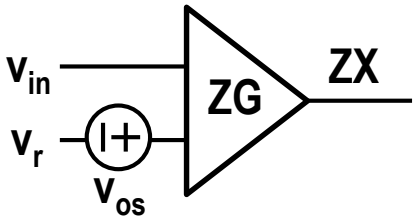


$v_n^2 = \int_0^\infty |H(f)|2(4kTRsw)df = kT/C \leftrightarrow$ energy equipartition

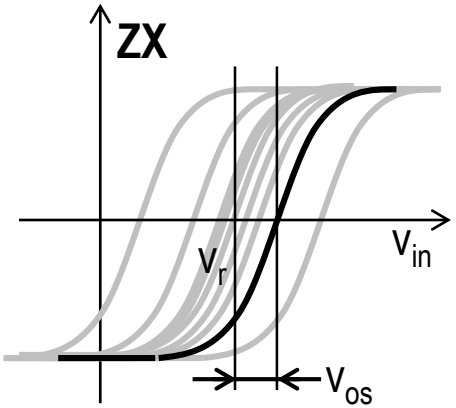
- Effects of R_{sw} (or g_m) on noise BW and level cancel each other.
- Each sampling (NOT each switch) incurs KT/C noise across C_{in}.
- Noise power inversely proportional to C and therefore power.
- Large signal is preferred to reduce C and current quadratically.
- Autozeroing ($1-z^{-1}$) is not effective on KT/C thermal noise.

Preamp Input Referred Offset: ZX Error





v_{os}: input referred offset

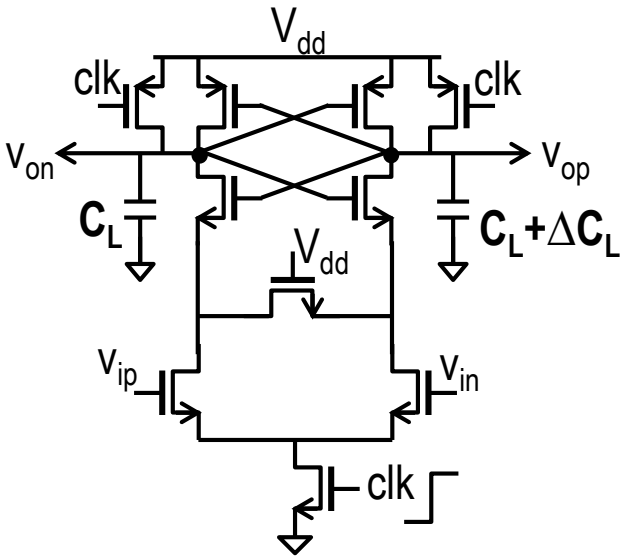


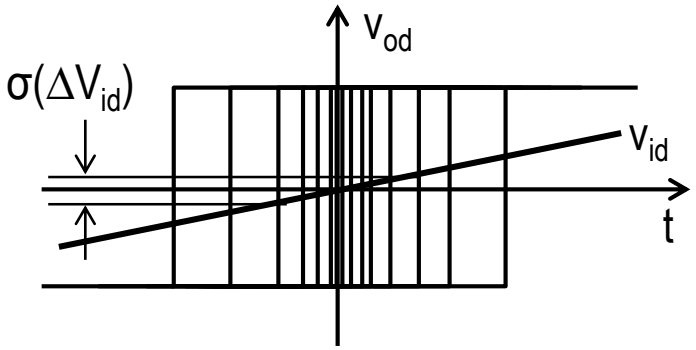
$$v_{os} = \delta_{n1} - \delta_{n2} + (\delta_{p2} - \delta_{p1})(g_{mp}/g_{mn})$$

$$\text{Variance: } (\sigma_{os})^2 = 2(\sigma_{vt\_n})^2 + 2(\sigma_{vt\_p})^2 (g_{mp}/g_{mn})^2$$

- Preamp offset arises from mismatch in MOSFET threshold V_t, carrier mobility, size, output load, etc.
- Static preamp offset is mitigated by auto-zeroing, sizing, averaging/spatial filtering, calibration, etc.

Latch Dynamic Offsets and Simulations

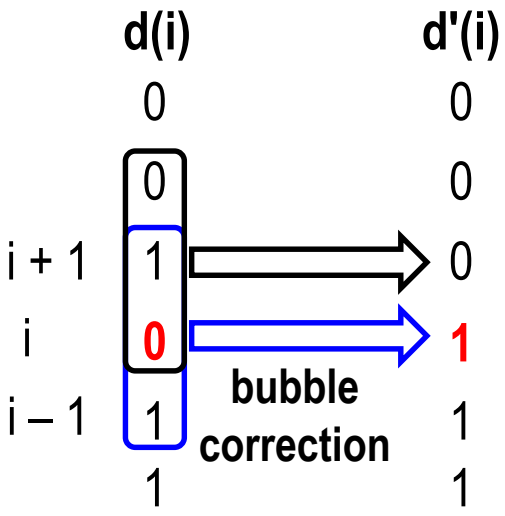




Transient Monte Carlo simulations for evaluation of input referred offset $\sigma(\Delta V_{id})$

- Latch switching activities cause dynamic offsets [*Kim, TCAS1 2009*]
  - Due to CM-to-DM conversion (e.g. $\Delta V_{out} = (\Delta C_L/C_L)\Delta V_{cm}$)
  - Due to kick back to input stages such as reference
  - Due to clock/signal feedthrough and noise coupling
  - Sensitive to supply, clock/signal, temperature, parasitic variations
  - Hard to be corrected, usually mitigated with preamps
- Dynamic offsets are simulated with clock running and input swept

Flash-ADC Bubble Error Correction



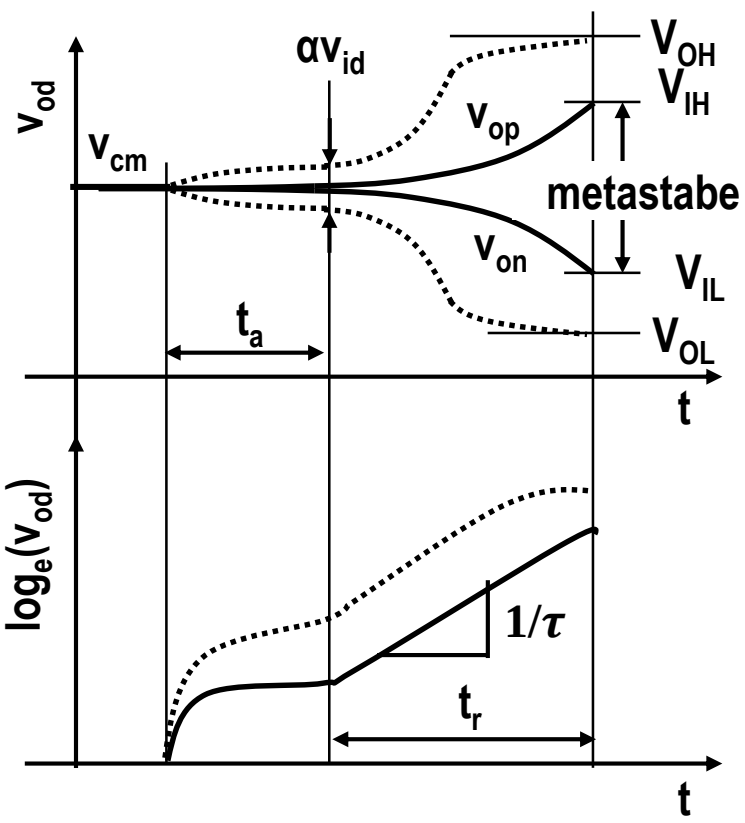
majority vote:
d'(i) = 1 when 2 out of 3
immediate neighbors are 1

d'(i) =
d(i-1) * d(i) + d(i) * d(i+1) + d(i-1) * d(i+1)

[*Mangelsdorf, JSSC 1990*]

- Adjacent comparator thresholds may cross each other, causing bubbles in the thermometer code and sparkle error
- This may happen in high speed ADCs due to excessive comparator offset and clock skew among adjacent comparators.
- Bubbles are detected and corrected by looking at more than two adjacent bits as is done in the majority vote scheme.

Latch Regeneration and Metastability

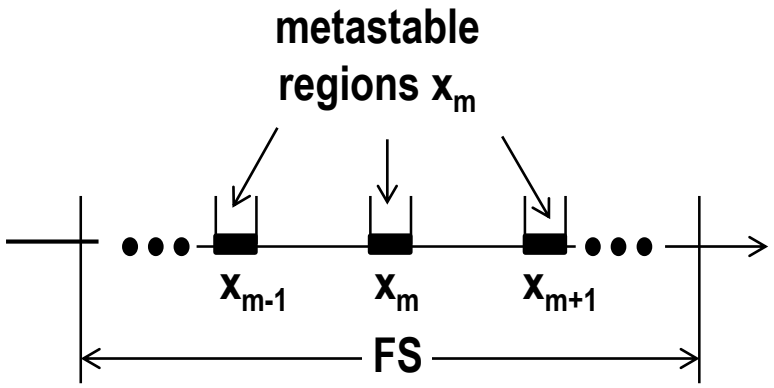


$$A = \alpha e^{t_r/\tau}$$

$$P_m(ZD) \approx (\alpha e^{t_r/\tau})^{-1}$$

- Small signal regeneration is linear operation and can be modelled with a negative resistance and negative time-constant $-\tau$.
- Time constant τ can be obtained from the slope of $\log_e(v_{od}(t))$.
- Metastability occurs when latch output v_{od} falls within $[V_{IL}, V_{IH}]$.
- Metastability Probability $P_m(ZD) = ((V_{IH}-V_{IL})/A)/FS \approx (\alpha e^{t/\tau})^{-1}$, not affected by noise. [*Figueiredo, JSSC 2013*]

ADC Metastability and Migitation



ADC Metastability Probability

$P_m(ADC) = (2^n x_m) / FS \approx 2^n P_m(ZD)$

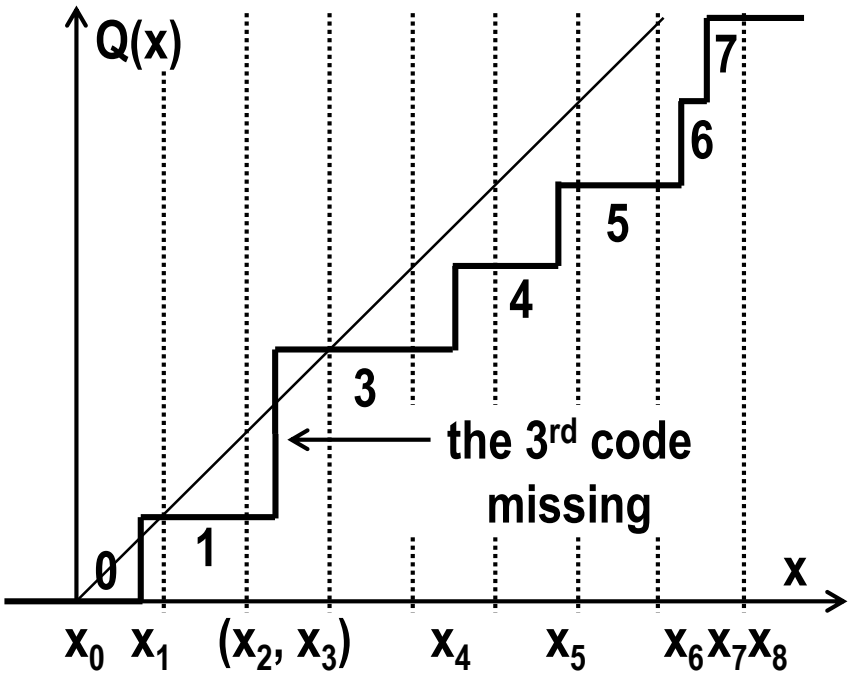
Comparator Metastability Probability

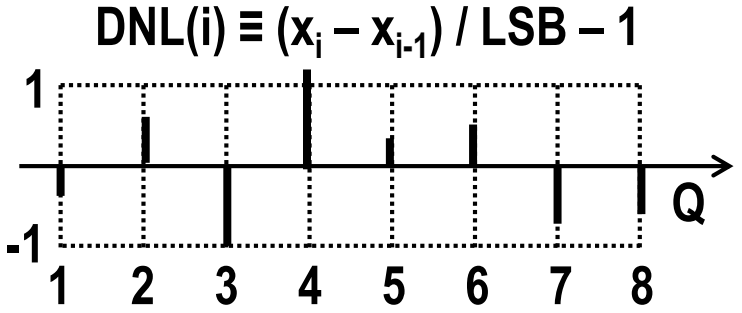
$P_m(ZD) = e^{-t_r/\tau}/A$

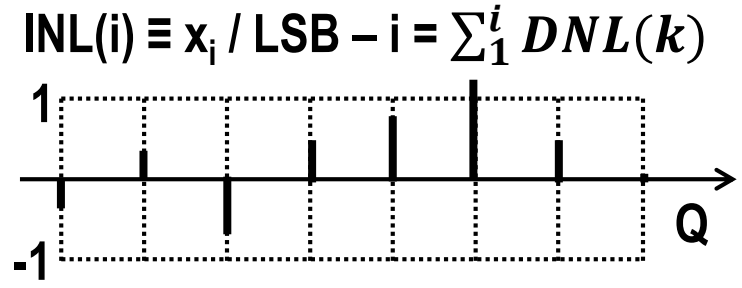
- Metastability is a fundamental ADC issue that can not be eradicated.
- Noise may break a metastable event but does not alter the probability.
- Metastaiblity causes large sparkle errors even at very high S/N levels.
- Metastability and its effect on ADC output error can be mitigated.
  - Increasing (effectively) the regeneration time t_r
    - Cascading latches or DFFs before the encoding logic
    - Time interleaving the ADCs or the comparators
    - Asynchronous clocking [*Chen, ISSC 2006*] for need based regeneration time.
  - Reducing the metastability impact on encoding output [*Portmann, JSSC 1996*]
  - Reducing regeneration time constant in fast technologies

Metrics and Measurements

Integral & Differential Nonlinearity (INL & DNL)

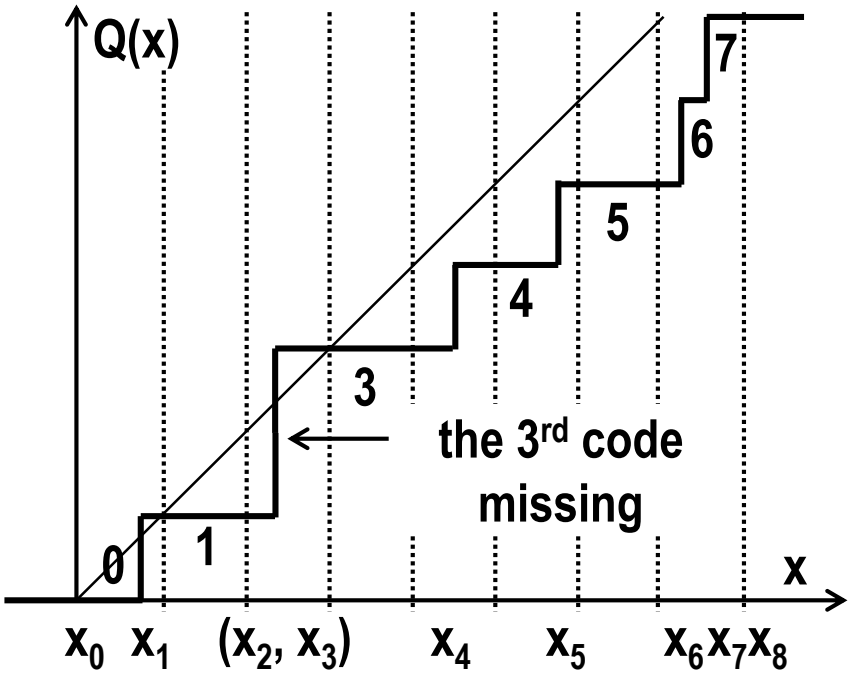


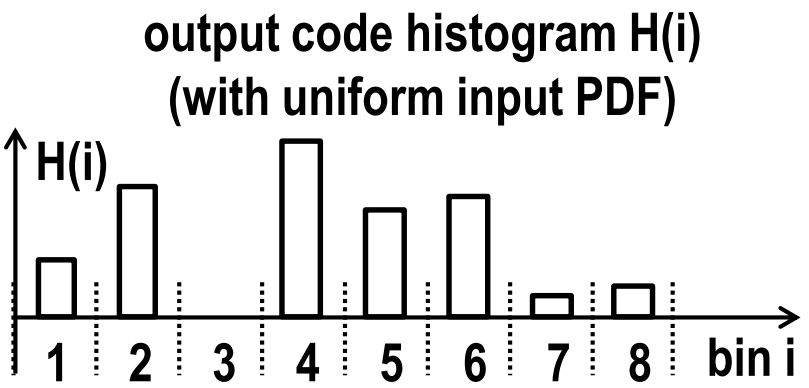




- Gain and offset errors are extracted by linear fitting and excluded from INL and DNL.
- INL and DNL both capture ADC nonlinearity as quantization threshold (x_i) errors in LSB.
- INL highlights low-order distortion from analog front-end such as input/ref. buffer, T/H, etc.
- DNL stresses high-order quantization errors from comparator offsets, RA inaccuracy, etc.
- INL and DNL do not capture signal dependent threshold errors (e.g. latch (ZD) hysteresis.)
- INL and DNL can be measured by static DC sweep or by dynamic code density test.

Output Code Density Test for DNL and INL





$$DNL(i) = (H(i) / \sum H(i)) / P(i) - 1$$

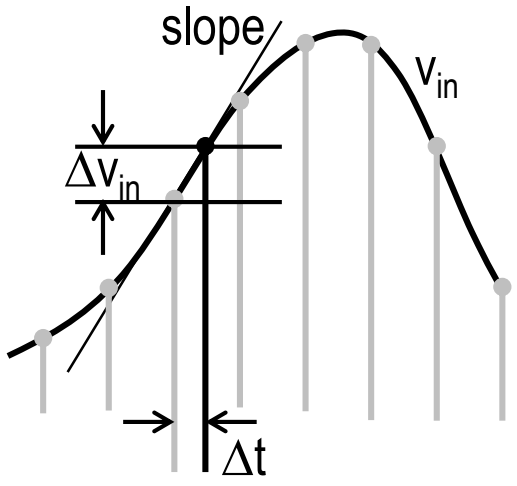
For uniform input PDF, $P(i) = 2^{-n}$.

For sinewave input, see the ref:

[*Doernberg, JSSC 1984*]

- Freq. of code occurrence is proportional to bin size R_i given uniform input PDF.
- FS sinewave asynchronous to f_s with well-defined P(i) is used as the test signal.
- H(i) averages out noise, resulting in accurate DNL/INL, gain, offset measurement.
- Frequency response and dependence on conversion rate are also captured.

Sampling Jitter Effect on ADC Performance



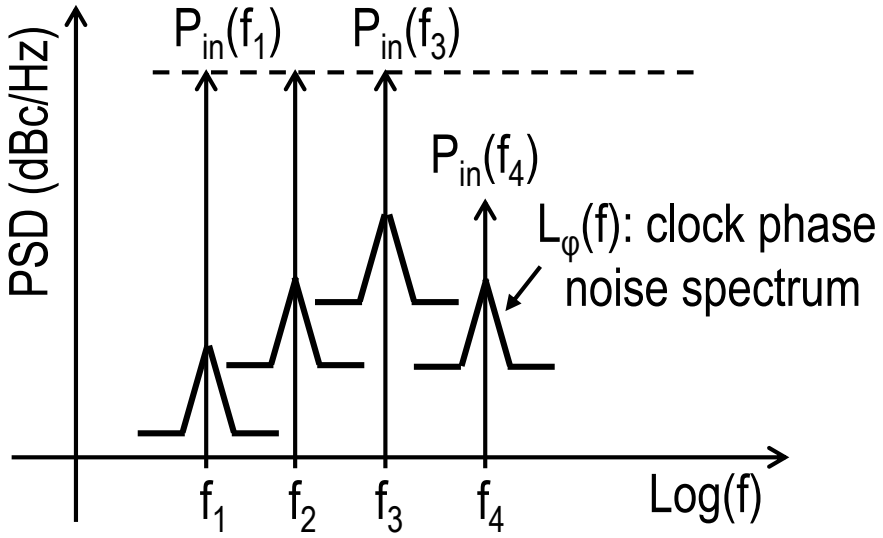
$$\Delta v_{in} \approx dV_{in}(t)/dt\ \Delta t \sim 2\pi f_{in} A\ \Delta t < LSB$$

$$\text{Jitter (rms) } \sigma(\Delta t) < T_{in}/2^n$$

$$FT(\Delta v_{in}) \approx j\omega V_{in}(\omega) \bigstar \Delta\varphi(\omega)/\omega_s$$

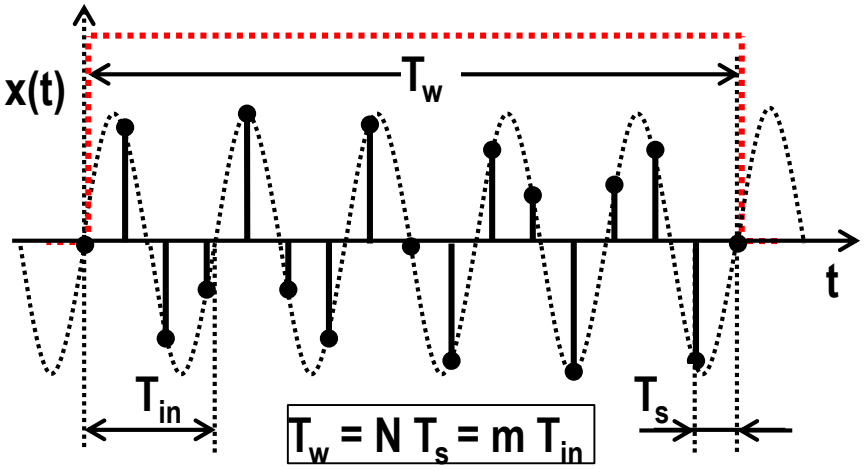
$\Delta\varphi(\omega)$: clock phase noise; ω_s: clock freq.

$$P_{jitter}(f) \approx (f_k^2/f_s^2) L_\varphi(f - f_k) P_{in}(f_k)$$

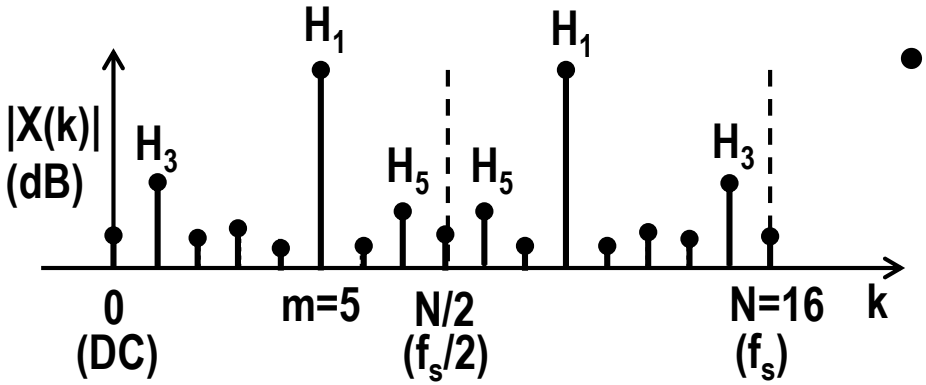


- Noise due to clock jitter scales with sampled signal frequency and amplitude.
- Jitter spec can be orders of magnitude relaxed for wideband and large PAPR.
- Jitter slower than system tracking BW or observation time can be excluded.

Frequency Domain Characterization Using FFT



FFT: DFT with $N = 2^n$



- Single-tone test: $|H_1|^2 \sim P_{FS}$

  SNDR ≡ $|H_1|^2 / (\sum_{k\neq m}^{N/2} |X(k)|^2)$

  SFDR ≡ $|H_1|^2$ / max$|X(k)|^2_{k\neq m}$)

  THD ≡ $\sum_2^I |H_i|^2 / |H_1|^2$
  (e.g. $I = 15$)

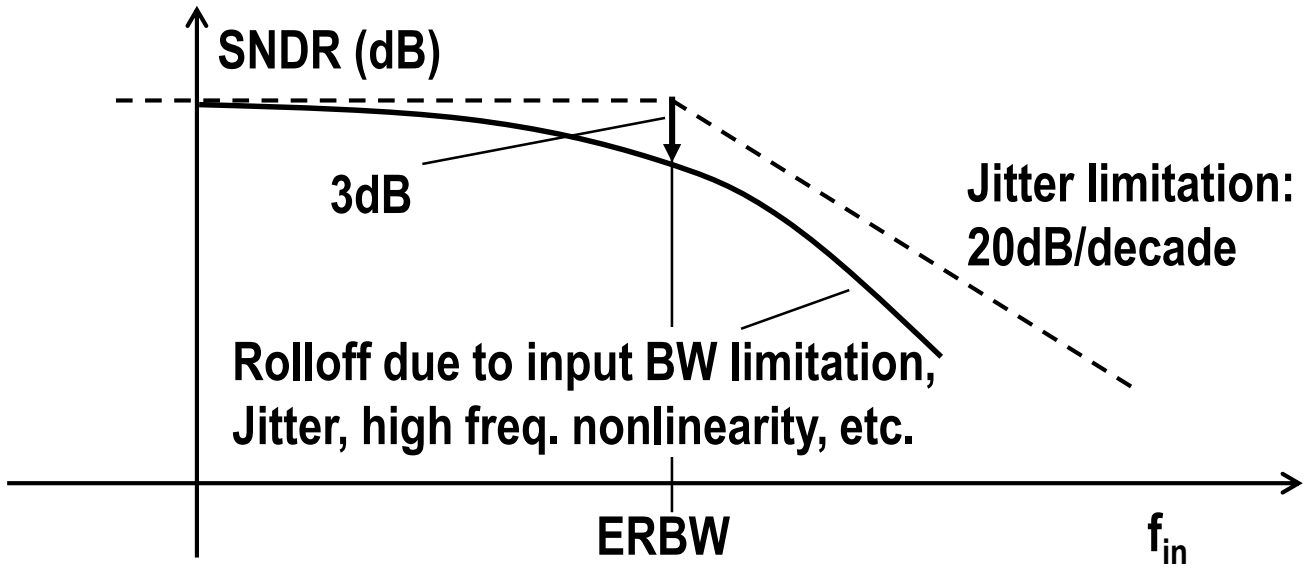
SNR ≡ $|H_1|^2 / (\sum_1^{N/2} |X(k)|^2 - \sum_2^I |H_i|^2)$

- Multi-tone test:

  $F_{inj} = m_j\, f_{bin}$; j = 1, 2, …, M

  $|H_{ji}|^2 = P_{FS} / M^2$

Effective Resolution Bandwidth (ERBW)



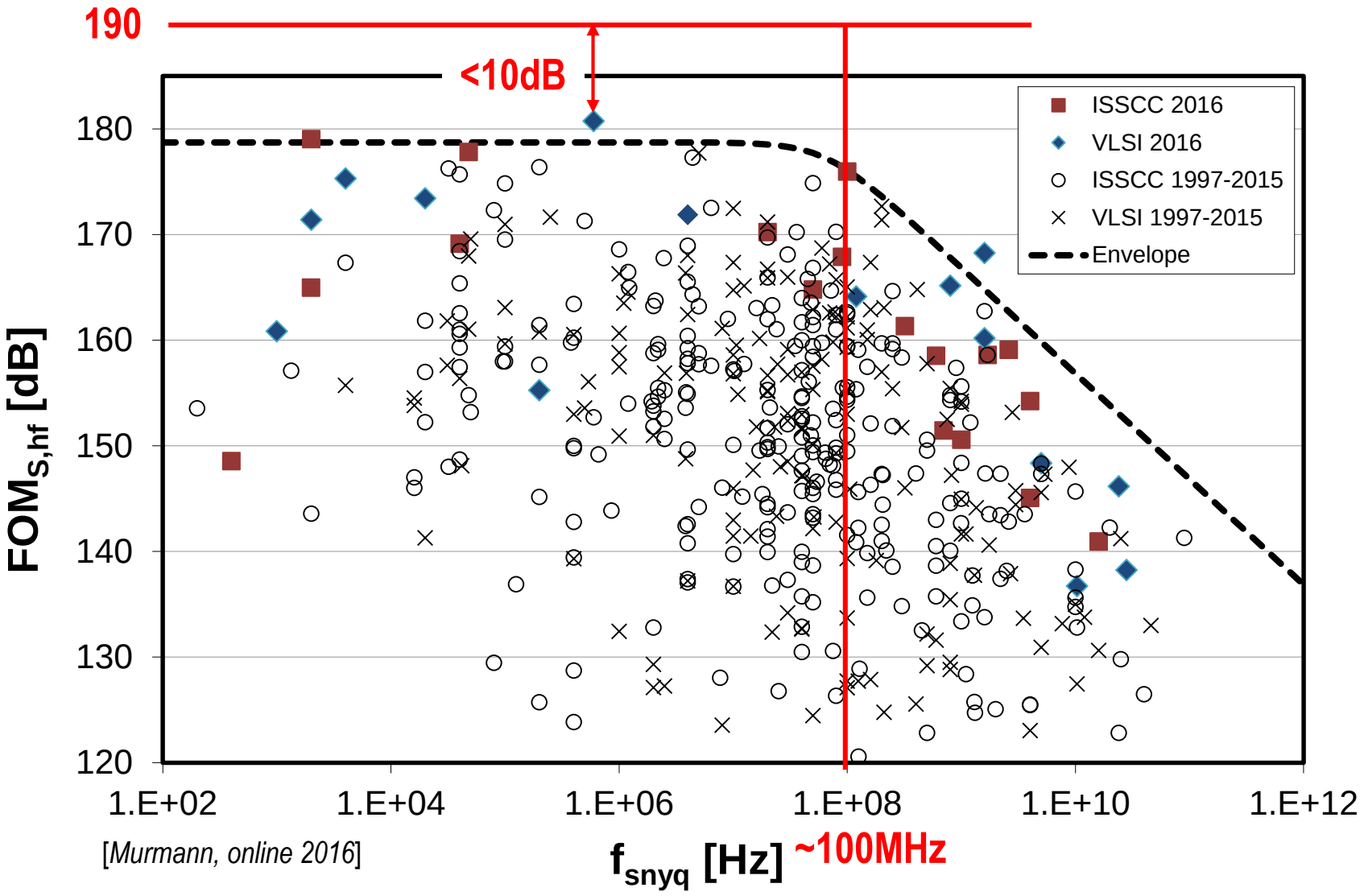
ERBW ≡ f_{in} @ ENOB = ENOB(dc) – 0.5

- An n-bit ADC is supposed to have ENOB(dc) > NOB – 0.5.
- An n-bit Nyquist ADC is supposed to have ERBW > f_s / 2.
- Metrics for FS single-tone test near Nyquist tend to over-specify ADCs.
  - Input signal freq. usually occupies the lower portion of the Nyquist band
  - Input signal amplitude rms is usually much smaller than the full scale

ADC Figures of Merit (FoM)

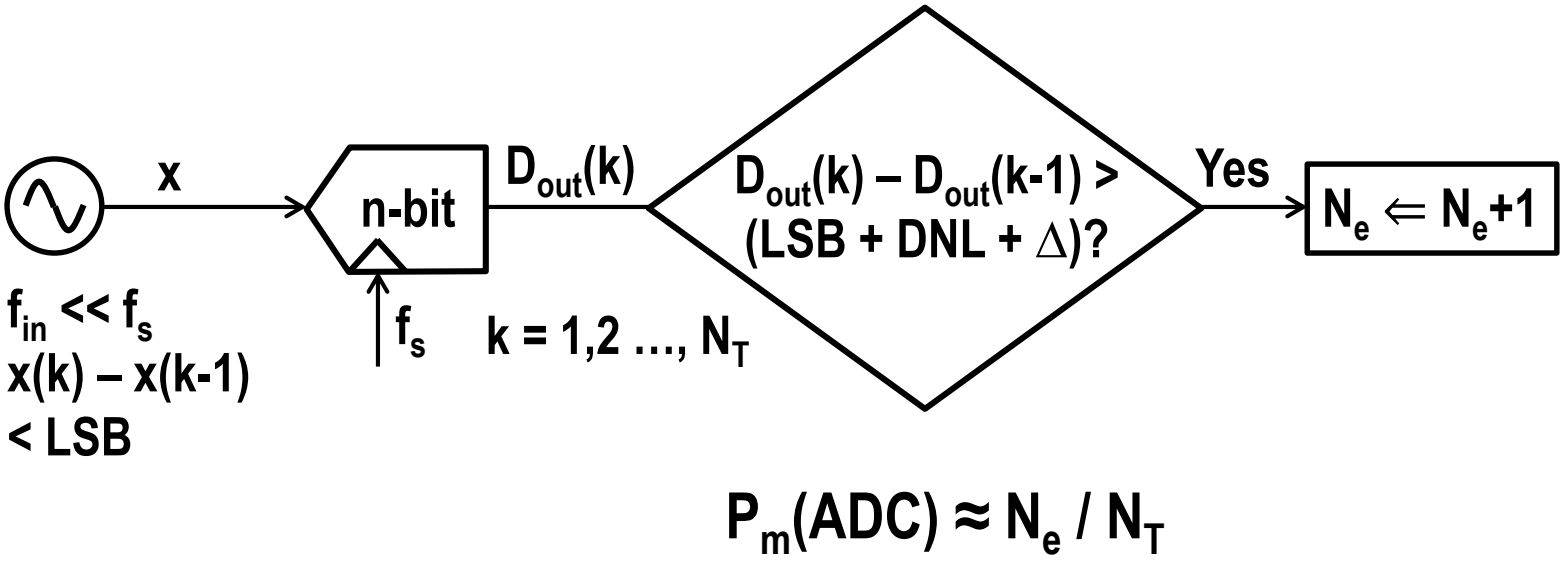
- Walden (ISSCC) $FoM_w = P / (2^{ENOB} f_s)$
  - For low resolution (n<10b) full-flash ADCs where ENOB dominates the total number of comparators and total power.
- Schreier $FoM_s = (2^{ENOB*2} BW) / P \approx SNDR + 10\log(BW/P)$ (dB)
  - For high resolution (n≥10b) sw-cap based ADCs, ENOB determines KT/C, and the capacitor C dominates the total power.
  - For $P=V_{FS}^2 C f_s = V_{FS}^2 f_s kT12/LSB^2 = 2^{ENOB*2} 12kTf_s$, $FoM=(24kT)^{-1} \approx 190$(dB).
- Many FoMs emphasize different aspects for different applications.
- Many factors affect the FoM
  - ADC definition (e.g. buffers/PGA/AAF), f_t, trimming, jitter, digital, etc.
- Many publications and surveys are there on FoMs
  - For example: http://converterpassion.wordpress.com/
  - B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

Survey Results: Schreier FoM vs. Fs



[*Murmann, online 2016*]

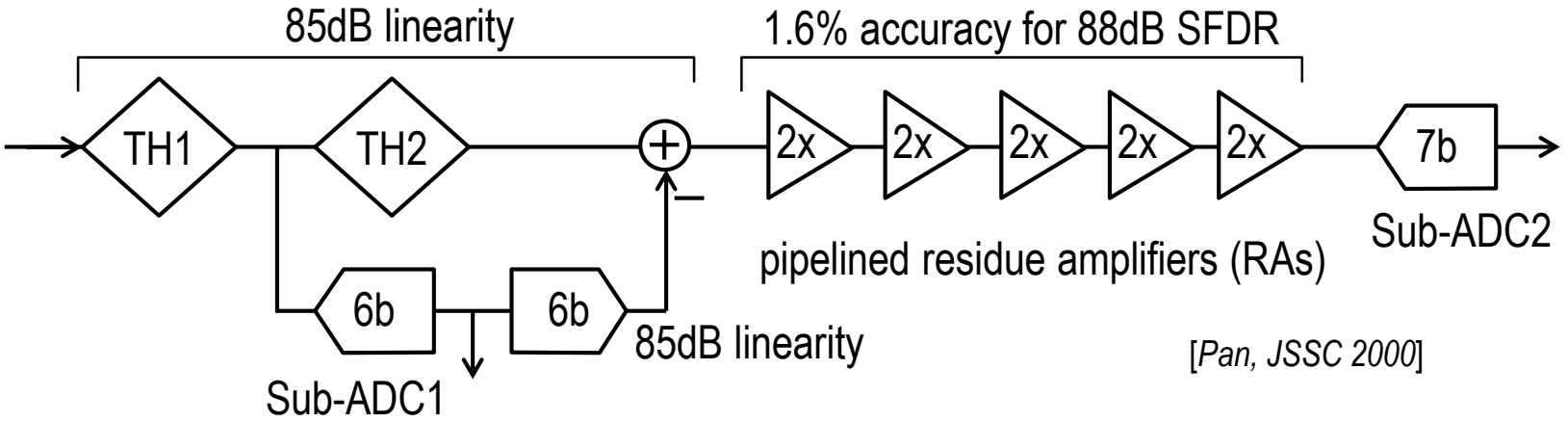
ADC Meta-Stability Test



- Meta-stability is hard to catch in transient simulations but can be easily measured on- or off-chip.
- Meta-stability probability P_m can be accurately estimated in simulation from regeneration transient slope.

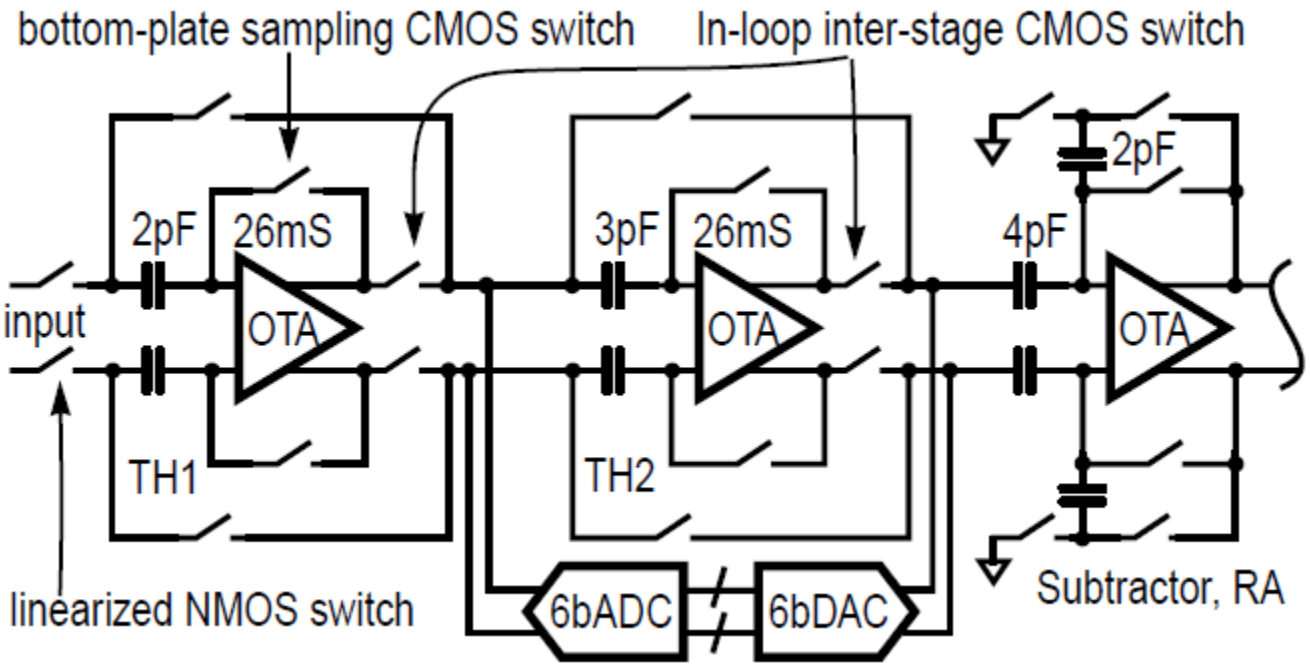
Evolutions and Trends

A 3.3V 50MS/s 12b ADC with 85dB SFDR in 0.6µm CMOS



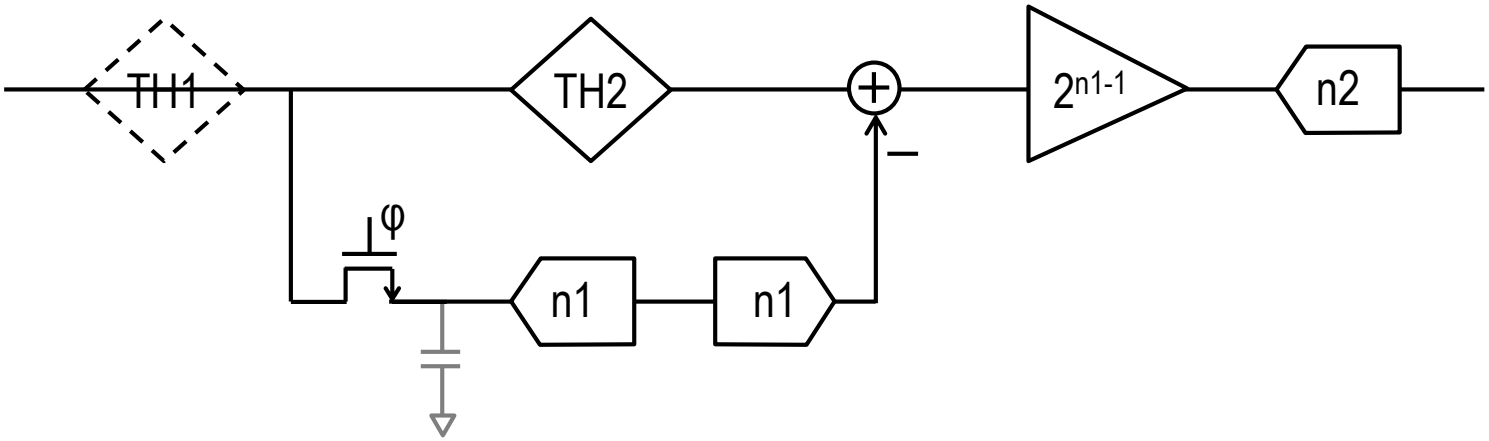
- This ADC is intended for low power base-station IF sampling.
- Pipelined 2-step conversion achieves 50MS/s and 85dB SFDR in 0.6µm CMOS with V_{dd} lowered to 3.3V from standard 5V.
- 6b first step removes SFDR bottleneck imposed by the residue gain inaccuracy; T/H and DAC linearity determine the SFDR.
- Pipelined RAs avoid tradeoff between amplifier gain and BW.
- Signal Folding reduces the 6b sub-ADC and the DAC complexity.
- Optimal spatial filtering reduces input cap of each sub-ADC by 7X.

Input T/Hs and MDAC



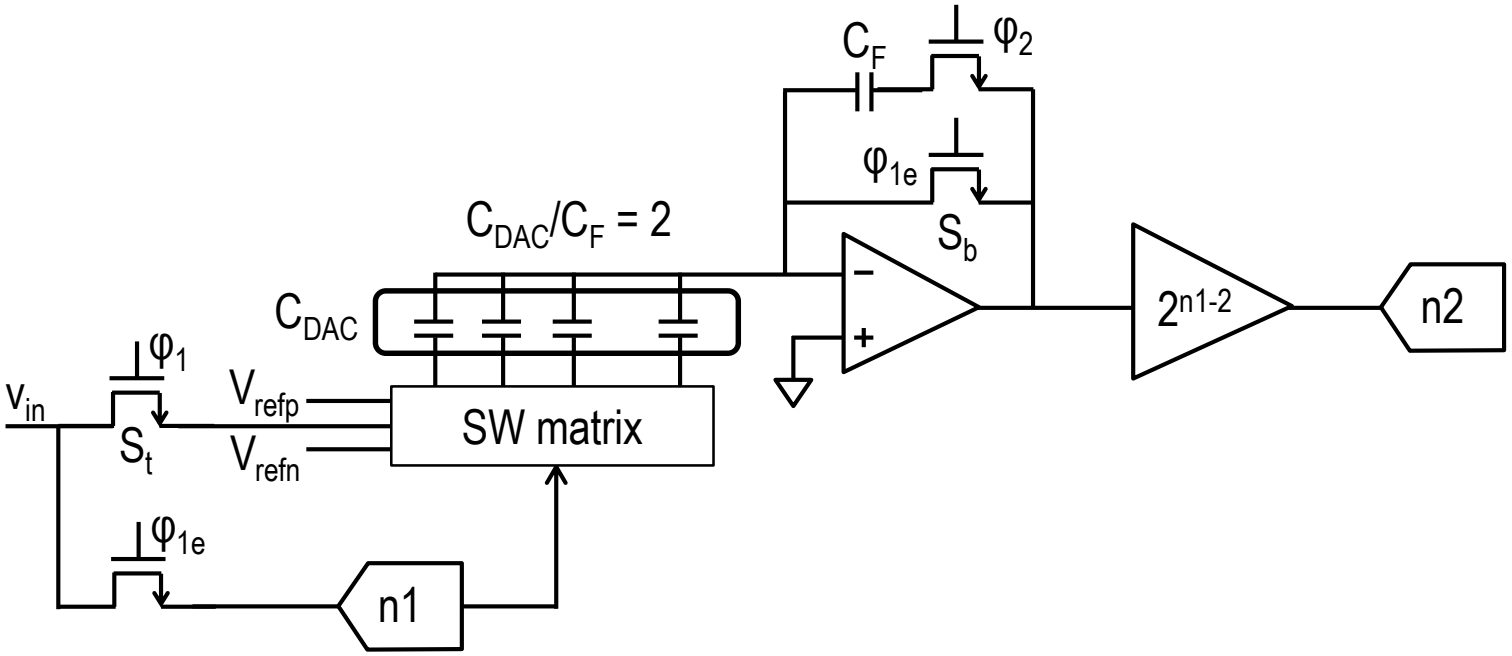
- Input switches are linearized with closed-loop bootstrapping for >85dB SFDR.
- Wrap-around T/Hs with bottom plate sampling for max. BW and min. errors.
- TH2 removes the ADC speed bottleneck associated with sub-ADC latency.
- In-loop inter-stage switch minimizes effect of finite switch BW on ADC speed.

Evolution with Technology: Remove 1st T/H Amplifier



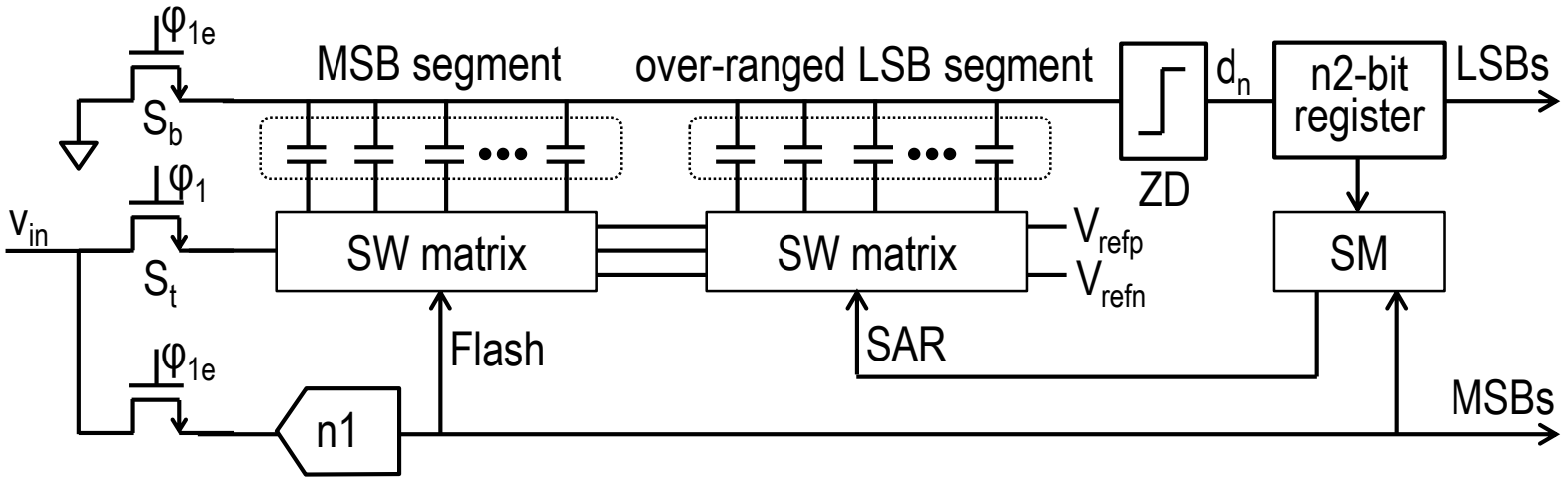
- A separate T/H driving the n1-bit sub-ADC needs only n1-bit accuracy and can use simple open-loop switch.
- Timing between the two signal paths needs to be within n1-bit, more feasible in an advanced technology.

Evolution with Technology: Remove 2nd T/H Amplifier



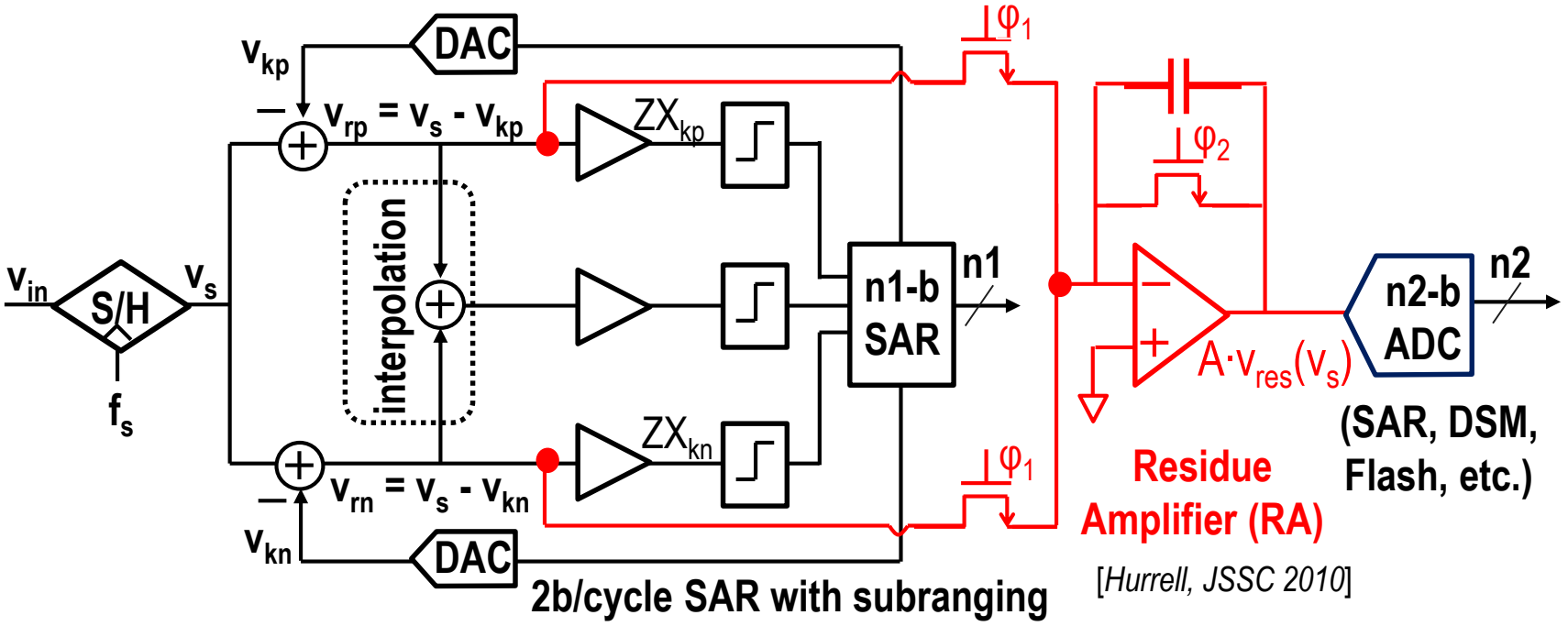
- Sub-ADC latency is reduced with fast comparator decision in advanced technology, obviating the need for the 2nd T/H.
- The reconstruction DAC caps are directly driven by the input, eliminating the T/Hs and the associated KT/C noises [*Lee, JSSC 2011*]..

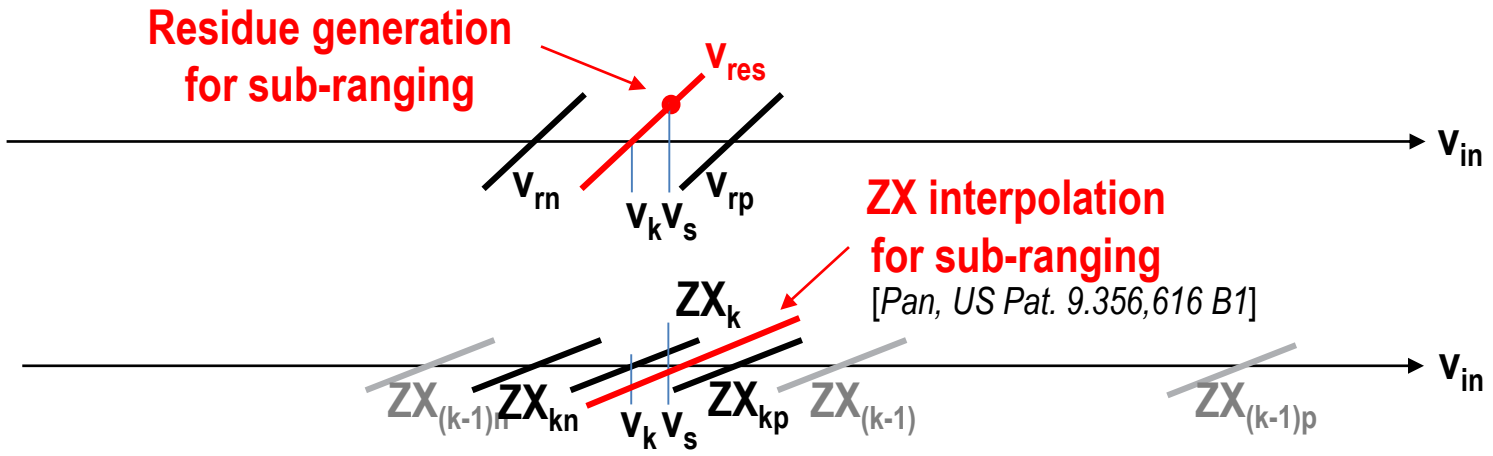
Evolution with Technology: Remove the RAs



- The 2nd sub-ADC is implemented in a SAR architecture that does not need residue amplification for using only one comparator for the entire conversion.
- The SAR in an advanced process can achieve the required conversion rate.
- The 1st sub-ADC output directly control the MSB segment of the SAR DAC.
- The SAR LSB segment is over-ranged using radix < 2 for the DAC array.
- The 2-step pipeline ADC evolves to a sub-ranged SAR ADC [*Lin, VLSI 2010*] …
- Technology has a drastic impact on ADC architecture evolutions and FoMs.

Pipelined Sub-ranging of Multi-bit/cycle SAR ADC





Closing Remarks

- Quantization is a search process ranging from the most efficient serial binary search to the fastest brute-force parallel search.
- Parallel search is reduced in complexity by signal folding but at the cost of delicate analog signal processing (e.g. MDAC).
- Serial binary search combined with comparator reuse results in the most efficient SAR ADCs at the expense of conversion rate.
- SAR ADC speed can be increased by time-interleaving as many quantizers as needed, with the mismatch error digitally calibrated.
- Digital calibration and error correction overheads diminish in advanced CMOS processes, leading to SAR ADC popularity.
- SAR ADC is enhanced with sub-ranging for resolution, pipelining for speed, optimal switching for power efficiency, etc.

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