A Simple Precharged CMOS Phase Frequency Detector

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***Abstract*— We propose a simple precharged CMOS phase frequency detector (PFD). The circuit uses 18 transistors and has a simple topology. Therefore, the detector, in a 0.8-μm CMOS process, works up to clock frequencies of 800 MHz according to SPICE simulations on extracted layout. Further, the detector has no dead-zone in the phase characteristic which is important in low jitter applications. The phase and frequency characteristics are presented and comparisons are made to other PFD's. The phase offset of the detector is sensitive to differences of the duty-cycle between the inputs. Mixed-mode simulations are presented of the lock-in procedure for a phase-locked loop (PLL) where the detector is used. Measurements on the detector are presented for a test-chip with a delay-locked loop (DLL) where the phase detection ability of the detector has been verified.**

***Index Terms*— CMOS integrated circuits, delay lock loops, phase detectors, phase lock loops.**

I. Introduction

A part of a phase-locked loop (PLL) is the phase detector (PD) [1]. The PD detects the phase difference between the reference frequency and the controlled slave frequency. Some PD's also detect frequency errors, they are then called phase frequency detectors (PFD's). A PFD is usually built with a state machine with memory elements such as flip-flops [2], [3], Figs. 1 and 2, respectively. We propose a new simple PFD, ncPFD, which uses two nc-stages [4] and six inverters, Fig. 3(a).

A drawback with some phase detectors is a dead zone in the phase characteristic at the equilibrium point. The dead zone generates phase jitter since the control system does not change the control voltage when the phase error is within the dead zone.

In Section II the ncPFD circuit is described. The phase and frequency characteristics are discussed in Sections III and IV, respectively, and comparisons are made to other PFD's. Behavioral mixed-mode simulations are made to check the lock-in properties of the ncPFD detector and these simulations are shown in Section V. Experiments on the phase detection abilities of the ncPFD are presented in Section VI.

II. Circuit

The transistor schematic of the ncPFD is shown in Fig. 3(a). The detector has a 0-rad phase offset. The main part of the circuit is the nc stage [4]. Delays (two inverters) are inserted at the reference and slave inputs in order to remove the dead zone in the phase characteristics around π rad phase error. In Fig. 4, waveforms for the circuit in Fig. 3(a) are shown when the slave input lags the reference input.

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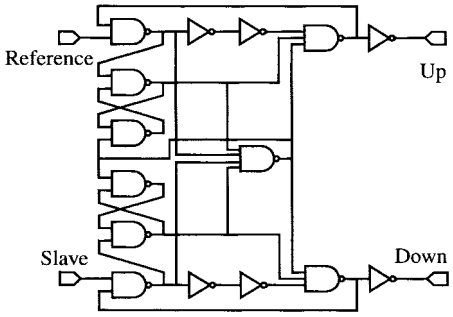

Fig. 1. Conventional phase frequency detector (conPFD) from [2].

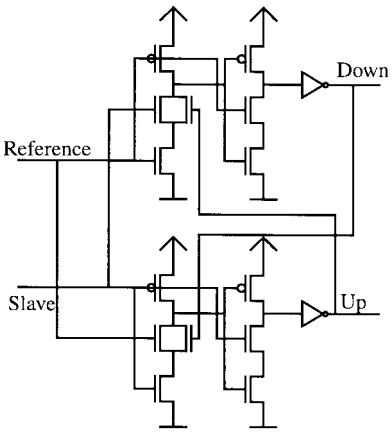

Fig. 2. Precharge type phase frequency detector (ptPFD) from [3].

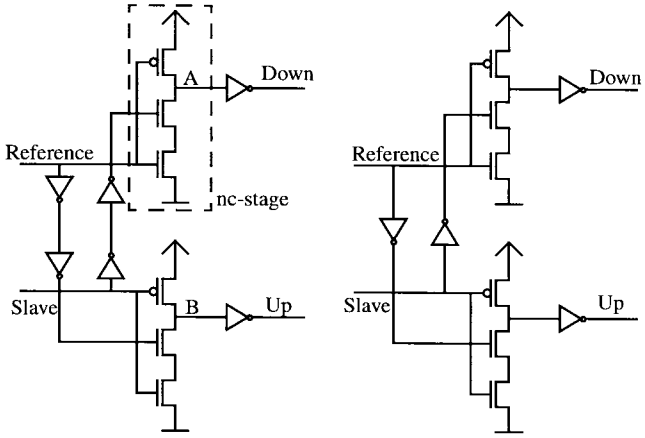

Fig. 3. (a) The ncPFD in zero degree phase offset version. (b) Modified version with π rad phase offset.

The detector can easily be modified to one with π-rad phase offset, as shown in Fig. 3(b), where one, or in general an odd number, of inverter(s) are used for the delays.

If the phase detector is used only as a phase detector, i.e., not as a frequency detector, the circuit in Fig. 3(a) can be used as

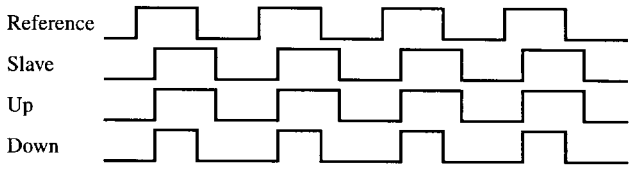

Fig. 4. Waveforms for the case when slave lags after the reference signal. The pulse width of the up signal is larger than for the down signal.

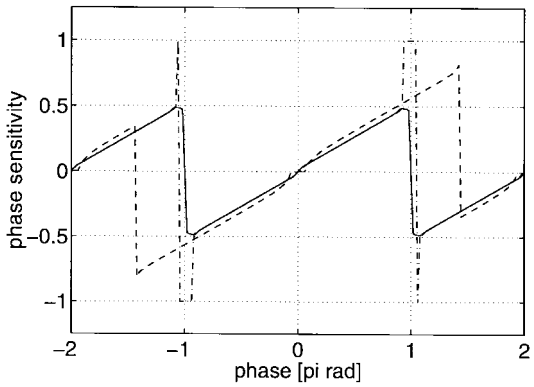

Fig. 5. Phase characteristics of the ncPFD (solid line), conPFD (dashed line), and the ptPFD (dash-dot line) from SPICE level-2 simulations of extracted layout, $V_{\rm DD} = 3.0$ V and $f = 50$ MHz.

a π-rad phase detector by switching the up and down signals. The equilibrium point will then be on the negative slope of the phase characteristics at π rad instead of at the positive slope at zero, Fig. 5. Similarly, the π-rad phase detector, Fig. 3(b), can be modified to a 0-rad phase detector.

III. Phase Characteristic

The phase characteristic of the proposed ncPFD is shown in Fig. 5 together with the characteristics of the conventional PFD (conPFD) of Fig. 1 [2] and the precharge type PFD (ptPFD) shown in Fig. 2 [3]. Unlike the conPFD and ptPFD, there is no dead-zone in the characteristics of the ncPFD. A magnification of the characteristics at zero phase is shown in Fig. 6. The dead zone of the conPFD can be reduced by inserting delay at the output of the four-input-NAND-gate. But if delays are inserted in the feedback signals from the up and down outputs of the ptPFD, the dead zone unfortunately increases.

In an ncPFD, when the PLL is locked, both up and down signals are active. Therefore the phase offset of the PLL depends on the matching between the up and down currents of the charge pump.

All data in this section are based on simulations of extracted layout with SPICE (level-2) when $V_{\rm DD} = 3.0$ V and $f = 50$ MHz unless otherwise stated. The layout was made in a 0.8-μm standard CMOS process and the N and P-transistors are 2.0 and 4.0 μm wide, respectively. The outputs were connected to 4.0 fF capacitors, and the inputs were driven with inverters with a tapering factor of one.

A. Duty-Cycle and Transition-Time Dependence

The output of the ncPFD depends on the pulse-width of the input signals. Hence, the duty cycle will affect the phase

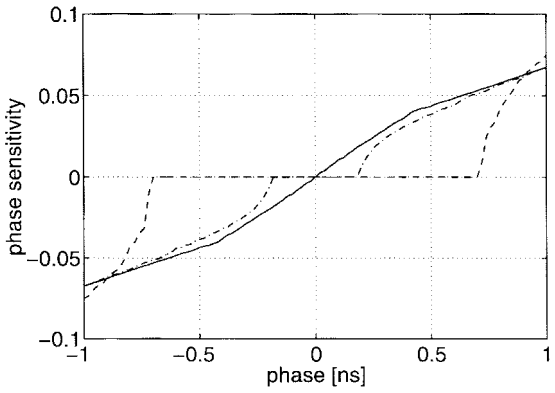

Fig. 6. Magnified phase characteristics at zero phase error of the ncPFD (solid line), conPFD (dashed line), and the ptPFD (dash-dot line) from SPICE level-2 simulations of extracted layout, $V_{\rm DD} = 3.0$ V and $f = 50$ MHz.

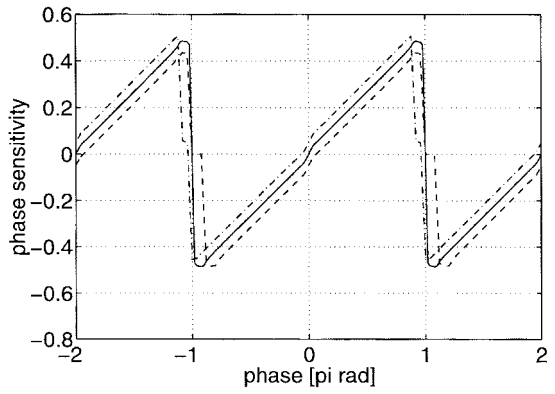

Fig. 7. Phase characteristics for three cases with different duty cycles. The reference input duty cycle is 50% for all cases and the slave input has the duty-cycles 45%, 50%, and 55% for the dashed, solid, and dashed–dotted lines, respectively.

characteristics. The phase characteristics are checked for three different duty cycles, 45, 50, and 55%.

When both the reference and slave have the same duty cycle, the phase offset is not affected. There is a dead zone at π-rad when the duty cycle is less than 50%. A duty cycle of 45% gives a dead zone width of 0.50 rad, 1.6 ns, at π rad. This dead zone may result in a metastable state of the control loop.

When the duty cycle is different for the two inputs, the phase offset will be nonzero, Fig. 7. A duty cycle difference of 5% at 50 MHz, i.e., 1 ns, gives a phase offset of $0.063 * \pi$ rad, i.e., 630 ps.

The phase characteristic of the ncPFD is not affected by variations of the rise and fall times when they are in the range of 300 ps up to 600 ps.

B. Maximum Operation Frequency

A maximum operation frequency definition can be found in [3]. The definition is that the maximum operation frequency is one over the shortest period with correct up and down signals when the inputs have the same frequency and 90° phase difference. This definition is easily applicable on flip-flop-based PFD's where this frequency is easily identified. Unfortunately, the degradation of the performance of the

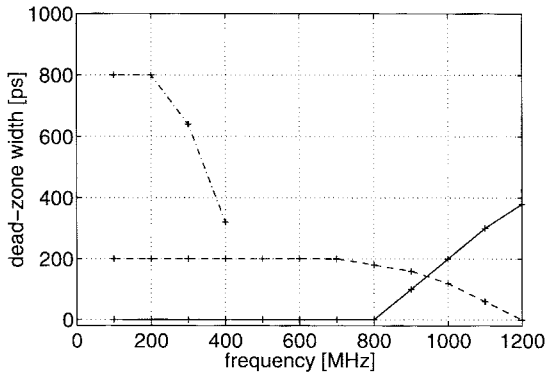

Fig. 8. The width of the dead zones of the ncPFD (solid), ptPFD (dashed), and conventional PFD (dash-dot) as function of frequency. The frequency resolution is 100 MHz and the supply voltage is 5.0 V. The plot is based on SPICE simulations of extracted layout.

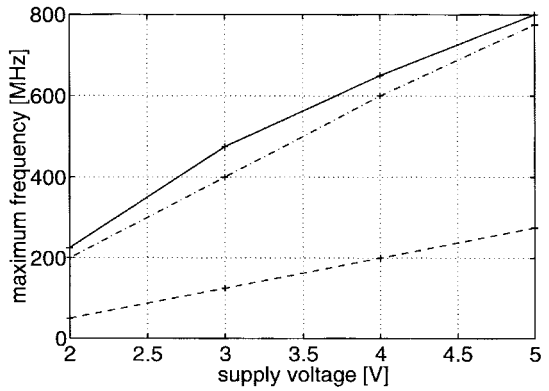

Fig. 9. Maximum frequency as function of supply voltage for the ncPFD (solid line), the ptPFD (dash-dot line), and the conPFD (dashed line). The frequency resolution is 25 MHz. The plot is based on simulations of extracted layout. The layouts are made in a standard 0.8-μm CMOS process.

ncPFD is gradual for increasing frequency and this makes it hard to find a specific frequency where the circuit starts to malfunction.

Therefore, we define the maximum operation frequency to be the frequency where the size of the dead zone starts to deviate significantly from the low-frequency value. This definition gives similar results for the flip-flop-based phase detectors as for the definition in [3], and it is applicable on the ncPFD. An example of how the dead-zone-width varies with the frequency is shown in Fig. 8.

The maximum speeds for different supply voltages are plotted in Fig. 9 for the three PFD's of Figs. 1, 2, and 3(a). As seen, the maximum speed of the ncPFD and the ptPFD are similar and the conPFD is approximately three times slower.

IV. Frequency Characteristics

A frequency dependent phase detector always has some kind of memory. For the ncPFD, the memory consists of the two dynamic nodes at the output of the nc-stages. In Fig. 10, the frequency of the slave input is approximately three times higher than the reference input frequency, as a result, the down signal has a higher duty cycle than the up signal. Thus the slave frequency should decrease.

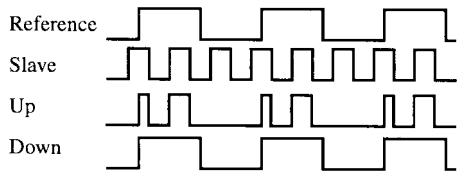

Fig. 10. Waveforms for the case when the slave has a higher frequency than the reference signal. The down signal has higher duty cycle than the up signal.

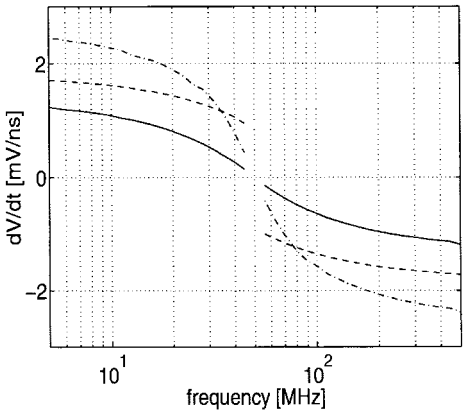

Fig. 11. Frequency sensitivity for the ncPFD (solid), ptPFD (dash-dot), and conPFD (dashed). The plot is based on behavioral simulations with 20 different initial phases for each frequency and the mean-value for each frequency is plotted. The reference frequency is 50 MHz.

The average frequency sensitivities of the ncPFD, ptPFD, and conPFD are shown in Fig. 11. The frequency sensitivity is represented by the rate of change in the control voltage of the loop filter of a PLL when the slave input is driven by a pulse generator with a fixed frequency instead of the voltage-controlled oscillator (VCO) output. Each frequency is simulated 20 times with different initial phases, i.e., skew between the inputs.

The ptPFD has the largest sensitivity, followed by the conPFD, and the ncPFD has the lowest. The sensitivity goes to zero as the slave frequency approaches the reference frequency for both the ncPFD and ptPFD. But for the conPFD, the sensitivity is relatively high even for frequencies close to the reference.

In Fig. 12 the sensitivity for the ncPFD is shown with the mean, minimum, and maximum values from the 20 simulations for each frequency. Note that the behavior of the minimum and maximum values are almost random.

For the ncPFD, the minimum absolute value of the sensitivity is close to zero for certain frequencies, Fig. 12. Actually, the sensitivity is zero for some frequency ratios and phase combinations. This is the case also for the ptPFD but not for the conPFD. The condition for this seems to be that when the frequency ratio of the reference and slave inputs is a rational number and the ratio is in the interval 1/2 to 2, including the limits, the sensitivity is zero for certain initial phases. We have no general proof of the previous statement but, for example, the sensitivity of the ncPFD for $f_{\text{slave}} = 4/5 * f_{\text{reference}}$ as function of initial phase is shown in Fig. 13. The sensitivity is zero for the phases 0.0, 2.5, and 5.0 ns. This lack of sensitivity may lead to false locking for a PLL in operation. However,

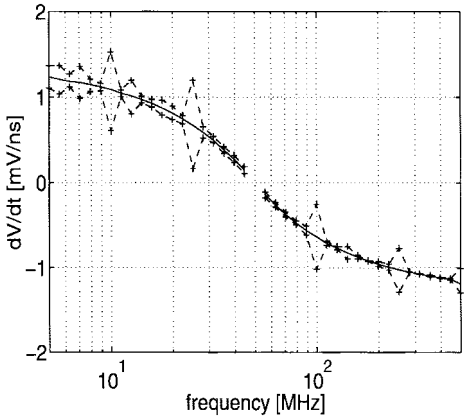

Fig. 12. Frequency sensitivity for the ncPFD for a number of frequencies. The plot is based on behavioral simulations with 20 different initial phases for each frequency. The solid line is the mean value and the "+" symbols are the minimum and maximum values. The reference frequency is 50 MHz.

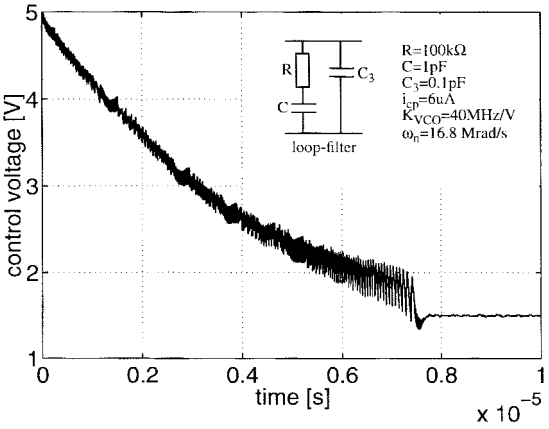

Fig. 14. Lock-in process of a third-order PLL with the ncPFD as phase frequency detector. The loop filter and PLL data are shown in the upper right corner.

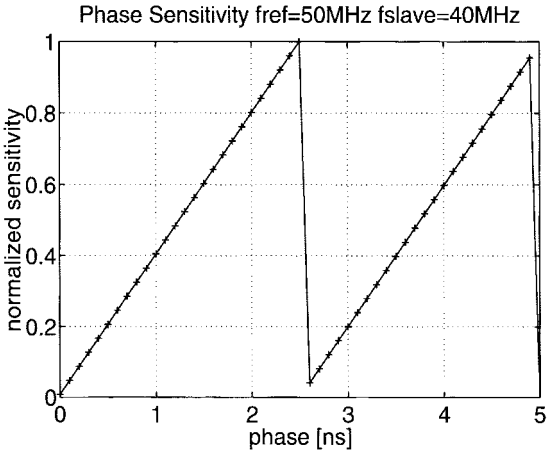

Fig. 13. Frequency sensitivity for the ncPFD when the slave frequency is 4/5 of the reference frequency. For the initial phases of 0.0, 2.5, and 5.0 ns the sensitivity is zero.

this false locking will not be stable, since a small phase change results in a nonzero sensitivity and drives the loop back to lock.

One way to add small phase changes to the simulation is to include phase noise which is always present in an oscillator. When we add phase noise of approximately 300 ps peak-to-peak to the simulations, the normalized minimum sensitivity which was zero will increase to approximately 0.01. The improvement is not significant but the sensitivity will be nonzero and positive for all phases. Hence, false locking is avoided. To further enhance the phase noise during the lock in process, one could use dithering techniques, i.e., add the signal from a noise/signal source to the control voltage of the VCO.

V. Behavioral Mixed-Mode Simulations

In order to understand the sensitivity to frequency errors and lock-in properties of the proposed detector, a complete third-order charge pump PLL system was simulated using a multilevel mixed-mode simulator, Lsim [5]. The PFD was represented by a schematic simulated in switch mode. The VCO, phase-noise generator, and charge pump are represented by behavioral models written in the hardware description language M [6]. The loop filter used ideal R and C models in circuit mode with analog voltages. The loop filter and PLL data are shown as an inset in Fig. 14. A lock-in simulation is shown in Fig. 14. The simulation is done with the presence of 300 ps peak-to-peak phase noise.

Because of the sawtooth-shaped frequency sensitivity of the ncPFD (for a fixed frequency offset and varied initial phase), Fig. 13, and the presence of noise, the lock-in time is not deterministic but random. The lock-in times for 60 simulations have been analyzed. Most simulations show a lock-in time of 7 μs and the largest time is 16 μs. There is no upper limit on the lock-in time. One simulation took approximately 3 cpu-min on a SPARC 10 workstation.

VI. Experiments

The phase detection properties of the ncPFD have been verified experimentally with a test chip. The test chip is a line receiver for serial data that utilizes several parallel samplers to receive bit rates of 2.0 Gb/s [7]. The phase detector was used in a delay-locked loop (DLL) which generates control signals for the sampling switches used in the line receiver. The ncPFD, Fig. 3(a), was used as a π-rad phase detector and the delay line was half a wavelength long.

The skew between the reference and slave signals is not possible to measure directly. This quantity has been measured indirectly through measurement error compensation circuits to be about 125 ps at $f = 250$ MHz. Unfortunately, there is no control of how large the measurement error is.

The circuit blocks used to measure the offset are shown in Fig. 15. The two clocks that we want to compare come from the beginning and the end of the delay line. They are fed into two matched inverter chains where the propagation delay for rising and falling edges are matched against process variations [8]. The delay from the multiplexer inputs to the oscilloscope screen for the two signal paths are not matched. Two measurements are done to compensate this. One where the delay line input signal goes uninverted through *Output buffer 1* and one where the same signal goes inverted through the *Output buffer 2*. The measured skew including the measurement error

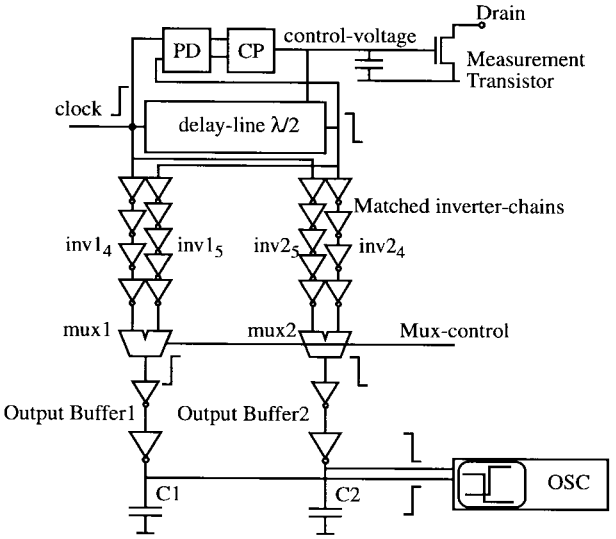

Fig. 15. DLL, phase offset measurement circuitry, and NMOS transistor to access the control voltage.

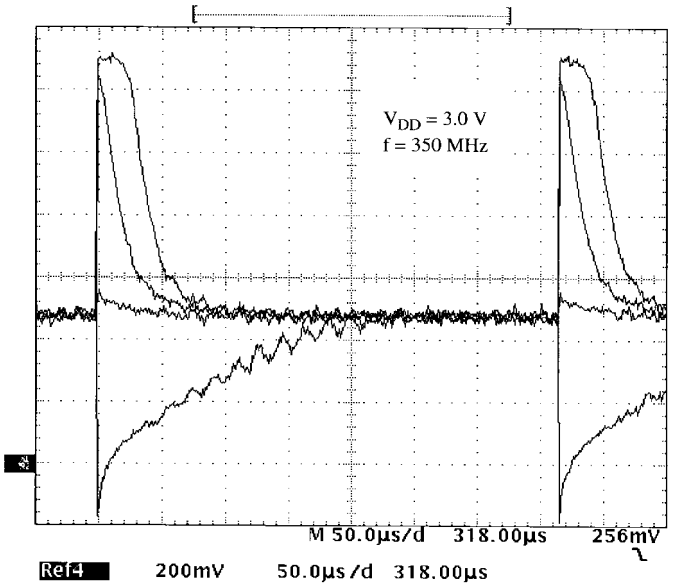

Fig. 16. Oscilloscope screen dump of the drain voltage of an NMOS transistor with external pull-up resistor where the gate is connected to the control voltage. Four different lock-in procedures are shown. The initial control voltages are 0.0, 1.0, 2.0, and 3.0 V for the curves from top to bottom, respectively.

for the measurements will be as follows:

$$\text{skew}_1 = (\Delta + \text{inv2}_{4\text{fall}} + \text{mux2}_{\text{fall}} + \text{Buf2}_{\text{fall}}) - (\text{inv1}_{4\text{rise}} + \text{mux1}_{\text{rise}} + \text{Buf1}_{\text{rise}}) \quad (1)$$

$$\text{skew}_2 = (\Delta + \text{inv1}_{5\text{fall}} + \text{mux1}_{\text{rise}} + \text{Buf1}_{\text{rise}}) - (\text{inv2}_{5\text{rise}} + \text{mux2}_{\text{fall}} + \text{Buf2}_{\text{fall}}) \quad (2)$$

where Δ is the real skew and $\text{inv2}_{4\text{fall}}$ and $\text{inv1}_{4\text{rise}}$ are the delays through the four inverters' long chains for falling and rising edges through the left and right chain, respectively. Similarly, $\text{inv1}_{5\text{fall}}$ and $\text{inv2}_{5\text{rise}}$ are for the five inverters' long chains. And $\text{mux1}_{\text{rise}}$ and $\text{mux2}_{\text{fall}}$ are the delays through the multiplexers. The $\text{Buf1}_{\text{rise}}$ and $\text{Buf2}_{\text{fall}}$ are the delays through the output-buffers and through the oscilloscope input-channels.

The sum of the skews (1) and (2) is

$$\text{skew}_1 + \text{skew}_2 = 2\Delta + \text{inv2}_{4\text{fall}} - \text{inv1}_{4\text{rise}} + \text{inv1}_{5\text{fall}} - \text{inv2}_{5\text{rise}}. \quad (3)$$

Note that the expression is independent of the *mux* and *Buf* delays. Hence, theoretically, if the rise and fall delays of the inverter chains are matched properly, there will not be any measurement error.

In Fig. 16 an oscilloscope screen dump with four lock-in procedures is shown. The signal is the drain voltage of an NMOS transistor with an external pull-up resistor and with the gate connected to the control voltage as shown in Fig. 15. The lock-in time is less than 200 μs. Ideally, the control voltage should go monotonically to the equilibrium voltage. Therefore, the beating in the lock-in procedure when the initial control voltage is 3.0 V is unexpected. The reason for this is unknown.

VII. Conclusions

A new PFD without a dead zone has been proposed. The circuit topology is simple and has no feedback loops. Simulation results indicate that the circuit can operate up to 800 MHz in 0.8-μm CMOS with a 5-V supply. The detector's phase offset depends on the duty cycle of the inputs. Measurements have been performed on the detector when it was used in a DLL as a phase detector and the functionality was verified.

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