Automotive Radar Sensors in Silicon Technologies

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Preface

Since the invention of the integrated circuit, the semiconductor industry has revolutionized the world in ways no one had ever anticipated. With the advent of silicon technologies, consumer electronics became light-weight and affordable and paved the way for an Information–Communication–Entertainment age. While silicon almost completely replaced compound semiconductors from these markets, it has been unable to compete in areas with more stringent requirements due to technology limitations. One of these areas is automotive radar sensors, which will enable next-generation collision-warning systems in automobiles. A low-cost implementation is absolutely essential for widespread use of these systems, which leads us to the subject of this book—silicon-based solutions for automotive radars.

This book presents architectures and design techniques for millimeter-wave automotive radar transceivers. Several fully-integrated transceivers and receivers operating at 22–29 and 77–81 GHz are demonstrated in both CMOS and SiGe BiCMOS technologies. Excellent performance is achieved indicating the suitability of silicon technologies for automotive radar sensors.

The first CMOS 22–29-GHz pulse-radar receiver front-end for ultra-wideband radars is presented. The chip includes a low noise amplifier, I/Q mixers, quadrature voltage-controlled oscillators, pulse formers, and variable-gain amplifiers. Fabricated in 180 nm CMOS, the receiver achieves a conversion gain of 35–38.1 dB and a noise figure of 5.5–7.4 dB.

Integration of multi-mode multi-band transceivers on a single chip will enable next-generation low-cost automotive radar sensors. Two highly-integrated silicon ICs are designed in a 180 nm BiCMOS technology. These designs are also the first reported demonstrations of mm-wave circuits with high-speed digital circuits on the same chip.

The first mm-wave dual-band frequency synthesizer and transceiver, operating in the 24 and 77 GHz bands, are demonstrated. All circuits except the oscillators are shared between the two bands. A multi-functional injection-locked circuit is used after the oscillators to reconfigure the division ratio inside the phase-locked loop. The synthesizer is suitable for integration in automotive radar transceivers and heterodyne receivers for 94 GHz imaging applications. The transceiver chip includes

a dual-band low noise amplifier, a shared downconversion chain, dual-band pulse formers, power amplifiers, a dual-band frequency synthesizer, and a high-speed programmable baseband pulse generator. Radar functionality is demonstrated using loopback measurements.

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Chapter 1
Introduction

Low-cost implementation of automotive RADARs (Radio Detection and Ranging) is a cornerstone in the development of intelligent transportation systems. While radars have been studied and developed exhaustively during the last century due to their military (and to a lesser extent, scientific and industrial) significance [1], commercialization of automotive radar sensors remains a challenge due to cost and performance limitations. Silicon-based (CMOS, SiGe and BiCMOS) technologies have become popular over the last decade, enabling revolutionary growth in consumer electronics and communication systems. Silicon fabrication technology has the potential to reduce sensor development cost to an extent that will make automotive sensor technology economically viable. This dissertation presents several experimental implementations of silicon-based millimeter-wave transceivers for short-range automotive radar applications.

1.1 Motivation

Research and development of silicon-based solutions for millimeter-wave (MMW) applications has gained significant momentum in recent years. These applications include 60-GHz short-range high data-rate communications, automatic cruise control (ACC) and collision-avoidance systems using 24/77-GHz automotive radars, and more recently, 94-GHz security applications using passive imaging.

Automotive radar sensors enable a 360° safety zone around the vehicle. Several short-range sensors are usually mounted around the vehicle to detect objects at close range (0–40 m), which enable advanced driver-assistance and security functions including collision avoidance, precise airbag activation, parking assistance, improved road handling, lane change support and short-range ACC stop-and-go capability (Fig. 1.1) [2]. On the other hand, a single forward-looking sensor may be sufficient for long-range detection (≈150 m), primarily used for ACC [3].

As will be shown in Chap. 2 theoretically, high range-resolution radars demand big chunks of frequency spectrum. An important factor in the development of such

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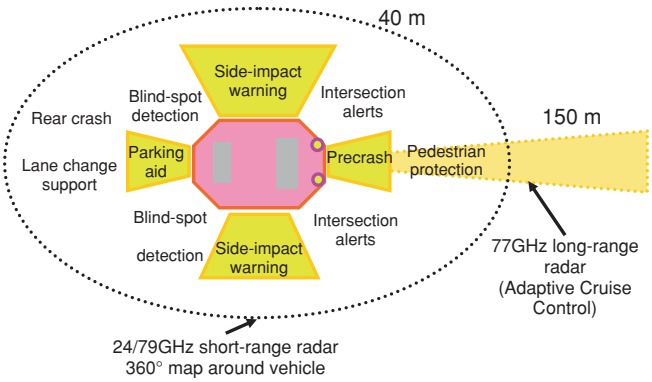

Fig. 1.1 Radars and their applications in an automotive environment

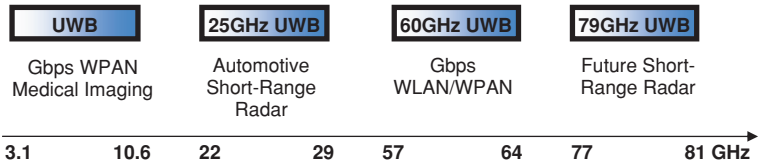

Fig. 1.2 UWB spectra allocated worldwide for several emerging applications

radar systems is thus a contiguous spectrum allocation by regulatory agencies worldwide. During the first half of this decade, several new bands were opened worldwide for UWB applications including data communications and automotive radars (Fig. 1.2). Frequency bands around 25 GHz have been allocated in both USA and Europe, exclusively for UWB vehicular radars. For example, Federal Communications Commission (FCC) in the USA has allocated an unlicensed 7-GHz-wide spectrum between 22–29-GHz (hereafter referred to as 24-GHz) with strict emission restrictions [4].

These allocations have instigated intensive research and development, both academic and industrial, to develop vehicular radar sensor systems. Long-range radars in III–V technologies enabling adaptive cruise control (ACC) operating in the 76–77-GHz (hereafter referred to as 77-GHz) band have been around for some time [3]. Since small form-factor and low cost are imperative for automotive applications, silicon-based implementations are attractive and can make radar sensors affordable to the end customer. In the last few years, silicon-based 24-GHz short-range automotive radars have been investigated both by industry and academia [2], [5–8]. Recent works have demonstrated the possibility of designing highly-integrated high-frequency circuits in advanced silicon technologies [9, 10]. In fact, 24-GHz silicon-based short-range radar sensors have already been deployed in the commercial automotive market [2]. Realization of 24-GHz

short-range radar transceiver circuits has been reported in a Silicon–Germanium (SiGe) process [2, 8], but suffers from limited integration, limited bandwidth and high power dissipation. Intensive research and development is also underway for developing 77-GHz long-range and 77–81-GHz short-range radars in silicon technologies [9–16]. Highly integrated silicon ICs with sophisticated electronically-steered phased arrays have also been demonstrated both in the K band [17–20] and the W band [21–22]. Most of the current efforts have focused on chip development in high-performance silicon–germanium (SiGe) technologies. A SiGe-based four-channel transceiver (TRX) IC for use in long-range ACC and collision-avoidance systems is in production [10]. Experimental results on a 75-GHz transceiver in 90-nm CMOS have recently been reported by the industry [23]. Narrowband silicon-based (SiGe and CMOS) transceivers for high data-rate wireless communications have also been reported in prior work [19, 20]. Nevertheless, the realization of fully-integrated truly-wideband automotive radars in silicon technologies is yet to be explored and is the subject of this dissertation.

This dissertation reports on the design, implementation and measurements of the first fully-integrated short-range automotive radar transceivers operating in the FCC-approved bands of 22–29 and 76–81 GHz in both CMOS and BiCMOS technologies. Novel circuit techniques employed in the transceiver designs enable the system to achieve a high range resolution and to detect objects at a close range, thereby demonstrating suitability for application in short-range radar systems. This work suggests that advanced silicon-based technologies will end the dominance of compound semiconductor technologies in automotive radar systems in the near future.

1.2 Organization

The remainder of this dissertation is organized as follows. Chapter 2 reviews the fundamentals and basic concepts of radars. In Chap. 3, the system-level details and considerations of ultra-wideband radars are discussed and specifications for 24/79-GHz radars are derived. The architecture, circuit design and implementation details of a 22–29-GHz 0.18 µm CMOS receiver front-end prototype are described in Chap. 4. Chapters 5 and 6 discuss the evolution, design and implementation of a dual-band radar transceiver in 0.18 µm BiCMOS technology. A 24/77-GHz dual-band frequency synthesizer is demonstrated in Chap. 4, while Chap. 5 discusses the design details of a 24/79-GHz dual-band radar transceiver chip. Finally, Chap. 6 provides concluding remarks and suggestions for future work.

Chapter 2
Radar Fundamentals

Radars are electronic systems that can detect and track objects. They can provide a highly accurate measurement of the distance, velocity and direction of the detected objects. In principle, every radar system (a) transmits electromagnetic energy to search for objects in a specific volume in space (b) detects the energy reflected from objects in that volume (c) measures the time between the two events, and (d) ultimately provides estimates of range, amplitude and velocity of the objects based on the detected energy and measured time. Several other conventional systems, including infrared and video sensors, have typically been used to perform the above functions, but radars have a significant advantage of being highly immune to environmental and weather conditions [10]. With technological advances leading to inexpensive radars, they are well-poised to replace existing low-functionality systems.

This chapter focuses on the basics of radars and reviews popular radar architectures, radar performance parameters and several performance enhancement techniques. The reader is referred to other texts for more detailed and comprehensive treatments of the subject [24, 25].

2.1 Radar Architectures

Several radar architectures have been studied and employed during the last century [1]. In the context of automotive radars, only a few architectures are of relevance, and can be classified into two categories: continuous-wave (CW) and pulsed. Performance of simple radars is seldom adequate for most applications and performance-enhancing techniques are almost always employed. One technique common to all radars is pulse compression, which is essentially frequency or phase modulation (FM/PM) of the radar signal for object detection at long range with adequate resolution, and will be described in a later section. Several architectures and techniques can be combined to form hybrid radars. Radar architectures are described in more detail in the following.

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2.1.1 Continuous-Wave Radars

Continuous-Wave (CW) radars transmit unmodulated or modulated frequency carrier as the radar signal. A simple unmodulated signal can only detect object velocity and not range, and hence is not useful in an automotive setting, which requires reliable detection of zero relative-velocity targets. In order to measure range, modulation of the radar signal is essential. Two popular modulation schemes in automotive CW radars are (a) Frequency chirp and (b) Pseudo-random Noise (PN) coding.

2.1.1.1 Frequency Chirped Radars

Frequency chirp architecture is the most popular for automotive radars, and has been employed traditionally in long-range high-power radar implementations. In frequency-chirped radars, the frequency of the radar signal is varied according to a pre-determined pattern. The most widely used patterns are (a) frequency-stepped, in which frequency is changed by a step in each time period and (b) linear frequency modulation (LFM), in which transmit frequency is changed continuously within each time period. This varying frequency essentially widens the bandwidth of the radar signal, which is equivalent to narrowing the signal in the time-domain. While detecting the velocity of the object, this pulse compression technique readily measures the range of the object. One of the main disadvantages of CW radars is that they suffer from limited dynamic range due to finite isolation between receive and transmit paths. In addition, the range resolution of frequency-chirped radars is dependent on the speed and bandwidth of the chirp, leading to stringent requirements on local-oscillator phase noise.

2.1.1.2 Pseudo-Random Noise Coded Radars

Pseudo-Random Noise (PN) codes are extensively used in communication systems for increased data-rate and superior interference-resilience [26]. A PN code is basically a binary periodic sequence with noise-like properties. It can readily be generated using a feedback shift register implemented with conventional digital circuits. Pulse compression in the context of PN coded radars is the same as coding or processing gain of the PN code [24]. PN codes are also known as spreading codes, and PN coded radars as direct-sequence spread spectrum (DSSS) radars, in conformity with their communications counterpart. While PN coded radars are robust to interference, their dynamic range is limited by the auto-correlation properties of the PN code. Furthermore, typical implementations of PN coded radars require complex frequency generation circuitry. Dynamic range limitations restrict the operating range of PN coded radars to 10 m typically [2]. A 79-GHz PN coded BPSK transmitter for short-range applications was recently presented [11], but no range performance was reported.

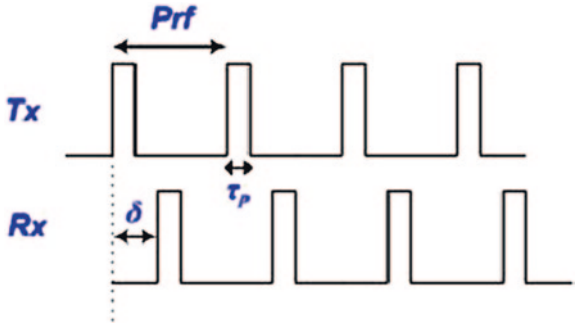

Fig. 2.1 Typical transmit and receive waveform envelopes in a pulsed-radar

2.1.2 Pulsed Radars

A pulsed-radar transmits modulated pulses at periodic intervals of time (i.e., a train of modulated pulses) as illustrated in Fig. 2.1. Range is readily extracted by measuring the time delay between the instants of pulse transmission and reception. Object velocity can be determined by measuring the rate of change of range, or by employing a bank of Doppler filters [24]. Pulse radar waveforms are characterized by three main parameters: (a) pulse-width, τ_p (b) carrier frequency, f_0 and (c) pulse repetition frequency, prf. The prf must be chosen to avoid range and Doppler ambiguities and to maximize average transmitted power. Range ambiguity decreases with decreasing prf, while Doppler ambiguity decreases with increasing prf. Radars with high prf are usually called pulsed Doppler radars. Intentional pre-determined jitter is sometimes introduced in the prf in order to avoid blind speeds and range and Doppler ambiguities.

In a pulsed-radar, the transmitter (TX) and the receiver (RX) essentially operate in a time-duplexed manner, and hence a high dynamic range can be attained. Although a complex timing engine with delay circuitry is required, pulsed radar is the simplest architecture to implement. Pulse compression is usually achieved using Binary Phase Shift Keying (BPSK) with Barker codes (more details in Sect. 2.7). In most of the following discussion, a pulsed-radar architecture is assumed.

2.2 Radar Range

The maximum target distance that radar can detect is usually referred to as the radar range. The target range, R, for a given pulse is determined by measuring the time delay, δ, it takes the pulse to travel the two-way path between the radar and the target. It is given by,

$$R = \frac{c\delta}{2}, \tag{2.1}$$

where $c = 3 \times 10^8$ m/s is the speed of light.

In order to avoid range ambiguity, after a pulse is transmitted, a pulsed radar must wait sufficiently long before it can transmit another pulse. This ensures that any returns from the targets at maximum range are detected. Then, for a given prf, the maximum unambiguous range can be determined as

$$R_u = \frac{c}{2 \cdot prf}. \tag{2.2}$$

2.3 Range Resolution

Range resolution is a radar performance metric, which measures the ability of the radar to detect objects in close proximity as distinct objects. The range resolution of radar determines the width of range gates or bins. It is easily observed that two objects need to be separated by at least $\tau_p/2$ in order to produce two distinct echo signals. Hence, the radar range resolution, ΔR, is given by

$$\Delta R = \frac{c\tau_p}{2} = \frac{c}{2B}, \tag{2.3}$$

where $B = 1/\tau_p$ is the signal bandwidth.

Short-range sensors demand high range resolution radars, implying wide signal bandwidth, and thus narrow pulses. This results in reduced average transmitted power. To maintain adequate range resolution without sacrificing transmitted power, pulse compression techniques must be employed.

2.4 Doppler Frequency

When a target is moving relative to the radar, the center frequency of the returned pulses is different from that of the incident pulses. The difference between the two is known as the Doppler shift or velocity, or just Doppler. It is given by

$$f_d = \pm\frac{2v}{\lambda} = \pm\frac{2v f_0}{c}, \tag{2.4}$$

where v is the target relative velocity, and λ is the radar wavelength. The shift is positive for an approaching target and negative for a receding target. If the target velocity is not in the radar line of sight, the Doppler shift becomes

$$f_d = \pm\frac{2v}{\lambda}\cos\theta = \pm\frac{2v f_0}{c}\cos\theta, \tag{2.5}$$

where $\cos\theta = \cos\theta_e \cos\theta_a$, μ_e is the elevation angle, and μ_a is the azimuth angle of the radar antenna.

2.5 Signal-to-Noise Ratio

Much of the determination of radar specifications depends on the required signal-to-noise ratio (SNR) at the radar receiver output, as will be shown theoretically in the next section. SNR itself depends on the required probability of detection and probability of false alarms for the radar. Probability of detection is the probability that the receiver output is above the detector threshold (i.e., the level above which an object is said to be detected) in the presence of signal and noise. Similarly, probability of false alarm is the probability that the receiver output is above the threshold in the presence of noise only. Determination of SNR from the aforementioned probabilities is complicated. A very accurate approximation is given by [27]

$$P_d \approx 0.5 \times erfc(\sqrt{-\ln P_{fa}} - \sqrt{SNR + 0.5}), \tag{2.6}$$

where P_d is the probability of detection, P_{fa} is the probability of false alarm, and erfc is the complementary error function.

2.6 The Radar Equation

The radar equation relates various radar system parameters to its range performance. It can be used to determine the required parameters from a given set of radar specifications. The power density at a distance R from a radar employing a directive antenna with gain G is given by Friis power transmission equation [28],

$$P_D = \frac{P_t G}{4\pi R^2}, \tag{2.7}$$

where P_t is the transmitter output power. When the radar signal is incident upon an object or target, it is scattered or radiated back. The amount of this radiation depends on the target size, orientation, shape and material, which are accounted for by an equivalent parameter called the radar cross section. It is the ratio of the power reflected by the target to the power density incident on it, and is denoted by σ. Thus, the total power received by the radar antenna is

$$P_r = \frac{P_t G \sigma A_e}{(4\pi R^2)^2}, \tag{2.8}$$

where A_e is the effective antenna aperture. A_e is related to the antenna gain by

$$G = \frac{4\pi A_e}{\lambda^2}. \tag{2.9}$$

Substituting A_e from (2.9) in (2.8),

$$P_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4}. \tag{2.10}$$

(2.10) can be re-arranged to determine target distance, R, as

$$R = \left(\frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 P_r} \right)^{1/4}. \tag{2.11}$$

Given the minimum detectable signal power, P_{min}, at the receiver, the radar maximum range, R_{max}, is readily obtained as

$$R_{\max} = \left(\frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 P_{\min}} \right)^{1/4}. \tag{2.12}$$

P_{min} can be written as

$$P_{\min} = kT_e B_n F (SNR_o)_{\min}, \tag{2.13}$$

where $k = 1.38 \times 10^{-23}$ Joules/Kelvin is the Boltzmann's constant, T_e is the effective noise temperature, B_n is the receiver noise bandwidth, F is the receiver noise factor (the ratio of input signal-to-noise ratio to output signal-to-noise ratio), and $(SNR_o)_{min}$ is the minimum required signal-to-noise ratio (SNR) at the receiver output. The radar range is then

$$R_{\max} = \left(\frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 k T_e B_n F (SNR_o)_{\min}} \right)^{1/4}. \tag{2.14}$$

Equivalently, the minimum output SNR is given by

$$(SNR_o)_{\min} = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 k T_e B_n F R^4}, \tag{2.15}$$

which is widely known as the radar equation (no radar losses and pattern propagation factors have been included for brevity). Usually, minimum output SNR is first determined from the probabilities of detection and false alarm. Then, the other parameters are calculated for a desired range performance. Due to implementation problems, most pulsed radars can not achieve sufficient output SNR for a desired range performance, with a single-pulse. This limitation is often resolved by integrating (coherently or incoherently [24]) several pulses returned from an object. Ideally, coherent integration of N pulses results in an N-times improvement in SNR, but system imperfections cause some amount of integration loss. The radar range can then (ideally again) be written as

$$R_{\max} = \left(\frac{P_t G^2 \lambda^2 N \sigma}{(4\pi)^3 k T_e B_n F (SNR_o)_{\min}} \right)^{1/4}, \tag{2.16}$$

where N is the number of integrated pulses.

Fig. 2.2 Barker codes

Code length	Code elements	Sidelobe level (dB)
2	+−,++	−6.0
3	++−	−9.5
4	++−+,+++−	−12.0
5	+++−+	−14.0
7	+++−−+−	−16.9
11	+++−−−+−−+−	−20.8
13	+++++−−++−+−+	−22.3

2.7 Pulse Compression

It was shown in Sect. 2.3 that short pulses exhibit better range resolution. But, this leads to a reduced average transmitted power, thereby reducing the radar range. In order to obtain average transmitted power of a long pulse and a range resolution of a short pulse, the signal can be frequency or phased modulated. This process is known as pulse compression.

Linear FM, PN coding and phase-coding are the most commonly used pulse compression techniques. High code-sidelobes are undesirable because noise and jammers located in the sidelobes may interfere with the target returns in the main lobe. While linear FM is easily implemented, its first sidelobe is approximately 13.2 dB below the main peak [24], which may not be sufficient for most radars. In phase-coding, a pulse is divided into sub-pulses, each of which has a particular phase selected according to a code sequence. The length of the code is known as the compression ratio. The most popular codes are the binary sequences, which have two phases. For binary sequences, it is highly desirable that the peak sidelobe of the autocorrelation function is the minimum possible for a given code length. One class of binary codes is the Barker code, which has optimal autocorrelation properties, and hence, is widely used in pulsed radars. All known Barker codes are listed in Fig. 2.2 with the corresponding sidelobe levels [24]. No Barker codes longer than 13 have been found to exist, and hence the maximum achievable compression ratio is 13. However, two or more Barker codes can be combined to generate higher compression ratios, although with sub-optimal autocorrelation. Barker codes (or binary codes in general) can be easily implemented using BPSK modulation.

For compression ratios larger than 13, PN coding is usually employed. PN codes and their generation were discussed in Sect. 2.1.1.

Chapter 3
Automotive Radars: System-Level Considerations

Design and implementation of radar transceivers require comprehensive understanding of system-level considerations and relevant spectral restrictions. This chapter presents an overview of the various spectra allocated for automotive radar sensors by regulatory agencies worldwide. Based on the regulatory requirements and using the concepts developed in the previous chapter, important system specifications for short-range radar transceivers are derived. These specifications govern the design of the circuit building blocks as will be clear in the following chapters.

3.1 Automotive Radar Spectra

Spectrum regulatory agencies worldwide have allocated several frequency bands exclusively for automotive radar applications. Fig. 3.1a shows the spectrum allocations, in United States and Europe, for the various systems that operate in the 22–29 and 77–81-GHz bands, including, in particular, the short range automotive radars. The above bands will hereafter be referred to as 24 GHz (or, K band) and 79 GHz (or, W band), for brevity.

The Federal Communications Commission (FCC) in USA has allocated an unlicensed 7-GHz-wide spectrum between 22–29 GHz with strict emission restrictions [4] [*cf*. Fig. 3.1a]. Similarly, the European Telecommunications Standards Institute (ETSI) has allocated the 22–26-GHz band for short-range automotive radars. The spectral density of the average transmitted signal should not exceed 41.3 dB m/MHz in this band [4]. As is clear from Fig. 3.1a, both FCC and ETSI allocations overlap with existing systems around 24 GHz. These systems include the unlicensed 24.125-GHz ISM (industrial, scientific, and medical) applications and more importantly, sensitive remote sensing and astronomy equipment [29]. While the FCC stipulates a transmitter center frequency above 24.075 GHz with limited emissions in the 23.6–24.0-GHz band in order to strongly minimize interference with remote sensing and radio astronomy equipment, the ETSI allocation is situated exactly at the center of the aforementioned sensitive applications.

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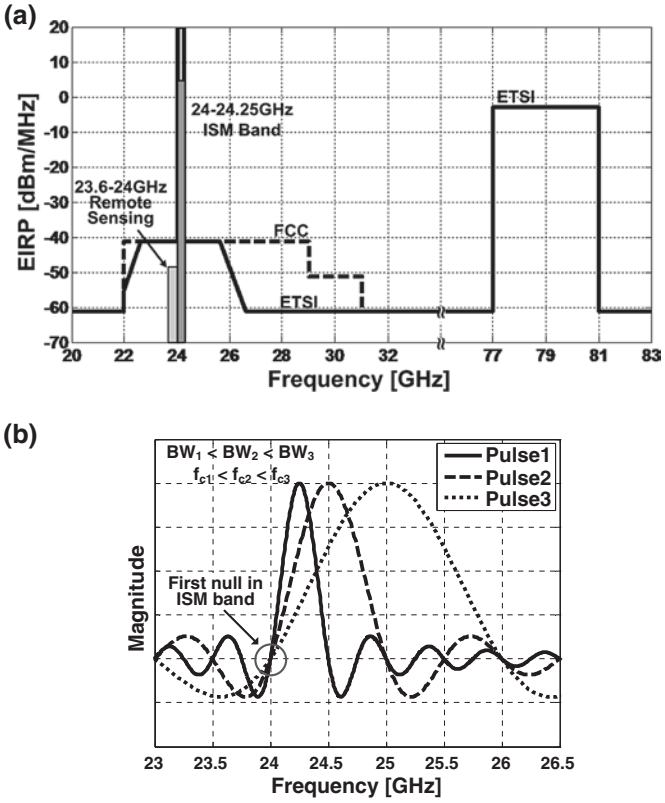

Fig. 3.1 Spectrum allocations for systems operating in the 24/79-GHz short-range automotive radar bands (*EIRP* Effective Isotropic Radiated Power). **b** Pulse-bandwidth (BW) dependent carrier frequency (f_c) ensures minimum emission in the ISM band located at 24.125 GHz

One potential solution to the above interference issue lies in adaptive waveform design. For instance, the local oscillator (LO) circuitry can be designed for a nominal center frequency of 26.5 GHz and a tuning range from 24.5 to 28.5 GHz. This choice of tuning range facilitates the use of a DSP (Digital Signal Processing) algorithm which sets the control voltage (and hence the oscillation frequency) of the oscillator, such that the first null of the sinc spectrum of a radar pulse falls in the aforementioned restricted band, thereby reducing unwanted emissions [2]. This idea is illustrated using Matlab simulations in Fig. 3.1b. As the pulse bandwidth increases, the carrier frequency is appropriately increased such that the first null stays in the ISM band.

A seemingly straightforward solution is to change the operation frequency to a different band, but requires regulatory action for spectrum allocation. Following this approach, the ETSI will discontinue the use of the 24-GHz allocation for automotive short-range sensors in mid-2013 [30], thereafter mandating a shift to 79 GHz. While this has spurred the interest in and the development

of 79-GHz radar sensors, the mature 24-GHz technology will likely continue to dominate the non-European markets. In fact, no corresponding 79-GHz allocation has yet been made available by the FCC. Therefore, next-generation radar sensors may well be required to support both frequency bands, for compatibility with frequency bands in the rest of the world and for lower overall cost. For this reason, the wideband 22–29 and 77–81-GHz short-range automotive radar bands have been chosen for the dual-band radar implementation in this work. As will be illustrated in detail in Chaps. 5 and 6, several novel circuit techniques are used to achieve dual-band operation, enabling a small die area and low power consumption.

The K-band allocations enable high range resolution due to the high instantaneous bandwidth (4–7 GHz), but restrict the transmitted power levels thereby limiting the maximum achievable range. FCC spectral occupancy limitations [4] and a range-resolution requirement of less than 5 cm [2] result in signal main-lobe (null-to-null) widths of around 10 GHz. Note that the FCC defines the bandwidth of a UWB signal as the frequency band bounded by the 10-dB c points of its spectrum. The 10-GHz null-to-null spectral width will therefore result in approximately an 8-GHz FCC signal bandwidth. In combination with the fact that the rise and fall times (≈50 ps) of the UWB pulses are not negligible compared to the pulse widths, this implies that pulses as short as 200 ps (unmodulated) are needed to occupy the entire FCC bandwidth of 22–29 GHz. Due to the relatively smaller bandwidth, longer pulses are necessary for the 77–81-GHz band. The rate at which the pulses are sent is called the pulse repetition frequency (prf) and is obtained from (Eq. 2.2) as

$$prf = \frac{c}{2R_u}, \tag{3.1}$$

where c is the speed of light and R_u is the minimum unambiguous radar range. Using (3.1), a minimum unambiguous radar range of 40 m results in a prf of 3.75 MHz. It is important to note that in order to meet the FCC average power emission requirements, either the prf or the pulse power must be decreased. A longer pulse can be transmitted with higher total pulse energy, resulting in a higher SNR. This would require a reduction in prf and the use of pulse compression techniques (e.g., BPSK and PN-coding) [24], in order to meet the spectral limitations and to achieve the same range resolution as a short pulse. Nevertheless, the pulse width cannot be arbitrarily increased due to the peak power emission restrictions.

3.2 Ultra-Wideband Radar Architectures

Several radar architectures have been studied and employed in the past (see [1, 24]). The choice of architecture for short-range radars is governed by the requirements of high range resolution, close-range detection and wide dynamic

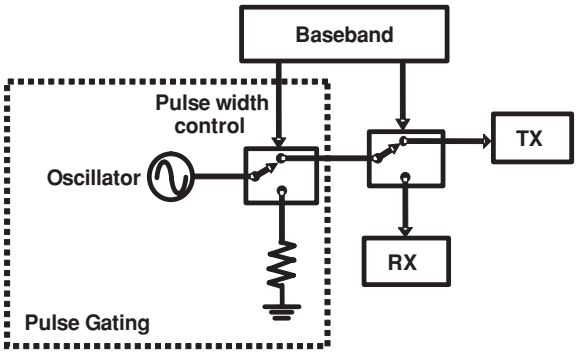

Fig. 3.2 Conceptual operation of a pulsed radar transceiver [2]

range. PN-coded radars and pulsed radars are the two most suitable architectures for meeting these requirements. Frequency chirped radars are difficult to implement for UWB bandwidth in excess of 1 GHz, due to the challenge of generating a wideband low phase-noise chirp in CMOS technologies. A recently published SiGe frequency synthesizer for 76-GHz long-range radars [11] exemplifies the level of complexity involved in meeting the phase-noise requirements of frequency-chirped radars. PN-coded radars, while interference-resilient, suffer from limited range due to poor isolation between the receiver and the transmitter (TX) and limited dynamic range [2]. Pulse-radars, on the other hand, can attain a high dynamic range as the RX and TX operate in a time-duplexed fashion. Higher dynamic range directly translates to improved range of the radar sensor, as objects at farther distances can be detected. The rather low complexity of the pulsed radar architecture makes it well suited for UWB 22–29 and 76–81 GHz millimeter-wave short-range radars.

In light of the aforementioned advantages, all of the radar prototypes described in the following chapters are based on pulse-radar architectures. In order to understand the radar operation, consider the conceptual block diagram of a pulse-radar transceiver shown in Fig. 3.2 [2]. The pulse width control signal gates the sinusoid from the oscillator to generate a high-frequency gated sine wave, which is then transmitted by the TX. This triggers a baseband delay circuitry which waits for a certain time until another trigger is enabled. At the second trigger, the second switch is changed from the TX to the RX. The receiver then samples its output at this instant. Thus, the input from the receiver antenna is multiplied with a replica of the transmitted pulse. If the two pulses do not overlap in time, the output will be zero, whereas if they are coincident, the output will be a maximum. The delay between the two triggers determines the range gate being scanned at the time. Thus, by changing this delay, objects at varying distances can be detected. Due to output power limitations and several other factors such as clutter, system losses and interference [25, 27], a single-pulse SNR can be negative for the desired range, and hence several received pulses need to be integrated to detect an object, as shown in the next section.

3.3 Radar System-Level Specifications

In the following discussion, we calculate the radar signal-to-noise ratio, given the typical requirement of detecting a 1-m^2 cross-section target at a 40-m range. For the 22–29-GHz FCC allocation, the peak EIRP (Effective Isotropically Radiated Power) must be less than 0 dBm in a 50-MHz bandwidth around the center frequency. This is equivalent to an EIRP of 17 dBm/MHz. For simplicity, we assume that this EIRP density is distributed uniformly across the 7-GHz bandwidth (this is optimistic, but sets the theoretical limit on the achievable performance; this also provides us with the worst-case transmitter output power.). Note that [2] makes the same assumption. This gives us the maximum peak EIRP of

$$EIRP_{pk} = -17 + 10 \cdot \log 7000 = 21.5 dBm. \tag{3.2}$$

Receiver antenna gain is calculated as [24]

$$G_{RX} = \frac{\pi^2}{\theta_e \theta_a} = 15.6 dBi, \tag{3.3}$$

where $\mu_e = 15°$ and $\mu_a = 60°$ are the elevation and azimuth half-power beamwidths in radians, respectively, and are typical values for short-range automotive radars.

Radar range equation can be written as

$$R_{\max}^4 = \frac{EIRP_{pk} \cdot G_{RX} \cdot \lambda^2 \cdot \sigma}{(4\pi)^3 \, kTBF \, (SNR_{\min})}, \tag{3.4}$$

where R_{max} is the radar range, λ is the signal wavelength, σ is the target cross-section, kT is the thermal noise power, B is the receiver noise bandwidth, F is the receiver noise factor and $(SNR_o)_{min}$ is the minimum required output signal-to-noise ratio. The required SNR is estimated to be about 11 dB, from the required probability of detection and probability of false alarm [27]. From (3.4), the single-pulse SNR is 1.1 dB, assuming a receiver noise figure of 4.5 dB based on the measured results of the 24-GHz receiver. It is clear that multiple received pulses must be integrated in order to improve the SNR and to raise the signal above the noise floor; coherent integration of n pulses ideally results in an n-fold improvement in SNR. Coherent integration of ten pulses is sufficient in this case to meet the required SNR target of 11 dB. In practice, more pulses would need to be integrated to ensure sufficient link margin.

For the 77–81-GHz band, ETSI has stipulated a generous 55-dBm peak EIRP limit. Following the same procedure as for the 22–29-GHz band above, we obtain a single-pulse SNR of about 25 dB assuming 8-dB noise figure, obviating the need to integrate multiple pulses. Nevertheless, in current silicon technologies, such power levels are difficult, if not impossible, to achieve. Using the

Range=40m, Target cross-section=1m^2, Probability of detection=0.9, Probability of false alarm=10^{-3}			
Frequency Range	22–29 GHz	77–81 GHz[a]	77–81 GHz[b]
Transmit peak EIRP	21.5 dBm	55 dBm	26.1 dBm
Receiver Antenna Gain	15.6 dBi	15.6 dBi	15.6 dBi
Signal Bandwidth	7 GHz	4 GHz	4 GHz
RX Noise Figure[c]	4.5 dB	8 dB	8 dB
Required SNR	11 dB	11 dB	11 dB
Single-pulse SNR	1.1 dB	24.9 dB	−1.2 dB
Number of integrated pulses	10	1	17

[a]Assuming maximum allowable EIRP by ETSI.

[b]Assuming maximum EIRP based on measured results from our transmitter (=10.5+15.6).

[c]Based on receiver measurements.

Fig. 3.3 Radar system-level specifications

measured transmitter output power of 10.5 dBm in the radar range equation and assuming the same transmit antenna gain as that of the receive antenna, we obtain a single-pulse SNR of 1.2 dB. In order to meet the SNR requirements, at least 17 pulses must be integrated. The above results are summarized in Fig. 3.3.

Chapter 4
A 22–29-GHz UWB Pulse-Radar Receiver Front-End

This chapter presents the detailed design and analysis of a CMOS short-range automotive pulse–radar receiver (RX) front-end operating in the UWB band from 22 to 29 GHz. Various design techniques are introduced in order to boost circuit performance at frequencies around only half of the transit (or unity current-gain) frequency, f_T, of the transistor ($f_T \approx 55$ GHz for 0.18 μm CMOS). An interference-reduction scheme is also presented that allows efficient use of the allocated power-constrained spectrum, while minimizing the interference with other systems operating in the same frequency range. Circuit techniques used in the UWB RX front-end design enable the radar sensor to potentially achieve a high range resolution and detect objects at a close range, thereby demonstrating suitability for integration in short-range radar systems.

The remainder of this chapter is organized as follows: Section. 4.1 discusses the architecture of the radar receiver. Section 4.2 describes the circuit design of the building blocks of the front–end. Measurement results are presented in Sect. 4.3. Finally, Sect. 4.4 provides concluding remarks.

4.1 Receiver Architecture

In light of the advantages described in Chap. 3, the proposed RX is based on a pulse-radar architecture. The receiver employs time-gated quadrature correlation architecture, as shown in Fig. 4.1. Essentially a direct-conversion architecture, this pulse-radar RX front-end is comprised mainly of:

(1) a 22–29-GHz UWB low noise amplifier (LNA);
(2) in-phase/quadrature (*I*/*Q*) mixers;
(3) a quadrature voltage controlled oscillator (QVCO);
(4) high-isolation pulse formers;
(5) baseband (BB) variable gain amplifiers (VGAs); and
(6) wideband integrate-and-dump circuits.

This work was done in collaboration with Sriramkumar Sundararaman [31–33]

V. Jain and P. Heydari, *Automotive Radar Sensors in Silicon Technologies*,
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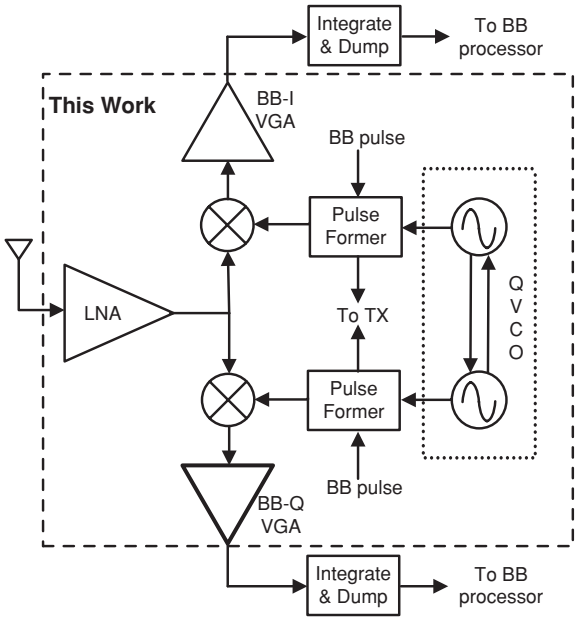

Fig. 4.1 Block diagram of the UWB pulse-radar receiver front-end

The UWB LNA amplifies the received wideband RF pulses with minimal magnitude- and phase-distortion. I/Q mixers correlate the amplified RF pulses with locally generated pulses (delayed replicas of the transmitted pulses) from the pulse formers. A free-running injection-locked QVCO generates I and Q differential LO signals, which are fed to the pulse formers through high-frequency tuned buffers. The pulse formers upconvert the baseband pulses to the vehicular radar band by modulating them on the 26.5-GHz (nominally) LO I/Q carriers. The cross-correlation products are then amplified by the baseband VGAs and fed to integrate-and-dump circuits for baseband processing. Note that the pulse generator and integrate-and-dump circuitry are not included, and are being developed as a continuation of this work.

4.2 Circuit Design

In addition to the numerous system-level issues discussed in the previous section, UWB radars present several circuit design issues. Particularly, obtaining a wide bandwidth with adequate circuit performance across the entire 22–29-GHz band is challenging. This is exacerbated by the limited gain of 0.18^{-1} m MOS transistors, with f_T of 55 GHz, over this desired range of frequencies. In this section, several circuit topologies for the critical building blocks of the proposed RX front-end are presented to address the UWB challenges. The circuits have been designed for a bandwidth of 7 GHz to maximize the achievable range, and to allow for process variations and design margins.

4.2.1 22–29-GHz UWB Neutralized LNA

Figure 4.2 shows the schematic of the UWB LNA comprising of two common-source amplifier stages employing wideband impedance matching and C_{GD} neutralization. Source–degeneration with inductor L_s is used in the first stage for impedance matching and linearity improvement, but not in the second stage so as to achieve sufficient gain. Each stage employs a feedback path consisting of a center-tapped inductor (L_4/L_6) and a MOS capacitor (C_{n1}/C_{n2}) to counteract the detrimental effects of the gate–drain capacitance, C_{GD}, on the frequency response and to guarantee the stability of the amplifier [34]. The center–tapped inductor (L_4/L_6) generates a phase-difference of 180° between its two terminals due to which the current flowing through the neutralization capacitor (C_{n1}/C_{n2}) is equal and opposite to that flowing through C_{GD}. MOS capacitors are used to realize the neutralization capacitors because they compensate (to the first order) for the voltage—and process-dependence of C_{GD}, thereby improving the neutralization accuracy. This technique ensures a stable amplifier, while eliminating the high-frequency noise and bandwidth degradation associated with a cascode LNA. This, in turn, yields a better noise figure (NF) and gain roll-off than the widely used cascode LNA. Intuitively, the NF of the LNA in this work is better than a cascode LNA, because it utilizes only one transistor per stage in the signal path. Moreover, at high frequencies, the parasitic inductance of the bypass capacitor connected to the gate of a cascode device can degrade the stability factor of the amplifier [35].

Simulation data comparing the behavior of minimum noise figure, gain, and reverse isolation with respect to frequency for common-source, cascode and perfectly-neutralized amplifier stages are shown in Fig. 4.3. As evident from this figure, a C_{GD}-neutralized stage provides higher gain and lower minimum noise figure than both common-source and cascode amplifiers, while achieving reverse isolation as good as that of a cascode stage. The suitability of an amplifier to be used in a multi-stage amplifier can be ascertained by determining its noise measure M given by [36].

$$M = \frac{F - 1}{1 - \frac{1}{G_A}} \tag{4.1}$$

where F is the noise factor and G_A is the available gain of the amplifier. Due to its higher available gain and lower minimum noise figure, the neutralized stage has a lower noise measure than both common-source and cascode stages, as shown in Fig. 4.3.

Since correct operation of the neutralized amplifier depends on the cancellation of C_{GD}, it is important to investigate the sources of imperfect cancellation and their impact on the circuit performance. One source of error originates from the center-tapped inductor itself, namely, the imperfect coupling factor, i.e., $k < 1$, between the two halves. A non-unity coupling factor results in a deviation from the

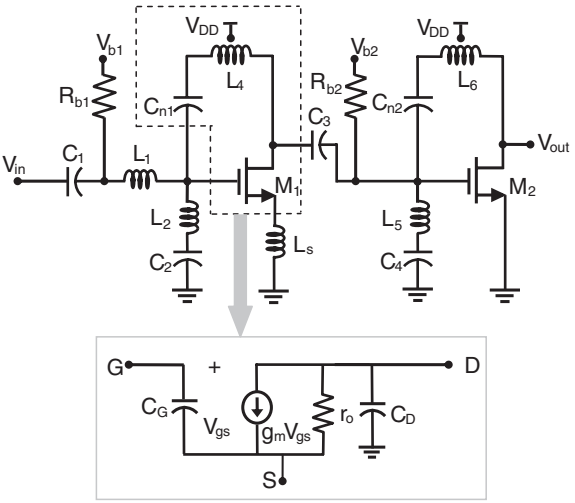

Fig. 4.2 Schematic of the UWB LNA with a simplified small-signal model of the first stage transistor

ideal 180° phase difference at the inductor terminals. Using the circuit analysis of the LNA, the phase error ε_ϕ can be expressed as

$$\varepsilon_\phi = \tan^{-1}\left[\left(1-k^2\right)\frac{\omega L}{Z_L}\right], \tag{4.2}$$

where L is the half-inductance of the center-tapped inductor and Z_L is the load impedance seen by the inductor at the amplifier's drain terminal. The change in phase error as a function of k is shown in Fig. 4.4a indicating negligible phase error due to imperfect coupling. For the center-tapped inductors used in the LNA, a k of 0.73 was extracted from electromagnetic (EM) simulations. The extracted broadband model of the center tapped inductors is shown in Fig. 4.5a, where element values are obtained from EM simulations. The EM-simulation result of the inductance and its quality factor with respect to frequency are shown in Fig. 4.5b.

Another source of imperfect cancellation is the variation in the neutralization capacitor caused by process/temperature variations and layout parasitics. While using a MOS capacitor to realize the neutralization capacitance reduces the effects of these variations, adequate tolerance to these variations is essential for robust circuit operation. Figure 4.4b shows the effect of variations in neutralization capacitance on reverse isolation of the amplifier at 30 GHz (upper corner of frequency band of interest), with $C_{GD} \approx 35$ fF. Even with more than 60 % deviation from the optimum value of the neutralization capacitor, the reverse isolation is still better than that of a common source amplifier, demonstrating the robustness of the cancellation technique.

It turns out that the presented neutralization technique is inherently broadband and largely independent of frequency. However, in an RF LNA, another constraint, namely impedance matching, must be taken into account. While this

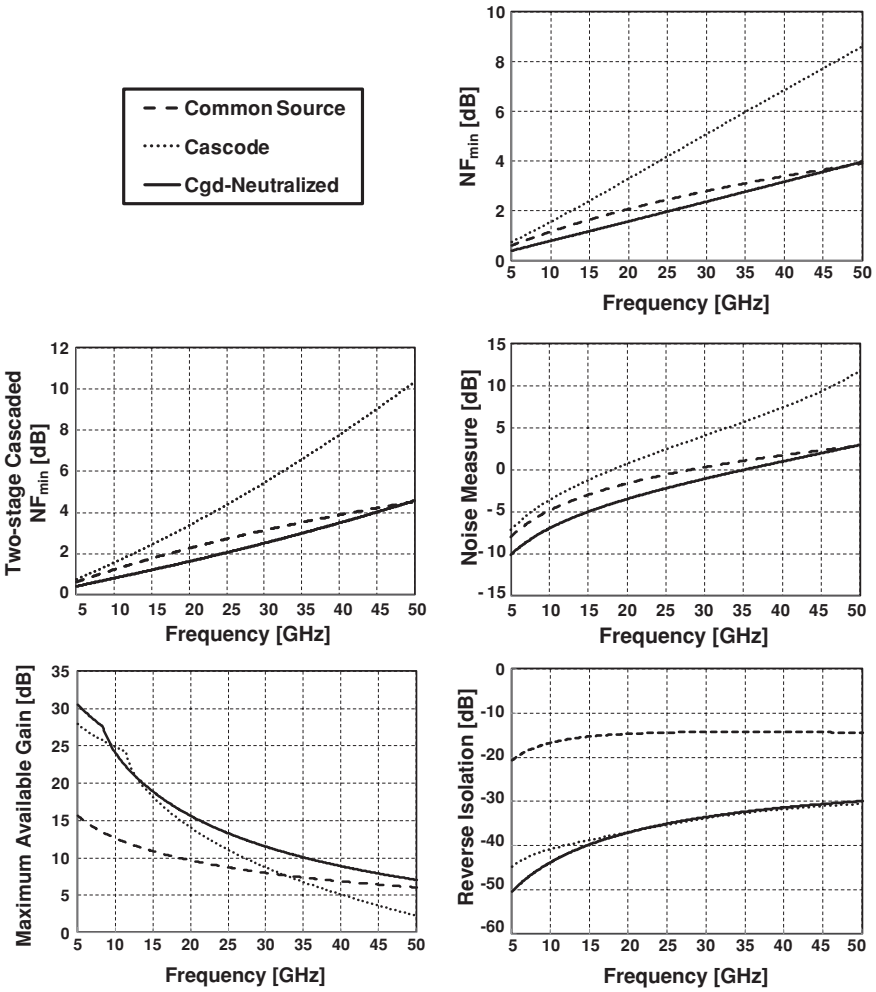

Fig. 4.3 Comparison of maximum available gain, reverse isolation and minimum noise figure

C_{GD}-neutralization technique does not affect the input match, it affects the output impedance of the common-source amplifier. In order to decouple neutralization and matching constraints, the output matching network is first designed to cancel the reactive part of the transistor output impedance, which sets the value of the neutralization inductor as a part of this matching network (*cf.* Fig. 4.6). The inductor is then converted to a center-tapped transformer with the same half-inductance. A neutralization capacitance value is then readily found, which completes the design.

Wideband power-match is essential at the input of the LNA for maximizing power gain across the entire signal bandwidth. To this end, a third-order elliptic

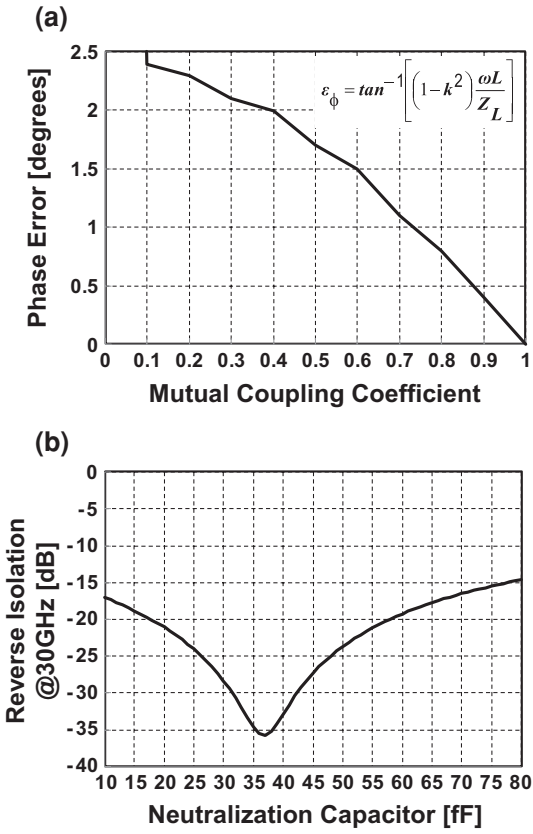

Fig. 4.4 Sources and effects of imperfect neutralization. **a** Phase error at the center-tapped inductor terminals as a function of the mutual coupling. **b** Reverse isolation of a C_{GD}-neutralized stage at 30 GHz with varying neutralization capacitor; $C_{GD} \approx 35$ fF

band–pass filter (BPF) network has been designed at the LNA input port. The BPF includes the source-degeneration inductor L_s and resonates out the reactive component of the LNA input impedance over the entire 22–29-GHz bandwidth, thus providing a wideband 50—input match. The initial BPF network was readily obtained by band–pass transformation of a third–order Cauer (or elliptic) low-pass filter. The network with actual device models was then optimized using simulations. A Cauer implementation is proven to be order–efficient [37], and hence the designed BPF requires fewer passive elements than an equivalent Butterworth or Chebyshev implementation (such as the one used in the 3.1–10.6-GHz LNA in [38]) for a given set of filter characteristics. The equivalent Cauer BPF is shown in Fig. 4.7a and the simulation of the standalone BPF exhibits a pass-band 3 dB bandwidth of 34 GHz, as shown in Fig. 4.7b. Furthermore, although an elliptic filter can be designed to obtain a superior transition band response, attempt here has been made to re-use the same components to realize the filter and the neutralization. Therefore, gain roll-off is not given a high priority. Note that the dc blocking capacitors C_1 and C_2, both 950 fF, are part of the wideband matching network.

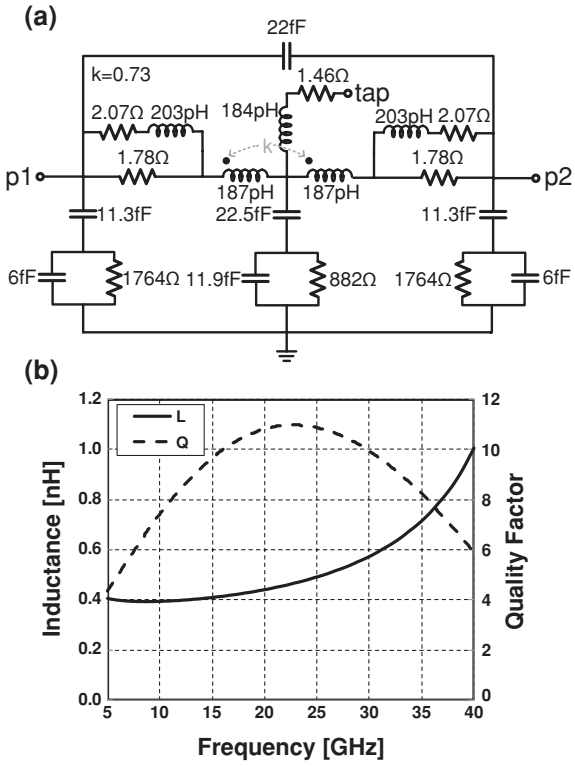

Fig. 4.5 **a** Broadband model of the center-tapped inductors extracted from electromagnetic simulations. **b** Simulated half-inductance and Q

The feedback path elements in the second stage along with the LC section L_5-C_4 constitute the inter-stage matching network in the LNA. The first stage is optimized for minimum noise figure, while the second stage is designed to be the major contributor to the overall power gain.

The use of common-source stages and inductive degeneration improves the linearity of the LNA, hence reducing distortion of the UWB pulses. The LNA achieves a peak power gain of 18 dB, input-referred 1-dB compression point of 7.2 dBm, and a noise figure less than 6 dB across the 22–29-GHz band.

To verify the superior performance of the proposed LNA compared to the cascode topology, and to prove guaranteed stability, a circuit analysis of the LNA is presented in the following.

Assuming perfect cancellation of C_{GD} using the neutralization technique, C_{GD}, the neutralization capacitor C_{n1}, and the center-tapped inductor are removed from the small-signal circuit model, shown in Fig. 4.2. Thus, the gain of the neutralized stage is

$$A_v = -g_{m,eq}(r_o||Z_L), \tag{4.3}$$

where $g_{m;eq} = Q_{in}g_m$ is the equivalent transconductance of the amplifier, Q_{in} is the Q-factor of the input matching network, Z_L is the load impedance including the drain

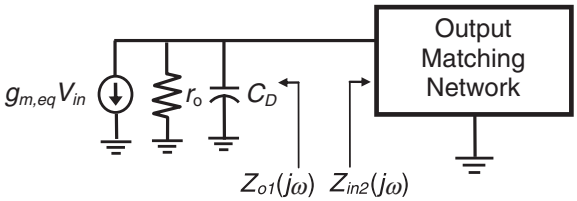

Fig. 4.6 The small-signal equivalent circuit at the output of LNA's first stage

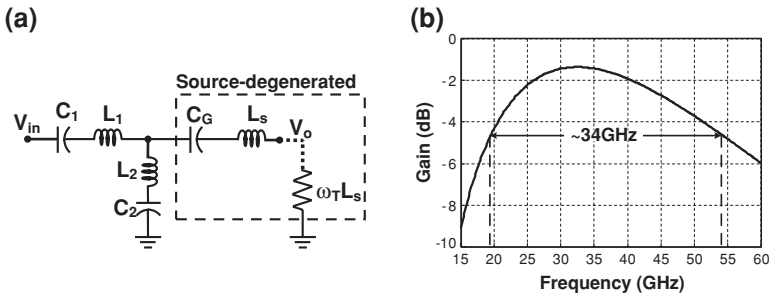

Fig. 4.7 **a** Equivalent third-order Cauer BPF matching network at the input of the LNA

capacitance C_D, and r_o is the output resistance of the transistor. The small-signal model of the first stage of the LNA with the above simplifications is shown in Fig. 4.2.

Considering only the drain current noise, the noise figure of the neutralized LNA can be shown to be

$$F_1 = 1 + \frac{(Y_s^2 + \omega^2 C_G^2)\gamma g_{d0} R_s}{g_m^2} \tag{4.4}$$

where Y_s is the source admittance, R_s is the source resistance, ω is the operating angular frequency, $^\circ$ is technology–dependent excess noise parameter [34], and g_{d0} is the drain–source conductance at zero drain–source voltage.

On the other hand, in a cascode LNA, the extra common–gate transistor contributes additional noise, resulting in an overall noise figure of

$$F_2 = F_1 + \frac{\omega^2 (C_{G1} + C_{G2})^2 (Y_s^2 + \omega^2 C_{G1}^2)\gamma g_{d02} R_s}{g_{m1}^2 g_{m2}^2} \tag{4.5}$$

where C_{G2}, g_{m2} and g_{d02} are the corresponding parameters of the cascode transistor. Because of the C_{GD} neutralization, the noise figure of the neutralized LNA approaches that of a common-source amplifier with C_{GD} ignored. Detailed analyses of the common-source LNA can be found in [38, 39].

A major noise source that becomes significant at high frequencies is the induced gate noise [34] resulting from the capacitive coupling of the gate to channel fluctuations and noise. With the aid of an analysis introduced in [40] and

taking into account the gate-induced noise and noise contribution of the physical gate resistance, the noise figure of the LNA without neutralization is obtained as

$$F_1' = 1 + \frac{r_G}{3R_s} + \frac{\gamma g_{d0}\left[\left\{\left(\frac{1}{|c^2|}-1\right)\kappa_c^2 + \left(\frac{C_{GD,M}}{C_G}+\kappa_c+1\right)^2\right\}\left\{\omega\left(\frac{r_G}{3}+R_s\right)C_G\right\}^2\right]}{g_m^2 R_s} \tag{4.6}$$

where $C_{GD,M} = (1 + g_m r_o)C_{GD}$ is the Miller equivalence of gate-drain overlap capacitance, r_G is the gate physical resistance, c is the correlation coefficient between gatsse and drain noise currents [34], and $\kappa_c = |c|\sqrt{\delta/(5\gamma)}$ (where $\pm$ is gate noise coefficient, a technology-dependent constant [34]). From (4.6), it is observed that the contribution of induced gate noise to the total noise figure becomes noticeable at high frequencies and with increasing gate–drain capacitance. Neutralization technique in the LNA, therefore, effectively reduces the C_{GD} effect, leading to a noise figure even better than the common-source amplifier, as also seen in simulations in Fig. 4.3.

Since the neutralized LNA relies on proper frequency–dependent feedback, its stability must be examined. A common-source amplifier becomes unstable at operating frequencies close to a significant fraction (dependent on foundry technology and transistor layout) of the transistor f_T. This is because the gate–drain capacitance provides undesirable positive feedback between the input and output, inducing oscillations in the circuit. The LNA demonstrated in this work, on the other hand, does not suffer from any such instability, owing to the C_{GD} cancellation technique. The real part of the input impedance of the neutralized LNA is obtained as

$$\mathrm{Re}\left[Z_{in}(\omega)\right] = \frac{(r_o + \mathrm{Re}\left[Z_L\right])^2 + \omega^2 L_s^2}{\omega^2 L_s C_G (r_o + \mathrm{Re}\left[Z_L\right])(\omega^2 L_s C_G + g_m r_o)} \tag{4.7}$$

Load impedances are typically on the order of tens of ohms in high-frequency CMOS amplifiers. Therefore, as readily ascertained from (4.7), the real part of the input impedance is positive for all frequencies and the amplifier stability is guaranteed. Furthermore, as expected, no stability problems were observed in simulations as well as measurements. The bulk terminal of each transistor in the amplifier is connected to the source, hence eliminating the body-effect and avoiding bandwidth degradation caused by the source-to-bulk capacitance. Although the drain-bulk capacitance affects the input impedance because of the feedback from source to gate, its contribution to bandwidth degradation at high frequencies is negligible due to the Miller effect [38].

4.2.2 Quadrature Mixers and Baseband VGAs

Two single-balanced mixers operating in quadrature mode correlate the amplified RF pulse (from the LNA) with local delayed replicas of the transmitted pulse. The schematic of one of the mixers is shown in Fig. 4.8, with the other mixer exactly

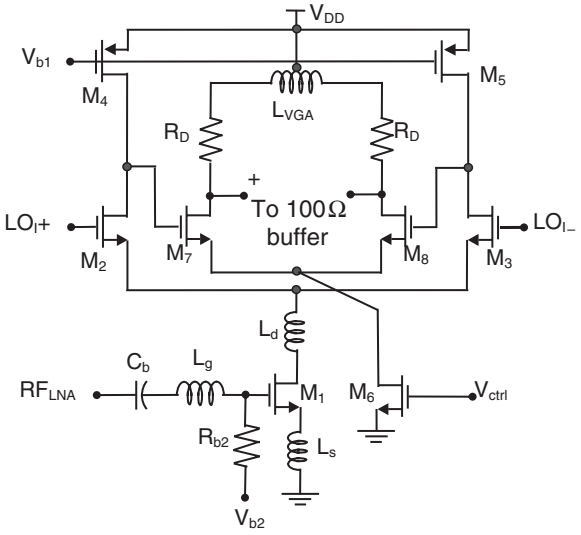

Fig. 4.8 Schematics of the mixer and variable gain amplifier

the same. The amplified pulse is applied at the RF port, while the local pulse drives the LO port. PMOS active loads are used to increase the conversion gain while maintaining a 3-dB bandwidth of about 3.5 GHz in each of the I and Q paths. The output load of the LNA (L_6, r_{o2}), the mixer input network (C_b, L_g, L_s) and C_{GD1} and L_d form a wideband matching network between the LNA and the mixer.

L_s also boosts mixer linearity as it provides a local series feedback path, but with accompanying reduction in gain. Besides participating in the impedance match at the mixer input, L_d enhances the RF transconductance's bandwidth by providing high-frequency isolation of the drain of M_1 from the noisy common source node of switch-pair M_2–M_3. It also improves the impedance-match at the LO port, where the switching transistors essentially operate in a common–source fashion at the switching instants. Each mixer is followed by a baseband (0–3.5-GHz bandwidth) differential amplifier with variable broadband gain of up to 10 dB controlled by the tail current of the amplifier. Shunt-peaking [34] optimized for maximally flat group delay is employed to enhance VGA bandwidth and to ensure minimum distortion of the baseband pulses at the output of the amplifier. Differential topology is used for the VGA to improve IIP_2 of the receiver. Baseband outputs are taken off–chip through doubly-terminated 100—differential buffers for differential measurements using standard 50—equipment. The mixers and VGAs draw a total of 20 mA while the output buffers draw 21 mA from a 1.8-V supply.

4.2.3 Pulse Formation

One of the most critical building blocks of the radar receiver presented in this work is the pulse generation circuitry. The conceptual operation of the LO pulse generation circuit is illustrated in Fig. 4.9 [41]. An oscillator generates a sinusoidal

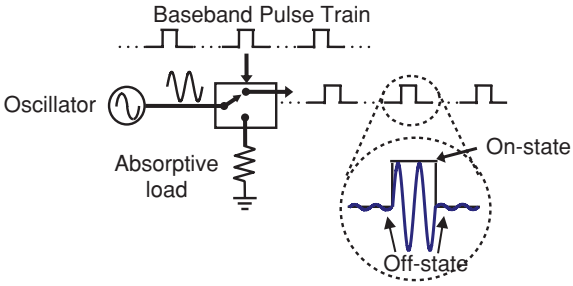

Fig. 4.9 Conceptual operation of the high-frequency pulse generation circuitry [41]

signal, which is either directly passed to the output when the baseband pulse is high, or directed into an absorptive load when the baseband pulse is low. As shown in the figure, the envelope of the output is ideally the same as the baseband pulse. It is also apparent that due to finite isolation of the conceptual single-pole double-throw switch, part of the sinusoid leaks to the output even when the switch is in its off–state.

It is readily inferred from the previous sections that a local oscillator with a wide tuning range (24.5–28.5 GHz) and quadrature outputs is needed. This is accomplished by employing an injection-locked quadrature VCO, first presented in [42]. For convenience, the circuit schematic of the QVCO is shown in Fig. 4.10. The QVCO consists of two cross-coupled LC VCOs with injection–locking signals provided through coupling transistors to establish quadrature relationship between the differential outputs of the two VCOs. The phase relationship between the VCO outputs is illustrated in Fig. 4.10. Frequency tuning is achieved through accumulation-mode MOS varactors, with variable capacitance controlled by an external voltage V_{cont}. The outputs of the VCOs are buffered to the pulse formers through high-frequency buffers. These tuned amplifiers shield the VCO circuits from the switching effects of the pulse formers, hence reducing frequency pulling. The center-tapped spiral inductor in the VCO tank is 495 pH and has a Q of 18. The Q of the varactors is 8.

The QVCO operates from a 1.5-V supply (lower than the receiver's nominal 1.8-V supply voltage) which linearizes the varactors, and hence, helps in achieving higher tuning range and lower phase noise. This is shown in Fig. 4.11, where varactor capacitance is plotted as a function of the supply voltage. The average change in capacitance over one oscillation cycle is lower at point A ($V_{DD} = 1.5$ V, where the slope is relatively constant) than at point B ($V_{DD} = 1.8$ V), resulting in a lower phase noise at 1.5-V supply. The measured phase noise at a carrier frequency of 26.5 GHz is 107 dBc/Hz at 1-MHz offset (cf. Sect. 4.3), which is better than the phase noise (104 dBc/Hz) of the SiGe VCO reported in [43]. Note that despite making efforts in lowering the phase noise of the QVCO of Fig. 4.10, the close-in phase noise of the oscillator will corrupt the extraction of Doppler information from the received signal, and hence a phase-locked loop (PLL) should be employed. The design of K-band PLLs has been reported in [19, 44–47].

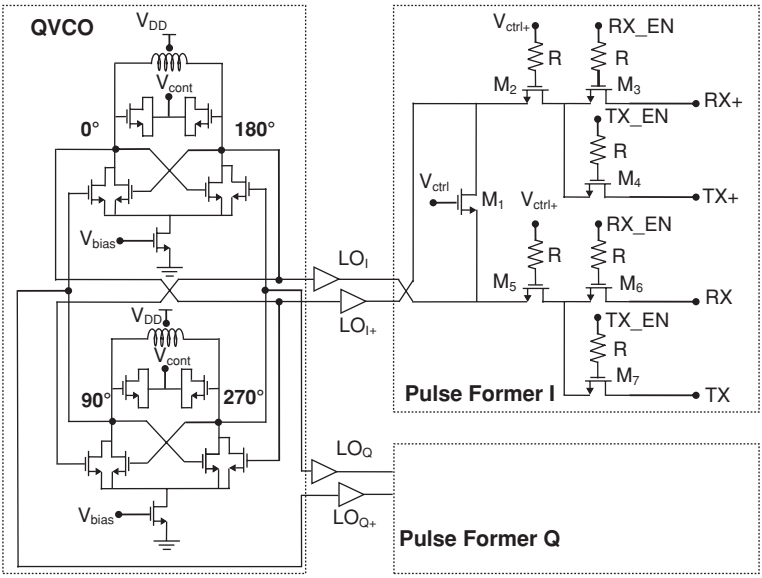

Fig. 4.10 Schematics of the quadrature VCO and pulse formers

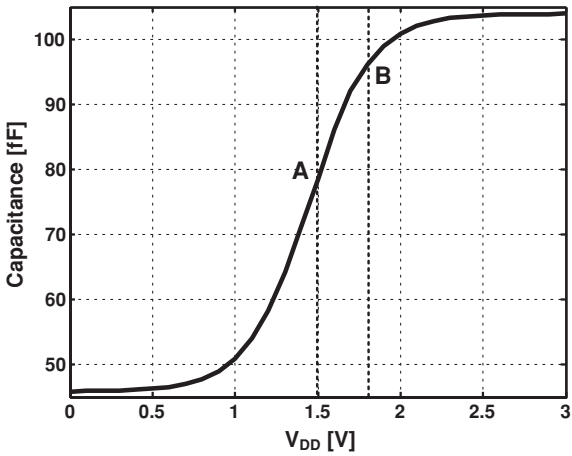

Fig. 4.11 Varactor capacitance as a function of VCO supply voltage

The pulse former shown in Fig. 4.10 is used in each of I and Q paths to upconvert the baseband pulse to the LO frequency. Prior art [48] suggests that the use of 0.18 μm MOS switches in RF transceivers is possible up to frequencies on the order of a few giga-hertz only. This limitation exists only for small signal operation and especially when the switch terminals need to be conjugate-matched to external 50—impedances, e.g., as in a transmit/receive antenna switch. With careful design, MOS switches can be efficiently used in high-frequency

large-signal systems as is demonstrated for the pulse former circuit presented in this work. In fact, the pulse former of Fig. 4.10 exhibits low on-state insertion loss and superior off-state LO leakage (cf. Sect. 4.3).

The design of this pulse former involves several trade-offs such as (1) minimizing on-state insertion loss, off-state LO leakage and, rise and fall times; and (2) maximizing dynamic range and pulse energy. In Fig. 4.10, M_2 and M_5 modulate the differential LO with the baseband pulse. The upconverted pulse is then sent either to the TX or the RX depending on the states of TX-enable (TX_EN) and RX-enable (RX_EN) signals. M_1 serves several important purposes in the pulse former: (1) it acts as a dissipative load for the LO sinusoids when the baseband signal is low; and (2) it also ensures that a constant impedance is presented to the LO outputs irrespective of the state of the baseband pulse. These functions are critical for shielding the LO from switching transients and pulling. While degrading the on-state insertion loss, M_1 improves off-state isolation. 3-V signals are used to enable the switch network so as to minimize on–resistances of the switch transistors. The common-mode at the LO port of the pulse former is chosen so as to provide adequate dynamic range while ensuring that the MOS switches operate outside the breakdown region (<2 V between any two MOS terminals for the foundry process used in this work). 1-kΩ resistors (R) are used to improve ac isolation between any two switches driven by the same control signal. Since this work does not include the transmitter, the differential TX ports of the pulse formers are terminated on–chip by precision 100—resistors. While exhibiting performance comparable to the SiGe design in [49], the I/Q pulse formers in this work occupy a die area of 0.05-mm^2 only and consume zero dc power.

4.3 Measurement Results

Device modeling, passive component performance and simulation methodology are major challenges for highly–integrated high-frequency designs. In order to alleviate these problems, the receiver design was optimized using measured data for active devices and a combination of electromagnetic (EM) simulations and measurements for passives as discussed below.

The radar receiver front-end was fabricated in a commercial 0.18 μm CMOS process with an NMOS f_T of 55 GHz and six metal layers. Substrate loss and noise-coupling severely affect signal integrity at high-frequencies, especially in systems with highly sensitive building blocks like VCO and LNA. To address these issues, spiral inductors designed in the 2.34 μm–thick top metal layer were surrounded by substrate contacts to reduce substrate noise coupling. Inductors were separated by a minimum distance of 50 μm to minimize both magnetic and electrical coupling. Moreover, the inductors in the I and Q branches in the LO path and the downconversion chain were oriented at 180° to minimize I/Q mismatch. This is especially critical for the QVCO as any stray coupling through the inductors can overshadow the injection-locking mechanism. Half-turn

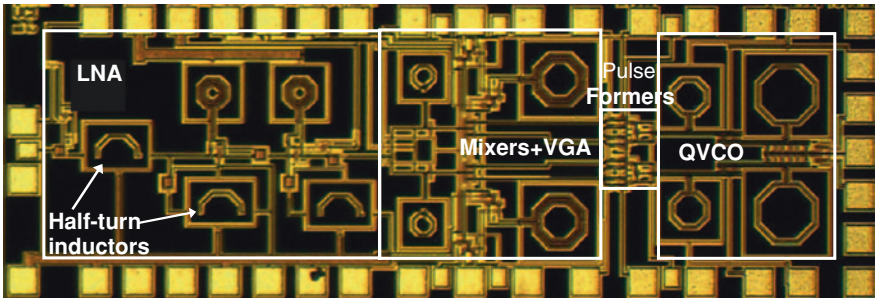

Fig. 4.12 Die micrograph of the receiver front-end measuring 3-mm × 1-mm

inductors (microstrip) with dedicated return path were designed to realize gate and source-degeneration inductances of 50–100 pH in the LNA. MOS transistors were laid out in a triple well for isolation from substrate noise. Small (70 μm × 50 μm) signal pads were used to reduce pad capacitance and hence substrate loss.

Test structures were fabricated for active and passive devices including MOSFETs, MOS varactors, transmission lines and spiral inductors with corresponding de-embedding structures. Measured S-parameter data for active devices was used directly for S-parameter and transient simulations. Parameterized models with optimization capability were developed for inductors and transmission lines using ADS Momentum EM simulator. These models were used to optimize the initial design of the entire receiver front-end. Sonnet EM simulator was calibrated against the measured data from the passive-device test structures [50]. The calibrated Sonnet simulator was then used for further verification and optimization of the passive devices designed with Momentum. Inductors were optimized for low loss and high self-resonance frequency. The microphotograph of the chip is shown in Fig. 4.12. The chip area is 3-mm × 1-mm including the pads. The dc pads of the chip were wire-bonded directly to a PCB and on-wafer microwave measurements were carried out to characterize the receiver performance. The LNA, QVCO and pulse formers were measured separately. The forward gain, S_{21}, and NF of the LNA vary from 15.2 to 18 dB and from 4.5 to 6 dB across the 22–29-GHz band. The input return loss, S_{11}, and reverse isolation, S_{12}, of the LNA are less than 15 and 35 dB, respectively. Two important parameters were measured for the pulse former. The on-state insertion loss varies from 2.2 dB (at 29 GHz) to 1.5 dB (at 22 GHz). The off-state LO leakage varies from 29.5 dB (at 22 GHz) to 26 dB (at 29 GHz). The QVCO achieves a measured phase noise of 107 dBc/Hz at an offset of 1 MHz from 26.5 GHz, as shown in the phase noise profile in Fig. 4.13a. The QVCO frequency is tunable from 24.3 to 28.2 GHz, as indicated in Fig. 4.13b.

The measured conversion gain and NF of the receiver front–end are shown in Fig. 4.14. The conversion gain varies from 35 to 38.1 dB and NF is less than

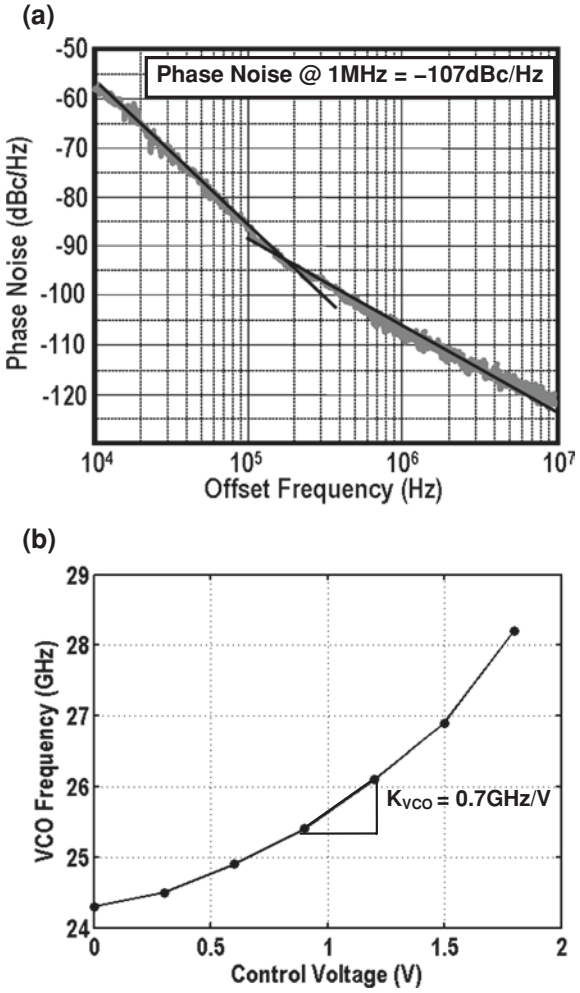

Fig. 4.13 **a** Measured phase noise and **b** tuning curve of the QVCO

7.5 dB across the entire 22–29-GHz band. NF varies less than 0.5 dB across the VGA gain settings, which is expected because the noise of the baseband circuits is suppressed by the high LNA gain. The wideband input return loss achieved by the receiver is shown in Fig. 4.15 and is lower than 14.5 dB in the desired band.

On-wafer measurements of the RX chip indicate an input–referred 1-dB compression point, P_{1dB}, of 20.8 dBm, as illustrated in Fig. 4.16, and an IIP_3 of 9 dBm. P_{1dB} varies from 20.8 dBm to 13 dBm between the highest and lowest gain settings of the VGA, respectively. Owing to the carefully designed pulse former, the RX achieves excellent port-to-port isolation. The measured LO-to-IF leakage and the LO-to-RF leakage are lower than 23 and 30 dB, respectively,

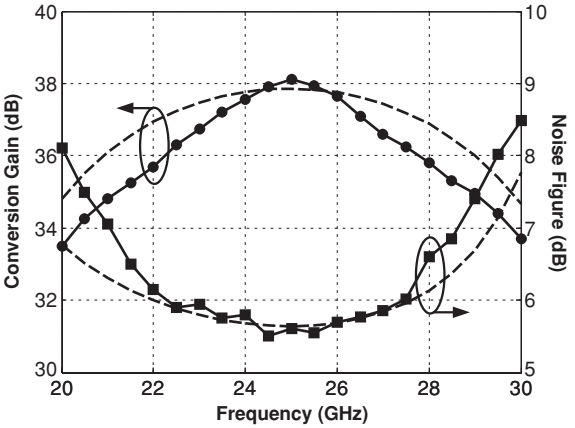

Fig. 4.14 Measured (*solid lines*) and simulated (*dashed lines*) conversion gain and noise figure of the receiver

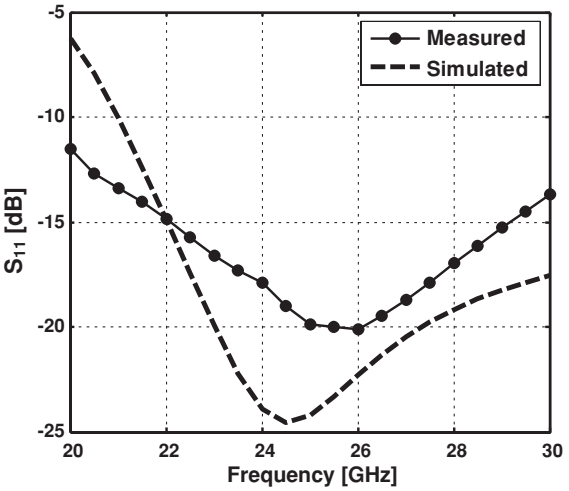

Fig. 4.15 Measured and simulated input return loss of the front-end

over the entire bandwidth. The measured power consumption of the receiver is 131 mW, more than half of which is due to the LO and output buffers.

In order to validate the UWB operation of the receiver front-end, pulse-based measurements were performed. A narrow-pulse train was applied at the baseband ports of the pulse formers, and a 24-GHz sinusoid was fed to the LNA input. The pulse train was upconverted to 24 GHz by the on-chip pulse former and then downconverted to the receiver baseband after multiplication with the 24-GHz sinusoid from the LNA. The measured transient waveform of the downconverted pulse is shown in Fig. 4.17. The measured 50 % pulsewidth is 250 ps, as shown in Fig. 4.17.

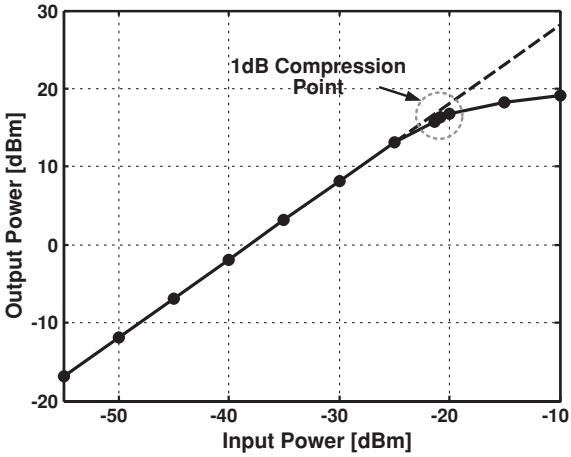

Fig. 4.16 1-db compression point

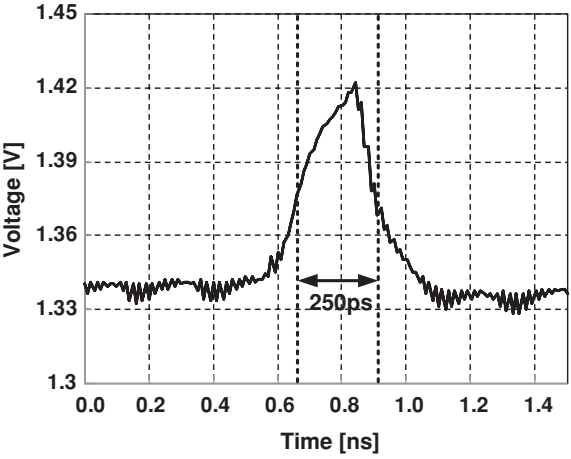

Fig. 4.17 Measured time-domain pulse output

Figure 4.18 compares this design with the SiGe RX in [8] designed for the same application. The measured performance of the receiver front-end is summarized in Fig. 4.19.

4.4 Chapter Summary

In this chapter, the design of a CMOS UWB receiver front-end operating in the 22–29-GHz band suitable for use in automotive short-range radar sensors has been described. On-wafer measurements of the fabricated prototype exhibited excellent

	This work	RFIC '06 [8]
Integration	LNA + Mixer + VGA + QVCO + Pulse former	LNA + Mixer + VGA + Switch + Integrator
Technology	0.18μm CMOS	SiGe
Bandwidth	21.3-29GHz	22-26GHz (LNA)
Conversion gain	38.1dB	45dB
Noise Figure	5.5dB	7.8dB
Power dissipation	131mW	1.08W

Fig. 4.18 Comparison with RX in [8]

Receiver		**QVCO**	
3dB Bandwidth	21.3-29GHz	Phase Noise @ 26.5GHz	−107dBc/Hz @ 1MHz
Power Gain	35-38.1dB	Tuning Range	24.3-28.2GHz (14.8%)
Noise Figure	5.5-7.4dB	**Pulse Former**	
Input Return Loss	<−14.5dB	On-state insertion loss	<−2.2dB
Output Return Loss	<−15dB	Off-state LO leakage	<−26dB
IF-to-RF isolation	<−45dB	**Power Dissipation**	
LO-to-RF isolation	<−30dB	LNA	8.3mA @1.8V
LO-to-IF isolation	<−23dB	I/Q Mixer + VGA	20mA @1.8V
1-dB compression point	−20.8dBm	QVCO & Buffers	28mA @1.5V
IIP3	−9dBm	Output buffers	21mA @1.8V
Technology	0.18μm RFCMOS	Total	49.3mA @1.8V 28mA @1.5V
Die Size	3mm^2		

Fig. 4.19 Summary of measured performance

results. The front-end achieved a gain of >35 dB and a noise figure <7.5 dB over the entire UWB 22–29-GHz frequency band, while consuming 131 mW. UWB pulse formation has also been demonstrated. The receiver front-end presented in this work has the best performance reported in 0.18 μm CMOS for short-range automotive radar applications.

Chapter 5
A BiCMOS Dual-Band Millimeter-Wave Frequency Synthesizer

Next-generation short- and long-range automotive radar sensors, operating in the millimeter-wave (MMW) spectrum, will almost certainly be manufactured in silicon (Si) or silicon–germanium (SiGe) technologies. SiGe is already a proven technology for automotive radars in the 24-GHz band [2, 8], and recent work has demonstrated its potential for MMW applications as well. Highly-integrated MMW SiGe transmitters and receivers, intended for 77-GHz radar applications as well as the more popular 60-GHz band, have been reported in recent literature [9–16, 21, 22, 51–53]. Performance of SiGe technology for imaging applications in the W band (94 GHz) and the D band (140 GHz) has also been explored [9, 52]. Recently reported SiGe transceivers have achieved record operation frequencies in the vicinity of 170 GHz [52, 53]. With further improvements in transistor performance, it is likely that SiGe will emerge as the technology of choice for beyond-100-GHz applications including passive imaging and short-range communications.

Similar to the trends in cellular and WLAN applications during the last decade, low-cost requirements will necessitate multiband operation with lower component count in future generations of radar sensors. For instance, long- and short-range detection can potentially be combined by integration of 22–29 GHz and 77 GHz radars on a single chip [5, 47]. A paramount challenge for these systems, however, will be the efficient generation of multiple frequencies on a single-chip while maintaining adequate isolation between different frequency bands. In this chapter, the first attempt to design a dual-band frequency source for such systems is described.

Only a few frequency synthesizers have been reported in the MMW spectrum, mostly for the 60-GHz band [54–58] and only two targeting the W band [46–59]. This chapter presents a highly-integrated MMW frequency synthesizer, based on the work first reported in [46, 47]. The design has been implemented in a 0.18 μm SiGe BiCMOS process featuring 200/180-GHz f_T/f_{max} heterojunction bipolar transistors (HBTs) with 0.15^{-1}m emitter-width. All circuits except the

This work was done in collaboration with Babak Javid [45, 46].

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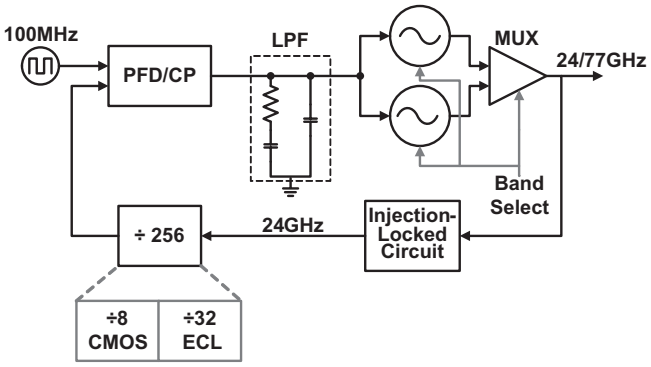


Division Ratio	
77GHz mode	768
24GHz mode	256

Fig. 5.1 Block diagram of the 24/77 GHz dual-band frequency synthesizer

voltage-controlled oscillators (VCOs) are shared between the two radar bands, and a seamless reconfiguration of division ratio is incorporated. All components except the loop filter are integrated on-chip. The synthesizer design is targeted for integration within a dual-band automotive radar direct-conversion transceiver chip as shown in Chap. 5 [5, 47]. It can potentially be utilized in a 94-GHz heterodyne receiver for imaging applications, as described later.

The remainder of this chapter is organized as follows: Section 5.1 discusses the architectural considerations for the dual-band synthesizer. The circuit design and analysis of key building blocks of the synthesizer are described in Sect. 5.2. Measurement results carried out on an experimental synthesizer prototype are presented in Sect. 5.3. Finally, Sect. 5.4 provides concluding remarks.

5.1 Dual-Band Architecture

The block diagram of the proposed dual-band architecture for the MMW frequency synthesizer is shown in Fig. 5.1. It consists of two LC VCOs, a divide-by-three injection-locked circuit (ILC),[1] a divide-by-32 emitter-coupled logic (ECL) frequency divider, a divide-by-8 static CMOS frequency divider, a CMOS phase/

[1] Hereafter, the circuit is referred to as ILC in order to avoid confusion between its two injection-locking modes.

frequency detector (PFD), a CMOS charge pump (CP), and an off-chip low-pass filter (LPF). In the W-band mode, the 77-GHz VCO is enabled and the division ratio is 768. The ILC is injection-locked to the 77-GHz VCO output. In the K-band mode, the 24-GHz VCO is enabled. In this mode, the ILC is locked to the 24-GHz VCO output and thus acts as a tuned buffer, resulting in a division ratio of 256. Although the ILC could be used as a VCO for the K-band mode (with the 77-GHz VCO disabled), the ILC phase noise is inadequate for this purpose. This is because the ILC in this work incorporates a tank with a relatively low quality factor (Q) in order to achieve a wide injection-locking range. The proposed scheme allows the use of the same low phase noise reference input in both operating bands of the synthesizer. The reference frequency of the synthesizer is 92–105 MHz.

A key building block that significantly influences the overall performance of a phase locked loop (PLL) or frequency synthesizer is the frequency divider in the feedback loop. Frequency division presents stringent trade-offs between operating frequency range, power consumption, and phase noise. Static dividers can achieve a broad operating frequency range, but at the cost of high power dissipation and phase noise. On the other hand, injection-locked frequency dividers (ILFDs) can achieve high operation frequency and low phase noise with moderate current consumption, due to their LC tank-based operation. It is not surprising then that an ILFD is often employed as the first divider stage in MMW frequency synthesizers [21, 46, 54, 56–59].

With an input signal of 77 GHz, a divide-by-two ILFD would provide an output frequency of 38 GHz. Although a static divider could be used following the divide-by-two ILFD, an additional ILFD would still be preferred to lower power dissipation and improve the phase noise, thus resulting in two back-to-back divide-by-two ILFDs. On the other hand, a divide-by-three circuit would divide the 77-GHz input down to 26 GHz, a frequency range in which static dividers can provide acceptable performance. Considering that ILFDs can achieve higher (>2) division ratios [54, 60], we determine that a divide-by-three ILFD is thus the optimum topology requiring no additional ILFDs in the divider chain. Moreover, recognizing that the divide-by-three output is in the 26-GHz band, a technique for dual-band operation is readily implemented, as discussed above and further elaborated in Sect. 5.2. It is interesting to note that a divide-by-four ILFD is also feasible [61, 62], but would require a higher input power to achieve the same locking range as a divide-by-three ILFD. In summary, the use of a divide-by-three ILFD enables a simple architecture for dual-band operation while also relaxing the requirements of the MMW divider-chain.

As mentioned earlier, the proposed synthesizer can also be employed in a 94-GHz heterodyne receiver. The 77-GHz VCO output can be used as the first local oscillator (LO) signal for the down-conversion of the 94-GHz input and the quadrature outputs of the divide-by-6 output (i.e., the output of the second divider) can provide the second LO signal. The synthesizer is therefore highly versatile and can serve as a useful building block in several MMW applications.

Next, the circuit design details of the key building blocks of the synthesizer are described.

5.2 Circuit Design

5.2.1 24-GHz and 77-GHz Voltage Controlled Oscillators

Several MMW VCOs have been reported in recent literature [46, 55–59, 61, 63–65]. While some novel topologies have been introduced, cross-coupled and Colpitts oscillators remain the most popular due to their simple design and usually adequate performance. The design of MMW cross-coupled oscillators in SiGe and BiCMOS technologies has been constrained by the relatively low maximum achievable oscillation frequency of a BJT/HBT-based negative-resistance cell. This is due to the high base resistance of bipolar devices. The oscillation frequency limit $f_{LIMIT,CC}$, defined by the point at which the effective negative resistance of the cross-coupled pair becomes positive, is given by [66].

$$f_{LIMIT,\,CC} = f_T \sqrt{\frac{\frac{1}{g_m} + R_E}{R_B + R_E}}, \tag{5.1}$$

where g_m is the device transconductance, and R_B and R_E are the base and emitter physical resistances, respectively. Figure 5.2a shows the simulated equivalent parallel resistance looking into the cross-coupled pair, R_{eq}, for the 0.18 μm BiCMOS technology used in this work, indicating an $f_{LIMIT,CC}$ of about 77 GHz. This restricts the practical operating frequency of cross-coupled oscillators in this technology to less than 60 GHz. Similarly, the maximum achievable oscillation frequency $f_{LIMIT,COLP}$ of a Colpitts oscillator can be expressed as [66].

$$f_{LIMIT,COLP} = \sqrt{\frac{f_T}{2\pi C_2 (R_B + R_E)}}, \tag{5.2}$$

where C_2 is the emitter degeneration capacitance in Fig. 5.2b. Unlike the cross-coupled case, the frequency limit of a Colpitts oscillator depends on the capacitances used to form its tank and is ultimately limited by the parasitic capacitances of the device. As confirmed by the simulation results[2] of Fig. 5.2b, a Colpitts oscillator can achieve higher oscillation frequency (a maximum of 135 GHz in the used technology) than a cross-coupled design. Note that (5.1) and (5.2) are approximate and exact values must be obtained through simulations; nevertheless, these limits provide great deal of insight in designing MMW oscillators. Moreover, $f_{LIMIT,CC}$ can be used to characterize device technologies in addition to the conventional figures-of-merit, f_T and f_{max} [67]. It is also noteworthy that CMOS technologies do

[2] Note that the graphs in Fig. 5.2 represent the highest oscillation frequencies possible for the corresponding topolgies. Device sizes and bias currents were varied to locate the optimum for each topology and ideal passives were used.

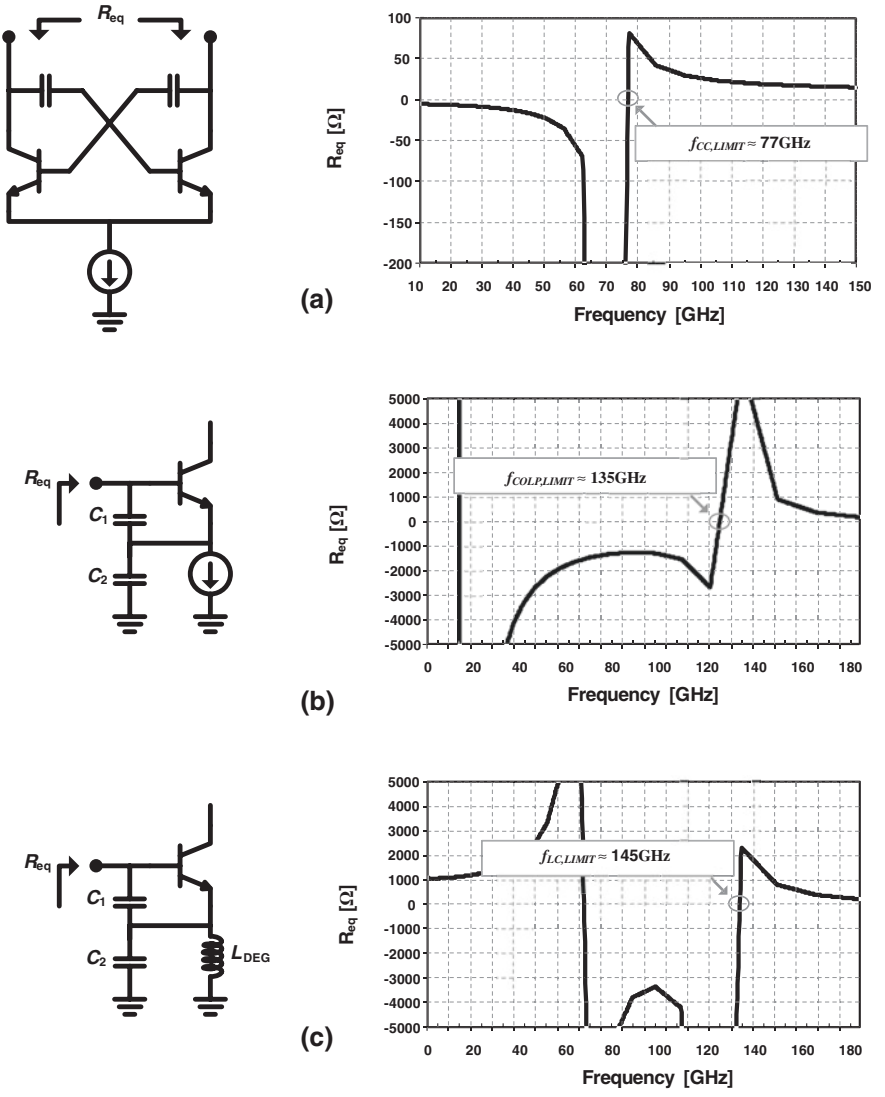
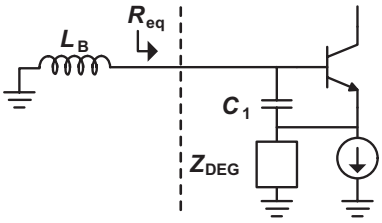


Fig. 5.2 Comparison of frequency capabilities of different oscillator topologies: **a** cross-coupled, **b** Colpitts, and **c** Colpitts with inductive degeneration. f_{LIMIT} indicates the frequency at which the equivalent parallel resistance of the active core turns positive, thereby preventing oscillation start-up

not suffer from a low $f_{LIMIT,CC}$ because gate resistance of MOSFETs can be minimized by optimizing the multi-finger layout of the transistor [68]. Consequently, the choice of topology for CMOS oscillators is governed by other performance parameters rather than the maximum achievable oscillation frequency. For



Z_{DEG}	$=\frac{1}{j\omega C_{DEG}}$	$=j\omega L_{DEG}$	$=j\omega L_{DEG}\left\|\frac{1}{j\omega C_{DEG}}\right.$
ω_o	$=\frac{1}{\sqrt{L_B\left(C_1\left\|C_{DEG}\right.\right)}}$	No oscillation*	$>\frac{1}{\sqrt{L_{DEG}C_{DEG}}}$

*Assuming there is no capacitance from emitter to ground other than Z_{DEG}.

Fig. 5.3 Colpitts topology with an arbitrary emitter degeneration impedance. The table shows the oscillation frequency of the circuit as the degeneration impedance is varied

instance, a Colpitts oscillator may still be preferred over a cross-coupled topology due to its better phase noise performance and higher tuning range, even though it may have a lower f_{LIMIT} in CMOS, as demonstrated in [69].

Due to the aforementioned reasons, the 77-GHz VCO design in this work is based on a modified differential Colpitts oscillator topology shown in Fig. 5.2c [65, 69]. Compared to a Colpitts topology, the design employs additional inductance for emitter degeneration. A simplified model for analysis is shown in Fig. 5.3, where Z_{DEG} is arbitrary degeneration impedance. The base inductance L_B is also included to complete the tank circuit. If Z_{DEG} is purely capacitive, the topology reduces to a simple Colpitts oscillator, whereas if Z_{DEG} is purely inductive, the circuit fails to oscillate. Furthermore, if Z_{DEG} is a parallel LC network, the effective impedance can be inductive, capacitive or resistive, depending on whether the operating frequency is lower than, higher than or equal to the LC resonant frequency $\omega_{DEG} = 1/\sqrt{L_{DEG}C_2}$, respectively. It is readily inferred that ω_{DEG} is the lower limit of the oscillation frequency for the topology of Fig. 5.2c, because the degeneration impedance below this frequency becomes inductive. Since the oscillation frequency must be above ω_{DEG}, the degeneration impedance is capacitive and an effective capacitance can be defined as.

$$C_{2,eff}(\omega) = C_2\left[1 - \left(\frac{\omega_{DEG}}{\omega}\right)^2\right] \tag{5.3}$$

From (5.3), it is observed that a higher oscillation frequency can be achieved with this topology, as also predicted by the simulation results in Fig. 5.2c. Although this simplistic picture is complicated by the presence of non-idealities such as finite quality factors of the degeneration inductance and capacitance (formed partly by lossy varactors), simulations indicate that higher oscillation frequencies can indeed

be achieved by optimizing the degeneration impedance. The oscillation frequency, f_{LC}, for this topology can be expressed approximately as [69].

$$f_{LC} = \frac{1}{2\pi} \cdot \sqrt{\frac{(C_1' + C_\mu)L_B + (C_1' + C_2)L_{DEG} + \sqrt{\left[(C_1' + C_\mu)L_B + (C_1' + C_2)L_{DEG}\right]^2 - 4(C_1' + C_\mu)C_2 L_B L_{DEG}}}{2(C_1' + C_\mu)C_2 L_B L_{DEG}}}, \tag{5.4}$$

where $C_1' = C_1 + C_\pi/(1 + g_m R_E)$, C_π is the base-to-emitter capacitance, and C_1 is the base-to-collector capacitance. Due to the complicated dependence of f_{LC} on circuit components in (5.4), simulations are necessary to estimate the maximum achievable f_{LC}. As indicated in Fig. 5.2c, this frequency limit, $f_{LIMIT,LC}$, is in the neighborhood of 145 GHz for the technology used in this work.

Since phase noise is one of the most critical specifications to meet in MMW systems, it is important to study the effect of LC emitter degeneration on the phase noise of the Colpitts oscillator. The phase noise of a conventional Colpitts oscillator, based on Leeson's model [70], is given by [71].

$$S_{\Delta\phi out,\, COLP} = \frac{1}{2}\frac{\left\langle \overline{I_n^2} \right\rangle}{V_O^2} \cdot \frac{C_2^2}{C_1'^2 (C_1' + C_2)^2} \cdot \frac{1}{\Delta\omega^2}, \tag{5.5}$$

where $S_{\Delta\Phi out;COLP}$ denotes the phase noise spectral density, $\left\langle \overline{I_n^2} \right\rangle$ is the average input white noise power of the transistor, V_O is the tank swing, and $\Delta\omega$ is the offset from the carrier angular frequency. It is shown in Appendix A that for a Colpitts oscillator with capacitive degeneration given by $C_{2,eff}$ in (5.3), the phase noise is expressed as.

$$S_{\Delta\phi out,\, LC} = \frac{1}{2}\frac{\left\langle \overline{I_n^2} \right\rangle}{V_{O,\, LC}^2} \cdot \frac{C_2^2}{C_1'^2 \left[\left(\frac{1+k}{1-k}\right) C_1' + C_2\right]^2} \cdot \frac{1}{\Delta\omega^2}, \tag{5.6}$$

where k is given by

$$k = \left(\frac{\omega_{DEG}}{\omega_{LC}}\right)^2, \tag{5.7}$$

and ω_{LC} is the oscillation frequency of the emitter-degenerated oscillator. Since $k < 1$, as discussed earlier, and $V_{O;\, LC} > V_O$ (Appendix A), the denominator in (5.6) is always larger than that in (5.5). Therefore, it can be inferred from (5.5–5.7) that LC degeneration improves the phase noise of the Colpitts oscillator.

Since Leeson's model does not account for the time-variant nature of the device-noise-to-phase-noise conversion, a linear time-variant (LTV) model based on impulse sensitivity function (ISF) [72–74] is now used to examine the phase noise of the oscillator topologies (see Appendix A for details). The phase noise of

the conventional Colpitts oscillator, taking only collector shot noise and tank noise into account, is

$$S_{\Delta\phi out,\, COLP} = \frac{k_B T}{4V_O^2} \cdot \frac{1}{R_T C_2^2} \cdot \frac{2 - n_{COLP}}{n_{COLP}^2 (1 - n_{COLP})} \cdot \frac{1}{\Delta\omega^2}, \tag{5.8}$$

where k_B is the Boltzmann's constant, R_T is the equivalent parallel tank resistance, and n_{COLP} is given by

$$n_{COLP} = \frac{C_1'}{C_1' + C_2}. \tag{5.9}$$

The LC emitter-degenerated Colpitts oscillator exhibits a lower phase noise (as shown in Appendix A) expressed as

$$S_{\Delta\phi out,\, LC} = \frac{k_B T}{4V_{O,\, LC}^2} \cdot \frac{1}{R_T C_2^2} \cdot \frac{2 - n_{LC}}{n_{LC}^2 (1 - n_{LC})} \cdot \frac{1}{(1 - k)^2} \cdot \frac{1}{\Delta\omega^2}, \tag{5.10}$$

where

$$n_{LC} = \frac{C_1'}{C_1' + C_{2,\, eff}\,(\omega_{LC})} = \frac{C_1'}{C_1' + (1 - k)\, C_2}. \tag{5.11}$$

Intuitively, the loaded quality factor of the tank is increased, because the frequency-dependent capacitance $C_{2,\, eff}$ results in a steeper phase transition at the oscillation frequency [65]. The faster transition manifests itself into a direct improvement of the phase noise of the oscillator. It is noteworthy here that if Z_{DEG} is a parallel LC network, the tank in Fig. 5.3 is readily identified as a fourth-order network. Recent work corroborates the potential of higher-order networks in achieving high oscillation frequencies [58, 59, 64, 69, 75].

The circuit schematic of the 77-GHz VCO is shown in Fig. 5.4. Microstrip transmission lines T_1 and T_2 are used at the HBT base terminals to realize small tank inductance (≈25 pH) with a high Q (≈20). A center-tapped spiral inductor with 150-pH half-inductance is used to realize the emitter degeneration. As discussed above, the emitter degeneration also improves the tuning range of the oscillator because the fixed portion of the effective tank capacitance is reduced. Tail current sources consisting of active devices are replaced by resistive biasing in order to avoid additional noise contributions. Moreover, LC emitter-degeneration helps in filtering the noise from the bias resistors. Metal–insulator-metal (MIM) capacitors C_1 and C_3 (150 fF) are employed to implement the additional base-to-emitter capacitances. The linear MIM capacitors reduce the effect of the voltage non-linearity of the base-to-emitter device capacitances on the VCO phase noise. At 77 GHz, the Q of 0.18 μm MOS varactors is too low to sustain oscillations with sufficient margin. Therefore, frequency tuning is achieved by using HBT varactors Q_3 and Q_4 (10×3 ^{1}m) with variable base-to-collector junction capacitance

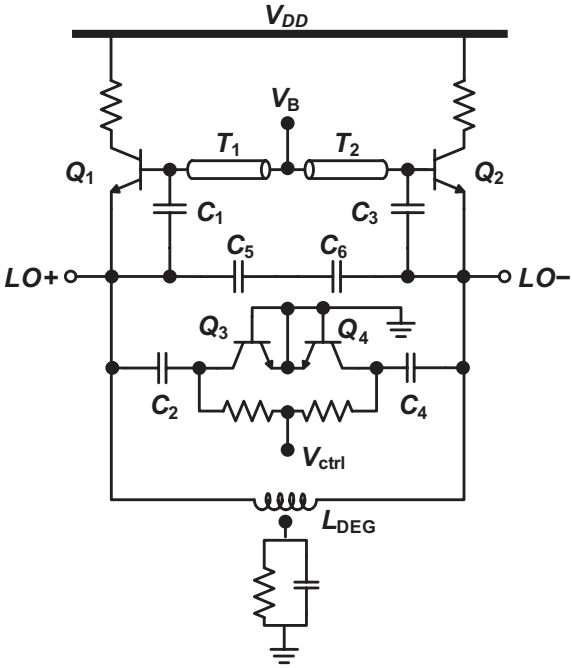


Fig. 5.4 Schematic of the 77-GHz differential Colpitts VCO with LC emitter-degeneration

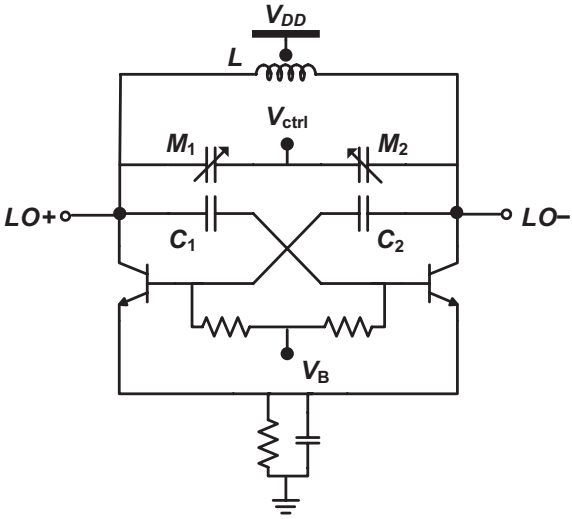


Fig. 5.5 24-GHz cross-coupled VCO schematic

of 85 fF to 110 fF ($C_{max}/C_{min} \approx 1.3$). The simulated Q of the HBT varactors is 10 at 77 GHz. The varactors are connected to the VCO tank through dc-blocking MIM capacitors C_2 and C_4 (0.5 pF), which operate beyond their self-resonant frequencies. Differential operation is achieved by connecting two MIM capacitors C_5 and C_6 (55 fF) across the emitters of the two HBTs, Q_1 and Q_2 (4 × 5.5 μm).

The VCO has been designed for a center frequency of 78 GHz with a simulated tuning range of 4 GHz to compensate for process variations and modeling errors. The VCO circuit draws 10 mA from a 2.5 V supply.

At 24 GHz, a cross-coupled oscillator can be employed, as the operating frequency is sufficiently lower than $f_{LIMIT,CC}$, and the topology achieves acceptable phase noise. An additional advantage is that a cross-coupled pair LC oscillator requires smaller loop gain than a Colpitts oscillator in order to start oscillating. Therefore, the cross-coupled topology results in lower power dissipation for the 24-GHz VCO. The schematic of the differential LC oscillator used for the 24-GHz VCO is shown in Fig. 5.5. The center-tapped inductor L (200 pH) and accumulation-mode MOS varactors M_1 and M_2 form the VCO tank. The varactor capacitance can be varied from 175 fF to 275 fF ($C_{max}/C_{min} \approx 1.6$). MIM capacitors C_1 and C_2 (0.75 pF) are employed to prevent forward biasing the base-to-collector p-n junction. Similar to the 77-GHz VCO, resistive biasing is used instead of an active tail current source to avoid phase noise degradation. The simulated tuning range of the VCO is from 24 GHz to 28.5 GHz. The 24-GHz VCO requires a bias current of 4 mA.

Each of the two VCOs is followed by two emitter-follower buffer stages, to provide sufficient isolation from the output load. The two VCO signals are then multiplexed together via an open-collector differential amplifier stage. The open-collector outputs of the 24-GHz and 77-GHz differential buffer chains are tied together and then connected to the load resistors. A digital control signal is used to switch between the two bands by turning on or off the NMOS tail current sources in the two differential pairs. At the same time, the unused VCO is disabled to avoid any leakage into the other band and to reduce power dissipation.

5.2.2 Dual-Mode Injection-Locked Frequency Divider

As discussed in Sect. 5.1, harmonic injection-locked frequency dividers are attractive at MMW frequencies as they have lower power consumption and lower phase noise than static frequency dividers. Intuitively, ILFDs have lower power consumption as there is little energy loss in the tank in each oscillation cycle, whereas more energy is required to charge and discharge the device capacitances in static dividers. This is also analogous to the difference between ring oscillators and LC oscillators, where LC oscillators can achieve higher operation frequency and lower phase noise. These improvements in the LC-tank-based injection-locked circuits are achieved at the expense of the operating frequency range of the circuit. Consequently, ILFDs suffer from a smaller locking range than that of static dividers.

In this work, an injection-locked circuit is employed to seamlessly reconfigure the division ratio between the two bands of the frequency synthesizer. The output of the ILC consists of a tank tuned in the 24-GHz band. When the input frequency is either 77 GHz or 24 GHz, the ILC output is phase-locked to the input signal. In other words, the circuit implements two functions: (i) frequency-division by three for a 77-GHz input and, (ii) tuned buffer for a 24-GHz input. Note that the ILC cannot lock to a 48-GHz input (second harmonic of 24 GHz), as discussed later in this section.

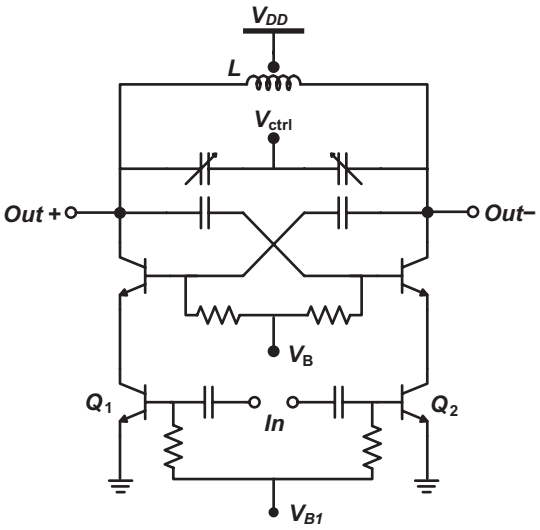


Fig. 5.6 Schematic of the dual-mode injection-locked circuit. The table lists the functions realized by the circuit in different operating modes

Modes of Operation		
Mode 0	No Input	Free-running 24GHz VCO
Mode I	77GHz input	Injection-locked divide-by-three
Mode II	24GHz input	Injection-locked 24GHz oscillator (tuned buffer)

Few injection-locked divide-by-three circuits operating in the MMW spectrum have been reported in the past [54, 76, 77]. In this work, a cascode HBT-based injection-locked LC oscillator circuit, based on the work reported in [54] and [60], has been designed to realize a division ratio of three. As mentioned before, a key feature of our design is its additional capability to act as an injection-locked oscillator for the fundamental frequency input. The ILC schematic is shown in Fig. 5.6. The circuit resembles a conventional cross-coupled LC VCO except that the tail current source has been replaced by an input pseudo-differential pair consisting of two common-emitter HBT amplifiers Q_1 and Q_2. The stand-alone ILC has three modes of operation as described next. However, during proper functioning of the dual-band synthesizer, only Modes I and II are apparent. Nevertheless, the third mode is critical for startup of the oscillations; we call it Mode 0.

5.2.2.1 Mode 0: Free-Running Operation

If no signal is applied at the input of the ILC, the circuit operates as a free-running oscillator at 24 GHz. Although it may seem that the circuit will fail to oscillate due to the emitter degeneration of the cross-coupled pair by the large output resistance

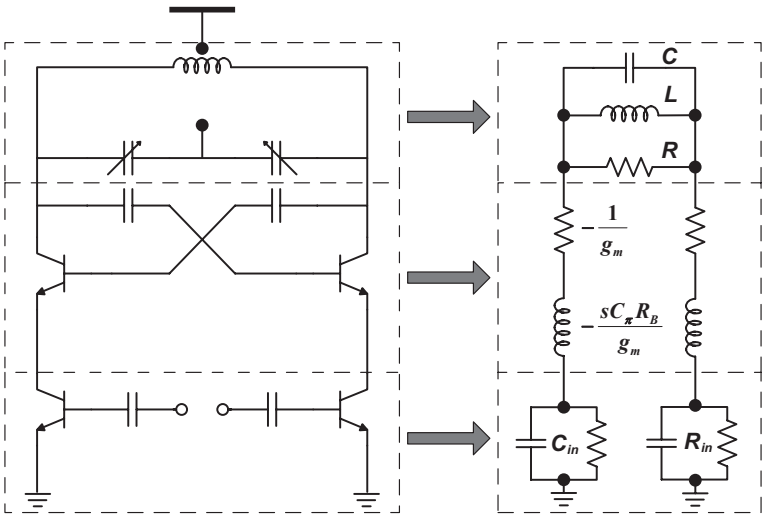


Fig. 5.7 Equivalent circuit of the ILC in the free-running mode

of the HBT current sources, a closer examination proves otherwise. A simplified equivalent circuit of the free-running ILC is shown in Fig. 5.7. The circuit is essentially a cross-coupled LC VCO with capacitive emitter degeneration. The capacitive degeneration, in fact, results in lower power consumption because it reduces the required negative resistance of the active cross-coupled pair [78]. The minimum required transconductances for oscillation in the absence and presence of capacitive degeneration are given by

$$g_m = \frac{1 + (\omega C_\pi R_B)^2}{R}, \tag{5.12}$$

and the quadratic equation,

$$g_m = \frac{1 + \left(\omega C_\pi R_B - \frac{g_m}{\omega C_E}\right)^2}{R}, \tag{5.13}$$

respectively [78], validating the lower required power dissipation of the emitter-degenerated VCO.

5.2.2.2 Mode I: Injection-Locked Oscillator

If a differential 24-GHz signal is applied at the ILC input, the output locks to the input frequency, and the circuit essentially operates as a tuned buffer. The LC tank provides the additional phase shift required to shift the output frequency from the

free-running oscillation frequency. The two-sided locking range ω_L of the ILC in this mode is given by [79]

$$\omega_L = \frac{\omega_o}{Q} \cdot \frac{K_I}{\sqrt{1 - K_I^2}}, \tag{5.14}$$

where ω_o is the free-running tank frequency, Q is the tank quality factor, and $K_I = I_{inj}/I_{dc} < 1$ is the injection strength. Injection-locked circuits typically suffer from a limited locking range. From (5.14), it is observed that the locking range can be enhanced by increasing the injected signal power and by reducing the tank Q.

5.2.2.3 Mode II: Injection-Locked Divide-by-Three

In this mode, a 77-GHz differential signal is injected into the ILC input. This injection signal modulates the free-running state of the LC tank. Due to the non-linearity of the active cross-coupled pair, several intermodulation products result from the multiplication of the input signal and the tank oscillation. It is important to note that the virtual ground of the differential pair in a conventional LC oscillator is non-existent in the ILC described here. Therefore, the even harmonics generated by the cross-coupled pair are not suppressed, enabling the divide-by-three operation (Appendix B). For a sufficiently large input signal, the ILC output is locked to the intermodulation product at one-third of the input frequency. As shown in Appendix B, the upper bound on the locking range of the divide-by-three ILC can be expressed as

$$\omega_L \approx \frac{\omega_o}{Q} \cdot \frac{K_I \alpha_2}{\alpha_1}, \tag{5.15}$$

where $®_1$ and $®_2$ denote the small-signal conversion gain and the second-order non-linearity, respectively, of the equivalent mixer formed by the cross-coupled pair. It is noteworthy here that the ratio $®_1/®_2$ is defined as the second-order intercept point (IP_2) of a circuit [80] and (11) can be recast as

$$\omega_L \approx \frac{\omega_o}{Q} \cdot \frac{K_I}{IP_{2,\ cross-coupled}}. \tag{5.16}$$

It is readily inferred from (5.16) that lowering the IP_2 (i.e., higher even-order circuit non-linearity) of the cross-coupled pair will improve the locking range of the divider.

As indicated by (5.14) and (5.15), the ILC has a smaller locking range in the divider mode than that in Mode I because α_2/α_1 is typically less than unity. To compensate for this and the lower gain at 77 GHz, higher current is drawn by the ILC in this mode. Alternatively, the current consumption in Mode I can be decreased to obtain the same locking range as that in Mode II. Since the ILC

locking range around its free-running frequency is small, varactors are used to tune the center frequency of the ILC. This necessitates the implementation of a calibration technique to align the center frequency of the ILC to that of the VCO, so that the PLL can lock to the correct frequency (Sect. 5.3).

One may wonder if the ILC, operating in Mode I, would lock to the inevitable second harmonic of the 24-GHz input. Fortunately, the underlying differential operation of the cross-coupled pair precludes locking to the second harmonic of the input. The even harmonics of the input produce in-phase signals at the ILC output, as discussed in [81].

In accordance with the foregoing discussion, the tank Q, the varactor C_{max}/C_{min} ratio ($\approx$1.4), and the input differential amplifier gain have all been optimized in order to maximize the locking range and the free-running tuning range of the ILC. The tank inductance (200 pH) has a Q of 9 at 25 GHz and MOS varactors (9×3 µm$\times$ 0.5 µm) have been used to provide a tuning range from 24.5 GHz to 28.3 GHz. The varactor finger length and width were optimized for a wide tuning range, at the expense of a little degradation in Q. The ILC consumes 6 mA from a 2.5-V supply in Mode II. In Mode I, the ILC can successfully lock to the input signal with a bias current as low as 2 mA.

5.2.3 Divider Chain, PFD/CP and Loop Filter

It is clear from above that the output of the ILC is always in the 24-GHz band. Static dividers can be used at these frequencies with reasonable power dissipation. In fact, static dividers are the more suitable choice because LC-tank-based injection-locked dividers would be costly in terms of die area. A chain of five static emitter-coupled logic (ECL) dividers follows the ILC and consumes only 15 mW from a 2.5-V supply. Three static flip-flop-based CMOS dividers further divide the signal frequency down to the reference frequency of the synthesizer. The ECL divider chain is optimized for low power consumption and the voltage swing of the signal is gradually increased through the cascaded ECL dividers by scaling up the load resistors in the latches. The output of the last ECL divider provides a differential peak-to-peak swing of 1.5 V, which is sufficiently large to completely switch the following CMOS divider. This, in turn, efficiently eliminates the need for an ECL-to-CMOS converter prior to the CMOS divider chain. The output of the entire divider chain provides a rail-to-rail signal at the input of the PFD, which is implemented as a standard tri-state topology.

The schematic of the charge pump circuit, inspired by the topology in [82], is shown in Fig. 5.8. Cascode current sources reduce the effect of the VCO control voltage variation on the charge pump UP/DOWN currents until V_{ctrl} comes within $2V_{dsat}$ of the supply rails, which in turn broadens the linearity of the PLL loop. Moreover, it reduces the UP/DOWN current mismatch. The use of a dummy branch to steer the charge pump current for the duration when V_{ctrl} is not integrating any charge, in addition to the charge-injection and clock feed-through

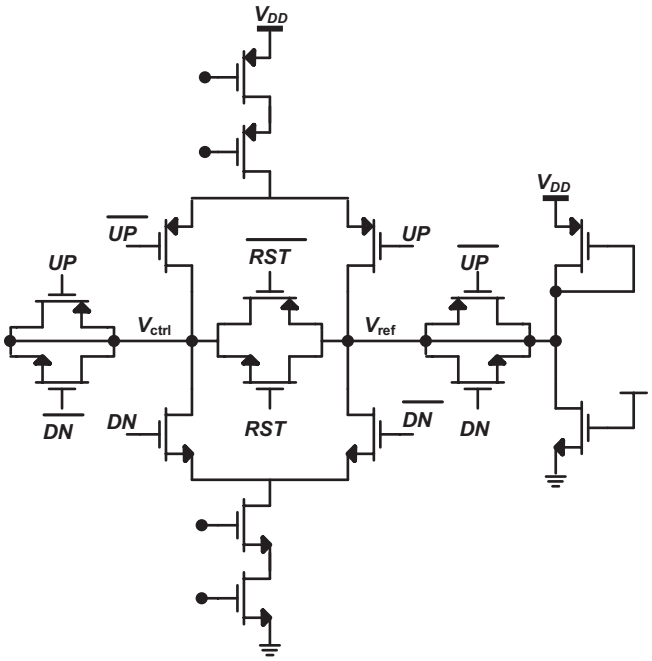


Fig. 5.8 Simplified schematic of the charge pump circuit

cancellation provided by the dummy switches, significantly reduces the non-idealities of the charge pump circuit.

The loop filter is placed off-chip to compensate for modeling errors in the MMW circuits. A Spectre-RF/Verilog-A co-simulation methodology is adopted for closed-loop simulations of the frequency synthesizer. The PLL loop has been optimized for a target bandwidth of 1 MHz.

5.3 Experimental Results

The dual-band frequency synthesizer has been fabricated in a 0.18-¹m 200/180-GHz f_T/f_{max} SiGe BiCMOS process with six metal layers. The emitter width of the HBTs in the technology is 0.15 ^{1}m. The micrograph of the 1-mm $\times$ 0.8-mm chip is shown in Fig. 5.9. The fabricated prototype also consists of a high-speed digital baseband circuit, reported elsewhere [5, 47], which occupies the top half of the die. The frequency synthesizer itself requires a chip area of about 0.4 mm^2 only.

The 2.8 μm-thick top metal is used to realize inductors and transmission lines in the VCOs and the ILC. Stray coupling to the ILC tank can subdue the injection-locking phenomenon resulting in an erroneous output frequency or undesired

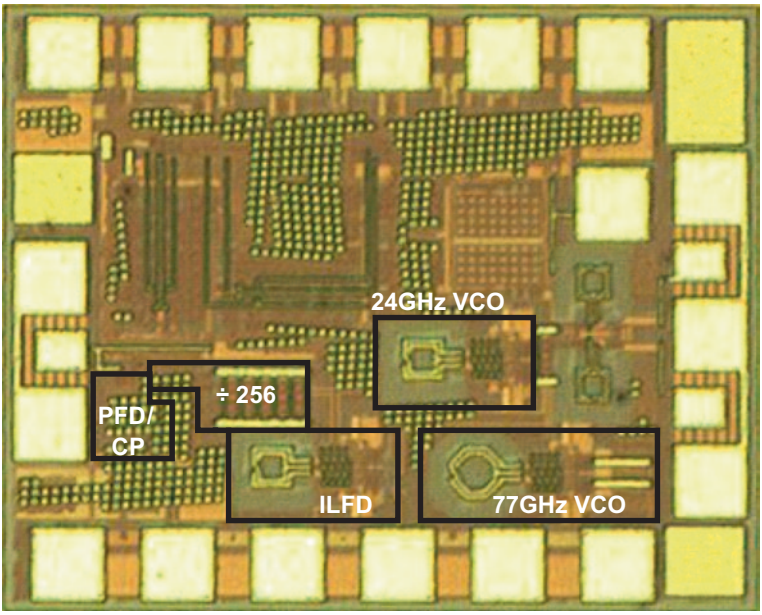


Fig. 5.9 Die micrograph of the $1 \times 0.8\text{-mm}^2$ dual-band synthesizer prototype

sidebands, and can even throw the circuit out of lock [79]. Therefore, signal distribution and routing between building blocks have been accomplished carefully using the 1.6^{-1}m-thick penultimate metal layer to minimize coupling to the oscillator tanks in the top-metal layer. Since transmission lines can provide excellent isolation between adjacent circuits, their use should be considered when integrating injection-locked circuits in a complex system such as a transceiver. In this work and in [5, 47], we have demonstrated the functionality of the ILC in a synthesizer and a transceiver environment, respectively. All passives, including MIM capacitors and interconnects, used in the synthesizer have been designed or characterized using planar 3-D electromagnetic simulations [50].

The synthesizer chip is attached to a PCB using a chip-on-board assembly. All DC pads are wirebonded to the PCB. The reference frequency input is provided by an on-board 50–125-MHz voltage controlled crystal oscillator (VCXO). With the PCB mounted on a probe station, the synthesizer performance is characterized by on-wafer measurements. The 24-GHz mode is measured using a simple coaxial setup. A WR-10 waveguide-based setup is used for the 77-GHz mode, including an Agilent 11970 W harmonic mixer. A simplified version of the setup is shown in Fig. 5.10. In order to avoid any noise pick-up, the control voltage is isolated from on-chip bias lines and the substrate using RF shielding techniques. The length of the wirebond from the V_{ctrl} pad to the PCB was minimized and the control voltage wiring on the PCB was isolated from other on-board interconnects.

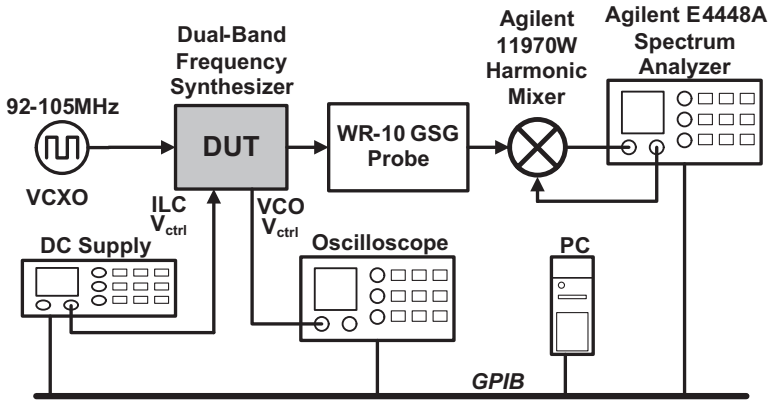


Fig. 5.10 Waveguide-based measurement setup for the synthesizer in the W-band mode. The basic setup for frequency calibration of the ILC is also shown

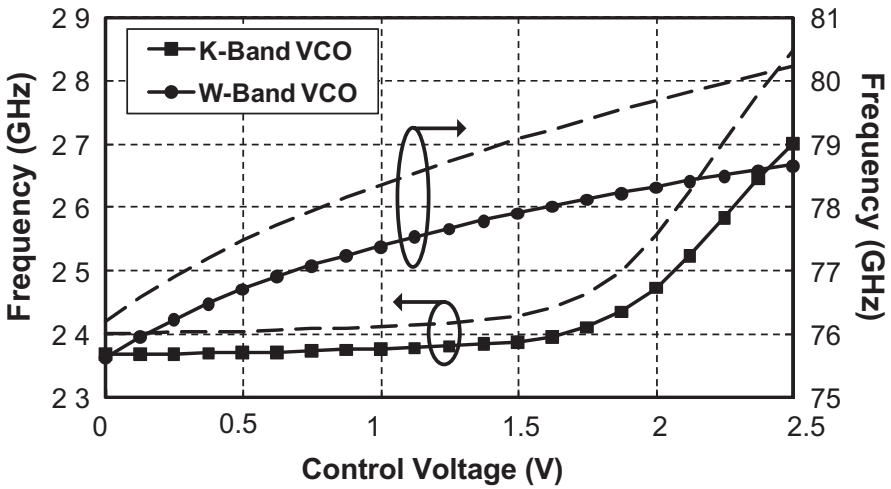


Fig. 5.11 Measured (*solid lines*) and simulated (*dashed lines*) tuning curves of the free-running 24-GHz and 77-GHz VCOs

To measure the free-running performance of the VCOs, the divider chain is disabled. As depicted in Fig. 5.11, the K-band VCO achieves a tuning range from 23.68 GHz to 27 GHz while the W-band VCO can be tuned from 75.6 GHz to 78.6 GHz. The K_{VCO} for the 24-GHz and 77-GHz VCOs are 3.9 GHz/V and 1 GHz/V, respectively, in the linear portion of the tuning curve. The error between the simulated and measured oscillation frequencies is less than 2 % for the 77-GHz oscillator and is slightly higher than 5 % for the 24-GHz oscillator. The higher error for the 24-GHz VCO is attributed to the presence of a thin but

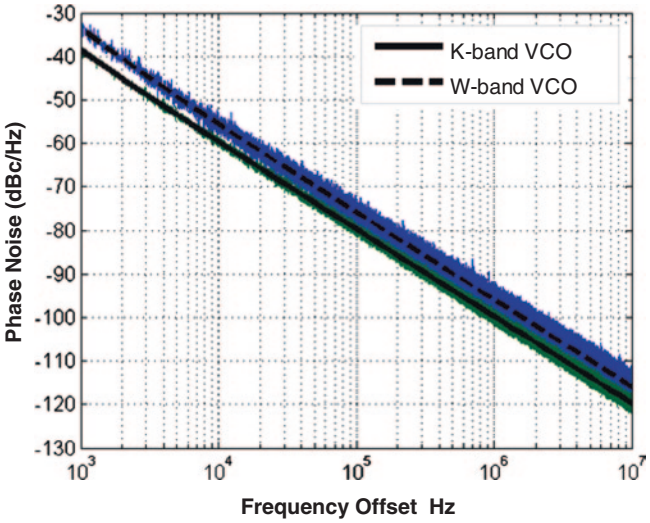


Fig. 5.12 Measured phase noise of the free-running VCOs

highly conductive diffusion layer on top of the silicon substrate, which resulted in an inaccurately modeled ground return path for the spiral inductor in the tank. The 77-GHz VCO is unaffected because the base inductance is implemented as a microstrip line, which is shielded from the substrate by a bottom-metal ground shield. The discrepancy for the 24-GHz VCO has been addressed in a newer version of the synthesizer, integrated within an MMW transceiver [5, 47]. The free-running VCOs achieve a phase noise better than 95 dBc/Hz at 1-MHz offset from the carrier, as shown in Fig. 5.12.

The performance of the divide-by-three ILC is measured with the on-chip W-band VCO as the injection-locking signal source. Figure 5.13 shows the measured and simulated divider tuning range. The simulated tuning range extends from 70.1 GHz to 82.3 GHz. The measured tuning range is 75.6–78.6 GHz, which is limited by the VCO tuning range. Since a circuit breakout of the ILC was unavailable, the divider locking performance could not be verified outside this range. Nevertheless, fairly good model-to-hardware correlation is obtained within the measured tuning range, validating the divider functionality adequately. The simulated locking range is also shown in Fig. 5.13, as a function of the divider control voltage, and varies from 1.8–2.7 GHz across the divider tuning range. The input power in the simulation results of Fig. 5.13 is set to 5dBm, which is the designed power level at the input of the divider. The simulated sensitivity curves of the divider are shown in Fig. 5.14. With a higher input power, the divider achieves a locking range as high as 6.95 GHz which, combined with the tuning capability, results in a wide input frequency range from 68.7–85 GHz. The simulated suppression of the second harmonic of the divider output frequency is more than

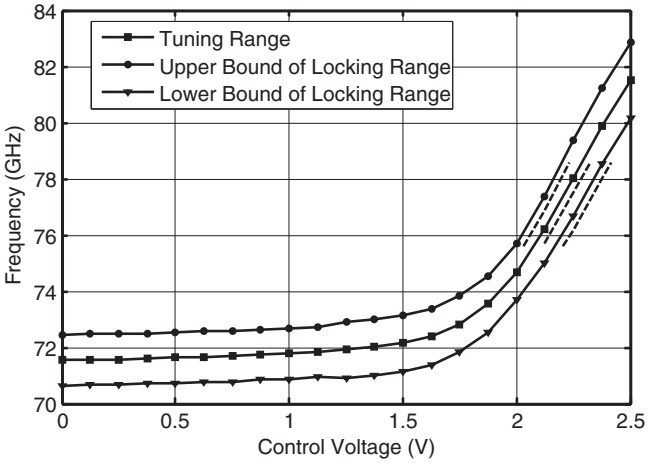


Fig. 5.13 Measured (*dashed lines*) and simulated (*solid lines*) tuning and locking ranges of the ILC in divide-by-three mode (mode II). The measured divider tuning range is limited by the tuning range of the on-chip 77-GHz VCO

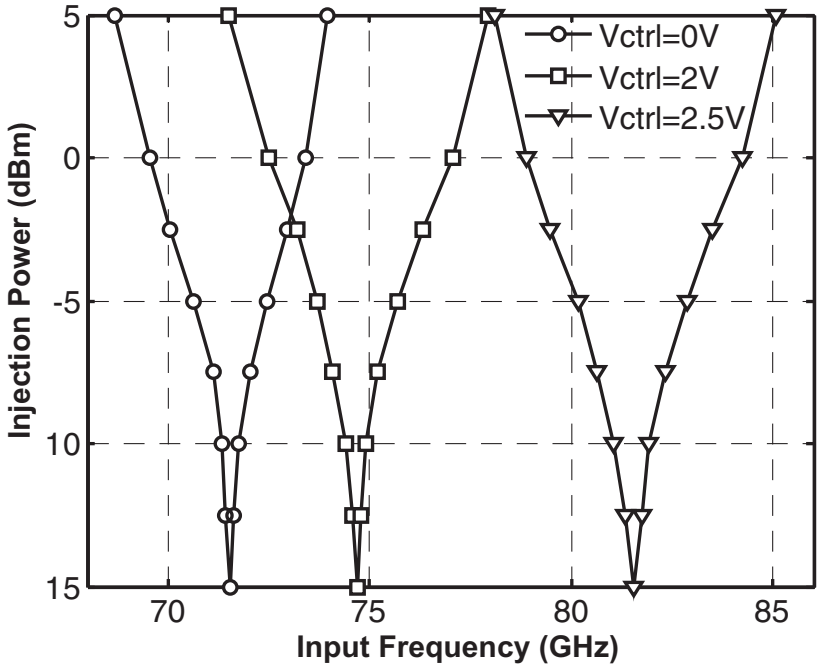


Fig. 5.14 Simulated input sensitivity of the divide-by-three injection-locked circuit at different V_{ctrl} settings

	Technology (μm)	Frequency (GHz)	Locking Range (GHz)	P_D (mW)	Chip Size (mm^2)
[54]	0.15 GaAs pHEMT	60.9	2.3	7	-
[76]	0.13 CMOS	66	6.3/1.5	2/16	0.328
[77]	0.13 CMOS	60	1.8	13	0.683
This Work	0.18 BiCMOS	75.6-78.6 (meas.)[a] 70.1-82.3 (sim.)	1.8-2.7	15	0.04

[a] The measured tuning range is limited by the on-chip VCO, which drives the divider.

Fig. 5.15 Comparison of state-of-the-art millimeter-wave divide-by-three circuits

33 dB below the fundamental. Figure 5.15 compares the performance of the divide-by-three ILC with prior art.

In frequency synthesizers that consist of an injection-locked divider within the PLL loop, a critical requirement for the loop to lock is that either (i) the divider locking range captures the VCO tuning range completely or, (ii) a mechanism is provided to tune the divider center frequency to within the VCO tuning range. Prior art in the MMW domain includes driving the VCO and the injection-locked divider by the same control voltage [56], and off-chip calibration of the divider control voltage [61]. Recently, on-chip digital calibration of the divider has also been reported [57]. In this work, a software-based calibration using MATLAB and GPIB control has been employed to tune the ILC control voltage until the loop is locked. As shown in the measurement setup of Fig. 5.10, the VCO control voltage is monitored on an oscilloscope and a lock condition is detected when it settles to a constant voltage. Note that an on-chip calibration can be readily implemented in a revised version.

In the locked state, the measured output spectrum of the synthesizer in the two bands is shown in Fig. 5.16. In each mode, the reference spurs at the output are 47–50 dB below the carrier power level. The locking range of the synthesizer in the K band is from 23.8 GHz to 26.95 GHz and in the W band is from 75.67 GHz to 78.5 GHz. The synthesizer output delivers an output power of 9.5 dBm at 25.6 GHz and 17.8 dBm at 76.8 GHz after de-embedding the losses of the waveguide probe, harmonic mixer, cables and other components of the measurement fixture.

The closed-loop phase noise performance of the synthesizer is depicted in Fig. 5.17. Phase noise of the reference input is also plotted in the same figure. At 100-kHz, 1-MHz, and 10-MHz offsets from the carrier, the locked 24-GHz VCO output shows a phase noise of 112, 114, and 117 dBc/Hz, respectively. The corresponding phase noise of the locked 77-GHz VCO output is 102 dBc/Hz, 103.5 dBc/Hz, and 116 dBc/Hz, respectively. Jumps in the phase noise plots of

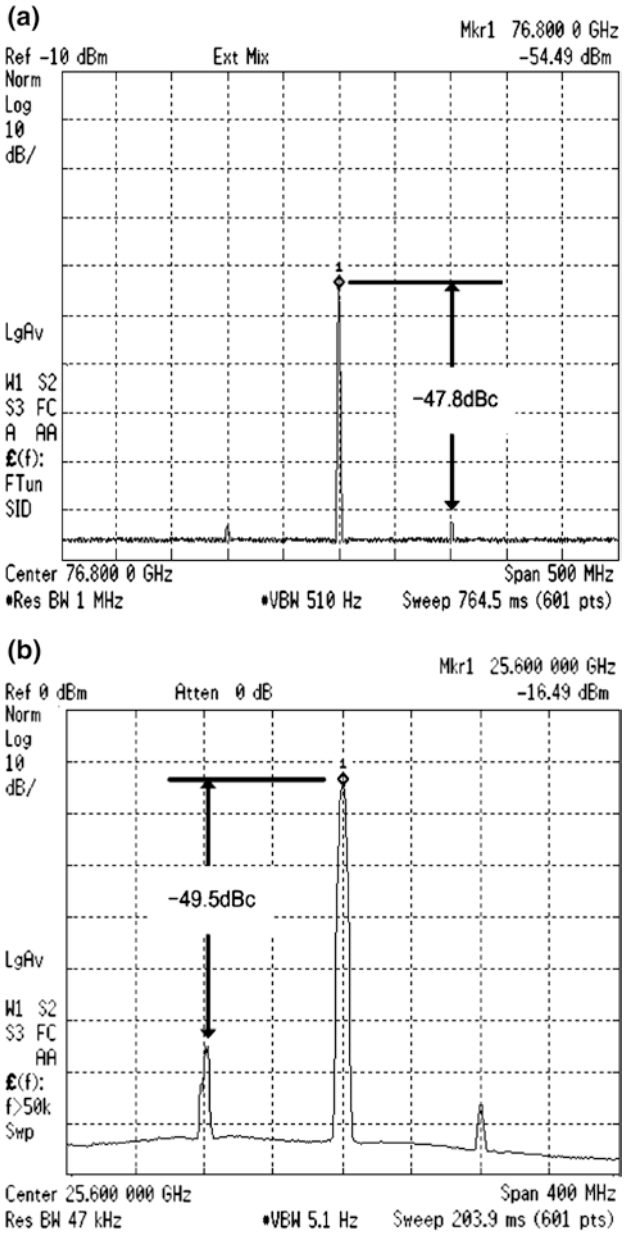


Fig. 5.16 Measured output spectrum of the synthesizer in **a** the W-band mode and **b** the K-band mode. Measurement setup losses have not been de-embedded

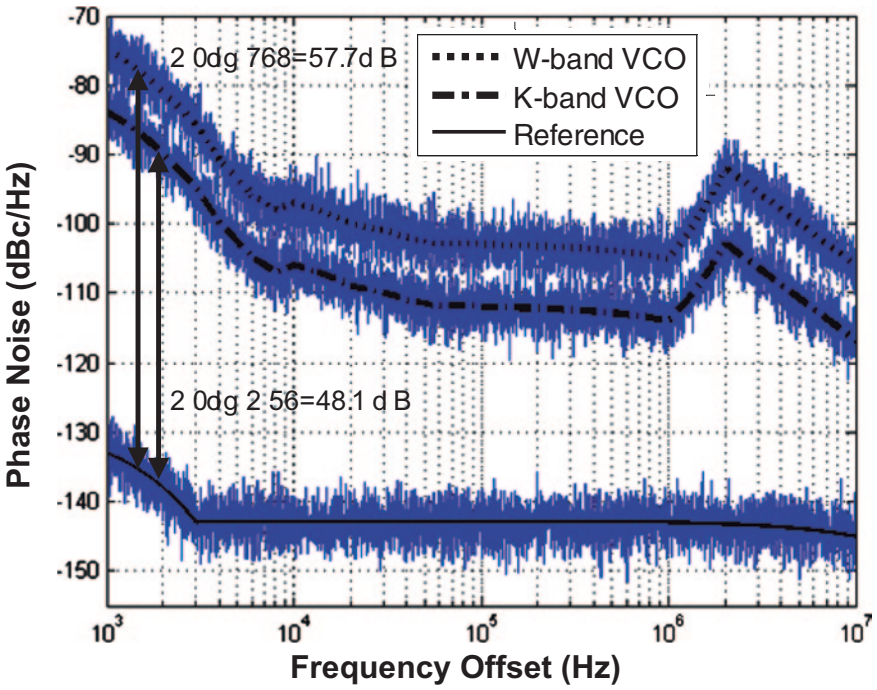


Fig. 5.17 Measured closed-loop phase noise of the synthesizer in the two bands. Reference phase noise is limited by noise floor of spectrum analyzer

Fig. 5.17 are observed at frequency offsets slightly greater than the loop bandwidth. This behavior occurs because the PLL output phase noise is no longer suppressed by the closed-loop dynamics. Also note that the synthesizer phase noise is not flat at frequency offsets less than 10 kHz, unlike the typical PLL characteristics reported in literature. This is because the synthesizer output follows the phase noise of the high-quality (i.e., low phase noise) voltage-controlled crystal oscillator used to provide the reference signal, which exhibits similar phase noise behavior as shown in Fig. 5.17. The reference phase noise shown in Fig. 5.17 is limited by the measurement noise floor.

The frequency synthesizer consumes 50 mW in the 24-GHz mode and 75 smW in the 77-GHz mode. A single 2.5-V supply is needed for the entire synthesizer. The 77-GHz and 24-GHz VCOs require 10 mA and 4 mA, respectively. The ILC consumes a maximum of 6 mA.

The measured performance of the dual-band synthesizer is summarized in Fig. 5.18. The authors are unaware of other implementations of MMW dual-band frequency synthesizers. Nevertheless, it is fair to compare the performance with single-frequency prior art in the MMW spectrum. Figure 5.19 provides a comparative list of state-of-the-art MMW frequency synthesizers.

	K-band	W-band
Locking Range	23.8-26.95GHz	75.67-78.5GHz
Phase Noise	- 114dBc/Hz@1MHz	- 103.5dBc/Hz@1MHz
Spurs	- 49.5dBc	- 47.8dBc
Output Power	- 9.5dBm	- 17.8dBm
Settling Time	<25μs	<25μs
Power Dissipation	50mW	75mW
- VCO	10mW	25mW
- ILC	5mW	15mW
- Static Divider	15mW	15mW
- PFD/CP	5mW	5mW
Technology	0.18μm BiCMOS	
Die Area	1mm × 0.8mm	

Fig. 5.18 Summary of the measured performance

	[54]	[55]	[56]	[57]	[58]	[59]	This Work
Frequency (GHz)	60	60	50	66	60	75	77
Technology	0.15μm GaAs pHEMT	200GHz SiGe	0.13μm CMOS	0.13μm CMOS	90nm CMOS	90nm CMOS	0.18μm BiCMOS
Locking Range (GHz)	0.15	3.3	4.6	1.9	2.4	0.32	2.83
Divide Ratio	12	1024	1024	128[a]	256/258	32	768
Phase Noise (dBc/Hz)	−95.5@100kHz −112.4@1MHz	−56@100kHz	−63.5@50kHz −72@1MHz	−84.1@1MHz	−85.1@1MHz	−88@100kHz −108@10MHz	−112@100kHz −114@1MHz
Spur (dBc)	-	−50	−40	−15.2	−50.75	<−72	−47
Loop Bandwidth (MHz)	178	0.2	0.5	1.8	-	2.5	1
P_D (mW)	370	650	57	72	80	88	75
Chip Area (mm^2)	4.23	0.8	0.87	1.41	0.95	0.8	0.8[b]

[a] The VCO has a push-push output, so the effective divide ratio is 256.
[b] The PLL only occupies 0.4mm^2 of the chip area with pads. The rest is other circuitry not part of the PLL.

Fig. 5.19 Performance comparison of millimeter-wave frequency synthesizers

5.4 Chapter Summary

A new dual-band architecture for MMW frequency synthesizers utilizing multiple modes of operation of an injection-locked circuit has been described. A highly-integrated synthesizer prototype chip has been designed and implemented in a 0.18 μm BiCMOS technology. The versatile synthesizer architecture targets 24/77-GHz automotive radars, and is also suitable for 94-GHz imaging applications. Measurements of the fabricated prototype demonstrate excellent results, including a locking range of 23.8–26.95 GHz and 75.67–78.5 GHz. Detailed design and analysis of a dual-mode injection-locked circuit, operating either as

a divide-by-three or as a tuned buffer, have been described. The divide-by-three circuit achieves the highest operating frequency reported to date inside a synthesizer loop. This work reveals the first step toward the realization of fully-integrated dual-band MMW radar transceivers.

Appendix A: Oscillation Amplitude and Phase Noise of Colpitts and LC Emitter-Degenerated Oscillator Topologies

A.1 Oscillation Amplitude

The steady-state base-to-emitter voltage V_{BE} for a Colpitts oscillator is given by [83]

$$V_{BE} = \frac{2I_{CC}}{g_{mc}}, \tag{A.1}$$

where I_{CC} is the collector bias current and g_{mc} is the minimum required transconductance for oscillation. For the conventional Colpitts oscillator, (A.1) can be written as

$$V_{BE} = V_O - n_{COLP}V_O = \frac{2I_{CC}}{\omega_{COLP}^2 C_1' C_2 R_S}, \tag{A.2}$$

where R_S is the series tank resistance. Replacing R_S by its parallel equivalent resistor R_T, we get

$$V_{BE} = (1 - n_{COLP})V_O = \frac{2I_{CC}R_T}{\omega_{COLP}^4 L_B^2 C_1' C_2}, \tag{A.3}$$

resulting in a peak oscillation amplitude of

$$V_O = 2I_{CC}R_T n_{COLP}. \tag{A.4}$$

For the LC emitter-degenerated oscillator,

$$\begin{aligned} V_{BE} = V_{O,LC} - n_{LC}V_{O,LC} &= \frac{2I_{CC}R_T}{\omega_{LC}^4 L_B^2 C_1' C_2 (1-k)} \\ &= 2I_{CC}R_T \cdot \frac{k^2}{1-k} \cdot \frac{L_{DEG}^2 C_2}{L_B^2 C_1'} \end{aligned} \tag{A.5}$$

from which we obtain

$$V_{O,\,LC} = 2I_{CC}R_T \cdot \frac{k^2}{n_{LC}(1-k)^2} \cdot \frac{L_{DEG}^2}{L_B^2}. \tag{A.6}$$

It is clear from (A.4) and (A.6) that for a given bias current, LC emitter degeneration provides more flexibility in setting the oscillation amplitude compared to

the conventional Colpitts topology. Assuming the same R_S for the two topologies[3] and assuming that the tank capacitors are kept constant for the purpose of comparison (which implies that the inductors in the tank are varied to obtain the same oscillation frequency for the two topologies), we can obtain the ratio of the two oscillation amplitudes as

$$\frac{V_{O,\,LC}}{V_O} = \frac{(1 - n_{COLP})}{(1 - n_{LC})} \cdot \frac{1}{(1 - k)} \tag{A.7}$$

for the same oscillation frequencies. Since $k < 1$, $n_{LC} > n_{COLP}$ and therefore, $V_{O;LC}$ is always greater than V_O.

A.2 Phase Noise Analysis Using Leeson's Model

From [71], the $1/f^2$ phase noise of the Colpitts oscillator can be expressed as

$$S_{\Delta\phi out,\,COLP} = 2\frac{\left\langle \overline{I_n^2} \right\rangle}{V_O^2} \cdot \left| \frac{A_0}{C_I'} \right|^2 \cdot \frac{1}{\Delta\omega^2}, \tag{A.8}$$

where A_o is the element A of the ABCD matrix of the feedback network (i.e., the tank), $C_I' = dC_I/d\omega\,|_{\omega_0}$, and C_I is the imaginary part of the element C of the matrix. For a Colpitts oscillator, $A_0 = -C_2/C_1'$ and

$$C_I = (C_1' + C_2)\omega - LC_1'C_2\omega^3 \tag{A.9}$$

Replacing C_2 by $C_{2;eff}$, differentiating C_I with respect to ω, and then setting $\omega = \omega_0 = \omega_{LC}$, we obtain, for an LC emitter-degenerated oscillator,

$$C_I' = -2\left(C_1' + C_{2,\,eff}\big|_{\omega_{LC}}\right) - \omega_{LC}C_1' \left| \frac{1}{C_{2,eff}} \frac{dC_{2,\,eff}}{d\omega} \right|_{\omega_{LC}}. \tag{A.10}$$

From (5.3),

$$C_{2,\,eff}\big|_{\omega_{LC}} = C_2\,(1 - k)\,, \text{ and} \tag{A.11}$$

$$\frac{1}{C_{2,\,eff}} \cdot \frac{dC_{2,\,eff}}{d\omega}\bigg|_{\omega_{LC}} = \frac{2k}{\omega_{LC}}, \tag{A.12}$$

where k is given by (5.7). Substituting (A.11) and (A.12) in (A.10), we obtain

$$C_I' = -2\left[(1 + k)C_1' + (1 - k)C_2\right]. \tag{A.13}$$

[3] In our design (and for W-band silicon-based designs in general), the tank resistance is dominated by varactor loss, validating this assumption.

Substituting the values of A_0 and C_I' in (A.8) and re-arranging the result, we obtain the expression for the close-in phase noise of an emitter-degenerated Colpitts oscillator as

$$S_{\Delta\phi out,\,LC} = \frac{1}{2}\frac{\left\langle \overline{I_n^2} \right\rangle}{V_{O,\,LC}^2} \cdot \frac{C_2^2}{C_1'^2\left[\left(\frac{1+k}{1-k}\right)C_1' + C_2\right]^2} \cdot \frac{1}{\Delta\omega^2}. \tag{A.14}$$

The phase noise of the conventional Colpitts topology is readily obtained from (A.14) by replacing k with 0,

$$S_{\Delta\phi out,\,COLP} = \frac{1}{2}\frac{\left\langle \overline{I_n^2} \right\rangle}{V_O^2} \cdot \frac{C_2^2}{C_1'^2(C_1' + C_2)^2} \cdot \frac{1}{\Delta\omega^2}. \tag{A.15}$$

A.3 Phase Noise Analysis Using Linear Time-Variant Model

Following the analysis in [74] for a Colpitts oscillator, the phase noise due to collector current noise can be expressed as

$$S_{\Delta\phi out,\,i_c,\,COLP} = \frac{k_B T}{4V_O^2} \cdot \frac{1}{R_T C_2^2} \cdot \frac{1}{n_{COLP}\,(1 - n_{COLP})} \cdot \frac{1}{\Delta\omega^2}, \tag{A.16}$$

and that due to R_T as

$$S_{\Delta\phi out,\,R_T,\,COLP} = \frac{k_B T}{2V_O^2} \cdot \frac{1}{R_T C_2^2} \cdot \frac{1}{n_{COLP}^2} \cdot \frac{1}{\Delta\omega^2} \tag{A.17}$$

The overall phase noise for the conventional Colpitts topology is then given by

$$S_{\Delta\phi out,\,COLP} = \frac{k_B T}{4V_O^2} \cdot \frac{1}{R_T C_2^2} \cdot \frac{2 - n_{COLP}}{n_{COLP}^2\,(1 - n_{COLP})} \cdot \frac{1}{\Delta\omega^2} \tag{A.18}$$

As discussed earlier, the LC degeneration impedance appears capacitive at the oscillation frequency of the emitter-degenerated oscillator. Therefore, the current and voltage waveforms of the emitter-degenerated oscillator are similar to those of the conventional Colpitts oscillator. This in turn implies that the device noise currents are injected into the tank at the voltage peaks, thereby reducing the amount of device noise conversion to phase noise [72]. Thus, the phase noise analysis carried out for the Colpitts topology is also valid for the LC emitter-degenerated oscillator topology.

By substituting C_2 with $C_{2,eff}\big|_{\omega_{LC}} = (1-k)C_2$ and n_{COLP} with n_{LC} in (A.18), the phase noise of an LC emitter-degenerated Colpitts oscillator is readily expressed as

$$S_{\Delta\phi out,\,LC} = \frac{k_B T}{4V_{O,\,LC}^2} \cdot \frac{1}{R_T C_2^2} \cdot \frac{2 - n_{LC}}{n_{LC}^2\,(1 - n_{LC})} \cdot \frac{1}{(1-k)^2} \cdot \frac{1}{\Delta\omega^2} \tag{A.19}$$

The ratio of the phase noises of the two oscillator topologies is

$$\frac{S_{\Delta\phi out,\,LC}}{S_{\Delta\phi out,\,COLP}} = \frac{V_O^2}{V_{O,\,LC}^2} \cdot \frac{(2-n_{LC})}{(2-n_{COLP})} \cdot \frac{(1-n_{COLP})}{(1-n_{LC})} \cdot \frac{n_{COLP}^2}{n_{LC}^2} \cdot \frac{1}{(1-k)^2} \tag{A.20}$$

Using the result of (A.7), and with the same assumptions, (A.20) is simplified to

$$\frac{S_{\Delta\phi out,\,LC}}{S_{\Delta\phi out,\,COLP}} = \frac{(2-n_{LC})}{(2-n_{COLP})} \cdot \frac{(1-n_{LC})}{(1-n_{COLP})} \cdot \frac{n_{COLP}^2}{n_{LC}^2} \tag{A.21}$$

Since $n_{LC} > n_{COLP}$, the ratio in (A.21) is always less than 1, indicating that the LC emitter-degenerated topology exhibits better phase noise than the conventional Colpitts oscillator.

From the foregoing analysis, the importance of using a linear time-variant model is clearly seen. In (A.8) and (A.14), all device noise sources are converted to phase noise by the same transfer function, whereas (A.16–A.19) indicate different transfer functions for different noise sources. The key concept that enables higher accuracy in the LTV model is the impulse sensitivity function (ISF), which is different for different noise sources and different circuit topologies [72]. Furthermore, the ISF takes into account the cyclo-stationary nature of device noise sources, whereas the Leeson's model treats all noise sources as stationary processes.

Appendix B: Locking Range of an LC-Tank-Based Injection-Locked Divide-by-Three Circuit

Figure B.1 shows a behavioral model for the analysis of an injection-locked divide-by-three circuit. The mixer output current can be expressed as [81]

$$I_o = \left[I_{dc} + I_{inj}\cos(3\omega t)\right] \sum_{k=1}^{\infty} \alpha_k \cos k\,(\omega t + \phi) \tag{B.1}$$

where ®k are the mixer non-linearity coefficients and Á is the divider output phase. The fundamental component of I_o, limiting the products to the fourth-order non-linearity, is

$$I_o = \frac{I_{dc}\alpha_1}{2}\cos(\omega t + \phi) + \frac{I_{inj}\alpha_2}{2}\cos(\omega t - 2\phi) + \frac{I_{inj}\alpha_4}{4}\cos(\omega t + 4\phi)\,, \tag{B.2}$$

from which the phase of the mixer output can be computed as

$$\gamma = \phi - \tan^{-1}\left[\frac{\frac{\alpha_2-\alpha_4}{2\alpha_1}\sin(3\phi)}{K_I + \frac{\alpha_2+\alpha_4}{2\alpha_1}\cos(3\phi)}\right] \tag{B.3}$$

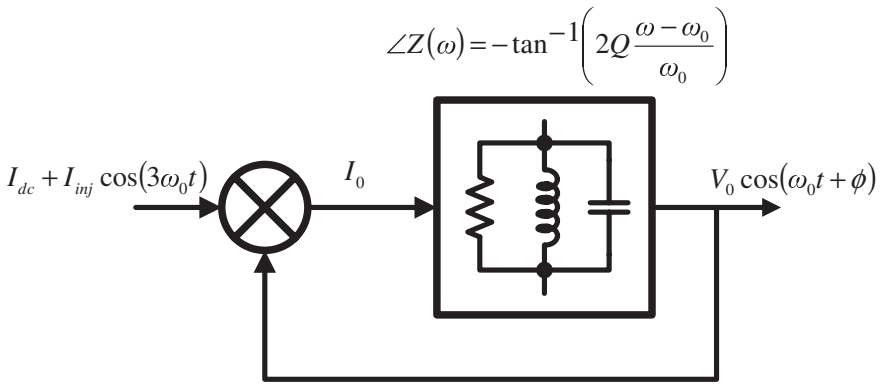


Fig. B.1 Behavioral model of the divide-by-three injection-locked frequency divider

where $K_I = I_{inj}/I_{dc}$.

The phase shift introduced by the tank is given by

$$\beta = -\tan^{-1}\left(2Q\frac{\omega-\omega_o}{\omega_o}\right) \tag{B.4}$$

and since $\beta = \phi - \gamma$, we obtain

$$-\tan^{-1}\left(2Q\frac{\omega-\omega_o}{\omega_o}\right) = \tan^{-1}\left[\frac{\frac{\alpha_2-\alpha_4}{2\alpha_1}\sin(3\phi)}{K_I + \frac{\alpha_2+\alpha_4}{2\alpha_1}\cos(3\phi)}\right] \tag{B.5}$$

After converting (B.5) into exponential form and solving the resulting quadratic equation, we get

$$\sin(3\phi) = \frac{4q\alpha_1 \pm \sqrt{16q^2\alpha_1^2 + (1-4q^2)K_I^2\alpha_2^2}}{(1+4q^2)K_I\alpha_2} \tag{B.6}$$

where $q = Q\frac{\omega_o-\omega}{\omega_o}$. Applying the identity $|\sin(3\phi)| \leq 1$, neglecting the q^2 terms and simplifying, we obtain the relation

$$q \leq \frac{K_I\alpha_2}{2\alpha_1} \tag{B.7}$$

The maximum two-sided locking range is then readily computed as

$$\omega_L = \frac{\omega_o}{Q}\frac{K_I\alpha_2}{\alpha_1} \tag{B.8}$$

Chapter 6
A Single-Chip Dual-Band 22–29-GHz/77–81-GHz BiCMOS Transceiver

A clear trend in wireless applications during the last decade has been the push towards higher integration, and multi-mode and multi-band operation, in order to enable low-cost high-functionality consumer devices. As the deployment of silicon-based MMW technology becomes widespread, similar trends may be expected in the MMW space. A dual-band 90 nm CMOS receiver chip, operating in the 60 GHz and 77 GHz bands, was recently reported [84]. Simultaneous operation of a 60 GHz device as a radar and a communication system has been investigated [85]. Furthermore, development of a multi-mode 76–81 GHz silicon-based phased-array transceiver for operation as both short-range and long-range radars has also been proposed [86].

The principal challenge in the development of any MMW multi-band systems, however, will be the efficient generation and processing of signals in different frequencies in the MMW range on a single chip, while maintaining adequate isolation between the different frequency bands. In order to address these challenges, we first developed a fully integrated dual-band frequency synthesizer for operation in the 24 GHz and 77 GHz radar bands, as demonstrated in Chap. 4 and in [45], [46]. As a continuation of that work, in this chapter, we present a highly-integrated MMW pulsed-radar transceiver operating in the 22–29 GHz and 77–81 GHz short-range automotive radar bands. The IC has been implemented in a 0.18 μm BiCMOS technology (f_T/f_{max} = 200/180 GHz) and was first reported by the authors in [5]. Together, the synthesizer and transceiver ICs represent the first reported attempts towards implementation of highly-integrated dual-band systems in the MMW regime, particularly for automotive radar applications.

The remainder of this chapter is organized as follows: The dual-band transceiver architecture is described in Sect. 6.1. The design and analysis of the constituent circuits and sub-systems of the transceiver are explained in Sect. 6.2. Measurement results carried out on an experimental synthesizer prototype are presented in Sect. 6.3. Finally, Sect. 6.4 provides concluding remarks.

This work was done in collaboration with Fred Tzeng and Lei Zhou [5], [47].

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6.1 Dual-Band Transceiver Architecture

The proposed dual-band transceiver is based on the pulsed-radar architecture described in Chap. 2 and in [2], [32]. This architecture is promising for short-range radars as the transmitter and receiver operate in a time-duplexed fashion, thereby achieving a better dynamic range than other radar architectures such as FM-CW and PN-coded radars. As discussed in Sect. 3.2, a baseband pulse is upconverted to the carrier frequency and is transmitted by the sensor at a rate determined by the prf. The reflected pulse from the target is correlated with a locally delayed version of the transmitted pulse in the receiver. The target range is then estimated by determining the delay between the instants of pulse transmission and receiver correlation.

Figure 6.1 shows the detailed block diagram of the dual-band TRX. The chip is comprised of a receiver (RX), a transmitter (TX), a dual-band frequency synthesizer and a high-speed CMOS pulse generator. Design efforts have been focused on maximizing the re-use of circuits in the two bands to reduce die area. As a result, the downconversion chain in the receiver, the divider chain in the synthesizer, the pulse formers, and the pulse generator are all shared between the two bands, resulting in a lower overall chip area. This design is the first demonstration of a W-band synthesizer integrated within a transceiver, and also is the first reported integration of high speed CMOS digital circuitry with a 24/79-GHz automotive radar transceiver.

6.2 Transceiver Implementation

6.2.1 Receiver

The receiver in Fig. 6.1 consists of a dual-band LNA (DB-LNA), I/Q broadband downconversion mixers, I/Q dual-band pulse-formers, and variable-gain baseband amplifiers and integrators. The design of the receiver pulse-formers is similar to that of the transmitter pulse-former, and is discussed in detail in Sect. 6.2.2. As mentioned before, the entire downconversion chain (i.e., following the LNA) is shared between the two bands, resulting in a simple architecture and reduced die area.

The key circuit that enables dual-band operation in the receiver is the DB-LNA. As shown in the circuit schematic of Fig. 6.2a, the DB-LNA has two inputs, RF_{24} and RF_{79}, corresponding to the two frequency bands, and a single multiplexed output, RF_{OUT}. A two-stage cascode LNA with inductive degeneration is used for each band. The outputs of the second stages in the two paths are combined into a dual-band passive network comprising of the center-tapped inductor L_3 (0.2 nH), the capacitors C_3–C_4 (0.2 pF) and the t-lines T_3–T_4 (0.1 nH), thereby resulting in a single output for both bands. Only one of the paths is active at a time, while the unused path is turned off.

In the 79 GHz path, emitter degeneration is implemented by short-circuited t-lines T_{12} (20 pH) and T_{14} (10 pH). T_{12} and T_{14} include the parasitic inductances

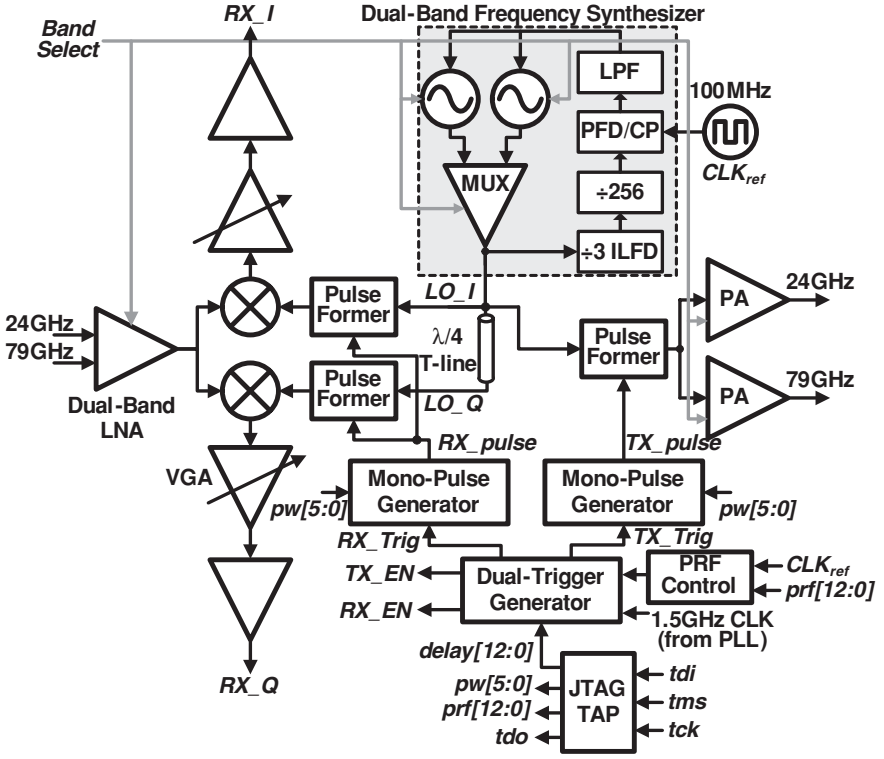

Fig. 6.1 Block diagram of the 24/79 GHz dual-band transceiver

of the vias—with approximately 3-pH value based on EM simulations—to the HBT emitters. The input pad, the DC blocking MIM capacitor C_{11} (0.2 pF) and the series t-line T_{11} (25 pH) are part of the input matching network. Inter-stage matching network is composed of T_{13} (125 pH) and C_{12} (0.2 pF). Similarly, the 24 GHz path includes degeneration inductances T_{22} and T_{24} (both 50 pH) for input matching and stability, respectively. The series inductance L_{21} (0.2 nH) and first-stage load L_{23} (0.29 nH) are implemented as spiral inductors. MIM capacitors C_{21} and C_{22} (both 0.2 pF) are used for inter-stage AC coupling. The core of the dual-band load at the outputs of the two LNAs is formed by the center-tapped spiral inductor L_3 (0.2 nH) and capacitors C_3–C_4 (0.2 pF). The outputs of the two paths are connected to this dual-band core through the t-lines T_3–T_4, as shown in the DB-LNA die micrograph of Fig. 6.2b. These interconnects are necessitated by the arrangement of the input/output pads, which itself is restricted by probing requirements. In Fig. 6.2b, additional t-line segments can be observed within the dual-band load and between the dual-band load and GSG pads. Although not explicitly shown in Fig. 6.2a, these passives are taken into account in the EM simulations during the design of the dual-band network.

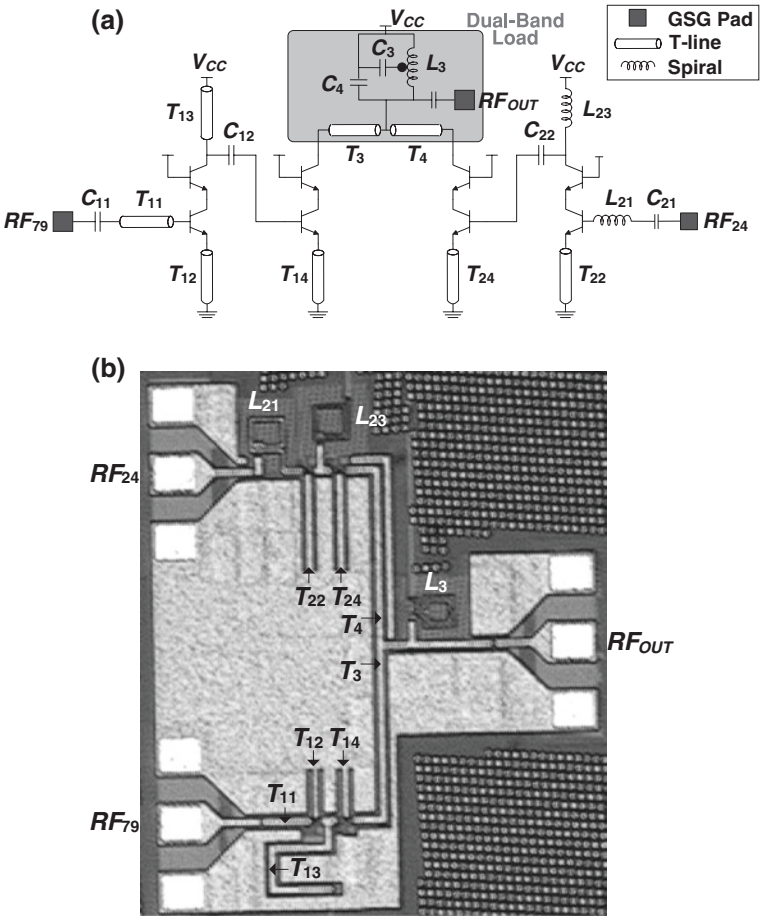

Fig. 6.2 (a) Simplified schematic of the dual-band LNA. (b) Die micrograph of the DBLNA indicating constituent t-lines and spirals

The dual-band operation of the LNA output matching network arises from the mutual coupling of the center-tapped inductor. This is shown in Fig. 6.3, where the dual-band core is redrawn along with its equivalent circuit. The center-tapped inductor, 2L, is replaced by a T-network consisting of two inductors of value $(1 - k)L$ and a third inductor of value kL, where k is the magnetic coupling factor between the two coils of the center-tapped spiral inductor ($k = 0.4$ for inductor L_3). The series combination of kL and C_1 results in a series resonance which provides the notch between the two bands. A plot of the driving-point impedance, Z_{in}, of this multi-order equivalent circuit as a function of frequency is shown in Fig. 6.3, clearly indicating two resonant frequencies.

The straightforward operation described above is complicated by the presence of other passive components that result due to unavoidable interconnects (such

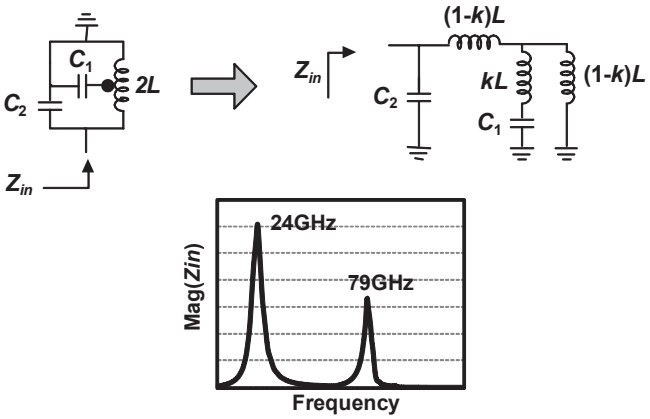

Fig. 6.3 Equivalent circuit and driving-point impedance of the dual-band load

as T_3 and T_4) and loading from the mixer input. T_3–T_4 have negligible effect on the performance in the K-band as their resonances with the HBT output capacitances occur beyond 100 GHz. The most critical loading is that due to the mixer input capacitance. Moreover, the design elements L, C_1, C_2 and k are in general frequency-dependent and therefore several iterations are necessary to obtain the desired circuit performance. First, the output impedances of the second cascode stages are obtained from simulations. These can be expressed as series RC networks as shown in Fig. 6.4. The real part varies from 25 - to 36 - between the two bands, while the capacitance is relatively constant at 15 fF. Similarly, the mixer input impedance is found as a series combination of 30 - and 70 fF and is connected to the output of the dual-band network. Now, the reactive impedances of the input and output terminations can be treated as part of the dual-band network design, as depicted in Fig. 6.4. The dual-band network is optimized for low loss in the 79 GHz band at the expense of some performance in the 24 GHz band, which is easily compensated by the high device gain in the K band. The resultant S-parameters of the network are shown in Fig. 6.4. The dual-band network achieves an insertion loss of 1.4–3.5 dB in the 22–29 GHz band and 1–1.1 dB in the 77–81 GHz band. Note that the input and output of the dual-band network in Fig. 6.4 show moderate match in the 79 GHz and 24 GHz bands, respectively. This shows that some performance is sacrificed in order to obtain dual-band operation. Nevertheless, the degradation in insertion loss is on the order of only a few tenths of a dB, as inferred from simulations.

Tapered coplanar GSG pads are used for better modeling accuracy [87] and are absorbed in the matching network design. All t-lines are implemented as conductor-backed coplanar waveguide structures [88]. The DB-LNA circuit occupies 0.75×0.65 mm^2 including the GSG pads.

A critical challenge in any single-chip multi-band system is to achieve sufficient isolation among the bands. Most implementations solve this problem

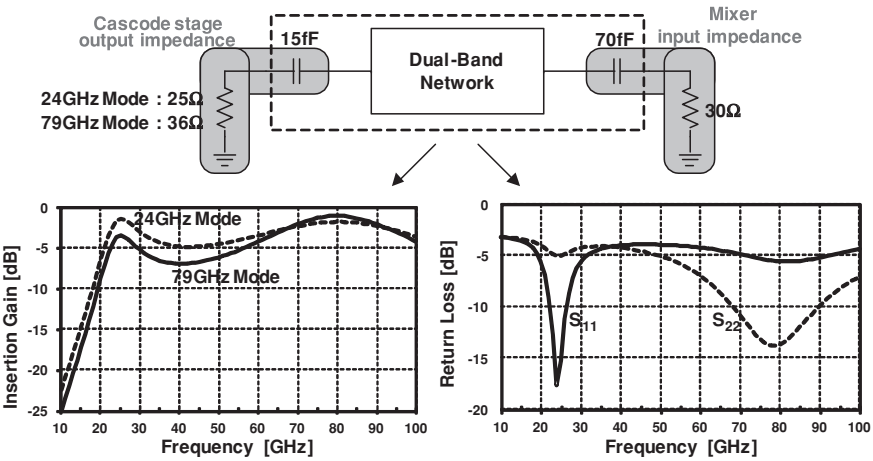

Fig. 6.4 Simulated S-parameters of the dual-band matching network terminated with the output impedance of the cascode stage and the input impedance of the mixer

by employing completely separate RF chains for different bands. In this work, the outputs of the LNAs in the two bands are multiplexed into a single output, resulting in high cross-band isolation requirements. Although only one path is active at a time, an interferer from the other input can desensitize the following mixer. In order to understand the need for isolation, consider the LNA-mixer block diagram of Fig. 6.5. In this example, the desired signal is centered at 25.5 GHz and an interferer appears at the 79 GHz input. Accordingly, the 24 GHz path is enabled while the 79 GHz path is turned off. Consequently, the 24 GHz LNA provides an on-state insertion gain of $G_{24,ON}$ to the desired signal while the 79 GHz interferer experiences an off-state attenuation of $G_{79,OFF}$. The LO signals of the downconversion mixers are in the 24 GHz band. The 24 GHz input signal is downconverted to DC by the mixer while also generating the sum frequency component at 51 GHz. The 79 GHz signal also results in two outputs, one at 53.5 GHz and the other at 104.5 GHz. Except the desired output at DC, all other mixing products are filtered in the low-pass baseband circuitry. Thus, the interferer does not result in in-band frequency components at the mixer output (ideally, at least). Nevertheless, if the interferer power level at the mixer input is higher than the input P_{1dB} (1 dB compression point) of the mixer, it will result in circuit non-linearities in the signal band, affecting the detection of the desired signal [89]. The above statements hold true for the other case as well, i.e. when the desired signal is in the 79 GHz band and the interferer in the 24 GHz band. Therefore, high isolation is necessary from each input to the LNA output in the off-state. To this end, a dedicated first stage is used in each path, and cascode topology is used for the amplifier stages. Furthermore, series T-lines T_3–T_4 improve isolation between the two paths by partially resonating out the parasitic capacitances at the collector terminals of the second-stage cascode transistors which, in turn, results in an increase in the amplifier's gain.

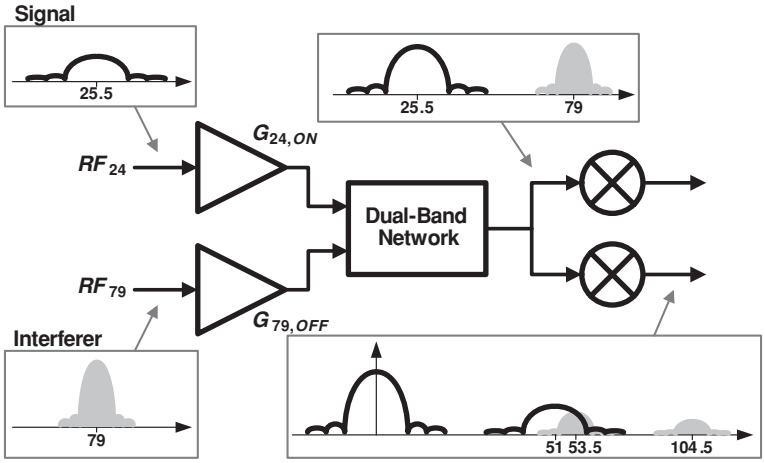

Fig. 6.5 Signal spectra along the receiver chain in the presence of an interferer in one of the paths

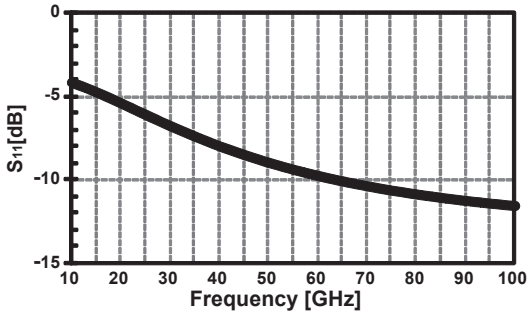

Fig. 6.6 Simulated input return loss of the mixer

The LNA is followed by double-balanced I/Q mixers, variable gain amplifiers (VGAs) and integrators. The I/Q mixers are Gilbert-cell mixers with resistive degeneration for input matching. As discussed earlier, the dual-band matching network provides power match between the LNA output and the mixer input. As observed from Fig. 6.4, the power match is better than −10 dB in the 79 GHz band and is around −5 dB in the 24 GHz band. Simulations of the standalone mixer (i.e., without the dual-band network), shown in Fig. 6.6, also reveal broadband input return loss better than −5 dB in the 24 GHz band and −10 dB in the 79 GHz band. Due to abundant HBT gain in the 24 GHz band, the relatively poor return loss is readily accommodated. Pulse formers generate the reference pulses for correlation with the received pulses in the mixers. The VGAs are also implemented as a Gilbert-cell topology, where their gains are controlled by the bias current. The integrate-and-dump circuitry is a G_m–C based design, similar to the one reported in [8].

6.2.2 Transmitter

The transmitter consists of a dual-band pulse former, and 24 GHz and 79 GHz wideband power amplifiers (PAs). The signal flow in the transmitter is the inverse of that in the receiver, except for the absence of quadrature signals. As shown in Fig. 6.1, the pulse former is shared between the 24 GHz and 79 GHz paths and its dual-band output drives the two PAs. The PAs provide separate outputs for the two radar bands.

Figure 6.7 illustrates the dual-band pulse-former circuit, which is essentially a double-balanced Gilbert-type upconversion mixer with dual-band LC tank outputs, enabling it to upconvert the baseband pulse to the transmitter carrier frequency in either of the two bands. The Gilbert cell is formed by the current-steering quad Q_3–Q_6 stacked on top of the lower differential pair Q_1–Q_2. An NMOS tail current source M_1 provides the bias current of the pulse former. The dual-band output loads have the same topology as the dual-band network used in the LNA. They consist of center-tapped spiral inductors L_1–L_2 (200 pH), MIM capacitors C_1–C_4 (200 fF) and load resistors R_1–R_2 (100 -). The dual-band network increases the conversion gain of the mixer and provides bandpass filtering in the 24 GHz and 79 GHz bands to restrict the transmitted signal within the regulated transmit mask. LO leakage is reduced by terminating one of the differential pair outputs in an AC short circuit, so that the mixer quad steers the output currents into the supply when the baseband pulse is in the off-state. The baseband pulse inputs are applied to the mixer quad Q_3–Q_6 and the LO inputs to the lower differential pair Q_1–Q_2. This configuration, combined with the inherent benefits of the double-balanced topology, further reduces the LO leakage to the transmitter output [11]. The pulse former is followed by emitter follower buffers to drive the two PAs. The input pads of the PAs, included for debugging purposes, are absorbed into the buffer design and can be removed in a revised implementation for improved performance.

The schematics of the 79 GHz and 24 GHz transmitter PAs are shown in Fig. 6.8a, b, respectively. Both PAs consist of common-emitter stages operating in Class-A mode. The 79 GHz PA is a cascade of three single-ended common-emitter HBT amplifier stages. The first and second stages each consists of two 10.16^{-1} m-long HBT devices (Q_3–Q_4) in parallel, while the third stage consists of four parallel HBTs (Q_5) in order to achieve higher output power. Due to the higher device gain in the 24 GHz band, only two stages are needed for the 24 GHz PA. The HBTs Q_6 (2×10.16 ¹m) and Q_7 (4×10.16 ¹m) are sized similar to the devices in the 79 GHz PA. A cascode pre-driver, consisting of the HBTs Q_1–Q_2 (2×10.16 ¹m), precedes the three-stage 79 GHz PA to provide additional signal amplification, while also improving the LO feedthrough and the isolation between the two transmit paths. The PAs operate from a 1.8 V supply as the BV_{CEO} of the high-speed HBTs in this process is 1.9 V. The bias networks of the amplifier stages are designed to provide a base impedance of about 200 -. This impedance corresponds to a BV_{CER} of 3.5 V, which is high enough to prevent HBT breakdown at the intended PA output power levels in this work. 0.2 pF and 1 pF MIM capacitors are used for inter-stage

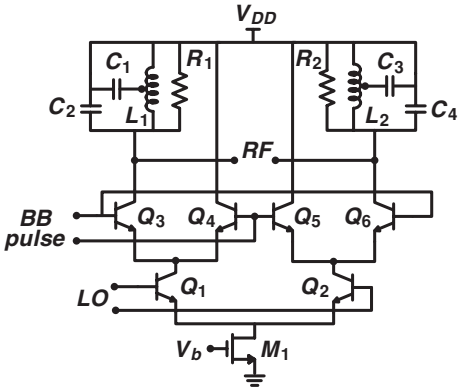

Fig. 6.7 Schematic of the dual-band pulse former circuit

AC coupling in the 79 GHz and 24 GHz PAs, respectively. Input, output and inter-stage matching networks are designed using t-lines and MIM capacitors. The t-lines are implemented as conductor-backed coplanar waveguide (CPW) structures. The GSG pads are absorbed in the input and output matching networks.

The design of the PAs was carried out with the aim of first-pass success, at the expense of some performance. Most importantly, the 24 GHz PA incorporates t-line-based matching networks instead of spiral inductors to ensure modeling accuracy, as t-lines provide well-defined return current paths. T-lines with characteristic impedance Z_0 of only 46 - are used in the design, with the exception of the shunt stubs in the single-stub tuned matching networks at the inputs of all stages in the 79 GHz PA. T-lines with a Z_0 of 74 - and an electrical length of 94° are used to implement these shunt stubs, which also feed the DC bias to the HBT inputs. The electrical lengths of the 46-- t-lines vary from 14° to 42° in the 79 GHz PA, and from 14° to 25° in the 24 GHz PA. The quarter-wavelengths of the 46- lines are about 425 ¹m and 1.5 mm in the 79 GHz and 24 GHz bands, respectively.

In order to design the inter-stage matching networks, the output impedance of the preceding stage and the input impedance of the following stage are determined. At this point, a matching network can be readily synthesized to directly match the aforementioned impedances. But, in this work, a different approach has been adopted. The methodology for the design of matching networks is illustrated in Fig. 6.9, taking the matching network between the second and third stages of the 79 GHz PA as an example. The output impedance of the second stage transistor, Q_3, is $Z_A = 8.5 - j6.2$ -, while the input impedance of the third stage HBT, Q_4, is depicted as $Z_B = 2.1 - j0.9$ -. Individual matching networks are designed to transform each of these impedances Z_A and Z_B to 50 -, as shown graphically on the Smith chart of Fig. 6.9. The resulting networks are then directly cascaded to accomplish inter-stage matching. While this approach results in more elements in the inter-stage matching networks and hence higher insertion loss of the matching networks, it enables easy and straightforward design. Each stage can be designed individually using this approach as its input/output matching networks are not

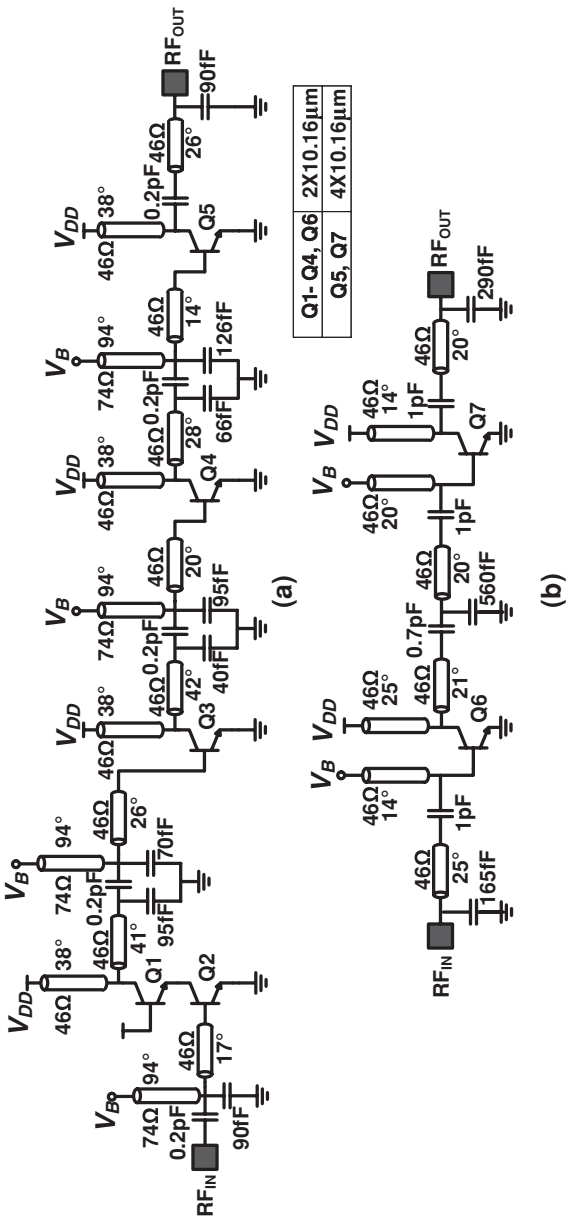

Fig. 6.8 Schematics of (a) the 79 GHz and (b) the 24 GHz power amplifiers

affected by the terminal impedances of the preceding and following stages. This is especially beneficial in the PA design in this work as the power HBTs have significant feedforward capacitance and the output matching network affects the input impedance of each amplifier stage.

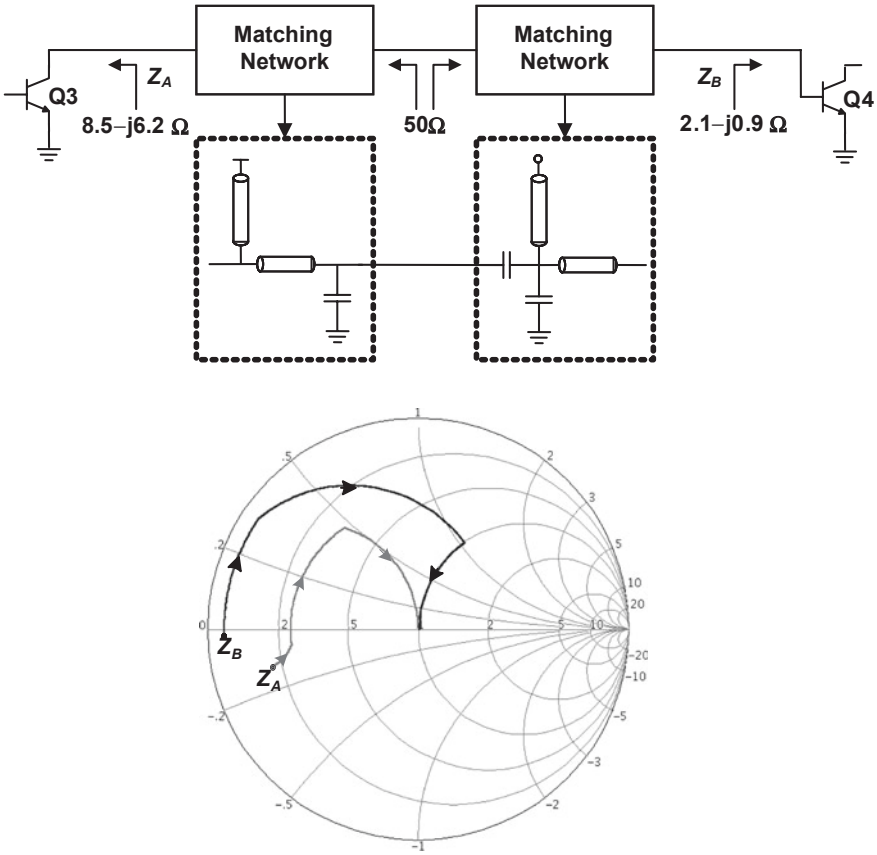

Fig. 6.9 Inter-stage matching methodology in the PAs

6.2.3 Dual-Band Frequency Synthesizer

The transceiver chip includes a dual-band frequency synthesizer which provides the sinusoidal carriers for upconversion of the baseband pulses to the 24 GHz and 79 GHz bands. The block diagram of the synthesizer is shown in Fig. 6.10. The design is an improved variant of the 24/77 GHz synthesizer chip reported in [45]–[46] and described in Chap. 5. The synthesizer consists of two VCOs, one for each radar band. The outputs of the VCOs are multiplexed into the input of an injection-locked circuit (ILC). The ILC acts as a divide-by-three circuit for the 79 GHz input and as a tuned buffer for the 24 GHz input. Thus, the division ratio is 768 in the 79 GHz band and 256 in the 24 GHz band. Static emitter-coupled logic (ECL) and CMOS dividers, CMOS phase-frequency detector, charge-pump and an off-chip low-pass filter close the loop and lock the synthesizer output to a 100 MHz crystal reference signal. Note that only one of the VCOs is operating

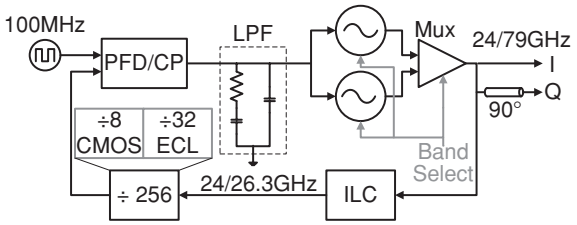

Fig. 6.10 Block diagram of the dual-band frequency synthesizer

at a time. Design, analyses and measurements of the synthesizer circuits are discussed in depth in Chap. 5. Only key additions and improvements over the original design are discussed here. Specific improvements include precise prediction of the operation frequency through a more accurate inductor model, as described in [46], and quadrature generation required for direct downconversion. Furthermore, the W-band VCO tuning range has been shifted to span the 77–81 GHz band.

The 79 GHz VCO is a modified differential Colpitts oscillator, with an LC degeneration technique which enables higher oscillation frequencies, higher tuning range and lower phase noise compared with other topologies [46]. The 24 GHz VCO is a cross-coupled LC oscillator design with the tank formed by a spiral inductor and MOS varactors. The 24 GHz and 79 GHz VCO cores draw 4 mA and 10 mA, respectively, from a 2.5 V supply. The injection-locked circuit enables seamless reconfiguration of the division ratio between the two bands of the frequency synthesizer. The ILC can lock to input signals in a wide frequency range of 68.7 GHz to 85 GHz [46]. The ILC draws 2 mA and 6 mA from a 2.5 V supply in the 24 GHz and 79 GHz bands, respectively. Details of the ILC design and operation can be found in [46] and [81].

An important addition in the synthesizer over the design in [46] is the generation of quadrature outputs. In this work, the dual-band quadrature signal is generated through varactor-loaded quarter-wave coupled transmission lines, depicted in Fig. 6.11a. In order to understand the circuit operation, consider a low-loss transmission line of length l. The phase shift introduced by the line is given by

$$\Delta\phi = \frac{2\pi l}{\lambda} \tag{6.1}$$

where λ is the line wavelength. If a line has a length $l_1 = \lambda_1/4$ at a frequency f_1 in the 24 GHz band, the phase-shift of the line at f_1 can be calculated from (6.1) as

$$\Delta\phi @ f_1 = \frac{2\pi}{\lambda_1} \cdot \frac{\lambda_1}{4} = \frac{\pi}{2} \tag{6.2}$$

indicating a phase-shift of 90°. The phase-shift at the frequency $3f_1$ can be similarly written as

$$\Delta\phi @ 3f_1 = \frac{2\pi}{\lambda_1/3} \cdot \frac{\lambda_1}{4} = \frac{3\pi}{2} \tag{6.3}$$

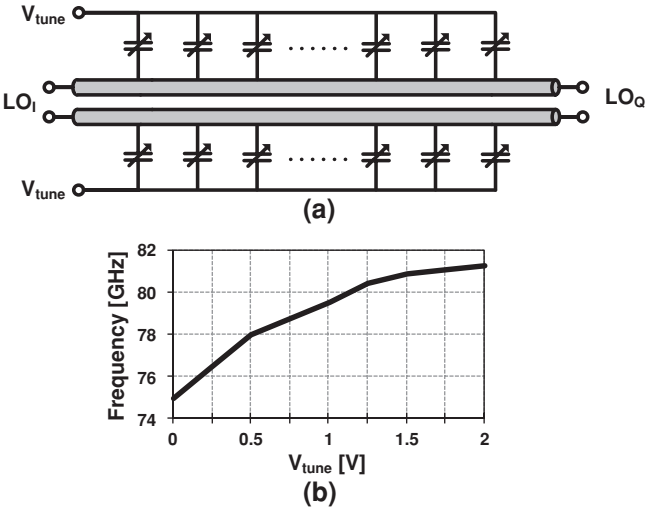

Fig. 6.11 (a) Dual-band quadrature LO generation using quarter-wave coupled lines. (b) Simulated frequency at which the coupled lines are 3λ/4 long, as a function of the varactor tuning voltage

indicating a phase-shift of 270° or equivalently −90°. Therefore, a quarter-wave t-line in the 24 GHz band can provide 90° phase shift in the 24 GHz band and −90° in the 79 GHz band. Such a t-line can then be used to generate a signal in quadrature with the LO signal from the frequency synthesizer in both bands (the sign of the phase shift is inconsequential in the signal downconversion). As shown in Fig. 6.11a, quarter-wave coupled lines (for differential signals) are used to generate LO_Q, which is in quadrature with the synthesizer output LO_I. Since a quarter-wave line provides 90° phase-shift only at a certain frequency, a tuning mechanism is necessary to cover the tuning range of the VCOs. Therefore, the coupled lines are periodically loaded with MOS varactors that fine tune the electrical length of the lines to λ/4. With the introduction of MOS varactors, the passive structure of Fig. 6.11a can be considered as a loaded line phase shifter [28]. Each of the varactors contributes a tunable phase-shift given by

$$\Delta\phi_{\text{var}} = \tan^{-1}\left[\pi f Z_0 C(V)\right] \tag{6.4}$$

where Z_0 is the characteristic impedance of the line and C(V) is the variable capacitance of the varactors. The coupled lines are laid out with side and bottom ground shields, and holes are made in the bottom ground plane where the lines connect to the varactors. Figure 6.11b shows the simulation plot of the frequency at which the phase-shifter provides a quadrature phase shift in the 79 GHz band, as a function of the varactor tuning voltage V_{tune}. The entire 79 GHz band is readily covered using the aforementioned tuning mechanism. The simulated I/Q mismatch is better than 2°. While the additional phase shift from the varactor helps reduce the line length, it also introduces loss due to signal reflection from the varactor

load. Furthermore, varactors inherently add loss due to finite Q, especially in the 79 GHz band. The LO buffers are designed to provide sufficiently high voltage swings at the inputs of the pulse formers so that their conversion gain is insensitive to the frequency-dependent losses in the 90° phase-shifter network. Note that the phase-shift in (6.4) is not linear with frequency, resulting in a dispersive line. This effect is further exacerbated by the non-linear tuning curve of the varactors. In spite of the above drawbacks, a directional coupler or a more complex I/Q generation circuitry was not employed, in order to obtain first-pass success.

6.2.4 Baseband Pulse Generator

Several pulse generator designs have been reported in prior art [6], [90]. A CMOS pulse generator, generating pulses directly in the 22–29 GHz band, was reported in [90]. The design required precise transistor dimensions for predicting the center frequency of the pulse accurately, and no method for controlling and programming the pulse width was reported. The pulse generator in this work has been designed using CMOS logic requiring no DC power consumption. The CMOS implementation enables a highly reconfigurable and programmable design. Furthermore, the pulse generator does not require an off-chip clock and the clock signals required for its operation are derived on-chip from the frequency synthesizer circuitry.

In order to detect targets over a wide range of 0.15 m to 40 m, a widely-tunable delay between the instants of pulse transmission and receiver correlation is necessary. Moreover, to achieve longer range and higher range resolution, it is desirable to incorporate variable prf and pulse width. These programmable parameters essentially provide a great deal of flexibility in designing radar DSP algorithms, leading to improved radar performance. For instance, longer pulse-widths (with pulse compression) can be transmitted to detect targets at longer ranges [2], [24]. Variable prf can be used to reduce ambiguities in either range (low prf) or Doppler velocity (high prf) [24]. To meet the aforementioned requirements, the CMOS baseband pulse generator, shown in Fig. 6.12, has been designed to generate pulses with widths ranging from 200 ps to 2 ns (pw[5:0]), with a variable prf of 1 MHz to 1.5 GHz (prf[12:0]). The delay between the TX and RX triggers can be tuned from 1 ns to 0.3 ¹s (delay[12:0]), corresponding to the 0.15–40 m radar range. An on-chip JTAG TAP interface is used to input the control bits of the pulse generator.

The constituent building blocks of the pulse generator are shown in Fig. 6.12. Timing diagrams of Fig. 6.13 illustrate the operation of the pulse generator. The prf generation circuitry consists of a 12-bit counter and is clocked by the 100 MHz reference of the dual-band frequency synthesizer. The 12-bit counter counts for a duration equal to 1/prf and generates a short pulse at the end of the count. The short pulse triggers the transmit enable (TX_EN) signal while the counter resets its count. The rising edge of TX_EN triggers a circuit which generates the transmit trigger (TX_Trig) sufficiently wide ($\approx$ 4 cycles of the trigger generator clock) for

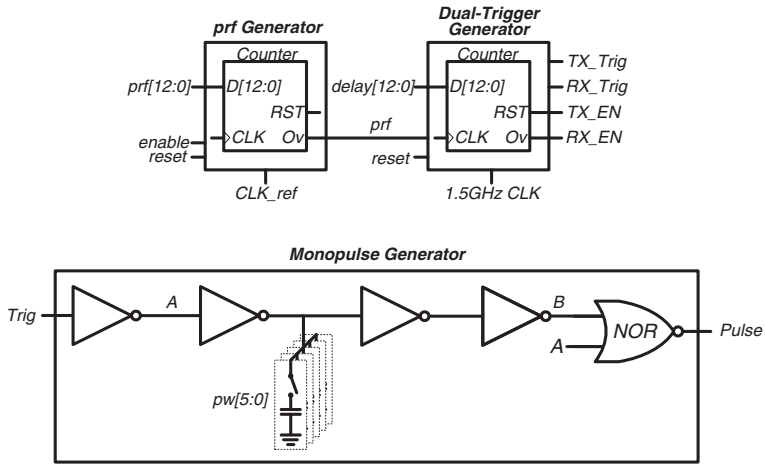

Fig. 6.12 Pulse generator schematics

reliable operation of the monopulse generator. At the same time, another 12-bit counter (in the dual-trigger generator) is reset and its count duration is set equal to the desired delay between the transmit and receive triggers. As mentioned before, by varying this delay using delay[12:0], targets in different range gates can be sequentially detected. At the end of the count, the receive enable signal, RX_EN, is set active and then generates the receiver trigger, RX_Trig. The 1.5 GHz clock required for the TX/RX trigger generation is derived from a divider output in the PLL loop.

The trigger signals, TX_Trig and RX_Trig, are each fed to separate monopulse generators (Fig. 6.12). The monopulse generator, whose schematic is shown in Fig. 6.12, derives the final baseband pulse from the trigger signal by a NOR operation of the original trigger signal and its delayed replica. The variable delay (and hence variable pulse width) is provided by a bank of binary weighted switched capacitors. By varying the capacitance using pw[5:0], the capacitor charging time is varied resulting in variable delay between the nodes A and B in Fig. 6.12. Representative waveforms of the transmit pulse, TX_Pulse, and receive pulse, RX_Pulse, are shown in Fig. 6.13.

6.3 Measurement Results

A prototype of the dual-band TRX has been implemented in a 0.18^{-1}m SiGe BiCMOS technology with six metal layers. The design utilizes the 0.15^{-1}m HBTs with $f_T = 200$ GHz and $f_{max} = 180$ GHz for processing MMW signals, while 0.18 μm MOSFETs are used for digital logic functions (including the high-speed pulse generator and the frequency synthesizer). Figure 6.14 shows the die

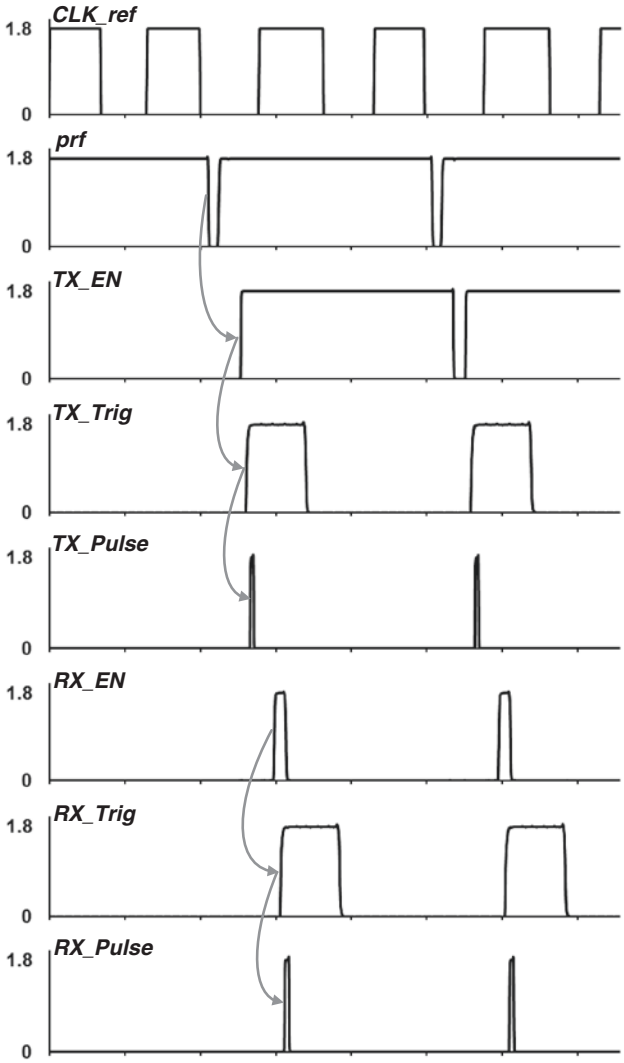

Fig. 6.13 Timing diagram of the pulse generator

micrograph of the 3.9 mm × 1.9 mm dual-band TRX. The LNA is at the top left, the dual-band synthesizer at the top center, the pulse generator at the bottom center, and the power amplifiers occupy the right-half of the chip.

As evident from circuit descriptions of Sect. 6.2 and the die micrograph in Fig. 6.14, both transmission lines and spiral inductors have been used extensively in the MMW circuits in the TRX. The 2.8^{-1}m-thick Al top metal, M_6, was used to realize inductors and transmission lines, while ground shields were laid out in bottom metal layer, M_1. Both microstrip and conductor-backed CPW structures were

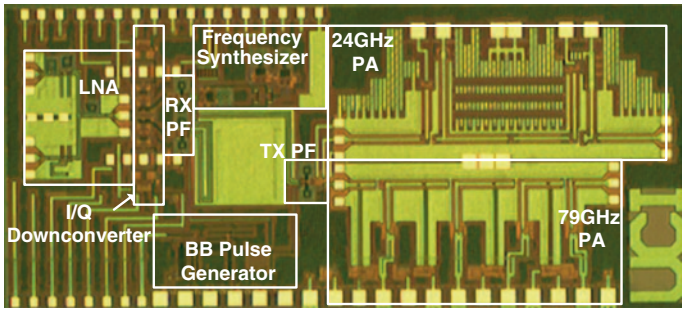

Fig. 6.14 Die micrograph of the 3.9 × 1.9 mm^2 dual-band transceiver chip

used for transmission lines in different parts of the design. The process also offers 2 fF/¹m^2 MIM capacitors. Broadband lumped circuit models for passive devices were extracted from planar 3-D electromagnetic simulation results [50].

Similar to the synthesizer chip reported in Chap. 5, the dual-band transceiver chip has been characterized in a chip-on-board environment. All pads except the MMW signals were wirebonded to a PCB. These included dc supplies, digital signals of the JTAG, control voltages of the VCO and divider and the 50–125 MHz crystal reference signal for the frequency synthesizer. In addition to circuit breakouts on the prototype chip, flexibility of monitoring and debugging signals at the inputs and outputs of major circuit blocks was enabled by internal pads. These internal pads have been absorbed as part of the circuit design. All high-frequency input/output signals of the transceiver chip were wafer-probed. While a coaxial setup was sufficient for the 24 GHz mode, the 79 GHz mode required a hybrid setup consisting of both coaxial and WR-10 waveguide components. Since the measurement frequency of the available vector network analyzer (VNA) was limited to 67 GHz, a custom measurement setup based on a scalar network analyzer (SNA) was used to measure reflection coefficients.

On-wafer measurements of the receiver reveal power conversion gains of 32–35 dB and 28–31 dB in the 24 GHz and 79 GHz bands, respectively. As observed from the measured conversion gain in Fig. 6.15, the receiver 3 dB bandwidth encompasses the 22–29 GHz and 76–81 GHz automotive radar bands. Figure 6.15 also shows the measured double-sideband noise figure (DSB–NF) of the receiver in the two bands. The receiver achieves a DSB–NF of 4.5–5.7 dB in the 22–29 GHz band and 7.5–9.5 dB in the 76–81 GHz band. Figure 6.16 shows the measured return losses at the two inputs of the receiver. The input match is better than 10 dB from 22-to-28 GHz and lower than 13 dB in the 76–81 GHz band. As described in detail in Sect. 6.2.1, when the LNA is in the off-state, the isolation between the LNA input and output should be high enough to prevent saturating the downconversion chain following the LNA. The measured off-state isolation is lower than 60 dB in the 24 GHz band and about 30 dB in the 79 GHz band, as depicted in Fig. 6.17. The receiver dissipates 107.5 mW and 162.5 mW in the 24 GHz and 79 GHz bands, respectively.

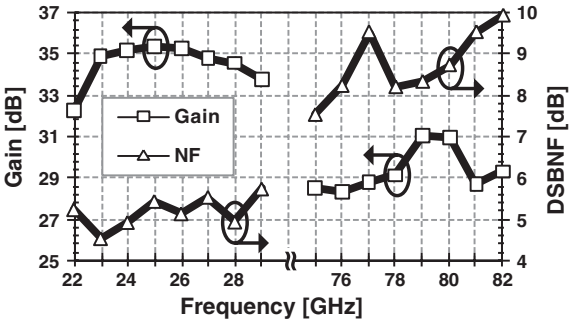

Fig. 6.15 Measured conversion gain and double-sideband noise Figure of the dual-band receiver

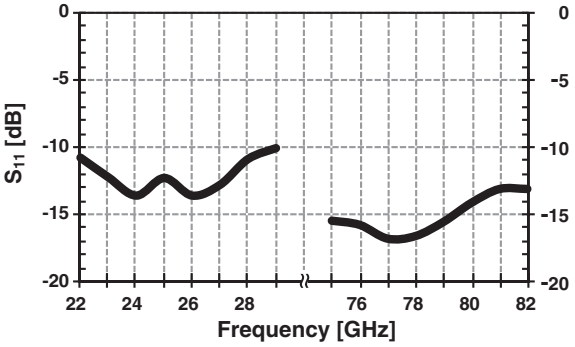

Fig. 6.16 Measured return loss at the receiver inputs in the two bands

Figure 6.18 depicts the power gain and output power at the 1 dB compression point of the MMW power amplifiers. The 24 GHz PA achieves a maximum power gain of 18 dB with a 3 dB bandwidth from 21 GHz to 28 GHz, and the 79 GHz PA achieves 10 dB gain with 75–80.5 GHz 3 dB bandwidth. The output P_{1dB} of the PAs are 14.5 dBm and 10.5 dBm in the 24 GHz and 79 GHz bands, respectively. The 24 GHz PA and the 79 GHz PA achieve power-added efficiencies (PAE) of 13.9 % and 4.7 %, respectively. The corresponding drain efficiencies are 14.2 % and 5.4 %. At the 1 dB compression point, the 24 GHz PA consumes 110 mA and the 79 GHz PA draws 115 mA, both from a 1.8 V supply. The measured output match of the PAs is better than {5 dB in the operating frequency bands, as shown in Fig. 6.19. The transmitter circuits dissipate 312.5 mW and 332.5 mW in the 24 GHz and 79 GHz bands, respectively.

The performance of the dual-band frequency synthesizer is characterized in the same fashion as described in Chap. 5. The synthesizer achieves a locking range from 23.8 GHz to 26.95 GHz in the K band and from 78.4 GHz to 81.1 GHz in the W band. The loop bandwidth of the synthesizer is about 1 MHz. The closed-loop phase noises at the outputs of the 24 GHz and 79 GHz VCOs are 114 dBc/Hz and 100.4 dBc/Hz, respectively, at 1 MHz offset from the carrier. The reference spurs are at least 47 dB below the carrier in both bands. The synthesizer consumes 90 mW in the 24 GHz band and 120 mW in the 79 GHz band. The interested reader

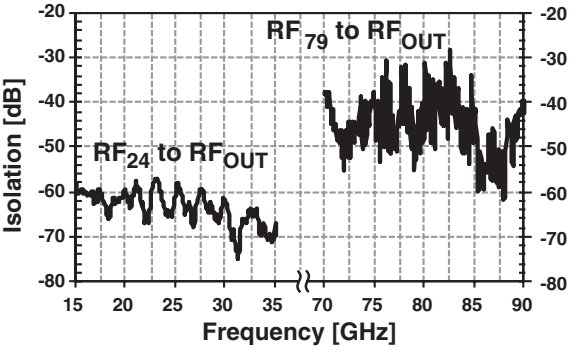

Fig. 6.17 Measured off-state isolation between LNA input and output in the two bands

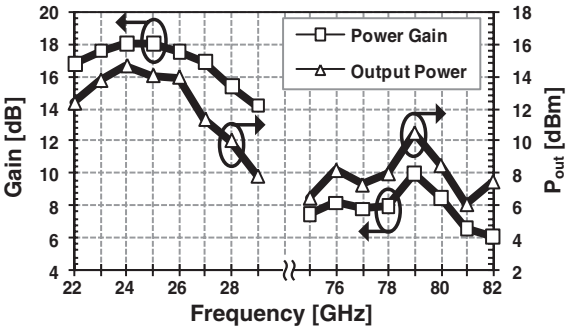

Fig. 6.18 Measured power gain and output P_{1dB} of the power amplifiers

is referred to Chap. 5 for details of the software-based frequency-lock calibration and representative measurement results of the synthesizer.

The MMW pulse measurements were performed with the transmitter, baseband pulse generator, frequency synthesizer and pulse former enabled, and with the receiver turned off. The time-domain waveform of the pulse at the output of the 24 GHz PA, observed directly on a sampling oscilloscope, is shown in Fig. 6.20a. The corresponding power spectral density in dBm/MHz is shown in Fig. 6.20b and meets the FCC mask except for an occasional spur. For this measurement, the LO frequency was set at the center of the band, i.e., 25.5 GHz, and the pulse-width was chosen to correspond to the maximum allowed bandwidth, i.e., 7 GHz. Figure 6.21a, b show the time-domain waveform and the power spectral density, respectively, of the pulse at the 79 GHz PA output. Analogous to the 24 GHz measurement, the LO frequency and the pulse bandwidth in this case were set at 79 GHz and 4 GHz, respectively. The power spectral density is well below the allowed limit of 3 dBm/MHz. The LO leakage at 79 GHz can be clearly seen in Fig. 6.21b. Note that the W-band signal was downconverted to a 4 GHz IF using a WR-10 waveguide mixer in order to enable measurement with lower-frequency spectrum analyzer. The x-axis of the spectral plot in Fig. 6.21b has been scaled back to the W-band for clarity. Spectral nulls corresponding to pulse-widths

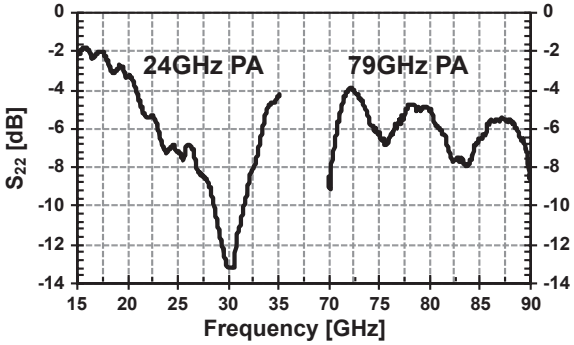

Fig. 6.19 Measured output return losses of the 24 GHz and 79 GHz power amplifiers

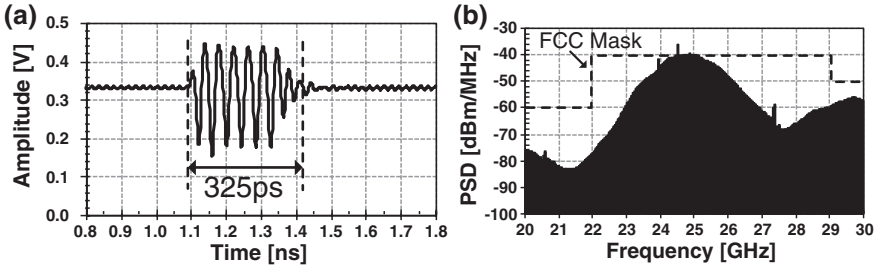

Fig. 6.20 Measured (a) time-domain waveform and (b) spectrum of the 24 GHz transmitter output pulse

of about 300 ps for the 24 GHz pulse and 1 ns for the 79 GHz pulse are readily observed in Figs. 6.20b, 6.21b, respectively.

The pulsed radar functionality of the transceiver chip can be verified either (i) through a wireless test or (ii) by inserting a tunable delay (on the order of the pulse repetition interval) between the transmitter output and the receiver input. Due to the unavailability of antennas and widely tunable delay lines at the operating frequencies of the transceiver, an alternative method of radar functionality verification has been devised. This method consists of emulating the delay between the transmitted and received pulses on-chip through the baseband pulse generator. Off-chip components are still required to provide an attenuated version of the transmitter output at the receiver input. The overall radar loopback setup, when the transceiver operates in the 79 GHz mode, is depicted in Fig. 6.22. Due to the mechanical rigidity of the WR-10 waveguides used for W-band signals, the attenuated output of the transmitter cannot be directly connected to the receiver input. Therefore, the 79 GHz transmitter output is first downconverted to a 4 GHz IF using a waveguide mixer. The signal is then supplied to a waveguide upconversion mixer through a coaxial cable. The resulting

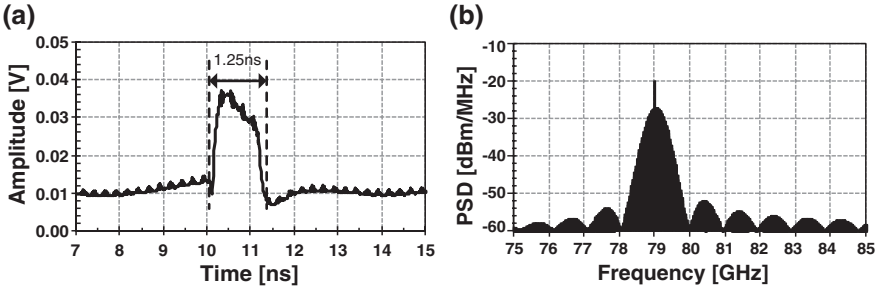

Fig. 6.21 Measured (a) time-domain waveform and (b) spectrum of the 79 GHz transmitter output pulse

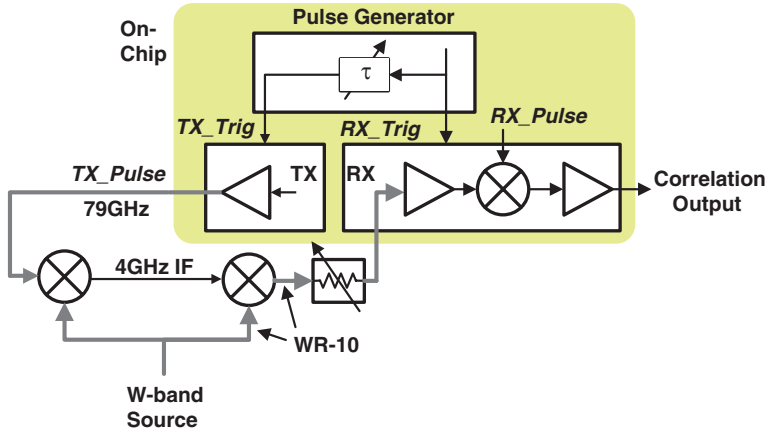

Fig. 6.22 Setup for the loopback measurement of the transceiver in the 79 GHz mode. WR-10 rigid waveguides are shown as thick *grey lines*

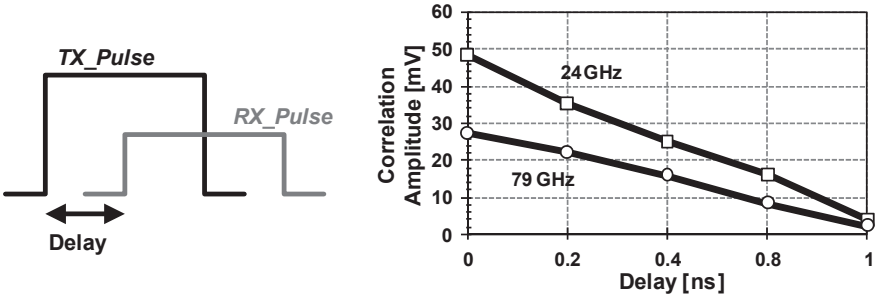

Fig. 6.23 Measured correlation output as a function of the delay between the transmitted and received pulses

Table 6.1 Summary of the measured performance

	K Band	W Band
Receiver		
Conversion Gain	35 dB	31 dB
DSB Noise Figure	4.5 dB	8 dB
Input P1dB	−33.2 dBm	−30.7 dBm
I/Q Mismatch	<2°, <1.1 dB	<5°, <1.5 dB
Input Return Loss	< −10 dB	
Output Return Loss	< −15 dB	
LO-to-RF Leakage	< −70 dB	
LO-to-IF Leakage	< −38 dB	
Power Dissipation	107.5 mW	162.5 mW
Transmitter		
Power Gain	18 dB	10 dB
Output P1dB	14.5 dBm	10.5 dBm
3dB Bandwidth	21–28 GHz	75–80.5 GHz
Power Dissipation	312.5 mW	332.5 mW
Frequency Synthesizer		
Locking Range	23.8–26.95 GHz	78.4–81.1 GHz
Phase Noise @1MHz	−114 dBc/Hz	−100.4 dBc/Hz
Reference Spurs	<−49.5 dBc	<−47 dBc
Power Dissipation	90 mW	120 mW
Transceiver		
Technology	0.18-μm BiCMOS (f_T/f_{max} = 200/180 GHz)	
Die Size	3.9 mm × 1.9 mm	
Supply Voltage	2.5 V (Analog), 1.8 V (Digital)	
Power Dissipation	510 mW	615 mW

W-band output is attenuated and fed to the receiver input. When the transceiver is operating in the 24 GHz mode, a fully-coaxial setup is possible and no frequency conversion is required. As shown in Fig. 6.22, the delay τ between the transmit trigger, TX_Trig, and the receive trigger, RX_Trig, is generated by the baseband pulse generator. This delay, in effect, introduces an offset between the transmitted pulse, TX_Pulse, and the received pulse, RX_Pulse. By varying τ, the correlation function of the receiver can be generated. As explained before, due to the power-limited transmit mask in the 24 GHz band and the high path loss in the 79 GHz band, several pulses need to be integrated to increase the signal above the noise floor.

The radar correlation function after coherent integration of 500 pulses is shown in the plot of Fig. 6.23 for a 1 ns-wide pulse, corresponding to a range resolution of 15 cm. As the delay is increased, the correlation output decreases due to the decreasing overlap between the two pulses. The delay in Fig. 6.23 is varied in steps of 200 ps corresponding to a range accuracy of 3 cm. The signal level at the

Table 6.2 Comparison of state-of-the-art 24 GHz transceivers

	Frequency (GHz)	Technology f_T/f_{max} (GHz)	RX Gain (dB)	RX NF (dB)	Phase noise[a] (dBc/Hz)	TX Pout (dBm)	DC Power (W)	Chip Area (mm^2)
[6]	22–26	0.13 µm SiGe BiCMOS	30	6	−104	3	0.37	9
[7]	22–26	0.13 µm SiGe BiCMOS 170 GHz	47	3	−104.3	1.5	0.64	5.9
[17]	24	0.13 µm CMOS	31	15 (Array)	−105	12.9	TX: 0.98 RX: 0.52	5.1
[8]	22–26	SiGe HBT 80 GHz	45	7.8	–	–	1.08	–
[18]	22–24	0.13 µm CMOS	12	7.5	–	–	0.11	3.02
[19]	24	0.18 µm SiGe BiCMOS 120 GHz	43	7.4	−103@19.2 GHz	–	0.91	11.55
[32]	22–29	0.18 µm CMOS 55 GHz	38	5.5	−107	–	0.13	3
[91]	24	0.13 µm CMOS	3.2	10 (LNA)	–	–	0.04	0.58
[92]	24	0.18 µm CMOS 60 GHz	28.4	6	−110@19.1 GHz	–	0.05	1.32
[93]	24	0.18 µm CMOS	27.5	7.7	–	–	0.06	0.2
[94]	23–25	65 nm CMOS	31.5	6.5	−110	–	0.09	2.1
[20]	24	0.18 µm CMOS	–	–	–	14	1.97	14.28
[95]	24	0.13 µm CMOS	–	–	−95.7@19.9 GHz	7	TX: 0.12 PLL: 0.04	TX: 2.2 PLL: 0.8
This work	22–29	0.18 µm SiGe BiCMOS 200/180 GHz	35	4.5	−114	14.5	0.51	7.4

[a]Phase noise at 1 MHz offset from a carrier frequency within the operating frequency range, unless otherwise noted

Table 6.3 Comparison of state-of-the-art 77/79 GHz transceivers

	Frequency (GHz)	Technology f_T/f_{max} (GHz)	RX Gain (dB)	RX NF (dB)	Phase Noise[a] (dBc/Hz)	TX Pout (dBm)	DC Power (W)	Chip Area (mm^2)
[9]	76–81	0.13 μm SiGe HBT 170/200 GHz	25.6	9	−99	5.8	0.74	1.17
[9]	77–85	0.13 μm SiGe HBT 200/300 GHz	40	3.85	−99	11.5	0.78	1.17
[10]	76–77	0.18 μm SiGe HBT 200/275 GHz	14.2	17.7	−75.3@100 kHz	8	3.3	6.82
[21], [22]	76–80	0.12 μm SiGe BiCMOS 200/250 GHz	37	8	−95@54 GHz	12.5	2.77	25.8
[23]	77	90 nm CMOS	3.5	6.8 (LNA)	−86	6.3	0.92	2.88
[12]	76.5	0.18 μm SiGe HBT 195/290 GHz	30	7 (LNA)	–	12.5	–	TX: 3.8 RX: 4.3
[13]	75–82	0.18 μm SiGe HBT 200/275 GHz	32	11 (SSB)	–	–	1.1	1.1
[14]	75–78	0.14 μm SiGe HBT 225/330 GHz	30	11.5 (SSB)	–	–	0.44	1.16
[15]	68–76	0.19 μm SiGe BiCMOS 220/250 GHz	24	4.8	−98	–	0.12	0.23
[96]	73–77	0.13 μm SiGe BiCMOS 200/250 GHz	46	7	−93@70.5 GHz	–	0.19	1.7
[16]	79	0.25 μm SiGe BiCMOS 180/200 GHz	26	–	−90	–	0.59	1.26
[11]	79	0.14 μm SiGe HBT 200/300 GHz	–	–	−96	1.5	4.12	1.16
This Work	76–81	0.18 μm SiGe BiCMOS 200/180 GHz	31	8	−100.4	10.5	0.61	7.4

[a]Phase noise at 1 MHz offset from a carrier frequency within the operating frequency range, unless otherwise noted

receiver input (i.e., the attenuator output) is set to {80 dBm for this measurement. This power level is restricted by the lower limit of the equipment and does not represent the minimum detectable signal of the receiver.

A 2.5 V supply is used for the analog circuits, with the exception of the PAs which run off a 1.8 V supply. Another 1.8 V supply drives the digital CMOS circuits. The entire transceiver dissipates 510 mW in the 24 GHz mode and 615 mW in the 79 GHz mode. In contrast, a 79 GHz transmitter reported in [11] for short-range radar applications dissipates 4.1 W. Table 6.1 summarizes the measured performance of the transceiver. Tables 6.2 and 6.3 provide comparisons of the dual-band transceiver with single-band prior art in the 24 GHz and 77/79 GHz bands, respectively.

6.4 Chapter Summary

In this chapter, a new dual-band architecture for MMW transceivers, operating in the 22–29 GHz and 76–81 GHz automotive radar bands, has been presented. A highly-integrated TRX prototype chip has been designed and implemented in a 0.18^{-1}m BiCMOS technology. Measurements of the fabricated prototype demonstrate excellent results. In the receive mode, a conversion gain of 35/31 dB and DSBNF of 4.5/8 dB have been obtained in the 24/79 GHz bands. Output powers of 14.5 dBm in the K band and 10.5 dBm in the W band have been achieved in the transmit mode. Radar functionality has been verified using loopback measurements. Detailed design and analysis of the key building blocks of the transceiver have been described. This work is the first reported integration of high-speed digital circuitry with an MMW automotive radar transceiver in the W-band.

Chapter 7
Conclusion

In this book, several UWB receiver and transceiver chip operating in the 22–29 GHz and 76–81 GHz bands and suitable for use in automotive short-range radar sensors have been demonstrated for the first time in CMOS and BiCMOS technologies. Novel circuit, system and device-level solutions were discussed and shown to be capable of meeting the performance requirements of the application. Measurement results of the fabricated prototypes demonstrate excellent results with adequate receiver gain, sufficiently low noise figure and good transmitter output power. To the best of the author's knowledge, the designs are the first-of-their-kind implementations for this application in silicon-based technologies.

An overview of fundamentals of radars was provided in Chap. 2. System-level details relevant to pulse-based radar transceiver design were discussed in Chap. 3.

In Chap. 4, the design of the first CMOS 22–29 GHz pulse-radar receiver front-end for ultra-wideband automotive radar sensors was presented. The chip includes a low noise amplifier, I/Q mixers, a quadrature voltage-controlled oscillator, pulse formers and baseband variable-gain amplifiers. The front-end achieved a gain of >35 dB and a noise figure <7.5 dB over the entire UWB 22–29 GHz frequency band, while consuming 131 mW. UWB pulse formation has also been demonstrated.

Integration of multi-mode multi-band transceivers on a single chip will enable low-cost millimeter-wave systems for next-generation automotive radar sensors. Two highly-integrated silicon ICs are designed to investigate the potential of silicon technologies for this emerging application. A new dual-band architecture for MMW frequency synthesizers utilizing multiple modes of operation of an injection-locked circuit has been described in Chap. 5. A highly-integrated synthesizer prototype chip has been designed and implemented in a 0.18 ¹m BiCMOS technology. Measurements of the 1 × 0.8 mm^2 prototype demonstrate a locking range of 23.8–26.95/75.67–78.5 GHz in the 24/77 GHz modes, with a low power consumption of 50/75 mW from a 2.5 V supply. The frequency synthesizer is suitable for integration in direct-conversion transceivers for K/W-band automotive radars and heterodyne receivers for 94 GHz imaging applications.

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The first dual-band millimeter-wave transceiver operating in the 22–29 GHz and 77–81 GHz short-range automotive radar bands was presented in Chap. 6. The transceiver chip includes a dual-band low noise amplifier, a shared downconversion chain, dual-band pulse formers, power amplifiers, a dual-band frequency synthesizer and a high-speed highly-programmable baseband pulse generator. In the receive mode, a conversion gain of 35/31 dB and DSBNF of 4.5/8 dB have been obtained in the 24/79 GHz bands. Output powers of 14.5 dBm in the K band and 10.5 dBm in the W band have been achieved in the transmit mode. Radar functionality has been verified using loopback measurements. This work is the first reported integration of high-speed digital circuitry with an MMW automotive radar transceiver in the W-band.

7.1 Future Work

As a continuation of this work, the researchers at the Nano-scale Communication IC Lab (at University of California, Irvine) are developing several single-chip silicon-based solutions for automotive radars and millimeter-wave imaging. More efforts are being concentrated on the design of low-loss passive devices. Furthermore, with the advent of advanced CMOS nodes, e.g., 65 nm, the possibility of W-band CMOS radars is also being explored. It is clear that in the near future, millimeter-wave circuit design in CMOS technologies will become mature and robust enough to replace compound semiconductors and silicon–germanium in several millimeter-wave applications.

The architectures presented in this work enable low-cost low-power compact integration of 24 GHz and 77/79 GHz radar transceivers. Further investigation and research are needed for more efficient dual-band quadrature signal generation. Efforts toward further reducing the component-count in dual-band synthesizers and transceivers are also encouraged. Development of novel architectures for integration of dual-band phased arrays is also a topic of future research. Multiple-mode phased arrays in the 77/79 GHz bands will ultimately enable integrated short-range and long-range detection using a single chip.

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