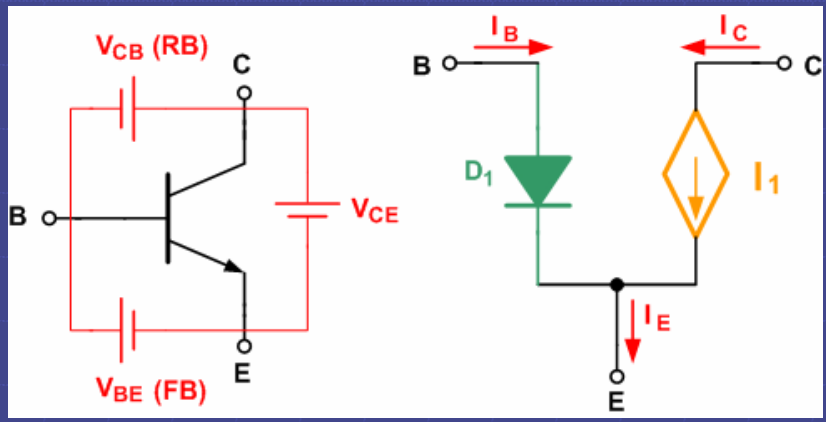
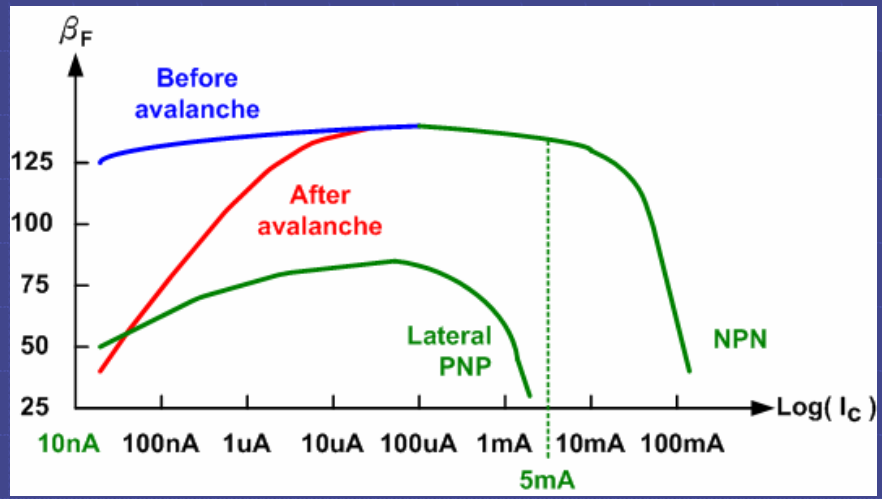
Chapter 5 Layout of Bipolar Transistor

- Bipolar Transistor Operation
- Standard Bipolar Small-Signal Transistors
- Alternative Small-Signal Bipolar Transistors
- Bipolar Transistors in a CMOS Process

Topics in bipolar transistor operation

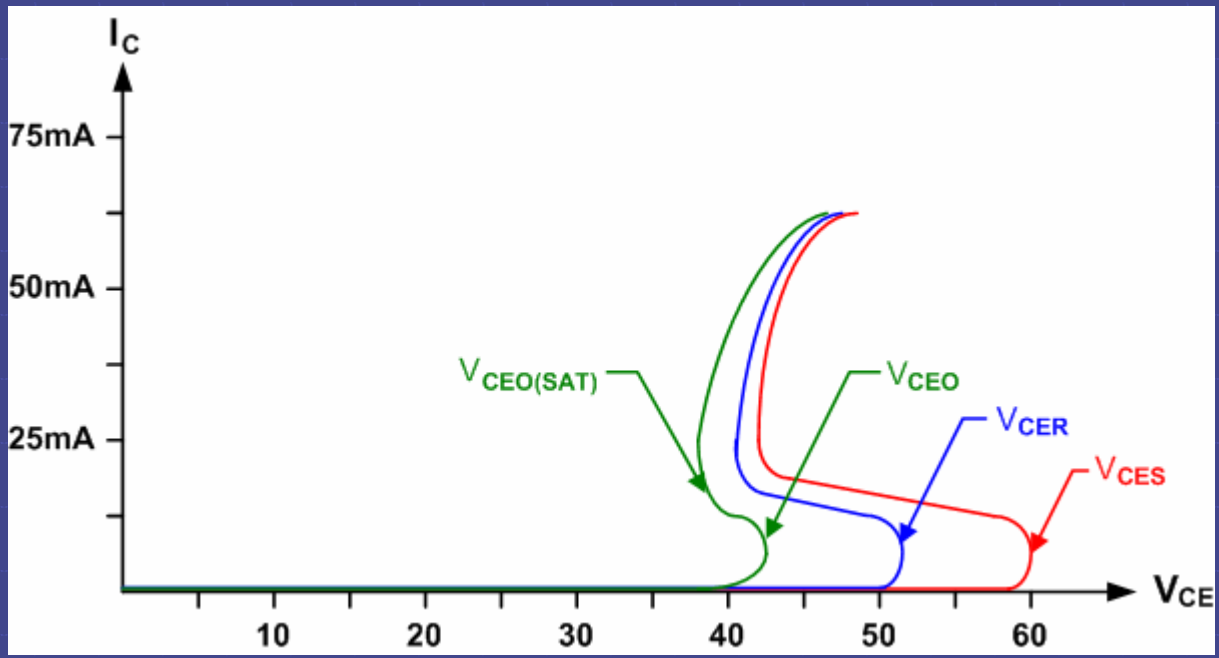


Simplified three-terminal model of an NPN transistor.

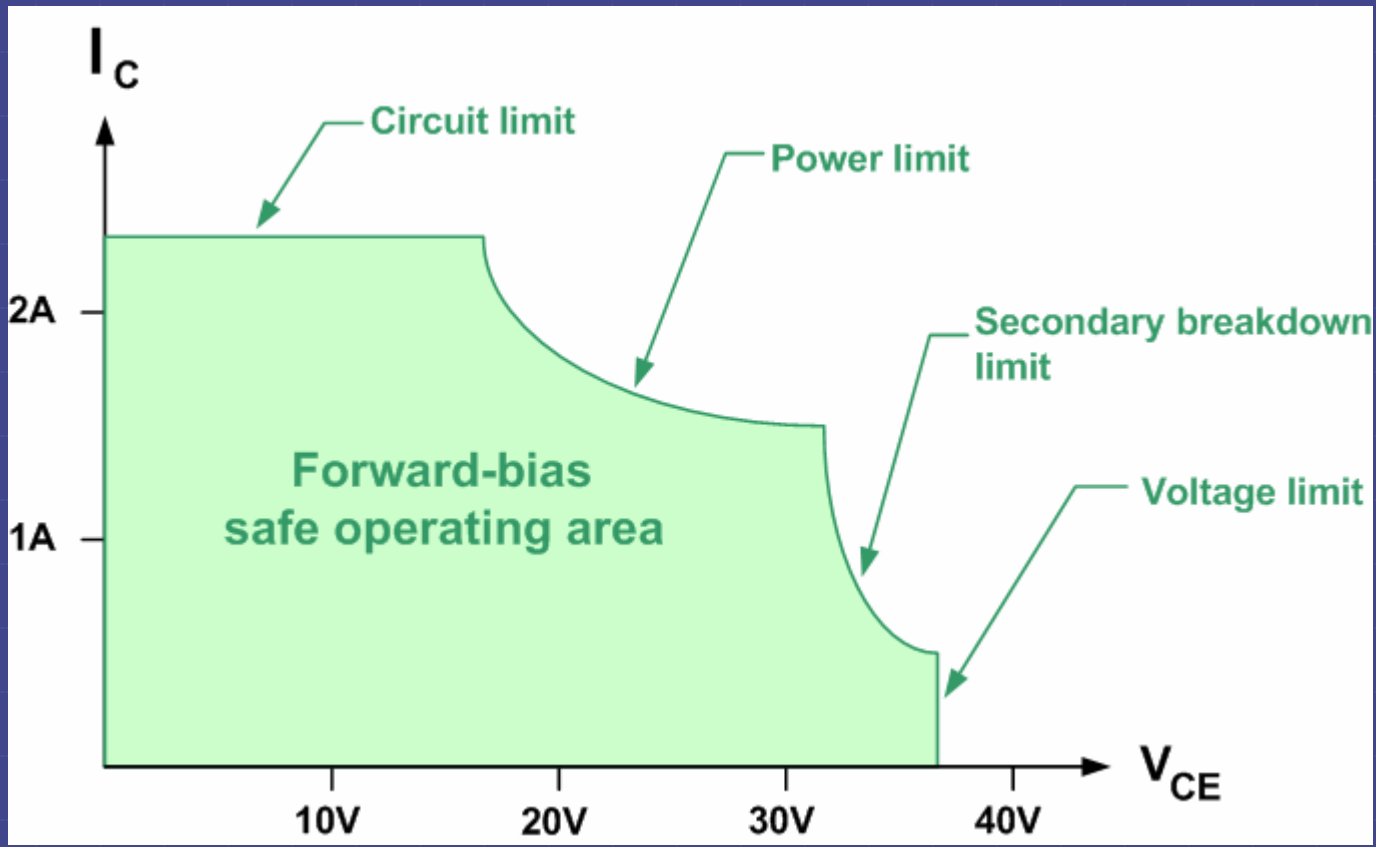


Beta versus collector current plots for small-signal NPN and lateral PNP transistors. The curve marked in gray shows the effect of emitter-base avalanche on NPN base.

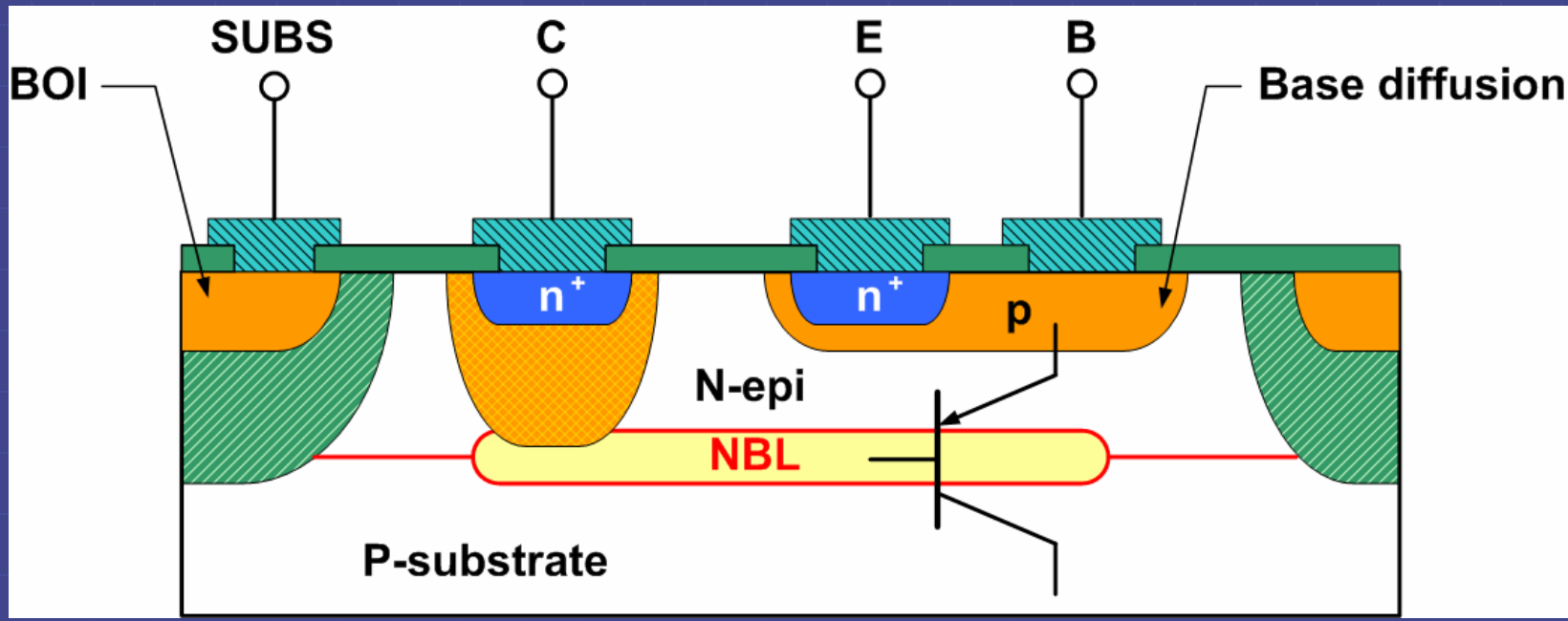
Idealized curve tracer plots of V_{CEO}, V_{CER}, and V_{CES} in an NPN transistor.



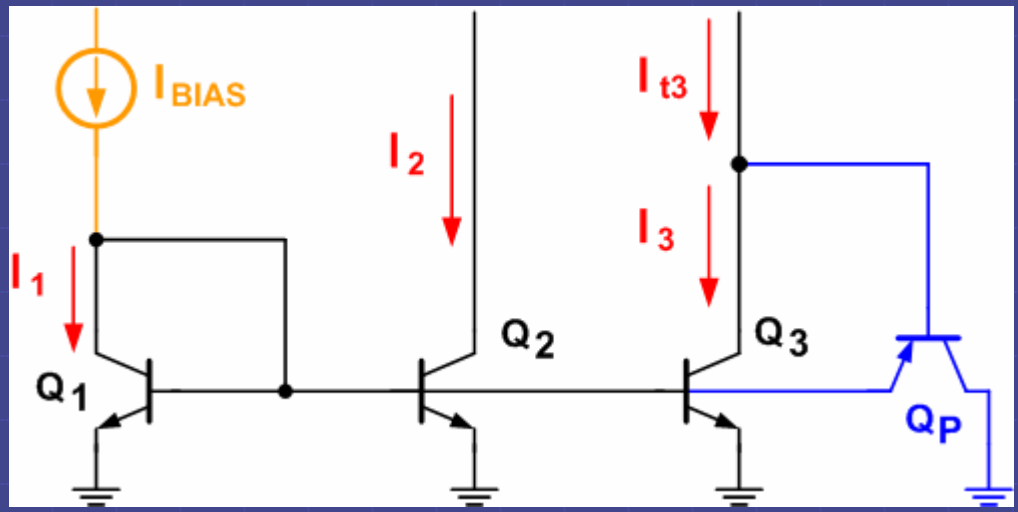
Forward-bias safe operating area (FBSOA) plot of a typical NPN power transistor.



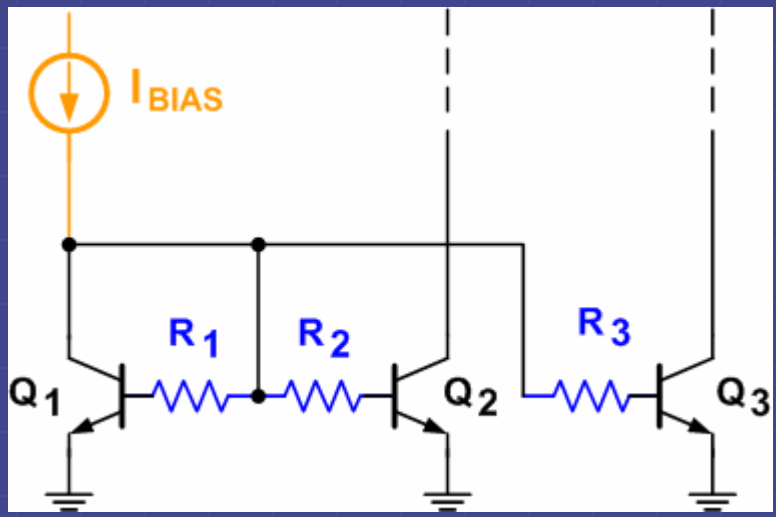
Cross section of an NPN transistor fabricated on a standard bipolar process, showing the parasitic PNP transistor.



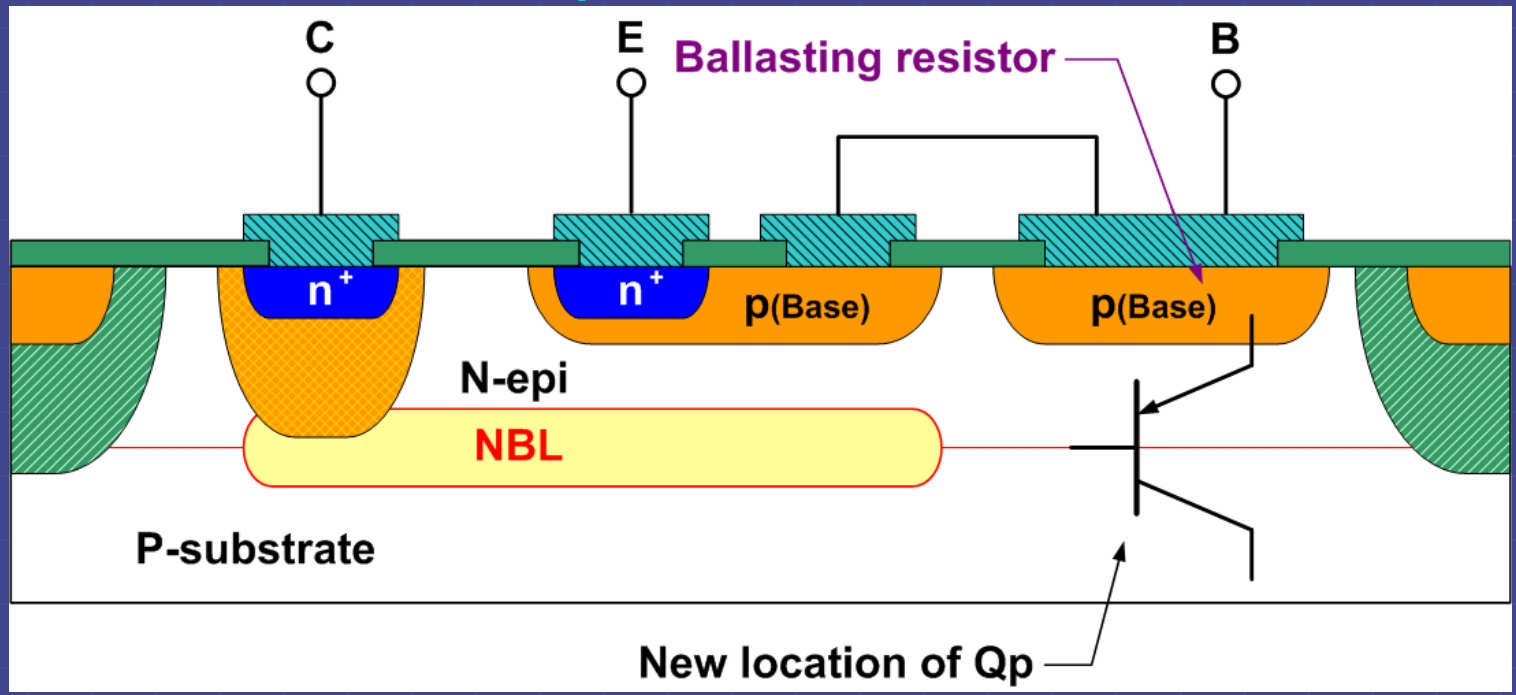
An example of a circuit that exhibits current hogging. Q_P represents the parasitic PNP transistor present in the structure of vertical NPN Q_3.



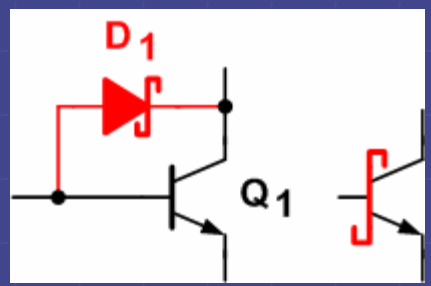
Base-side ballasting applied to the circuit shown above.



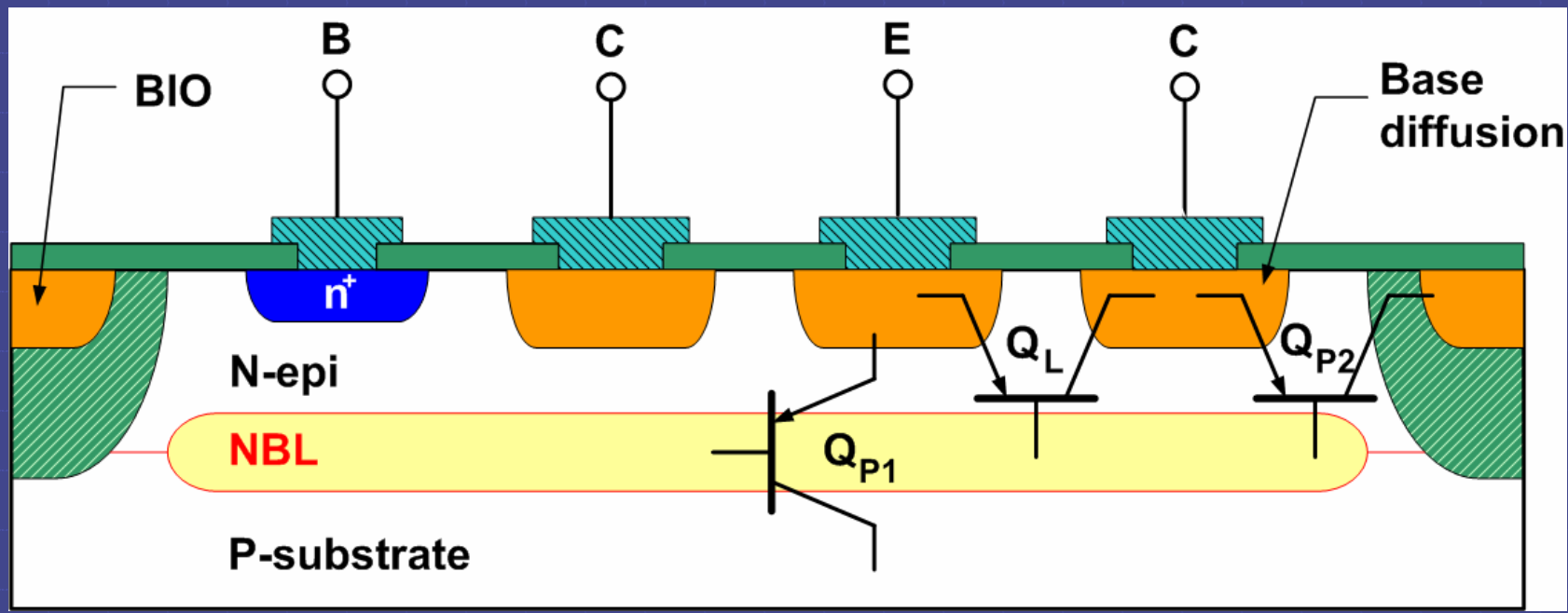
A base-side ballasting resistor becomes ineffective when merged into the same tank as the NPN it protects.



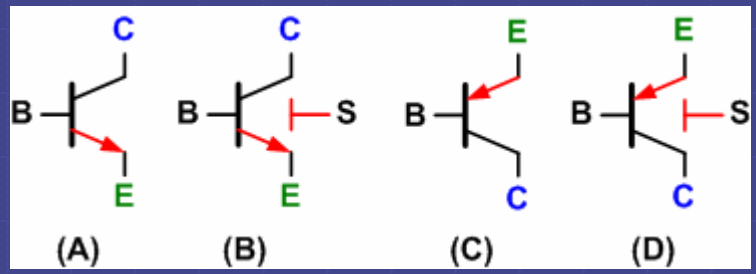
(a) Schottky-clamped NPN transistor and (b) its conventional schematic symbol.



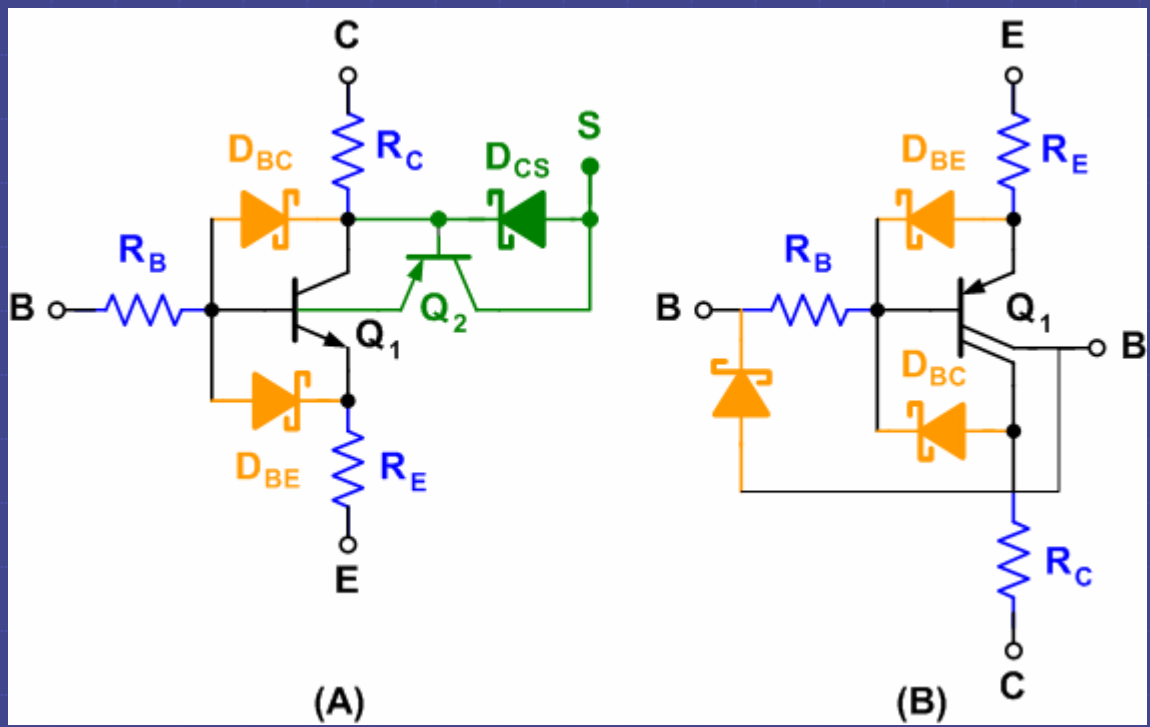
Cross section of a lateral PNP transistor constructed on a standard bipolar process showing parasitic substrate PNP transistors Q_{P1} and Q_{P2}.



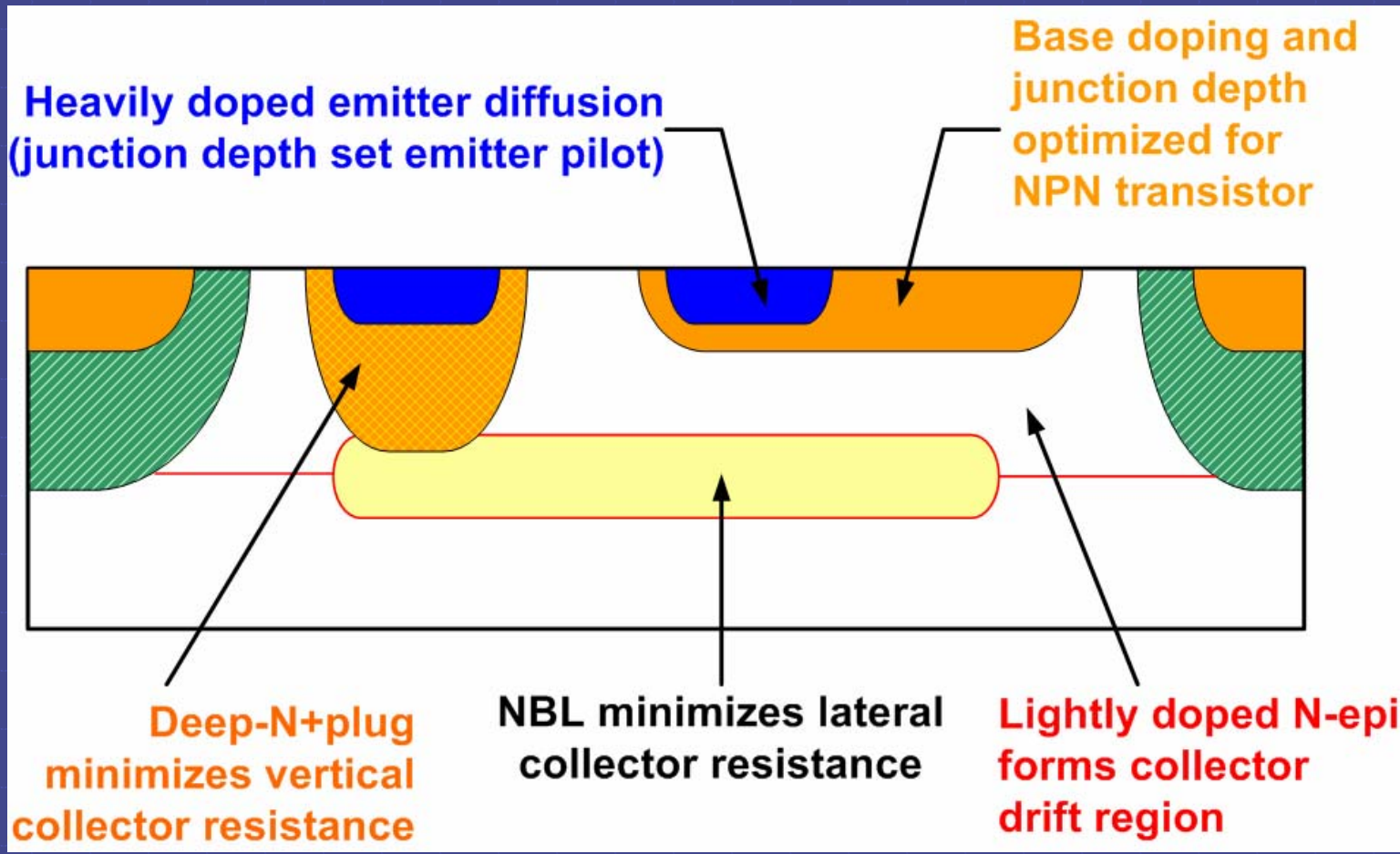
Symbols for three-terminal and four-terminal transistors (E: emitter, B: base, C: collector, S:substrate) .



Subcircuit models for (a) vertical NPN transistor and (b) lateral PNP transistor.

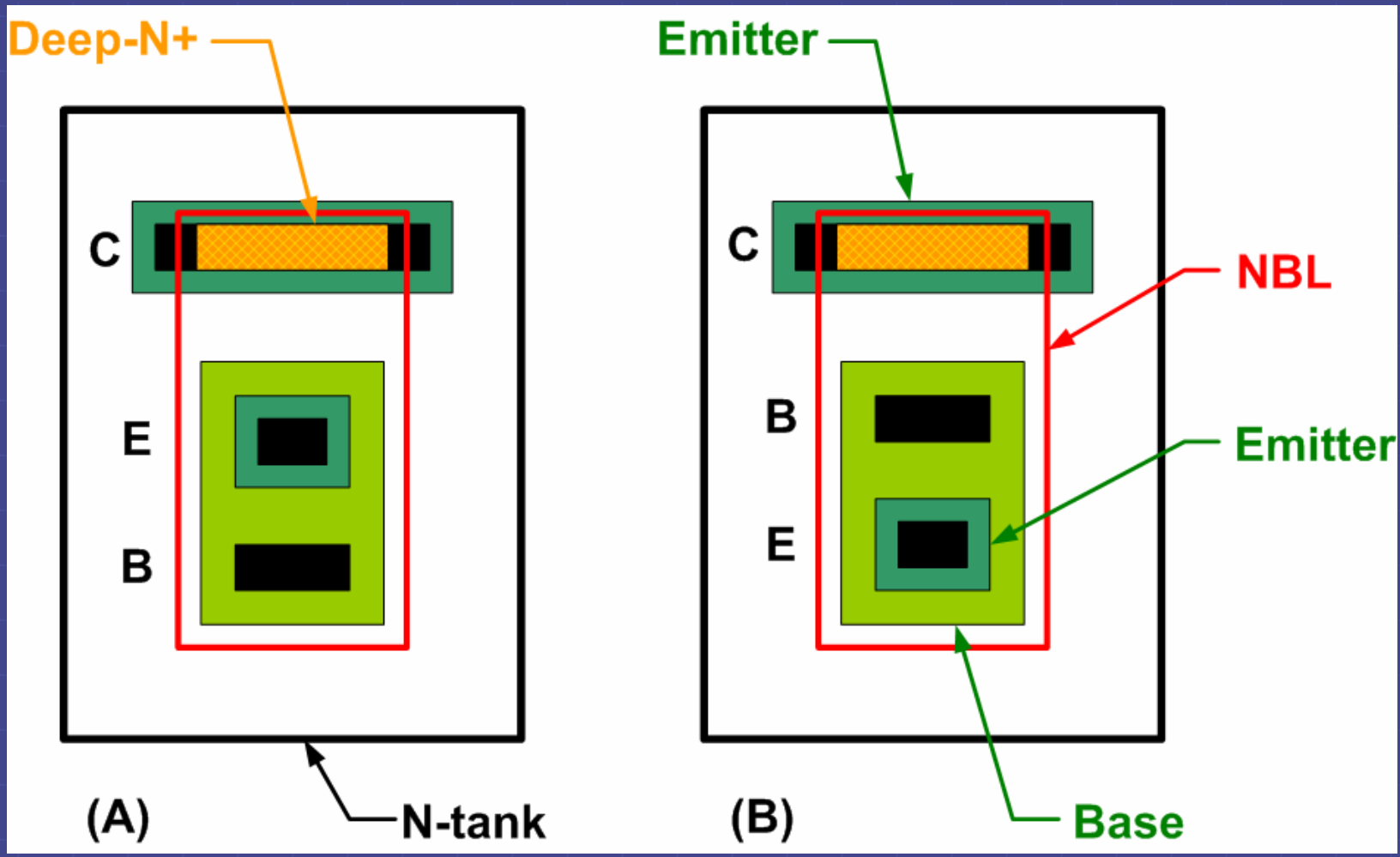


Standard Bipolar Small- Signal Transistors

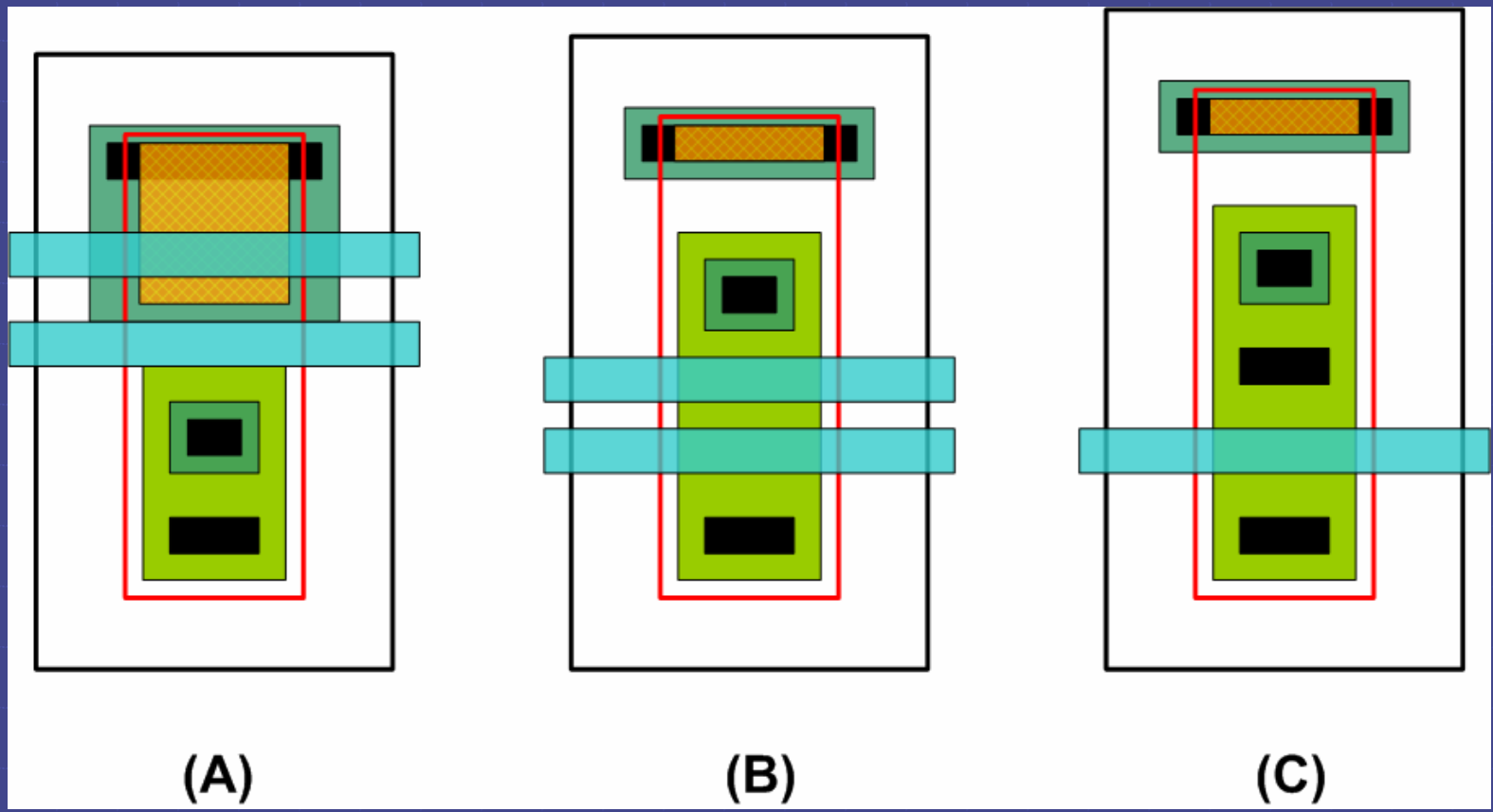


Key features of the standard bipolar vertical NPN transistor.

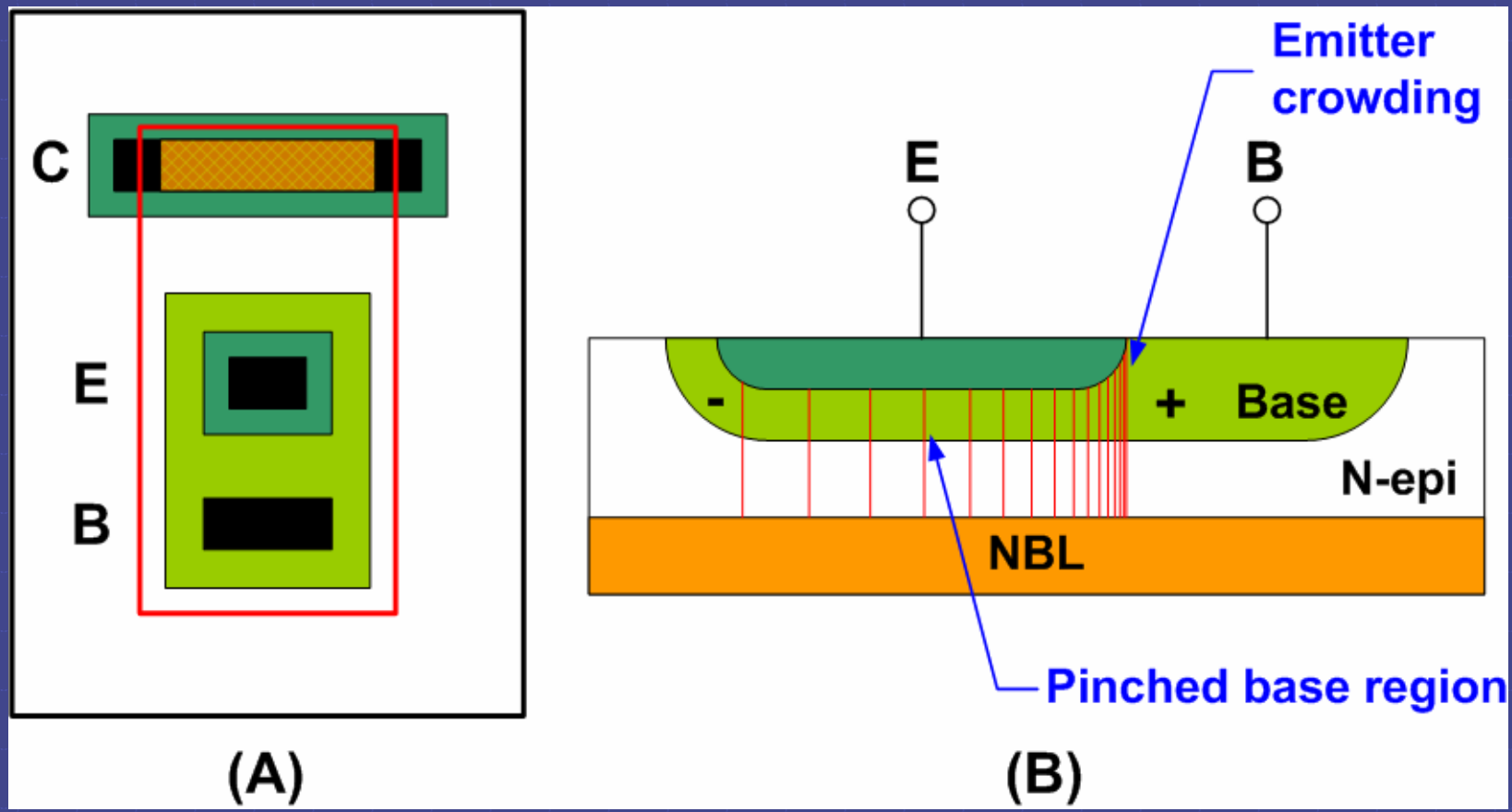
Two styles of NPN transistors: (a) collector- emitter-base (CEB), and (b) collector-base-emitter (CBE).



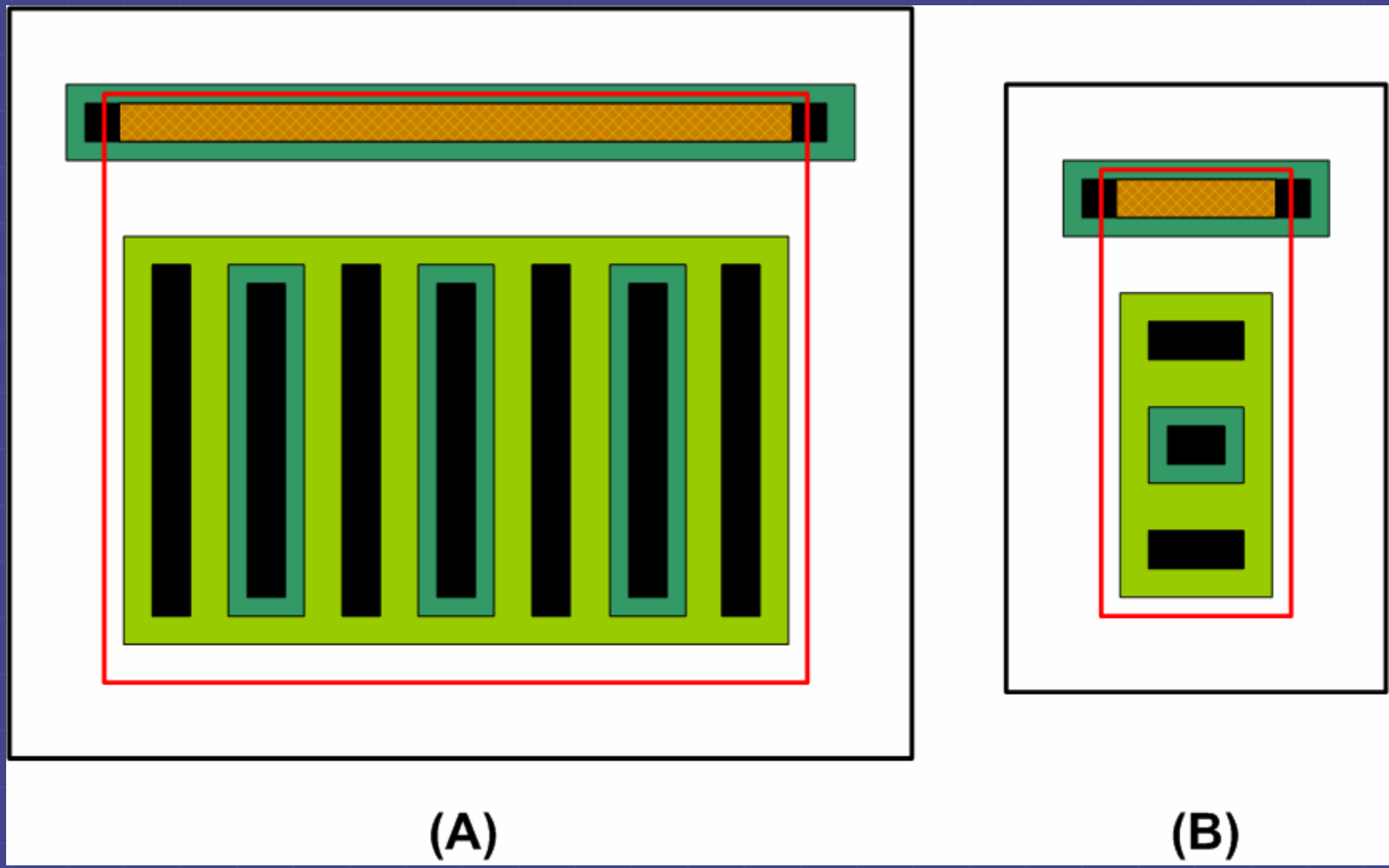
Three examples of stretched NPN transistors.



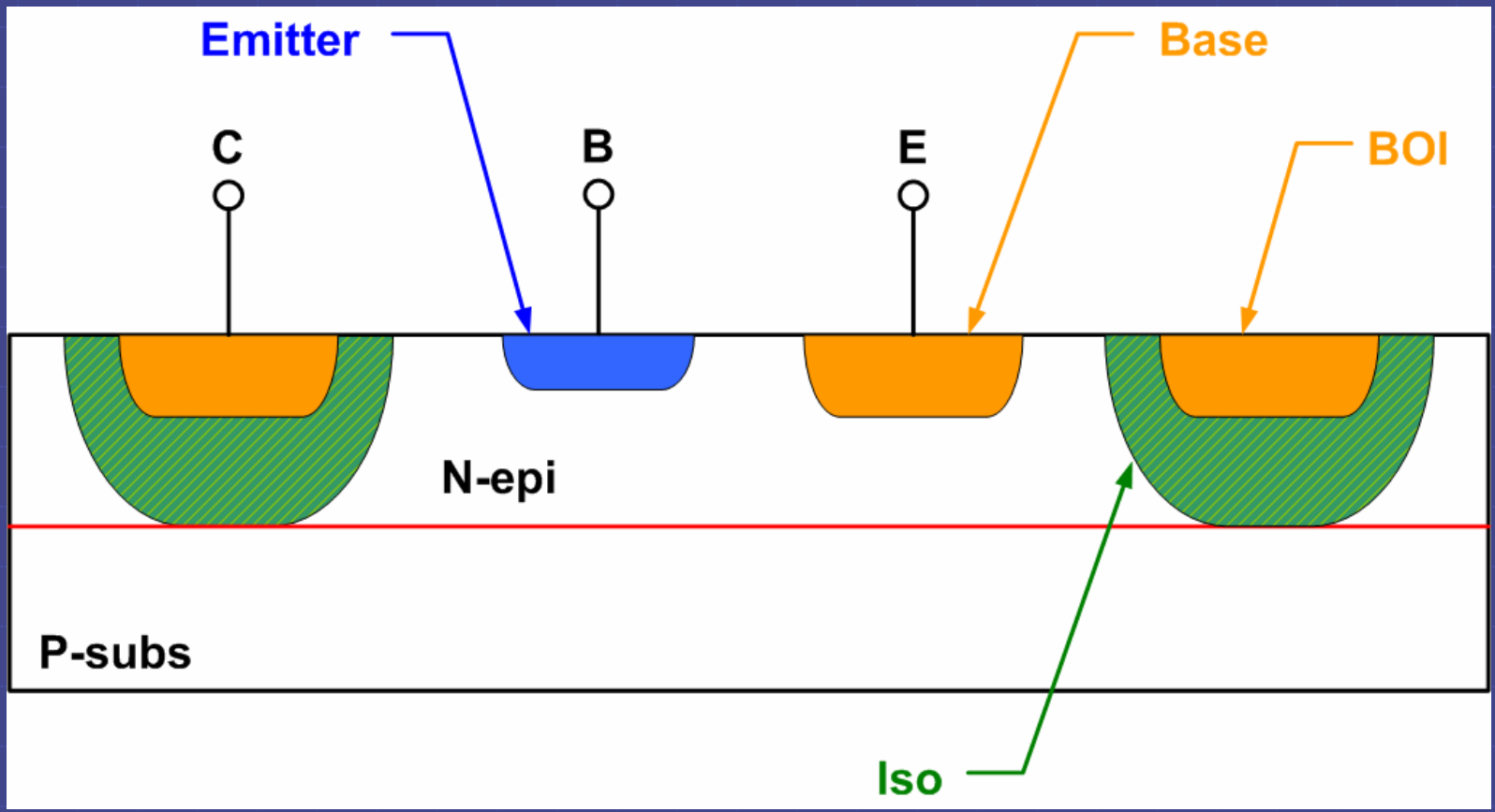
(a) Layout of a compact emitter NPN transistor and (b) a cross section of the active region of this device that illustrates the effects of emitter crowding.



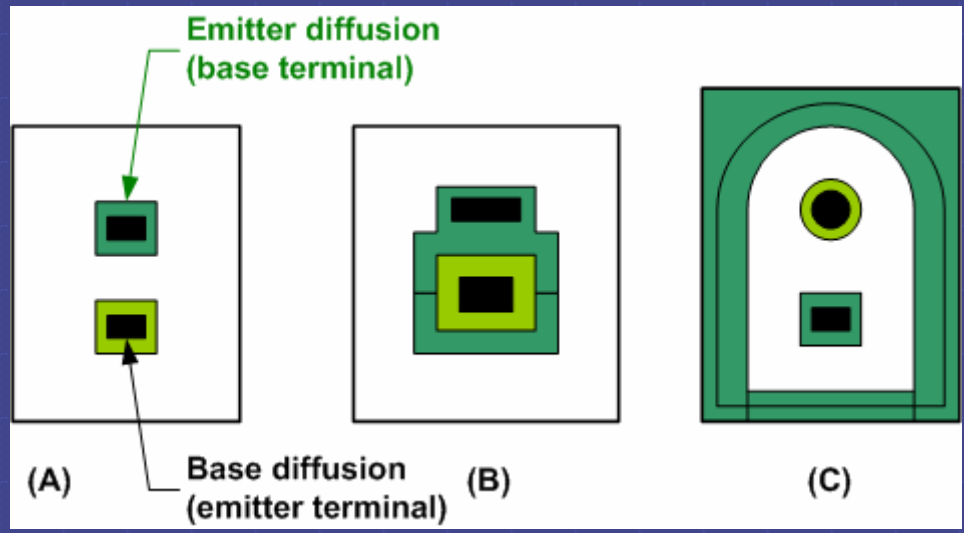
(a) The narrow-emitter transistor and (b) its equivalent minimum-size layout, the double-base transistor.

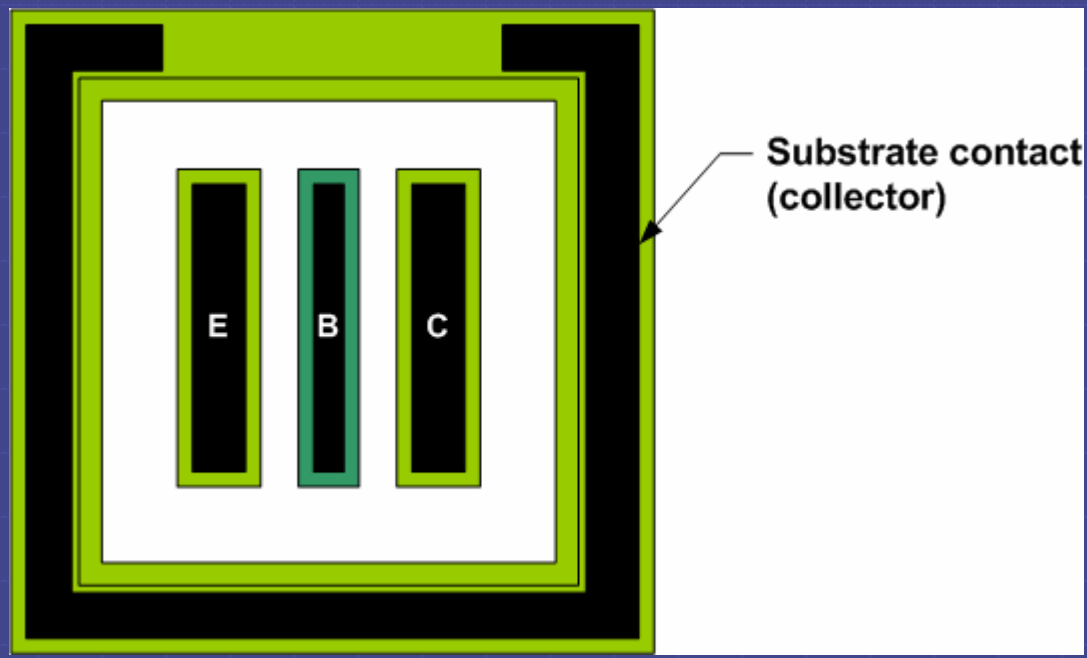


Cross section of a typical substrate PNP transistor fabricated in standard bipolar.



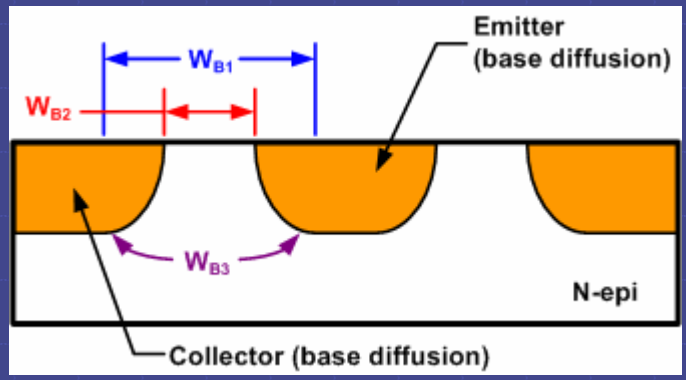
Example of (a) standard, (b) emitter-ringed, and (c) verti-lat styles of substrate PNP transistor.

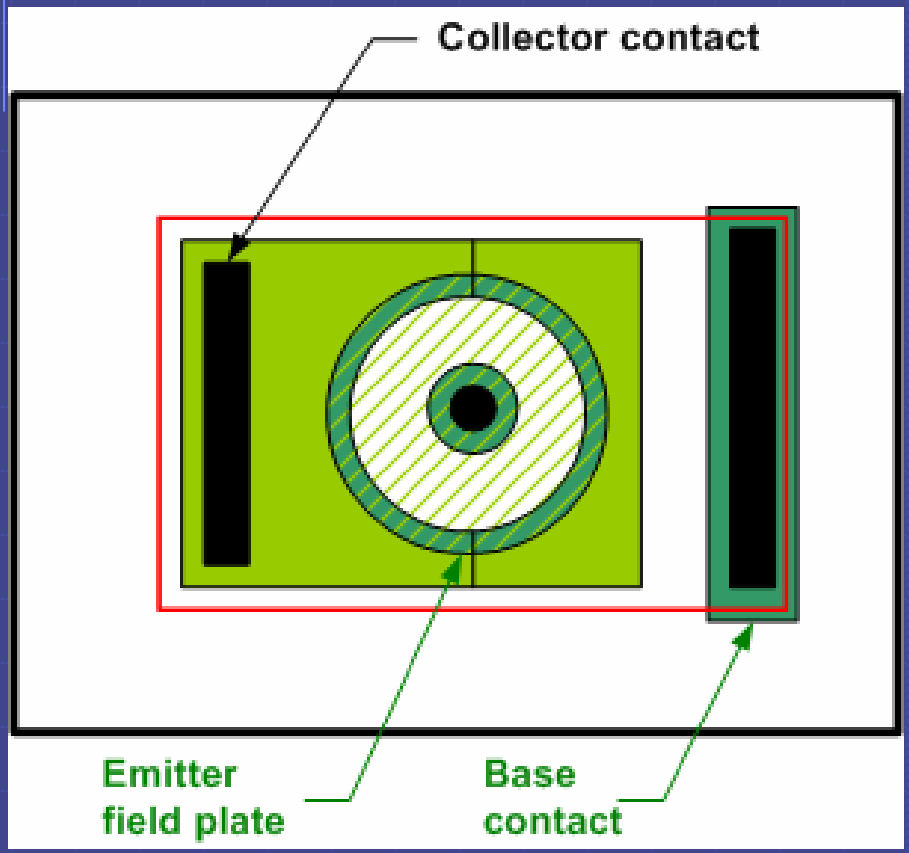




Higher-current substrate PNP transistor employing two wide emitter stripes and a single narrow base stripe.

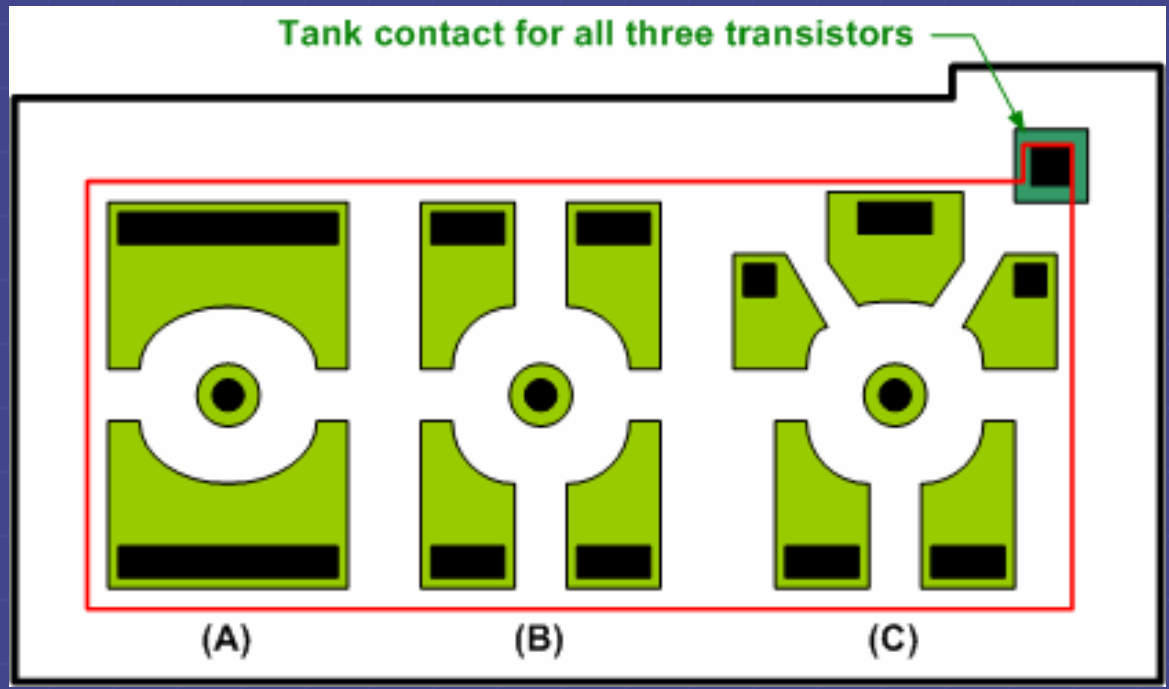
Cross section of a lateral PNP transistor depicting three different measures of neutral base width discussed in the text (drawn base width, W_{B1}, actual base width at the surface, W_{B2}, and effective base width beneath the surface, W_{B3}.



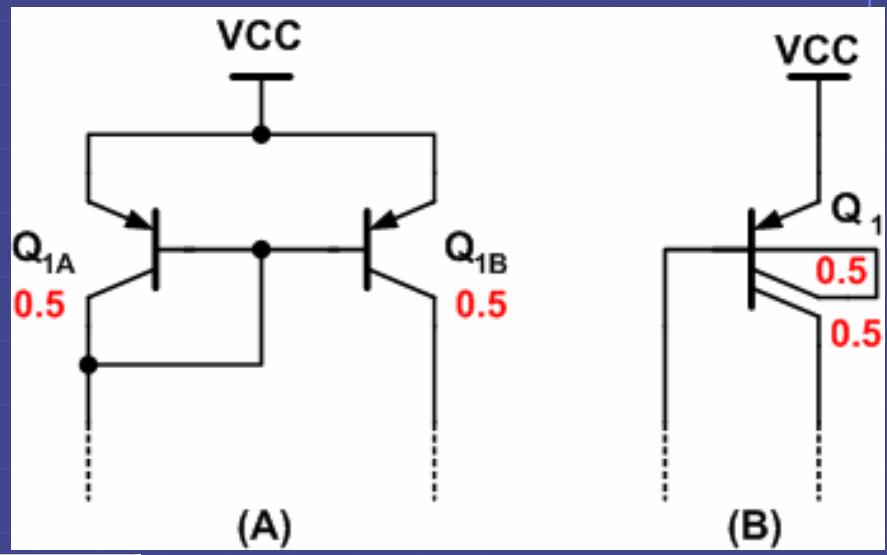


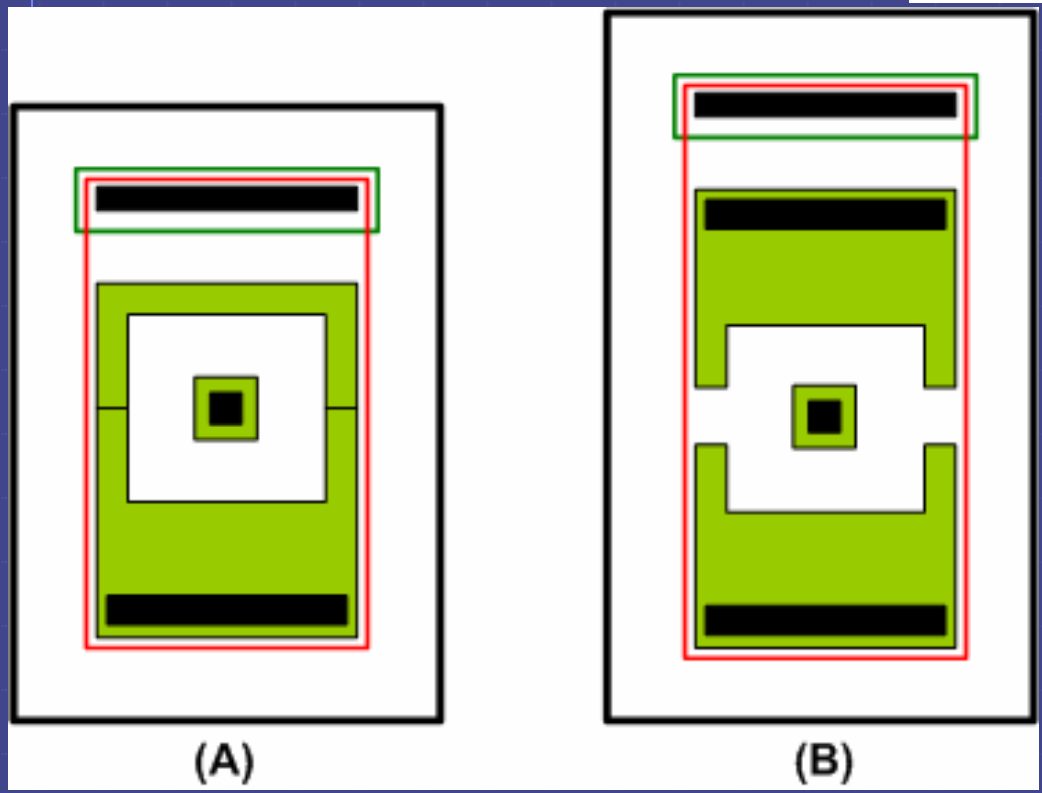
Layout of a lateral PNP transistor showing emitter field plate.

Example of split collector transistors: (a) ½ - ½ (b) ¼ - ¼ - ¼ - ¼ , (c)1/6 – 1/6- 1/6 - ¼ - ¼ . The field plates have been omitted for clarity.



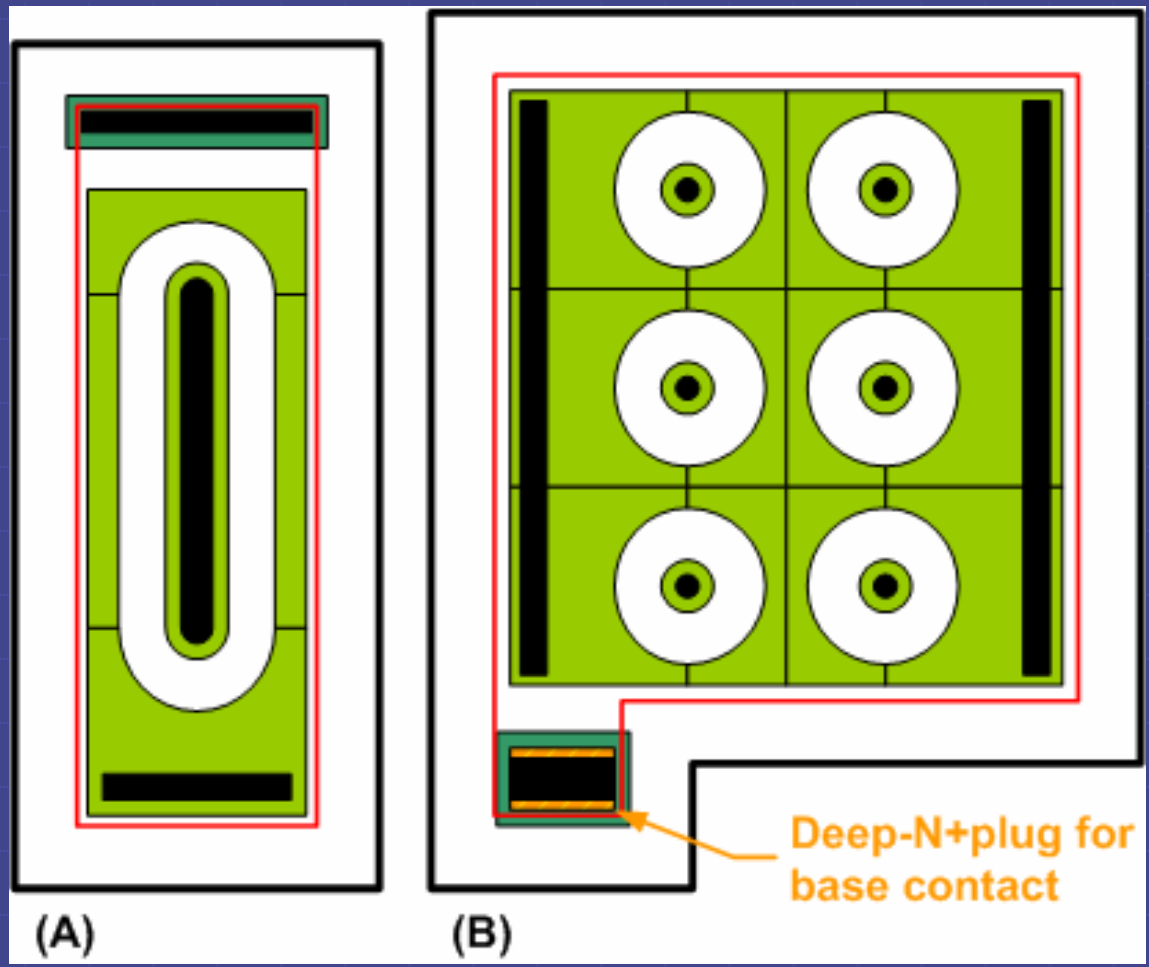
Schematic diagrams for 1:1 current mirrors constructed using split collector lateral PNP transistors: (a) conventional schematic diagram and (b) simplified schematic diagram.



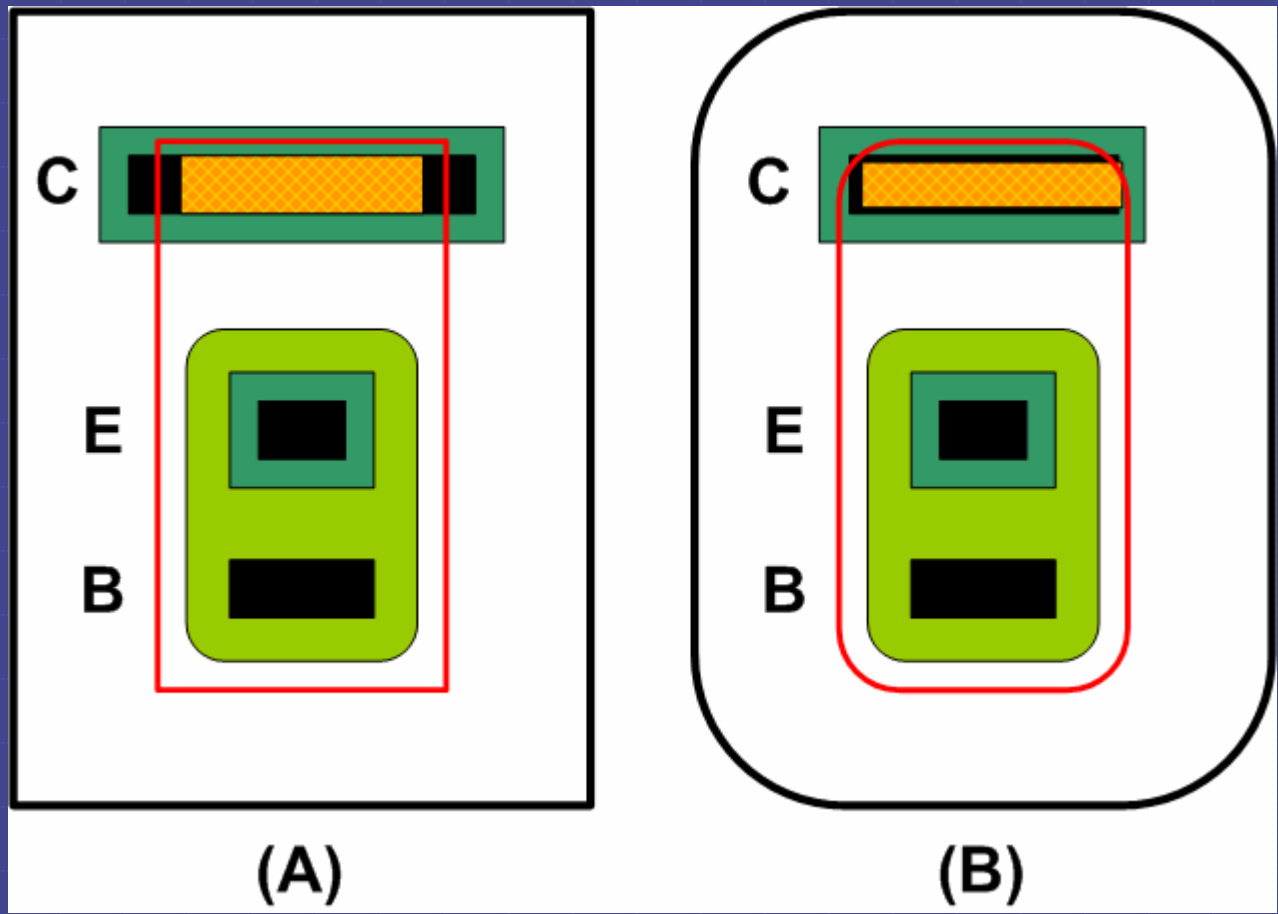


Square geometry lateral PNP transistors: (a) minimum-emitter and (b) ½- ½ split collector. The field plates have been omitted for clarity.

Higher-current lateral PNP transistors: (a) elongated-emitter or hotdog transistor and (b) a small arrayed-emitter transistor.

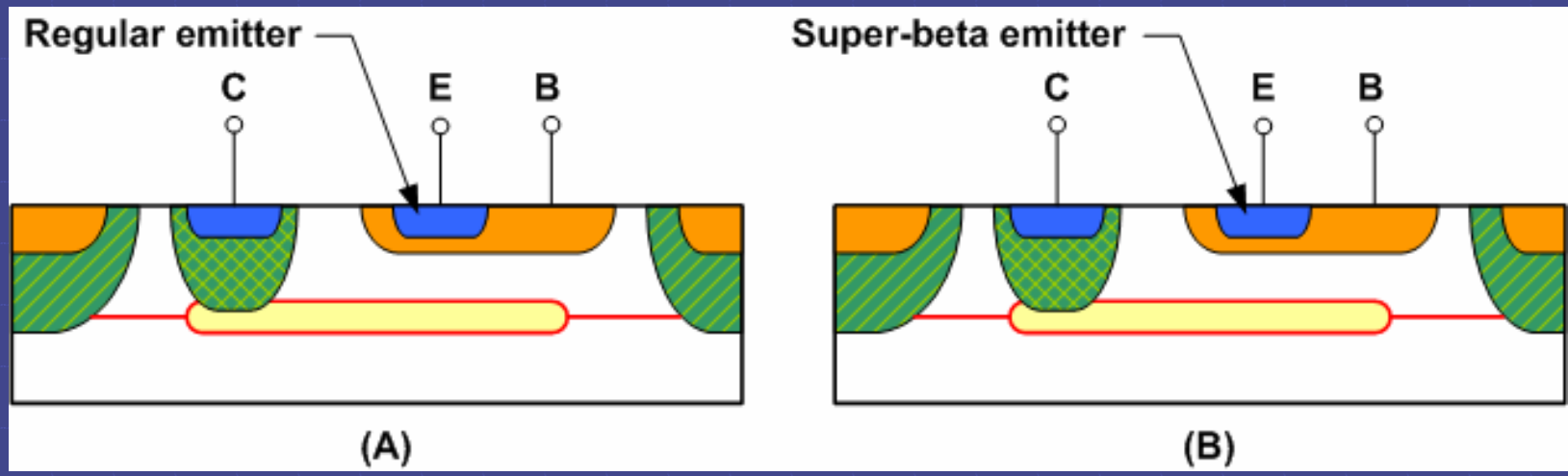


High-voltage Bipolar Transistors

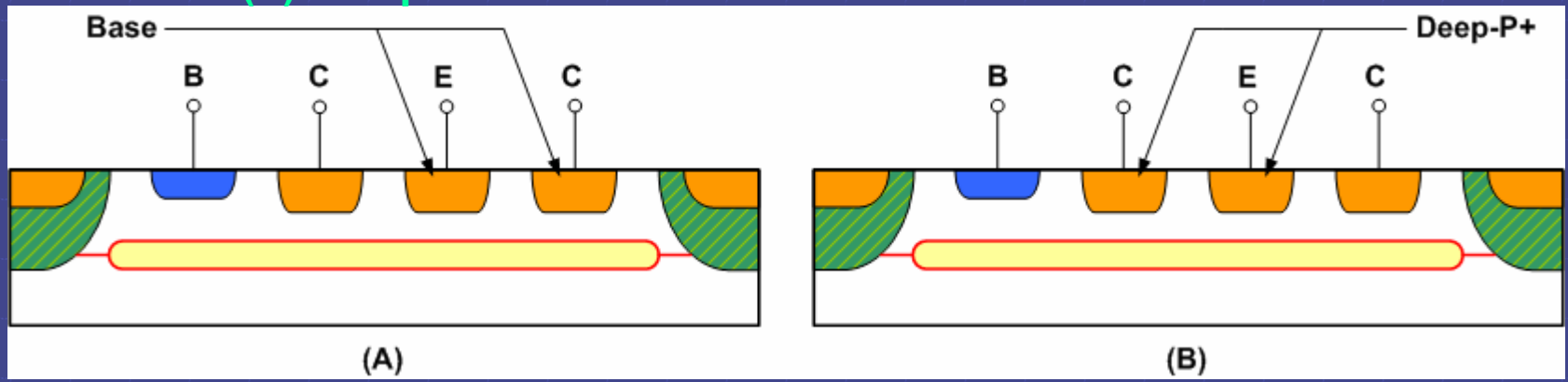


NPN transistors incorporating high-voltage fillets (a) on base only and (b) on base, NBL, and isolation.

Alternative Small-Signal Bipolar Transistors

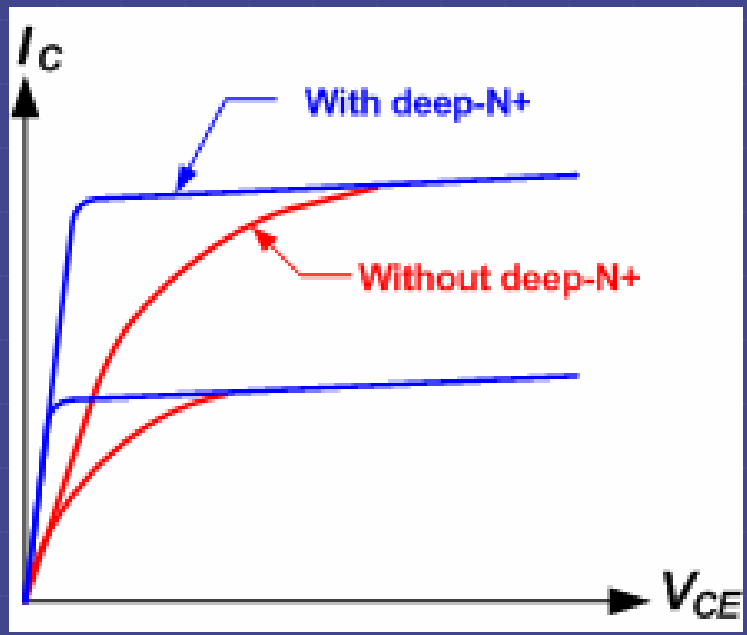


Comparison of representative cross sections of (a) a standard bipolar NPN and (b) a super-beta NPN.

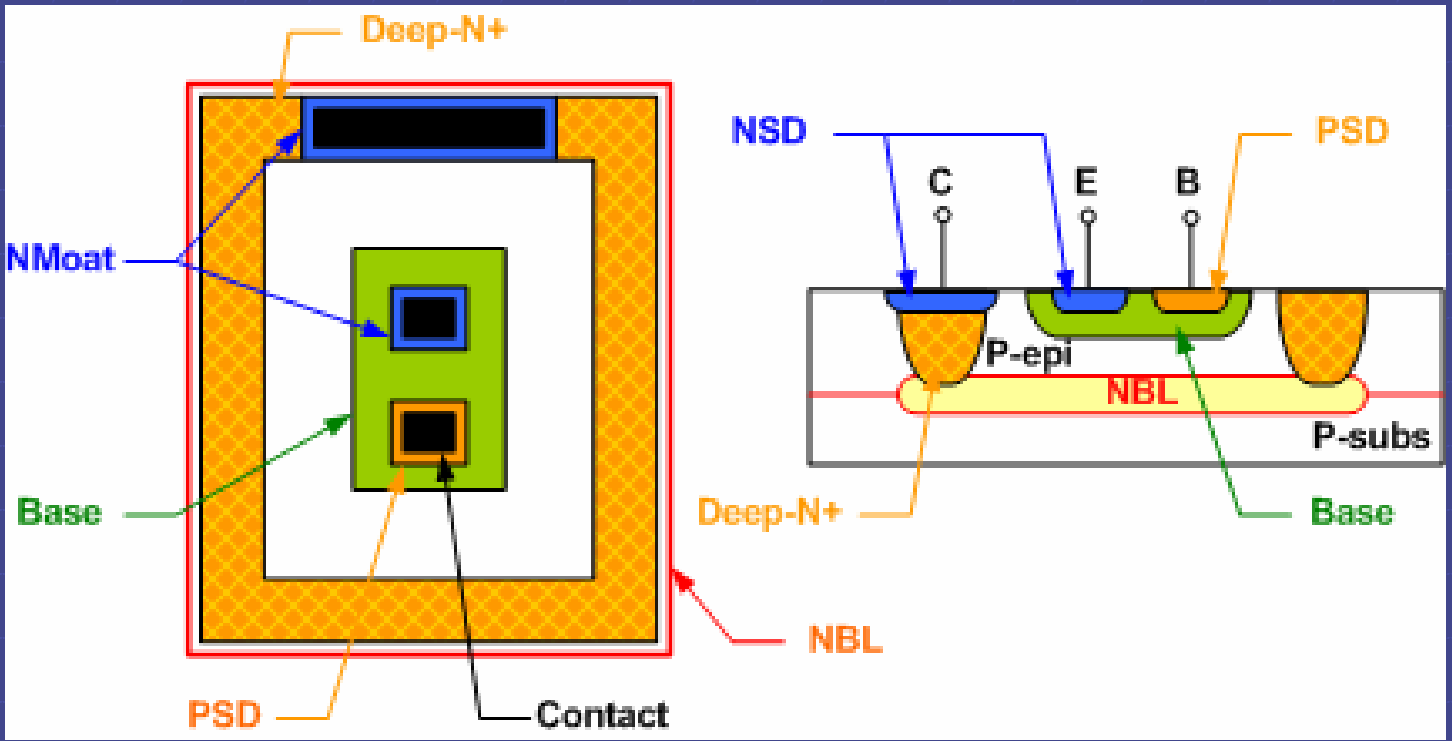


Comparison of representative cross sections of (a) a standard bipolar lateral PNP and (b) a deep-P+ lateral PNP.

Analog BiCMOS Bipolar Transistors

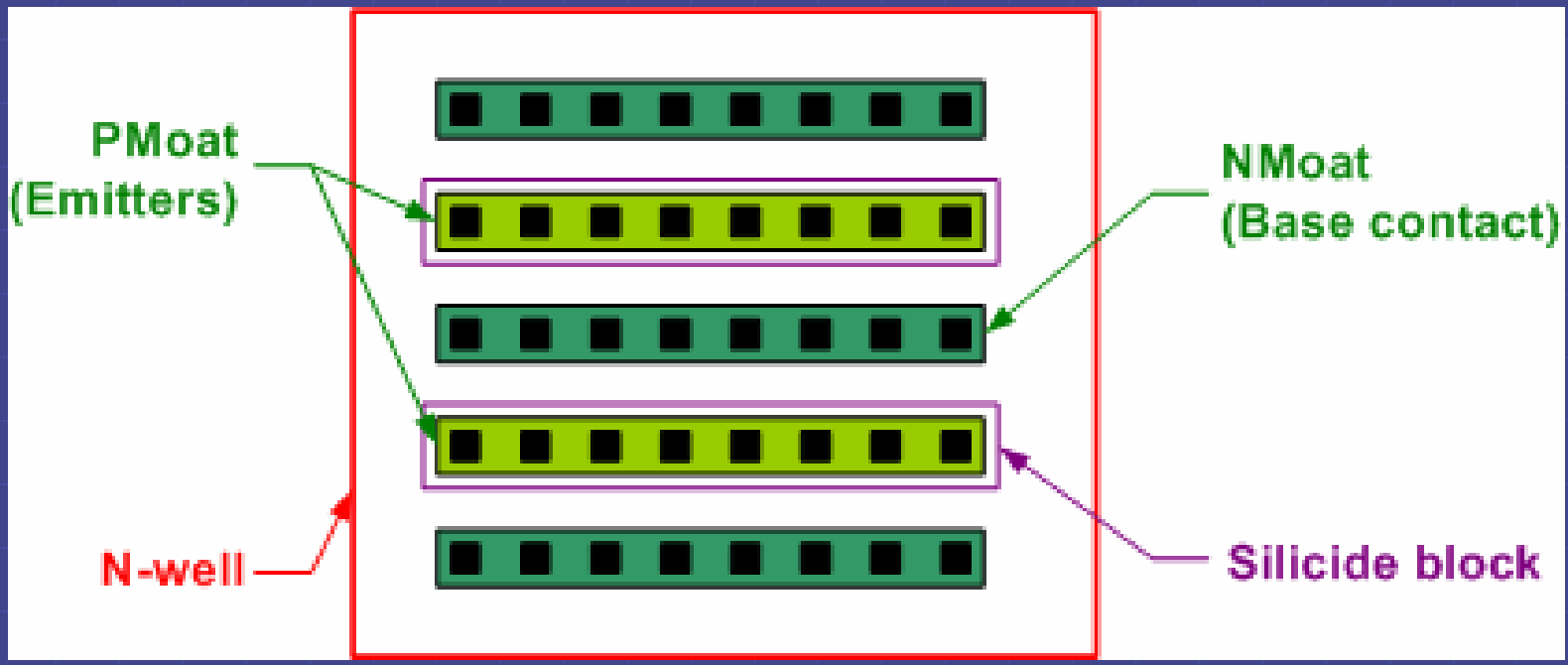


Comparison of saturation characteristics of CDI NPN transistors with and without the addition of deep-N+ sinkers.



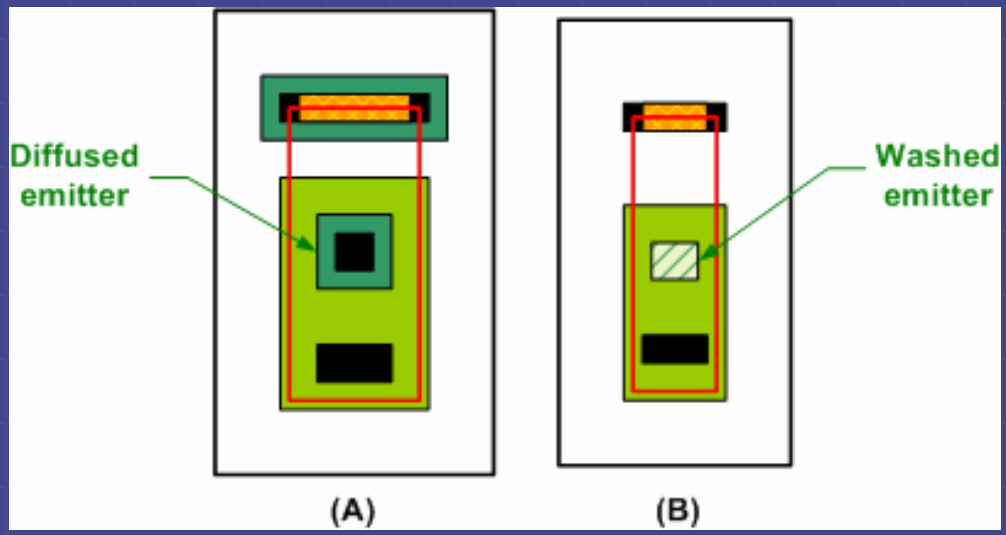
Layout and cross section of an extended- base NPN transistor.

Bipolar Transistors in a CMOS Process

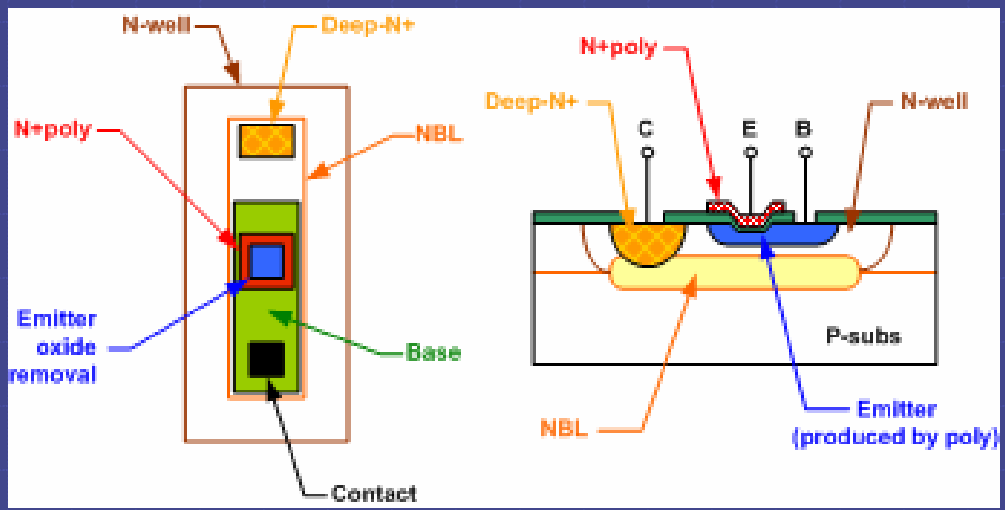


Layout of a substrate PNP transistor compatible with an N-well CMOS process.

Advanced-technology Bipolar Transistors

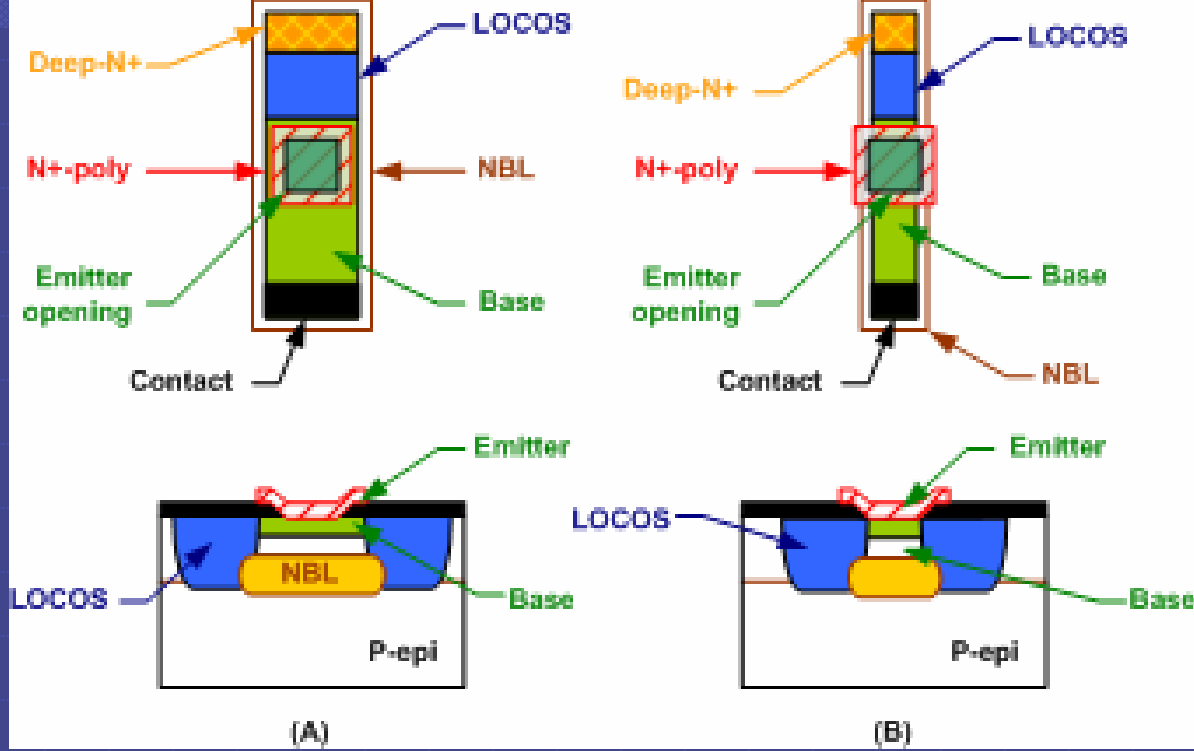


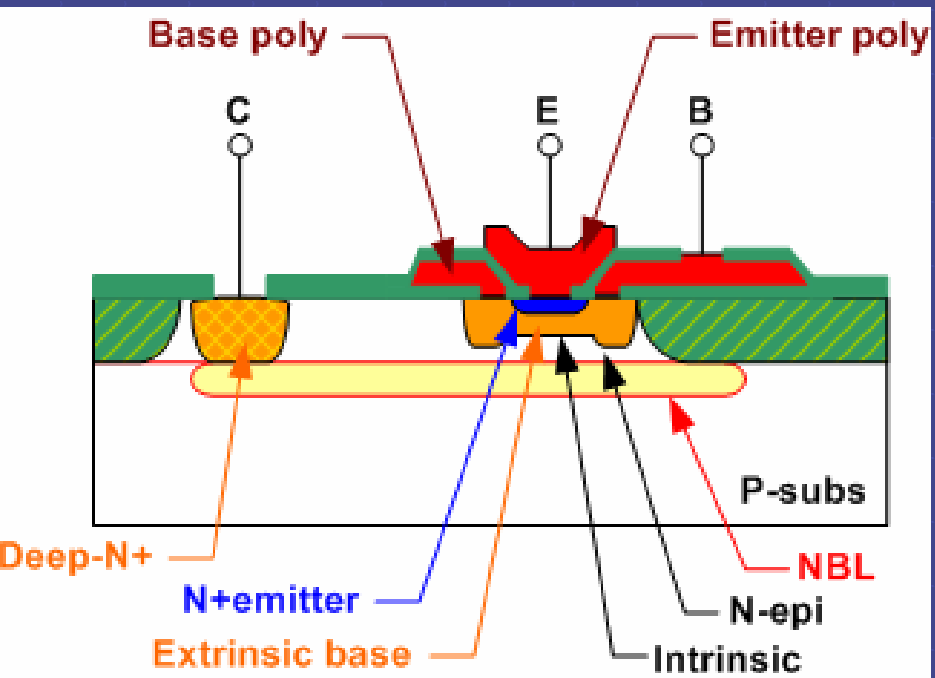
Comparison between (a) a conventional diffused emitter and (b) a washed emitter.



Layout and cross section of a CDI NPN transistor with a polysilicon emitter.

Partial oxide-isolated NPN transistors: (a) conventional , and (b) walled-emitter.

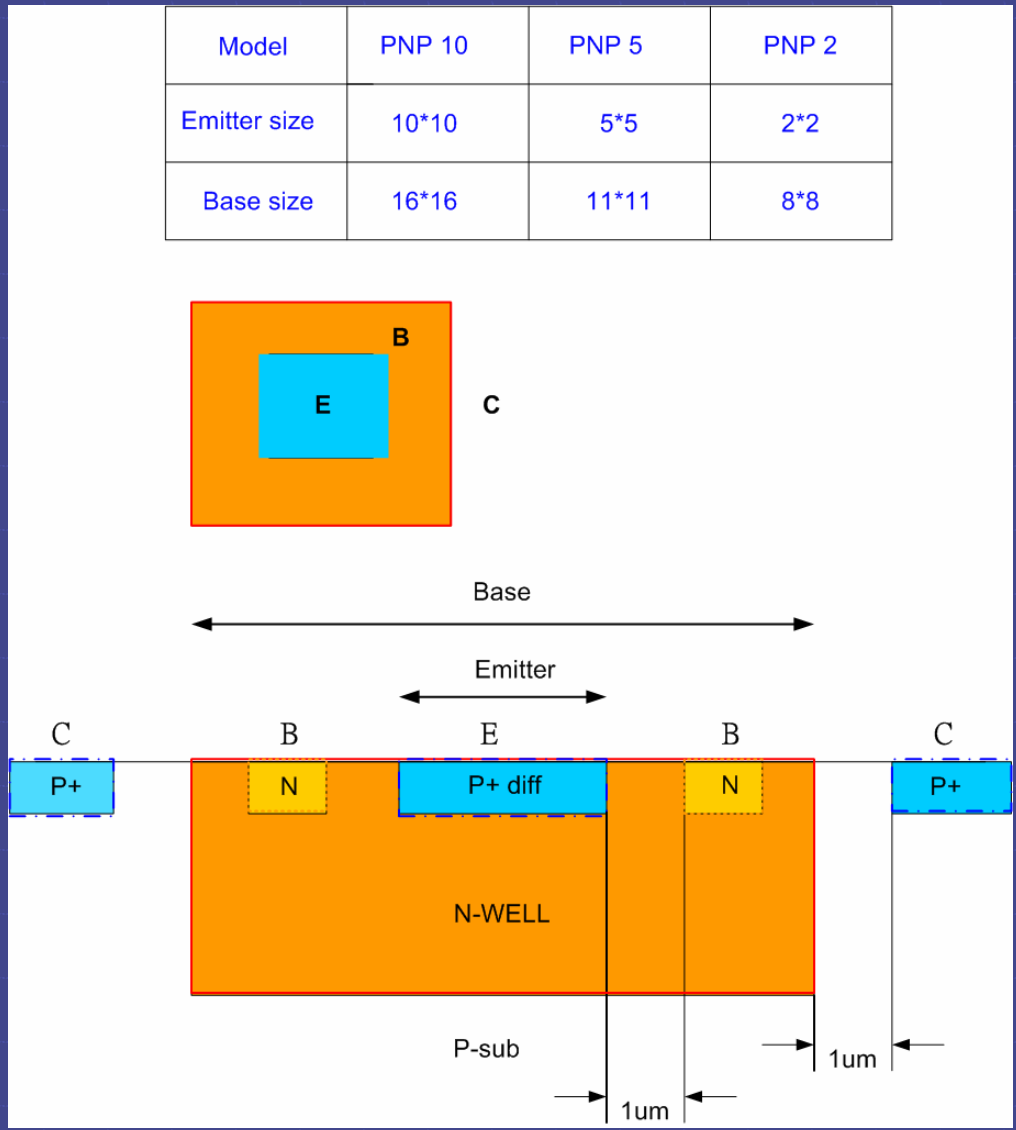




Cross section of a super self-aligned transistor.

Bipolar Gummel-Poon Model

Model	PNP 10	PNP 5	PNP 2
Emitter size	10*10	5*5	2*2
Base size	16*16	11*11	8*8



PNP x 9