Current Mode Logic Divider

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Outline

- Introduction
- Current Mode Logic
- CML Analysis
- Dynamic Current Mode Logic
- Conventional CML DFF
- Super-Dynamic CML D-FF
- Power Efficient CML Divider
- Inductor Peaking for Broadband CMOS CML Logic
- Summary
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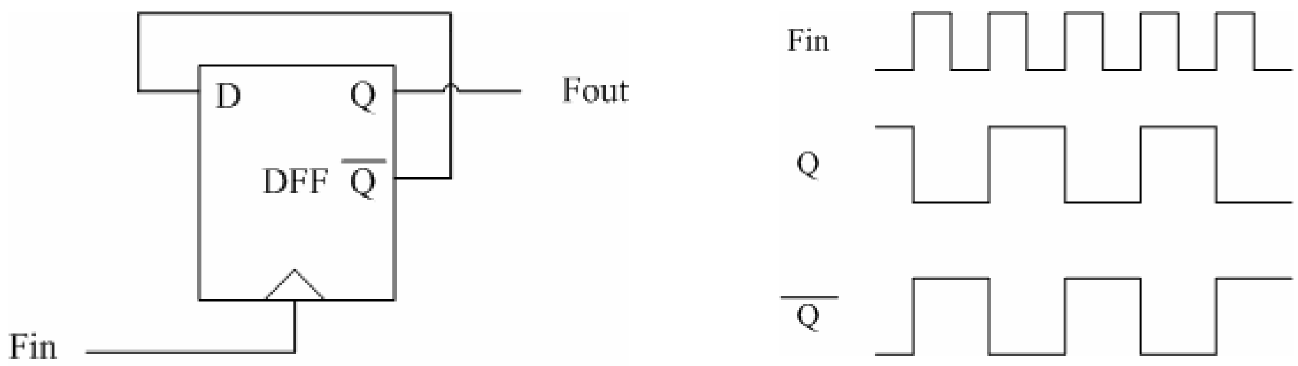
Introduction

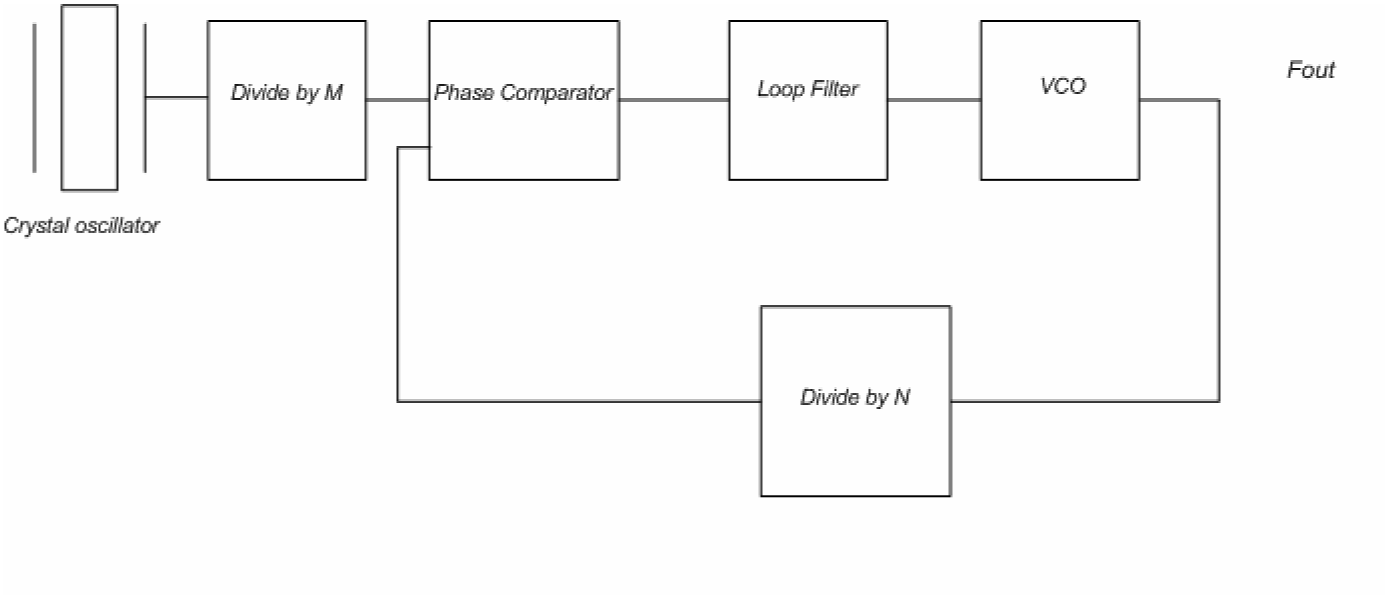
- Three categories
  - Flip-flop-based frequency dividers
  - Injection-locked frequency dividers
  - Regenerative frequency dividers



Flip-flop-based frequency divider

Introduction

- Divider application
  - Behind crystal oscillator to generate desire input signal frequency
  - Divide signal generate by VCO



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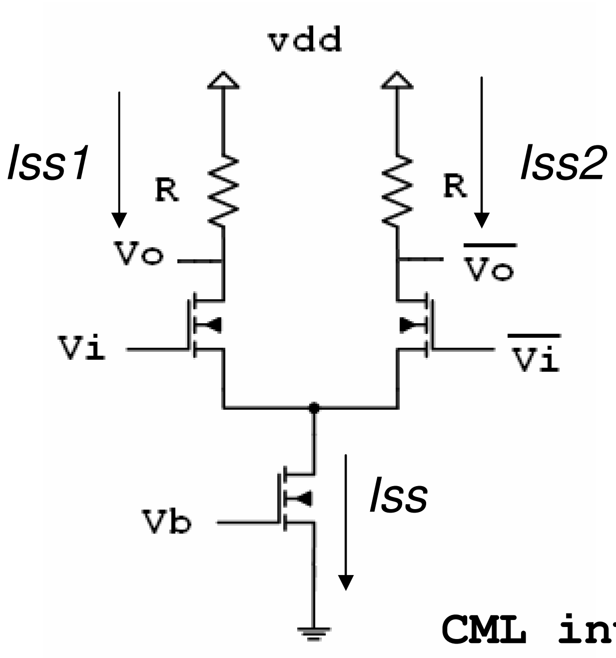
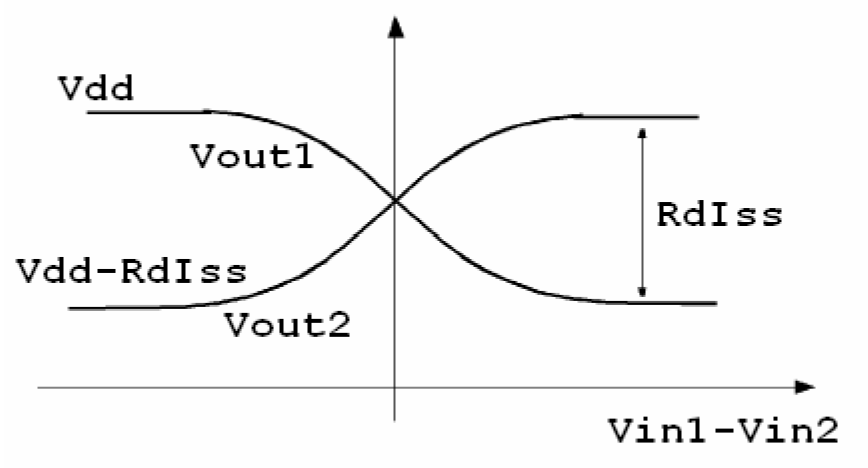
Current Mode Logic

- Differential operation
- Inherent common-mode rejection
- Robust in the presence of common-mode disturbance





CML inverter

CML Analysis

- Common mode voltage

$$V_{gs1} + (V_{GS3} + V_{THN}) \le V_{in,cm} \le \min[VDD - R_D \frac{I_{SS}}{2} + V_{THN}, VDD]$$

- The minimal value is tail current begins to operate in saturation.

- The maximal value of Vcm is M1 or M2 enter the triode region or vdd.

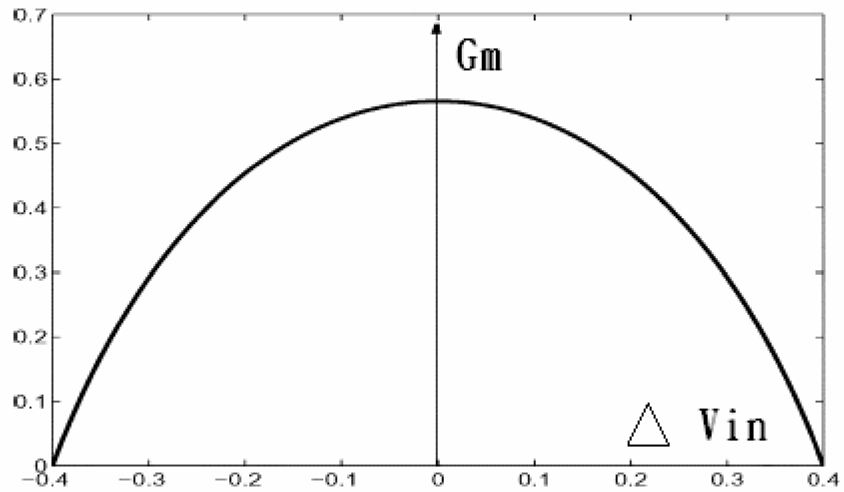
CML Analysis

$$\Delta I_D = I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$$Gm = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}{}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}{}^2}}$$

CML Analysis

$$Gm,avg = \frac{\int_0^{\Delta Vin,\max} Gm(\Delta Vin)d(\Delta Vin)}{\int_0^{\Delta Vin,\max} d(\Delta Vin)} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}I_{SS}}$$



Large-signal G_m as a function of the differential input.

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Dynamic Current Mode Logic

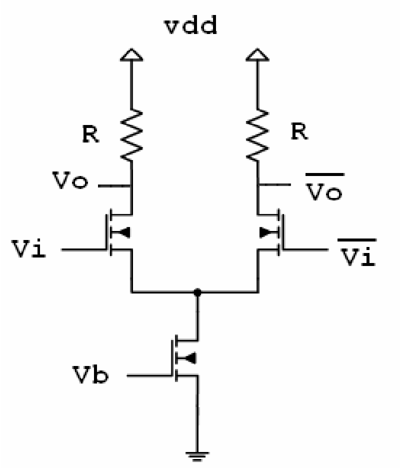
- Achieve the high-speed characteristics of CML, current source and load resistors should be redesigned

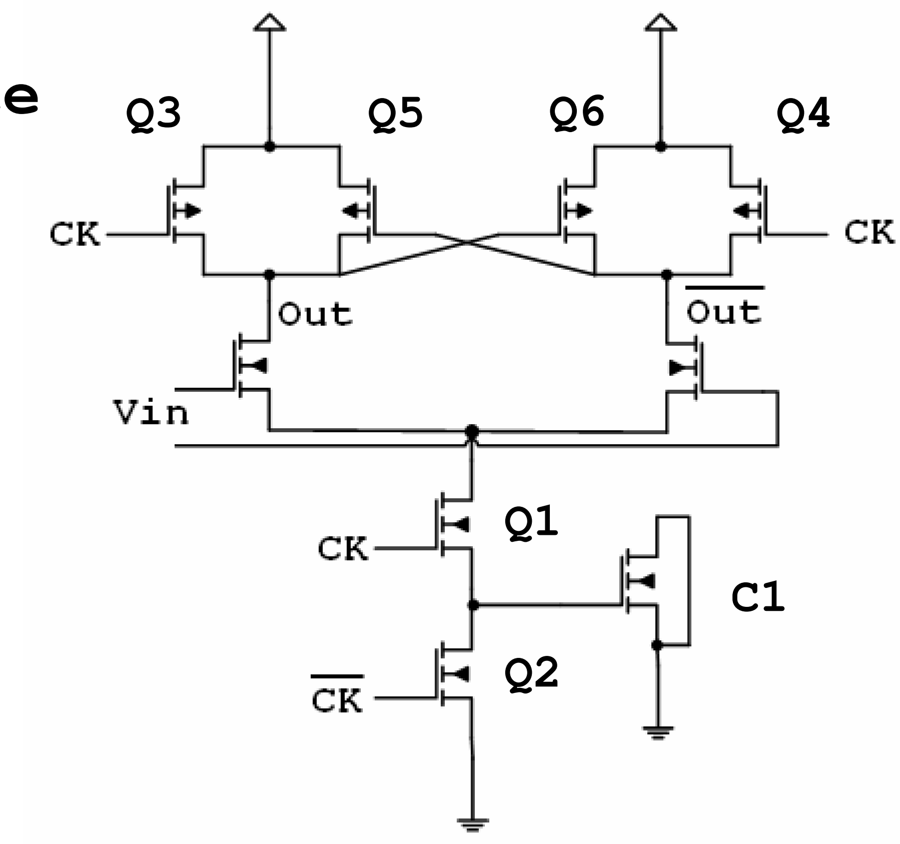
- Dynamic CML employs a dynamic current source with a virtual ground to eliminate the static power

- Use active load, instead of traditional load resistors to reduce power dissipation

Dynamic Current Mode Logic

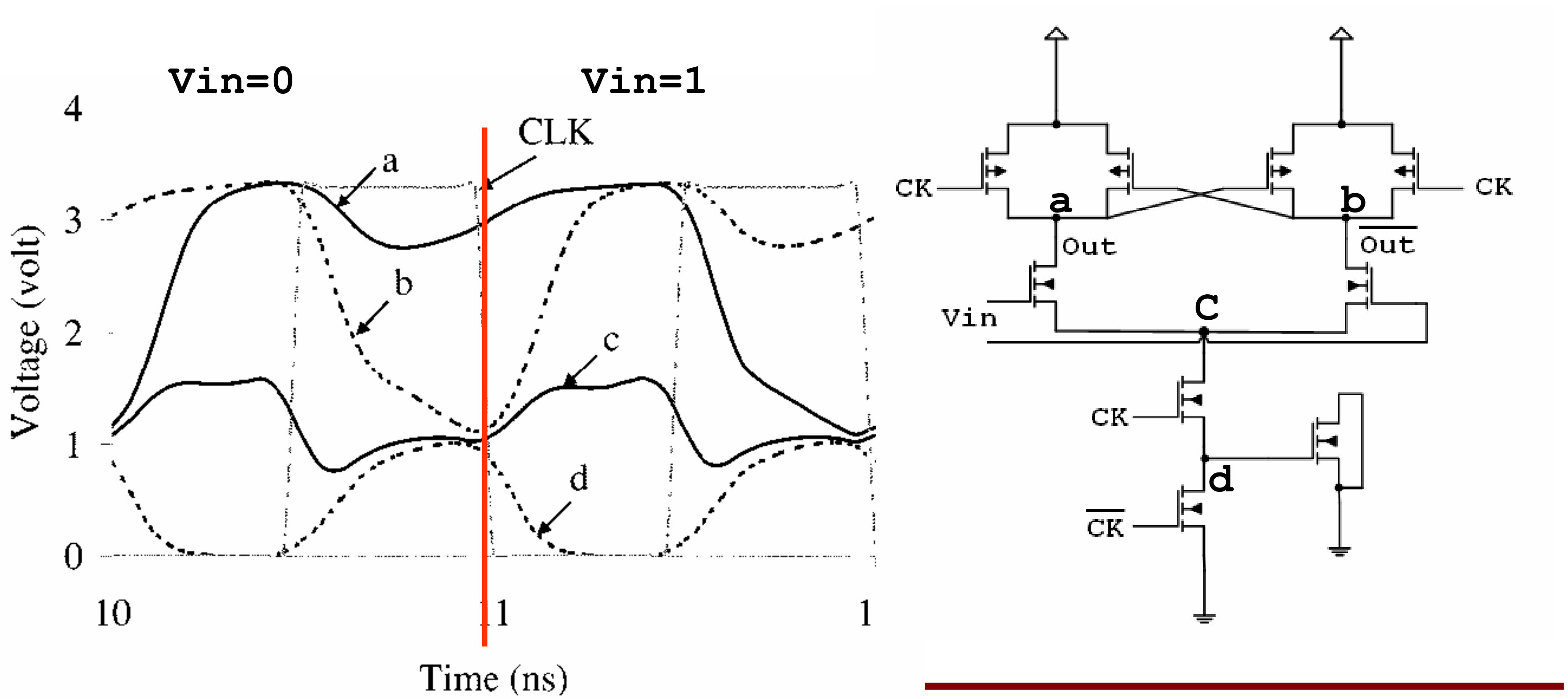
- Precharge circuit
  (Q2,Q3,Q4)
- Dynamic current source
  (Q1,C1)
- Preserve logic value
  after evaluation
  (Q5,Q6)





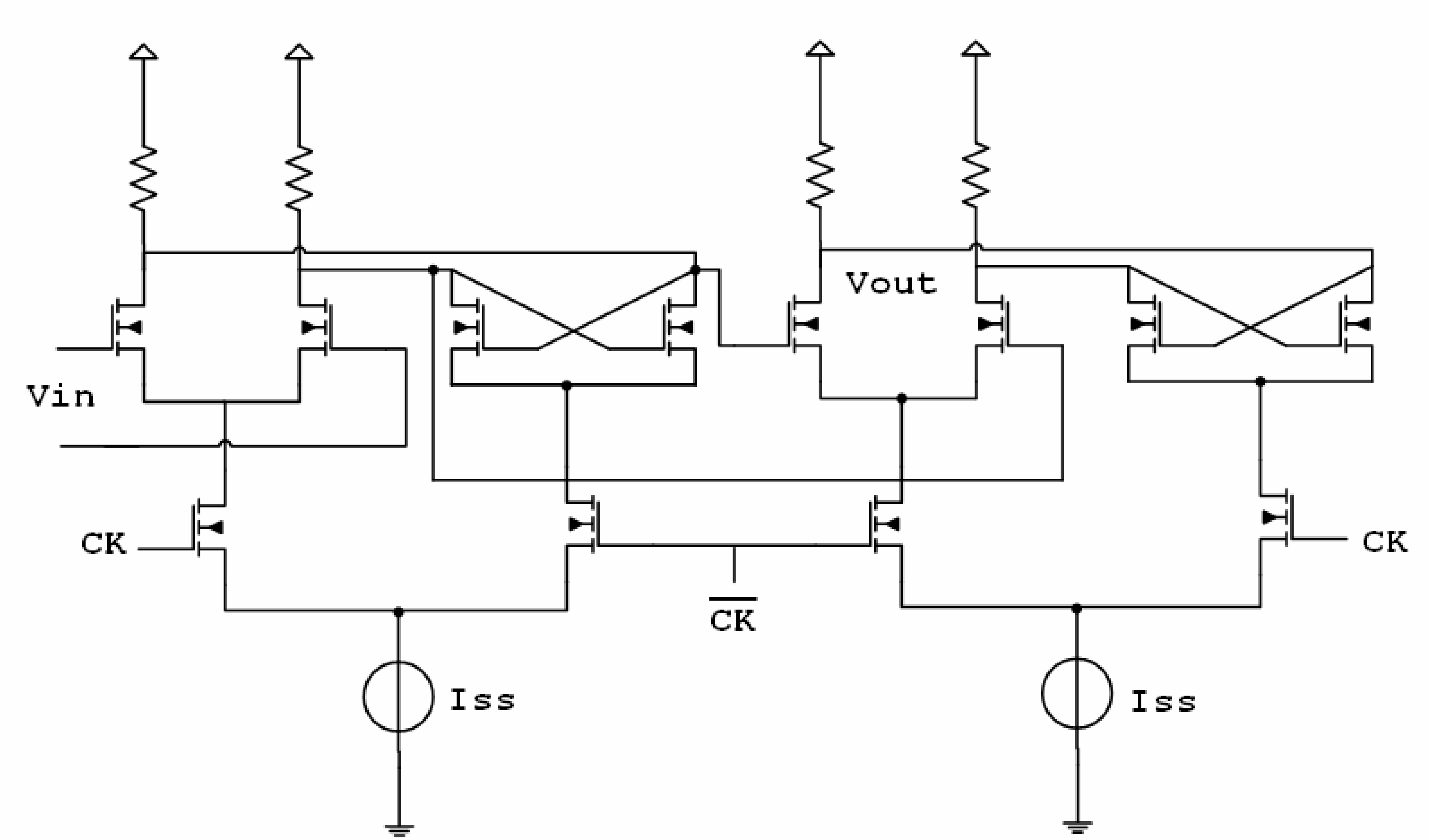
Dynamic Current Mode Logic

- V_{ds} of transistor Q1≈0 after the evaluation

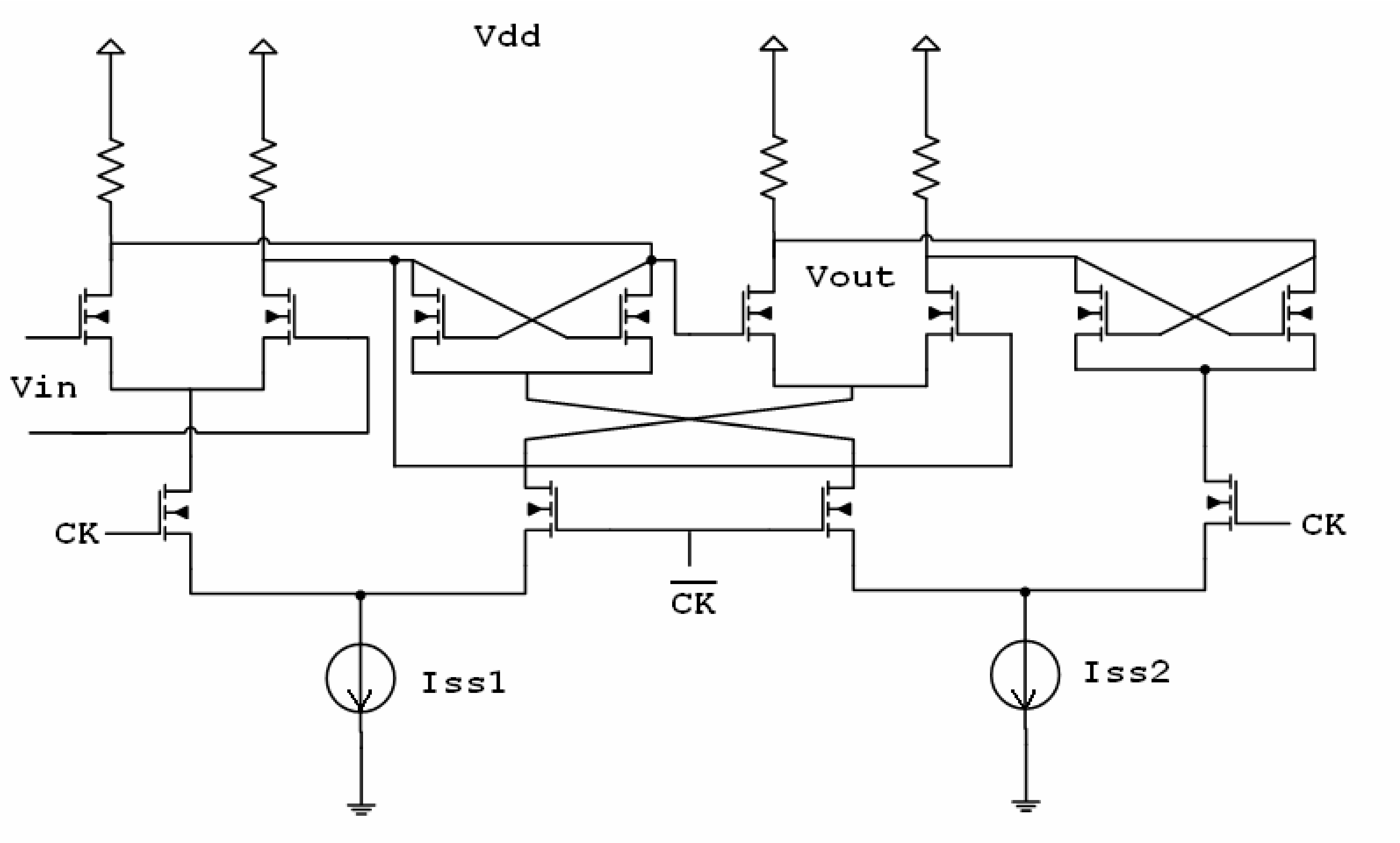


Conventional CML D-FF

- Read and latch use the same current source



Super-Dynamic CML D-FF



Super-Dynamic CML D-FF

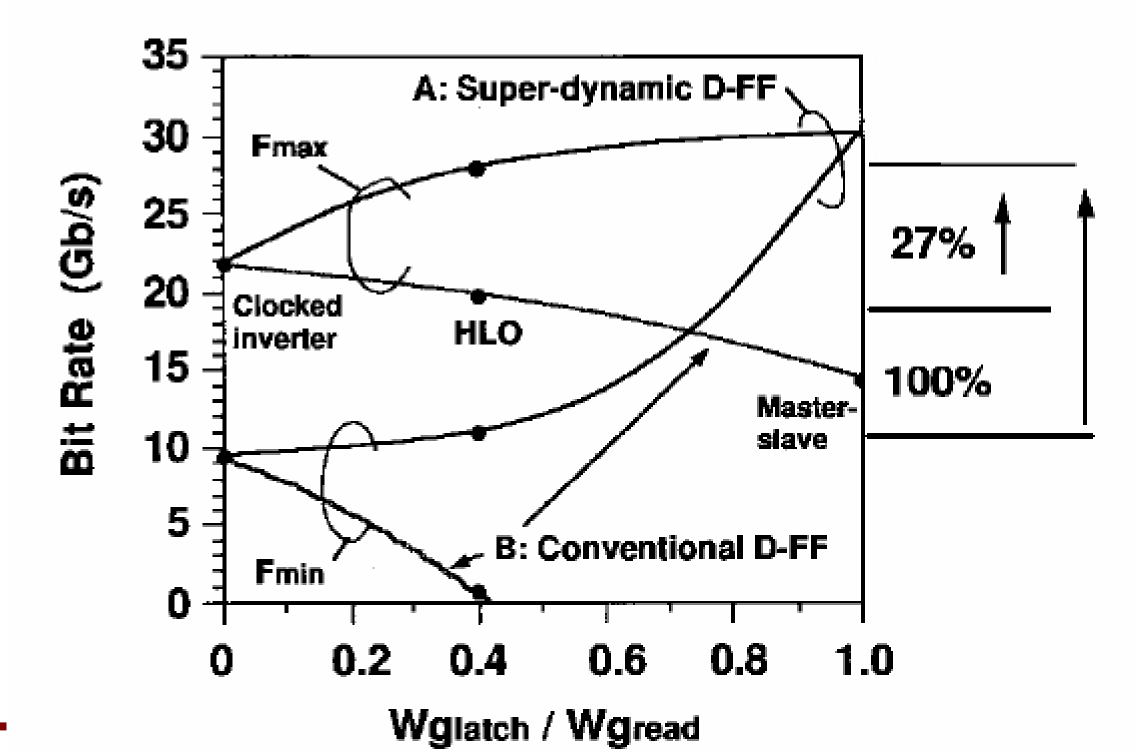
- Different current source of read and latch.

- Reduce cross couple size and increase operation speed

- Power consumption is less than conventional CML DFF

Super-Dynamic CML D-FF

- Super-dynamic D-FF increases speed about 30% over than Clock inverter, and 100% over than conventional D-DFF when Wg_{latch}/Wg_{read} = 0.4.



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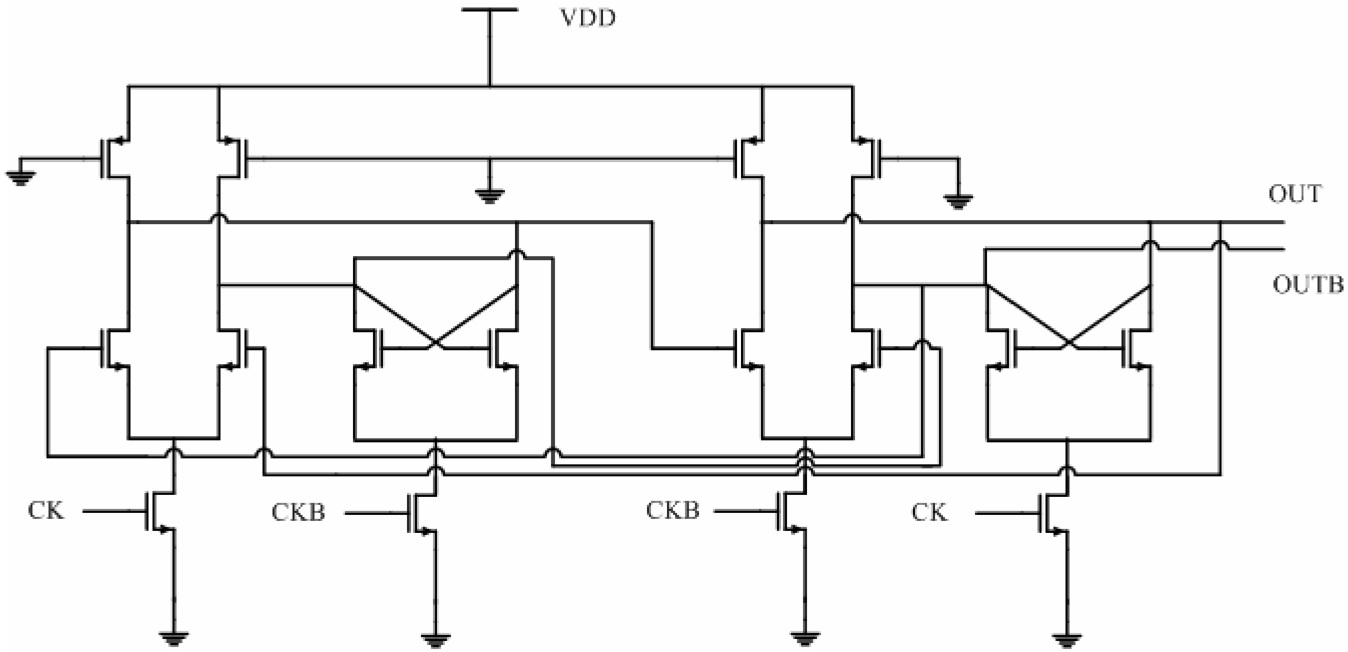
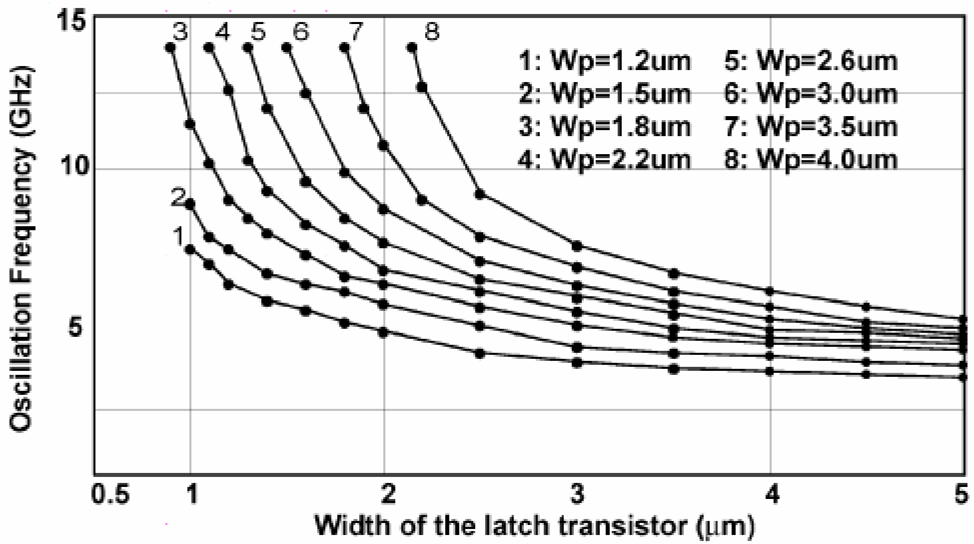
Power Efficient CML Divider

- Transistors size analysis to achieve smaller power consumption and high speed operation.



Power Efficient CML Divider

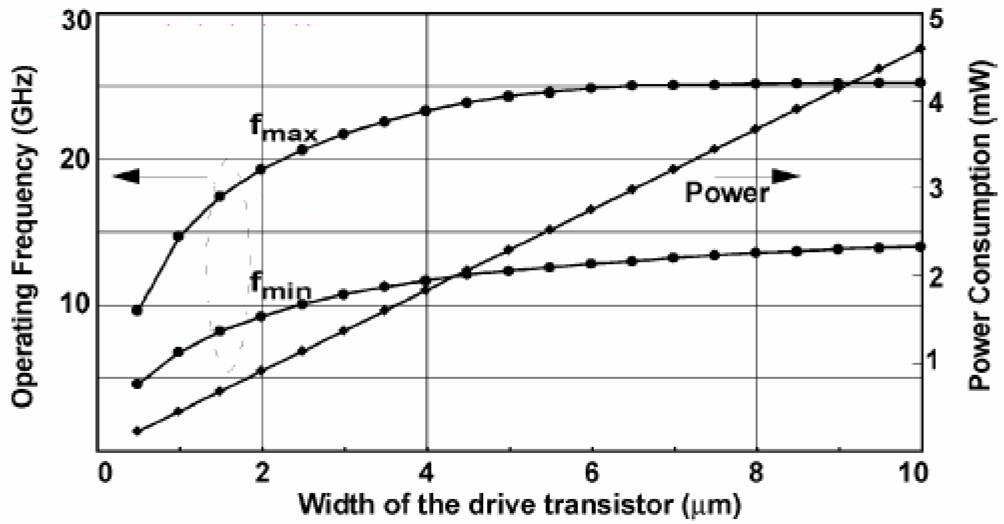
- The smaller load transistors size lead to lower oscillation frequency.
- Delay ($R_L C_L$) dependents on transistor size.
- Wider latch size lead to smaller oscillation frequency.



(a)

Power Efficient CML Divider

- To limit power consumption, load and latch size should be small, while avoiding the region where the circuit fail to oscillate.
- However latch size should large enough to generate sufficient voltage swing.



(b)

Power Efficient CML Divider

TABLE I

POWER CONSUMPTION AND MAXIMUM OPERATING FREQUENCY FOR SEVERAL RECENT PUBLISHED 2:1 CMOS STATIC FREQUENCY DIVIDERS

Ref	V_{dd} [V]	Power [mW]	Input Power [dBm]	Max. Freq. [GHz]	Technology
[7]	1.5	60.9*	9	25	120-nm CMOS
[8]	1.5	45*	10	27	120-nm CMOS
[9]	1.5	66*	0	18.5	120-nm CMOS
[10]	1.0	2.7	-7	25	120-nm SOI CMOS
	1.5	7.66	-7	28.6	
This work	1.2	1.86	0	22.5	130-nm CMOS
	1.5	3.88	0	26	

* including the power consumption of output buffers, which is about 1/3 of total power consumption

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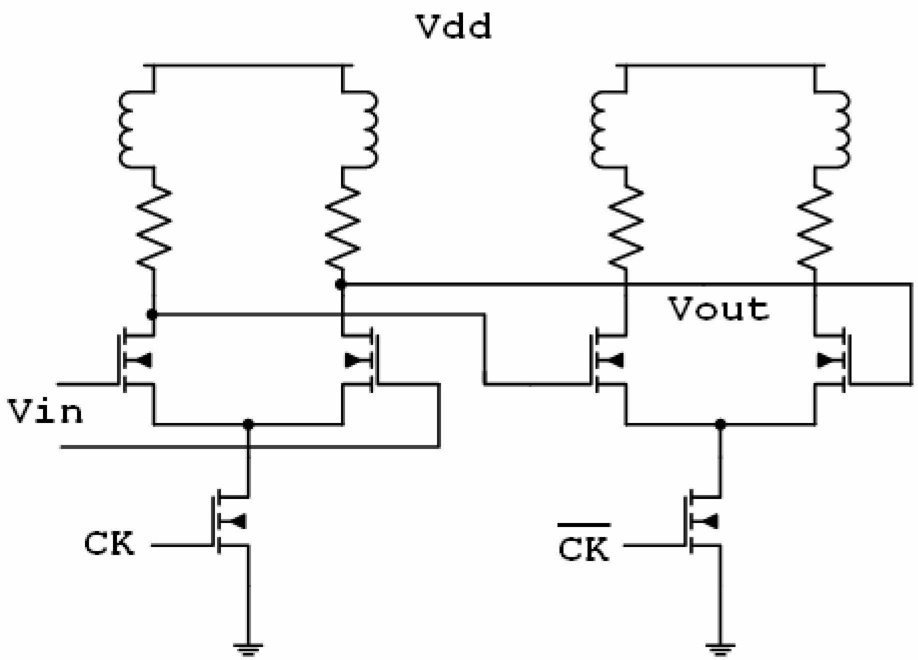
Inductor Peaking for Broadband CMOS CML

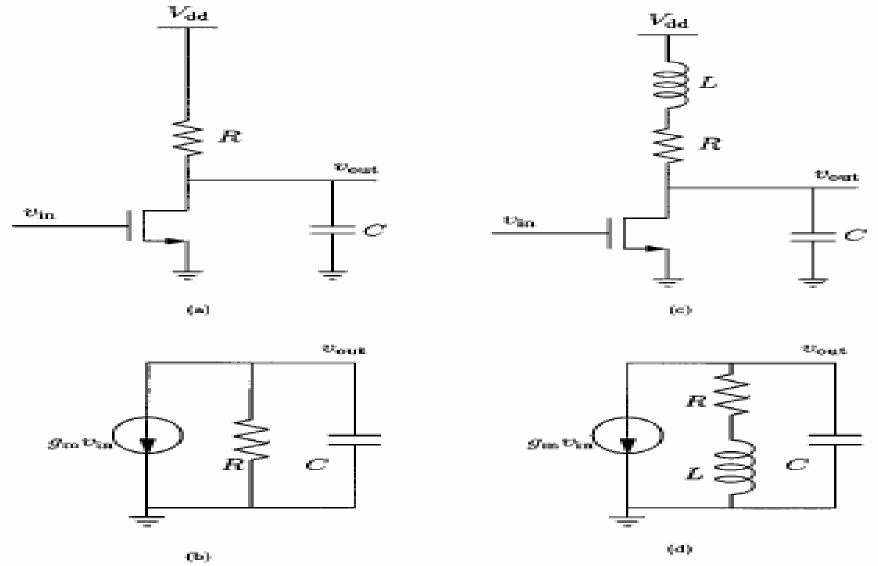
- The inductive peaking was proposed as an efficient and simple circuit technique to speed up the buffer's response



Inductor Peaking for Broadband CMOS CML

- **Shunt peaking:**

  Enhance the Bandwidth by Transforming frequency response form a single port to two poles and a zero .



$$\frac{v_{out}}{v_{in}}(\omega) = \frac{g_m R}{1 + j\omega RC},$$

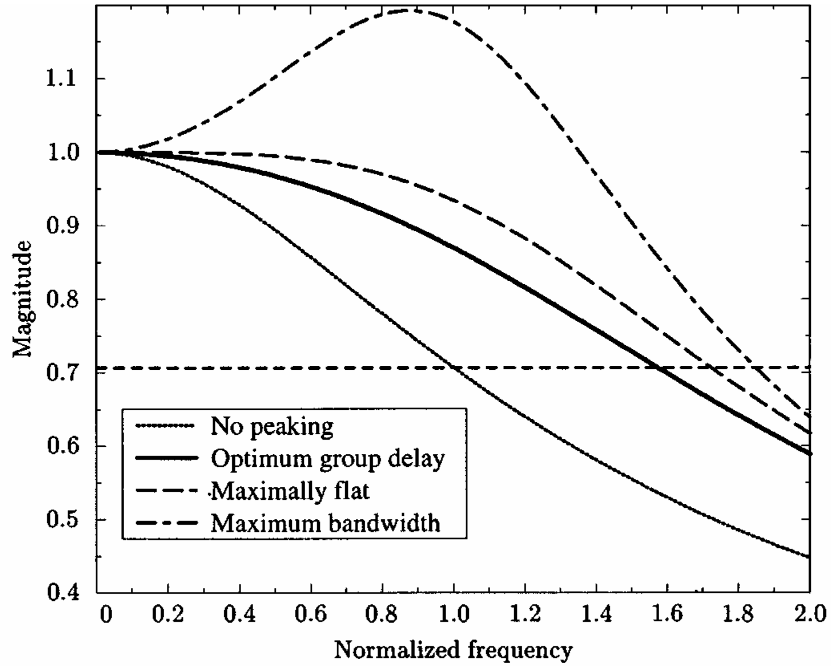
$$\frac{v_{out}}{v_{in}}(\omega) = \frac{g_m (R + j\omega L)}{1 + j\omega RC - \omega^2 LC}.$$

Inductor Peaking for Broadband CMOS CML

- m is the ratio of pole and zero.
- $L = m R^2 C$.

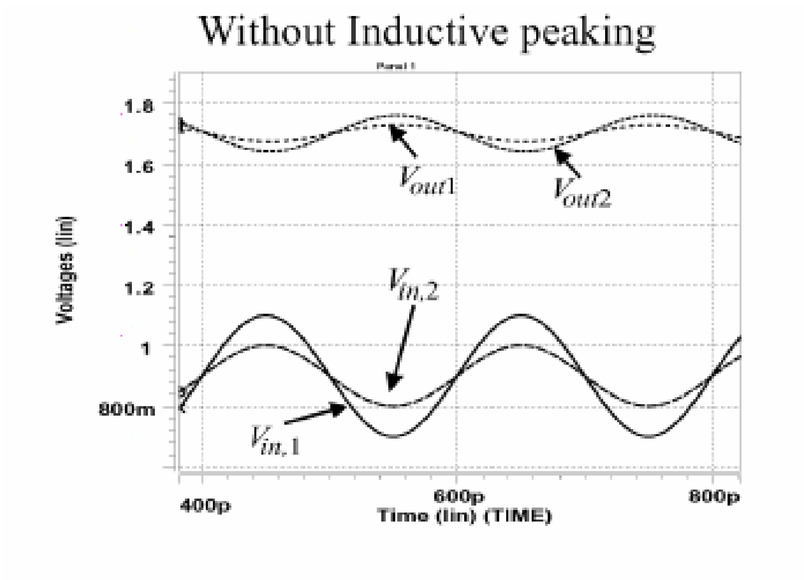
TABLE I
PERFORMANCE METRICS FOR SHUNT PEAKING

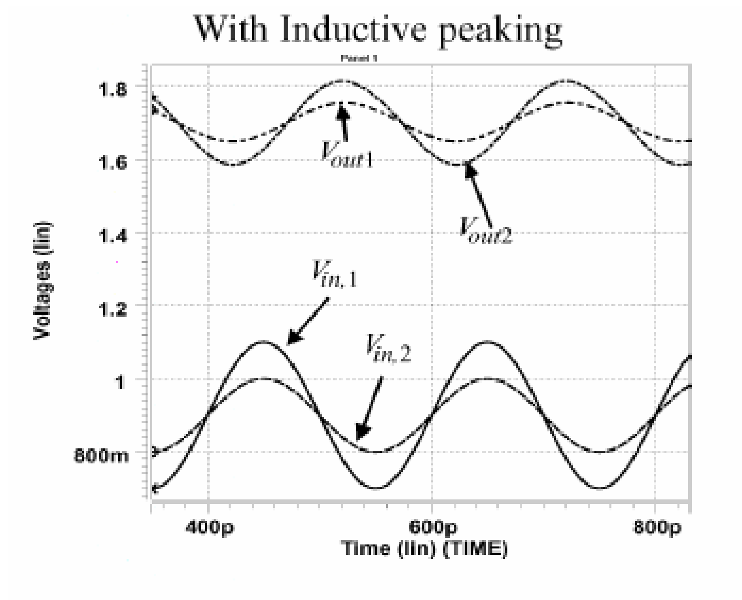
Factor (m)	Normalized ω_{3dB}	Response
0	1.00	No shunt peaking
0.32	1.60	Optimum group delay
0.41	1.72	Maximally flat
0.71	1.85	Maximum bandwidth



Inductor Peaking for Broadband CMOS CML

- **Inductive peaking will have larger amplitude and faster rise and fall time.**





Summary

- Current mode logic
  - Basic structure
- Dynamic current mode logic
  - Improve for power consumption
- Super-dynamic current mode logic
  - Improve for power consumption
  - High speed
- Inductor-peaking for broadband CMOS CML
  - Broadband

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Thanks for your listening