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Design guidelines of CMOS class-AB output stages: a tutorial

Walter Aloisi · Giuseppe Di Cataldo · Gianluca Giustolisi · Gaetano Palumbo

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Abstract This article presents useful guidelines for designing CMOS class-AB output stages. Three Quality Factors, which allow analysis and comparison of different output stages, are used to design two CMOS class-AB stages. We show that using the proposed Quality Factors and the related strategy leads to an efficient design in terms trade-off among area, current consumption, bandwidth and distortion. Indeed, for one of the two stages adopted as example, the design through the Quality Factors results in superior distortion performance with respect to the design suggested in the original article. Design examples and simulations are provided to validate the design strategy.

Keywords CMOS analog circuits · Analog integrated circuits · Operational amplifiers · Output stages

1 Introduction

In most analog circuits, the power operational amplifier (OpAmp) represents a fundamental building block. Unlike the operational transconductance amplifier (OTA), the OpAmp also includes an output stage to drive low load resistances [1, 2], which determines several features of the OpAmp itself. In particular, the output stage significantly affects the power dissipation, linearity and bandwidth of the OpAmp [3, 4].

The performance of output stages is measured in terms of output swing, drive capability, dissipation (or efficiency) and linearity. In general, the push–pull topology reported in Fig. 1 is used to maximize the output swing (in this manner the output swing, V_{swing}, intrinsically reaches the value of $V_{DD} - V_{SS} - 2V_{DSsat}$), and the drive capability required is guaranteed by properly setting the aspect ratio, (W/L), of transistors MNO and MPO in Fig. 1.

Efficiency generally depends on the bias current, which, being a tradeoff between power dissipation and bandwidth, must be properly controlled. Moreover, as a consequence, linearity, which strictly depends on the above parameters, is often sacrificed and its final value is determined by the topology adopted. Several topologies have been presented in the literature with the objective of satisfying such disparate requirements. However, their different structures and characteristics make it hard for the designer to choose the best option [5–8].

In the article [9], the authors defined three Quality Factors for comparing different output stage topologies designed for very low voltage power supply. These Quality Factors can also be used to give the designer a better understanding of relationships among current dissipation, area consumption, bandwidth and linearity of a generic output stage topology. Thus they can be used profitably during the design of an output stage.

In this tutorial, we present the use of the Quality Factors for obtaining useful design guidelines for the design of output stage topologies. In particular, Sect. 2 deals with an

W. Aloisi · G. Di Cataldo · G. Giustolisi (✉) · G. Palumbo
Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi, Universitá Degli Studi Di Catania, Viale Andrea Doria 6, 95125 Catania, Italy
e-mail: ggiustolisi@diees.unict.it

W. Aloisi
e-mail: waloisi@diees.unict.it

G. Di Cataldo
e-mail: gdicataldo@diees.unict.it

G. Palumbo
e-mail: gpalumbo@diees.unict.it

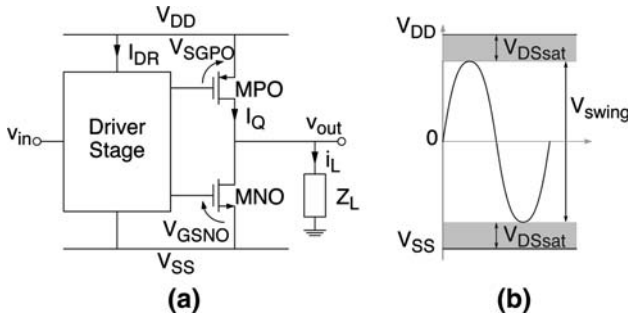

Fig. 1 (**a**) Generic output stage based on push–pull topology. (**b**) Output swing

overview of output stages with emphasis on low-voltage (LV) applications; then, in Sect. 3 we define and introduce the three Quality Factors which relate bandwidth, distortion, efficiency and current consumption; in Sect. 4 we use the three Quality Factors to analyze two output stages and to extrapolate some useful design guidelines; in Sect. 5 design examples as well as simulations are given and, finally, in Sect. 6, conclusions are drawn.

2 Overview of output stage features

With the term *drive capability* we means the ability of an output stage to provide current to a resistive load. In particular, considering Fig. 1, with R_L being the real part of the load Z_L, it is apparent that the output stage have to provide a maximum current $i_{L(MAX)} = V_{swing}/2R_L$ in both positive and negative direction. Hence, the maximum amount of current, $i_{L(MAX)}$, depends on the aspect ratio of final transistors MNO and MPO and on the overdrive that the driver stage of Fig. 1 can provide to them. Since, in general, the silicon area of the final transistors is not negligible and should be minimized, the driver stage has to provide the maximum allowable overdrive (i.e., the voltage $V_{DD} - V_{SS} - V_{DSsat}$) to MNO and MPO [10–13].

In general, for analog circuits a trade-off between bandwidth and power consumption exists, and it depends on the quiescent current, I_Q, of transistors MNO and MPO. In fact, if we consider the stage used in a complete amplifier, as shown in Fig. 2, the compensation is typically achieved by using the Miller (or Nested Miller) approach [2–4, 14–17]. Thus the maximum achievable amplifier bandwidth, ω_{GBW} (given by g_{mOTA}/C_C), is upper bounded (through the required phase margin) by the second pole, ω_2, which results equal to $(G_{Mout} + 1/R_L)/C_L$. Moreover, since stability must be achieved independently of the load resistance, the maximum amplifier bandwidth is bounded by the worst-case second pole, $\omega_2 = G_{Mout}/C_L$, which is only due to the output stage [18].

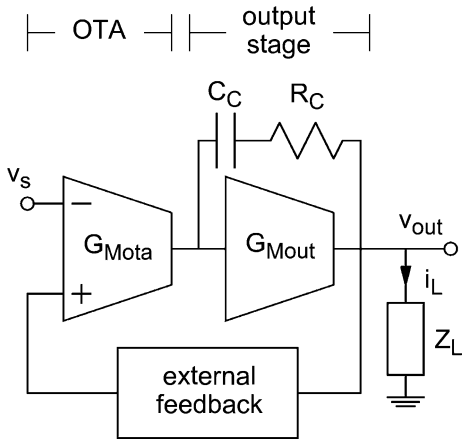

Fig. 2 Two-stage OpAmp in voltage follower configuration

Noting that both the dissipation and G_{Mout} increases with I_Q (the former with linear law and the second with a square-root law), the quiescent current must be properly set and accurately controlled. Indeed, the ability to accurately control quiescent current I_Q is key factor of a real output stage [19–21].

Finally, also the linearity, which is measured in terms of *total harmonic distortion* (*THD*), is strictly related to the quiescent current of the output stage, and in particular, it is improved (i.e., *THD* decreases) increasing I_Q [22, 23].

3 Quality factors

The discussion in the previous section highlights the trade-offs among the various features that an output stage has to exhibit. In general, for the designer, it is not simple to choose or design such stages. To overcome this difficulty we use the three Quality Factors previously presented in [9]. In particular, two Quality Factors, namely Q_B and Q_D, respectively, deal with bandwidth-dissipation and distortion-dissipation performance. The third one, named Q_C, supplies the relationship between the bias current of final transistors, I_Q, and the (undesired) current, I_{DR}, required to bias the driver stage as in Fig. 1. All these Quality Factors may be used to analyze and compare different output stages as well as to find useful guidelines which may be used by designers in the design phase.

3.1 Quality factor Q_B and bandwidth

Consider the real output stage shown in Fig. 1(a). Assume that its current I_{DR} biases the driver stage, that current I_Q flows in the final branch and that the aspect ratios of MPO and MNO are equal to S_{PO} and S_{NO}, respectively. Assume also that, when inserted in an OpAmp, it is responsible of an open-loop second pole equal to $\omega_2 = G_{Mout}/C_L$ where G_{Mout}

depends on the driver topology and is a function of I_{DR}, I_Q, S_{PO} and S_{NO} (that is, G_{Mout} is a function of current and area consumption). The Quality Factor Q_B is defined as the ratio between ω_2 of the real stage and the open-loop second pole of an ideal stage, referred to as the *normal stage*, which exhibits the same current and area consumption.

The *normal stage* is defined as the ideal output stage with the following characteristics: (1) the driver stage has unity gain; (2) the driver stage current I_{DR}, is zero; (3) final transistors MPO and MNO have the same aspect ratios as in the real stage (i.e., S_{PO} and S_{NO}, respectively); (4) the total current of the *normal stage* equals the total current of the real stage (i.e., the current in the output branch of the normal stage is $I_Q + I_{DR}$ of the real stage). The *normal stage* can be always developed for any real stage. Moreover, assuming that only MPO and MNO are responsible for area occupation, the normal stage is unique for any real stage with equal current dissipation and equal area occupation. Hence its open-loop second pole, ω_{2NORM}, can be used as a normalizing parameter for the open-loop second pole of the real stage.

Assuming a first-order model for MOS transistors, it is easy to show that the open-loop second pole of the *normal stage* is equal to $\omega_{2NORM} = \left(\sqrt{2\beta_{PO}I_{TOT}} + \sqrt{2\beta_{NO}I_{TOT}}\right)/C_L$, where β_{PO} and β_{NO} are the gain factors of the PMOS and NMOS output transistors, respectively. Consequently, we can define Q_B as

$$Q_B = \frac{\omega_2}{\omega_{2NORM}} = \frac{G_{Mout}}{\left(\sqrt{2\beta_{PO}} + \sqrt{2\beta_{NO}}\right)\sqrt{I_{TOT}}} \tag{1}$$

This Quality Factor tells the designer if both area and current are worth expending to obtain the present bandwidth performance. The higher Q_B is the better the stage topology.

3.2 Quality factor Q_C and efficiency in bias condition

Referring to Fig. 1, current I_Q of an ideal output stage should be set by bandwidth and distortion requirements while current I_{DR} should be ideally equal to zero. Obviously, to work properly, the driver stage requires a finite current, I_{DR}, that should be as low as possible (generally much smaller than I_Q). Therefore, we can define the Quality Factor Q_C as

$$Q_C = I_{DR}/I_Q \tag{2}$$

representing the ratio between the current needed by the driver stage and the current required by the output branch.

Defining the total current of the stage as $I_{TOT} = I_Q + I_{DR}$, the efficiency of the stage under bias condition (defined as the ratio between I_Q—useful current—and the total current dissipated by the stage, I_{TOT}), is: $\eta_{BIAS} = I_Q/I_{TOT} = 1/(1 + Q_C)$.

A good design should exhibit η_{BIAS} as large as possible, that is, close to unity or, equivalently, it should exhibit Q_C close to zero. Somehow the two parameters give the same information and the reader, when dealing with Q_C, should keep in mind the physical meaning of this quality factor that also represents a sort of bias-condition efficiency.

3.3 Quality factor Q_D and distortion

Several indicators are used to measure the amount of non-linearity in analog circuits but, among them, the most convenient are based on the Fourier decomposition and on the harmonic analysis. If the analog circuit is fed by a pure single-tone signal at frequency ω_0, non-linearity causes undesired tones (harmonics) at the output. Defining Y_k as the amplitude of the kth tone, harmonic distortion components, HD, are defined as $HD_k = Y_k/Y_1$ and the total harmonic distortion is defined as $THD = \sqrt{\sum_k HD_k^2}$. In the case of low distortion and in a first-order approximation, HD_2 and HD_3 components dominate over higher-order components and so we may write $THD \approx \sqrt{HD_2^2 + HD_3^2}$.

Another way to characterize distortion is to use intermodulation distortion. In this case two sinusoidal tones of equal amplitude and frequencies ω_1 and ω_2, respectively, are applied to the input. The output exhibits intermodulation products made of two tones at $\omega_1 \pm \omega_2$ and four tones at $2\omega_1 \pm \omega_2$ and at $\omega_1 \pm 2\omega_2$. Intermodulation products are measured in terms of IM_2 and IM_3. The former is the ratio of the two components at $\omega_1 \pm \omega_2$ to the fundamental while the latter is the ratio of the four components at $2\omega_1 \pm \omega_2$ and $\omega_1 \pm 2\omega_2$ to the fundamental. In a first-order approximation, HD_2 and HD_3 are related to IM_2 and IM_3 as $IM_2 = 2HD_2$ and $IM_3 = 3HD_3$ [24]. Therefore, HD or IM components may be used to express distortion equivalently. Moreover, IM components may be derived by the knowledge of HD components and vice versa [24]. In our discussion, we shall use THD to measure distortion and, since very often either HD_2 dominates over HD_3 or vice versa, intermodulation components may be obtained by the knowledge of THD, easily.

In output stages THD decreases while the quiescent current increases and, for a given bias current, THD mainly depends on the driver stage topology adopted. Moreover, THD is a function of the output signal and assuming the load resistor to be linear, it depends on the load current i_L. At a first approximation, THD increases with the load current and reaches the maximum value for $i_{L(MAX)} = V_{swing}/2R_L$, as focused in Sect. 2. Consequently, an effective definition for the third Quality Factor, Q_D, is obtained assuming THD is proportional to $i_{L(MAX)}$ and $1/I_{TOT}$ and setting the following:

$$Q_D = THD \cdot \frac{I_{TOT}}{i_{L(MAX)}} \tag{3}$$

If *THD* is really proportional to $i_{L(MAX)}$ and $1/I_{TOT}$, Q_D is a unique number, independent of current consumption, that individually defines the stage properties from a distortion (or linearity) point of view regardless of its dissipation. Specifically, it tells the designer what is the maximum distortion the stage can exhibit after paying the price I_{TOT} in static current consumption. Obviously, the lower the Q_D the better the stage, since for a given dissipation and for a given output swing the stage exhibits better linearity performance.

4 Output stage design guidelines

Starting from the quality factor described above, we can derive useful guidelines to design CMOS output stages and, in particular, to size transistors in the driver stage. We shall show their use through the design of two CMOS output stages. The first one is the well-known symmetric differential-input (SDI) stage originally proposed in [25], the second is an interesting CMOS output stage suited for LV application and proposed in [26]. As far as the latter stage is concerned, it is worth noting that, following our design procedure, we obtain different transistor dimensions and better linearity performance compared to the original work [26].

Before starting with the exposition of the two examples, we define some key parameters that will be useful in the following. The first parameter is the well-known transistor *gain factor*, defined as

$$\beta_i = \mu C_{ox}\left(\frac{W}{L}\right)_i \tag{4}$$

Assuming a first-order model for the saturated MOSFET, the drain current of transistor M*i* takes the following expression

$$i_{Di} = \frac{\beta_i}{2}(v_{GSi} - V_T)^2 \tag{5}$$

To define the remaining parameters we refer to generic schema of output stage in Fig. 3 where we identify transistors MND and MPD as those transistors of the driver stage directly connected to the output transistors MNO and MPO, respectively. Therefore, we define

$$n = \frac{\beta_{NO}}{\beta_{ND}} = \frac{\beta_{PO}}{\beta_{PD}} \tag{6}$$

as the ratio between the gain factors of the output transistors and the corresponding directly connected transistors of the driver stage. Note that, we assumed that the stage is symmetric, that is, $\beta_{NO} = \beta_{PO}$ and $\beta_{ND} = \beta_{PD}$.

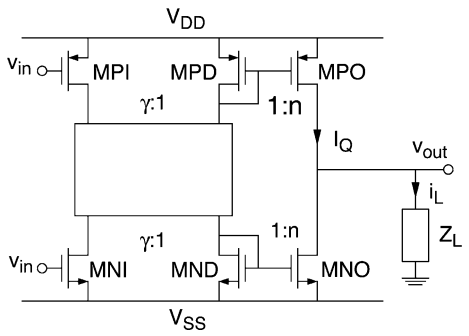

Fig. 3 Geometrical parameters common to output stages

Finally, referring to Fig. 3, we may distinguish transistors MNI and MPI as the input transistors of the driver stage and define

$$\gamma = \frac{\beta_{NI}}{\beta_{ND}} = \frac{\beta_{PI}}{\beta_{PD}} \tag{7}$$

as the ratio between the gain factors of the input transistors, MNI and MPI, and transistors MND and MPD and of the same type. Note that, depending on the topology of the stage, either MPI or MNI may not be present. In this case the existent input transistor defines the parameter γ.

4.1 Symmetric differential-input CMOS output stage

The SDI CMOS output stage originally proposed in [25] is shown in Fig. 4. This stage exhibits high linearity thanks to the symmetry of the driver structure. In fact, all NMOS transistors are designed with a gain factor equal to that of the corresponding PMOS transistors (i.e. $\beta_{Ni} = \beta_{Pi}$) and A- and B-type transistors in Fig. 4 are designed with the same aspect ratio.

Parameter n is defined as in (6) and, observing that the input transistor is MNIA (and MNIB), parameter γ is defined as

$$\gamma = \frac{\beta_{NIA}}{\beta_{ND}} \tag{8}$$

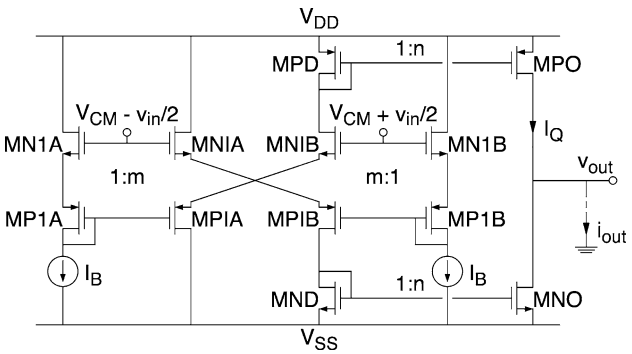

Fig. 4 Schematic of the SDI output stage

In addition, we introduce the ratio between the gain factors of transistors MI and M1 as

$$m = \frac{\beta_I}{\beta_1} \tag{9}$$

4.1.1 Large signal behavior

The large signal behavior may be found inspecting the circuit in Fig. 4. Assuming that all transistors operate in the saturation region and considering the first-order model for MOS transistors in (4, 5), following the paths composed by the gate-source voltages of MNIB-MPIA-MP1A-MN1A and MNIA-MPIB-MP1B-MN1B, we obtain

$$\left(V_{CM}+\frac{v_{IN}}{2}\right)-\left(V_{CM}-\frac{v_{IN}}{2}\right) = 2V_T+2\sqrt{\frac{2i_{DPD}}{\beta_I}}-2V_T-2\sqrt{\frac{2mI_B}{\beta_I}} \tag{10a}$$

$$\left(V_{CM}-\frac{v_{IN}}{2}\right)-\left(V_{CM}+\frac{v_{IN}}{2}\right) = 2V_T+2\sqrt{\frac{2i_{DND}}{\beta_I}}-2V_T-2\sqrt{\frac{2mI_B}{\beta_I}} \tag{10b}$$

which, considering that $i_{DPO} = ni_{DPD}$ and $i_{DNO} = ni_{DND}$, lead to

$$i_{DPO} = \frac{n\beta_I}{2}\left(\sqrt{\frac{2mI_B}{\beta_I}}+\frac{v_{IN}}{2}\right)^2; \quad \text{for } \frac{v_{IN}}{2} < -V_{CM} + (2V_T + V_{DSsat}) \tag{11a}$$

$$i_{DNO} = \frac{n\beta_I}{2}\left(\sqrt{\frac{2mI_B}{\beta_I}}-\frac{v_{IN}}{2}\right)^2; \quad \text{for } \frac{v_{IN}}{2} > V_{CM} - (2V_T + V_{DSsat}) \tag{11b}$$

Note that the two conditions of validity of (11a) and (11b) guarantee either the saturation of MNIB-MPIA or the saturation of MNIA-MPIB. Consequently, since $v_{OUT} = R_L i_{OUT}$, we may write

$$v_{OUT} = \begin{cases} R_L i_{DPO} & \frac{v_{IN}}{2} > V_{CM} - (2V_T + V_{DSsat}) \\ R_L(i_{DPO} - i_{DNO}) & \left|\frac{v_{IN}}{2}\right| < V_{CM} - (2V_T + V_{DSsat}) \\ -R_L i_{DNO} & \frac{v_{IN}}{2} < -V_{CM} + (2V_T + V_{DSsat}) \end{cases} \tag{12}$$

4.1.2 Quality factor determination

Manipulating (11) it is easy to show that

$$I_Q = nmI_B \tag{13}$$

$$I_{TOT} = \left(1+2\frac{m+1}{n\,m}\right)I_Q \tag{14}$$

$$G_{Mout} = n\,g_{mI} = \sqrt{\gamma}\,g_{mO} \tag{15}$$

where the latter term is expressed as a function of the transconductance of output branch transistors, g_{mO}.

As we shall demonstrate in the Appendix B, due to the symmetric structure of the circuit, the main contribution to harmonic distortion is given by HD_3. This may be evaluated exploiting the approach suggested in [12, 27–29]. The method gives the third-order harmonic distortion as a function of the small-signal voltage gain, a_1, as well as the output derivative at the highest and lowest extreme of the input variation, a^+ and a^-, respectively. In particular, once we evaluate a_1, a^+ and a^-, we may write for the harmonic distortion term

$$HD_3 = \frac{a^+ + a^- - 2a_1}{24a_1} \tag{16}$$

In our case the small-signal voltage gain is

$$a_1 = \left.\frac{\partial v_{OUT}}{\partial v_{IN}}\right|_{v_{IN}=0} \approx n g_{mI} R_L \tag{17}$$

and, assuming that a sinusoidal input is applied, that is $v_{IN} = V_A \sin(\omega t)$, a^+ and a^- are

$$a^+ = \left.\frac{\partial v_{OUT}}{\partial v_{IN}}\right|_{v_{IN}=V_A} = \frac{n g_{mI} R_L}{2}\left(1+\frac{g_{mI}}{4mI_B}V_A\right) \tag{18}$$

$$a^- = \left.\frac{\partial v_{OUT}}{\partial v_{IN}}\right|_{v_{IN}=-V_A} = \frac{n g_{mI} R_L}{2}\left(1+\frac{g_{mI}}{4mI_B}V_A\right) \tag{19}$$

Therefore, we have for *THD*

$$THD \approx HD_3 = \frac{1}{24}\left|\frac{g_{mI}}{4mI_B}V_A - 1\right| = \frac{1}{24}\left|\frac{i_{L(MAX)}}{4I_Q} - 1\right| \approx \frac{1}{96}\frac{i_{L(MAX)}}{I_Q} \tag{20}$$

where $i_{L(MAX)} \approx G_{Mout} V_A \gg I_Q$ was assumed.

Starting from (13) to (15) and (20) it is easy to compute the Quality Factors Q_C, Q_B and Q_D, obtaining

$$Q_B = \frac{\sqrt{\gamma}}{2\sqrt{1+2\frac{m+1}{nm}}} \tag{21a}$$

$$Q_C = 2\frac{m+1}{nm} \tag{21b}$$

$$Q_D = \frac{1}{96}\left(1+2\frac{m+1}{nm}\right) \tag{21c}$$

4.1.3 Design comments

The three Quality Factors are depicted in Figs. 5–8 as a function of the ratio n and for different values of m. Their analysis reveals that m and n should be as large as possible. In this situation, the Quality Factors reach the theoretical value of $Q_C = 0$, $Q_B = \sqrt{\gamma}/2$ and $Q_D = 1/96$. However, as

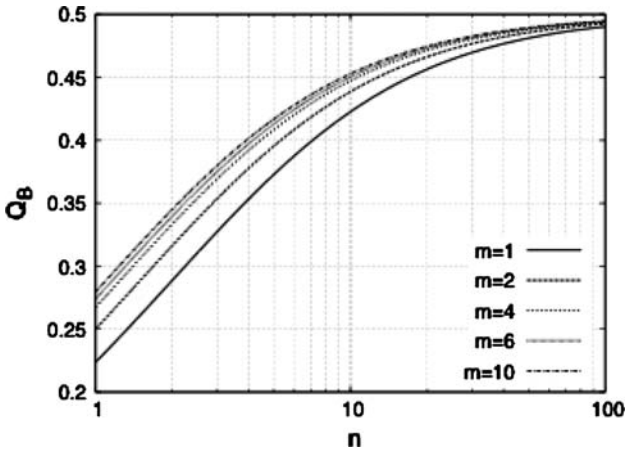

Fig. 5 Quality Factor Q_B for the SDI output stage ($\gamma = 1$)

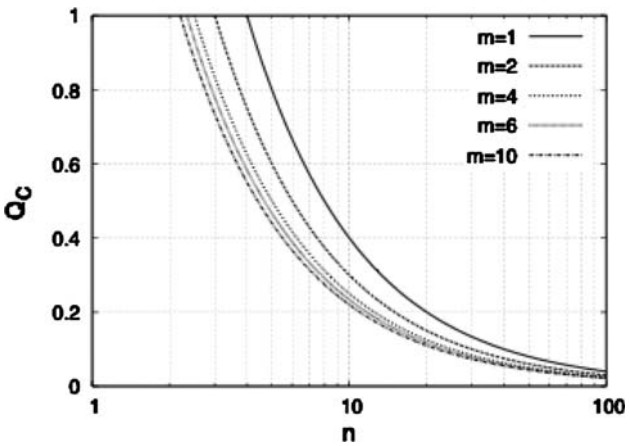

Fig. 6 Quality Factor Q_C for the SDI output stage

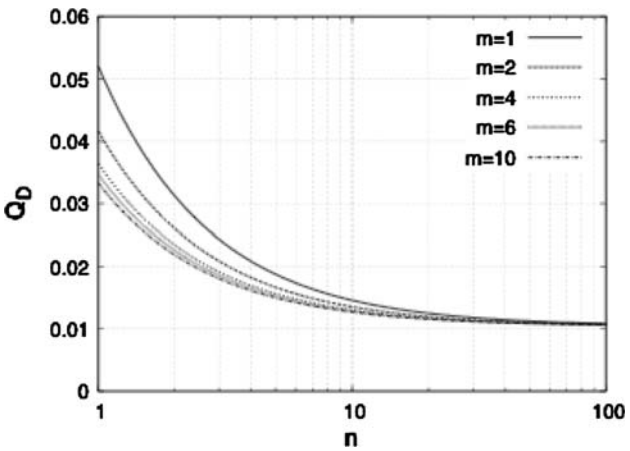

Fig. 7 Quality Factor Q_D for the SDI output stage

this would require excessive area consumption, recourse to a trade-off becomes mandatory.

Parameter m plays a role in both Q_B and Q_C where we have the ratio $(m + 1)/m$. This ratio has a maximum value

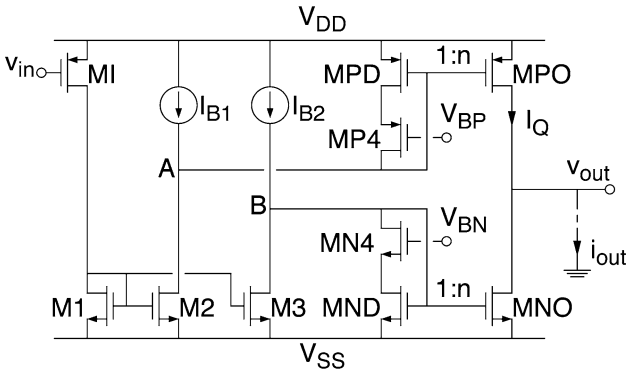

Fig. 8 Schematic of the LV output stage

of 2 (for $m = 1$) and moves to 1 by increasing m. Therefore, a good choice for this parameter is setting m about 4–6 for which the ratio $(m + 1)/m$ is about 1.25–1.17. Note that a larger value does not improve Q_B and Q_C significantly.

Parameter n mainly affects Q_C which represents stage efficiency in the bias condition. A good choice for n is setting it so that the current of the driver stage is not higher than the 20% of the output-branch current. If we set $m = 5$, this means setting n to a value higher than 12.

Finally, parameter γ can be found by forcing the stage to exhibit at least the same bandwidth as the normal stage, which means $Q_B \geq 1$. However a better choice is setting $\gamma = m$, since this satisfies bandwidth requirements and, at the same time, saves area consumption.

4.2 Low-voltage CMOS output stage

The considered LV output stage was introduced in [26] and is shown in Fig. 8. It consists of a push–pull output pair, MNO and MPO and two adaptive loads made up of transistors MP4-MPD and MN4-MND which are driven by transistors M2 and M3, respectively. Two voltages, V_{BP} and V_{BN} are required to bias the adaptive load while the whole stage is biased by current generators, I_{B1} and I_{B2}. Finally, transistors MI and M1 operate the phase inversion required for frequency compensation.

4.2.1 Large signal circuit behavior

The output stage depicted in Fig. 8 uses transistors M4-MD as adaptive loads. In fact, in quiescent conditions, all the transistors are in saturation region and, hence, the resistive loads connected to node A and B are small. When the input level increases, for example in the negative direction, transistor MI delivers an extra current to M1 which is subsequently mirrored to both M2 and M3. The extra current in M2 flows through MP4-MPD and, consequently, the gate of MPD is pulled down, while its drain voltage

tends to V_{DD} because of the presence of MP4 whose gate-source voltage increases, too. If V_{BP} is set properly, MPD enters the triode region thus causing the overall resistance at node A to increase as well. In such a situation, any small increment of current from M2 causes large swing at node A and provides the adequate overdrive to the gate of MPO. In the meantime, once the extra current in M3 equals I_{B2}, transistors MN4-MND and, consequently, MNO turn off. Therefore the load is supplied by MPO only.

On the other hand, when the input level increases in the positive direction, the current in both M2 and M3 decreases. Then, the current in MN4 and MND increases, and, if V_{BN} is set properly, transistor MND goes to triode region thus increasing the resistance at node B. Any other increment of current through MND, makes node B high thus affording the adequate overdrive to output transistor MNO which supplies the load. At the same time, once the current in M2 equals I_{B1}, transistors MP4, MPD and, consequently, MPO, turn off.

It is worth noting that there is a different behavior in class-B mode. Specifically, when the input level increases negatively, the current which flows in MP4-MPD is supplied by M2 and, hence, is not limited. Instead, when the input level increases in the opposite direction, the current that flows in MN4-MND is bounded by the current generator I_{B2}. However, in this condition, the class-B operation is guaranteed by the adaptive load performed by MN4-MND which turns node B into a high-impedance node. Anyway, in order to make up for the current limitation given by I_{B2}, a high bias current is required for the output stage in order to guarantee a proper overdrive to output transistor MNO.

As mentioned above, to achieve proper class-B operation, both voltages V_{BP} and V_{BN} must be set so that, in bias condition, MPD and MND are in the edge between saturation and triode regions. In this manner, a small increment of drain current in MP4 (MN4) causes $V_{SGP4}(V_{GSN4})$ to increase and $V_{SDPD}(V_{SDND})$ to decrease. Therefore, the stage must satisfy the following design constraint

$$V_{BN} = V_{Tn} + 2V_{DSsat} \tag{22a}$$

$$V_{BP} = V_{DD} - \left|V_{Tp}\right| - 2V_{DSsat} \tag{22b}$$

For the stage to work properly we set

$$\beta_1 = \beta_2 = \beta_3 \tag{23a}$$

$$I_{B1} = (1-\alpha)I_B \tag{23b}$$

$$I_{B2} = (1+\alpha)I_B \tag{23c}$$

being $0 < \alpha < 1$ the amount of current I_B used to bias MDP and MDN and

$$I_B = \frac{I_{B1} + I_{B2}}{2} = I_{D2,3} \tag{24}$$

4.2.2 Quality factor determination

By inspection it is easy to show that

$$I_Q = n\alpha I_B \tag{25}$$

$$I_{TOT} = \left(1 + \frac{3+\alpha}{n\alpha}\right) I_Q \tag{26}$$

$$G_{Mout} = 2ng_{mI} = 2\sqrt{\frac{\gamma}{\alpha}}g_{mO} \tag{27}$$

Also in this case, thanks to the symmetric structure of the circuit, HD_3 dominates over HD_2 and the former may be evaluated using again (16). In this case, term a_1 results

$$a_1 = -2ng_{mI}R_L \tag{28}$$

In order to evaluate a^+ we assume that MP4, MPD and MPO are switched off and that MND is in the triode region. This leads to

$$v_{OUT} = -\frac{\beta_{NO}}{2}(v_{GSNO} - V_{Tn})^2 R_L \tag{29}$$

$$\begin{aligned} i_{DND} &= \beta_{ND}\left(v_{GSNO} - V_{Tn} - \frac{v_{DSND}}{2}\right)v_{DSND} \\ &\approx \beta_{ND}(v_{GSNO} - V_{Tn})V_{DSNDsat} \end{aligned} \tag{30}$$

$$i_{DND} = I_{B2} - \frac{\beta_I}{2}\left(V_{DD} - v_{IN} - \left|V_{Tp}\right|\right)^2 \tag{31}$$

which may be used to evaluate

$$\begin{aligned} a^+ &= \left.\frac{\partial v_{OUT}}{\partial v_{IN}}\right|_{v_{IN}=V_A} = \left.\frac{\partial v_{OUT}}{\partial v_{GSNO}}\frac{\partial v_{GSNO}}{\partial i_{DND}}\frac{\partial i_{DND}}{\partial v_{IN}}\right|_{v_{IN}=V_A} \\ &\approx -ng_{mI}R_L\frac{\alpha I_B + g_{mI}V_A}{\beta_{ND}V_{DSNDsat}^2} = -ng_{mI}R_L\frac{\alpha I_B + g_{mI}V_A}{2\alpha I_B} \end{aligned} \tag{32}$$

where we used the approximation $g_{mI}V_A \ll 2I_B$. A similar procedure let us find a^- that results

$$a^- \approx -ng_{mI}R_L\frac{\alpha I_B + g_{mI}V_A}{\beta_{DP}V_{SDPDsat}^2} = -ng_{mI}R_L\frac{\alpha I_B + g_{mI}V_A}{2\alpha I_B} \tag{33}$$

Consequently, *THD*, approximately equal to the third harmonic distortion component, results

$$\begin{aligned} THD \approx HD_3 &= \frac{1}{24}\left|\frac{\alpha I_B + g_{mI}V_A}{2\alpha I_B} - 2\right| = \frac{1}{24}\left|\frac{i_{L(MAX)}}{4I_Q} - \frac{3}{2}\right| \\ &\approx \frac{1}{96}\frac{i_{L(MAX)}}{I_Q} \end{aligned} \tag{34}$$

where we assumed $i_{L(MAX)} \approx G_{Mout}V_A \gg I_Q$.

From (25), (26), (27) and (34) we may evaluate the Quality Factors, that is

$$Q_B = \sqrt{\frac{\gamma n}{\alpha(n+1)+3}} \tag{35a}$$

$$Q_C = \frac{1}{n}\left(1 + \frac{3}{\alpha}\right) \tag{35b}$$

$$Q_D = \frac{1}{96n}\left(n + 1 + \frac{3}{\alpha}\right) \tag{35c}$$

4.2.3 Design comments

The three Quality Factors are depicted in Figs. 9–11 as a function of the ratio n and for different values of α. Their analysis reveals that n should be as large as possible. In such a situation, the Quality Factors reach the theoretical value of $Q_C = 0, Q_B = \sqrt{\gamma/\alpha}$ and $Q_D = 1/96$ where the bandwidth can be improved either by decreasing α or increasing γ (Fig. 12).

In order to save area while maintaining an acceptable value for Q_B, the best choice is setting small values for both α and γ as in the original work where α was set to 0.2. However, α small leads to very large n (e.g., from (35b), making $Q_C = 0.2$ with $\alpha = 0.2$ leads to $n = 80$). Large n means also setting Q_D and Q_B very close to their theoretical limits. Moreover, as far as Q_B is concerned, we may also improve the bandwidth performance by choosing γ without much effort. As a consequence, setting α small requires n large for the stage to work efficiently. This is indeed the case of the design in the original work.

5 Design examples

The SDI and the LV stages were designed in a standard 0.35-μm CMOS process whose main parameters are reported in Table 1. Both stages are inserted in two complete amplifiers whose overall open-loop gains are 60 dB. The amplifiers exploit Miller compensation to achieve stability and are connected as in Fig. 2 with unity-gain external feedback. In both cases the OTA was built with ideal (and linear) components so to obtain an effective comparison of output stages' characteristics, only.

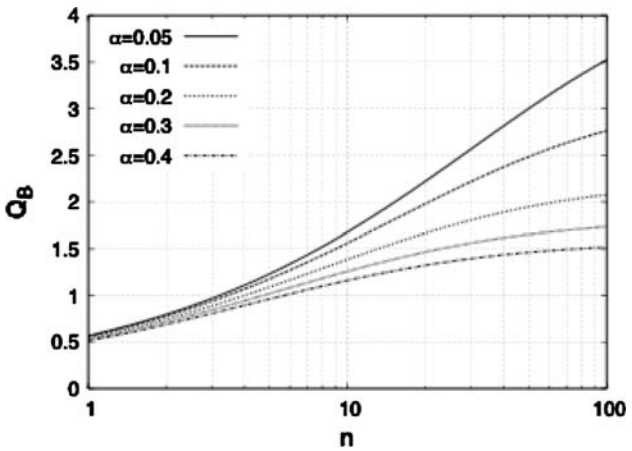

Fig. 9 Quality Factor Q_B for the LV output stage ($\gamma = 1$)

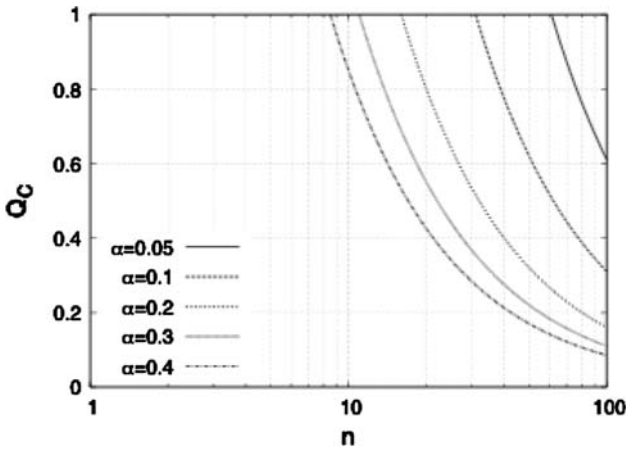

Fig. 10 Quality Factor Q_C for the LV output stage

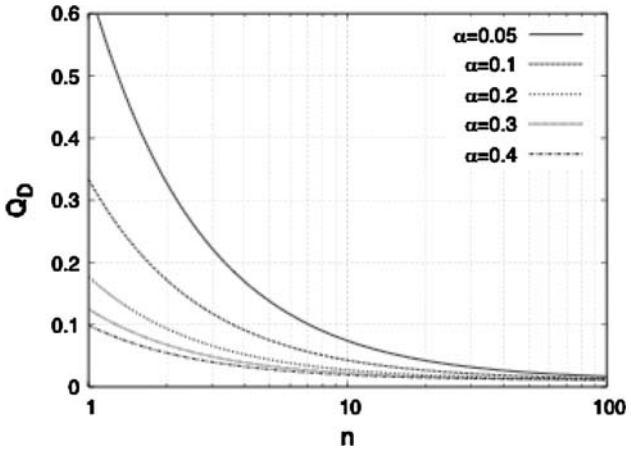

Fig. 11 Quality Factor Q_D for the LV output stage

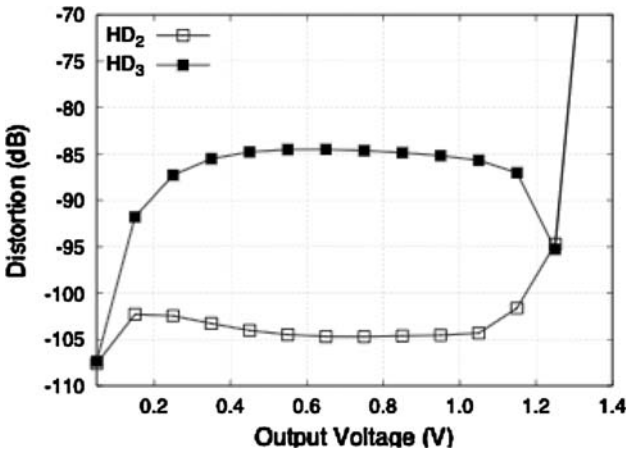

Fig. 12 Distortion simulation of the SDI output stage

5.1 Symmetric differential-input CMOS output stage

The SDI stage was designed following the design comments of Subsect. 4.1.3, therefore ratios m, n and γ were set

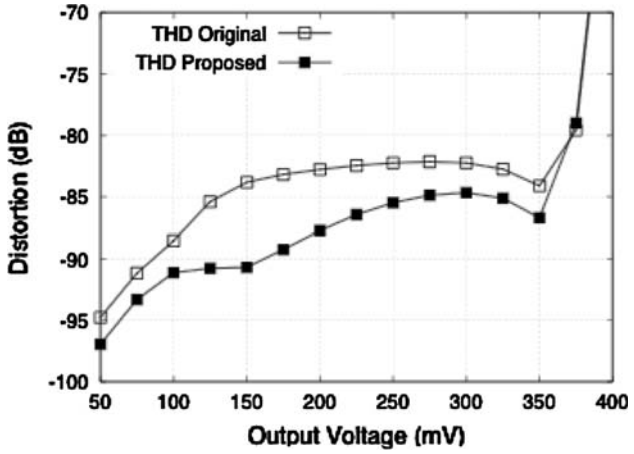

Fig. 13 Distortion simulation of the LV output stage

Table 1 Main technology parameters

Parameter	Value
$\mu_{n0}C_{ox}$	175 μA/V^2
$\mu_{p0}C_{ox}$	60 μA/V^2
V_{Tn0}	0.55 V
V_{Tp0}	−0.65 V

to 5, 12 and 5, respectively. Final transistor aspect ratios as well as bias elements (i.e., I_B and V_{DD}) are reported in Table 2. The circuit was simulated using SPECTRE and, as expected, it exhibits a simulated quiescent current, I_Q, of about 90 μA. Some output stage performance parameters were evaluated in closed-loop condition, that is, using the schematic depicted in Fig. 2. In this case the output stage was fed back by a proper ideal OTA which was designed so that the overall amplifier exhibited a dc open-loop gain of 60 dB when loaded with a 500-Ω resistor. The compensation network was designed so that the worst-case phase margin of the amplifier (without load resistance) would be about 70° for a maximum capacitive load of 50 pF. Table 3 reports the OTA and the compensation network parameters while Table 4 reports the open loop gain, the transition frequency and the corresponding phase margin. The efficiency of the stage in terms of power consumption is reported in Table 5.

As far as the Quality Factors are concerned, they are summarized in Tables 6–8. As forecasted, the bias current of the driver is about the 20% of the quiescent current of the final stage. The analytical value of Q_C(=0.2) is therefore in agreement with the simulated value. Quality Factor Q_B is reported in Table 7. The simulated Q_B is the ratio between the simulated second pole of the loop gain, ω_2, and the estimated second pole of the normal stage. The analytical Q_B is evaluated from (21a). Also in this case an excellent agreement is apparent. Similarly, for the third Quality Factor, we simulated the *THD* in closed loop

Table 2 Output stage design parameters

Parameter	SDI stage	LV stage
MI	–	45/0.6
MNIA, MNIB	25/0.3	–
MPIA, MPIB	75/0.3	–
M1	–	15/0.6
MN1A, MN1B	5/0.3	–
MP1A, MP1B	15/0.3	–
M2	–	15/0.6
M3	–	15/0.6
MN4	–	3/0.6
MND	5/0.3	3/0.6
MP4	–	9/0.6
MPD	15/0.3	9/0.6
MNO	60/0.3	150/0.6
MPO	180/0.3	450/0.6
I_B	1.5 μA	–
I_{B1}	–	8 μA
I_{B2}	–	12 μA
V_{BN}	–	725 mV
V_{BP}	–	160 mV
V_{DD}	3 V	1 V

Table 3 OTA and compensation network parameters

	G_{MOTA} (μA/V)	R_{OTA} (MΩ)	C_C (pF)	R_C (Ω)
SDI stage	500	1	20	300
LV stage	100	1	2	60

Table 4 Simulated amplifier frequency performance

	A_0 (dB)	f_T (MHz)	M_φ (deg)
SDI stage	60	2.72	73.7
LV stage	60	8.61	69.0

Table 5 Efficiency simulations

	P_{LOAD} (simulated) (μW)	P_{SUPPLY} (simulated) (μW)	η (simulated) (%)
SDI stage	90.82	279.6	32.5
LV stage	92.56	236.6	39.1

configuration in terms of the first two harmonic distortion factors (i.e., HD_2 and HD_3), as shown in Fig. 12. As expected, the main contribution to nonlinearity comes from HD_3 which is lower than −80 dB up to 2.5 V_{pp} of the output voltage. The open-loop *THD* reported in Table 8 is evaluated multiplying the simulated closed-loop *THD* (−84.65 dB at 750-mV output voltage) by the overall loop

Table 6 Quiescent current and Q_C

	I_Q (simulated) (μA)	I_{DR} (simulated) (μA)	Q_C (simulated)	Q_C (analytical)
SDI stage	108.7	20.4	0.19	0.20
LV stage	94.61	31.57	0.33	0.32

Table 7 Bandwidth performance (open-loop second pole) and Q_B

	ω_2 (simulated) (Mrad/s)	ω_{2NORM} (estimated) (Mrad/s)	Q_B (simulated)	Q_B (analytical)
SDI stage	81.2	85.4	0.95	1.02
LV stage	382	81.6	4.68	4.35

Table 8 THD and Q_D

	Open-loop THD (simulated, dB)	Q_D (simulated)	Q_D (analytical)
SDI stage	−24.65	12.59×10^{-3}	13.02×10^{-3}
LV stage	−25.18	11.59×10^{-3}	13.75×10^{-3}

gain of the amplifier (60 dB) [4]. Finally, we evaluated the simulated Q_D reported in the second column of Table 8, which is in agreement with the analytical Q_D evaluated from (21c).

5.2 Low-voltage CMOS output stage

The LV stage was designed following the design comments of Sect. 4.2.3, therefore parameter α was set to 0.2 and n was set to 50. Parameter γ was set to 5 while m (which actually does not play any role in the Quality Factors) was set to 3. Final transistor aspect ratios as well as bias elements are shown in Table 2. The circuit was simulated using SPECTRE and, as expected, it exhibits a simulated quiescent current, I_Q, of about 100 μA. The output stage was fed back by a proper ideal OTA which was designed so that the overall amplifier exhibited a dc open-loop gain of 60 dB when loaded with a 500-Ω resistor. The compensation network was designed so that the worst-case phase margin of the amplifier (without load resistance) would be about 70° for a maximum capacitive load of 50 pF. Table 3 reports the OTA and the compensation network parameters while Table 4 reports the open loop gain, the transition frequency and the corresponding phase margin. The efficiency of the stage in terms of power consumption is reported in Table 5.

The Quality Factors are summarized in Tables 6–8. The bias current of the driver is about the 33% of the quiescent current of the final stage. The analytical value of Q_C (=0.32) is therefore in agreement with the simulated value. Quality Factor Q_B is reported in Table 7. Note the superior performance of this stage with respect to bandwidth/dissipation performance. Also in this case an excellent agreement is apparent between the simulated and the analytical value of Q_B. As a final step, we simulated the *THD* as shown in Fig. 13. The same figure reports the *THD* for a LV stage designed as in the original work, also (see the Appendix A for details). In this latter case the circuit is asymmetric and the worst *THD* behavior is due to HD_2 which dominates over the whole output range. The poor *THD* performance of the original stage may be evinced by comparing the Quality Factor Q_D in (35c), which refers to our design, to the Quality Factor Q_D in (A.21), which refers to the same stage designed as in the original work. Once again, the open-loop *THD* reported in Table 8 is evaluated multiplying the simulated closed-loop *THD* (−85.18 dB at 300-mV output voltage) by the overall loop gain of the amplifier (60 dB) [4]. Finally, the simulated Q_D reported in the second column of Table 8 is in agreement with the analytical Q_D evaluated from (35c).

6 Conclusions

In this article, we have presented useful guidelines for designing output stages. Three Quality Factors, which were previously introduced to analyze and compare different output stages, are used to design two CMOS class-AB stages. It has been shown that using the proposed Quality Factors and the related strategy that arises from their adoption, leads to an efficient design in terms trade-off among area, current consumption, bandwidth and distortion. Indeed, for one of the two stages adopted as example, the design through the Quality Factors resulted in superior distortion performance with respect to the design suggested in the original article. Design examples and simulations were provided to validate the design strategies.

Appendix A

In the original work, the LV stage was designed setting [26]

$$\left(\frac{W}{L}\right)_2 = (1+\alpha)\left(\frac{W}{L}\right)_3 \tag{A.1a}$$

$$I_{B1} = I_B \tag{A.1b}$$

$$I_{B2} = (1+\alpha)I_B \tag{A.1c}$$

As we shall see from the Quality Factor analysis, this strongly degrades the harmonic distortion with respect to the design procedure of Sect. 4.2 where aspect ratios of M2 and M3 and bias currents I_{B1} and I_{B2} were set as in (23).

By inspection, it is easy to show that

$$I_Q = n\,\alpha\, I_B \tag{A.2}$$

$$I_{TOT} = \left(1 + \frac{3+2\alpha}{n\,\alpha}\right) I_Q \tag{A.3}$$

$$G_{Mout} = (2+\alpha) n\, g_{mI} = (2+\alpha)\sqrt{\frac{\gamma}{\alpha}}\, g_{mO} \tag{A.4}$$

Due to the different transconductance factor of M2 and M3,[1] the circuit is asymmetric and HD_2 dominates over HD_3. To evaluate HD_2, we exploit the approach suggested in [30] and compared in [29]. The method, properly modified, shows that the second harmonic distortion factor arises due to the two different paths that process large positive and negative signals. Specifically, if $v_{IN} = V_A \sin(\omega\, t)$, assuming that V_{PO} and V_{NO} are the values that the output voltage assumes when v_{IN} equals $-V_A$ and V_A, respectively, the second harmonic distortion component is given by

$$HD_2 = \left(\frac{3}{2} - \frac{16}{5\pi}\right)\left|\frac{V_{PO}+V_{NO}}{V_{PO}-V_{NO}}\right| \approx 0.48\left|\frac{V_{PO}+V_{NO}}{V_{PO}-V_{NO}}\right| \tag{A.5}$$

Assuming the circuit in Fig. 8 is designed following the constraints in (A.1), large positive signals are processed by MI, the current mirror M1–M3 and the adaptive stage MN4–MND–MNO (for large positive signals, the current through the other adaptive stage is negligible). Transistor MND works in the triode region while MN4 and MNO work in the saturation region, therefore we may write

$$\begin{aligned} i_{DND} &= \beta_{ND}\left(v_{GSND} - V_T - \frac{v_{DSND}}{2}\right) v_{DSND} \\ &\approx \beta_{ND}(v_{GSND} - V_T)(V_{BN} - v_{GSN4}) \end{aligned} \tag{A.6}$$

$$v_{GSN4} = V_T + \sqrt{\frac{i_{DND}}{\frac{\beta_{N4}}{2}}} \tag{A.7}$$

$$i_{DNO} = \frac{\beta_{NO}}{2}(v_{GSND} - V_T)^2 \tag{A.8}$$

Substituting (A.7) in (A.6), we obtain

$$v_{GSND} - V_T = \frac{\frac{i_{DND}}{\beta_{ND}}}{V_{BN} - V_T - \sqrt{\frac{i_{DND}}{\frac{\beta_{N4}}{2}}}} \tag{A.9}$$

and (A.8) becomes

$$i_{DNO} = \frac{\beta_{NO}}{2}\left(\frac{\frac{i_{DND}}{\beta_{ND}}}{V_{BN} - V_T - \sqrt{\frac{i_{DND}}{\frac{\beta_{N4}}{2}}}}\right)^2 \tag{A.10}$$

Current i_{DND} comes from the drain of M3 and may be approximated as

$$i_{DND} \approx \alpha I_B + g_{mI} v_{IN} \tag{A.11}$$

Large negative signals are processed by MI, the current mirror M1–M2 and the adaptive stage MP4–MPD–MPO. For i_{DPO} and i_{DPD} expressions similar to (A.10) and (A.11) hold, specifically

$$i_{DPO} = \frac{\beta_{PO}}{2}\left(\frac{\frac{i_{DPD}}{\beta_{PD}}}{(V_{DD} - V_{BP}) - V_T - \sqrt{\frac{i_{DPD}}{\frac{\beta_{P4}}{2}}}}\right)^2 \tag{A.12}$$

$$i_{DPD} \approx \alpha I_B - (1+\alpha) g_{mI} v_{IN} \tag{A.13}$$

Since for large signals v_{OUT} equals $R_L i_{DPO}$ for $v_{IN} < 0$ and $-R_L i_{DNO}$ for $v_{IN} > 0$, we have for V_{PO} and V_{NO}

$$\begin{aligned} V_{PO} &= \frac{\beta_{PO} R_L}{2}\left(\frac{\frac{\alpha I_B + (1+\alpha) g_{mI} V_A}{\beta_{PD}}}{(V_{DD} - V_{BP}) - V_T - \sqrt{\frac{\alpha I_B + (1+\alpha) g_{mI} V_A}{\frac{\beta_{P4}}{2}}}}\right)^2 \\ &\approx K[\alpha I_B + (1+\alpha) g_{mI} V_A]^2 \end{aligned} \tag{A.14}$$

$$\begin{aligned} V_{NO} &= -\frac{\beta_{NO} R_L}{2}\left(\frac{\frac{\alpha I_B + g_{mI} V_A}{\beta_{ND}}}{V_{BN} - V_T - \sqrt{\frac{\alpha I_B + g_{mI} V_A}{\frac{\beta_{N4}}{2}}}}\right)^2 \\ &= -K(\alpha I_B + g_{mI} V_A)^2 \end{aligned} \tag{A.15}$$

where the approximation in (A.14) takes into account the fact that in the denominator $1 + \alpha \approx 1$ and, due to the stage symmetry, K is

$$\begin{aligned} K &= \frac{\frac{\beta_{PO} R_L}{2\beta_{PD}^2}}{\left((V_{DD} - V_{BP}) - V_T - \sqrt{\frac{\alpha I_B + g_{mI} V_A}{\frac{\beta_{P4}}{2}}}\right)^2} \\ &= \frac{\frac{\beta_{NO} R_L}{2\beta_{ND}^2}}{\left(V_{BN} - V_T - \sqrt{\frac{\alpha I_B + g_{mI} V_A}{\frac{\beta_{N4}}{2}}}\right)^2} \end{aligned} \tag{A.16}$$

Substituting (A.14) and (A.15) in (A.5) we have

$$HD_2 = 0.48\frac{\alpha g_{mI} V_A[(2+\alpha) g_{mI} V_A + 2\alpha I_B]}{2(g_{mI} V_A + \alpha I_B)^2} \tag{A.17}$$

which, considering that $i_{L(MAX)} = G_{Mout} V_A = (2+\alpha) n g_{mI} V_A$ and $I_Q = n\alpha I_B$, may be written as

$$\begin{aligned} HD_2 &= 0.48\frac{\alpha}{2+\alpha}\frac{i_{L(MAX)}}{I_Q}\frac{1 + \frac{i_{L(MAX)}}{2I_Q}}{\left[1 + \frac{i_{L(MAX)}}{(2+\alpha) I_Q}\right]^2} \\ &\approx 0.48\frac{\alpha}{2+\alpha}\frac{\frac{i_{L(MAX)}}{I_Q}}{1 + \frac{i_{L(MAX)}}{(2+\alpha) I_Q}} \end{aligned} \tag{A.18}$$

[1] Their aspect ratios are set in (A.1a) and it is easy to show that $I_{D2} = (1+\alpha) I_{D3}$. Therefore $g_{m2} = (1+\alpha) g_{m3}$.

where the approximation holds for $2 + \alpha \approx 2$. Note that, if $i_{L(MAX)} \gg I_Q$, HD_2 is almost constant and equal to 0.48α.

From (A.2) to (A.4) and (A.18) we may evaluate the Quality Factors, which result

$$Q_C = \frac{1}{n}\left(2 + \frac{3}{\alpha}\right) \tag{A.19}$$

$$Q_B = \frac{2+\alpha}{2}\sqrt{\frac{\gamma n}{\alpha(n+2)+3}} \tag{A.20}$$

$$Q_D = 0.48\frac{\alpha}{2+\alpha}\frac{1+\frac{3+2\alpha}{n\alpha}}{1+\frac{i_{L(MAX)}}{(2+\alpha)I_Q}} \tag{A.21}$$

Comparing (A.21) with (37) reveals that, for typical values of $i_{L(MAX)}$ and I_Q, the LV stage has better linearity performance if designed taking into account constraints (23)–(24) instead of (A.1) as in the original work.

Appendix B

Following the paths composed of the gate-source voltages of MNIB–MPIA–MP1A–MN1A and MNIA–MPIB–MP1B–MN1B, we obtain

$$\begin{aligned}&\left(V_{CM}+\frac{v_{IN}}{2}\right)-\left(V_{CM}-\frac{v_{IN}}{2}\right)\\&\quad=V_{TNIB}+\sqrt{\frac{2i_{DPD}}{\beta_{NIB}}}+V_{TPIA}+\sqrt{\frac{2i_{DPD}}{\beta_{PIA}}}-V_{TP1A}\\&\qquad-\sqrt{\frac{2I_B}{\beta_{P1A}}}-V_{TN1A}-\sqrt{\frac{2I_B}{\beta_{N1A}}}\end{aligned} \tag{B.1a}$$

$$\begin{aligned}&\left(V_{CM}-\frac{v_{IN}}{2}\right)-\left(V_{CM}+\frac{v_{IN}}{2}\right)\\&\quad=V_{TNIA}+\sqrt{\frac{2i_{DND}}{\beta_{NIA}}}+V_{TPIB}+\sqrt{\frac{2i_{DnD}}{\beta_{PIB}}}-V_{TP1B}\\&\qquad-\sqrt{\frac{2I_B}{\beta_{P1B}}}-V_{TN1B}-\sqrt{\frac{2I_B}{\beta_{N1B}}}\end{aligned} \tag{B.1b}$$

In MOS circuits mismatch can affect the gain factor, β, and the threshold voltage, V_T. However, in analog circuits, where small $V_{GS} - V_T$ are set, mismatch in threshold voltages is dominant with respect to mismatch in gain factors [31]. Therefore, referring to the circuit in Fig. 4, we may assume that the mismatch of the aspect ratio of two NMOS transistors is negligible and that the same holds between two PMOS transistors. More specifically, the ratios of MNIA–MN1A, MNIB–MN1B, MPIA–MP1A and MPIB–MP1B still remain m, the ratios of MNIA–MND, MNIB–MND, MPIA–MPD and MPIB–MPD remain γ and, finally, the ratios of MPO–MPD and MNO–MND remain n. NMOS and PMOS transistors, however, behave differently and, in case of mismatch, the condition that $\beta_{Ni} = \beta_{Pi}$ cannot be guaranteed anymore and must be taken into account.

Considering our assumptions on mismatch, relationships (B.1) become

$$v_{IN} = \Delta V_{TN1} + \Delta V_{TP1} + 2\sqrt{\frac{2i_{DPD}}{\beta_I^*}} - 2\sqrt{\frac{2mI_B}{\beta_I^*}} \tag{B.2a}$$

$$-v_{IN} = \Delta V_{TN2} + \Delta V_{TP2} + 2\sqrt{\frac{2i_{DPD}}{\beta_I^*}} - 2\sqrt{\frac{2mI_B}{\beta_I^*}} \tag{B.2b}$$

where we defined

$$\Delta V_{TN1} = V_{TNIB} - V_{TN1A} \tag{B.3a}$$

$$\Delta V_{TP1} = V_{TPIA} - V_{TP1A} \tag{B.3b}$$

$$\Delta V_{TN2} = V_{TNIA} - V_{TN1B} \tag{B.3c}$$

$$\Delta V_{TP2} = V_{TPIB} - V_{TP1B} \tag{B.3d}$$

and

$$\frac{1}{\sqrt{\beta_I^*}} = \frac{1}{2}\left(\frac{1}{\sqrt{\beta_{NIB}}} + \frac{1}{\sqrt{\beta_{PIA}}}\right) \tag{B.3e}$$

Solving (B.2) for currents i_{DPD} and i_{DND} yields

$$i_{DPD} = \frac{\beta_I^*}{2}\left(\frac{v_{IN}}{2} - \frac{\Delta V_{TN1} + \Delta V_{TP1}}{2} + \sqrt{\frac{2mI_B}{\beta_I^*}}\right)^2 \tag{B.4a}$$

$$i_{DND} = \frac{\beta_I^*}{2}\left(-\frac{v_{IN}}{2} - \frac{\Delta V_{TN2} + \Delta V_{TP2}}{2} + \sqrt{\frac{2mI_B}{\beta_I^*}}\right)^2 \tag{B.4b}$$

which, neglecting higher order terms (i.e., ΔV_T^2), become

$$\begin{aligned}i_{DPD} = {} & mI_B + g_{mI}\frac{v_{IN}}{2} + \frac{\beta_I^*}{2}\left(\frac{v_{IN}}{2}\right)^2 - \beta_I^*\frac{\Delta V_{TN1} + \Delta V_{TP1}}{2}\frac{v_{IN}}{2}\\&- g_{mI}\frac{\Delta V_{TN1} + \Delta V_{TP1}}{2}\end{aligned} \tag{B.5a}$$

$$\begin{aligned}i_{DND} = {} & mI_B - g_{mI}\frac{v_{IN}}{2} + \frac{\beta_I^*}{2}\left(\frac{v_{IN}}{2}\right)^2 + \beta_I^*\frac{\Delta V_{TN2} + \Delta V_{TP2}}{2}\frac{v_{IN}}{2}\\&- g_{mI}\frac{\Delta V_{TN2} + \Delta V_{TP2}}{2}\end{aligned} \tag{B.5b}$$

Output currents i_{DNO} and i_{DPO} are obtained through mirrors MND–MNO and MPD–MPO, respectively, and, considering statistical deviations of threshold voltages they are [31]

$$i_{DPO} = ni_{DPD} + g_{mO}\Delta V_{TP3} \tag{B.6a}$$

$$i_{DNO} = ni_{DND} + g_{mO}\Delta V_{TN3} \tag{B.6b}$$

being g_{mO} the small signal transconductance of both MNO and MPO, $\Delta V_{TP3} = -V_{TPO} + V_{TPD}$ and $\Delta V_{TN3} = -V_{TNO} + V_{TND}$. Finally, the output voltage, v_{OUT}, takes the same expression as in (12).

For evaluating HD_2 we use (A.5) where $V_{PO} = [R_L i_{DPO}]_{v_{in}=V_A}$ and $V_{NO} = [-R_L i_{DNO}]_{v_{in}=-V_A}$ are given by

$$V_{PO} = g_{mO}R_L\Delta V_{TP3} + nR_L\left[mI_B + g_{mI}\frac{V_A}{2} + \frac{\beta_I^*}{2}\left(\frac{V_A}{2}\right)^2 - \left(\frac{\beta_I^*}{2}\frac{V_A}{2} + \frac{g_{mI}}{2}\right)(\Delta V_{TN1} + \Delta V_{TP1})\right] \quad \text{(B.7a)}$$

$$V_{NO} = -g_{mO}R_L\Delta V_{TN3} - nR_L\left[mI_B + g_{mI}\frac{V_A}{2} + \frac{\beta_I^*}{2}\left(\frac{V_A}{2}\right)^2 - \left(\frac{\beta_I^*}{2}\frac{V_A}{2} + \frac{g_{mI}}{2}\right)(\Delta V_{TN2} + \Delta V_{TP2})\right] \quad \text{(B.7b)}$$

Hence, HD_2 results

$$HD_2 \approx 0.48\frac{\left|\frac{\Delta V_{TP3}-\Delta V_{TN3}}{\sqrt{\gamma}} - \frac{1}{2}\left(\frac{\beta_I^*}{g_{mI}}\frac{V_A}{2}+1\right)(\Delta V_{TN1} + \Delta V_{TP1} - \Delta V_{TN2} - \Delta V_{TP2})\right|}{\frac{2mI_B}{g_{mI}}\left[1 + \frac{g_{mI}}{mI_B}\frac{V_A}{2} + \frac{\beta_I^*}{2mI_B}\left(\frac{V_A}{2}\right)^2\right]} \quad \text{(B.8)}$$

Some simplifications based on reasonable assumptions can be made in (B.8). First of all, we may presume that in the denominator the main contribution is given by the addend containing V_A. Then we may suppose that all ΔV_{Ti} gives the same contribution. Hence we have

$$HD_2 \approx 0.48\frac{\frac{\beta_I^* V_A}{g_{mI}}|\Delta V_T|}{\frac{2mI_B}{g_{mI}}\left[1 + \frac{g_{mI}}{mI_B}\frac{V_A}{2} + \frac{\beta_I^*}{2mI_B}\left(\frac{V_A}{2}\right)^2\right]} \approx 0.48\frac{\left(\frac{g_{mI}V_A}{4mI_B}\right)}{1 + 2\left(\frac{g_{mI}V_A}{4mI_B}\right) + \left(\frac{g_{mI}V_A}{4mI_B}\right)^2}\left(\frac{g_{mI}|\Delta V_T|}{mI_B}\right) \quad \text{(B.9)}$$

where the latter term results after a few algebra. Equation (B.9) has a maximum for $V_A = 4mI_B/g_{mI}$ for which HD_2 results

$$HD_2^{(\max)} \approx \frac{0.48}{4}\frac{g_{mI}}{mI_B}|\Delta V_T| \quad \text{(B.10)}$$

Comparing (B.10) with (20) (i.e., $HD_3 \approx \frac{1}{48}\frac{g_{mI}}{mI_B}V_A$), it is easy to show that HD_3 is larger than HD_2 for $V_A > 6|\Delta V_T|$, that is, for a typical case of $|\Delta V_T| \approx 25$ mV, when V_A is above about 150 mV. As a consequence, even in the presence of mismatch, HD_3 dominates over HD_2 for the SDI topology.

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Walter Aloisi Walter Aloisi was born in Catania, Italy, in 1973. He received the Laurea degree (cum laude) in Electronic Engineering from University of Catania, Catania, Italy, in 1999, discussing his thesis whose main topic was the design of integrated linear regulator with low quiescent current. Since then he worked, as Ph.D. student, at the Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi (DIEES) of the same University. In 2003 he received the Ph.D. degree in Electronics and Automation Engineering from University of Catania, discussing a thesis on the design of low-voltage CMOS SC Filters for high-frequency applications. His research interests include analysis, modeling and design of analog integrated circuits and systems with particular emphasis on linear regulator, switching regulator and both low-voltage and low-power circuits.

Giuseppe Di Cataldo Giuseppe Di Cataldo received the Laurea degree in Electronic Engineering from the Politecnico di Milano in 1972. Since 1974 he has been Assistant Professor of Applied Electronic in the University of Catania. Currently he is full Professor of Applied Electronic in the same University. His past scientific activity was mainly devoted in digital filtering design, the neural networks and circuit theory. At present his research interests include the signal elaboration, the VLSI architectures and microsystem design.

Gianluca Giustolisi Gianluca Giustolisi was born in Catania, Italy, in 1971. He received the Laurea degree (cum laude) in Electronic Engineering from University of Catania in 1995. Up to 1999, he remained, as Ph.D. student, at the Dipartimento Elettrico Elettronico e Sistemistico (DEES) of the same University. In 1999 he received the Ph.D. degree discussing his thesis on the design of a CMOS Fuzzy controller based on the Switched Capacitor approach. In 2002, he joined the Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi (DIEES) as an Assistant Professor. Then, he became an Associate Professor in 2005. In the academic years 1998/1999 and 1999/2000 he held the course of Microelectronics for the diploma degree in Electronic Engineering. From 2003 to 2005, he held the course of Analog Electronics II for the laurea degree in Automation Engineering. Since 2003 he has been teaching the course of Electronic Devices for the laurea degree in Electronic Engineering. His research interests include analysis, modeling and design of analog integrated circuits and systems with particular emphasis on compensation techniques, Fuzzy integrated circuits, non-linear applications and both LV and low-power circuits. He is author of more than 50 scientific papers on international journals and conferences. He is also author of the textbook Introduzione ai dispositivi elettronici, published by Franco Angeli in 2005.

Gaetano Palumbo Gaetano Palumbo was born in Catania, Italy, in 1964. He received the laurea degree in Electrical Engineering in 1988 and a Ph.D. degree from the University of Catania in 1993. Since 1993 he conducts courses on Electronic Devices, Electronics for Digital Systems and Basic Electronics. In 1994 he joined the Dipartimento Elettrico Elettronico e Sistemistico (DEES), now Dipartimento di Ingegneria

Elettrica Elettronica e dei Sistemi (DIEES), at the University of Catania as a researcher, subsequently becoming an Associate Professor in 1998. Since 2000 he is a full Professor in the same department. His primary research interest has been analog circuits with particular emphasis on feedback circuits, compensation techniques, current-mode approach, LV circuits. Then, his research has also embraced digital circuits with emphasis on bipolar and MOS current-mode digital circuits, adiabatic circuits, and high-performance building blocks focused on achieving optimum speed within the constraint of low power operation. In all these fields he is developing some the research activities in collaboration with STMicroelectronics of Catania. He was the co-author of three books "CMOS Current Amplifiers" and "Feedback Amplifiers: theory and design" and "Model and Design of Bipolar and MOS Current-Mode Logic (CML, ECL and SCL Digital Circuits)" all by Kluwer Academic Publishers, in 1999, 2001 and 2005, respectively, and a textbook on Electronic Device in 2005. He is the author of 300 scientific papers on referred international journals (over 120) and in conferences. Moreover he is co-author of several patents. Since June 1999 to the end of 2001 and since 2004 to 2005 he served as an Associated Editor of the *IEEE Transactions on Circuits and Systems Part I* for the topic "Analog Circuits and Filters" and "digital circuits and systems", respectively. Since 2006 he is serving as an Associated Editor of the *IEEE Transactions on Circuits and Systems Part II*. In 2005 he was one of the 12 panelists in the scientific-disciplinare area 09—industrial and information engineering of the Committee for Evaluation of Italian Research (CIVR), which has the aim to evaluate the Italian research in the above area for the period 2001–2003. In 2003 he received the Darlington Award. He is an IEEE Fellow.