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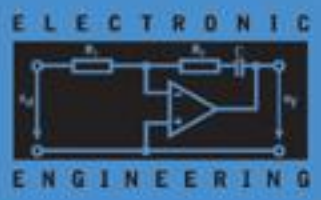

RF and Microwave Power Amplifier Design

- ✔ Active device modeling
- ✔ High-power amplifier design
- ✔ High-efficiency operation techniques
- ✔ Broadband power amplifiers
- ✔ Wireless communications applications

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Contents

Preface

The main objective of this book is to present all the relevant information required for RF and micro-wave power amplifier design including well-known and novel theoretical approaches and practical design techniques as well as to suggest optimum design approaches effectively combining analytical calculations and computer-aided design. This book can also be very useful for lecturing to promote the analytical way of thinking with practical verification by making a bridge between theory and practice of RF and microwave engineering. As it often happens, a new result is the well-forgotten old one. Therefore, the demonstration of not only new results based on new technologies or circuit schematics is given, but some sufficiently old ideas or approaches are also introduced, that could be very useful in modern practice or could contribute to appearance of new ideas or schematic techniques.

As a result, this book is intended for and can be recommended to:

- *University-level professors and scientists*, as possible reference and well-founded material for creative research and teaching activity that will contribute to strong background for graduate and postgraduate students
- *R & D staff*, to combine the theoretical analysis and practical aspect including computer-aided design and to provide a sufficient basis for new ideas in theory and practical circuit technique
- *Practicing RF designers and engineers*, as an anthology of many well-known and new practical RF and microwave power amplifier circuits with detailed description of their operational principles and applications and clear practical demonstration of theoretical results

In Chapter 1, the two-port networks are introduced to describe the behavior of linear and nonlinear circuits. To characterize the nonlinear properties of the bipolar or field-effect transistors, their equivalent circuit elements are expressed through the impedance Z-parameters, admittance Y-parameters, or hybrid H-parameters. On the other hand,

the transmission *ABCD*-parameters are very important in the design of the distributed circuits as a transmission line or cascaded elements, whereas the scattering *S*-parameters are widely used to simplify a measurement procedure.

The main purpose of Chapter 2 is to present widely used nonlinear circuit design techniques to analyze nonlinear power amplifier circuits. In general, there are several approaches to analyze and design these nonlinear circuits, depending on their main specifications—for example, an analysis in time domain when it is necessary to determine the transient circuit behavior or in frequency domain to provide improvement of the power and spectral performances when both parasitic effects such as instability and spurious effects must be eliminated or minimized. Using the time-domain technique it is quite easy to describe the circuit by differential equations, whereas frequency-domain analysis is more explicit when a relatively complex circuit can be reduced to one or more sets of immitances at each harmonic component.

In Chapter 3, all the necessary steps to provide an accurate device modeling procedure starting with the determination of the small-signal equivalent circuit parameters are described and discussed. A variety of nonlinear models for MOSFET, MESFET, HEMT, and bipolar devices including HBTs, which are very prospective for modern microwave monolithic integrated circuits of power amplifiers and oscillators, are presented. In order to highlight the advantages or drawbacks of one nonlinear device model over the other, a comparison of the measured and modeled volt-ampere and voltage-capacitance characteristics or a frequency range of model application is made.

A concept of impedance matching and the impedance-matching technique, which is very important when designing power amplifiers, is presented in Chapter 4. First, the main principles and impedance-matching tools such as the Smith chart are described, giving the starting point of the matching-design procedure. As an engineering solution in general depends on the different circuit requirements, the designer should choose the optimum solution among a variety of the matching networks including either lumped elements or transmission lines or both of them. To simplify and visualize the matching-design procedure, an analytical approach, which allows calculating the parameters of the matching circuits using simple equations, and Smith chart traces is discussed and illustrated with several examples of the narrowband and broadband RF and microwave power amplifiers using bipolar or MOSFET devices. Finally, the design formulas and curves are presented for different types of transmission lines including stripline, microstrip line, slotline, and coplanar waveguide.

Chapter 5 describes the basic properties of three-port and four-port networks as well as a variety of different combiners, transformers, and

directional couplers for RF and microwave power applications. So, for power combining in view of insufficient power performance of the active devices, it is best to use the coaxial cable combiners with ferrite core to combine the output powers of RF power amplifiers intended for wideband applications. As the device output impedance for high power levels is usually too small, to match this impedance with a standard 50-Ω load, it is necessary to use the co-axial line transformers with specified impedance transformation. For narrowband applications, the *N*-way Wilkinson combiners are widely used due to the simplicity of their practical realization. At the same time in microwaves, the size of the combiners should be very small. Therefore, the commonly used hybrid microstrip combiners including different types of microwave hybrid and directional couplers are described and analyzed.

Chapter 6 represents the fundamentals of the power amplifier design, which is generally a complicated procedure when it is necessary to provide simultaneously accurate active device modeling, effective impedance matching depending on the technical requirements and operation conditions, stability in operation, and ease in practical implementation. Therefore, at the beginning of the chapter the key definitions of different power gains and stability are introduced. For a stable operation mode of the power amplifier, it is necessary to evaluate the operating frequency domains where the active device may be potentially unstable. To avoid parasitic oscillations, the stabilization circuit technique for different frequency domains from low frequencies to high frequencies close to the device transition frequency is analyzed and discussed. One of the key parameters of the power amplifier is its linearity, which is very important for many TV and cellular applications. Therefore, the relationships between the output power, 1-dB gain compression point, third-order intercept point, and intermodulation distortions of the third and higher orders are given and illustrated for different active devices. The basic classes of the power amplifier operation A, AB, B, and C are introduced, analyzed, and illustrated. The device biasing conditions and examples of bias circuits for MOSFET and bipolar devices to improve linearity or to increase efficiency are shown and discussed. Also the concept of push-pull amplifiers and their circuit design using balanced transistors is given. In the final section, the numerous practical examples of power amplifiers using MOSFET, MESFET, and bipolar devices in different frequency ranges and for output powers are shown and discussed.

Modern commercial and military communication systems require high-efficiency long-term operating conditions. Chapter 7 describes in detail the possible circuit solutions to provide a high-efficiency power amplifier operation based on using different overdriven (Class B, Class F, and Class E) classes of operation or newly developed subclasses,

depending on the technical requirements. In Class F amplifiers analyzed in frequency domain, the fundamental and harmonic load impedances are optimized by short-circuit termination and open-circuit peaking in order to control the voltage and current waveforms at the drain of the device to obtain maximum efficiency. In Class E amplifiers analyzed in time domain, an efficiency improvement is achieved by realizing the on/off switching operation with special current and voltage waveforms so that high voltage and high current do not exist at the same time. The parallel-circuit Class E load network configuration can be easily implemented in the broadband high-efficiency power amplifier design. The Class E load network with a quarterwave transmission line provides an addidtional suppression of even harmonic components.

In many telecommunication, radar or testing systems, the transmitters operate in a very wide frequency range. Chapter 8 describes the power amplifier design based on a broadband concept that provides some advantages when there is no need to tune the resonant circuit parameters. However, there are many factors that restrict the frequency bandwidth depending on the active device parameters. So, it is sufficicently easy to provide multioctave amplification from very low frequencies up to ultrahigh frequencies using the power MOSFET devices when loss gain compensation is easily realized. At higher frequencies when the device input impedance is significantly smaller and the influence of its internal feedback and parasitic parameters is substantially higher, it is necessary to use multisection-matching networks with lumped and distributed elements. A variety of broadband power amplifiers using different frequency ranges are presented and described.

Chapter 9 describes the different approaches to improve linearity and efficiency of the power amplifiers in telecommunication systems. To improve the efficiency of operation, the Kahn envelope and restoration and envelope-tracking techniques, the outphasing and Doherty power amplifier archi-tectures, and the switched-mode and dual-path power amplifier configurations are shown and analyzed. To improve the linearity of operation, the feedforward linearizing technique and predistoration linearization circuit schematics are described and presented. Special attention is payed to practical realization of monolithic integrated circuits of HBT and CMOS power amplifiers for handset applications using modern technologies.

Andrei Grebennikov

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Chapter

1

Two-Port Network Parameters

Two-port-equivalent circuits are widely used in radio frequency (RF) and microwave circuit design to describe the electrical behavior of both active and passive devices. A two-port network (whose elements are expressed through the impedance Z-parameters, admittance Y parameters, or hybrid H-parameters) is most suitable to characterize the nonlinear properties of the active devices, bipolar or field-effect transistors, when designing power amplifiers or oscillators. Transmission $ABCD$-parameters of a two-port network are very convenient for designing the distributed circuit as transmission lines or cascaded elements. Scattering S-parameters are used to simplify the measurement procedure.

This chapter discusses the main properties of two-port network parameters, as well as the ratios between the different systems. In addition, examples are given to illustrate how to best analyze power amplifiers and oscillators. The final part of this chapter describes the transmission line and its main parameters. Additional information on more specific aspects of two-port network circuits can be found in Refs. [1–4] listed at the end of the chapter.

Traditional Network Parameters

The basic diagram of a two-port nonautonomous transmission system can be represented by the equivalent circuit shown in Fig. 1.1, where V_S is the independent voltage source, Z_S is the source impedance, LN is the linear time-invariant two-port network without independent source, and Z_L is the load impedance. Two independent phasor currents, I_1 and I_2 (flowing across input and output terminals), and phasor voltages,

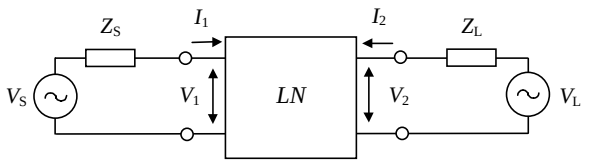


Figure 1.1 Basic diagram of two-port nonautonomous transmission system.

V_1 and V_2, characterize such a two-port network. For autonomous oscillator systems, in order to provide an appropriate analysis in the frequency domain of the two-port network in the negative one-port representation, it is sufficient to set the source impedance to infinity. For power amplifier and oscillator design, the elements of the matching or resonant circuits, which are assumed to be linear or appropriately linearized, can be found among the LN-network elements, or additional two-port linear networks can be used to describe their frequency domain behavior.

For a two-port network, the following equations can be considered to be imposed boundary conditions:

$$V_1 + Z_S I_1 = V_S \tag{1.1}$$

$$V_2 + Z_L I_2 = V_L \tag{1.2}$$

Suppose that it is possible to obtain a unique solution for the linear time-invariant circuit shown in Fig. 1.1. Then the two linearly independent equations, which describe the general two-port network representation in terms of circuit variables V_1, V_2, I_1, and I_2, can be expressed in matrix form as

$$[M][V] + [N][I] = 0 \tag{1.3}$$

or

$$\left.\begin{aligned} m_{11}V_1 + m_{12}V_2 + n_{11}I_1 + n_{12}I_2 = 0 \\ m_{21}V_1 + m_{22}V_2 + n_{21}I_1 + n_{22}I_2 = 0 \end{aligned}\right\} \tag{1.4}$$

In Eq. (1.3), the complex 2×2 matrices $[M]$ and $[N]$ are independent of the source and load impedances Z_S and Z_L and voltages V_S and V_L, respectively; they depend only on the circuit elements inside the LN network.

If matrix $[M]$ in Eq. (1.3) is nonsingular when $|M| \neq 0$, then this matrix equation can be rewritten in terms of $[I]$ as

$$[V] = -[M]^{-1}[N][I] = [Z][I] \tag{1.5}$$

where $[Z]$ is the open-circuit impedance two-port network matrix. In scalar form, matrix Eq. (1.5) is given by

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \tag{1.6}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \tag{1.7}$$

where Z_{11} and Z_{22} are the open-circuit driving-point impedances, and Z_{12} and Z_{21} are the open-circuit transfer impedances of the two-port network. The voltage components V_1 and V_2, due to the input current I_1 are found by defining $I_2 = 0$ in Eqs. (1.6) and (1.7), which results in an open output terminal. Similarly, the same voltage components V_1 and V_2 are determined by setting $I_1 = 0$ when the input terminal becomes open-circuited. The resulting driving-point impedances can be written as follows:

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} \tag{1.8}$$

The two transfer impedances are

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} \tag{1.9}$$

Dual analysis can be used to derive the short-circuit admittance matrix when the current components I_1 and I_2 are considered as outputs caused by V_1 and V_2. If matrix $[N]$ in Eq. (1.3) is nonsingular when $|N| \neq 0$, this matrix equation can be rewritten in terms of $[V]$ as

$$[I] = -[N]^{-1}[M][V] = [Y][V] \tag{1.10}$$

where $[Y]$ is the short-circuit admittance two-port network matrix. In scalar form, matrix Eq. (1.10) is written as

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \tag{1.11}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \tag{1.12}$$

where Y_{11} and Y_{22} are the short-circuit driving-point admittances, and Y_{12} and Y_{21} are the short-circuit transfer admittances of the two-port network. In this case the current components I_1 and I_2, due to the input voltage source V_1, are determined by setting $V_2 = 0$ in Eqs. (1.11) and (1.12), which creates a short output terminal. Similarly, the same current components I_1 and I_2 are determined by setting $V_1 = 0$ when the input terminal becomes short-circuited. As a result, the two driving point admittances are

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \qquad Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} \tag{1.13}$$

The two transfer admittances are

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \qquad Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} \tag{1.14}$$

In some cases, an equivalent two-port network representation can be obtained to express voltage source V_1 and output current I_2 in terms of input current I_1 and output voltage V_2. By solving Eq. (1.4), if the submatrix

$$\begin{bmatrix} m_{11} & n_{12} \\ m_{21} & n_{22} \end{bmatrix}$$

is nonsingular, then

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = -\begin{bmatrix} m_{11} & n_{12} \\ m_{21} & n_{22} \end{bmatrix}^{-1} \begin{bmatrix} n_{11} & m_{12} \\ n_{21} & m_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = [H] \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \tag{1.15}$$

where $[H]$ is the hybrid two-port network matrix. In scalar form, it is best to represent matrix Eq. (1.15) as

$$V_1 = h_{11}I_1 + h_{12}V_2 \tag{1.16}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \tag{1.17}$$

where h_{11}, h_{12}, h_{21}, and h_{22} are the hybrid H-parameters. The voltage source V_1 and current component I_2 are determined by defining $V_2 = 0$ for the short output terminal in Eqs. (1.16) and (1.17):

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \tag{1.18}$$

where h_{11} is the driving-point input impedance and h_{21} is the forward current transfer function. Similarly, the input voltage source V_1 and output current I_2 are determined by defining $I_1 = 0$ when the input terminal is open-circuited:

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} \qquad h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} \tag{1.19}$$

where h_{12} is the reverse voltage transfer function and h_{22} is the driving-point output admittance.

Transmission parameters, often used for passive device analysis, are determined for independent input voltage source V_1 and input current I_1 in terms of output voltage V_2 and output current I_2. Solving Eq. (1.4), if the submatrix

$$\begin{bmatrix} m_{11} & n_{11} \\ m_{21} & n_{21} \end{bmatrix}$$

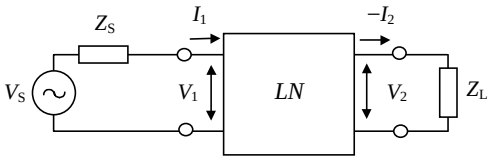


Figure 1.2 Basic diagram of loaded two-port transmission system.

is nonsingular, then we obtain

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = -\begin{bmatrix} m_{11} & n_{11} \\ m_{21} & n_{21} \end{bmatrix}^{-1} \begin{bmatrix} m_{12} & n_{12} \\ m_{22} & n_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = [ABCD] \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (1.20)$$

where [*ABCD*] is the forward transmission two-port network matrix. In scalar form, we can write

$$V_1 = AV_2 - BI_2 \quad (1.21)$$

$$I_1 = CV_2 - DI_2 \quad (1.22)$$

where A, B, C, and D are the transmission parameters. The voltage source V_1 and current component I_1 are determined by defining $I_2 = 0$ for the open output terminal in Eqs. (1.21) and (1.22):

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0} \qquad C = \left.\frac{I_1}{V_2}\right|_{I_2=0} \quad (1.23)$$

where A is the reverse voltage transfer function and C is the reverse transfer admittance. Similarly, input-independent variables V_1 and I_1 are determined by defining $V_2 = 0$ when the output terminal is short circuited:

$$B = \left.\frac{V_1}{I_2}\right|_{V_2=0} \qquad D = \left.\frac{I_1}{I_2}\right|_{V_2=0} \quad (1.24)$$

where B is the reverse transfer impedance and D is the reverse current transfer function. The reason that a minus sign is associated with I_2 in Eqs. (1.20) and (1.21) is that historically, for transmission networks, the input signal is considered as going to the input port whereas the output current is flowing to the load. The current $-I_2$ entering the load is shown in Fig. 1.2.

Scattering Parameters

The concept of incident and reflected voltage and current parameters can be illustrated by the one-port network shown in Fig. 1.3, where network impedance Z is connected to the signal source V_S with internal impedance Z_S. In a common case, the terminal current I and

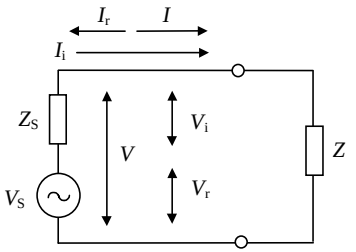


Figure 1.3 Incident and reflected voltages and currents.

voltage V consist of incident and reflected components (assume their rms values). When the load impedance Z is equal to the conjugate of source impedance expressed as $Z = Z_S^*$, the terminal current becomes the incident current. It is calculated from

$$I_i = \frac{V_S}{Z_S^* + Z_S} = \frac{V_S}{2\,\mathrm{Re}Z_S} \tag{1.25}$$

The terminal voltage, defined as the incident voltage, can be determined from

$$V_i = \frac{Z_S^* V_S}{Z_S^* + Z_S} = \frac{Z_S^* V_S}{2\,\mathrm{Re}Z_S} \tag{1.26}$$

Consequently, the incident power, which is equal to the maximum available power from the source, can be obtained by

$$P_i = \mathrm{Re}\left(V_i I_i^*\right) = \frac{|V_S|^2}{4\,\mathrm{Re}Z_S} \tag{1.27}$$

The incident power can be presented in normalized form using Eq. (1.26) as

$$P_i = \frac{|V_i|^2\,\mathrm{Re}Z_S}{\left|Z_S^*\right|^2} \tag{1.28}$$

This allows the normalized incident voltage wave a to be defined as the square root of the incident power P_i by

$$a = \sqrt{P_i} = \frac{V_i\sqrt{\mathrm{Re}Z_S}}{Z_S^*} \tag{1.29}$$

Similarly, the normalized reflected voltage wave b, defined as the square root of the reflected power P_r, can be given by

$$b = \sqrt{P_r} = \frac{V_r\sqrt{\mathrm{Re}Z_S}}{Z_S} \tag{1.30}$$

The incident power can be expressed in terms of the incident current I_i and the reflected power can be expressed in terms of the reflected

current I_r:

$$P_i = |I_i|^2 \operatorname{Re} Z_S \tag{1.31}$$

$$P_r = |I_r|^2 \operatorname{Re} Z_S \tag{1.32}$$

This allows an incident voltage wave a and reflected voltage wave b to be defined by

$$a = \sqrt{P_i} = I_i \sqrt{\operatorname{Re} Z_S} \tag{1.33}$$

$$b = \sqrt{P_r} = I_r \sqrt{\operatorname{Re} Z_S} \tag{1.34}$$

Parameters a and b also can be called *normalized incident current wave* and *normalized reflected current wave* respectively, or simply *normalized incident and reflected waves* (since the normalized current waves and the normalized voltage waves are the same parameters).

The voltage V and current I related to the normalized incident and reflected waves, a and b, can be written as

$$V = V_i + V_r = \frac{Z_S^*}{\sqrt{\operatorname{Re} Z_S}} a + \frac{Z_S}{\sqrt{\operatorname{Re} Z_S}} b \tag{1.35}$$

$$I = I_i - I_r = \frac{1}{\sqrt{\operatorname{Re} Z_S}} a - \frac{1}{1\sqrt{\operatorname{Re} Z_S}} b \tag{1.36}$$

where

$$a = \frac{V + Z_S I}{2\sqrt{\operatorname{Re} Z_S}} \qquad b = \frac{V - Z_S^* I}{2\sqrt{\operatorname{Re} Z_S}} \tag{1.37}$$

Source impedance Z_S is often purely active. Therefore, it is often used as normalized impedance. In microwave design technique, the characteristic impedance of used two-port networks, including transmission lines and connectors, is adopted as an active impedance equal to 50 Ω. This is very important for measuring S-parameters when all transmission lines, source, and load should have the same active impedance. When $Z_S = Z_S^* = Z_0$, where Z_0 is the characteristic impedance, the ratio of the normalized reflected wave and the normalized incident wave for a one-port network is called the reflection coefficient Γ defined by

$$\Gamma = \frac{b}{a} = \frac{V - Z_S^* I}{V + Z_S I} = \frac{V - Z_S I}{V + Z_S I} = \frac{Z - Z_S}{Z + Z_S} \tag{1.38}$$

where $Z = V/I$.

For a two-port network, shown in Fig. 1.4, the normalized reflected waves b_1 and b_2 can also be represented by the normalized incident waves a_1 and a_2 as

$$b_1 = S_{11} a_1 + S_{12} a_2 \tag{1.39}$$

$$b_2 = S_{21} a_1 + S_{22} a_2 \tag{1.40}$$

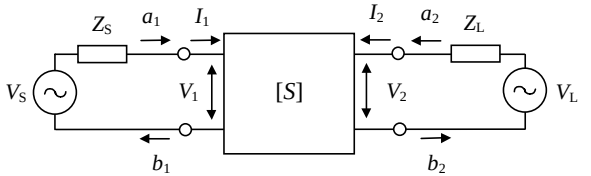


Figure 1.4 Basic diagram of S-parameter two-port network.

or in matrix form

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{21} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{1.41}$$

where the incident waves a_1 and a_2 and the reflected waves b_1 and b_2 for complex source and load impedances Z_S and Z_L are given by

$$a_1 = \frac{V_1 + Z_S I_1}{2\sqrt{\text{Re}Z_S}} \qquad a_2 = \frac{V_2 + Z_L I_2}{2\sqrt{\text{Re}Z_L}} \tag{1.42}$$

$$b_1 = \frac{V_1 - Z_S^* I_1}{2\sqrt{\text{Re}Z_S}} \qquad b_2 = \frac{V_2 - Z_L^* I_2}{2\sqrt{\text{Re}Z_L}} \tag{1.43}$$

S_{11}, S_{12}, $S_{21,}$and S_{22} are the S-parameters of the two-port network.

From Eq. (1.41) it follows that if $a_2 = 0$, then

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{1.44}$$

where S_{11} is the reflection coefficient and S_{21} is the transmission coefficient for ideal matching condition at the output terminal when there is no incident power reflected from the load. Similarly,

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{1.45}$$

where S_{12} is the transmission coefficient and S_{22} is the reflection coefficient for ideal matching condition at the input terminal.

Conversions between Two-Port Parameters

The parameters describing the same two-port network through different two-port matrices (impedance, admittance, hybrid, or transmission) can be cross-converted: the elements of each matrix can be expressed by the elements of other matrices. For example, Eqs. (1.11) and (1.12) for the Y-parameters can be easily solved for independent input voltage

source V_1 and input current I_1 as

$$V_1 = -\frac{Y_{22}}{Y_{21}}V_2 - \frac{1}{Y_{21}}I_2 \tag{1.46}$$

$$I_1 = -\frac{Y_{11}Y_{22} - Y_{12}Y_{21}}{Y_{21}}V_2 - \frac{Y_{11}}{Y_{21}}I_2 \tag{1.47}$$

Comparing the equivalent Eqs. (1.21) and (1.22) and (1.46) and (1.47) gives the following relationship between the transmission *ABCD*-parameters and admittance *Y*-parameters:

$$A = -\frac{Y_{22}}{Y_{21}} \qquad B = -\frac{1}{Y_{21}} \tag{1.48}$$

$$C = -\frac{\Delta Y}{Y_{21}} \qquad D = -\frac{Y_{11}}{Y_{21}} \tag{1.49}$$

where $\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21}$.

A summary of the relationships between impedance *Z*-parameters, admittance *Y*-parameters, hybrid *H*-parameters, and transmission *ABCD*-parameters is shown in Table 1.1 where $\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}$, $\Delta H = h_{11}h_{22} - h_{12}h_{21}$.

To convert *S*-parameters to the admittance *Y*-parameters, it is convenient to represent Eqs. (1.42) and (1.43) as follows:

$$I_1 = (a_1 - b_1)\frac{1}{\sqrt{Z_0}} \qquad I_2 = (a_2 - b_2)\frac{1}{\sqrt{Z_0}} \tag{1.50}$$

$$V_1 = (a_1 + b_1)\sqrt{Z_0} \qquad V_2 = (a_2 + b_2)\sqrt{Z_0} \tag{1.51}$$

where it is assumed that the source and load impedances are purely active and equal to $Z_S = Z_L = Z_0$.

Applying Eqs. (1.50) and (1.51) to Eqs. (1.11) and (1.12) yields

$$\frac{a_1 - b_1}{\sqrt{Z_0}} = Y_{11}(a_1 + b_1)\sqrt{Z_0} + Y_{12}(a_2 + b_2)\sqrt{Z_0} \tag{1.52}$$

$$\frac{a_2 - b_2}{\sqrt{Z_0}} = Y_{21}(a_1 + b_1)\sqrt{Z_0} + Y_{22}(a_2 + b_2)\sqrt{Z_0} \tag{1.53}$$

Accordingly, Eqs. (1.52) and (1.53) can be converted:

$$-b_1(1 + Y_{11}Z_0) - b_2Y_{12}Z_0 = -a_1(1 - Y_{11}Z_0) + a_2Y_{12}Z_0 \tag{1.54}$$

$$-b_1Y_{21}Z_0 - b_2(1 + Y_{22}Z_0) = a_1Y_{21}Z_0 - a_2(1 - Y_{22}Z_0) \tag{1.55}$$

TABLE 1.1 Relationships between *Z*-, *Y*-, *H*-, and *ABCD*-Parameters

	$[Z]$	$[Y]$	$[H]$	$[ABCD]$
$[Z]$	$\begin{matrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{matrix}$	$\begin{matrix} \frac{Y_{22}}{\Delta Y} & -\frac{Y_{12}}{\Delta Y} \\ -\frac{Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{matrix}$	$\begin{matrix} \frac{\Delta H}{h_{22}} & \frac{h_{12}}{h_{22}} \\ -\frac{h_{21}}{h_{22}} & \frac{1}{h_{22}} \end{matrix}$	$\begin{matrix} \frac{A}{C} & \frac{AD-BC}{C} \\ \frac{1}{C} & \frac{D}{C} \end{matrix}$
$[Y]$	$\begin{matrix} \frac{Z_{22}}{\Delta Z} & -\frac{Z_{12}}{\Delta Z} \\ -\frac{Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{matrix}$	$\begin{matrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{matrix}$	$\begin{matrix} \frac{1}{h_{11}} & -\frac{h_{12}}{h_{11}} \\ \frac{h_{21}}{h_{11}} & \frac{\Delta H}{h_{11}} \end{matrix}$	$\begin{matrix} \frac{D}{B} & -\frac{AD-BC}{B} \\ -\frac{1}{B} & \frac{A}{B} \end{matrix}$
$[H]$	$\begin{matrix} \frac{\Delta Z}{Z_{22}} & \frac{Z_{12}}{Z_{22}} \\ -\frac{Z_{21}}{Z_{22}} & \frac{1}{Z_{22}} \end{matrix}$	$\begin{matrix} \frac{1}{Y_{11}} & -\frac{Y_{12}}{Y_{11}} \\ \frac{Y_{21}}{Y_{11}} & \frac{\Delta Y}{Y_{11}} \end{matrix}$	$\begin{matrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{matrix}$	$\begin{matrix} \frac{B}{D} & \frac{AD-BC}{D} \\ -\frac{1}{D} & \frac{C}{D} \end{matrix}$
$[ABCD]$	$\begin{matrix} \frac{Z_{11}}{Z_{21}} & \frac{\Delta Z}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{matrix}$	$\begin{matrix} -\frac{Y_{22}}{Y_{21}} & -\frac{1}{Y_{21}} \\ -\frac{\Delta Y}{Y_{21}} & -\frac{Y_{11}}{Y_{21}} \end{matrix}$	$\begin{matrix} -\frac{\Delta H}{h_{21}} & -\frac{h_{11}}{h_{21}} \\ -\frac{h_{22}}{h_{21}} & -\frac{1}{h_{21}} \end{matrix}$	$\begin{matrix} A & B \\ C & D \end{matrix}$

Equations (1.54) and (1.55) can be easily solved for the reflected waves b_1 and b_2:

$$b_1\left[(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2\right]$$
$$=a_1\left[(1-Y_{11}Z_0)(1+Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2\right]-2a_2Y_{12}Z_0 \qquad (1.56)$$
$$b_2\left[(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2\right]$$
$$=-2a_1Y_{21}Z_0+a_2\left[(1+Y_{11}Z_0)(1-Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2\right] \qquad (1.57)$$

Comparing equivalent Eqs. (1.39) and (1.40) and (1.56) and (1.57) gives the following relationship between the scattering S-parameters and admittance Y-parameters:

$$S_{11}=\frac{(1-Y_{11}Z_0)(1+Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \qquad (1.58)$$

$$S_{12}=\frac{-2Y_{12}Z_0}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \qquad (1.59)$$

$$S_{21}=\frac{-2Y_{21}Z_0}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \qquad (1.60)$$

$$S_{22}=\frac{(1+Y_{11}Z_0)(1-Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \qquad (1.61)$$

The relationships of S-parameters with Z-, H-, and $ABCD$ parameters can be obtained in a similar fashion. Table 1.2 shows the conversions between S-parameters and Z-, Y-, H-, and $ABCD$-parameters for the simplified case when the source impedance Z_S and the load impedance Z_L are equal to the characteristic impedance Z_0 [5].

TABLE 1.2 Conversions between *S*-Parameters and *Z*-, *Y*-, *H*-, and *ABCD*-Parameters

S-parameters through Z-, Y-, H-, and $ABCD$-parameters	Z-, Y-, H-, $ABCD$-parameters through S-parameters
$S_{11} = \dfrac{(Z_{11} - Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}}$	$Z_{11} = Z_0 \dfrac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$
$S_{12} = \dfrac{2Z_{12}Z_0}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}}$	$Z_{12} = Z_0 \dfrac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$
$S_{21} = \dfrac{2Z_{21}Z_0}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}}$	$Z_{21} = Z_0 \dfrac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$
$S_{22} = \dfrac{(Z_{11} + Z_0)(Z_{22} - Z_0) - Z_{12}Z_{21}}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}}$	$Z_{22} = Z_0 \dfrac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}$
$S_{11} = \dfrac{(1 - Y_{11}Z_0)(1 + Y_{22}Z_0) + Y_{12}Y_{21}Z_0^2}{(1 + Y_{11}Z_0)(1 + Y_{22}Z_0) - Y_{12}Y_{21}Z_0^2}$	$Y_{11} = \dfrac{1}{Z_0} \dfrac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$
$S_{12} = \dfrac{-2Y_{12}Z_0}{(1 + Y_{11}Z_0)(1 + Y_{22}Z_0) - Y_{12}Y_{21}Z_0^2}$	$Y_{12} = \dfrac{1}{Z_0} \dfrac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$
$S_{21} = \dfrac{-2Y_{21}Z_0}{(1 + Y_{11}Z_0)(1 + Y_{22}Z_0) - Y_{12}Y_{21}Z_0^2}$	$Y_{21} = \dfrac{1}{Z_0} \dfrac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$
$S_{22} = \dfrac{(1 + Y_{11}Z_0)(1 - Y_{22}Z_0) + Y_{12}Y_{21}Z_0^2}{(1 + Y_{11}Z_0)(1 + Y_{22}Z_0) - Y_{12}Y_{21}Z_0^2}$	$Y_{22} = \dfrac{1}{Z_0} \dfrac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$
$S_{11} = \dfrac{(h_{11} - Z_0)(1 + h_{22}Z_0) - h_{12}h_{21}Z_0}{(h_{11} + Z_0)(1 + h_{22}Z_0) - h_{12}h_{21}Z_0}$	$h_{11} = Z_0 \dfrac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$
$S_{12} = \dfrac{2h_{12}Z_0}{(h_{11} + Z_0)(1 + h_{22}Z_0) - h_{12}h_{21}Z_0}$	$h_{12} = \dfrac{2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$
$S_{21} = \dfrac{-2h_{21}Z_0}{(h_{11} + Z_0)(1 + h_{22}Z_0) - h_{12}h_{21}Z_0}$	$h_{21} = \dfrac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$
$S_{22} = \dfrac{(h_{11} + Z_0)(1 - h_{22}Z_0) + h_{12}h_{21}Z_0}{(h_{11} + Z_0)(1 + h_{22}Z_0) - h_{12}h_{21}Z_0}$	$h_{22} = \dfrac{1}{Z_0} \dfrac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$
$S_{11} = \dfrac{AZ_0 + B - CZ_0^2 - DZ_0}{AZ_0 + B + CZ_0^2 + DZ_0}$	$A = \dfrac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}}$
$S_{12} = \dfrac{2(AD - BC)Z_0}{AZ_0 + B + CZ_0^2 + DZ_0}$	$B = Z_0 \dfrac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{2S_{21}}$
$S_{21} = \dfrac{2Z_0}{AZ_0 + B + CZ_0^2 + DZ_0}$	$C = \dfrac{1}{Z_0} \dfrac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{2S_{21}}$
$S_{22} = \dfrac{-AZ_0 + B - CZ_0^2 + DZ_0}{AZ_0 + B + CZ_0^2 + DZ_0}$	$D = \dfrac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}}$

Interconnection of Two-Port Networks

When analyzing the behavior of an electrical circuit, it is often necessary to define the parameters of a combination of two or more internal two-port networks. For example, the feedback amplifier circuit consists of an active two-port network representing the amplifier stage, which is connected in parallel with a passive feedback two-port network. Commonly, two-port networks can be interconnected using parallel, series, series-parallel, or cascade connections.

To characterize the resulting two-port networks, it is necessary to take into account which currents and voltages are common for individual two-port networks. The most convenient set of parameters is one for which the common currents and voltages represent a simple linear combination of the independent variables. For the interconnection shown in Fig. 1.5(a), two-port networks Z_a and Z_b are connected in series for both the input and the output terminals. Therefore, the currents flowing through these terminals are equal when

$$I_1 = I_{1a} = I_{1b} \qquad I_2 = I_{2a} = I_{2b} \tag{1.62}$$

or in matrix form

$$[I] = [I_a] = [I_b] \tag{1.63}$$

The terminal voltages of the resulting two-port network are the appropriate sums of the terminal voltages of the individual two-port networks when

$$V_1 = V_{1a} + V_{1b} \qquad V_2 = V_{2a} + V_{2b} \tag{1.64}$$

or in matrix form

$$[V] = [V_a] + [V_b] \tag{1.65}$$

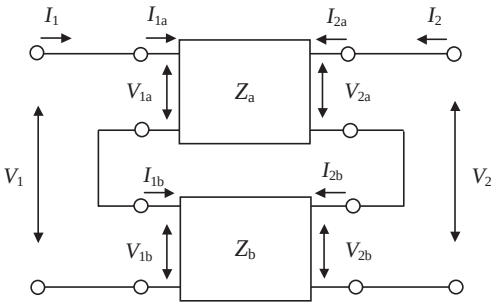
The currents are common components for both the resulting and the individual two-port networks. To describe the properties of such a circuit, it is best to use the impedance matrices. For each two-port network Z_a and Z_b, we can write, using Eq. (1.62)

$$[V_a] = [Z_a][I_a] = [Z_a][I] \tag{1.66}$$

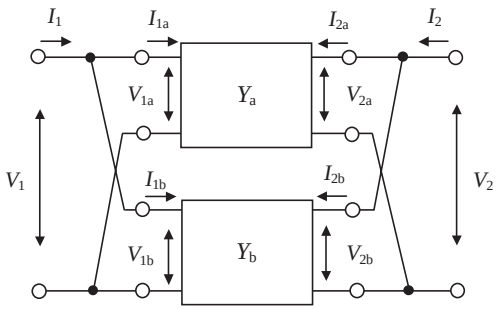
$$[V_b] = [Z_b][I_b] = [Z_b][I] \tag{1.67}$$

Adding both sides of Eqs. (1.66) and (1.67) yields

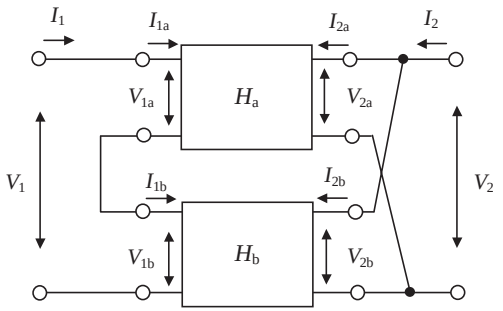
$$[V] = [Z][I] \tag{1.68}$$



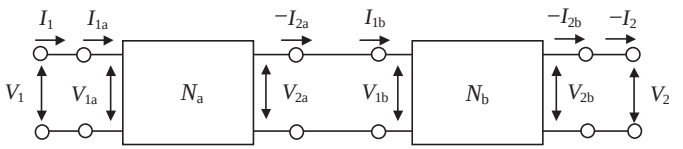
(a)



(b)



(c)



(d)

Figure 1.5 Different interconnections of two-port networks.

where

$$[Z] = [Z_a] + [Z_b] = \begin{bmatrix} Z_{11a} + Z_{11b} & Z_{12a} + Z_{12b} \\ Z_{21a} + Z_{21b} & Z_{22a} + Z_{22b} \end{bmatrix}$$

The circuit shown in Fig. 1.5(*b*) is composed of the two-port networks Y_a and Y_b connected in parallel, where the common components for both the resulting and individual two-port networks are input and output voltages:

$$V_1 = V_{1a} = V_{1b} \qquad V_2 = V_{2a} = V_{2b} \tag{1.69}$$

or in matrix form

$$[V] = [V_a] = [V_b] \tag{1.70}$$

Consequently, to describe the circuit properties, it is convenient to use the admittance matrices that give the resulting matrix equation in the form of

$$[I] = [Y][V] \tag{1.71}$$

where

$$[Y] = [Y_a] + [Y_b] = \begin{bmatrix} Y_{11a} + Y_{11b} & Y_{12a} + Y_{12b} \\ Y_{21a} + Y_{21b} & Y_{22a} + Y_{22b} \end{bmatrix}$$

The series connection of the input terminals and parallel connection of the output terminals is characterized by the circuit in Fig. 1.5(*c*), which shows a series-parallel connection of two-port networks. The common components for this circuit are the input currents and the output voltages. As a result, it is most convenient to analyze the circuit properties using hybrid matrices. The resulting two-port hybrid matrix is equal to the sum of two individual hybrid matrices.

$$[H] = [H_a] + [H_b] = \begin{bmatrix} h_{11a} + h_{11b} & h_{12a} + h_{12b} \\ h_{21a} + h_{21b} & h_{22a} + h_{22b} \end{bmatrix} \tag{1.72}$$

In Fig. 1.5(*d*), the cascade connection of two individual two-port networks is presented. For such an approach using the one-by-one interconnection of two-port networks, the output voltage and the output current of the first network are equal to the input voltage and the input current of the second one, respectively, i.e.,

$$V_1 = V_{1a} \qquad I_1 = I_{1a} \tag{1.73}$$

$$V_{2a} = V_{1b} \qquad -I_{2a} = I_{1b} \tag{1.74}$$

$$V_{2b} = V_2 \qquad -I_{2b} = -I_2 \tag{1.75}$$

In this case, it is convenient to use a system of *ABCD*-parameters given by Eqs. (1.21) and (1.22). As a result, for the first individual two port network shown in Fig. 1.5(*d*)

$$\begin{bmatrix} V_{1a} \\ I_{1a} \end{bmatrix} = \begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} \begin{bmatrix} V_{2a} \\ -I_{2a} \end{bmatrix} \tag{1.76}$$

or using Eqs. (1.73) and (1.74)

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} \begin{bmatrix} V_{1b} \\ I_{1b} \end{bmatrix} \tag{1.77}$$

Similarly, for the second individual two-port network

$$\begin{bmatrix} V_{1b} \\ I_{1b} \end{bmatrix} = \begin{bmatrix} A_b & B_b \\ C_b & D_b \end{bmatrix} \begin{bmatrix} V_{2b} \\ -I_{2b} \end{bmatrix} = \begin{bmatrix} A_b & B_b \\ C_b & D_b \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{1.78}$$

Then, substituting matrix Eq. (1.78) to matrix Eq. (1.77) yields

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} \begin{bmatrix} A_b & B_b \\ C_b & D_b \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{1.79}$$

Consequently, the transmission matrix of the resulting two-port network obtained by the cascade connection of two or more individual two-port networks is determined by multiplying the transmission matrices of the individual networks. This important property is widely used in the analysis and design of transmission networks and systems.

Practical Two-Port Circuits

Single-element networks

The simplest networks, which include only one element, can be constructed by (*a*) a series connected admittance *Y*, or (*b*) a parallel connected impedance *Z*, as shown in Fig. 1.6.

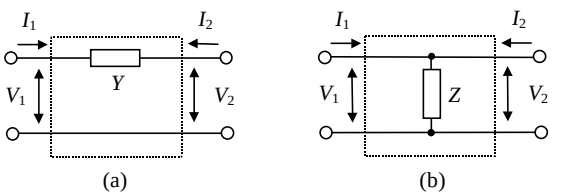


Figure 1.6 Single-element networks.

The two-port network consisting of a series admittance Y in a system of Y-parameters can be described as follows:

$$I_1 = Y V_1 - Y V_2 \tag{1.80}$$

$$I_2 = -Y V_1 + Y V_2 \tag{1.81}$$

or in matrix form

$$[Y] = \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix} \tag{1.82}$$

which means that $Y_{11} = Y_{22} = Y$ and $Y_{12} = Y_{21} = -Y$. The resulting matrix is a singular matrix with $|Y| = 0$. Consequently, it is impossible to determine such a two-port network with the series admittance Y-parameters through a system of Z-parameters. However, using H- and $ABCD$-parameters, it can be described respectively by

$$[H] = \begin{bmatrix} 1/Y & 1 \\ -1 & 0 \end{bmatrix} \qquad [ABCD] = \begin{bmatrix} 1 & 1/Y \\ 0 & 1 \end{bmatrix} \tag{1.83}$$

Similarly, for a two-port network with a parallel impedance Z

$$[Z] = \begin{bmatrix} Z & Z \\ Z & Z \end{bmatrix} \tag{1.84}$$

which means that $Z_{11} = Z_{12} = Z_{21} = Z_{22} = Z$. The resulting matrix is a singular matrix with $|Z| = 0$. In this case, the determination of such a two-port network with the parallel impedance Z-parameters through a system of Y-parameters is impossible. Using H- and $ABCD$-parameters, the two-port network can be described by

$$[H] = \begin{bmatrix} 0 & 1 \\ -1 & Y \end{bmatrix} \qquad [ABCD] = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \tag{1.85}$$

π-and *T*-networks

Figure 1.7 shows a two-port network in the form of (a) π-circuit and (b) T-circuit. The π-circuit includes the current source $g_m V_1$ and the T-circuit includes the voltage source $r_m I_1$.

By writing the two loop equations using Kirchhoff's current law or applying Eqs. (1.13) and (1.14) for the π-circuit, we obtain

$$I_1 - (Y_1 + Y_3)V_1 + Y_3 V_2 = 0 \tag{1.86}$$

$$I_2 + (g_m - Y_3)V_1 + (Y_2 + Y_3)V_2 = 0 \tag{1.87}$$

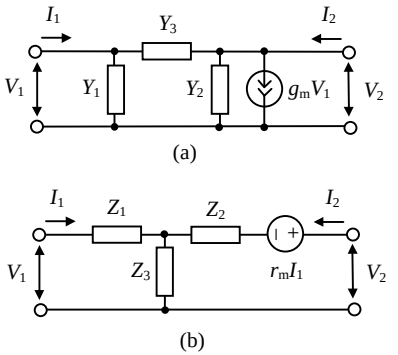


Figure 1.7 Basic diagrams of π - and T-networks.

Equations (1.86) and (1.87) are written as matrix Eq. (1.3) with

$$[M] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad \text{and} \quad [N] = \begin{bmatrix} -(Y_1 + Y_3) & Y_3 \\ -g_\text{m} + Y_3 & -(Y_2 + Y_3) \end{bmatrix}$$

Since matrix $[M]$ is nonsingular, such a two-port network can be described by a system of Y-parameters:

$$[Y] = -[M]^{-1}[N] = \begin{bmatrix} Y_1 + Y_3 & -Y_3 \\ g_\text{m} - Y_3 & Y_2 + Y_3 \end{bmatrix} \tag{1.88}$$

Similarly, for a two-port network in the form of a T-circuit using Kirchhoff's voltage law or applying Eqs. (1.8) and (1.9), we obtain

$$[Z] = -[M]^{-1}[N] = \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ r_\text{m} + Z_3 & Z_2 + Z_3 \end{bmatrix} \tag{1.89}$$

If $g_\text{m} = 0$ for a π-circuit and $r_\text{m} = 0$ for a T-circuit, their appropriate matrices in a system of $ABCD$-parameters can be written as follows:

for π-circuit

$$[ABCD] = \begin{bmatrix} 1 + \dfrac{Y_2}{Y_3} & \dfrac{1}{Y_3} \\ Y_1 + Y_2 + \dfrac{Y_1 Y_2}{Y_3} & 1 + \dfrac{Y_1}{Y_3} \end{bmatrix} \tag{1.90}$$

for T-circuit

$$[ABCD] = \begin{bmatrix} 1 + \dfrac{Z_2}{Z_3} & Z_1 + Z_2 + \dfrac{Z_1 Z_2}{Z_3} \\ \dfrac{1}{Z_3} & 1 + \dfrac{Z_1}{Z_3} \end{bmatrix} \tag{1.91}$$

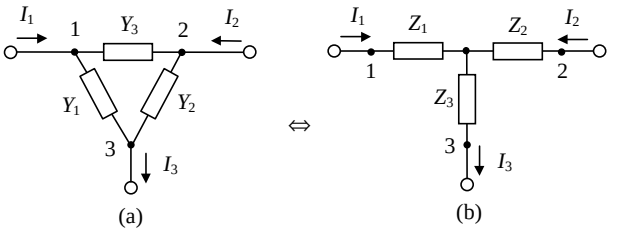


Figure 1.8 Equivalence of π- and T-circuits.

For the appropriate relationships between impedances of T-circuit and admittances of π-circuit, these two circuits become equivalent with respect to their effect on any other two-port network. For π-circuit shown in Fig. 1.8(a), we can write

$$I_1 = Y_1 V_{13} + Y_3 V_{12} = Y_1 V_{13} + Y_3 (V_{13} - V_{23}) = (Y_1 + Y_3) V_{13} - Y_3 V_{23} \tag{1.92}$$

$$I_2 = Y_2 V_{23} - Y_3 V_{12} = Y_2 V_{23} - Y_3 (V_{13} - V_{23}) = -Y_3 V_{13} + (Y_2 + Y_3) V_{23} \tag{1.93}$$

Solving Eqs. (1.92) and (1.93) for voltages V_{13} and V_{23} yields

$$V_{13} = \frac{Y_2 + Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_1 + \frac{Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_2 \tag{1.94}$$

$$V_{23} = \frac{Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_1 + \frac{Y_1 + Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_2 \tag{1.95}$$

Similarly, for T-circuit shown in Fig. 1.8(b)

$$V_{13} = Z_1 I_1 + Z_3 I_3 = Z_1 I_1 + Z_3 (I_1 + I_2) = (Z_1 + Z_3) I_1 + Z_3 I_2 \tag{1.96}$$

$$V_{23} = Z_2 I_2 + Z_3 I_3 = Z_2 I_2 + Z_3 (I_1 + I_2) = Z_3 I_1 + (Z_2 + Z_3) I_2 \tag{1.97}$$

The equations for currents I_1 and I_2 can be obtained by

$$I_1 = \frac{Z_2 + Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{13} - \frac{Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{23} \tag{1.98}$$

$$I_2 = -\frac{Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{13} + \frac{Z_1 + Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{23} \tag{1.99}$$

To establish a T- to π-transformation, it is necessary to equate the coefficients for V_{13} and V_{23} in Eqs. (1.98) and (1.99) to the corresponding coefficients in Eqs. (1.92) and (1.93). Similarly, to establish a π- to T-transformation, it is necessary to equate the coefficients for I_1 and I_2 in Eqs. (1.96) and (1.97) to the corresponding coefficients in Eqs. (1.94)

TABLE 1.3 Relationships between π- and T-Circuit Parameters

T- to π-transformation	π-to T- transformation
$Y_1 = \dfrac{Z_2}{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}$	$Z_1 = \dfrac{Y_2}{Y_1Y_2 + Y_2Y_3 + Y_1Y_3}$
$Y_2 = \dfrac{Z_1}{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}$	$Z_2 = \dfrac{Y_1}{Y_1Y_2 + Y_2Y_3 + Y_1Y_3}$
$Y_3 = \dfrac{Z_3}{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}$	$Z_3 = \dfrac{Y_3}{Y_1Y_2 + Y_2Y_3 + Y_1Y_3}$

and (1.95). The resulting relationships between admittances for a π circuit and impedances for a T-circuit are presented in Table 1.3.

Three-Port Network with Common Terminal

The concept of two-port network with two independent sources can be extended to multiport networks, in particular for a three-port network (see Fig. 1.9) when all three independent sources are connected to a common point. The three-port network matrix Eq. (1.3) in scalar form is as follows:

$$\left.\begin{aligned} m_{11}V_1 + m_{12}V_2 + m_{13}V_3 + n_{11}I_1 + n_{12}I_2 + n_{13}I_3 = 0 \\ m_{21}V_1 + m_{22}V_2 + m_{23}V_3 + n_{21}I_1 + n_{22}I_2 + n_{23}I_3 = 0 \\ m_{31}V_1 + m_{32}V_2 + m_{33}V_3 + n_{31}I_1 + n_{32}I_2 + n_{33}I_3 = 0 \end{aligned}\right\} \qquad (1.100)$$

Likewise, if matrix $[N]$ in Eq. (1.100) is nonsingular when $|N| \neq 0$, similarly to a two-port network, then this system of three equations in admittance matrix representation can be rewritten in terms of voltage

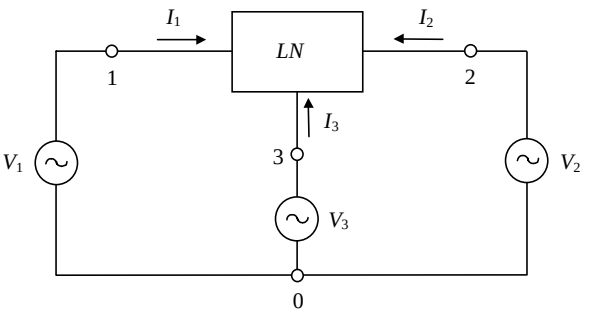


Figure 1.9 Basic diagram of three-port network with common terminal.

matrix $[V]$ as

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{1.101}$$

The matrix $[Y]$ in Eq. (1.101) is the indefinite admittance matrix of the three-port circuit and is a singular matrix with the following important properties:

The sum of all terminal currents entering the circuit is equal to zero, that is, $I_1 + I_2 + I_3 = 0$.

All terminal currents entering the circuit depend on the voltages between circuit terminals, which makes the sum of all terminal voltages equal to zero, that is, $V_{13} + V_{32} + V_{21} = 0$.

According to the first property, adding the left and right parts of matrix Eq. (1.101) leads to

$$(Y_{11} + Y_{21} + Y_{31})V_1 + (Y_{12} + Y_{22} + Y_{32})V_2 + (Y_{13} + Y_{23} + Y_{33})V_3 = 0 \tag{1.102}$$

Since all terminal voltages (V_1, V_2 or V_3) can be set independently, Eq. (1.102) can be satisfied only if any column sum is zero:

$$\left.\begin{aligned} Y_{11} + Y_{21} + Y_{31} &= 0 \\ Y_{12} + Y_{22} + Y_{32} &= 0 \\ Y_{13} + Y_{23} + Y_{33} &= 0 \end{aligned}\right\} \tag{1.103}$$

Terminal current will neither decrease nor increase with the simultaneous change of all terminal voltages by the same magnitude. Consequently, if all terminal voltages are equal to a nonzero value $V_1 = V_2 = V_3 = V_0$, a lack of the terminal currents occurs when $I_1 = I_2 = I_3 = 0$. For example, for the first row of the matrix Eq. (1.101), $I_1 = Y_{11}V_1 + Y_{12}V_2 + Y_{13}V_3$, we can write

$$0 = (Y_{11} + Y_{12} + Y_{13})V_0 \tag{1.104}$$

Due to the nonzero value V_0 from Eq. (1.104), it follows that

$$Y_{11} + Y_{12} + Y_{13} = 0 \tag{1.105}$$

Applying the same approach to the other two rows results in

$$\left.\begin{aligned} Y_{11} + Y_{12} + Y_{13} &= 0 \\ Y_{21} + Y_{22} + Y_{23} &= 0 \\ Y_{31} + Y_{32} + Y_{33} &= 0 \end{aligned}\right\} \tag{1.106}$$

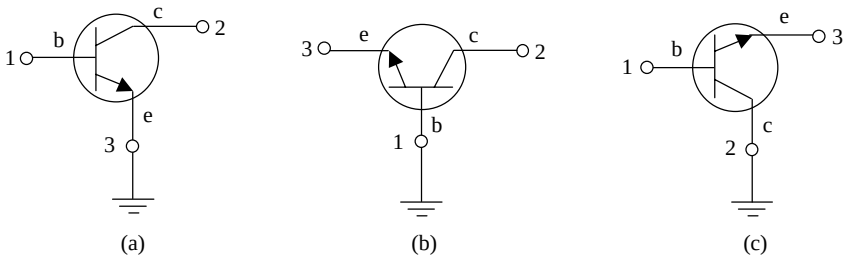


Figure 1.10 Bipolar transistors with different common terminals.

Consequently, by using Eqs. (1.103) through (1.106), the indefinite admittance Y-matrix of three-port network can be rewritten as

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} & -(Y_{11}+Y_{12}) \\ Y_{21} & Y_{22} & -(Y_{21}+Y_{22}) \\ -(Y_{11}+Y_{21}) & -(Y_{12}+Y_{22}) & Y_{11}+Y_{12}+Y_{21}+Y_{22} \end{bmatrix} \quad (1.107)$$

By choosing successively terminal 1, 2, and 3 as the datum terminal, we can obtain the appropriate three definite two-port admittance matrices of the initial three-port network. Consider finding these two port matrices as the admittance matrices of (a) the common-emitter, (b) the common-base, and (c) the common-collector circuit connection of the bipolar transistor, as shown in Fig. 1.10. If the common-emitter device is treated as a two-port circuit characterized by four Y-parameters, (Y_{11}, Y_{12}, Y_{21}, and Y_{22}) the two-port matrix of the common-collector circuit with grounded collector terminal is simply obtained by deleting the second row and the second column in matrix Eq. (1.107). For the common-base circuit with grounded base terminal, the first row and the first column should be deleted because the emitter terminal is considered the input terminal.

A similar approach can be applied to the indefinite three-port impedance network. This allows the determination of the Z-parameters of the impedance matrices of the common-base and the common-collector circuit from the known impedance Z-parameters of the common-emitter circuit. Parameters of the three-port network with the different common terminals for bipolar and field-effect devices are given in Table 1.4.

Transmission Line

Transmission lines are widely used in matching circuits in power amplifiers, in resonant and feedback circuits in the oscillators, filters, directional couplers, power combiners, and dividers. When the propagated signal wavelength is compared to its physical dimension, the transmission line can be considered as a distributed-parameter two-port

TABLE 1.4 Active Device *Y*- and *Z*-Parameters with Different Common Terminal

	Y-parameters	*Z*-parameters
Common emitter (source)	$\begin{matrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{matrix}$	$\begin{matrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{matrix}$
Common base (gate)	$\begin{matrix} Y_{11}+Y_{12}+Y_{21}+Y_{22} & -(Y_{12}+Y_{22}) \\ -(Y_{21}+Y_{22}) & Y_{22} \end{matrix}$	$\begin{matrix} Z_{11}+Z_{12}+Z_{21}+Z_{22} & -(Z_{12}+Z_{22}) \\ -(Z_{21}+Z_{22}) & Z_{22} \end{matrix}$
Common collector (drain)	$\begin{matrix} Y_{11} & -(Y_{11}+Y_{12}) \\ -(Y_{11}+Y_{21}) & Y_{11}+Y_{12}+Y_{21}+Y_{22} \end{matrix}$	$\begin{matrix} Z_{11} & -(Z_{11}+Z_{12}) \\ -(Z_{11}+Z_{21}) & Z_{11}+Z_{12}+Z_{21}+Z_{22} \end{matrix}$

network, where the voltages and currents vary in magnitude and phase over length.

Schematically, a transmission line is often represented as a two-wire line, as shown in Fig. 1.11(*a*). Its electrical parameters are distributed along its length. The physical properties of a transmission line are determined by four basic parameters:

- The series inductance L due to the self-inductive phenomena of two conductors
- The shunt capacitance C in view of the close proximity between two conductors
- The series resistance R due to the finite conductivity of the conductors
- The shunt conductance G in view of dielectric losses in the material.

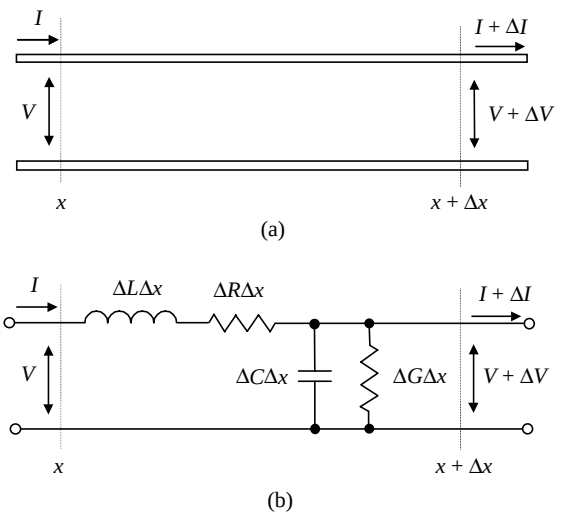


Figure 1.11 Transmission line schematic.

As a result, a transmission line of length Δx represents a lumped element circuit shown in Fig. 1.11(b), where ΔL, ΔC, ΔR, and ΔG are the series inductance, the shunt capacitance, the series resistance, and the shunt conductance per unit length, respectively. If all these elements are distributed uniformly along a transmission line, and their values do not depend on the chosen position of Δx, this transmission line is called a *uniform transmission line*. Any finite length of the uniform transmission line can be viewed as a cascade of section length Δx.

To define the distribution of the voltages and currents along the uniform transmission line, it is necessary to write the differential equations using Kirchhoff's voltage law for instantaneous values of the voltages and currents in the line section of length Δx distant x from its beginning. For the sinusoidal steady-state condition, the telegrapher equations for $V(x)$ and $I(x)$ are given by

$$\frac{\mathrm{d}^2V(x)}{\mathrm{d}x^2} - \gamma^2 V(x) = 0 \tag{1.108}$$

$$\frac{\mathrm{d}^2I(x)}{\mathrm{d}x^2} - \gamma^2 I(x) = 0 \tag{1.109}$$

where $\gamma = \alpha + j\beta = \sqrt{(\Delta R + j\omega\Delta L)(\Delta G + j\omega\Delta C)}$ is the complex propagation constant (which is a function of frequency), α is the attenuation constant, and β is the phase constant. The general solutions of Eqs. (1.108) and (1.109) for voltage and current of the traveling wave in the transmission line can be written as

$$V(x) = A_1 \exp(-\gamma x) + A_2 \exp(\gamma x) \tag{1.110}$$

$$I(x) = \frac{A_1}{Z_0} \exp(-\gamma x) - \frac{A_2}{Z_0} \exp(\gamma x) \tag{1.111}$$

where $Z_0 = \sqrt{(\Delta R + j\omega\Delta L)/(\Delta G + j\omega\Delta C)}$ is the characteristic impedance of the transmission line, $V_\mathrm{i}(x) = A_1 \exp(-\gamma x)$ and $V_\mathrm{r}(x) = A_2 \exp(\gamma x)$ represent the incident voltage and the reflected voltage, respectively, and $I_\mathrm{i}(x) = A_1 \exp(-\gamma x)/Z_0$ and $I_\mathrm{r}(x) = A_2 \exp(\gamma x)/Z_0$ are the incident current and the reflected current, respectively.

From Eqs. (1.110) and (1.111) it follows that the characteristic impedance of the transmission line Z_0 represents the ratio of the incident (reflected) voltage to the incident (reflected) current at any position on the line as

$$Z_0 = \frac{V_\mathrm{i}(x)}{I_\mathrm{i}(x)} = \frac{V_\mathrm{r}(x)}{I_\mathrm{r}(x)} \tag{1.112}$$

For a lossless transmission line, when $R = G = 0$ and the voltage and current do not change with position, the attenuation constant $\alpha = 0$, the propagation constant $\gamma = j\beta = j\omega\sqrt{\Delta L \Delta C}$ and the phase constant

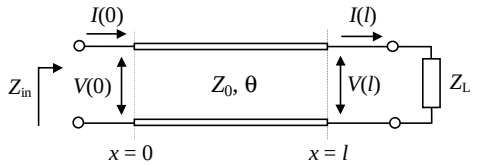


Figure 1.12 Loaded transmission line.

$\beta = \omega\sqrt{\Delta L \Delta C}$. Consequently, the characteristic impedance is reduced to $Z_0 = \sqrt{L/C}$ and represents a real number. The wavelength is defined as $\lambda = 2\pi/\beta = 2\pi/\omega\sqrt{\Delta L \Delta C}$ and the phase velocity as $v_p = \omega/\beta = 1/\sqrt{\Delta L \Delta C}$.

Figure 1.12 represents a transmission line of characteristic impedance Z_0 terminated with a load Z_L. In this case, the constants A_1 and A_2 are determined at the position $x = l$ by

$$V(l) = A_1 \exp(-\gamma l) + A_2 \exp(\gamma l) \tag{1.113}$$

$$I(l) = \frac{A_1}{Z_0} \exp(-\gamma l) - \frac{A_2}{Z_0} \exp(\gamma l) \tag{1.114}$$

equal to

$$A_1 = \frac{V(l) + Z_0 I(l)}{2} \exp(\gamma l) \tag{1.115}$$

$$A_2 = \frac{V(l) - Z_0 I(l)}{2} \exp(-\gamma l) \tag{1.116}$$

As a result, wave equations for voltage $V(x)$ and current $I(x)$ can be rewritten as

$$V(x) = \frac{V(l) + Z_0 I(l)}{2} \exp[\gamma(l - x)] + \frac{V(l) - Z_0 I(l)}{2} \exp[-\gamma(l - x)] \tag{1.117}$$

$$I(x) = \frac{V(l) + Z_0 I(l)}{2Z_0} \exp[\gamma(l - x)] - \frac{V(l) - Z_0 I(l)}{2Z_0} \exp[-\gamma(l - x)] \tag{1.118}$$

which allows their determination at any position on the transmission line.

The voltage and current amplitudes at $x = 0$, $V(0)$ and $I(0)$, as functions of the voltage and current amplitudes at $x = l$, $V(l)$ and $I(l)$, can be determined from Eqs. (1.117) and (1.118) as

$$V(0) = \frac{V(l) + Z_0 I(l)}{2} \exp(\gamma l) + \frac{V(l) - Z_0 I(l)}{2} \exp(-\gamma l) \tag{1.119}$$

$$I(0) = \frac{V(l) + Z_0 I(l)}{2Z_0} \exp(\gamma l) - \frac{V(l) - Z_0 I(l)}{2Z_0} \exp(-\gamma l) \tag{1.120}$$

Using the ratios $\cosh x = [\exp(x) + \exp(-x)]/2$ and $\sinh x = [\exp(x) - \exp(-x)]/2$, we can rewrite Eqs. (1.119) and (1.120) in the form of

$$V(0) = V(l)\cosh(\gamma l) + Z_0 I(l)\sinh(\gamma l) \tag{1.121}$$

$$I(0) = \frac{V(l)}{Z_0}\sinh(\gamma l) + I(l)\cosh(\gamma l) \tag{1.122}$$

which represents the transmission equations of the symmetrical reciprocal two-port network expressed through *ABCD*-parameters when $AD - BC = 1$ and $A = D$. Consequently, the transmission *ABCD*-matrix of the lossless transmission line with $\alpha = 0$ can be given by

$$[ABCD] = \begin{bmatrix} \cos\theta & jZ_0 \sin\theta \\ \frac{j\sin\theta}{Z_0} & \cos\theta \end{bmatrix} \tag{1.123}$$

Using the formulas to transform *ABCD*-parameters into *S* parameters gives

$$[S] = \begin{bmatrix} 0 & \exp(-j\theta) \\ \exp(-j\theta) & 0 \end{bmatrix} \tag{1.124}$$

where $\theta = \beta l$ is the electrical length of the transmission line.

One of the useful concepts of such a loaded lossless transmission line is the *reflection coefficient* Γ, which is defined as the ratio of the reflected voltage wave and the incident voltage wave given at x by

$$\Gamma(x) = \frac{V_\mathrm{r}}{V_\mathrm{i}} = \frac{A_2}{A_1}\exp(2j\beta x) \tag{1.125}$$

The reflection coefficient for $x = l$ (taking into account Eqs. (1.115) and (1.116)) can be defined as

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{1.126}$$

where Γ represents the load reflection coefficient and $Z = Z_\mathrm{L} = V(l)/I(l)$. If the load is mismatched, only part of the available power from source is delivered to the load. This power loss is called a *return loss*, *RL*, and is calculated in decibels as

$$RL = -20\log_{10}|\Gamma| \tag{1.127}$$

For a matched load, when $\Gamma = 0$, return loss is of ∞ dB. A total reflection with $\Gamma = 1$ means a return loss of 0 dB when all incident power is reflected.

According to the general solution for voltage at a position x in the transmission line

$$V(x) = V_{\mathrm{i}}(x) + V_{\mathrm{r}}(x) = V_{\mathrm{i}}[1 + \Gamma(x)] \tag{1.128}$$

Hence for two waves, incident and reflected, being in phase, the maximum amplitude is

$$V_{\max}(x) = |V_{\mathrm{i}}|[1 + |\Gamma(x)|] \tag{1.129}$$

and the minimum amplitude (when these two waves are out of phase) is

$$V_{\min}(x) = |V_{\mathrm{i}}|[1 - |\Gamma(x)|] \tag{1.130}$$

The ratio of $V_{\max}$ to $V_{\min}$, which is a function of the reflection coefficient Γ, is the *voltage standing wave ratio* (*VSWR*). The *VSWR* is a measure of mismatch and can be written as

$$VSWR = \frac{V_{\max}}{V_{\min}} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{1.131}$$

which can change from 1 to ∞ (where $VSWR = 1$ implies a matched load). For purely active loads when $Z_{\mathrm{L}} = R_{\mathrm{L}}$, the *VSWR* can be calculated using $VSWR = R_{\mathrm{L}}/Z_0$ when $R_{\mathrm{L}} \geq Z_0$ and $VSWR = Z_0/R_{\mathrm{L}}$ when $Z_0 \geq R_{\mathrm{L}}$.

From Eqs. (1.121) and (1.122) it follows that the input impedance of the loaded lossless transmission line can be obtained using

$$Z_{\mathrm{in}} = \frac{V(0)}{I(0)} = Z_0 \frac{Z_{\mathrm{L}} + jZ_0 \tan(\theta)}{Z_0 + jZ_{\mathrm{L}} \tan(\theta)} \tag{1.132}$$

which gives an important dependence between the input impedance, the transmission line parameters (electrical length and characteristic impedance), and the arbitrary load impedance.

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Chapter

2

Nonlinear Circuit Design Methods

This chapter presents the most commonly used design techniques for analyzing nonlinear circuits, including transistor power amplifiers. There are several approaches to analyzing and designing these nonlinear circuits, depending on their main specifications, typically, an analysis in both the time domain (to determine transient circuit behavior) and in the frequency domain (to improve power and spectral performances when parasitic effects, such as instability and spurious emission, must be eliminated or minimized). Using the time domain technique, it is relatively easy to describe a circuit with differential equations, which must be solved numerically. The time domain analysis is limited: it cannot operate with the circuit immitance parameters, and can be practically realized only for circuits with lumped parameters or ideal transmission lines. The frequency domain analysis is less ambiguous because a relatively complex circuit often can be reduced to one or more sets of immitances at each harmonic component. For example, using a quasilinear approach, the nonlinear circuit parameters averaged by fundamental components allow a linear circuit analysis to be applied. At the same time, harmonic balance analysis can be applied to nonlinear circuits and can combine both frequency and time domain analysis. Some practical equations, such as the Taylor and Fourier series expansions, Bessel functions, trigonometric identities, and the concept of the conduction angle, which simplify the circuit design procedure, are given.

Spectral Domain Analysis

Spectral domain analysis is used to define power amplifier output performance. Such an analysis allows the output current response to be

determined in view of the nonlinear device transfer characteristic approximated by

$$i(t) = f[v(t)] \tag{2.1}$$

when, in a common case, the following multiple frequency signal is applied to the device input:

$$v(t) = \sum_{k=1}^{N} V_{\mathrm{k}} \cos(\omega_{\mathrm{k}} t + \phi_{\mathrm{k}}) \tag{2.2}$$

The result of the spectral domain analysis is shown as a summation of the harmonic components, the amplitudes and phases of which will determine the output signal spectrum. This problem is solved using trigonometric identities, piecewise linear approximation, or Bessel functions.

Trigonometric identities

The use of the trigonometric identities is very convenient when the transfer characteristic of the nonlinear element can be represented by the power series

$$i = a_{\mathrm{o}} + a_1 v + a_2 v^2 + \cdots + a_{\mathrm{n}} v^{\mathrm{n}} \tag{2.3}$$

Let the input signal represent the only fundamental harmonic component in the form of

$$v = V \cos(\omega t + \phi) \tag{2.4}$$

Then, by substituting Eq. (2.4) for Eq. (2.3), the power series can be written as follows:

$$i = a_0 + a_1 V \cos(\omega t + \phi) + a_2 V^2 \cos^2(\omega t + \phi) + \cdots + a_{\mathrm{n}} V^{\mathrm{n}} \cos^{\mathrm{n}}(\omega t + \phi) \tag{2.5}$$

To represent the right part of Eq. (2.5) as a sum of first-order cosine components, the following trigonometric identities, which allow the n order cosine components to be replaced, can be used:

$$\cos^2 \psi = \frac{1}{2}(1 + \cos 2\psi) \tag{2.6}$$

$$\cos^3 \psi = \frac{1}{4}(3 \cos \psi + \cos 3\psi) \tag{2.7}$$

$$\cos^4 \psi = \frac{1}{8}(3 + 4 \cos 2\psi + \cos 4\psi) \tag{2.8}$$

$$\cos^5 \psi = \frac{1}{16}(10 \cos \psi + 5 \cos 3\psi + \cos 5\psi) \tag{2.9}$$

where $\psi = \omega t + \phi$.

Using the appropriate substitution from Eqs. (2.6) to (2.9) and equating the signal frequency component terms allows Eq. (2.5) to be rewritten as

$$i = I_0 + I_1 \cos(\omega t + \phi) + I_2 \cos 2(\omega t + \phi) + I_3 \cos 3(\omega t + \phi) \cdots + I_n \cos n(\omega t + \phi) \tag{2.10}$$

where

$$I_0 = a_0 + \tfrac{1}{2}a_2V^2 + \tfrac{3}{8}a_4V^4 + \cdots$$
$$I_1 = a_1V + \tfrac{3}{4}a_3V^3 + \tfrac{5}{8}a_5V^5 + \cdots$$
$$I_2 = \tfrac{1}{2}a_2V^2 + \tfrac{1}{2}a_4V^4 + \cdots$$
$$I_3 = \tfrac{1}{4}a_3V^3 + \tfrac{5}{16}a_5V^5 + \cdots$$

Comparing Eqs. (2.3) and (2.10), we find:

For nonlinear elements, the output spectrum contains frequency components, which are multiples of the input signal frequency. A number in the highest frequency component is equal to a maximum degree of the power series. Therefore, if it is necessary to know the amplitude of n-harmonic response, the volt-ampere characteristic of nonlinear element should be approximated by a power series of order not less than n.

The dc output component and even-order harmonic components are determined by only the even voltage degrees in the device transfer characteristic given by Eq. (2.3). The odd-order harmonic components are defined by only the odd voltage degrees for the single harmonic input signal given in Eq. (2.4).

The current phase ψ_k of k-order harmonic component $\omega_k = k\omega$ is k times larger than the input signal current phase ψ:

$$\psi_k = \omega_k t + \phi_k = k(\omega t + \phi) \tag{2.11}$$

that is also applied to their initial phases, which are defined as

$$\phi_k = k\phi \tag{2.12}$$

Piecewise-linear approximation

The piecewise-linear approximation of the active device volt-ampere characteristic results from replacing the real nonlinear current-voltage dependence $i = f(v)$ with an approximated one that consists of the straight lines tangent to the real dependence at the specified points. Such an approximation for the case of two straight lines is shown in Fig. 2.1.

The output current waveforms for the initial actual voltage-ampere dependence (dashed line) and its two-straight-line approximation

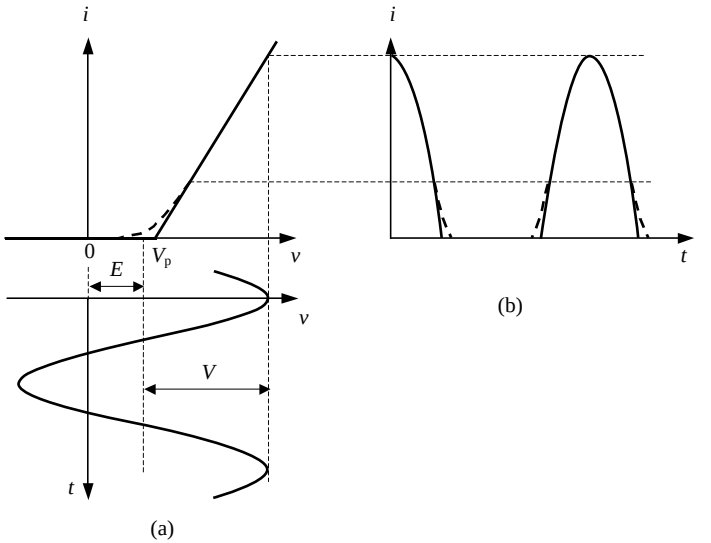

Figure 2.1 Piecewise-linear approximation.

(solid line) are plotted in Fig. 2.1(*b*). Under large-signal operation mode, the waveforms of these two dependencies are practically the same, with negligible deviations for small current values. Consequently, at least two first output current components, dc and fundamental, can be calculated through a Fourier-series expansion with sufficient accuracy. Therefore, such a piecewise-linear approximation with two straight lines is quite popular in practice when it is necessary to determine the result of the large-signal effect.

The active device volt-ampere characteristic is

$$i = \begin{cases} 0 & \text{when } v \le V_p \\ g_m(v - V_p) & \text{when } v \ge V_p \end{cases} \tag{2.13}$$

where g_m is the transconductance and V_p is the approximated pinch-off voltage.

Consider the effect of the input signal in the form of

$$v = E + V\cos\omega t \tag{2.14}$$

on the nonlinear element, the volt-ampere characteristic of which is approximated by two straight lines (as shown in Fig. 2.2), where E is the bias voltage. As a result, the output current represents a sequence of the cosinusoidal pulses with maximum height of I_{max} and width of 2θ, and can be calculated within the interval $-\theta \le \omega t \le \theta$ as follows:

$$i = KN - MN = I\cos\omega t - I\cos\theta = I(\cos\omega t - \cos\theta) \tag{2.15}$$

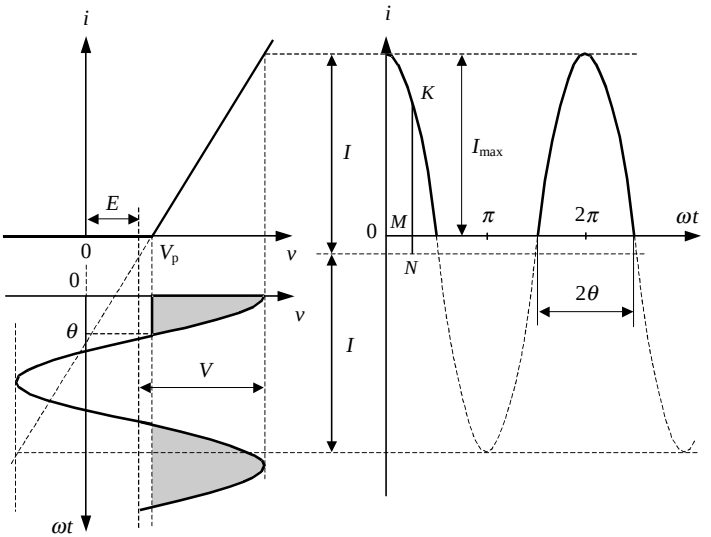

Figure 2.2 Schematic definition of conduction angle.

Taking into account that $I = g_m V$, Eq. (2.15) can be rewritten as

$$i = g_m V(\cos \omega t - \cos \theta) \tag{2.16}$$

When $\omega t = 0$, then $i = I_{max}$, and

$$I_{max} = g_m V(1 - \cos \theta) \tag{2.17}$$

The angular time θ characterizes the class of the active device operation. If $\theta = \pi$ (or 180°), the device operates in the active region during the entire period (class A operation). When $\theta = \pi/2$ (or 90°), the device operates half a wave period in the active region and half a wave period in the pinch-off region (class B operation). The values of $\theta > 90°$ correspond to class AB operation with a certain value of the quiescent output current. Therefore, it is advisable to name the angular time 2θ as the conduction angle, the value of which directly indicates a class of the active device operation.

The Fourier-series expansion of the even function when $i(t) = i(-t)$ contains only even component functions, and can be written as

$$i(t) = I_0 + I_1 \cos \omega t + I_2 \cos \omega t + I_3 \cos \omega t + \cdots \tag{2.18}$$

The dc, fundamental, and n-order components are calculated as

follows:

$$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} g_m V(\cos\omega t - \cos\theta)d(\omega t) = g_m V\gamma_0(\theta) \tag{2.19}$$

$$I_1 = \frac{1}{\pi}\int_{-\theta}^{\theta} g_m V(\cos\omega t - \cos\theta\cos\omega t d(\omega t) = g_m V\gamma_1(\theta) \tag{2.20}$$

$$I_n = \frac{1}{\pi}\int_{-\theta}^{\theta} g_m V(\cos\omega t - \cos\theta)\cos(n\omega t)\,d(\omega t) = g_m V\gamma_n(\theta) \tag{2.21}$$

where $\gamma_0(\theta) = \dfrac{1}{\pi}(\sin\theta - \theta\cos\theta)$

$$\gamma_1(\theta) = \frac{1}{\pi}(\theta - \sin\theta\cos\theta)$$

$$\gamma_n(\theta) = \frac{2}{\pi}\frac{\sin n\theta\cos\theta - n\cos n\theta\sin\theta}{n(n^2-1)}, \quad n = 2, 3, \ldots$$

The dependencies of $\gamma_n(\theta)$ for the dc, fundamental, and second current components are shown in Fig. 2.3. The maximum value of $\gamma_n(\theta)$ is achieved when $\theta = 180^\circ/n$. By using these dependencies the appropriate current component amplitude can be determined as

$$I_n = g_m V\gamma_n(\theta) \tag{2.22}$$

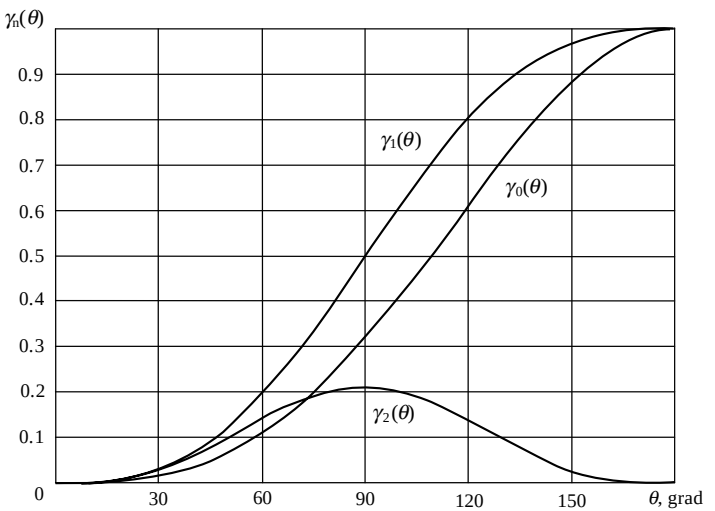

Figure 2.3 Dependencies of $\gamma_n(\theta)$ for dc, fundamental, and second current components.

A plot of the Fourier amplitudes on the frequency axis, given by Eqs. (2.19) to (2.21), is called the single-sideband amplitude spectrum of $i(t)$. The normalized power of $i(t)$, according to Parseval's theorem for real periodic waveforms, is equal to the sum of the normalized powers of the individual components, i.e.,

$$\frac{1}{T}\int_0^T i^2(t)\,\mathrm{d}t = I_o^2 + \frac{1}{2}\sum_{n=1}^{\infty} I_n^2 \tag{2.23}$$

A plot of the normalized powers corresponding to the Fourier components in Eq. (2.18) versus frequency is called the *single-sideband power spectrum* of $i(t)$. The height of each spectrum component is numerically equal to the average power that would be dissipated if the nth harmonic current were applied across the terminals of a 1-Ω resistance. Consequently, the sum of the heights of all components in the power spectrum is numerically equal to the average power that would be dissipated if $i(t)$ were applied across the terminals of a 1-Ω resistance.

Sometimes it is required to retain the value of $I_{\max}$ is constant at any values of θ. This requires an appropriate change in the input amplitude V. In this case, it is more convenient to use the following coefficients to determine the ratios of the current harmonic component amplitudes to the current cosinusoidal pulse amplitude:

$$\alpha_n = I_n / I_{\max} \tag{2.24}$$

From Eqs. (2.17) and (2.22) it follows that

$$\alpha_n = \gamma_n(\theta)/(1-\cos\theta) \tag{2.25}$$

and the maximum value of $\alpha_n(\theta)$ is achieved when $\theta = 120^\circ/n$.

Bessel functions

The Bessel functions are used to analyze the power amplifier operation mode when the nonlinear behavior of the active device can be described by the exponential functions. The transfer voltage-ampere characteristic of the bipolar transistor is approximated by the following simplified exponential dependence, neglecting reverse base-emitter current:

$$i(v) = I_{\text{sat}}\left[\exp\left(\frac{v}{V_T}\right) - 1\right] \tag{2.26}$$

where I_{sat} is the minority carrier saturation current, and V_T is the temperature voltage. If the effect of the input signal given by Eq. (2.14) is

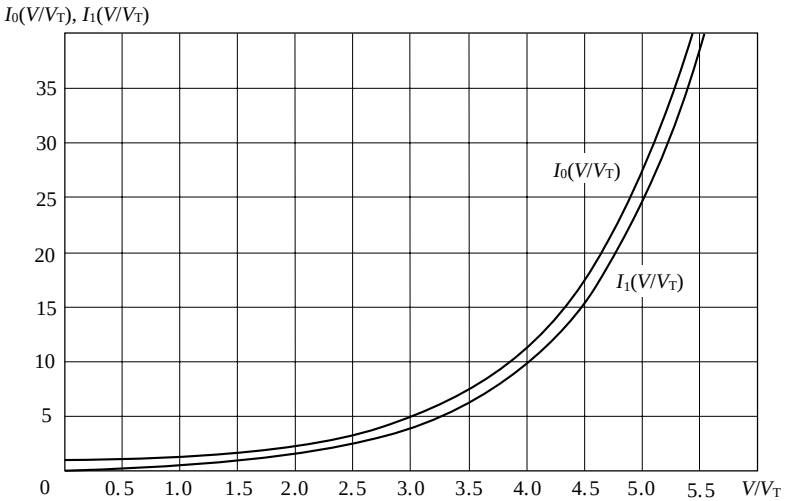

Figure 2.4 Zero-order and first-order modified Bessel functions of the first kind.

considered, then Eq. (2.26) can be rewritten as follows:

$$i(t) = I_{\text{sat}}\left[\exp\left(\frac{E}{V_T}\right)\exp\left(\frac{V\cos\omega t}{V_T}\right) - 1\right] \tag{2.27}$$

The current i in Eq. (2.27) is the even function of ωt and, consequently, it can be represented by the Fourier-series expansion given by Eq. (2.18). To determine the Fourier components, the following expressions are used:

$$\exp\left(\frac{V\cos\omega t}{V_T}\right) = I_0\left(\frac{V}{V_T}\right) + 2\sum_{k=1}^{\infty} I_k\left(\frac{V}{V_T}\right)\cos(k\omega t) \tag{2.28}$$

where $I_k(V/V_T)$ are the k-order modified Bessel functions of the first kind for an argument of V/V_T shown in Fig. 2.4 for the zero-order and first-order components. It should be noted that $I_0(0) = 1$ and $I_1(0) = I_2(0) = \cdots = 0$, and with an increase of the component number its amplitude appropriately decreases.

According to Eq. (2.28), the current i defined by Eq. (2.26) can be rewritten as

$$i(t) = I_{\text{sat}}\left[\exp\left(\frac{E}{V_T}\right)I_0\left(\frac{V}{V_T}\right) - 1\right] + 2I_{\text{sat}}\exp\left(\frac{E}{V_T}\right)I_1\left(\frac{V}{V_T}\right)\cos(\omega t) + 2I_{\text{sat}}\exp\left(\frac{E}{V_T}\right)I_2\left(\frac{V}{V_T}\right)\cos(2\omega t) + 2I_{\text{sat}}\exp\left(\frac{E}{V_T}\right)I_3\left(\frac{V}{V_T}\right)\cos(3\omega t) + \cdots \tag{2.29}$$

As a result, comparing Eq. (2.29) with Eq. (2.18) allows constant, fundamental, and n-order Fourier current components to be determined:

$$I_0 = I_{\text{sat}}\left[\exp\left(\frac{E}{V_{\text{T}}}\right) I_0\left(\frac{V}{V_{\text{T}}}\right) - 1\right] \tag{2.30}$$

$$I_1 = 2I_{\text{sat}} \exp\left(\frac{E}{V_{\text{T}}}\right) I_1\left(\frac{V}{V_{\text{T}}}\right) \tag{2.31}$$

$$I_{\text{n}} = 2I_{\text{sat}} \exp\left(\frac{E}{V_{\text{T}}}\right) I_{\text{n}}\left(\frac{V}{V_{\text{T}}}\right), \quad n = 2, 3, \ldots \tag{2.32}$$

When using the Bessel functions, the following relationships can be applied:

$$2\frac{\text{d}I_{\text{n}}(V/V_{\text{T}})}{\text{d}(V/V_{\text{T}})} = I_{\text{n}+1}\left(\frac{V}{V_{\text{T}}}\right) + I_{\text{n}-1}\left(\frac{V}{V_{\text{T}}}\right) \tag{2.33}$$

$$\frac{\text{d}I_0(V/V_{\text{T}})}{\text{d}(V/V_{\text{T}})} = I_1\left(\frac{V}{V_{\text{T}}}\right) \tag{2.34}$$

$$\frac{2n}{(V/V_{\text{T}})} I_{\text{n}}\left(\frac{V}{V_{\text{T}}}\right) = I_{\text{n}-1}\left(\frac{V}{V_{\text{T}}}\right) - I_{\text{n}+1}\left(\frac{V}{V_{\text{T}}}\right) \tag{2.35}$$

$$I_{\text{n}}\left(-\frac{V}{V_{\text{T}}}\right) = (-1)^{\text{n}} I_{\text{n}}\left(\frac{V}{V_{\text{T}}}\right) \tag{2.36}$$

Time Domain Analysis

A time domain analysis establishes the relationships between voltage and current in each circuit element in the time domain when a system of equations is obtained by applying Kirchhoff's law to the circuit to be analyzed. Commonly, in a nonlinear circuit, such a system will be composed of nonlinear integro-differential equations. The solution to this system can be found by applying the numerical integration methods. Therefore, the choices of the time interval and the initial point are very important to provide a compromise between the speed and accuracy of calculation; the smaller the interval, the smaller the error, but the number of points to be calculated for each period will be greater, which will make the calculation slower.

To analyze a nonlinear system in the time domain, it is necessary to know the voltage-current relationships for all elements used in RF and microwave circuits. For example, for linear resistance R, when the sinusoidal voltage applies and current is flowing through it, the voltage-current relationship in the time domain is given by

$$V = RI \tag{2.37}$$

where V is the voltage amplitude and I is the current amplitude. For linear capacitance C,

$$i(t) = \frac{\mathrm{d}q(t)}{\mathrm{d}t} = \frac{\mathrm{d}q}{\mathrm{d}v}\frac{\mathrm{d}v}{\mathrm{d}t} = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{2.38}$$

For linear inductance L,

$$v(t) = \frac{\mathrm{d}\varphi(t)}{\mathrm{d}t} = \frac{\mathrm{d}\varphi}{\mathrm{d}i}\frac{\mathrm{d}i}{\mathrm{d}t} = L\frac{\mathrm{d}i}{\mathrm{d}t} \tag{2.39}$$

where φ is the magnetic flux across the inductance.

Nonlinear dependencies, such as $q(v)$ or $\varphi(i)$, should each be expanded in a Taylor series by subtracting the dc components and substituting into Eqs. (2.38) and (2.39) to obtain the expressions for appropriate incremental capacitance and inductance. Then, for the quasilinear case, the capacitance and inductance can be defined by

$$C(E) = \left.\frac{\mathrm{d}q(v)}{\mathrm{d}v}\right|_{v=E} \tag{2.40}$$

and

$$L(I) = \left.\frac{\mathrm{d}\varphi(i)}{\mathrm{d}i}\right|_{i=I_0} \tag{2.41}$$

where E is the dc voltage across the capacitor, and I_0 is dc current flowing through the inductance.

Figure 2.5 shows the electrical schematic of the first-order RL-circuit connected to the independent voltage source E at the moment $t = 0$. When we first connect a voltage source to a circuit containing an inductance as an energy-storage element, the current in the RL-circuit does not immediately reach its steady-state value. This means that there is a transient response that characterizes the step-driven circuit with an energy-storage element. Let us assume the zero initial conditions of the RL-circuit. Now we wish to solve for current i at all $t > 0$. According to Kirchhoff's voltage law, the algebraic sum of the voltages across the

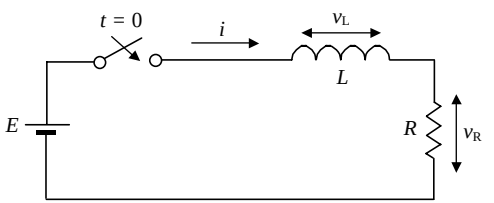

Figure 2.5 Schematic of RL-circuit with connected source for $t > 0$.

circuit elements ($v_L = Ldi/dt$, $v_R = Ri$, and $v = E$) should be equal to zero, $v_L + v_R - v = 0$, resulting in the following linear nonhomogeneous first-order differential equation:

$$L\frac{di}{dt} + Ri = E \tag{2.42}$$

which general solution can be obtained in the form of

$$i(t) = \frac{E}{R} + A\exp\left(-\frac{R}{L}t\right) \tag{2.43}$$

The unknown coefficient A can be found from the initial conditions when, for $t = 0$, the circuit current $i(0) = 0$. Consequently,

$$i(t) = \frac{E}{R}\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] \tag{2.44}$$

and

$$v_L(t) = L\frac{di}{dt} = \frac{E}{R}\exp\left(-\frac{t}{\tau}\right) \tag{2.45}$$

where $\tau = L/R$ is the time constant of the RL-circuit.

Thus, the current $i(t)$ in the RL-circuit starts to monotonically grow from its zero value, $i(0) = 0$ at $t = 0$, asymptotically (by means of exponential functions) approaching the final dc value of $i(\infty) = I = E/R$ at $t \to \infty$ when $v_L(\infty) = 0$ and $v_R(\infty) = E$ according to Eqs. (2.44) and (2.45).

Figure 2.6 shows the electrical schematic of the nonlinear parallel circuit that contains the capacitance as a nonlinear element depending on the applied voltage. Such a capacitance can represent the nonlinear capacitance of p-n junction of the bipolar transistor or internal gate source and gate-drain capacitances of MOSFET or MESFET devices. Let us assume that the loaded quality factor of the parallel circuit is high enough for us to expect that the voltage across the circuit is sinusoidal, $v = V\sin\omega t$, even if the current i contains the higher-order harmonic components. Then, according to Eq. (2.38) where $C = C(v)$,

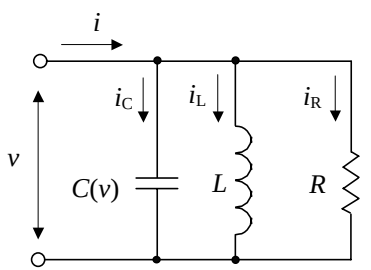

Figure 2.6 Schematic of nonlinear parallel circuit.

the following equation for current flowing through the nonlinear capacitance C can be obtained:

$$i_C = C(v)\omega V \cos \omega t \tag{2.46}$$

In the case of the second-order polynomial approximation of the nonlinear capacitance given by

$$C(v) = C_0 + A_1 v + A_2 v^2 \tag{2.47}$$

where C_0, A_1, and A_2 are the coefficients with positive values, by using the trigonometric identity given by Eq. (2.6), Eq. (2.46) can be rewritten in the form of

$$i_C = \left(C_0 + \frac{A_2}{2} V^2 + A_1 V \sin \omega t - \frac{A_2}{2} V^2 \cos 2\omega t \right) \omega V \cos \omega t \tag{2.48}$$

From Eq. (2.48), it follows that the fundamental harmonic of this current i_{C1} through the nonlinear capacitance C can be represented by

$$i_{C1} = \left(C_0 + \frac{A_2}{4} V^2 \right) \omega V \cos \omega t \tag{2.49}$$

The same result for current i_{C1} can be obtained by including the equivalent (or fundamentally averaged) capacitance C_{avr} instead of the nonlinear capacitance according to

$$C_{avr} = C_0 + \frac{A_2}{4} V^2 \tag{2.50}$$

whose value increases for larger values of voltage amplitude V.

The transmission line in the time domain can be represented as an element with finite delay time depending on its electrical length. Consider the simple load network of the power amplifier shown in Fig. 2.7, which consists of a parallel quarterwave transmission line RF grounded at the end by a bypass capacitor, a series fundamentally tuned L_0C_0 circuit, and a load resistance R. In an idealized case, the intrinsic device output capacitance is assumed to be negligible to affect the power amplifier RF performance. The loaded quality factor Q_L of the series resonant L_0C_0-circuit is high enough to provide the sinusoidal output current i_R flowing into the load R.

To define the collector voltage and current waveforms, consider the electrical behavior of a homogeneous lossless quarterwave transmission line connected to the dc voltage supply with RF grounding [1]. In this case, the voltage $v(t, x)$ in any cross section of such a transmission line can be represented as a sum of the incident and reflected voltages, $v_{inc}(\omega t - 2\pi x/\lambda)$ and $v_{refl}(\omega t + 2\pi x/\lambda)$, generally with an

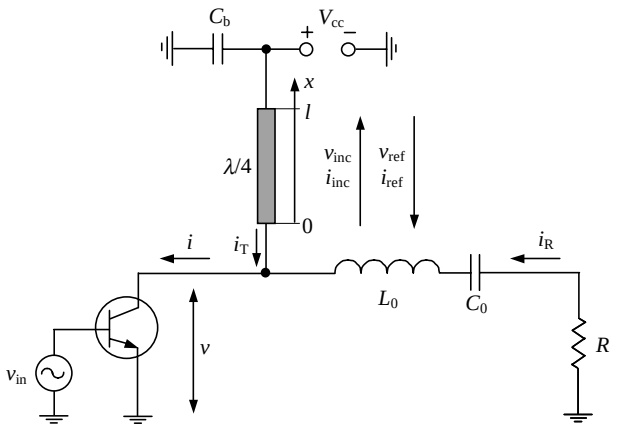

Figure 2.7 Power amplifier load network with quarterwave transmission line.

arbitrary waveform. When $x = 0$, the voltage $v(t, x)$ is equal to the collector voltage:

$$v(\omega t) = v(t, 0) = v_{\text{inc}}(\omega t) + v_{\text{refl}}(\omega t) \tag{2.51}$$

At the same time, at another end of the transmission line when $x = \lambda/4$, the voltage is constant and equal to

$$V_{\text{cc}} = v(t, \pi/2) = v_{\text{inc}}(\omega t - \pi/2) + v_{\text{refl}}(\omega t + \pi/2) \tag{2.52}$$

Since the time moment t was chosen arbitrarily, let us rewrite Eq. (2.52) using a phase shift of $\pi/2$ for each voltage by

$$v_{\text{inc}}(\omega t) = V_{\text{cc}} - v_{\text{refl}}(\omega t + \pi) \tag{2.53}$$

Substituting Eq. (2.53) into Eq. (2.51) yields

$$v(\omega t) = v_{\text{refl}}(\omega t) - v_{\text{refl}}(\omega t + \pi) + V_{\text{cc}} \tag{2.54}$$

Consequently, for the phase shift of π, the collector voltage can be obtained by

$$v(\omega t + \pi) = v_{\text{refl}}(\omega t + \pi) - v_{\text{refl}}(\omega t + 2\pi) + V_{\text{cc}} \tag{2.55}$$

For idealized operation conditions with a 50 percent duty cycle (when during half a period the transistor is turned on and during another half a period the transistor is turned off) with overall period of 2π, the voltage $v_{\text{refl}}(\omega t)$ can be considered as the periodical function with a period of 2π:

$$v_{\text{refl}}(\omega t) = v_{\text{refl}}(\omega t + 2\pi) \tag{2.56}$$

As a result, the summation of Eqs. (2.54) and (2.55) results in the following equation for collector voltage:

$$v(\omega t) = 2V_{cc} - v(\omega t + \pi) \tag{2.57}$$

From Eq. (2.57) it follows that the maximum value of the collector voltage cannot exceed a value of $2V_{cc}$ and the time duration with maximum voltage of $v = 2V_{cc}$ coincides with the time duration with minimum voltage of $v = 0$.

Similarly, an equation for the current i_T flowing into the quarterwave transmission line can be obtained by

$$i_T(\omega t) = i_T(\omega t + \pi) \tag{2.58}$$

which means that the period of signal flowing into the quarterwave transmission line is equal to π because it contains only even harmonic components, as such a transmission line has an infinite impedance at odd harmonics.

Let the transistor operate as an ideal switch when it is closed during the interval $0 < \omega t \leq \pi$ where $v = 0$ and opened during the interval $\pi < \omega t \leq 2\pi$ where $v = 2V_{cc}$ according to Eq. (2.57). During the interval $\pi < \omega t \leq 2\pi$ when the switch is opened, the load is directly connected to the transmission line and $i_T = -i_R = -I_R \sin \omega t$. Consequently, during the interval $0 < \omega t \leq \pi$ when the switch is closed, $i_T = I_R \sin \omega t$ according to Eq. (2.58). Hence, the current flowing into the quarterwave transmission line at any ωt can be represented by

$$i_T(\omega t) = I_R |\sin \omega t| \tag{2.59}$$

where I_R is the amplitude of current flowing into the load.

Since the collector current is defined as $i = i_T + i_R$,

$$i(\omega t) = I_R(\sin \omega t + |\sin \omega t|) \tag{2.60}$$

which means that the collector current represents half-sinusoidal pulses with amplitude equal to double the load current amplitude.

Consequently, for purely sinusoidal current flowing into the load—due to the infinite loaded quality factor of the series fundamentally tuned L_0C_0-circuit shown in Fig. 2.8(*a*)—the ideal collector voltage and current waveforms can be represented by the appropriate normalized waveforms shown in Figs. 2.8(*b*) and 2.8(*c*), respectively, where I_0 is the dc current. Here, a sum of odd harmonics approximates a square voltage waveform and a sum of the fundamental and even harmonics approximates a half-sinusoidal collector current waveform. The waveform corresponding to the normalized current flowing into the quarterwave transmission line shown in Fig. 2.8(*d*) represents a sum of

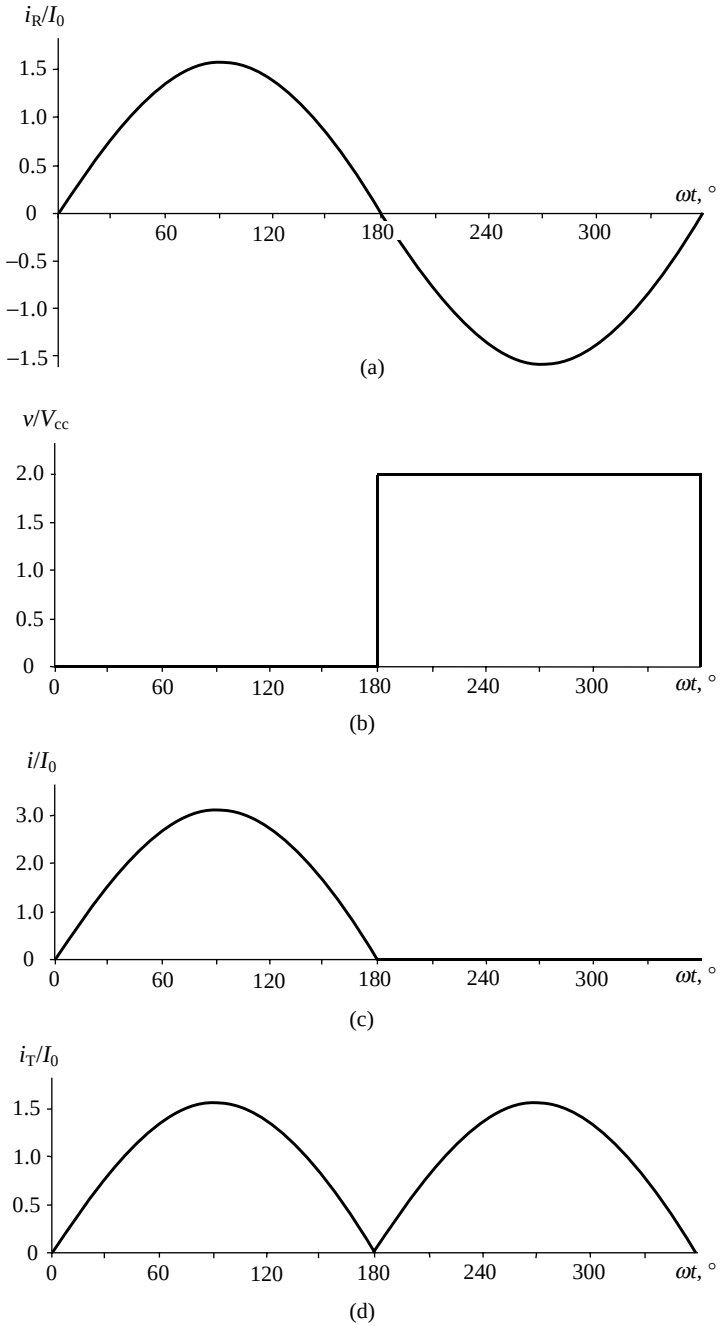

Figure 2.8 Ideal waveforms of power amplifier with quarterwave transmission line.

even harmonics. As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously. Such a condition, with symmetrical collector voltage and current waveforms, corresponds to idealized Class F operation mode with 100 percent collector efficiency (see Chap. 7).

Newton-Raphson Algorithm

To describe circuit behavior, it is necessary to solve the nonlinear algebraic equation, or system of equations, which do not admit a closed form solution analytically. One of the most common numerical methods to solve such equations is a method based on the Newton-Raphson algorithm [2]. The initial guess for this method is chosen using a Taylor series expansion of the nonlinear function. Consider a practical case when the device is represented by a two-port network where all nonlinear elements are the functions of two unknown voltages, input voltage v_{in} and output voltage v_{out}. As a result, after combining linear and nonlinear circuit elements, a system of two equations can be written as

$$\begin{cases} f_1(v_{\text{in}}, v_{\text{out}}) = 0 \\ f_2(v_{\text{in}}, v_{\text{out}}) = 0 \end{cases} \tag{2.61}$$

Assume that the variables v_{in0} and v_{out0} are the initial approximate solution of a system of Eq. (2.61). Then, the variables can be written as $v_{\text{in}} = v_{\text{in0}} + \Delta v_{\text{in}}$ and $v_{\text{out}} = v_{\text{out0}} + \Delta v_{\text{out}}$, where Δv_{in} and Δv_{out} are the linear increments of the variables. Applying a Taylor series expansion to Eq. (2.61) yields

$$f_1(v_{\text{in0}} + \Delta v_{\text{in}}, v_{\text{out0}} + \Delta v_{\text{out}}) = f_1(v_{\text{in0}}, v_{\text{out0}}) + \left.\frac{\partial f_1}{\partial v_{\text{in}}}\right|_{\substack{v_{\text{in}} = v_{\text{in0}} \\ v_{\text{out}} = v_{\text{out0}}}} \times \Delta v_{\text{in}} + \left.\frac{\partial f_1}{\partial v_{\text{out}}}\right|_{\substack{v_{\text{in}} = v_{\text{in0}} \\ v_{\text{out}} = v_{\text{out0}}}} \Delta v_{\text{out}} + o\left(\Delta v_{\text{in}}^2 + \Delta v_{\text{out}}^2 + \cdots\right) = 0 \tag{2.62}$$

$$f_2(v_{\text{in0}} + \Delta v_{\text{in}}, v_{\text{out0}} + \Delta v_{\text{out}}) = f_2(v_{\text{in0}}, v_{\text{out0}}) + \left.\frac{\partial f_2}{\partial v_{\text{in}}}\right|_{\substack{v_{\text{in}} = v_{\text{in0}} \\ v_{\text{out}} = v_{\text{out0}}}} \times \Delta v_{\text{in}} + \left.\frac{\partial f_2}{\partial v_{\text{out}}}\right|_{\substack{v_{\text{in}} = v_{\text{in0}} \\ v_{\text{out}} = v_{\text{out0}}}} \Delta v_{\text{out}} + o\left(\Delta v_{\text{in}}^2 + \Delta v_{\text{out}}^2 + \cdots\right) = 0 \tag{2.63}$$

where $o(\Delta v_{\text{in}}^2 + \Delta v_{\text{out}}^2 + \cdots)$ denotes the second- and higher-order components.

Neglecting the second- and higher-order components, Eqs. (2.62) and (2.63) can be rewritten in the matrix form:

$$-\begin{bmatrix} f_1 \\ f_2 \end{bmatrix} = \begin{bmatrix} \dfrac{\partial f_1}{\partial v_{\text{in}}} & \dfrac{\partial f_1}{\partial v_{\text{out}}} \\ \dfrac{\partial f_2}{\partial v_{\text{in}}} & \dfrac{\partial f_2}{\partial v_{\text{out}}} \end{bmatrix} \begin{bmatrix} \Delta v_{\text{in}} \\ \Delta v_{\text{out}} \end{bmatrix} \tag{2.64}$$

In the phasor form,

$$-\mathbf{F} = \mathbf{J}\Delta\mathbf{v} \tag{2.65}$$

where $\mathbf{J}$ is the Jacobian matrix of Eq. (2.61).

A solution of Eq. (2.65) for a nonsingular matrix $\mathbf{J}$ can be obtained by

$$\Delta\mathbf{v} = -\mathbf{J}^{-1}\mathbf{F} \tag{2.66}$$

This means that if

$$\mathbf{v}_0 = \begin{bmatrix} v_{\text{in0}} \\ v_{\text{out0}} \end{bmatrix}$$

is the initial guess of this system of equations, then the next (more precise) solution can be written as

$$\mathbf{v}_1 = \mathbf{v}_0 - \mathbf{J}^{-1}\mathbf{F} \tag{2.67}$$

where

$$\mathbf{v}_1 = \begin{bmatrix} v_{\text{in1}} \\ v_{\text{out1}} \end{bmatrix}$$

Thus, starting with initial guess $\mathbf{v}_0$, we compute $\mathbf{v}_1$ at the first iteration. For the iteration $n + 1$, we can write

$$\mathbf{v}_{\text{n}+1} = \mathbf{v}_{\text{n}} - \mathbf{J}^{-1}\mathbf{F}(\mathbf{v}_{\text{n}}) \tag{2.68}$$

The iterative Eq. (2.68) is given for a system of two equations; however, it can be directly extended to a system of k nonlinear equations with k unknown parameters. This iterative procedure is terminated after $n + 1$ iterations whenever

$$|\mathbf{x}_{\text{n}+1} - \mathbf{x}_{\text{n}}| = \sqrt{\sum_{k=1}^{K} \left(x_{\text{n}+1}^{k} - x_{\text{n}}^{k}\right)^2} < \varepsilon \tag{2.69}$$

where ε is a small positive number depending on the desired accuracy. For practical purposes, it is desirable that the Newton-Raphson algorithm should converge in a few steps. Therefore, the choice of an appropriate initial guess is crucial to the success of the algorithm.

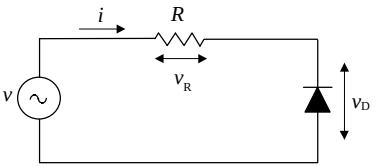

Figure 2.9 Circuit schematic with resistor, diode, and voltage source.

Consider the circuit shown in Fig. 2.9. According to Kirchhoff's voltage law,

$$v = v_R + v_D \tag{2.70}$$

where $v_R = iR$. The electrical behavior of the diode is described by Eq. (2.26). Rearranging Eq. (2.26) gives the equation for v_D in the form of

$$v_D = V_T \ln\left(\frac{i}{I_{sat}} + 1\right) \tag{2.71}$$

Thus, from Eqs. (2.70) and (2.71) it follows that

$$v = iR + V_T \ln\left(\frac{i}{I_{sat}} + 1\right) \tag{2.72}$$

This allows current i to be determined for a specified voltage v. However, because it is impossible to solve this equation analytically for current i in an explicit form, the solution must be found numerically.

Consider a case of dc voltage source V with constant current I. For the sinusoidal voltage source, it is necessary to calculate the Bessel functions for dc, fundamental, and higher-order harmonic current components. It is convenient to rewrite Eq. (2.72) as

$$f(I) = IR + V_T \ln\left(\frac{I}{I_{sat}} + 1\right) - V = 0 \tag{2.73}$$

from which

$$f'(I) = R + V_T \frac{1}{I + I_{sat}} \tag{2.74}$$

Then, applying the iterative algorithm for one variable,

$$I_n = I_{n-1} - \frac{f(I_{n-1})}{f'(I_{n-1})} \tag{2.75}$$

we obtain

$$I_n = I_{n-1} - \frac{I_{n-1}R + V_T \ln\left(\frac{I_{n-1}}{I_{sat}} + 1\right) - V}{R + V_T \frac{1}{I_{n-1} + I_{sat}}} \tag{2.76}$$

TABLE 2.1 Three-Step Iteration Procedure

n	I_n, A	ε_n
0	0.05	0.899371786
1	0.878469005	0.070902781
2	0.948955229	0.000416557
3	0.949371786	

The results of the numerical calculation of the currents I_n for each iteration for $V_T = 25.9$ mA/V, $R = 5\ \Omega$, $V = 5$ V, $I_{sat} = 10\ \mu$A, and initial current $I_0 = 50$ mA are given in Table 2.1. The calculation error $\varepsilon_n = I_N - I_n : n = 0, 1, \ldots, N$, for each iteration step illustrates the fast convergence to the solution. The error at each subsequent iteration step is approximately proportional to the square error at the previous step. If a required accuracy of $\varepsilon < 0.1\%$ is set in advance, the procedure will be stopped at the third iteration step.

Quasilinear Method

To simplify the power amplifier design procedure, in some cases it is enough to apply a quasilinear method based on the use of the ratios between the fundamental harmonics of currents and voltages, and the replacement of nonlinear elements by equivalent averaged fundamental linear ones. The derivation of equivalent averaged linear elements in terms of signal voltages is based on static voltage-ampere and voltage-capacitance active device characteristics.

For example, for a bipolar transistor all elements of its equivalent circuit are nonlinear, depending significantly on operation mode, especially transconductance g_m and base-emitter capacitance C_π. Taking into account that $\omega_T = g_m/C_\pi$, it is sufficient to limit the design to the nonlinear elements g_m, ω_T, and collector capacitance C_c, as the base resistance r_b poorly depends on a bias mode. The averaged large-signal transconductance can be easily determined from Eq. (2.31):

$$g_{m1} = \frac{I_1}{V} = \frac{2I_{sat}}{V}\exp\left(\frac{E}{V_T}\right) I_1\left(\frac{V}{V_T}\right) \tag{2.77}$$

The collector capacitance represents a junction capacitance and can be approximated by

$$C_c = C_{co}/\left(1 + \frac{v_c}{\varphi}\right)^{\gamma} \tag{2.78}$$

where φ is the built-in junction potential. If our interest is restricted to the fundamental frequency, and $v_c = E_c + V_c \sin \omega t$, where E_c is the

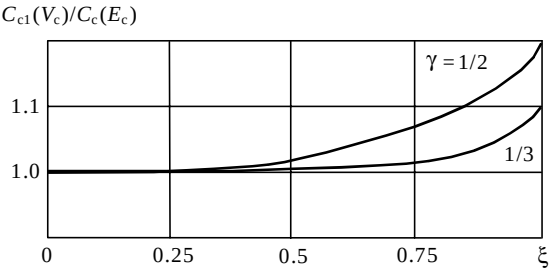

Figure 2.10 Large-signal behavior of device junction capacitance.

collector dc supply voltage, then the following current flows through the collector capacitance which is defined for the quasilinear case as

$$i_c = C_c(v_c)\frac{dv_c}{dt} = \frac{\omega C_{co} V_c \cos \omega t}{\left(1 + \frac{E_c}{\varphi} + \frac{V_c}{\varphi}\sin \omega t\right)^{\gamma}} = \frac{\omega C_c(E_c) V_c \cos \omega t}{(1 + \xi \sin \omega t)^{\gamma}} \tag{2.79}$$

where $C_c(E_c)$ is the small-signal capacitance in the operating point, $\xi = V_c/(E_c + \varphi)$. As a result, the averaged large-signal collector capacitance C_{c1} can be calculated through the fundamental Fourier series component as follows:

$$C_{c1} = I_{c1}/\omega V_c = \frac{C_c(E_c)}{\pi} \int_0^{2\pi} \frac{\cos^2 \omega t}{(1 + \xi \sin \omega t)^{\gamma}} d(\omega t) \tag{2.80}$$

Figure 2.10 shows the voltage dependencies of the averaged collector capacitance. Within a range of $\xi < 1$, the maximum large-signal value of $C_{c1}(V_c)$ deviates from the small-signal value of $C_c(E_c)$ by not more than 20 percent for an abrupt junction with $\gamma = 1/2$.

For a MESFET device, the drain current i_d is a function of the gate-source voltage v_{gs} and the drain-source voltage v_{ds}, $i_d = f(v_{gs}, v_{ds})$, which can be expanded in a two-dimensional Taylor series:

$$\begin{aligned} i_d(t) = I_{do} &+ \left.\frac{\partial f}{\partial v_{gs}}\right|_{\substack{v_{gs}=E_{gs}\\ v_{ds}=E_{ds}}} (v_{gs} - E_{gs}) + \left.\frac{\partial f}{\partial v_{ds}}\right|_{\substack{v_{gs}=E_{gs}\\ v_{ds}=E_{ds}}} (v_{ds} - E_{ds}) \\ &+ \frac{1}{2}\left[\left.\frac{\partial^2 f}{\partial v_{gs}^2}\right|_{\substack{v_{gs}=E_{gs}\\ v_{ds}=E_{ds}}} (v_{gs} - E_{gs})^2 + 2\left.\frac{\partial^2 f}{\partial v_{gs}\partial v_{ds}}\right|_{\substack{v_{gs}=E_{gs}\\ v_{ds}=E_{ds}}} (v_{gs} - E_{gs}) \right. \\ &\left. \times (v_{ds} - E_{ds}) + \left.\frac{\partial^2 f}{\partial v_{ds}^2}\right|_{\substack{v_{gs}=E_{gs}\\ v_{ds}=E_{ds}}} (v_{ds} - E_{ds})^2\right] + \cdots \end{aligned} \tag{2.81}$$

In the small-signal quasilinear case, the high-degree terms are neglected and

$$i_{\mathrm{d}}(t) = I_{\mathrm{do}} + \left.\frac{\partial f}{\partial v_{\mathrm{gs}}}\right|_{\substack{v_{\mathrm{gs}} = E_{\mathrm{gs}} \\ v_{\mathrm{ds}} = E_{\mathrm{ds}}}} (v_{\mathrm{gs}} - E_{\mathrm{gs}}) + \left.\frac{\partial f}{\partial v_{\mathrm{ds}}}\right|_{\substack{v_{\mathrm{gs}} = E_{\mathrm{gs}} \\ v_{\mathrm{ds}} = E_{\mathrm{ds}}}} (v_{\mathrm{ds}} - E_{\mathrm{ds}}) \tag{2.82}$$

The gate-source and drain-source instantaneous voltages can be written, respectively, as

$$v_{\mathrm{gs}} = E_{\mathrm{gs}} + V_{\mathrm{gs}} \cos(\omega t + \phi) \tag{2.83}$$

$$v_{\mathrm{ds}} = E_{\mathrm{ds}} + V_{\mathrm{ds}} \cos \omega t \tag{2.84}$$

where E_{gs} and E_{ds} are the dc bias voltages, V_{gs} and V_{ds} are the gate source and drain-source voltage amplitudes, and ϕ is the phase difference between gate-source and drain-source voltages.

Consequently, the instantaneous drain current given by Eq. (2.81) can be rewritten as [3]

$$i_{\mathrm{d}}(t) = f(v_{\mathrm{gs}}, v_{\mathrm{ds}}) = I_{\mathrm{do}} + \mathrm{g}_{\mathrm{m1}} V_{\mathrm{gs}} \cos(\omega t + \phi) + G_{\mathrm{ds1}} V_{\mathrm{ds}} \cos \omega t \tag{2.85}$$

where $g_{\mathrm{m1}} = \left.\frac{I_{\mathrm{d}}}{V_{\mathrm{gs}}}\right|_{V_{\mathrm{ds}}=0}$, $G_{\mathrm{ds1}} = \left.\frac{I_{\mathrm{d}}}{V_{\mathrm{ds}}}\right|_{V_{\mathrm{gs}}=0}$, I_{do} is the dc drain current, and I_{d} is the fundamental drain current amplitude, $G_{\mathrm{ds1}} = 1/R_{\mathrm{ds1}}$.

Multiplying the right and left parts of Eq. (2.85) by $\sin \omega t$ and integrating over a complete signal period, the averaged transconductance g_{m1} is obtained by

$$g_{\mathrm{m1}} = -\frac{1}{\pi V_{\mathrm{gs}} \sin \phi} \int_0^{2\pi} i_{\mathrm{d}} \sin \omega t \, \mathrm{d}(\omega t) \tag{2.86}$$

Similarly, multiplying by $\sin(\omega t + \phi)$, the averaged drain-source conductance can be obtained by

$$G_{\mathrm{ds1}} = \frac{1}{\pi V_{\mathrm{ds}} \sin \phi} \int_0^{2\pi} i_{\mathrm{d}} \sin(\omega t + \phi) \, \mathrm{d}(\omega t) \tag{2.87}$$

The averaged large-signal gate-source capacitance C_{gs1} can be calculated similarly to the abrupt collector capacitance C_{c1} of the bipolar transistor with $\gamma = 1/2$. The averaged gate forward conductance G_{gf1} is defined as

$$G_{\mathrm{gf1}} = \frac{2I_{\mathrm{sat}}}{V_{\mathrm{gs}}} \exp\left(\frac{E_{\mathrm{gs}}}{V_{\mathrm{T}}}\right) \cdot I_1\left(\frac{V_{\mathrm{gs}}}{V_{\mathrm{T}}}\right) \tag{2.88}$$

where I_{sat} is the saturation current of the Schottky barrier and $I_1(V_{gs}/V_T)$ is the first-order modified Bessel function of the first kind.

The gate charging resistance R_{gs} varies with the gate-source capacitance C_{gs} in such a way that the charging time constant $\tau_g = R_{gs}C_{gs}$ changes insignificantly, and it can be treated as a constant value for quasilinear approximation.

Harmonic Balance Method

Harmonic balance analysis determines the periodic steady-state circuit responses because the basis signal set chosen to represent the physical signals in the circuit consists of sinusoidal functions [4, 5]. The harmonic balance method requires that the circuit be divided into two subcircuits connected by wires forming multiports. One subcircuit contains the linear components of the circuit, and another contains the only nonlinear device model parameters, as shown in Fig. 2.11. The linear parasitic elements of the device are taken into account by the linear subcircuit. Sources and loads are concentrated in a separate multiport network. The N wires at the linear-nonlinear interface connect the two subcircuits and define corresponding nodes. Current flowing out of one subcircuit must equal that flowing into another. Matching the frequency components in each wire satisfies the continuity equation for current. An iterative process calculates the current at each wire so that the obtained dependencies are satisfied for both the linear and nonlinear sides of the overall circuit.

The nonlinear subcircuit is represented by a set of nonlinear equations:

$$i_k(t) = f[v_1(t), v_2(t), \ldots, v_N(t)] \tag{2.89}$$

where f is an arbitrary nonlinear function (and can include differentiation and integration), and i_k and v_k are the kth-port current and voltage, respectively. The linear subcircuit response is calculated in the frequency domain at each harmonic component by linear analysis and is represented by an $N \times (N + M)$ matrix. The M additional variables are the additional external nodes to which voltage or current sources

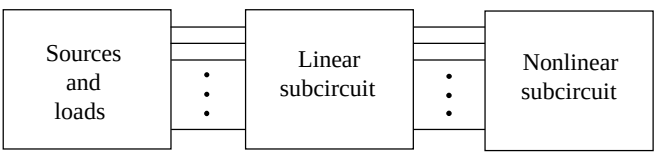

Figure 2.11 Harmonic balance circuit representation.

are connected. In the case of an applied input signal containing a sum of harmonics at ω, $2\omega, \ldots, K\omega$, there will be $(K+1)$ matrices so that the matrix relationship between the port voltages and currents can be written as

$$\begin{bmatrix} v_1(k\omega) \\ \vdots \\ v_{\mathrm{N}}(k\omega) \end{bmatrix} = \begin{bmatrix} H_{11}(k\omega) & H_{12}(k\omega) & \cdots & H_{1(\mathrm{N+M})}(k\omega) \\ H_{21}(k\omega) & H_{22}(k\omega) & \cdots & H_{2(\mathrm{N+M})}(k\omega) \\ \vdots & \vdots & \ddots & \vdots \\ H_{\mathrm{N1}}(k\omega) & H_{\mathrm{N2}}(k\omega) & \cdots & H_{\mathrm{N(N+M)}}(k\omega) \end{bmatrix} \begin{bmatrix} i_1(k\omega) \\ \vdots \\ i_{\mathrm{N}}(k\omega) \\ i_{\mathrm{N+1}}(k\omega) \\ \vdots \\ i_{\mathrm{N+M}}(k\omega) \end{bmatrix} \tag{2.90}$$

where $H_{\mathrm{ij}}(k\omega)$ are impedance or transfer ratios, depending on which of the variables are voltages and which are currents, $k = 0, 1, \ldots, K$. The harmonic balance program finds a simultaneous solution to Eqs. (2.89) and (2.90) for $v_1, v_2, \ldots, v_{\mathrm{N}}$, so that $i_1, i_2, \ldots, i_{\mathrm{N}}$ can be determined.

Figure 2.12 illustrates the application of the harmonic balance method to a three-terminal MESFET device. The MESFET device is presented by only nonlinear elements whereas all its parasitics, matching and output networks are incorporated into a linear subcircuit. The source terminal is chosen as a reference, so that $N = 2$. Here, the voltages v_1 and v_2 are independent variables, as are the currents i_1 and i_2. Additional applied sources are the external voltage sources V_1 and V_2. As a result, the output current flowing into the load or voltage across the load can be readily found once i_1 and i_2 are determined. Since Eq. (2.89) is stated in the time domain and Eq. (2.90) is stated in the frequency domain, time-to-frequency conversion is achieved using a discrete Fourier transform. An initial estimate must be made for $i_{\mathrm{j}}(t)$ and $v_{\mathrm{j}}(t)$, $j = 1, \ldots, N$, because their values are unknown at the beginning of calculation. Iteration between Eqs. (2.89) and (2.90) is performed using a discrete

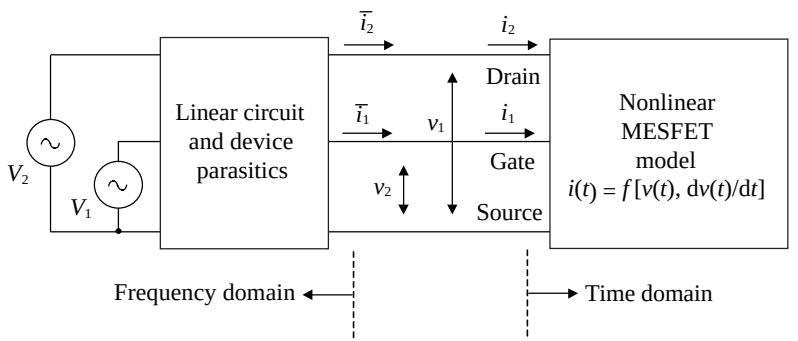

Figure 2.12 Application of harmonic balance method to three-terminal MESFET device.

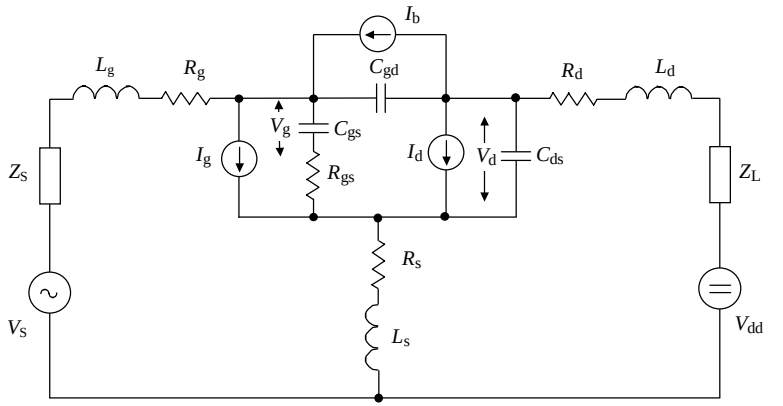

Figure 2.13 MESFET power amplifier equivalent circuit.

Fourier transform to obtain the frequency components calculated in the time domain using Eq. (2.89) until a self-consistent set of variables that satisfy the current continuity equations is attained. The continuity equation for current states that the "nonlinear" currents i_j must be equal to the "linear" currents $\bar{i}_j$ that corresponds to zero error function as a solution.

Figure 2.13 shows the equivalent circuit of a power amplifier, including a nonlinear MESFET circuit model, the input and output matching circuits, and the source and load impedances [5]. The device model includes both linear and nonlinear elements which can be characterized by the appropriate measurement or modeling. The largest contributions to the nonlinear device behavior are made by the nonlinear drain current source I_d, forward-bias gate current source I_g and gate-to-drain current source I_b which are assumed to be functions of the instantaneous internal gate voltage V_g and drain voltage V_d. An analysis of the circuit shown in Fig. 2.13 using Kirchhoff's voltage and current laws in the frequency domain results in two complex algebraic equations with V_g and V_d as the independent variables for each kth Fourier component:

$$AV_{gk} + BV_{dk} = C \tag{2.91}$$

$$DV_{gk} + EV_{dk} = F \tag{2.92}$$

where $A = 1 + jk\omega\lfloor(Z_2 + R_{gs})C_{gs} + (Z_1 + Z_S)(C_{gs} + C_{gd} + jk\omega R_{gs}C_{gs}C_{gd})\rfloor$

$B = jk\omega\lfloor-(Z_1 + Z_S)C_{gd} + Z_2C_{ds}\rfloor$

$C = -(Z_1 + Z_2 + Z_S)I_g + (Z_1 + Z_S)I_b - Z_2I_d + V_S$

$D = jk\omega\lfloor Z_2C_{gs} - (Z_3 + Z_L)(C_{ds} + jk\omega R_{gs}C_{gs}C_{ds})\rfloor$

$E = 1 + jk\omega\lfloor Z_2C_{gs} + (Z_3 + Z_L)(C_{gd} + C_{gs})\rfloor$

$F = -Z_2I_g - (Z_3 + Z_L)I_b + (Z_2 + Z_3 + Z_L)I_d + V_{DD}$

$Z_1 = R_g + jk\omega L_g$, $Z_2 = R_s + jk\omega L_s$, $Z_3 = R_d + jk\omega L_d$, $k = 1, \ldots, N$

Here, the matrices A, B, D, and E describe the linear network and the matrices C and F represent independent driving sources. The nonlinearity in these equations is contained in the currents I_g, I_b, and I_d, which commonly depend on both V_g and V_d. Consequently, Eqs. (2.91) and (2.92) determine voltages V_g and V_d only implicitly. The system of these equations is best solved computationally using an iterative technique.

The iterative solution process begins with an initial approximation to the solution, which can be made by neglecting the gate forward bias current I_g and the gate-to-drain current I_b and assuming a linear device output conductance or transconductance. Setting and substituting the initial values of the bias current, fundamental drain current amplitude and phase into Eqs. (2.91) and (2.92) (rearranged with the real and imaginary parts) allows calculation of the appropriate bias gate and drain voltages and fundamental gate and drain voltages in the frequency domain. Rewriting the voltages $v_g(t)$ and $v_d(t)$ in the time domain,

$$v_g(t) = V_{g0} + V_{g1}\cos(\omega t + \phi_{g1}) \tag{2.93}$$

$$v_d(t) = V_{d0} + V_{d1}\cos(\omega t + \phi_{d1}) \tag{2.94}$$

and substituting them into nonlinear current expressions $i_g(v_g, v_d)$ and $i_d(v_g, v_d)$ gives the Fourier components for each current harmonic with the appropriate amplitude and phase. Then, at each iteration step, inserting every gate and drain current written in a complex form into Eqs. (2.91) and (2.92) allows us to obtain the complex gate and drain harmonic voltages. Their representation in the time domain can be given by

$$v_g(t) = \sum_{k=1}^{N} V_{gk}\cos(k\omega t + \psi_{gk}) \tag{2.95}$$

$$v_d(t) = \sum_{k=1}^{N} V_{dk}\cos(k\omega t + \psi_{dk}) \tag{2.96}$$

which, in turn, allows us to define the complex gate and drain currents by insertion into their nonlinear expressions. Finally, when the accuracy of the solution is satisfied, the iterative process ends. In this case, an error function, which defines the duration of this iterative procedure, can be written in a mean square form.

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Chapter

3

Nonlinear Active Device Modeling

Power amplifier and oscillator circuit design and simulation is based mostly on active device electrical equivalent circuits, closed-form design equations, and semiempirical techniques. Accurate device modeling is extremely important for the development of monolithic integrated circuits. Better approximations of the final design can be achieved only if the nonlinear device behavior is described accurately. Once a device model has been incorporated into a circuit simulator, it requires the parameters to specify the device characteristics according to the model equations. The next step is to provide a procedure for adequate extraction of S-parameter data. This poses the problem of how to extract the device parameters from the measurement results accurately, rapidly, and without unnecessary measurement complexity. The best way is to minimize the device bias points under S-parameter measurements and to combine the analytical approach with a final optimization procedure to provide the best fitting of the experimental curves and empirical equation-based model curves. Numerical optimization is often used to fit the model S-parameters to the measured parameters since the resulting device element values depend on the starting values and are not unique. The analytical approach incorporates a derivation of the basic intrinsic device parameters from its equivalent circuit based on S- to Y-parameter or Z-parameter transformations using sufficiently simple equations. However, it is crucial that we choose an appropriately large-signal model that is suitable for a specific active device, accurately describes the nonlinear behavior of its equivalent circuit parameters and contains a reasonable number of model parameters to be determined.

This chapter describes all necessary steps for an accurate device modeling procedure, beginning with the determination of the small-signal equivalent circuit parameters. A variety of nonlinear models for MOSFET, MESFET, HEMT, and bipolar devices including HBTs, which are very prospective for modern microwave monolithic integrated circuits of power amplifiers and oscillators, are presented. Measured and modeled volt-ampere and voltage-capacitance characteristics are analyzed to show the advantages and drawbacks of nonlinear device models.

Power MOSFETs

Personal wireless communication services have been driving the development of silicon MOSFET worldwide to provide reliable low-cost and high-performance technology. For example, the LDMOS device structures have proven to be highly efficient, high gain and linear for both high-power and low-voltage microwave and RF applications, including power amplifiers, low-noise amplifiers, mixers, and voltage–controlled oscillators [1–3]. To develop low cost silicon MOSFET for higher speed and higher frequency integrated circuits and subsystems within a shorter design time, it is necessary to create accurate device models that allow efficient CAD simulation. Several well-known physically based MOSFET models describe the device behavior [4, 5]. However, some of them, such as Level 1, Level 2, or Level 3 large-signal models, are very simple and cannot describe the volt-ampere and voltage-capacitance characteristics with acceptable accuracy. Other popular models, as the BSIM3v3 model, are too complicated and may not be as accurate for RFIC simulation due to their derivative discontinuity regarding the overall bias conditions. Moreover, microwave parasitic effects in silicon MOSFET are not easy physically predictable. Table-based models, such as the HP Root model, are only accurate for the characterized structures and measurement conditions. An empirical analytical modeling approach is a valid compromise between physical models and data-based models, which has been proven successfull in GaAs MMIC development.

Small-signal equivalent circuit

To describe accurately the nonlinear properties of the large MOSFET devices, it is necessary to take into account the distributed nature of the gate capacitor, because the channel resistance is not equal to zero. In this case, the channel of such a device can be modeled as a bias-dependent *RC* distributed transmission line along the channel length, as shown in Fig. 3.1. This one-dimensional approach assumes a gradual channel approximation when the quantity of charge in the channel is

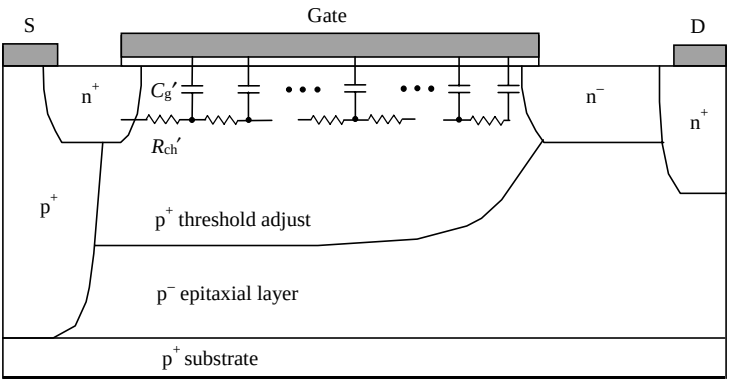


Figure 3.1 Schematic representation of MOSFET distributed channel structure.

controlled completely by the gate electrode; only fields in the vertical dimension influence the depletion region and channel current is provided entirely by drift with a constant mobility. Despite some drawbacks related to short-channel devices, this approach allows a compromise between the accuracy and simplicity of a model derivation.

The [*ABCD*]-matrix of the given *RC* transmission line can be written as follows:

$$[ABCD] = \begin{bmatrix} \cosh \gamma L & Z_0 \sinh \gamma L \\ \dfrac{\sinh \gamma L}{Z_0} & \cosh \gamma L \end{bmatrix} \tag{3.1}$$

where $\gamma = \sqrt{j\omega R'_{\text{ch}} C'_{\text{g}}}$ is the propagation constant, $Z_0 = R'_{\text{ch}}/\gamma$ is the characteristic transmission line impedance, L is the channel length, $R'_{\text{ch}} = R_{\text{ch}}/L$, $C'_{\text{g}} = C_{\text{g}}/L$, R_{ch} is the channel charging resistance, which is a result of non-instantaneous respond to the changes of the gate-source voltage, and C_{g} is the total gate capacitance. Under the assumptions mentioned above, the equivalent gate-source impedance Z_{gs} can be written using Eq. (3.1) as

$$Z_{\text{gs}} = \frac{\text{A}}{C} = R_{\text{ch}} \frac{\coth \gamma L}{\gamma L} \tag{3.2}$$

The first-order approximation of Z_{gs} obtained from series expansion of Eq. (3.2) yields the following result:

$$Z_{\text{gs}} = R_{\text{ch}} \frac{\coth \gamma L}{\gamma L} \cong \frac{R_{\text{ch}}}{\gamma L} \left(\frac{1}{\gamma L} + \frac{\gamma L}{3} \right) = \frac{R_{\text{ch}}}{3} + \frac{1}{j\omega C_{\text{g}}} \tag{3.3}$$

From Eq. (3.3) it follows that the MOSFET intrinsic gate-source circuit can be realized using a simple series circuit with the resistance

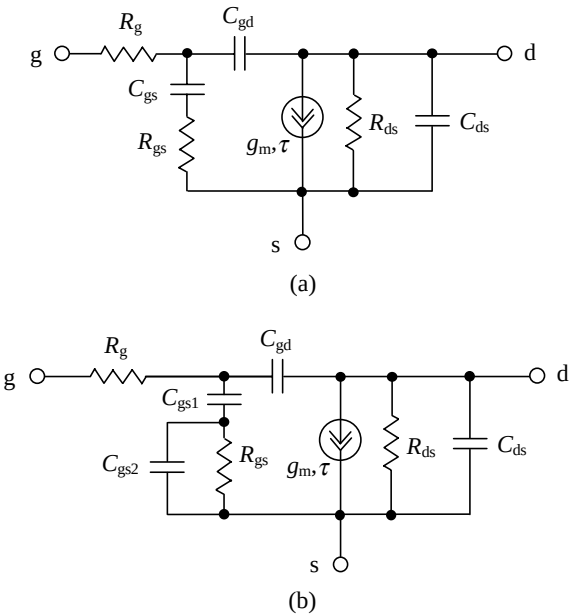


Figure 3.2 Intrinsic MOSFET equivalent circuit corresponding to (*a*) first- and (*b*) second-order channel approximation.

$R_{gs} = R_{ch}/3$ and the capacitance $C_{gs} = C_g$. The intrinsic transistor equivalent circuit corresponding to the first-order approximation is shown in Fig. 3.2(*a*).

The second-order approximation of Z_{gs} is also derived from a series expansion of Eq. (3.2) as

$$Z_{gs} = R_{ch}\frac{\coth \gamma L}{\gamma L} \cong \frac{R_{ch}}{\gamma L}\left[\frac{1}{\gamma L} + \frac{\gamma L}{3} - \frac{(\gamma L)^2}{45}\right] = \frac{R_{ch}}{3}\left(1 - \frac{j\omega C_g R_{ch}}{15}\right) + \frac{1}{j\omega C_g} \cong \frac{R_{ch}}{3} / \left(1 + j\omega \frac{R_{ch}}{3}\frac{C_g}{5}\right) + \frac{1}{j\omega C_g} \tag{3.4}$$

As a result, the second-order approximation of the device channel structure can be realized by series connection of the capacitance $C_{gs1} = C_g$ and the parallel RC circuit, which consists of the resistance $R_{gs} = R_{ch}/3$ and the capacitance $C_{gs2} = C_g/5$. The intrinsic transistor equivalent circuit corresponding to the second-order approximation is shown in Fig. 3.2(*b*).

For high power MOSFET devices whose channel width is significantly larger than their channel length, the distributed character of the total gate resistance $R_t = R_{sh}W/L$ across the width W (where R_{sh} is the sheet

resistance of the gate material) has to be taken into consideration. Silicon MOSFET can be decomposed into n devices, each with a width of W/n and a gate resistance of R_t/n. For $n \to \infty$, it will be viewed as array of the small transistors distributed along the gate of the device. Commonly, it is necessary to consider a two-dimensional power MOSFET distributed model because it contains a gate-distributed character along both the channel length and channel width. But because of the short channel size of MOSFETs, a distributed gate effect along the channel length can be taken into account in only the frequency range close to the transition frequency f_T and higher. When $\omega R_{gs} C_{gs} << 1$, an analysis of the distributed gate model along the channel width based on transmission line theory shows that all transistor Y-parameters should be modified by the term $\tanh(\gamma W)/\gamma W$ [6]. However, a linear series expansion of this term in the form of

$$\frac{\tanh(\gamma W)}{\gamma W} = 1 - j\omega C_g \frac{R_t}{3} \cong \frac{1}{1 + j\omega C_g \frac{R_t}{3}} \tag{3.5}$$

leads to only the additional use of a series lumped gate resistance $R_t/3$ that does not alter the structure of the transistor equivalent circuit. Consequently, the total gate resistance R_g can be divided in two series resistances as $R_g = R_{ge} + R_{gi}$, where R_{ge} is the extrinsic contact and ohmic gate electrode resistance and $R_{gi} = R_t/3$ is the intrinsic gate resistance due to the distributed gate structure of the power MOSFET.

The complete small-signal MOSFET equivalent circuit with the extrinsic parasitic elements is shown in Fig. 3.3. Here, L_g is the gate lead inductance, R_s, L_s are the source bulk and ohmic resistance and lead inductance, R_d, L_d are the drain bulk and ohmic resistance and lead inductance, and C_{gp}, C_{dp} are the gate and source pad capacitances, respectively.

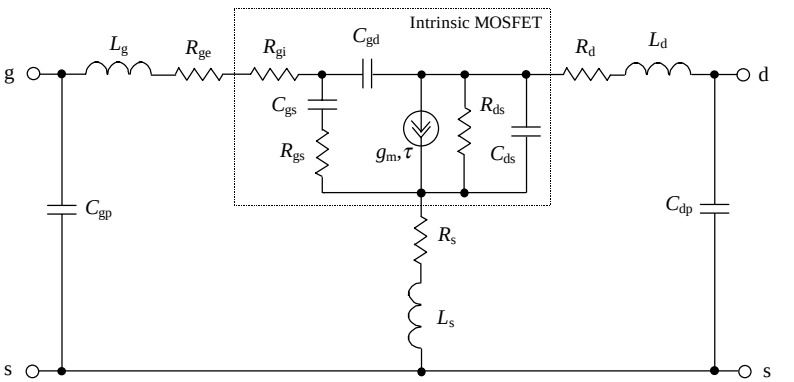


Figure 3.3 Nonlinear MOSFET equivalent circuit with extrinsic linear elements.

Determination of equivalent circuit elements

To characterize the transistor electrical properties, it is sufficient to use the grounded-source intrinsic Y-parameters. Their two-port admittance matrix is:

$$Y = \begin{bmatrix} \dfrac{j\omega C_{gs}}{1+j\omega\tau_g} + j\omega C_{gd} & -j\omega C_{gd} \\ \dfrac{g_m \exp(-j\omega\tau)}{1+j\omega\tau_g} - j\omega C_{gd} & G_{ds} + j\omega(C_{ds} + C_{gd}) \end{bmatrix} \tag{3.6}$$

where $G_{ds} = 1/R_{ds}$, $\tau_g = R_{gs}C_{gs}$, and τ is the effective channel carrier transit time. It is advisable to consider the intrinsic gate resistance R_{gi} as an external gate element. In this case, the MOSFET intrinsic Y-matrix is the same as for the MESFET or HEMT devices. Consequently, to determine the elements of the intrinsic MOSFET small-signal equivalent circuit, it is possible to use the same analytical approach, which allows the determination of its elements through the real and imaginary parts of the device intrinsic admittance Y-parameters.

For known extrinsic parasitic elements, the determination of the intrinsic Y-parameters from experimental data can be presented by the following procedure (see Fig. 3.4):

- Measurement of the S-parameters of the extrinsic device
- Transformation of the S-parameters to the admittance Y-parameters with subtraction of the parallel capacitances C_{gp} and C_{dp}
- Transformation of the admittance Y-parameters to the impedance Z-parameters with subtraction of series inductances L_g, L_s, L_d and resistances R_g, R_s, R_d
- Transformation of the impedance Z-parameters to the admittance Y-parameters of the intrinsic device two-port network.

The device extrinsic parasitic resistances and inductances can be directly determined from measurements performed at zero drain-source voltage. For known values of C_{gp} and C_{dp} and for the forward gate biasing condition (when the gate-source voltage is substantially larger than the pinch-off voltage) the device equivalent circuit can be presented, as shown in Fig. 3.5. Then, the extrinsic impedance Z-parameters are written as follows:

$$Z_{11} = R_s + R_g + j\left[\omega(L_s + L_g) - \frac{1}{\omega C_{gs}} \frac{1 + j\omega C_{gs}R_{gs}}{1 + \frac{C_{gd}}{C_{gs}}(1 + j\omega C_{gs}R_{gs})}\right] \tag{3.7}$$

$$Z_{12} = Z_{21} = R_s + j\omega L_s \tag{3.8}$$

$$Z_{22} = R_s + R_d + j\omega(L_s + L_d) \tag{3.9}$$

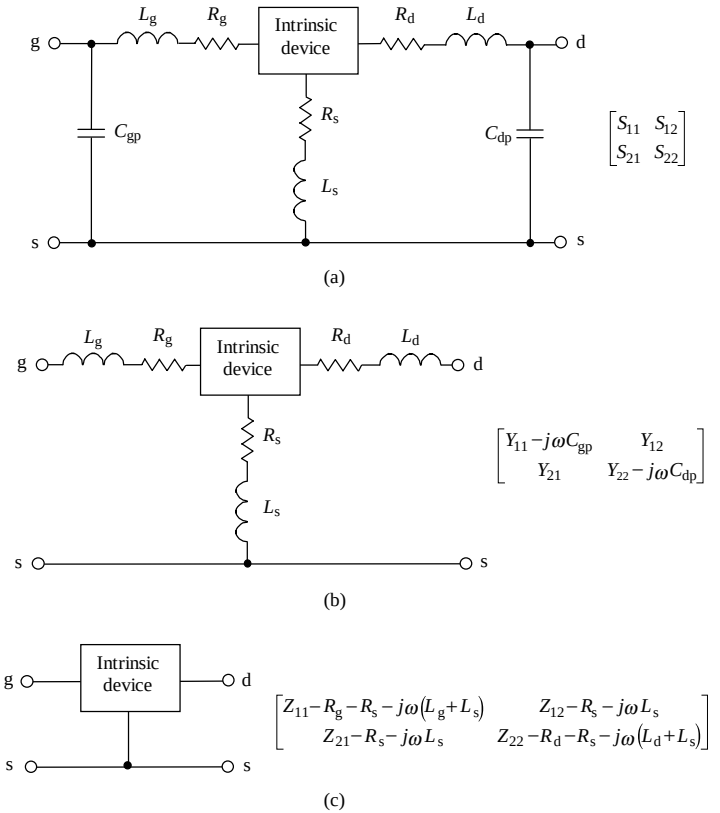


Figure 3.4 Method for extracting the device intrinsic Z-parameters.

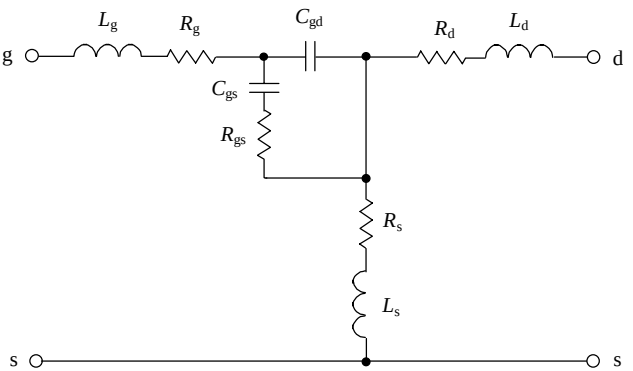


Figure 3.5 Device equivalent circuit corresponding to forward gate biasing condition.

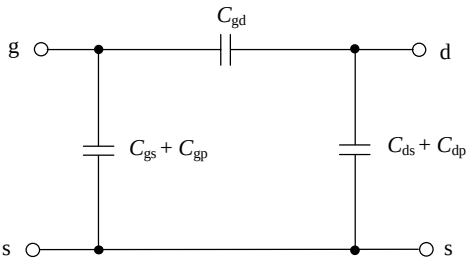


Figure 3.6 Device equivalent circuit corresponding to zero drain biasing condition.

As a result, when (1) the parasitic source inductance L_s is defined directly from measured $\mathrm{Im}Z_{12}$ and (2) the parasitic source resistance R_s is defined from measured $\mathrm{Re}Z_{12}$, then the parasitic drain inductance L_d and resistance R_d can be calculated from measured $\mathrm{Re}Z_{22}$ and $\mathrm{Im}Z_{22}$, respectively. The parasitic gate resistance R_g can be calculated directly from measured $\mathrm{Re}Z_{11}$ for a specified value of R_s.

Low frequency measurements allow the determination of the input, output, and feedback MOSFET capacitances. In this case, at zero drain bias and for the gate voltages lower than the pinch-off voltage V_p, the device small-signal equivalent circuit can be simplified to the one shown in Fig. 3.6. For low frequency measurements of less than a 100 MHz, when the extrinsic parasitic resistances and inductances have no influence on the device behavior, the imaginary parts of the Y-parameters can be written as

$$\mathrm{Im}Y_{11} = j\omega(C_{gs} + C_{gp} + C_{gd}) \tag{3.10}$$

$$\mathrm{Im}Y_{12} = \mathrm{Im}Y_{21} = -j\omega C_{gd} \tag{3.11}$$

$$\mathrm{Im}Y_{22} = j\omega(C_{ds} + C_{dp} + C_{gd}) \tag{3.12}$$

The parameters of the small-signal equivalent circuit can also be extracted using computer optimization. For example, the intrinsic device parameters are calculated analytically for each bias condition as the functions of the extrinsic parasitic elements, which are treated as global bias-independent data in the associated fitting process [7]. The measured and simulated real and imaginary parts of S-parameters in a wide frequency range are compared to minimize the error function

$$\varepsilon_{ij} = \frac{1}{4}\sum_{i,j=1}^{2}\left(\frac{1}{N}\sum_{n=1}^{N}\frac{|\mathrm{meas}S_{ijn} - \mathrm{sim}S_{ijn}|}{\mathrm{meas}S_{ijn}}\right)\cdot 100\% \tag{3.13}$$

where $\mathrm{meas}S_{ijn}$ are the measured S-parameter data, $\mathrm{sim}S_{ijn}$ are the simulated S-parameter data, N is the number of frequencies, and $i, j = 1, 2$. So, for the power lateral double-diffused MOSFET device with the gate length $L = 1.25$ μm and the gate width $W = 1.44$ mm in a frequency

range of 50 MHz up to 10 GHz, the maximum error does not exceed 2.5 percent. This indicates a good accuracy of the MOSFET small-signal equivalent circuit model presented in Fig. 3.3.

Nonlinear I-V models

An empirical approach to approximate the drain current source I_{ds} (V_{gs}, V_{ds}) of a JFET device is described in [8]. Instead of using separate equations for the triode and pinch-off regions, irrespective of the device geometry and material parameters, Eq. (3.14) with hyperbolic function was used:

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tanh\alpha \left|\frac{V_{ds}}{V_p - V_{gs}}\right| \tag{3.14}$$

where I_{dss} is the saturation drain current for $V_{gs} = 0$, α is the saturation voltage parameter, and V_p is the pinch-off voltage. As a result, good agreement was obtained between the predicted and experimental results, which shows a promising prospect for such a simple empirical model.

An empirical nonlinear model, which is single piece and continuously differentiable, developed for silicon LDMOS transistors is presented by [9]:

$$\begin{aligned} I_{ds} = {} & \beta V_{gst}^{VG\exp}(1 + \lambda V_{ds})\tanh\left(\frac{\alpha V_{ds}}{V_{gst}}\right)[1 + K_1 \exp(V_{BReff1})] \\ & + I_{ss}\exp\left(\frac{V_{ds} - V_{BR}}{V_T}\right) \end{aligned} \tag{3.15}$$

where

$$\begin{aligned} V_{gst} &= V_{st}\ln\left[1 + \exp\left(\frac{V_{gst2}}{V_{st}}\right)\right] \\ V_{gst2} &= V_{gst1} - \frac{1}{2}\left(V_{gst1} + \sqrt{(V_{gst1} - V_K)^2 + \Delta^2} - \sqrt{V_K^2 + \Delta^2}\right) \\ V_{gst1} &= V_{gs} - V_{th0} - \gamma V_{ds} \\ V_{BReff1} &= \frac{V_{ds} - V_{BReff}}{K_2} + M_3\frac{V_{ds}}{V_{BReff}} \\ V_{BReff} &= \frac{V_{BR}}{2}[1 + \tanh(M_1 - V_{gst}M_2)] \end{aligned}$$

λ = drain current slope parameter
β = transconductance parameter

V_{th0} = forward threshold voltage
V_{st} = subthreshold slope coefficient
V_T = temperature voltage
I_{ss} = forward diode leakage current
V_{BR} = breakdown voltage
K_1, K_2, M_1, M_2, and M_3 = breakdown parameters
V_K, $VGexp$, and Δ, γ = gate-source voltage parameters

A similar and sufficiently simple nonlinear MOSFET RF model to describe the device I-V characteristics using hyperbolic function is proposed in [10]:

$$I_{ds} = \beta_{eff} V_{gst}^{VG\,exp}(1 + \lambda V_{ds}) \tanh\left(\frac{\alpha V_{ds}}{V_{gst}^{SAT\,exp}}\right) \tag{3.16}$$

where

$$\beta_{eff} = \beta/\left(1 + \mu_{crit} V_{gst}^{GMexp}\right)$$
$$V_{gst} = V_{st} \ln\left[1 + \exp\left(\frac{V_{gst1}}{V_{st}}\right)\right]$$
$$V_{gst1} = V_{gs} - V_{th0} - \gamma V_{ds}$$

GMexp, *SATexp*, and μ_{crit} are the channel current parameters.

In many applications, it is necessary to take into consideration the MOSFET operation in the weak-inversion region when the gate-source voltage V_{gs} is smaller than the threshold voltage V_{th}. For example, to improve the conversion gain of a mixer or to reduce the intermodulation distortion of a class AB power amplifier (when device biasing is usually used at a low current level around the onset of the strong-inversion region from the weak-inversion region). The drain current in the weak-inversion region is dominated mainly by the diffusion component that increases exponentially with the gate voltage [11]. On the other hand, in the strong-inversion saturation region when the gate-source voltage is greater than the threshold voltage, the drain current is proportional to the square of $(V_{gs} - V_{th})$. To obtain continuous behavior from the weak-inversion region to the strong-inversion region for the drain current, and to achieve a compromise between accurate device modeling and ease of circuit analysis, we can use

$$I_{ds}(V_{gs}) = A\{\ln[1 + \exp(B(V_{gs} - V_{th}))]\}^2 \tag{3.17}$$

where A and B are the approximation parameters. The drain current is effectively proportional to the square of $(V_{gs} - V_{th})$ when V_{gs} is larger than V_{th} and exponentially decreases with the gate-source voltage when

V_{gs} is smaller than V_{th}. The approximation parameters A and B are defined from the following conditions:

$$I_{ds}|_{V_{gs}=V_{th}} = I_{th} \qquad \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{gs}=V_{th}} = S_{th} \tag{3.18}$$

where I_{th} is the threshold drain current, as shown in Fig. 3.7(a), S_{th} is a slope of the voltage-ampere transfer characteristic in the threshold point. Then,

$$A = \frac{I_{th}}{(\ln 2)^2} \qquad B = \frac{S_{th}}{I_{th}} \ln 2 \tag{3.19}$$

The transfer characteristic can be defined in terms of only two physical parameters I_{th} and S_{th}, which are easily defined from device measurements.

The EKV MOST model has been successfully applied to low-voltage and low-current analog circuit design and simulation, referring voltage

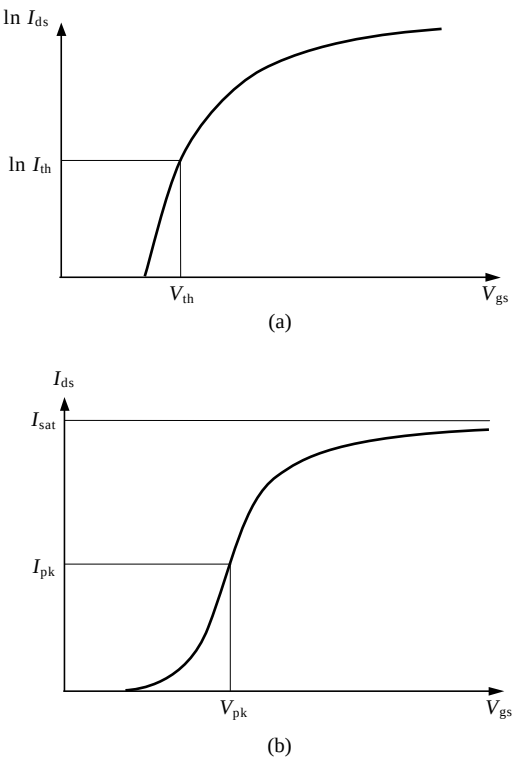


Figure 3.7 Drain current versus gate-source voltage.

V_g, V_d and V_s to the device local substrate [12]. In this case, the drain current I_d can be expressed as

$$I_d(V_g, V_s, V_d) = I_F(V_g, V_s) - I_R(V_g, V_d) \tag{3.20}$$

where $I_F(V_g, V_s)$ is the forward current component and $I_R(V_g, V_d)$ is the reverse current component. The current components I_F and I_R are

$$I_F(V_g, V_s) = I_s \left\{ \ln \left[1 + \exp \left(\frac{(V_g - V_{th0} - nV_s)}{2nV_T} \right) \right] \right\}^2 \tag{3.21}$$

$$I_R(V_g, V_d) = I_s \left\{ \ln \left[1 + \exp \left(\frac{(V_g - V_{th0} - nV_d)}{2nV_T} \right) \right] \right\}^2 \tag{3.22}$$

where $I_s = 2n\beta V_T^2$, β is the transfer parameter, V_T is the temperature voltage (26 mV at 300 K), V_{th0} is the gate-to-bulk threshold voltage defined with zero channel inversion charge, and n is the slope factor defined from the device physics.

The function to describe the I-V curves of the HEMT devices was used to link the linear and saturation regions by a suitable continuous analytical dependence [13]:

$$I_{ds}(V_{gs}, V_{ds}) = \left(I_{max}^{-1} + I_{gdo}^{-1} \right)^{-1} \tag{3.23}$$

where I_{gdo} is an exponential function of V_{gs} and V_{ds}, I_{max} is maximum channel current expressed as

$$I_{max}(V_{ds}) = I_{pk}(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \tag{3.24}$$

I_{pk} is the drain current, which corresponds to the maximum slope of the I_{ds}–V_{gs} characteristic, as shown in Fig. 3.7(*b*). The saturation voltage parameter α affects a slope of the I_{ds}–V_{ds} characteristics in the linear region, and parameter λ determines a slope of the same drain characteristics in the saturation region.

In view of the more sloping character of I_{ds}–V_{ds} characteristics, and taking into account two analytic preliminary premises [see Eqs. (3.17) and (3.23)], the entire drain volt-ampere characteristics of a MOSFET can be described as follows [14]:

$$I_{ds}(V_{gs}, V_{ds}) = I_o / \left[1 + \left(\frac{I_o}{I_{max}} \right)^n \right]^{\frac{1}{n}} \tag{3.25}$$

where

$$I_o = \frac{I_{th}}{(\ln 2)^2 (1 - \beta V_{gs})} \left\{ \ln \left[1 + \exp \left(\frac{S_{th} \ln 2}{I_{th}} (V_{gs} - V_{th}) \right) \right] \right\}^2$$

$$I_{max} = I_{sat}(1 + \lambda V_{ds}) \tanh(\alpha V_{ds})$$

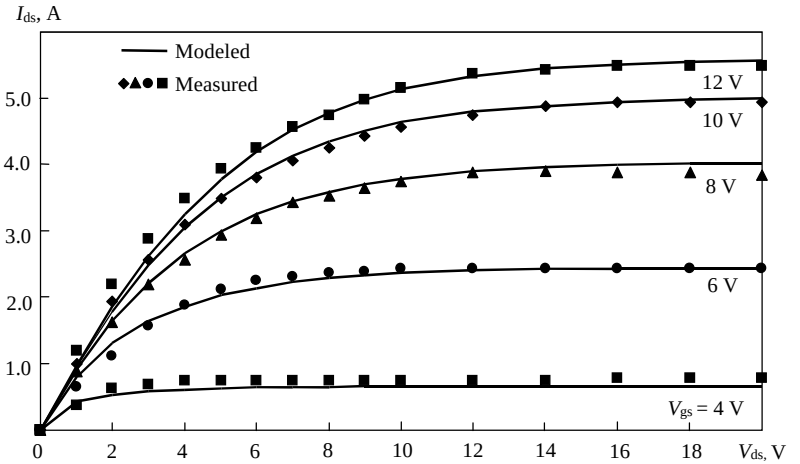


Figure 3.8 Measured and modeled I_{ds}-V_{ds} curves of high voltage LDMOSFET.

I_{sat} is the saturated drain current as shown in Fig. 3.7(*b*), $V_{th} = V_{tho} - \sigma V_{ds}$, β is the fitting parameter (which determines a slope of the transfer characteristics under the large values of V_{gs}), and σ is the parameter that expresses empirically the dependence of the threshold voltage on V_{ds}. Better accuracy can be achieved by using I_{sat} for I_{max} in Eq. (3.24) instead of I_{pk}.

To verify the new empirical *I*-*V* model, a high-power LDMOSFET with gate width $W = 4$ cm and gate length $L = 1.1$ μm, type LP801 from Polyfet RF Devices, was used. The theoretical and experimental output $I_{ds}(V_{ds})$ curves are presented in Fig. 3.8. To define a deviation between the measured and modeled simulated data and express the error in percentage, the following current mean-square relative error function was chosen:

$$\varepsilon_{sq} = \frac{1}{M}\sum_{m=1}^{M}\left[\frac{1}{N}\sum_{n=1}^{N}\left(\frac{\text{meas}I_{dsnm} - \text{sim}I_{dsnm}}{\text{meas}I_{dsnm}}\right)^2\right]\cdot 100\% \qquad (3.26)$$

where $\text{meas}I_{dsnm}$ are the measured drain current values, $\text{sim}I_{dsnm}$ are the simulated drain current values, N is the number of measured drain voltage bias points for the appropriate gate bias voltage V_{gs}, and M is the number of measured gate voltage bias points. The resulting current mean-square error of a family of the output I_{ds}–V_{ds} characteristics is 0.5 percent.

The values of the simulated model parameters are given in Table 3.1.

The theoretical approximation of $I_{ds}(V_{ds})$ curves is sufficient and accurate for high-power LDMOSFET and requires only six fitting parameters, four of which are easily determined by the experimental curves.

TABLE 3.1 Simulated *I-V* Model Parameters of High-Voltage LDMOSFET

Parameters	α, 1/V	β, 1/V	λ, 1/V	V_{th}, V	I_{th}, A	S_{th}, A/V	I_{sat}, A	n	σ
Values	0.15	0	0.0005	2.7	0.115	0.2	6.8	1.0	0

When comparing the measured and theoretical data of the transfer I_{ds}–V_{gs} characteristic, it is advisable to use the normalized difference function

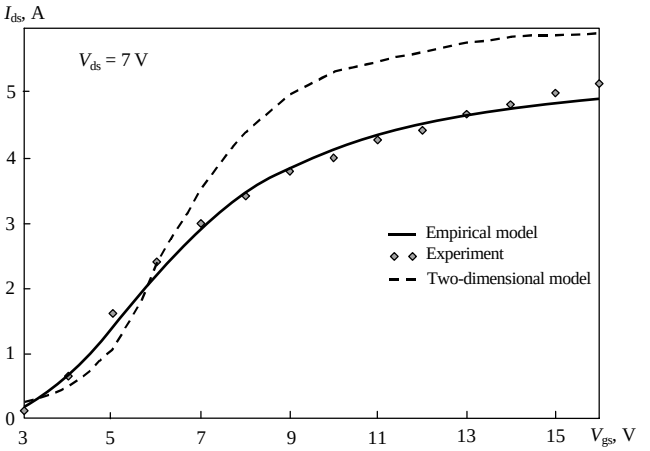
$$\Delta I_{ds} = \frac{\text{meas}I_{dsn} - \text{sim}I_{dsn}}{\text{meas}I_{dsn}} \cdot 100\% \tag{3.27}$$

Substantially better fitting to $I_{ds}(V_{gs})$ and $g_m(V_{gs})$ experimental curves is achieved compared with the results obtained from two-dimensional simulations [15] shown in Fig. 3.9. The deviation of the theoretical $I_{ds}(V_{gs})$ curve from the experimental curve is shown in Fig. 3.10. An empirical model allows the description of I_{ds} and g_m as a function of V_{gs} in a weak-inversion region as well as in the strong-inversion region of the LDMOSFET operation.

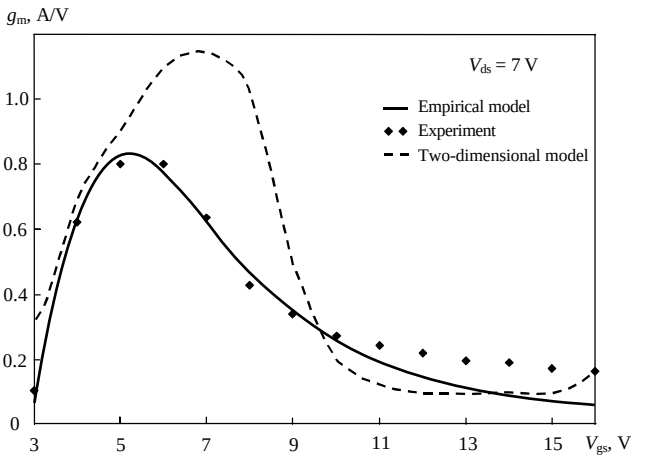
To verify that this model is applicable to low-voltage MOSFET devices, the appropriate low-voltage RF power MOSFET with a gate width of $W = 2$ mm was chosen [16]. In Fig. 3.11, the transistor theoretical and experimental drain current $I_{ds}(V_{ds})$ curves are presented. In this case, to improve the sensitivity of drain current I_{ds} under large values of V_{gs}, the term $(1 - \beta V_{gs})$ was introduced to the approximation function (3.25). The resulting current mean-square error of a family of the output I_{ds}–V_{ds} characteristics is 0.42 percent. The values of simulated I_{ds}–V_{ds} model parameters are presented in Table 3.2. The transfer I_{ds}–V_{gs} characteristics have been compared with the same characteristics calculated by means of the BSIM3v3 model developed for modeling of deep submicron device [15]. The results presented in Fig. 3.12 show a good agreement with the experimental curves (practically the same in the case of the BSIM3v3 approximation).

Nonlinear C-V models

The input capacitance C_{gs} influences the intermodulation (IMD) level when the frequency increases in the microwave region [17]. Moreover, the use of nonlinear capacitance C_{gs} significantly improves the accuracy of the simulated dc power consumption [18]. Calculating the gate-source capacitance C_{gs} or the gate-drain capacitance C_{gd} from the charges corresponding to only the accurate strong-inversion model results in a mathematically complicated expression [11]. Therefore, when using MOSFET modeling, the capacitances C_{gs} and C_{gd} can be modeled as the fixed capacitances measured at the quiescent bias voltage and the *p-n* junction diode capacitance model can be applied to the capacitance



(a)



(b)

Figure 3.9 Measured and modeled (*a*) I_{ds}-V_{gs} and (*b*) g_m (V_{gs}) curves of high voltage LDMOSFET.

C_{ds} [15]. In [19], only the drain-source capacitance C_{ds} and gate-drain capacitance C_{gd} are considered as the bias-dependent junction capacitances. With the increase in the drain bias voltage a depletion region is formed under the oxide in the lightly doped drain region. Therefore, the capacitance C_{gd} can be considered as a junction capacitance, which strongly depends on the drain-source bias voltage V_{ds}. According to the accurate charge model calculations in [11], C_{gd} has a strong dependence on V_{gs} only in the moderate-inversion region when $V_{gs} - V_{th} < 1$ V. In this region, the behavior of C_{gd} is similar to C_{gs} and can be evaluated

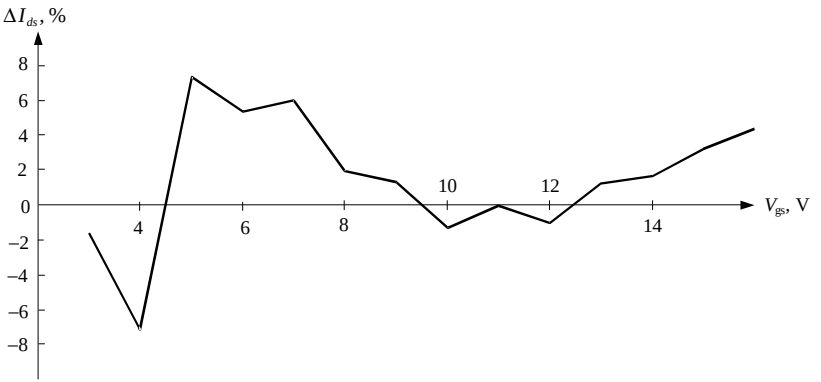


Figure 3.10 Deviation between theoretical and experimental I_{ds}-V_{gs} curves.

using the same hyperbolic tangent functions. However, for high-voltage LDMOSFET devices, since the dependence of C_{gd} on V_{gs} is quite small, it seems sufficient to limit the dependence to V_{ds} only. The capacitance C_{ds} varies due to the change in the depletion region, which is mainly determined by the value of V_{ds}.

The gate-source capacitance C_{gs} can be described as a function of the gate-source bias voltage. First, we consider an appropriate behavior for

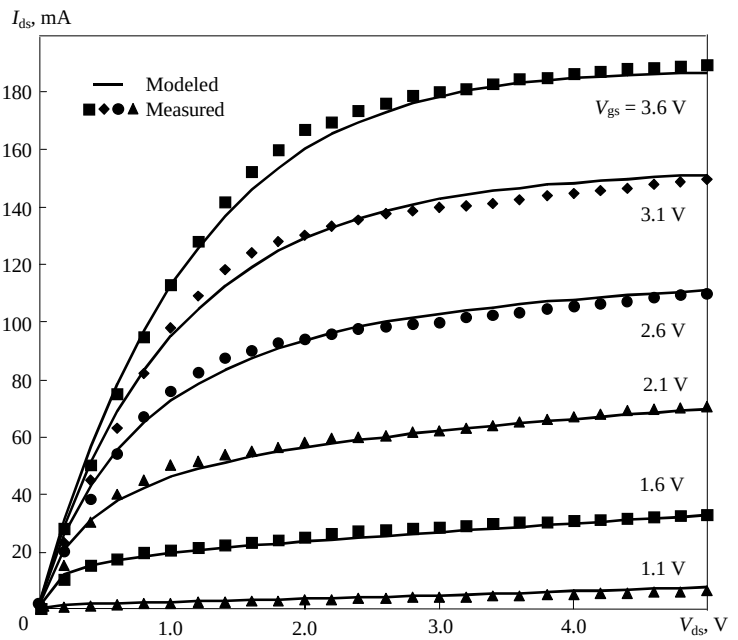


Figure 3.11 Measured and modeled I_{ds}-V_{ds} curves of low voltage MOSFET.

TABLE 3.2 Simulated *I-V* Model Parameters of Low-Voltage MOSFET

Parameters	α, 1/V	β, 1/V	λ, 1/V	V_{th}, V	I_{th}, mA	S_{th}, mA/V	I_{sat}, A	n	σ
Values	0.58	0.17	0	0.9	0.029	1.05	0.31	0.78	0.05

each of its main composite parts: the intrinsic gate-source capacitance C_{gsi} (including both the gate-source and the source-substrate charge fluctuations) and the gate-substrate capacitance C_{gbi}. The gate-source voltage dependence of these components is substantially different [11]. The intrinsic gate-substrate capacitance C_{gbi} is constant in the accumulation region (where it is equal to the total intrinsic oxide capacitance C_{ox}), slightly decreases in the weak-inversion region, significantly reduces in the moderate-inversion region and becomes practically constant in the strong-inversion or saturation region. The intrinsic gate-source capacitance C_{gsi} grows rapidly in the moderate inversion region and equals $2C_{ox}/3$ in the saturation region. The dependence of the total gate-source capacitance C_{gs} as a sum of its components C_{gsi} and C_{gbi} on V_{gs} is shown in Fig. 3.13.

A hyperbolic tangent function can be used for each of two parts of the dependence $C_{gs}(V_{gs})$ where the gate-source capacitance can be approximated by the following function:

$$C_{gs} = C_{gsmin} + C_s \left\{ 1 + \tanh\left[\frac{S}{C_s}(V_{gs} - V_s) \right] \right\} \tag{3.28}$$

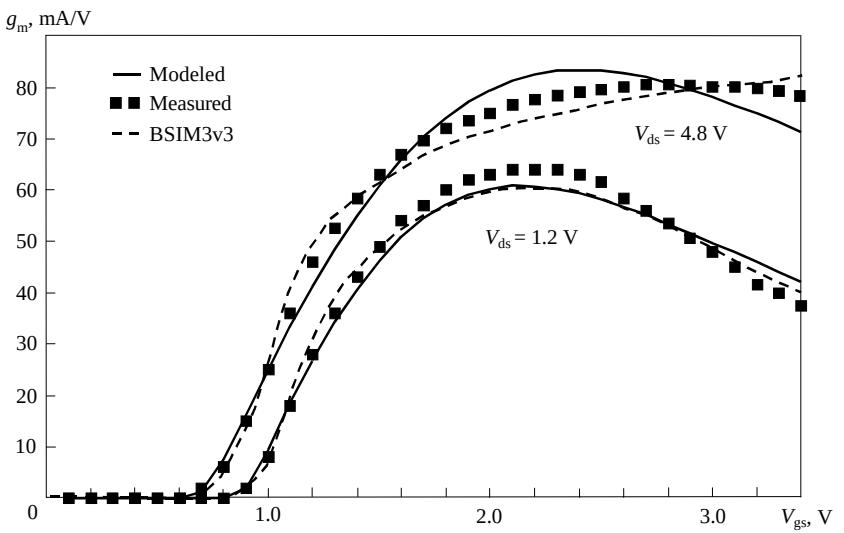


Figure 3.12 Meaured and modeled $g_m(V_{gs})$ curves of low voltage MOSFET.

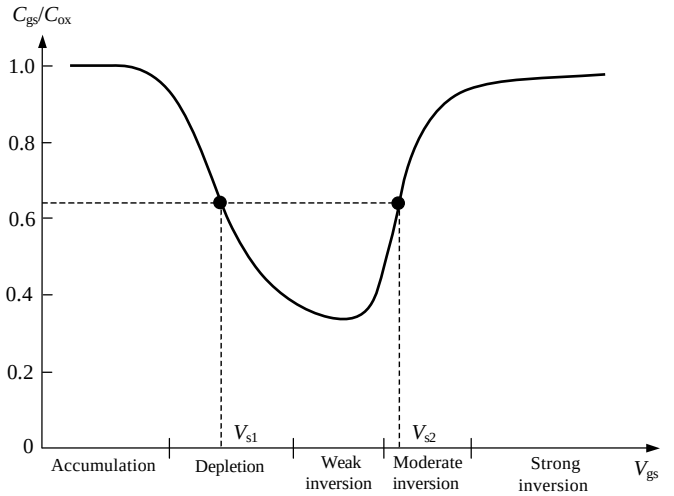


Figure 3.13 Gate-source capacitance versus gate-source voltage.

where $C_s = (C_{gsmax} - C_{gsmin})/2$, C_{gsmax} is maximum gate-source capacitance, C_{gsmin} is minimum gate-source capacitance, and $S = (S_1, S_2)$ is the slope of C_{gs} (V_{gs}) at each bend point $V_{gs} = V_s = (V_{s1}, V_{s2})$, as shown in Fig. 3.13,

$$S_1 = \frac{\partial C_{gs}}{\partial V_{gs}}\bigg|_{V_{gs}=V_{s1}} \qquad S_2 = \frac{\partial C_{gs}}{\partial V_{gs}}\bigg|_{V_{gs}=V_{s2}} \tag{3.29}$$

The total gate-source capacitance C_{gs} as a function of V_{gs} can be described by [14]

$$C_{gs} = C_{gsmax} - C_{gso}\left\{1 + \tanh\left[\frac{S_1}{C_s}(V_{gs} - V_{s1})\right]\right\}\left\{1 + \tanh\left[\frac{S_2}{C_s}(V_{gs} - V_{s2})\right]\right\} \tag{3.30}$$

where $C_{gsmax} = C_{ox}$, C_{gso} is the model fitting capacitance.

The approximation function for the gate-source capacitance as the dependence of V_{gs} can also be presented in the following form by using two components containing hyperbolic functions [9]:

$$C_{gs} = C_{gs1} + C_{gs2}\{1 + \tanh[C_{gs6}(V_{gs} + C_{gs3})]\} + C_{gs4}[1 - \tanh(C_{gs5}V_{gs})] \tag{3.31}$$

where C_{gs1}, C_{gs2}, C_{gs3}, C_{gs4}, C_{gs5}, and C_{gs6} are the approximation parameters.

If we consider the dependence of the gate-source capacitance on V_{ds} for submicron MOSFET devices, when C_{gs} slightly increases with the

increase of V_{ds}, the approximation equation used for the C_{gs} as a function of V_{gs} and V_{ds} can be as follows [20]:

$$C_{gs} = C_{gs0} + C_{gs1}\{A_s + B_s \tanh[C_s(V_{gs} - V_{th})]\} \times\{D_s + E_s[1 + \tanh(V_{gs} - V_{ds})] \tanh[F_s V_{ds} - G_s V_{gs}]\} \quad (3.32)$$

where C_{gs0} is a bias dependent capacitance, V_{th} is the threshold voltage, C_{gs1} is a scaling factor, and A_s, B_s, C_s, D_s, E_s, F_s, G_s are the model fitting parameters to match this equation to the measured data.

On the other hand, for high-voltage MOSFET devices, the dependencies of gate-drain capacitance C_{gd} and drain-source capacitance C_{ds} on V_{ds} can be accurately evaluated by means of the junction diode capacitance model as follows:

$$C_{gd(ds)} = C_{gdo(dso)} \left(\frac{\varphi + V_{dso}}{\varphi + V_{ds}} \right)^m \quad (3.33)$$

where $m (m_1$ for C_{gd} or m_2 for $C_{ds})$ is the junction sensitivity, φ is the contact potential—a value that depends on a doping profile ($m = 1/3$ for the linearly graded junction, $m = 1/2$ for the abrupt junction, $m > 1/2$ for the hyperabrupt junction)—and C_{gdo} and C_{dso} are the junction capacitances under dc drain-source bias of V_{dso}. For practical profiles of the junction, which are neither exactly abrupt nor exactly linearly graded, one often chooses the parameters m and φ to obtain the best match between the theoretical model and the measurements.

The results of the approximation of C_{ds} and C_{gd} as the junction capacitances for high-power LDMOSFET, type LP801, are given in Figs. 3.14

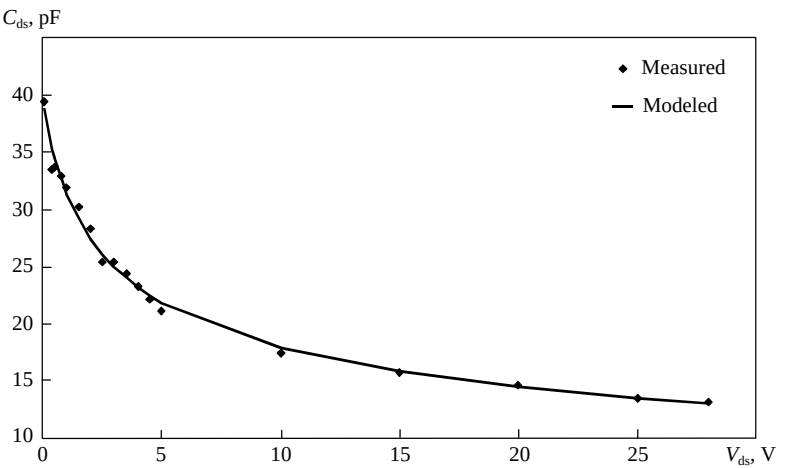


Figure 3.14 Measured and modeled $C_{ds}(V_{ds})$ dependencies of high voltage LDMOSFET.

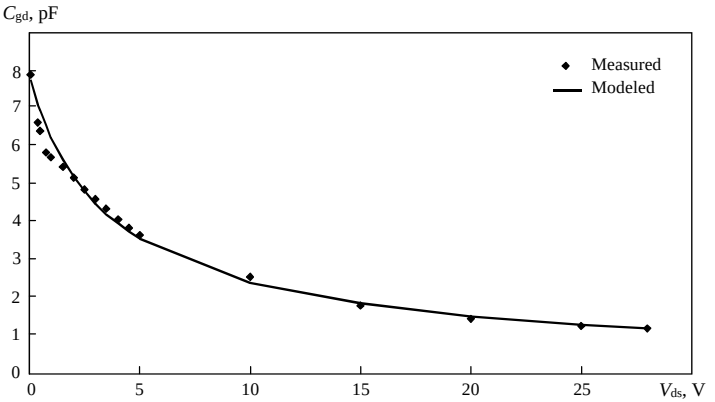


Figure 3.15 Simulated *C-V* junction model parameters.

and 3.15. The fitting parameters of the approximation curves $C_{gd}(V_{ds})$ and $C_{ds}(V_{ds})$ are presented in Table 3.3. The linear deviation of the theoretical dependence $C_{gd}(V_{ds})$ from the experimental one calculated by means of the normalized difference function is presented in Fig. 3.16.

The resulting drain-source capacitance average normalized difference error according to

$$\varepsilon_{Cds} = \frac{1}{N}\sum_{n=1}^{N}\frac{|\text{meas}C_{dsn} - \text{sim}C_{dsn}|}{\text{meas}C_{dsn}} \cdot 100\% \tag{3.34}$$

(where $\text{meas}C_{dsn}$ are the measured capacitance values, $\text{sim}C_{dsn}$ are the simulated capacitance values, and N is the number of measured voltage bias points) is only 4.3 percent.

For submicron MOSFET devices, to take into account the dependence of C_{gd} on both V_{gs} and V_{ds}, the approximation equation used for the C_{gd} is [20]:

$$C_{gd} = C_{gd0} + C_{gd1}\{A_d + B_d \tanh[C_d(D_d V_{gs} - V_{ds}) - V_{th}]\} \tag{3.35}$$

where C_{gd0} is a bias dependent capacitance, V_{th} is the threshold voltage, C_{gd1} is a scaling factor, while A_d, B_d, C_d, and D_d are the model fitting parameters.

TABLE 3.3 Simulated *C-V* Junction Model Parameters

Capacitance	$C_{gd(ds)o}$, pF	m	φ, V
C_{gd}	7.88	0.8	2.94
C_{ds}	39.42	39.42	1.0

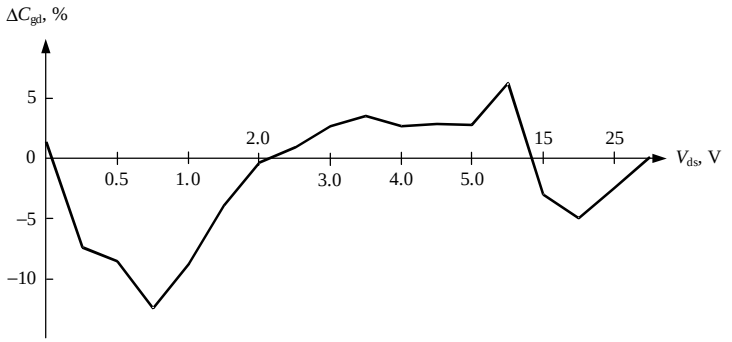


Figure 3.16 Deviation between theoretical and experimental C_{gd}-V_{ds} curves.

Charge conservation

To describe small-signal and large-signal device models, it is necessary to satisfy the charge conservation condition. For the three-terminal MOSFET device, the matrix equation for small-signal charging circuit in the frequency domain representation is given by [11]

$$\begin{bmatrix} I_g \\ I_d \\ I_s \end{bmatrix} = j\omega \begin{bmatrix} C_{gg} & -C_{gd} & -C_{gs} \\ -C_{dg} & C_{dd} & -C_{ds} \\ -C_{sg} & -C_{sd} & C_{ss} \end{bmatrix} \begin{bmatrix} V_g \\ V_d \\ V_s \end{bmatrix} \tag{3.36}$$

where I_g, I_d, I_s are the terminal current amplitudes, V_g, V_d, V_s are the terminal voltage amplitudes, and the capacitance between any two device terminals (k, l) is described as $C_{kl} = \partial Q_k / \partial V_l$. To transform a three-terminal device into a two-port network with a common source terminal, the current and voltage terminal conditions of $I_g = I_{gs}$, $I_d = I_{ds}$, $I_s = -(I_{gs} + I_{ds})$, $V_g - V_s = V_{gs}$, $V_d - V_s = V_{ds}$ should be taken into account. In addition, for three-terminal devices the following relations between terminal capacitances are valid:

$$\begin{aligned} C_{gg} &= C_{gd} + C_{gs} = C_{dg} + C_{sg} \\ C_{dd} &= C_{dg} + C_{ds} = C_{gd} + C_{sd} \\ C_{ss} &= C_{sg} + C_{sd} = C_{gs} + C_{ds} \end{aligned} \tag{3.37}$$

The admittance Y_c-matrix for such a capacitive two-port network is

$$Y_c = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ -j\omega(C_{gd} + C_m) & j\omega(C_{ds} + C_m + C_{gd}) \end{bmatrix} \tag{3.38}$$

where $C_m = C_{dg} - C_{gd}$ is the transcapacitance, C_{gd} represents the effect of the drain on the gate, and C_{dg} represents the effect of the gate on the drain, and these effects are different [11]. Analogous to the I-V

characteristics, there is no reason to expect that the effect of the drain voltage on the gate current, which is zero assuming no leakage, is the same as the effect of the gate voltage on the drain current, which is significantly large.

Therefore, for power MOSFET devices, because the transcapacitance C_m is substantially less than C_{gs} it can be translated to an additional delay time τ_c in a frequency range up to f_T by combining with the transconductance g_m according to

$$\begin{aligned} g_m - j\omega C_m &= g_m \sqrt{1 + \left(\frac{\omega}{\omega_T}\frac{C_m}{C_{gs}}\right)^2} \exp\left[-j \tan^{-1}\left(\frac{\omega}{\omega_T}\frac{C_m}{C_{gs}}\right)\right] \\ &\cong g_m \exp(-j\omega\tau_c) \end{aligned} \tag{3.39}$$

where $\tau_c = C_m/\omega_T C_{gs}$. To satisfy a charge conservation condition, the total delay time τ presented in the MOSFET equivalent circuit in Fig. 3.3 should contain delay time due to both the ideal transit time and the transcapacitance. The transcapacitance C_m can be easily added to the drain-source capacitance C_{ds} under the parameter extraction procedure.

Gate-source resistance

The gate-source resistance R_{gs} is determined by the effect of the channel inertia in responding to rapid changes of the time-varying gate-source voltage, and varies in such a manner that the charging time $\tau_g = R_{gs}C_{gs}$ remains approximately constant. Thus, the increase of R_{gs} in the velocity saturation region, when the channel conductivity decreases, is partially compensated by the decrease of C_{gs} due to nonuniform channel charge distribution [21]. The effect of R_{gs} becomes significant at higher frequencies close to the transition frequency f_T of the MOSFET and cannot be taken into consideration when designing RF circuits that operate below 2 GHz, as used for commercial wireless applications [16, 22]. For example, for the MOSFET with the depletion region doping concentration value $N_A = 1700\ \mu m^{-3}$, the phase of the small-signal transconductance g_m near f_T reaches the value of only –15° [11].

Temperature dependence

Silicon MOSFET devices are very sensitive to the operation temperature T and their characteristics are strongly temperature-dependent [11]. The main parameters responsible for this are the effective carrier mobility μ and the threshold voltage V_{th}, resulting in the increase of the drain current through $V_{th}(T)$ and the decrease of the drain current through $\mu(T)$ with temperature. Increasing temperature decreases the slope of the $I_{ds}(V_{gs})$ curves. A value of V_{gs} can be found at which the drain

current becomes practically temperature-independent over a large temperature range. The variation of V_{th} with temperature in a wide range from -50°C up to 200°C represents a nonlinear function, which is slowly decreased with temperature [15], and can be approximated by

$$V_{th}(T) = V_{th}(T_{nom}) + V_{T1}\Delta T + V_{T2}\Delta T^2 \tag{3.40}$$

where $\Delta T = T - T_{nom}$, $T_{nom} = 300$ K (27°C), and V_{T1} and V_{T2} are the linear and quadratic temperature coefficients for threshold voltage.

The variation of μ with temperature can be taken into account by introducing the appropriate temperature variation of I_{sat} in Eq. (3.25). The temperature variation of I_{sat} represents an almost straight line [15], which decreases with temperature. The dependence of $I_{sat}(T)$ on temperature can be approximated by the linear function

$$I_{sat}(T) = I_{sat}(T_{nom}) + I_T\Delta T \tag{3.41}$$

where I_T is the linear temperature coefficient for saturation current.

The temperature dependencies of the MOSFET capacitances and series resistances can be described by the following linear equations [5, 23]:

$$C(T) = C(T_{nom}) + C_T\Delta T \tag{3.42}$$

$$R(T) = R(T_{nom}) + R_T\Delta T \tag{3.43}$$

where $C = (C_{gs}, C_{ds}, C_{gd})$, $R = (R_g, R_s, R_d)$, and R_T and C_T are the linear temperature coefficients for the capacitances and resistances, respectively.

Figure 3.17 shows the modeled temperature dependencies of $V_{th}(T)$ and $g_m(T)$ for high-power LDMOSFET LP801. The results obtained by using the simple approximation Eqs. (3.40) and (3.41) with the values of $V_{T1} = -2$ mV/°C, $V_{T2} = -8.55$ μV/(°C)^2 and $I_T = -4.5$ mA/°C show a good prediction of the I–V characteristics in a wide temperature range.

At high values of V_{gs} and V_{ds} under dc measurement, the slope of I_{ds}-V_{ds} curves can be negative, which occurs due to the self-heating effect for a highly dissipated power region. For the drain current model in Eq. (3.16), this effect can be taken into account by adding a linear component that describes the temperature dependence [10]:

$$\beta(T) = \beta(T_{nom}) + \beta_T\Delta T_j' \tag{3.44}$$

$$\gamma(T) = \gamma(T_{nom}) + \gamma_T\Delta T_j' \tag{3.45}$$

where $\Delta T_j' = R_{th}P_{dis} + \Delta T$, R_{th}(°C/W) is thermal resistance, P_{dis}(W) is dc power consumption in watts caused by dc biasing, and β_T, γ_T are the linear temperature coefficients with negative values.

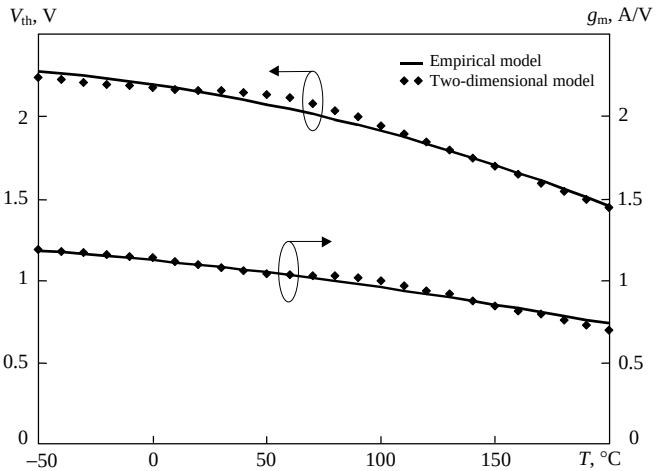


Figure 3.17 Modeled temperature dependencies of V_{th} and g_m.

Another way of taking into account the effect of the negative conductance at high biasing is to write the nonlinear $I - V$ model as follows:

$$I_{ds}(T, p_T) = \frac{I_{ds}(T)}{1 + p_T V_d I_{ds}(T)} \tag{3.46}$$

where the drain current source $I_{ds}(T)$ is presented in Eq. (3.25), $V_d = V_{ds}/\sqrt{1 + (\omega\tau_{th})^2}$, p_T is self-heating temperature coefficient, V_{ds} is the drain-source supply voltage, $\tau_{th} = R_{th}C_{th}$ is the thermal time constant, R_{th} is the thermal resistance, C_{th} is the thermal capacitance. A thermal equivalent circuit can be added to the large-signal MOSFET model as a parallel $R_{th}C_{th}$ circuit as it is presented in [9]. The thermal resistance R_{th} can be extracted from the temperature measurement of the dc characteristics. Since the slope of the dc measured $I_{ds}(V_{ds})$ curves changes its sign from positive to negative, the temperature coefficient p_T can be evaluated using the following condition:

$$\frac{dI_{ds}(T, p_T)}{dV_{ds}} = 0 \tag{3.47}$$

As a result,

$$p_T = \frac{1}{I_{ds}^2(T)} \frac{dI_{ds}(T)}{dV_{ds}} \tag{3.48}$$

where $I_{ds}(V_{ds})$ curves are defined by measurement of the pulsed $I_{ds}(V_{ds})$ curves at ambient temperature T, and a value of $I_{ds}(T)$ is fixed the same as for zero slope of $I_{ds}(T, p_T)$.

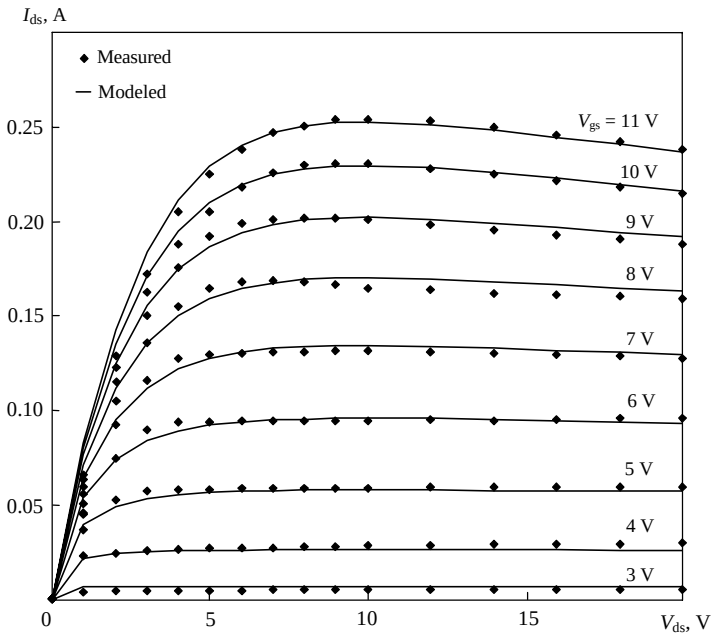


Figure 3.18 Measured and modeled I_{ds}-V_{ds} curves of low-voltage LDMOSFET.

The thermal time constant τ_{th} can be extracted by comparing pulsed $I_{ds}(V_{ds})$ curves calculated under different pulse width and duty factors. A plot of I_{ds} as a function of pulse width under the fixed gate-source and drain-source biasing voltages gives an appropriate value of τ_{th}.

Figure 3.18 shows the comparison between the measured (dc measurement) and modeled I_{ds}–V_{ds} curves for a 12.5 V LDMOSFET cell with gate geometry of $L = 1.25$ μm and $W = 1.44$ mm. The effect of self heating for the model parameters $p_T = 0.035$ 1/AV, $\alpha = 0.2$ 1/V, $\beta = \sigma = 0$, $S_{th} = 37$ mA/V, $I_{th} = 1.5$ mA, $V_{th} = 2.25$ V, $I_{sat} = 0.48$ A, $n = 1$, and $\lambda = 0.0005$ 1/V is described by Eq. (3.46).

GaAs MESFETs and HEMTs

Small-signal equivalent circuit

The small-signal equivalent circuit shown in Fig. 3.19 proves to be an adequate representation for MESFETs and HEMTs in a frequency range up at least to 25 GHz. Here, the extrinsic elements R_g, L_g, R_d, L_d, R_s, and L_s are the bulk and ohmic resistances and lead inductances associated with the gate, drain and source, C_{gp} and C_{dp} are the gate and source pad capacitances, respectively. Capacitance C_{dsd} and resistance R_{dsd}

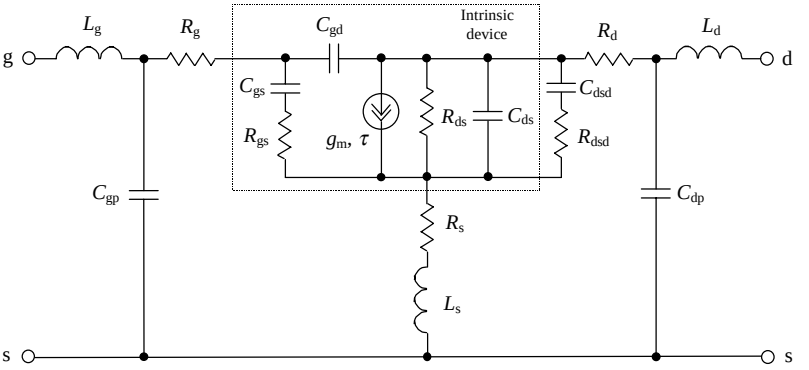


Figure 3.19 Small-signal equivalent circuit of field-effect transistor.

model the dispersion of the MESFET or HEMT I-V characteristics due to the trapping effect in the device channel, which leads to discrepancies between dc measurements and S-parameter measurements at high frequencies [24–26]. The intrinsic model is described by the channel charging resistance R_{gs}, which represents the resistive path for the charging of the gate-source capacitance C_{gs}, the feedback gate-drain capacitance C_{gd}, the output conductance $G_{ds} = 1/R_{ds}$, the drain-source capacitance C_{ds} and the transconductance g_m. The gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} represent the charge depletion region and are nonlinear functions. The influence of the drain-source capacitance C_{ds} on the device behavior is insignificant and its value is practically bias independent. To model the transit time of electrons along the channel, transconductance g_m usually includes the time constant τ.

To describe small-signal and large-signal device models, it is necessary to satisfy the charge conservation condition. The models for the device gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} should be derived from the charge model. There are commonly four partial derivatives of the two device terminal charges—the gate charge Q_g and the drain charge Q_d with regard to V_{gs} and V_{ds} respectively—which appropriately represent totally four capacitances (see Fig. 3.20(a)). However, the intrinsic small-signal equivalent circuit contains only two capacitances. Consequently, in this case, they can be defined as [25]

$$C_{gs} = \frac{\partial(Q_g + Q_d)}{\partial V_{gs}} \qquad C_{gd} = \frac{\partial(Q_g + Q_d)}{\partial V_{gd}} \tag{3.49}$$

The admittance Y_c-matrix for such a capacitive two-port network in Fig. 3.20(a) is

$$Y_c = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ -j\omega(C_{gs} - C_m) & j\omega C_{gd} \end{bmatrix} \tag{3.50}$$

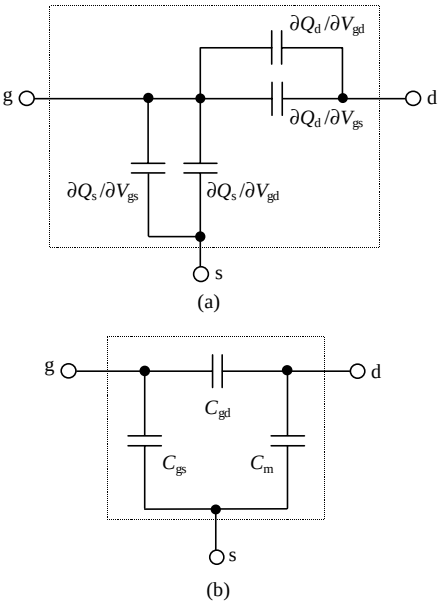


Figure 3.20 Capacitance equivalent circuits consistent with charge conservation.

where C_m is an additional transcapacitance, which is determined by

$$C_m = \frac{\partial Q_g}{\partial V_{gd}} - \frac{\partial Q_d}{\partial V_{gs}} \tag{3.51}$$

Adding the transcapacitance C_m results in the capacitance equivalent circuit consistent with the charge conservation condition, as shown in Fig. 3.20(b). Given that for MESFET devices the transcapacitance C_m is substantially less than C_{gs}, in a frequency range up to $\omega \leq \omega_T$, it can be translated to an additional delay time τ_c by combining with the transconductance g_m according to $g_m - j\omega C_m \cong g_m \exp(-j\omega\tau_c)$, where $\tau_c = C_m/\omega_T C_{gs}$.

Determination of equivalent circuit elements

To characterize the device electrical properties, we use the admittance Y-parameters expressed through the intrinsic small-signal equivalent circuit as

$$Y_{11} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_{gs}} + j\omega C_{gd} \tag{3.52}$$

$$Y_{12} = -j\omega C_{gd} \tag{3.53}$$

$$Y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + j\omega C_{gs} R_{gs}} + j\omega C_{gd} \tag{3.54}$$

$$Y_{22} = \frac{1}{R_{ds}} + j\omega(C_{ds} + C_{gd}) \tag{3.55}$$

Dividing these equations into their real and imaginary parts, the elements of the small-signal equivalent circuit can be determined as follows [27]:

$$C_{\mathrm{gd}} = -\frac{\mathrm{Im}Y_{12}}{\omega} \tag{3.56}$$

$$C_{\mathrm{gs}} = -\frac{\mathrm{Im}Y_{11} - \omega C_{\mathrm{gd}}}{\omega}\left[1 + \left(\frac{\mathrm{Re}Y_{11}}{\mathrm{Im}Y_{11} - \omega C_{\mathrm{gd}}}\right)^2\right] \tag{3.57}$$

$$R_{\mathrm{gs}} = \frac{\mathrm{Re}Y_{11}}{(\mathrm{Im}Y_{11} - \omega C_{\mathrm{gd}})^2 + (\mathrm{Re}Y_{11})^2} \tag{3.58}$$

$$g_{\mathrm{m}} = \sqrt{(\mathrm{Re}Y_{21})^2 + (\mathrm{Im}Y_{21} + \omega C_{\mathrm{gd}})^2} \cdot \sqrt{1 + (\omega C_{\mathrm{gs}} R_{\mathrm{gs}})^2} \tag{3.59}$$

$$\tau = \frac{1}{\omega}\sin^{-1}\left(\frac{-\omega C_{\mathrm{gd}} - \mathrm{Im}Y_{21} - \omega C_{\mathrm{gs}} R_{\mathrm{gs}} \mathrm{Re}Y_{21}}{g_{\mathrm{m}}}\right) \tag{3.60}$$

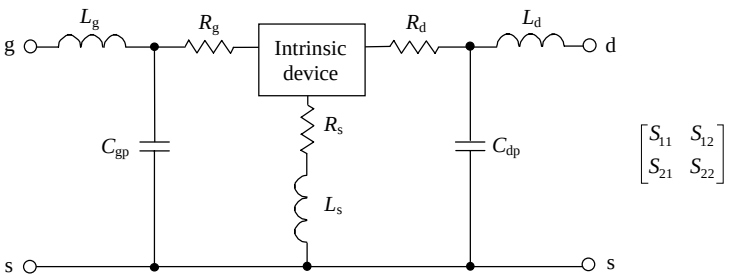
$$C_{\mathrm{ds}} = \frac{\mathrm{Im}Y_{22} - \omega C_{\mathrm{gd}}}{\omega} \tag{3.61}$$

$$R_{\mathrm{ds}} = \frac{1}{\mathrm{Re}Y_{22}} \tag{3.62}$$

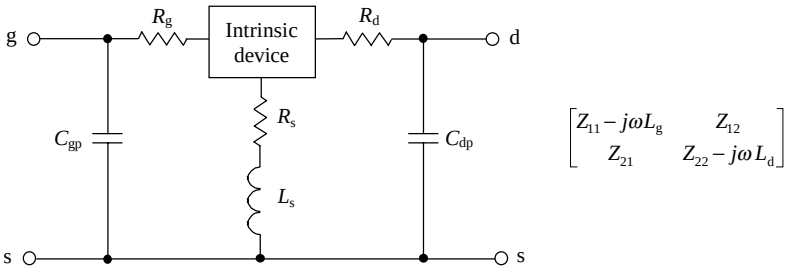
Equations (3.56) to (3.62) are valid for the entire frequency range and for the drain voltages of $V_{\mathrm{ds}} > 0$ V. If we suppose that all extrinsic parasitic elements are known, the only problem is to determine the admittance Y-parameters of the intrinsic two-port network from experimental data. Consecutive stages shown in Fig. 3.21 can represent such a determination procedure [28]:

- Measurement of the S-parameters of the extrinsic device
- Transformation of the S-parameters to the impedance Z-parameters with subtraction of the series inductances L_{g} and L_{d}
- Transformation of the impedance Z-parameters to the admittance Y-parameters with subtraction of the parallel capacitances C_{gp} and C_{dp}
- Transformation of the admittance Y-parameters to the impedance Z-parameters with subtraction of series resistances R_{g}, R_{s}, R_{d}, and inductance L_{s}
- Transformation of the impedance Z-parameters to the admittance Y-parameters of the intrinsic device two-port network.

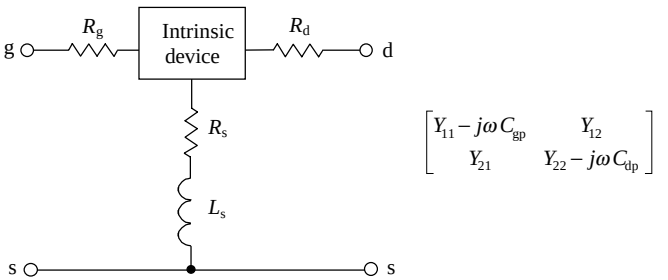
The device extrinsic parasitic elements can be directly determined from measurements performed at $V_{\mathrm{ds}} = 0$. Figure 3.22 presents the distributed RC channel network under the device gate for zero drain



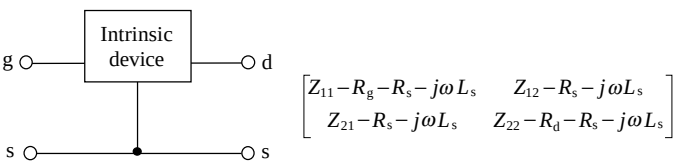
(a)



(b)



(c)



(d)

Figure 3.21 Method for extracting device intrinsic Z-parameters.

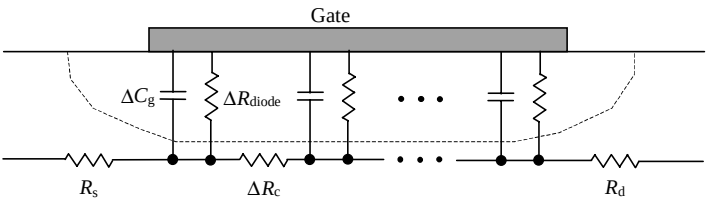


Figure 3.22 Distributed *RC* channel network schematic under device gate.

biasing condition, where ΔC_g is the distributed gate capacitance, ΔR_{diode} is the distributed Schottky diode resistance, and ΔR_c is the distributed channel resistance. For any gate biasing conditions, taking into account the negligible influence of C_{gp} and C_{dp}, the extrinsic impedance Z-parameters are

$$Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} + j\omega(L_s + L_g) \tag{3.63}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + j\omega L_s \tag{3.64}$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d) \tag{3.65}$$

where R_c = total channel resistance under the gate
nkT/qI_g = differential resistance of the Schottky diode
n = ideality factor
k = Boltzmann constant
T = Kelvin temperature
q = electron charge
I_g = dc gate current

As a result, if the parasitic inductance L_s can be defined directly from measured $\mathrm{Im}Z_{12}$, the parasitic inductances L_g and L_d are calculated from measured $\mathrm{Im}Z_{11}$ and $\mathrm{Im}Z_{22}$, respectively. The resistance R_c is the channel technological parameter, which is usually known. The measured real parts of the Z-parameters yield the values of R_s, R_g, and R_d.

At zero drain bias, and for the gate voltages lower than the pinch-off voltage V_p, the small-signal equivalent circuit can be simplified to the one shown in Fig. 3.23. Here, the capacitance C_b represents the fringing capacitance due to the depleted layer extension at each side of the gate. For low-frequency measurements usually up to a few gigahertz, when the extrinsic parasitic resistances and inductances have no influence on the device behavior, the imaginary parts of the Y-parameters can be written as

$$\mathrm{Im}Y_{11} = j\omega(C_{gp} + 2C_b) \tag{3.66}$$

$$\mathrm{Im}Y_{12} = \mathrm{Im}Y_{21} = -j\omega C_b \tag{3.67}$$

$$\mathrm{Im}Y_{22} = j\omega(C_b + C_{dp}) \tag{3.68}$$

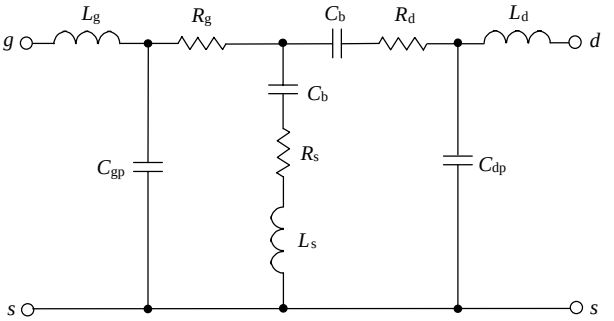


Figure 3.23 Small-signal FET circuit at zero drain bias voltage.

Curtice quadratic nonlinear model [29]

A simple nonlinear intrinsic large-signal model for GaAs MESFET device for use in the design of GaAs integrated circuits is shown in Fig. 3.24. It consists of a voltage-controlled source $I_{ds}(V_{gs}, V_{ds})$, the gate-source capacitance $C_{gs}(V_{gs})$, and a clamping diode between gate and source. The gate-drain capacitance C_{gd} is assumed to be constant.

The following analytical function is used to describe the current source:

$$I_{ds} = \beta(V_{gs} - V_p)^2(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \tag{3.69}$$

where β is the transconductance parameter determined from experimental data, V_p is the pinch-off voltage, and λ is the slope of the drain characteristic in the saturated region. Due to the finite value of maximum charge velocity of about 10^7 cm/s during transient operation, a change in gate voltage does not cause an instantaneous change in drain current. For example, it takes the order of 10 ps for a change in the drain current after the gate voltage is changed in a 1 μm gate length MESFET. Consequently, the most important result of this effect is a time delay between gate-source voltage and drain current. Therefore, the current source, given by Eq. (3.69) as $I_{ds}[V_{gs}(t), V_{ds}(t)]$, should be altered to be $V_{gs} = I_{ds}[V_{gs}(t - \tau), V_{ds}(t)]$, where τ is equal to the transit time under the gate.

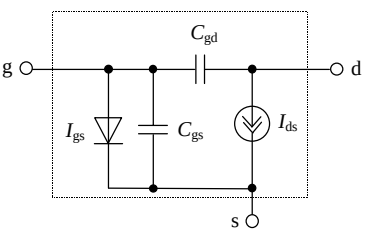


Figure 3.24 Curtice quadratic nonlinear intrinsic model.

The gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} can be treated as voltage-dependent Schottky barrier diode capacitances. For a negative gate-source voltage and small drain-source voltage, these capacitances are practically equal. But, when the drain-source voltage is increased beyond the current saturation point, the gate-drain capacitance C_{gd} is much more heavily back-biased than the gate-source capacitance C_{gs}. Therefore, the gate-source capacitance C_{gs} is significantly more important, and usually dominates the input impedance of the MESFET device. In this case, an analytical expression to approximate the gate-source capacitance C_{gs} is

$$C_{gs} = C_{gs0} / \left(1 - \frac{V_{gs}}{V_{gsi}}\right)^{0.5} \tag{3.70}$$

where C_{gs0} is the gate-source capacitance for $V_{gs} = 0$ and V_{gsi} is the built-in gate voltage. When V_{gs} approaches V_{gsi}, the denominator in Eq. (3.70) must not be allowed to approach zero, since C_{gs} will continue to increase as the depletion width reduces, so that a forward bias condition occurs, and diffusion gate-source capacitance becomes of great importance. The built-in voltage V_{gsi} should be equal to the built-in voltage of the Schottky barrier junction plus some part of the voltage drop along the channel under the gate.

Curtice-Ettenberg cubic nonlinear model [30]

The nonlinear intrinsic large-signal model for the GaAs MESFET device, for the design of output circuits for power amplifiers, is shown in Fig. 3.25. It includes an additional drain-gate voltage-controlled source $I_{gd}(V_{gs}, V_{ds})$, which represents the drain-gate avalanche current that can occur at large-signal operation, and the channel resistance R_{gs} (which is assumed to be constant) as well as the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd}.

To approximate a relationship between the drain current and the gate-source voltage more accurately, a cubic approximation is proposed:

$$I_{ds} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right) \tanh(\gamma V_{ds}) \tag{3.71}$$

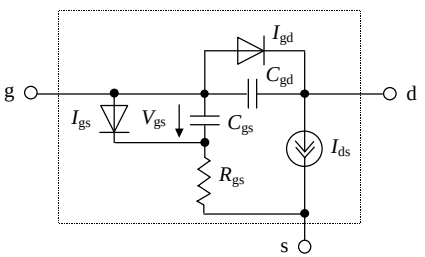


Figure 3.25 Curtice-Ettenberg cubic nonlinear intrinsic model.

where

$$V_1 = V_{gs}(t-\tau)\left[1+\beta\left(V_{ds}^0 - V_{ds}(t)\right)\right] \tag{3.72}$$

β = coefficient for pinch-off change
γ = slope of drain characteristic in the linear region
τ = internal time delay of MESFET
V_{ds}^0 = drain-source voltage at which A_0, A_1, A_2, A_3 are evaluated

The coefficients A_0, A_1, A_2, A_3 can be evaluated from experimental data; in the saturation region where A_0 is the drain saturation current for $V_{gs} = 0$, A_1 can be preliminary evaluated as the transconductance parameter.

The drain current cannot be pinched off at large drain-source voltages because of the gate current produced by avalanche breakdown. Therefore, in this model, the drain-gate avalanche current is

$$I_{gd} = \begin{cases} \dfrac{V_{gd}(t) - V_B}{R_1} & V_{gd} \geq V_B \\ 0 & V_{gd} < V_B \end{cases} \tag{3.73}$$

where

$$V_B = V_{B0} + R_2 I_{ds} \tag{3.74}$$

R_1 is the approximate breakdown resistance and R_2 is the resistance that relates breakdown voltage to the channel currents.

The forward-biased gate current can be determined from

$$I_{gs} = \begin{cases} \dfrac{V_{gs}(t) - V_{gsi}}{R_F} & V_{gs} \geq V_{gsi} \\ 0 & V_{gs} < V_{gsi} \end{cases} \tag{3.75}$$

whereV_{gsi} is the built-in gate voltage and R_F is the effective value of forward-bias resistance.

Materka-Kacprzak nonlinear model [31, 32]

The large-signal MESFET model for computer calculation of GaAs MESFET amplifier characteristics is shown in Fig. 3.26, where the gate-source diode is connected in parallel to the gate source capacitance C_{gs}. The main nonlinear elements are: the equivalent gate-source capacitance C_{gs}, the diode in parallel to C_{gs} (which represents the current in the gate-channel junction), the drain current source I_{ds}, and the gate-drain current source I_{gd} (which represents the effect of the gate-drain breakdown). The remaining parameters of this model are assumed to be linear.

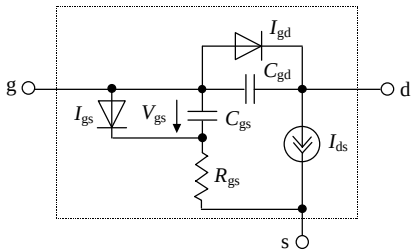


Figure 3.26 Materka-Kacprzak nonlinear intrinsic model.

The voltage-controlled drain current source $I_{ds}(V_{gs}, V_{ds})$ is given by

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tanh\left(\frac{\alpha V_{ds}}{V_{gs} - V_p}\right) \tag{3.76}$$

where

$$V_p = V_{po} + \gamma V_{ds}$$

I_{dss} = saturation drain current for $V_{gs} = 0$
α = saturation voltage parameter
γ = voltage slop parameter of pinch-off voltage
V_{po} = pinch-off voltage for $V_{ds} = 0$

To take into account the time delay between drain current I_{ds} and gate voltage V_{gs}, it is necessary to calculate the instantaneous drain current $I_{ds}(t)$ from Eq. (3.76) with $V_{gs} = V_{gs}(t - \tau)$ and $V_{ds} = V_{ds}(t)$, where τ is the model parameter.

The nonlinear gate-source capacitance C_{gs} can be described for $V_{gs} < 0.8V_{gsi}$ using Eq. (3.70) as Schottky barrier capacitance. For $V_{gs} \geq 0.8V_{gsi}$, C_{gs} is approximated by a straight line with the slope equal to the derivative dC_{gs}/dV_{gs} obtained from Eq. (3.70) at $V_{gs} = 0.8V_{gsi}$.

The current of the gate-diode I_{gs} and gate-drain current I_{gd} can be calculated from

$$I_{gs} = I_{gss}[\exp(\alpha_s V_{gs}) - 1] \tag{3.77}$$

$$I_{gd} = I_{gdsr}[\exp(\alpha_{sr} V_{gd}) - 1] \tag{3.78}$$

where I_{gss}, I_{gdsr}, α_s, and α_{sr} are the model parameters. It should be noted that the current source I_{gd} does not represent any forward biased *p-n* or Schottky barrier junction connected between gate and drain terminals, and only approximates the breakdown current. Therefore, the breakdown current calculated from Eq. (3.78) is negligibly small but can be increased considerably at large values of the gate-drain voltages.

Raytheon (Statz et al.) nonlinear model [33]

The large-signal MESFET model used for circuit simulation in SPICE is presented in Fig. 3.27. All elements are nonlinear.

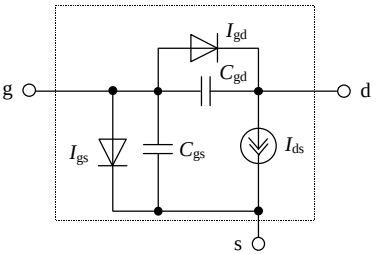


Figure 3.27 Statz nonlinear intrinsic model.

The following drain current source model for $V_{gs} > V_p$ is proposed to describe more accurately the behavior of the drain current I_{ds} as a function of the gate-source voltage V_{gs} in the pinch-off region:

$$I_{ds} = \begin{cases} \dfrac{\beta(V_{gs} - V_p)^2}{1 + b(V_{gs} - V_p)}(1 + \lambda V_{ds}) \left[1 - \left(1 - \dfrac{\alpha V_{ds}}{3}\right)^3\right] & 0 < V_{ds} < \dfrac{3}{\alpha} \\ \dfrac{\beta(V_{gs} - V_p)^2}{1 + b(V_{gs} - V_p)}(1 + \lambda V_{ds}) & V_{ds} \geq \dfrac{3}{\alpha} \end{cases} \tag{3.79}$$

where

V_p = pinch-off voltage
α = slope of drain characteristic in the linear region
λ = channel length modulation parameter
b = doping profile extending parameter
β = transconductance coefficient

As a result, the approximation in Eq. (3.79) is quadratic for small values of $V_{gs} - V_p$; for their large values it becomes almost linear in $V_{gs} - V_p$, which is more realistic behavior of I_{ds} as a function of V_{gs} for real MESFET devices. A tanh function used in previous models below saturation was approximated by a simple polynomial with $n = 3$ that gives the best fit.

The approximations for C_{gs} and C_{gd} are calculated based on assumptions of the charge conservation law for symmetrical MESFET devices when C_{gs} and C_{gd} are equal at zero V_{ds}, and of a smooth transition from positive to negative drain-source voltages to avoid a discontinuity at $V_{ds} = 0$. Thus, the gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} can be calculated as follows:

$$C_{gs} = \frac{1}{2} \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{new}}{V_B}}} \frac{F_1 F_2}{2} + C_{gd0} \frac{F_3}{2} \tag{3.80}$$

$$C_{gd} = \frac{1}{2} \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{new}}{V_B}}} \frac{F_1 F_3}{2} + C_{gd0} \frac{F_2}{2} \tag{3.81}$$

where

$$F_1 = 1 + \frac{V_{\text{eff1}} - V_{\text{p}}}{\sqrt{(V_{\text{eff1}} - V_{\text{p}})^2 + \delta^2}} \qquad F_2 = 1 + \frac{V_{\text{gs}} - V_{\text{gd}}}{\sqrt{(V_{\text{gs}} - V_{\text{gd}})^2 + \left(\frac{1}{\alpha}\right)^2}}$$

$$F_3 = 1 - \frac{V_{\text{gs}} - V_{\text{gd}}}{\sqrt{(V_{\text{gs}} - V_{\text{gd}})^2 + \left(\frac{1}{\alpha}\right)^2}}$$

$$V_{\text{new}} = \frac{1}{2}\left(V_{\text{eff1}} + V_{\text{p}} + \sqrt{(V_{\text{eff1}} - V_{\text{p}})^2 + \delta^2}\right)$$

$$V_{\text{eff1}} = \frac{1}{2}\left(V_{\text{gs}} + V_{\text{gd}} + \sqrt{(V_{\text{gs}} - V_{\text{gd}})^2 + \left(\frac{1}{\alpha}\right)^2}\right)$$

C_{gso} is the gate-source Schottky-barrier capacitance at $V_{\text{gs}} = 0$, C_{gdo} is the gate-source Schottky-barrier capacitance at $V_{\text{gd}} = 0$, V_{B} is the built-in barrier voltage, and δ is the voltage width with smooth transition from V_{p} to V_{eff}, which can be chosen to be 0.2 V.

Figure 3.28 shows the approximate voltage behavior of normalized gate-source capacitance $C_{\text{gs}}/C_{\text{gs0}}$ for a GaAs MESFET device with pinch-off voltage of –2.5 V. For normal biasing conditions, when $V_{\text{ds}} >> 0$, the gate-source capacitance C_{gs} follows a Schottky-barrier capacitance model whereas, when V_{gs} approaches the pinch-off voltage V_{p}, it falls rapidly to zero within a voltage range δ. For reverse biasing conditions, when $V_{\text{ds}} << 0$, the gate-source capacitance C_{gs} is really the gate-drain

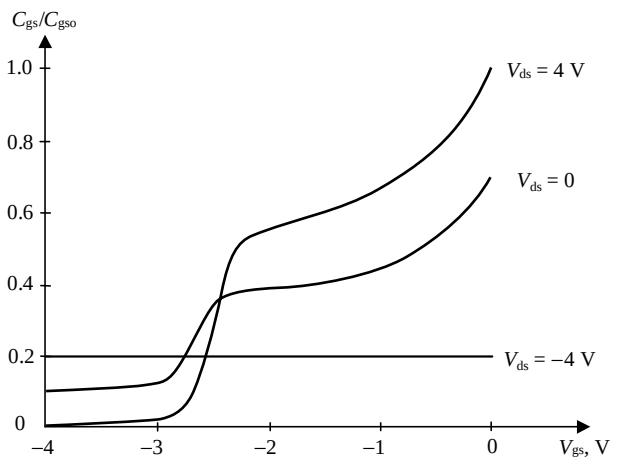


Figure 3.28 Gate-source capacitance versus gate-source voltage.

capacitance C_{gd0} because the reverse bias interchanges the roles of source and drain. In that case, the capacitance becomes small and independent of V_{gs}. Due to the smooth transition from positive to negative drain-source voltages, the behavior of the gate-source capacitance C_{gs} for $V_{ds} = 0$ is intermediate between the two cases of positive and negative V_{ds} mentioned above.

Because of their simplicity and strict convergence criteria, the proposed capacitance model is very attractive for large signal simulators. The latest measurement results of ion implanted GaAs MESFET show that, if the bias dependence of C_{gs} is modeled correctly, then the simulated values of C_{gd} deviate significantly from the measurement [24]. In this case, the approximation for C_{gs} and C_{gd} can be calculated according to

$$C_{gs} = \frac{1}{2}\frac{C_{gs0}}{\sqrt{1-\dfrac{V_{new}}{V_B}}}\frac{F_1F_2}{2} + C_{gd0}\frac{F_3}{2}\frac{V_B}{\sqrt{V_{eff2}^2+V_B^2}} \tag{3.82}$$

$$C_{gd} = \frac{1}{2}\frac{C_{gs0}}{\sqrt{1-\dfrac{V_{new}}{V_B}}}\frac{F_1F_3}{2} + C_{gd0}\frac{F_2}{2}\frac{V_B}{\sqrt{V_{eff2}^2+V_B^2}} \tag{3.83}$$

where

$$V_{eff2} = \frac{1}{2}\left(V_{gs}+V_{gd}-\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}\right)$$

F_1, F_2, F_3, V_{eff1}, and V_{new} are the same as in Eqs. (3.79) and (3.80).

Figure 3.29 shows the approximate behavior of the improved normalized characteristic of C_{gd} (curve 1) compared to the original one (curve 2) calculated by Eq. (3.81).

Since, in the saturation region, the dc output conductance is much smaller than the RF output conductance, the Statz large-signal model can be made more precise by adding a series *RC*-circuit, as shown in Fig. 3.30. The parameters of a bias dependent drain-source dispersive resistance R_{dsd} decoupled by a large capacitance C_{dsd} are chosen to correctly model the output conductance at high frequencies. The drain-source dispersive resistance is modeled as follows [24]:

$$R_{dsd} = R_{dsd0}\left[1+\left(\frac{2}{\alpha V_{eff3}}\right)^2\right]\left(1-\frac{V_g}{2V_{dis}}\right) \tag{3.84}$$

where $V_{eff3} = \sqrt{V_{ds}^2+\delta^2}$, $V_g = V_{gs}$ for $V_{ds} > 0$ V, $V_g = V_{gd}$ for $V_{ds} < 0$, R_{dsd0} and V_{dis} are the fitting parameters.

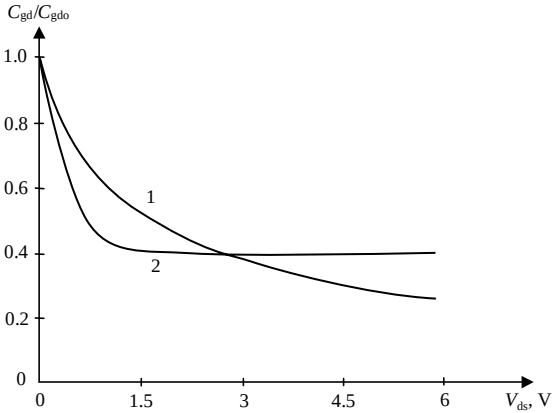


Figure 3.29 Gate-drain capacitance versus drain-source voltage.

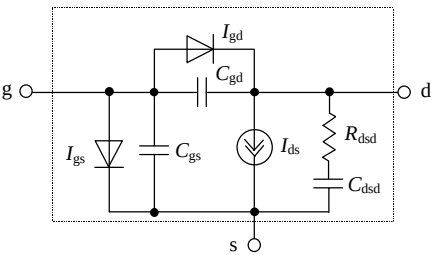


Figure 3.30 Statz nonlinear intrinsic model with series *RC* circuit.

TriQuint nonlinear model [34]

This model represents a modification of Statz model for more accurate modeling of I-V characteristics of GaAs MESFET transistors. The first modification is designed to improve a poor fit at near-pinch-off values of V_{gs} whereas the second modification takes into account a decrease of I_{ds} at higher values of current and voltage, showing a smaller slope than could result from the Statz model. As a result, the following model of drain current source for $V_{gs} > V_p$ is proposed:

$$I_{ds} = \frac{I_{ds0}}{1 + \delta V_{ds} I_{ds0}}$$

$$I_{ds0} = \begin{cases} \beta(V_{gs} - V_T)^Q \left[1 - \left(1 - \dfrac{\alpha V_{ds}}{3}\right)^3\right] & 0 < V_{ds} < \dfrac{3}{\alpha} \\ \beta(V_{gs} - V_T)^Q & V_{ds} \geq \dfrac{3}{\alpha} \end{cases} \tag{3.85}$$

where

$$V_T = V_p - \gamma V_{ds}$$

γ = slope parameter of pinch-off voltage
V_p = pinch-off voltage
α = slope of drain characteristic in the linear region
δ = slope of drain characteristic in the saturated region
Q = power law parameter
β = transconductance coefficient

The approximations for C_{gs} and C_{gd} are practically the same as for the Statz model, except for the new voltage V_T that has to be taken into account:

$$C_{gs} = \frac{1}{2}\frac{C_{gs0}}{\sqrt{1-\dfrac{V_{new}}{V_B}}}\frac{F_1F_2}{2} + C_{gd0}\frac{F_3}{2} \tag{3.86}$$

$$C_{gs} = \frac{1}{2}\frac{C_{gs0}}{\sqrt{1-\dfrac{V_{new}}{V_B}}}\frac{F_1F_3}{2} + C_{gd0}\frac{F_2}{2} \tag{3.87}$$

where

$$F_1 = 1 + \frac{V_{eff1} - V_T}{\sqrt{(V_{eff1} - V_T)^2 + \delta^2}}$$

$$V_{new} = \frac{1}{2}\left(V_{eff1} + V_T + \sqrt{(V_{eff1} - V_T)^2 + \delta^2}\right)$$

F_2, F_3, and V_{eff1} are the same as in Eqs. (3.80) and (3.81).

Chalmers (Angelov) nonlinear model [35, 36]

A simple and accurate large-signal model for different submicron gate-length HEMT devices and commercially available MESFETs, capable of modeling the drain current-voltage characteristics and its derivatives, as well as the gate-source and gate-drain capacitances, is shown in Fig. 3.31. This model can be used not only for large-signal analysis of power amplifiers and oscillators but also for predicting the performance of multipliers and mixers including intermodulation simulation.

The drain current source is described by using the hyperbolic functions as follows:

$$I_{ds} = I_{pk}(1 + \tanh\psi)(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{3.88}$$

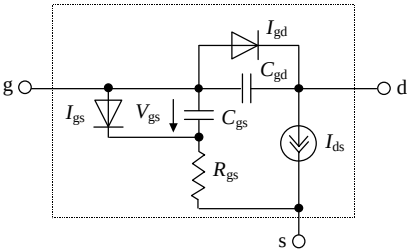


Figure 3.31 Angelov nonlinear intrinsic model.

where I_{pk} is the drain current at maximum transconductance with the contribution from the output conductance subtracted, λ is the channel length modulation parameter, and $\alpha = \alpha_0 + \alpha_1 \tanh \psi$ is the saturation voltage parameter, where α_0 is the saturation voltage parameter at pinch-off, and α_1 is the saturation voltage parameter at $V_{gs} > 0$.

The parameter ψ is a power series function centered at V_{pk} with bias voltage V_{gs} as a variable:

$$\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 + \cdots \tag{3.89}$$

where V_{pk} is the gate voltage for maximum transconductance g_{mpk}. The model parameters as a first approximation can be easily obtained from the experimental $I_{ds}(V_{gs}, V_{ds})$ dependencies at a saturated channel condition when all higher terms in ψ are assumed to be zero, and λ is the slope of the I_{ds}-V_{ds} characteristic.

The intrinsic maximum transconductance g_{mpk} is calculated from the measured maximum transconductance g_{mpkm} by taking into account the feedback effect due to the source resistance R_s:

$$g_{mpk} = \frac{g_{mpkm}}{1 - g_{mpkm} R_s} \tag{3.90}$$

To evaluate the gate voltage V_{pk} and parameter P_1, it is necessary to define the derivatives of the drain current. If higher order terms of ψ are neglected, the transconductance g_m becomes equal to

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = I_{pk} P_1 \operatorname{sech}[P_1(V_{gs} - V_{pk})]^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \tag{3.91}$$

The gate voltage V_{pk} that depends on the drain voltage can be extracted by finding the gate voltages for maximum transconductance, at which the second derivative of the drain current is equal to zero. In this case, it is advisable to use the following simplified expression:

$$V_{pk}(V_{ds}) = V_{pk0} + (V_{pks} - V_{pk0})(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \tag{3.92}$$

where V_{pk0} is measured at V_{ds} close to zero and V_{pks} is measured atV_{ds} in the saturation region.

A good fitting of P_1 and good results in harmonic balance simulations are obtained using

$$P_1 = P_{1\text{sat}}\left[1 + \left(\frac{P_{10}}{P_{1\text{sat}}} - 1\right)\frac{1}{\cosh^2(BV_{\text{ds}})}\right] \tag{3.93}$$

where $P_{10} = g_{\text{m0}}/I_{\text{pk0}}$ at V_{ds} close to zero and B is the fitting parameter ($B \approx 1.5\alpha$). The parameter P_2 makes the derivative of the drain current asymmetric whereas parameter P_3 changes the drain current values at voltages V_{gs} close to the pinch-off voltage V_{p}. Three terms in Eq. (3.89) are usually enough to describe the behavior of the different MESFET or HEMT devices with acceptable accuracy.

The same hyperbolic functions can be used to model the intrinsic device capacitances. When a 5 to 10 percent accuracy is sufficient, the gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} can be described by the following simplified expressions:

$$C_{\text{gs}} = C_{\text{gs0}}[1 + \tanh(P_{1\text{gsg}}V_{\text{gs}})][1 + \tanh(P_{1\text{gsd}}V_{\text{ds}})] \tag{3.94}$$

$$C_{\text{gd}} = C_{\text{gd0}}[1 + \tanh(P_{1\text{gdg}}V_{\text{gs}})][1 - \tanh(P_{1\text{gdd}}V_{\text{ds}} + P_{1\text{cc}}V_{\text{gs}}V_{\text{ds}})] \tag{3.95}$$

where the product $P_{1\text{cc}}V_{\text{gs}}V_{\text{ds}}$ reflects the cross-coupling of V_{gs} and V_{ds} on C_{gd}, and the coefficients $P_{1\text{gsg}}$, $P_{1\text{gsd}}$, $P_{1\text{gdg}}$, and $P_{1\text{gdd}}$ are the fitting parameters. These dependencies, unlike the diode-like models, are suitable for HEMT devices with an undoped AlGaAs spacer layer because of the saturation effect the gate-source capacitance C_{gs} has in increasing V_{gs}. This is due to the absence of parasitic MESFET channel formation in the undoped AlGaAs layer, found in HEMTs with a doped AlGaAs layer. The approximate behavior of normalized gate-source capacitance $C_{\text{gs}}/C_{\text{gs0}}$ (curve 1) and gate-drain capacitance $C_{\text{gd}}/C_{\text{gd0}}$ (curve 2) as functions of V_{ds} for zero gate-source voltage is shown in Fig. 3.32, where C_{gs0} and C_{gd0} are the gate-source and gate-drain capacitances, respectively, at $V_{\text{ds}} = 0$. The character of the curves is the same for positive and negative V_{gs}, except that with the decrease of V_{gs} the capacitance range decreases for the same range of V_{ds}.

The drain-source dispersive resistance R_{dsd} as a nonlinear function of gate-source voltage V_{gs} can be defined by using the following expression [26]:

$$R_{\text{dsd}} = R_{\text{dsd0}} + \frac{R_{\text{dsdp}}}{1 + \tanh\psi} \tag{3.96}$$

where R_{dsd0} is minimum value of R_{dsd} and R_{dsdp} determines the value of R_{dsd} at the pinch-off.

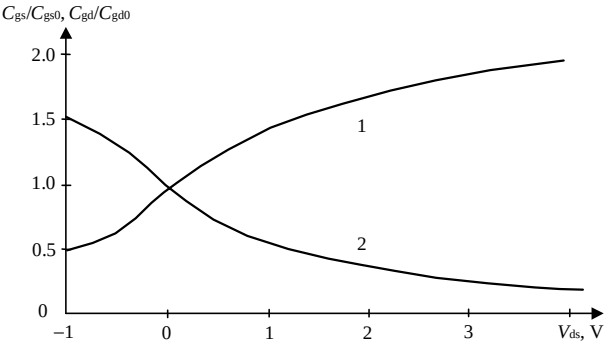


Figure 3.32 Gate-source and gate-drain capacitances versus drain-source voltage.

IAF (Berroth) nonlinear model [37]

An analytical charge-conservative large-signal model for HEMT devices, which is valid for frequency range up to 60 GHz, is shown in Fig. 3.33. The current sources I_{gs}, I_{gd}, I_{ds} and capacitances C_{gs}, C_{gd} are considered as the nonlinear elements in this model.

The drain current source is represented by the following nonlinear equation with 10 fitting parameters:

$$I_{ds} = f(V_{gs})\left[1 + \frac{\lambda}{1 + \Delta_\lambda\left(V_{gs} - V_c + \frac{2}{\beta}\right)} V_{ds}\right] \tanh(\alpha V_{ds}) \qquad (3.97)$$

where

$$f(V_{gs}) = CD_{vc}\{1 + \tanh[\beta(V_{gs} - V_c) + \gamma(V_{gs} - V_c)^3]\} + CD_{vsb}\{1 + \tanh[\delta(V_{gs} - V_{sb})]\}$$

α = slope of drain current in the pinch-off region
β = slope parameter of drain current
γ = slope parameter of drain current in the pinch-off region
λ = slope of drain current in the saturation region

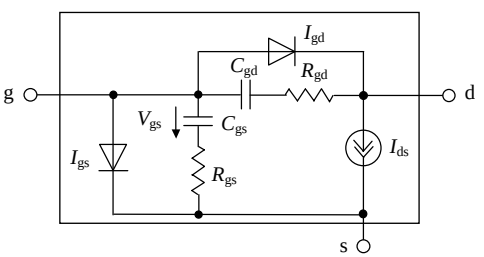


Figure 3.33 Berroth nonlinear intrinsic model.

Δ_λ = gate voltage parameter for slope of drain current
δ = drain current slope parameter correction term
V_c = gate voltage for maximum transconductance
V_{sb} = gate voltage for maximum transconductance correction term
CD_{vc} = drain current multiplication factor
CD_{vsb} = drain current multiplication factor correction term

To describe the I_{gs} and I_{gd} current sources, the diode model for both forward and reverse bias operation modes was used, with the forward bias fitting parameters I_{dsat} and n represented by

$$I_{diode} = I_{dsat}\left[\exp\left(\frac{V_{diode}}{nV_T}\right) - 1\right] \tag{3.98}$$

where V_T is the temperature voltage, and n is the diode ideality factor.

The nonlinear capacitances C_{gs} and C_{gd} are calculated by differentiating the following voltage-dependent charge function $Q_g(V_{gs}, V_{ds})$ with respect to V_{gs} and V_{ds}, which leads to the input capacitance $C_{11} = C_{gs} + C_{gd}$ and transcapacitance $C_{12} = -C_{gd}$, respectively:

$$Q_g(V_{gs}, V_{ds}) = Af_1 f_2 + E(V_{gs} - 0.5V_{ds}) \tag{3.99}$$

where

$$f_1 = \frac{1}{B}\ln\cosh\{B[(V_{gs} - V_1) - 0.5\tanh(CV_{ds})]\} + (V_{gs} - V_1) - 0.5\tanh(CV_{ds})$$

$$f_2 = 1 + D\ln\cosh(FV_{ds})$$

V_1 is the transition voltage, and A, B, C, D, E, and F are the model fitting parameters.

Model selection

A large-signal device model should be sufficiently accurate for all operation conditions, and as simple as possible. Let us first compare several large-signal models. Some models are not consistent with a common small-signal model—for example, the charging resistance R_{gs} is not described in the Curtice quadratic, Statz or TriQuint models—and in most of the models the effect of the frequency dispersion of transconductance and output conductance is omitted. Besides, another important problem of some large-signal models is their failure to carry out a charge conversation condition. A quantitative example to verify the described I-V models for 0.5 μm GaAs MESFET is shown in Table 3.4, where the maximum error and the RMS (root-mean-square) error between

TABLE 3.4 Accuracy of Various Drain Current Models

Model	$I_{ds} = I_{ds}(V_{gs})$		$I_{ds} = I_{ds}(V_{ds})$		Number of fitting parameters
	Max. error %	RMS error %	Max. error %	RMS error %	
Curtice quadratic	10.64	2.888	17.05	8.136	4
Curtice cubic	13.31	3.133	48.61	9.336	7
Statz	10.64	2.565	12.99	7.472	5
Materka	4.646	1.933	20.58	6.085	4
TriQuint	6.214	2.875	7.142	2.296	6

simulated and measured characteristics of I_{ds} versus V_{gs} and I_{ds} versus V_{ds} are shown [38].

The Curtice cubic model produces the largest maximum and RMS errors. The Statz and Materka models are slightly superior regarding maximum error, although the Materka model provides much better description of the slopes of the volt-ampere characteristics in the pinch-off region [39]. The TriQuint model is more accurate in describing $I_{ds}(V_{ds})$ than the presented models. Although the Materka model does not fulfill charge conservation, it seems to be an acceptable compromise between accuracy and model simplicity for MESFETs but not for pseudomorphic HEMTs, where it is preferable to use the Angelov method [39]. A diode-like capacitance model does not approximate the measured C-V characteristics closely enough. For HEMT devices, an analytical charge-conservative Berroth model can be used to model the large-signal parameters in the frequency range up to 60 GHz.

BJTs and HBTs

Small-signal equivalent circuit

The complete bipolar transistor small-signal equivalent circuit with extrinsic parasitic elements is shown in Fig. 3.34. This hybrid π-type representation allows the description of the electrical properties of bipolar transistors, in particularly HBT devices, with sufficient accuracy, up to 30 GHz [40, 41]. Here, the extrinsic elements R_b, L_b, R_c, L_c, R_e, and L_e are the series resistances and lead inductances associated with the base, collector and emitter, and C_{pbe}, C_{pbc}, and C_{pce} are the parasitic capacitances associated with the contact pads, respectively. The lateral resistance and the base semiconductor resistance underneath the base contact and the base semiconductor resistance underneath the emitter are combined into a base-spreading resistance r_b. The intrinsic model is described by the dynamic diode resistance r_π, total base-emitter junction capacitance and base charging capacitance C_π, the transconductance

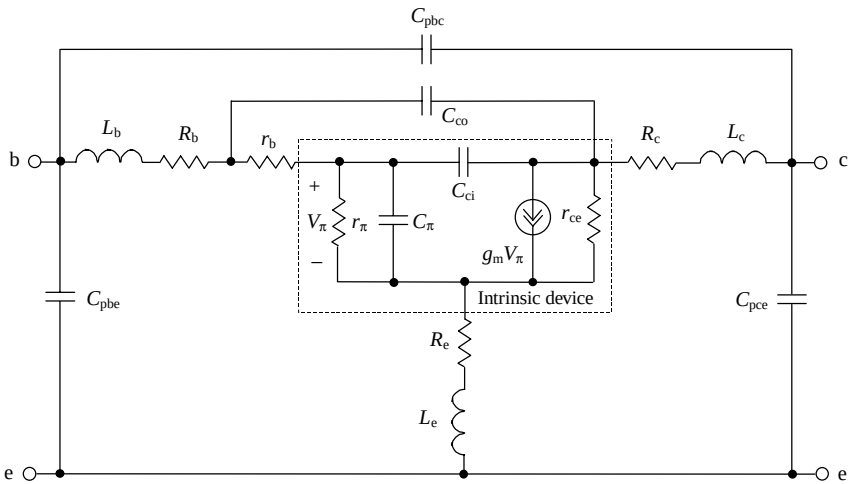


Figure 3.34 Small signal equivalent circuit of bipolar device.

g_m and the output Early resistance r_{ce}, that model the effect on the transistor characteristics of base-width modulation due to variations in the collector-base depletion region. To increase the usable operating frequency range of the device up to 50 GHz, it is necessary to properly include the collector current delay time in the collector current source as $g_m \exp(-j\omega\tau_\pi)$, where τ_π is the transit time [42].

Determination of equivalent circuit elements

If all extrinsic parasitic elements of the device equivalent circuit shown in Fig. 3.34 are known, the intrinsic two-port network parameters from the parasitics can be embedded with the following determination procedure [40]:

- Measurement of the S-parameters of the extrinsic device
- Transformation of the S-parameters to the admittance Y-parameters with subtraction of the parasitic shunt capacitances C_{pbe}, C_{pbc}, and C_{pce}
- Transformation of the new Y-parameters to the impedance Z-parameters with subtraction of the parasitic series elements L_b, R_b, L_e, R_e, and L_c, R_c
- Transformation of the new Z-parameters to the Y-parameters with subtraction of the parasitic shunt capacitance C_{co}
- Transformation of the new Y-parameters to the Z-parameters with subtraction of the parasitic series resistance r_b
- Transformation of the new Z-parameters to the Y-parameters of the intrinsic device two-port network

The bipolar transistor intrinsic Y-parameters can be written as

$$Y_{11} = \frac{1}{r_\pi} + j\omega(C_\pi + C_{ci}) \tag{3.100}$$

$$Y_{12} = -j\omega C_{ci} \tag{3.101}$$

$$Y_{21} = g_m \exp(-j\omega\tau_\pi) + j\omega C_{ci} \tag{3.102}$$

$$Y_{22} = \frac{1}{r_{ce}} + j\omega C_{ci} \tag{3.103}$$

After separating Eqs. (3.100) to (3.103) into their real and imaginary parts, the elements of the intrinsic small-signal equivalent circuit can be determined analytically as follows:

$$C_\pi = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega} \tag{3.104}$$

$$r_\pi = \frac{1}{\mathrm{Re}Y_{11}} \tag{3.105}$$

$$C_{ci} = -\frac{\mathrm{Im}Y_{12}}{\omega} \tag{3.106}$$

$$g_m = \sqrt{(\mathrm{Re}Y_{21})^2 + (\mathrm{Im}Y_{21} + \mathrm{Im}Y_{12})^2} \tag{3.107}$$

$$\tau_\pi = \frac{1}{\omega}\cos^{-1}\frac{\mathrm{Re}Y_{21} + \mathrm{Re}Y_{12}}{\sqrt{(\mathrm{Re}Y_{21})^2 + (\mathrm{Im}Y_{21} + \mathrm{Im}Y_{12})^2}} \tag{3.108}$$

$$r_{ce} = \frac{1}{\mathrm{Re}Y_{22}} \tag{3.109}$$

The parasitic capacitances associated with the pads can be determined by the measurement of the open test structure with the corresponding circuit model shown in Fig. 3.35(a). When the values of these pad capacitances are known, it is easy to determine the values of the parasitic series inductances by measuring the shorted test structure

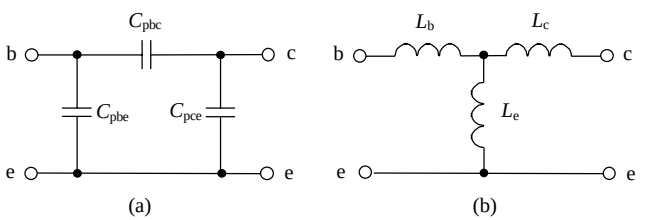


Figure 3.35 Models for parasitic (a) pad capacitances and (b) lead inductances.

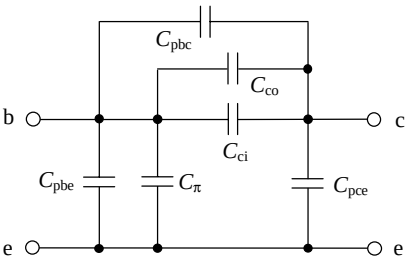


Figure 3.36 Small-signal model at low frequencies and cutoff operation mode.

with the corresponding circuit model presented in Fig. 3.35(*b*).

The values of the series parasitic resistances can be calculated on the basis of the physical parameters of the device, or by adding them to the intrinsic device parameters (with the appropriate solution of a nonlinear system of eight equations with eight independent variables using iterative technique) [41]. In the latter case, it is supposed that the influence of the device transit time τ_π on the HBT electrical properties in a frequency range up to 30 GHz is negligible.

The external parasitic parallel capacitance C_{co}, as well as other device capacitances, can be estimated from the device behavior at low frequencies and cutoff operating conditions [43, 44]. For such conditions, the device small-signal equivalent circuit is reduced to capacitive elements, as shown in Fig. 3.36.

The device capacitances can be directly calculated from measured *Y*-parameters by

$$C_{pbe} + C_\pi = \frac{\mathrm{Im}\,(Y_{11} + Y_{12})}{\omega} \tag{3.110}$$

$$C_{pce} = \frac{\mathrm{Im}\,(Y_{11} + Y_{12})}{\omega} \tag{3.111}$$

$$C_{pbc} + C_{co} + C_{ci} = -\frac{\mathrm{Im}Y_{12}}{\omega} \tag{3.112}$$

Since C_{pbc} and C_{co} are the bias independent capacitances and C_{ci} is the base-collector junction capacitance, the extraction of $(C_{pbc} + C_{co})$ can be carried out by fitting the sum $(C_{pbc} + C_{co} + C_{ci})$ to the expression for junction capacitance at different base-collector voltages. If an approximation expression for C_{co} is given by

$$C_{co} = C_{jco}/\sqrt{1 + \frac{V_{bc}}{\varphi_c}} \tag{3.113}$$

then the extraction of the parameters C_{jco}, φ_c, and C_{ci} can be performed using the linear equation

$$\left(\frac{C_{jco}}{\frac{\mathrm{Im}Y_{12}}{\omega} + C_{pbc} + C_{ci}}\right)^2 = 1 + \frac{1}{\varphi_c}V_{bc} \tag{3.114}$$

As a result, linearizing this equation by choosing a proper value for C_{ci} with known value of C_{pbc} gives the values for the remaining two parameters, C_{co} and φ_c, from the slope and intercept point of the final linearized dependence.

Equivalence of intrinsic π-circuit and T-circuit topologies

The small-signal equivalent circuit of the bipolar transistor can be represented by both π-model and T-model topologies. The T-model representation is appealing because all the model parameters can be tied directly to the physics of the device, and provide an excellent fit between measured and simulated S-parameters in the frequency range up to 30–40 GHz [42–45]. The HBT small-signal equivalent circuit with T-like topology is shown in Fig. 3.37.

One-to-one correspondence exists between the π-model and T-model of the device circuit topology. Comparing small-signal equivalent circuits shown in Figs. 3.34 and 3.37 demonstrates the only difference in

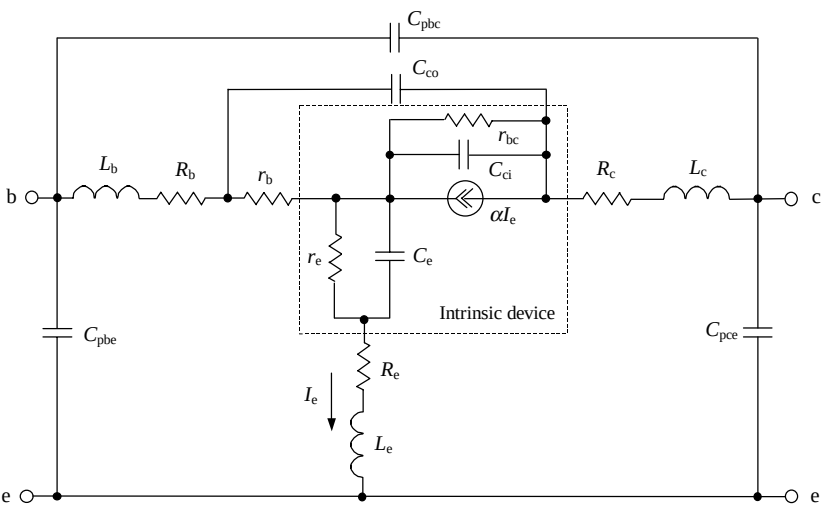


Figure 3.37 Small-signal T-model of bipolar device.

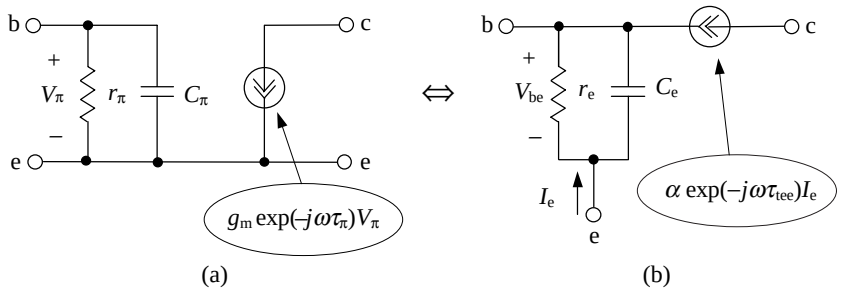


Figure 3.38 Intrinsic (*a*) π-model and (*b*) T-model topologies.

the presentation of the intrinsic device model enclosed in dashed boxes. From Fig. 3.38, the admittances $Y_e = I_e/V_{be}$ for π- and T-models are defined by

$$Y_e = \frac{1}{r_e} + j\omega C_e = \frac{1}{r_\pi} + j\omega C_\pi + g_m \exp(-j\omega\tau_\pi) \tag{3.115}$$

The collector source currents for both models are the same:

$$\alpha \exp(-j\omega\tau_{tee}) I_e = g_m \exp(-j\omega\tau_\pi) V_\pi \tag{3.116}$$

where

$$\alpha = \alpha_0/(1 + j\omega\tau_\alpha)$$
$$\tau_\alpha = 1/2\pi f_\alpha$$

f_α = alpha cutoff frequency
α_0 = low frequency collector-to-emitter current gain

The expressions for intrinsic π-model parameters can be derived from the intrinsic T-model parameters as follows [42]:

$$g_m = \alpha_0 \sqrt{(1/r_e)^2 + (\omega C_e)^2} / \sqrt{1 + (\omega\tau_\alpha)^2} \tag{3.117}$$

$$\tau_\pi = \tau_{tee} - \frac{1}{\omega}\left[\tan^{-1}(\omega C_e r_e) + \tan^{-1}(\omega\tau_\alpha)\right] \tag{3.118}$$

$$\frac{1}{r_\pi} = \frac{1}{r_e} - g_m \cos(\omega\tau_\pi) \tag{3.119}$$

$$C_\pi = C_e - g_m \frac{\sin(\omega\tau_\pi)}{\omega} \tag{3.120}$$

Both π-model and T-model topologies describe HBT electrical properties in a very wide frequency range and when optimized, up to 50 GHz.

Nonlinear bipolar device modeling

Since the bipolar transistor can be considered to be an interacting pair of *p-n* junctions, the approach to model its nonlinear properties is the same as that used for the diode modeling. The simple large-signal Ebers-Moll model with a single current source between the collector and emitter is shown in Fig. 3.39 [5]. The collector-emitter source current I_{ce} is defined by

$$I_{ce} = I_{sat}\left[\exp\left(\frac{V_\pi}{V_T}\right) - \exp\left(\frac{V_{bc}}{V_T}\right)\right] \tag{3.121}$$

where I_{sat} is the bipolar transistor saturation current and V_T is the thermal voltage calculated by

$$V_T = \frac{kT}{q} \tag{3.122}$$

where q is the electron charge, k is Boltzmann's constant, and T is the temperature in Kelvin.

The device terminal currents are defined as $I_c = I_{ce} - I_{bc}$, $I_e = -I_{ce} - I_{be}$, $I_b = I_{be} + I_{bc}$, where the diode currents are given by

$$I_{be} = \frac{I_{sat}}{\beta_F}\left[\exp\left(\frac{V_\pi}{V_T}\right) - 1\right] \tag{3.123}$$

$$I_{bc} = \frac{I_{sat}}{\beta_R}\left[\exp\left(\frac{V_{bc}}{V_T}\right) - 1\right] \tag{3.124}$$

where β_F and β_R are the large-signal forward current gain and reverse current gain of a common-emitter BJT, respectively.

The device capacitances C_π and C_{bc} each consist of two components, and are modeled by the diffusion capacitance and junction capacitance,

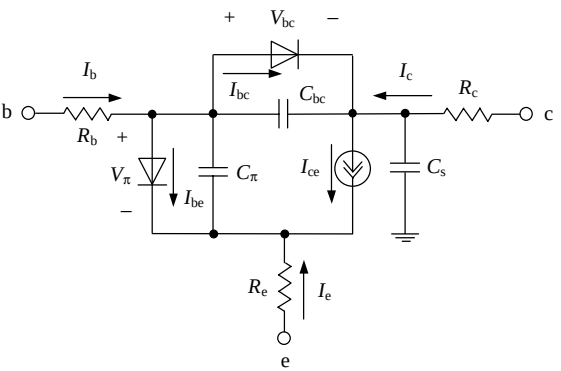


Figure 3.39 Large-signal Ebers-Moll model.

respectively:

$$C_\pi = \tau_F \frac{dI_{be}}{dV_\pi} + C_{jeo}\left(1 - \frac{V_\pi}{\varphi_e}\right)^{-m_e} \tag{3.125}$$

$$C_{bc} = \tau_R \frac{dI_{bc}}{dV_{bc}} + C_{jco}\left(1 - \frac{V_{bc}}{\varphi_c}\right)^{-m_c} \tag{3.126}$$

where τ_F and τ_R are the ideal total forward time and reverse transit time, C_{jeo} and C_{jco} are the base-emitter and base-collector zero-bias junction capacitances, and m_e and m_c are the base-emitter and base-collector junction grading factors, respectively.

The substrate capacitance C_s should be taken into account when designing integrated circuits. Its representation is adequate for many cases, since the epitaxial-layer-substrate junction is reverse-biased for isolation purposes, and usually it is modeled as a capacitance with constant value.

The Ebers-Moll model cannot present the second-order effects due to low current and high-level injection, such as base-width modulation (Early effect) and variation of the large-signal forward current gain β_F with collector current I_c. In addition, to find a better approximation of the distributed structure of the base-collector junction at microwave frequencies, the junction capacitance should be divided into two sections, as shown in Fig. 3.40. This large-signal model is called the Gummel-Poon model.

For the Gummel-Poon large-signal model, the collector-emitter source current I_{ce} is given by [5]

$$I_{ce} = \frac{I_{ss}}{q_b}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - \exp\left(\frac{V_{bc}}{n_R V_T}\right)\right] \tag{3.127}$$

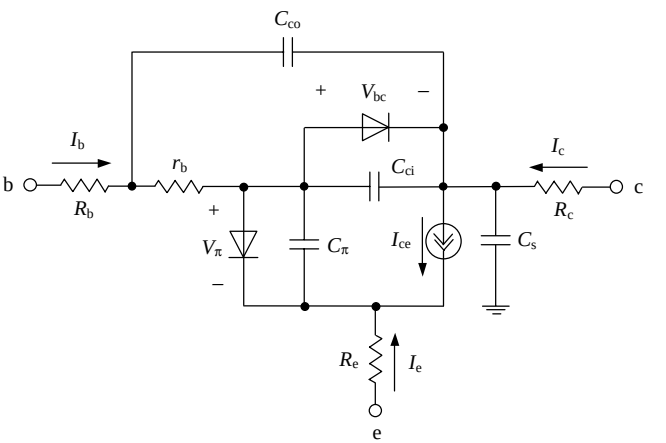


Figure 3.40 Large-signal Gummel-Poon model.

where

I_{ss} = BJT fundamental constant defined at zero-bias condition
n_F = forward current emission coefficient
n_R = reverse current emission coefficient
q_b = variable parameter defined by

$$q_b = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2} \tag{3.128}$$

where

$$q_1 = 1 + \frac{V_\pi}{V_B} + \frac{V_{bc}}{V_A}$$

$$q_2 = \frac{I_{ss}}{I_{KF}}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - 1\right] + \frac{I_{ss}}{I_{KR}}\left[\exp\left(\frac{V_{bc}}{n_R V_T}\right) - 1\right]$$

V_A is the forward Early voltage, V_B is the reverse Early voltage, I_{KF} is the knee current for high-level injection in the normal active region, and I_{KR} is the knee current for low-level injection in inverse region.

The currents through the model diodes are defined by

$$I_{be} = \frac{I_{sat}(0)}{\beta_{FM}(0)}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - 1\right] + C_2 I_{sat}(0)\left[\exp\left(\frac{V_\pi}{n_{EL} V_T}\right) - 1\right] \tag{3.129}$$

$$I_{bc} = \frac{I_{sat}(0)}{\beta_{RM}(0)}\left[\exp\left(\frac{V_{bc}}{n_R V_T}\right) - 1\right] + C_4 I_{sat}(0)\left[\exp\left(\frac{V_{bc}}{n_{CL} V_T}\right) - 1\right] \tag{3.130}$$

where $I_{sat}(0)$ is the saturation current for $V_{bc} = 0$, $\beta_{FM}(0)$ and $\beta_{RM}(0)$ are the large-signal forward current gain and reverse current gain of a common-emitter BJT in mid-current region for $V_{bc} = 0$, C_2 and C_4 are the forward and reverse low-current non-ideal base current coefficients, respectively, n_{EL} is the non-ideal low-current base-emitter emission coefficient, and n_{CL} is the non-ideal low-current base-collector emission coefficient.

The nonlinear behavior of the intrinsic base resistance r_b can be described by the following expression [5]:

$$r_b = r_{bm} + 3(r_{b0} - r_{bm})\frac{\tan z - z}{z\tan^2 z} \tag{3.131}$$

where

$$z = \frac{\sqrt{1 + 144 I_b/\pi^2 I_{rb}} - 1}{(24/\pi^2)\sqrt{I_b/I_{rb}}}$$

r_{bm} = minimum base resistance that occurs at high current level
r_{b0} = base resistance at zero bias with small base current level
I_{rb} = current where the base resistance falls halfway to its minimum value

The intrinsic device capacitances C_π, C_{ci}, and C_{co} are modeled by the diffusion capacitance and junction capacitance, respectively, as follows:

$$C_\pi = \frac{\mathrm{d}}{dV_\pi}\left(\tau_{FF}\frac{I_{cc}}{q_b}\right) + C_{jeo}\left(1 - \frac{V_\pi}{\varphi_e}\right)^{-m_e} \tag{3.132}$$

$$C_{ci} = \tau_R\frac{dI_{bc}}{dV_{bc}} + k_c C_{jco}\left(1 - \frac{V_{bc}}{\varphi_c}\right)^{-m_c} \tag{3.133}$$

$$C_{co} = C_{jco}(1 - k_c)\left(1 - \frac{V_{bco}}{\varphi_c}\right)^{-m_c} \tag{3.134}$$

where k_c is the fraction of base-collector junction capacitance connected to the base resistance r_b, V_{bco} is the voltage through the capacitance C_{co}, and τ_{FF} is the modulated transit time defined by

$$\tau_{FF} = \tau_F\left[1 + X_{\tau F}\left(\frac{I_{cc}}{I_{cc} + I_{\tau F}}\right)^2 \exp\left(\frac{V_{bc}}{1.44V_{\tau F}}\right)\right]$$

where $X_{\tau F}$ is the transit time bias dependence coefficient, $I_{\tau F}$ is the high-current parameter for effect on τ_F , $V_{\tau F}$ is the value of V_{bc} where the exponential equals to 0.5, and

$$I_{cc} = \frac{I_{ss}}{q_b}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - 1\right]$$

As it follows from Eq. (3.132), the nonlinear behavior of capacitance C_π strongly depends on the effect of transit time modulation characterized by τ_{FF}. This transit charge variation results in significant changes of transition frequency f_T at various operation conditions. For example, at medium currents, f_T reaches its peak value and is practically constant. Here, the ideal transit time is defined by $\tau_F = 1/2\pi f_T$ and the dominated base-emitter diffusion capacitance increases linearly with collector current. At low currents, f_T is dominated by the junction capacitance and increases with the increase in collector current. At high currents, the widening of the charge-neutral base region and the pushing of the entire space-charge region toward the heavily doped collector region (the Kirk effect) degrades the frequency response of the transistor by increasing the transit time and decreasing f_T. In this case, the transit time is modeled by τ_{FF}.

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Chapter

4

Impedance Matching

This chapter begins by describing the main principles and tools for impedance matching. Generally, an optimum solution depends on the circuit requirements, such as the simplicity in practical realization, the frequency bandwidth and minimum power ripple, design implementation and adjustability, stable operation conditions, and sufficient harmonic suppression. As a result, many types of the matching networks are available, including lumped elements and transmission lines. To simplify and visualize the matching design procedure, an analytical approach (which allows calculation of the parameters of the matching circuits using simple equations) and Smith chart traces are discussed. In addition, several examples of the narrowband and broadband power amplifiers using bipolar or MOSFET devices are given, including successive and detailed design considerations and explanations. Finally, design formulas and curves are presented for several types of transmission lines including stripline, microstrip line, slotline, and coplanar waveguide.

Main Principles

Impedance matching means to provide maximum delivery to the load of the RF power available from the source. To determine an optimum value of the load impedance Z_L at which the power delivered to the load is maximum, consider the equivalent circuit shown in Fig. 4.1(*a*).

The power delivered to the load can be defined as follows:

$$P = \frac{1}{2} V_{in}^2 \operatorname{Re}\left(\frac{1}{Z_L}\right) = \frac{1}{2} V_S^2 \left|\frac{Z_L}{Z_S + Z_L}\right|^2 \operatorname{Re}\left(\frac{1}{Z_L}\right) \tag{4.1}$$

where $Z_S = R_S + jX_S$, $Z_L = R_L + jX_L$, V_S is the source voltage amplitude, and V_{in} is the load voltage amplitude. Substituting the real and

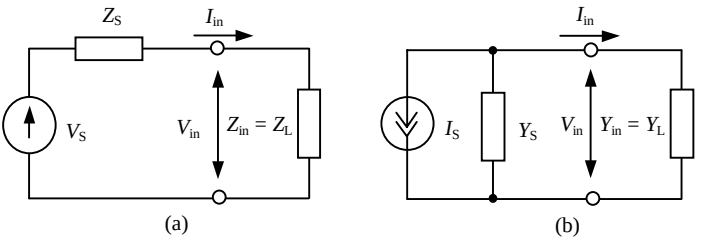


Figure 4.1 Equivalent circuits with (a) voltage and (b) current sources.

imaginary parts of the source and load impedances, Z_S and Z_L, into Eq. (4.1) yields

$$P = \frac{1}{2} V_S^2 \frac{R_L}{(R_S + R_L)^2 + (X_S + X_L)^2} \tag{4.2}$$

Assume the source impedance Z_S is fixed and it is necessary to vary the real and imaginary parts of the load impedance Z_L until maximum power is delivered to the load. To maximize the output power, the following conditions are applied:

$$\frac{\partial P}{\partial R_L} = 0 \qquad \frac{\partial P}{\partial X_L} = 0 \tag{4.3}$$

Applying these conditions and taking into consideration Eq. (4.2), the following system of two equations can be written:

$$\begin{cases} \dfrac{1}{(R_L + R_S)^2 + (X_L + X_S)^2} - \dfrac{2R_L(R_L + R_S)}{[(R_L + R_S)^2 + (X_L + X_S)^2]^2} = 0 \\ \dfrac{2X_L(X_L + X_S)}{[(R_L + R_S)^2 + (X_L + X_S)^2]^2} = 0 \end{cases} \tag{4.4}$$

Simplifying system (4.4) gives

$$\begin{cases} R_S^2 - R_L^2 + (X_L + X_S)^2 = 0 \\ X_L(X_L + X_S) = 0 \end{cases} \tag{4.5}$$

Solving system (4.5) simultaneously for R_S and X_S, we obtain:

$$\begin{cases} R_S = R_L \\ X_L = -X_S \end{cases} \tag{4.6}$$

or in a common impedance case

$$Z_L = Z_S^* \tag{4.7}$$

Equation (4.7) is called a *conjugate matching condition*, and its fulfillment results in maximum power delivered to the load for a fixed source impedance.

Maximum power delivered to the load must be equal to

$$P = \frac{V_S^2}{8R_S} \tag{4.8}$$

The admittance conjugate matching conditions applied to the equivalent circuit presented in Fig. 4.1(*b*)

$$Y_L = Y_S^* \tag{4.9}$$

can be readily obtained in the same way. Maximum power delivered to the load in this case can be written as

$$P = \frac{I_S^2}{8G_S} \tag{4.10}$$

where $G_S = \mathrm{Re}Y_S$, and I_S is the source current amplitude.

Thus, the conjugate matching conditions in a common case can be determined through the immittance parameters, i.e., any system of impedance Z-parameters or admittance Y-parameters, in the following form:

$$W_L = W_S^* \tag{4.11}$$

The matching circuit is connected between the source and input electrodes of an active device shown in Fig. 4.2(a) and between the output electrodes of an active device and load shown in Fig. 4.2(b). For a

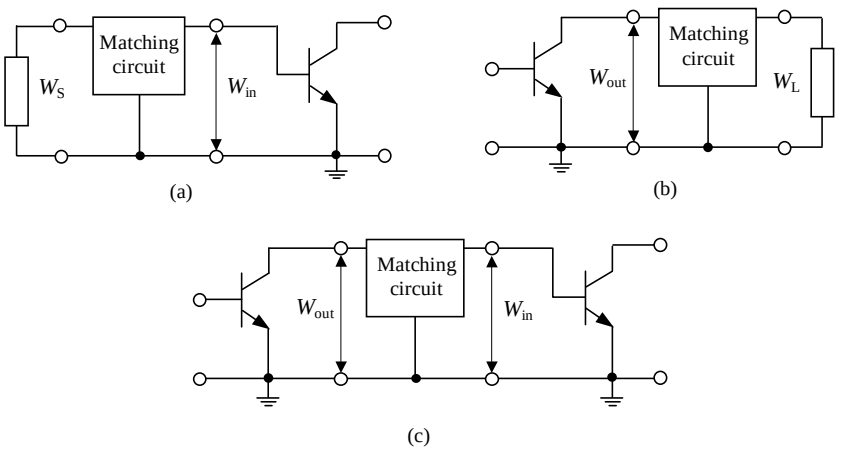


Figure 4.2 Matching circuit arrangements.

multistage power amplifier, the load is an input circuit of the next stage. Therefore, the matching circuit is connected between the output of the active device of the previous amplifier stage and the input of the active device of the subsequent stage of the power amplifier presented by Fig. 4.2(*c*). Usually, the load immittance W_L differs from the output immittance W_{out}, which is necessary to realize the optimal operation mode of the power amplifier. The main objective is, therefore, to transform the load immittance W_L to the optimal output immittance W_{out}, the value of which is determined by the supply voltage, the output power, the saturation voltage of the active device and the selected class of the active device operation. In addition, the matching circuits should be chosen according to the requirements for the amplitude and phase characteristics, the control of the active device voltage and current waveforms, and the stability of operation conditions. The losses in the matching circuits must be as small as possible in order to transmit the output power to the load with maximum efficiency. Finally, it is desirable that the matching circuit be easy to tune.

Smith Chart

The Smith chart is one of the tools most widely used to match circuit designs because it gives a graphical representation of the consecutive matching design procedure [1]. The Smith chart can be applied for matching using either lumped elements or transmission lines. The Smith chart is particularly useful for matching circuit designs that use the transmission lines, because analytical calculation in this case is very complicated. Also, when using the complete Smith chart, the circuit parameters such as *VSWR*, reflection coefficient, return loss, or losses in the transmission line, can be directly calculated.

The Smith chart represents a relationship between the load impedance Z and the reflection coefficient Γ given in Eq. (1.126). It is convenient to rewrite this equation in the normalized form of

$$\frac{Z}{Z_0} = \frac{1+\Gamma}{1-\Gamma} \tag{4.12}$$

to define a normalized impedance Z/Z_0 as

$$\frac{Z}{Z_0} = \frac{R}{Z_0} + j\frac{X}{Z_0} \tag{4.13}$$

and represent the reflection coefficient Γ by

$$\Gamma = \Gamma_r + j\Gamma_i \tag{4.14}$$

Then, substituting Eqs. (4.13) and (4.14) into Eq. (4.12) gives

$$\frac{R}{Z_0} + j\frac{X}{Z_0} = \frac{1 + \Gamma_r + j\Gamma_i}{1 - \Gamma_r - j\Gamma_i} \tag{4.15}$$

By equating the real and imaginary parts, we obtain

$$\left(\Gamma_r - \frac{R}{R + Z_0}\right)^2 + \Gamma_i^2 = \left(\frac{Z_0}{R + Z_0}\right)^2 \tag{4.16}$$

$$(\Gamma_r - 1)^2 + \left(\Gamma_i - \frac{Z_0}{X}\right)^2 = \left(\frac{Z_0}{X}\right)^2 \tag{4.17}$$

As a result, in the Γ_r-Γ_i coordinate plane, Eq. (4.16) represents a family of circles centered at points $\Gamma_r = R/(R + Z_0)$ and $\Gamma_i = 0$ with radii of $Z_0/(R + Z_0)$ called *constant-*(R/Z_0) *circles*. Equation (4.17) represents a family of circles at points $\Gamma_r = 1$ and $\Gamma_i = Z_0/X$ with radii of Z_0/X called *constant-*(X/Z_0) *circles*. These constant-(R/Z_0) and constant-(X/Z_0) circles with different normalized parameters are shown in Fig. 4.3(*a*) where the points $\Gamma_r = -1$ and $\Gamma_r = 1$ are also indicated. The plot of such circles is called the *impedance Smith chart* or the *Z Smith chart*. The curve from the point A to the point C represents the impedance transformation from the pure resistance of 25 Ω to the inductive impedance of $(25 + j25)\,\Omega$, which can be provided by using the inductance connected in series with the resistance.

Eqs. (4.16) and (4.17) can be rewritten easily in the admittance form with the real part G and imaginary part B when a relationship between the impedance Y and the reflection coefficient Γ can be written as

$$\frac{G}{Y_0} + j\frac{B}{Y_0} = \frac{1 - \Gamma_r - j\Gamma_i}{1 + \Gamma_r + j\Gamma_i} \tag{4.18}$$

where $Y_0 = 1/Z_0$. Then,

$$\left(\Gamma_r + \frac{G}{G + Y_0}\right)^2 + \Gamma_i^2 = \left(\frac{Y_0}{G + Y_0}\right)^2 \tag{4.19}$$

$$(\Gamma_r + 1)^2 + \left(\Gamma_i + \frac{Y_0}{B}\right)^2 = \left(\frac{Y_0}{B}\right)^2 \tag{4.20}$$

From Eqs. (4.19) and (4.20) it follows that the *constant-*(G/Y_0) *circles* are centered at $\Gamma_r = -G/(G + Y_0)$ and $\Gamma_i = 0$ with radii of $Y_0/(G + Y_0)$. The *constant-*(B/Y_0) *circles* are centered at points $\Gamma_r = -1$ and $\Gamma_i = -Y_0/B$ with radii of Y_0/B which are shown in Fig. 4.3(*b*). The circles shown are centered at antisymmetric points in contrast to the impedance Smith chart. The *admittance Smith chart* or the *Y Smith chart*, whose admittances coincide with the appropriate impedances plotted at the

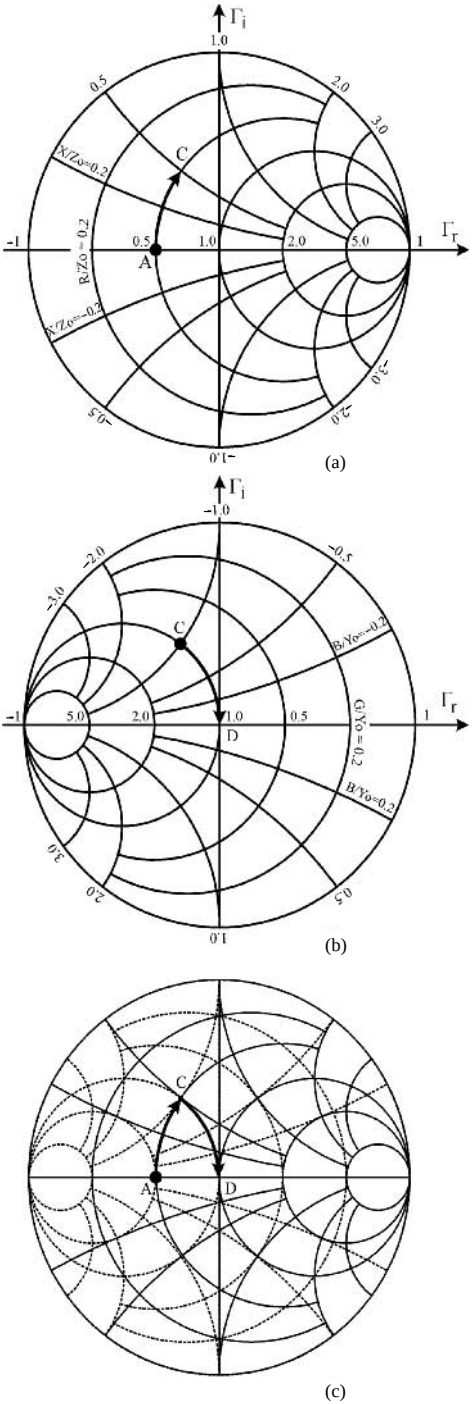


Figure 4.3 Simplified impedance and admittance Smith charts.

Z Smith chart, is the mirror-reflected impedance Smith chart as a result of its rotation by 180°. The curve from the point C to the point D shows the admittance transformation from the inductive admittance of $(20 - j20)$ mS to the pure conductance of 20 mS or resistance of 50 Ω, which can be provided by using the capacitance connected in parallel with the initial admittance. The impedances and admittances can be determined at any impedance or admittance Smith chart where the normalized parameters are indicated. This diagram is called the *immittance Smith chart*. However, in this case, the impedance point and its corresponding admittance value are located one against another at the same distance from the center (1, 0).

Therefore, sometimes it is advisable to use the combined impedance-admittance Smith chart shown in Fig. 4.3(c). This is the case when, for any point, we can read the normalized impedance from the Z Smith chart and normalized admittance from the Y Smith chart. This Z-Y Smith chart avoids the necessity of rotating the impedance by 180° to find the corresponding admittance. A combined impedance-admittance Smith chart is very convenient for matching using lumped elements. For example, it is necessary to convert the source active impedance of 25 Ω (point A) into the load resistance of 50 Ω (point D). First, the series inductance plotted at the Z Smith chart changes the source impedance by moving along the constant-(X/Z_0) circle from point A until point C. Then, it is converted to the Y Smith chart. As a result, the parallel capacitance starting at this point changes the given admittance by moving along the constant-(B/Y_0) circle from point C until point D. A transformation between two resistances for normalizing impedance $Z_0 = 50$ Ω is shown in Fig. 4.3(c).

When designing RF and microwave power amplifiers, it is very important to determine such parameters as *VSWR*, reflection coefficient or losses in the matching circuits based on the lumped parameters or use of the transmission lines. A linear reference scale, placed below the indication of these additional characteristics, has been added to the Smith chart shown in Fig. 4.4. Scales around its periphery show the calibrated electrical wavelength and the angles of the reflection coefficients. The Smith chart can be easily implemented to the graphical design using the transmission lines. Equation (1.132) for the input impedance of the lossless transmission line can be rewritten in terms of the reflection coefficient as

$$\frac{Z_{\text{in}}}{Z_0} = \frac{1 + \Gamma \exp(-2j\theta)}{1 - \Gamma \exp(-2j\theta)} \tag{4.21}$$

This equation differs from Eq. (4.12) only by the added phase angle. This means that the normalized input impedance seen looking into the transmission line with electrical length of θ can be found by rotating this

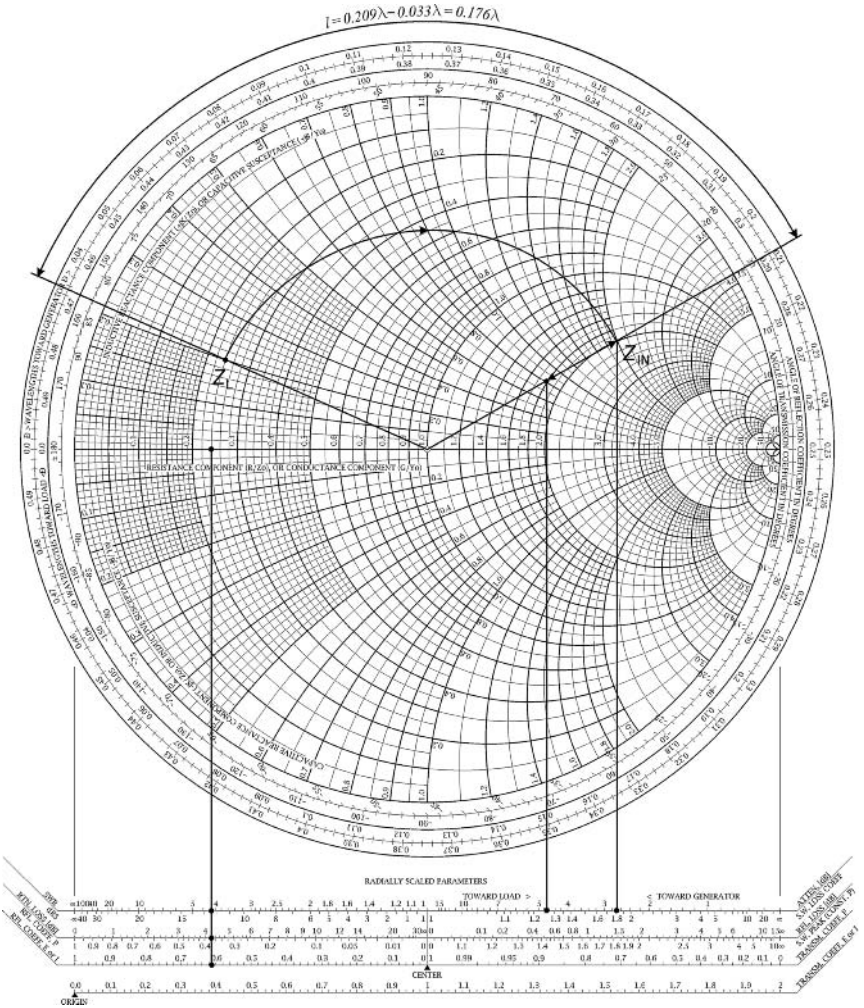


Figure 4.4 Smith chart.

impedance point clockwise by 2θ about the center of the Smith chart with the same radius $|\Gamma|$. By subtracting 2θ from the phase angle of the reflection coefficient, its value decreases in the clockwise direction, according to the periphery scale. In this case, the half wave transmission line provides a clockwise rotation of 2π or 360° about the center, returning the point to its original position.

For example, a typical 50-Ω transmission line provides a transformation of load impedance from $Z_L = (12 + j10)\,\Omega$ to a new impedance of $Z_{in} = (100 + j100)\,\Omega$. The normalized load impedance is $Z_L/Z_0 = (0.24 + j0.2)\,\Omega$, which is plotted on the Smith chart, as shown in Fig. 4.4.

By using a compass to draw the circle from this point to the intersection point with a real axis, we obtain $|\Gamma| = 0.61$ at the reflection coefficient scale, $RL = 4.3$ dB at the return loss scale, and $VSWR = 4.2$ at the standing wave ratio (SWR) scale. To determine the angle of the reflection coefficient, we draw a radial line through the load impedance point to the intersection of the periphery circle (an angle of 83° can be read). If a radial line is drawn through the point of the input impedance at the outer wavelength scale, the difference between points of 0.209λ and 0.033λ gives the length of the transmission line as 0.176λ. However, in the case of the transmission line with losses of 2 dB, the point obtained should be moved to the point of $Z_{\text{in}} = (90 + j40)\,\Omega$, according to the attenuation scale.

Matching with Lumped Elements [2]

The lumped matching circuits in the form of (a) L-transformer, (b) π-transformer, and (c) T-transformer that are presented in Fig. 4.5 have proved to be most effective for power amplifier design. The simplest matching circuit is in the form of the L-transformer. The transforming properties of this matching circuit can be analyzed by using the equivalent transformation of the parallel into the series representation of RX circuit. Let (a) R_1 and X_1 be the resistance and reactance of the impedance $Z_1 = jX_1R_1/(R_1 + jX_1)$ of the parallel circuit, and (b) R_2 and X_2 be the resistive and reactive parts of the impedance $Z_2 = R_2 + jX_2$ of the series circuit presented in Fig. 4.6. As a result, these two circuits

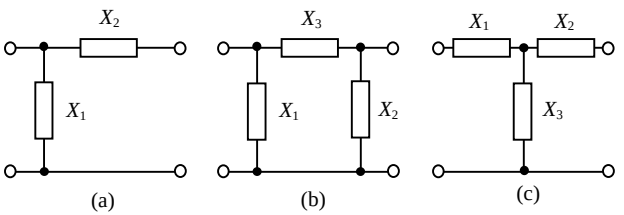


Figure 4.5 Matching circuits in the form of (a) L-, (b) π-, and (c) T-transformers.

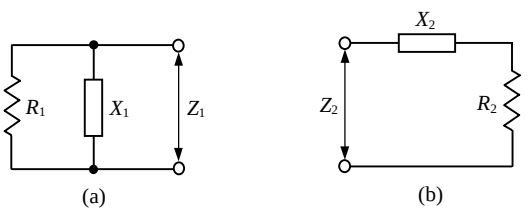


Figure 4.6 Impedance (a) parallel and (b) series equivalent circuits.

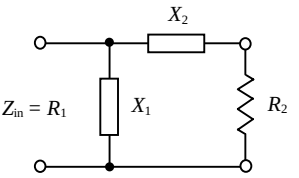


Figure 4.7 Input impedance of two-port network.

are equivalent at some frequency if $Z_1 = Z_2$, that is, when

$$R_2 + jX_2 = \frac{R_1 X_1^2}{R_1^2 + X_1^2} + j\frac{R_1^2 X_1}{R_1^2 + X_1^2} \tag{4.22}$$

Equation (4.22) can be solved as follows:

$$R_1 = R_2(1 + Q^2) \tag{4.23}$$

$$X_1 = X_2(1 + Q^{-2}) \tag{4.24}$$

where $Q = R_1/|X_1| = |X_2|/R_2$ is the quality factor, which is equal for both the series and parallel circuits.

Consequently, if the reactive impedance $X_1 = -X_2(1 + Q^{-2})$ is connected to the series circuit R_2X_2, it allows the reactive impedance of the equivalent parallel circuit to be compensated. The input impedance of the obtained two-port network presented in Fig. 4.7 will be only resistive and equal to R_1. Thus, to transform the resistance R_1 into another resistance R_2 at the given frequency, it is sufficient to connect between them a two-port L-transformer with the opposite signs of the reactances X_1 and X_2 having the following parameters:

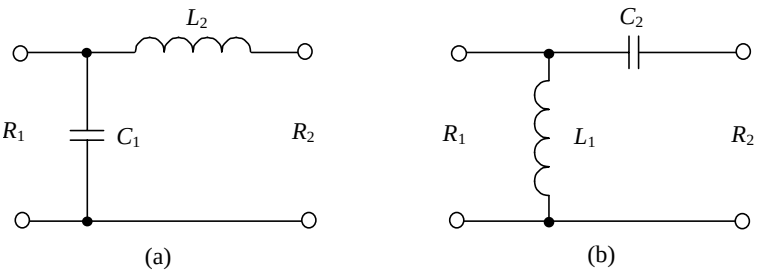
$$\begin{cases} |X_1| = R_1/Q \\ |X_2| = R_2 Q \\ Q = \sqrt{R_1/R_2 - 1} \end{cases} \tag{4.25}$$

Due to the opposite signs of the reactances X_1 and X_2, two possible circuit configurations of the L-transformer with the same transforming properties can be realized (see Fig. 4.8). The following expression allows direct and fast calculation of the parameters of the L-transformers:

$$R_1 R_2 = L/C \tag{4.26}$$

where $C = C_1$, $L = L_2$ for the matching circuit in Fig. 4.8(a), and $L = L_1$, $C = C_2$ for the matching circuit in Fig. 4.8(b).

The matching circuits in the form of the L-transformer loaded on the resistance R_2 can be also considered as the parallel resonant circuit



$$\left.\begin{aligned}\omega C_1 &= Q/R_1\\ \omega L_2 &= QR_2\end{aligned}\right\} \quad Q = \sqrt{\frac{R_1}{R_2} - 1} \quad \left\{\begin{aligned}\omega L_1 &= R_1/Q\\ \omega C_2 &= 1/(QR_2)\end{aligned}\right.$$

Figure 4.8 L-type matching circuits and relevant equations.

shown in Fig. 4.9. The series inductance L_2' and resistance R_2' are the frequency-dependent functions

$$\begin{cases} R_1 = R_2' = R_2(1 + Q^2) \\ L_2' = L_2(1 + Q^{-2}) \end{cases} \tag{4.27}$$

where $Q = \omega L_2/R_2$. The resonant frequency of such an equivalent parallel resonant circuit is determined from the following equation:

$$\omega_0 = 2\pi f_0 = \sqrt{\frac{1}{L_2 C_1} - \left(\frac{R_2}{L_2}\right)^2} \tag{4.28}$$

If this matching circuit has small values of Q, wider frequency bandwidth but poor out-of-band suppression can be achieved. However, with large values of Q the frequency bandwidth is substantially reduced. For the case of $R_1/R_2 \geq 10$, which corresponds to the condition of $Q \geq 3$, the frequency bandwidth $2\Delta f$ and out-of-band suppression factor F_n of such an L-transformer can be evaluated by the same formulas as for a

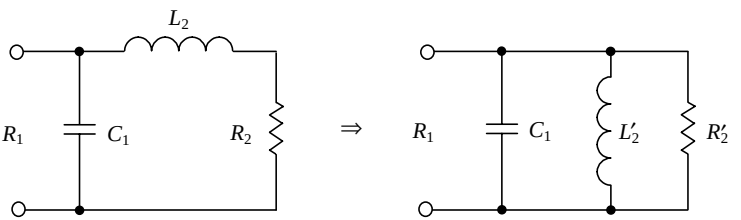


Figure 4.9 Parallel resonant circuit resulting from loading L-transformer.

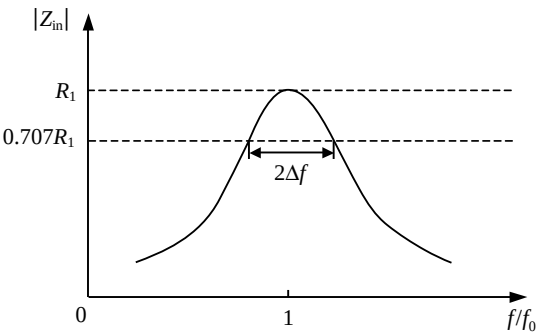


Figure 4.10 Frequency plot of input impedance for parallel resonant circuit.

parallel resonant circuit [3]:

$$\begin{cases} 2\Delta f \cong f_0/Q \\ F_n \cong Q^2(n^2-1) \end{cases} \tag{4.29}$$

where f_0 is the operating frequency and n is the harmonic number. Figure 4.10 shows the frequency behavior of the input impedance magnitude of the parallel resonant circuit $|Z_{in}|$.

The transformer efficiency η_T is determined by the ratio P_L/P_{in}, where P_{in} is the power at the input of the transformer and P_L is the load transformer power. The efficiency for the L-transformer with negligible losses in the capacitor is calculated from the following equation:

$$\eta_T \cong 1/\left(1+\frac{Q}{Q_{ind}}\right) \tag{4.30}$$

where Q_{ind} is the inductor quality factor. From Eq. (4.30) it follows that with the increase of Q the efficiency of the transformer decreases. This means that, for the same R_1 and the series parasitic resistance of the circuit inductance L, the lower resistance R_2 provides the higher current flowing through the inductance, which leads to an additional dissipation. The analysis of Eqs. (4.25) and (4.26) shows that, for the given resistances R_1 and R_2, each parameter of the L-transformer can have only one value. As a result, it is difficult to satisfy simultaneously such contradictory requirements as efficiency, frequency bandwidth, and out-of-band suppression.

To avoid the parasitic low-frequency oscillations and increase the level of the harmonic suppression, it may be necessary to connect an additional $L_f C_f$ series circuit with a resonant frequency equal to the operating frequency of the power amplifier, as shown in Fig. 4.11.

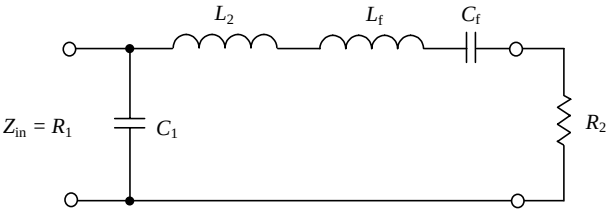


Figure 4.11 L-transformer with additional LC resonant circuit.

It is advisable to use single two-port L-transformers in power amplifiers as the interstage matching circuits, where the requirements for out-of-band suppression and efficiency are not as high as for the matching circuits in the output stages. In this case, the main advantages of such a transformer are that it has only two elements and that simple tuning can be achieved. For larger values of Q, $Q \geq 10$, it is possible to use a cascade connection of L-transformers, which allows wider frequency bandwidth and transformer efficiency to be realized.

The matching circuits in the form of (a) the π-transformer and (b) the T-transformer can be realized by the appropriate connection of two L-transformers, as shown in Fig. 4.12. For each L-transformer the resistances R_1 and R_2 are transformed to some intermediate resistance R_0, with the value of $R_0 < (R_1, R_2)$ for the π-transformer and the value of $R_0 > (R_1, R_2)$ for the T-transformer. The choice of R_0 allows some variation in the quality factor and the matching circuit selectivity. By taking into account the two circuit configurations of the L-transformer shown in Fig. 4.8, it is possible to realize the different circuit configurations of such two-port transformers where $X_3 = X'_3 + X''_3$ in Fig. 4.12(a) and $X_3 = X'_3 X''_3/(X'_3 + X''_3)$ in Fig. 4.12(b).

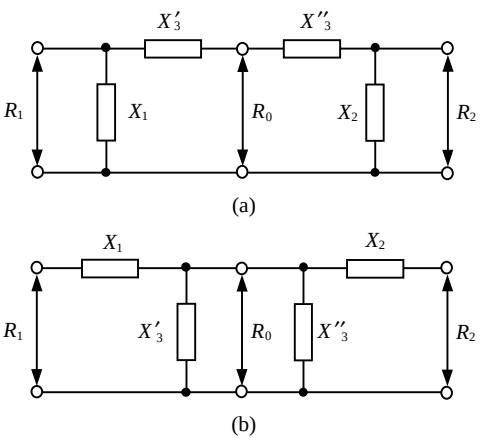
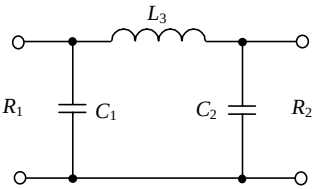


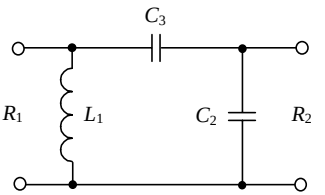
Figure 4.12 Matching circuits developed by connecting two L-transformers.



$$\omega C_1 = Q_1/R_1 \qquad \omega C_2 = Q_2/R_2 \qquad \omega L_3 = R_1(Q_1+Q_2)/\left(1+Q_1^2\right)$$

$$Q_2 = \sqrt{\frac{R_2}{R_1}\left(1+Q_1^2\right)-1} \qquad Q_1^2 > \frac{R_1}{R_2}-1$$

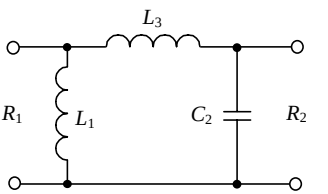
(a)



$$\omega L_1 = R_1/Q_1 \qquad \omega C_2 = Q_2/R_2 \qquad \omega C_3 = \left(1+Q_2^2\right)/\left[R_2(Q_1-Q_2)\right]$$

$$Q_2 = \sqrt{\frac{R_2}{R_1}\left(1+Q_1^2\right)-1} \qquad Q_1^2 > \frac{R_1}{R_2}-1$$

(b)



$$\omega L_1 = R_1/Q_1 \qquad \omega C_2 = Q_2/R_2 \qquad \omega L_3 = R_2(Q_2-Q_1)/\left(1+Q_2^2\right)$$

$$Q_1 = \sqrt{\frac{R_1}{R_2}\left(1+Q_2^2\right)-1} \qquad Q_2^2 > \frac{R_2}{R_1}-1$$

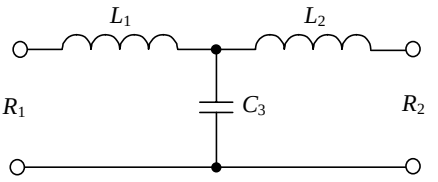
(c)

Figure 4.13 π-transformers and relevant equations.

Several of the most widely used two-port π-transformers, together with the design formulas, are presented in Fig. 4.13 [4]. The π-transformers are usually used as output matching circuits of high power amplifiers in class B operation when it is necessary to achieve a sinusoidal drain or collector voltage waveform by appropriate harmonic suppression. In addition, they are also convenient to use as interstage matching circuits in low-power and medium-power amplifiers when it is necessary to provide sinusoidal voltage waveforms both at the drain

or collector of the previous transistor and at the gate or base of the next transistor. In this case, the input and output capacitances of these transistors can be easily taken into account in the matching circuit elements C_1 and C_2, respectively. Finally, the use of the π-transformers with additional series resonant circuits are very important for high-efficiency class E operation.

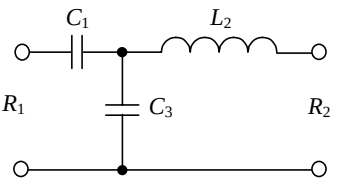
Some of the matching circuit configurations of two-port T-transformers, together with the design formulas, are given in Fig. 4.14 [4].



$$\omega L_1 = Q_1 R_1 \qquad \omega L_2 = Q_2 R_2 \qquad \omega C_3 = \left(Q_1 + Q_2\right)/\left[R_2\left(1+Q_2^2\right)\right]$$

$$Q_1 = \sqrt{\frac{R_1}{R_1}\left(1+Q_2^2\right)-1} \qquad Q_2^2 > \frac{R_1}{R_2} - 1$$

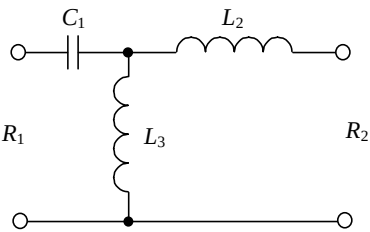
(a)



$$\omega C_1 = 1/\left(R_1 Q_1\right) \qquad \omega L_2 = Q_2 R_2 \qquad \omega C_3 = \left(Q_2 - Q_1\right)/\left[R_2\left(1+Q_2^2\right)\right]$$

$$Q_1 = \sqrt{\frac{R_2}{R_1}\left(1+Q_2^2\right)-1} \qquad Q_2^2 > \frac{R_1}{R_2} - 1$$

(b)



$$\omega C_1 = 1/\left(R_1 Q_1\right) \qquad \omega L_2 = Q_2 R_2 \qquad \omega L_3 = R_2\left(1+Q_2^2\right)/\left(Q_1 - Q_2\right),$$

$$Q_1 = \sqrt{\frac{R_1}{R_2}\left(1+Q_1^2\right)-1} \qquad Q_1^2 > \frac{R_2}{R_1} - 1$$

(c)

Figure 4.14 T-transformers and relevant equations.

The T-transformers are usually used in the high-power amplifiers as input, interstage, and output matching circuits, especially the matching circuit with two capacitances. If a high value of the inductance L_2 is chosen, then the current waveform at the input of the transistor with a small input resistance will be close to sinusoidal. By using such a matching circuit for the output matching of a power amplifier, it is possible to realize a high-efficiency class F operation mode because the series inductance at the drain or collector of the active device creates open circuit harmonic impedance conditions.

If the elements of π- and T-transformers are chosen according to the condition $X_1 = X_2 = -X_3$, then the input transformer impedance loaded by the resistance R_L (from any side) is equal to

$$Z_{in} = R_{in} = X^2/R_L \tag{4.31}$$

where $X = |X_i|, i = 1, 2, 3$. As a result, the input impedance Z_{in} will be resistive, regardless of the magnitude of the load resistance R_L. For example, setting $R_L = R_2$ for the transformers shown in Fig. 4.13(a) and Fig. 4.14(a), yields

$$R_1 = X^2/R_2 \tag{4.32}$$

When $X_1 \neq X_2 \neq -X_3$, the input impedance of the π- and T-transformers will be resistive for only one particular magnitude of R_L.

Bipolar UHF power amplifier

The first design example is a 10 W 300 MHz bipolar power amplifier with a supply voltage of 12.5 V providing a power gain of at least 10 dB. The first step is to select an appropriate active device that allows both simplifying the circuit design procedure (by using the matching circuit with minimum elements) and satisfying the specified requirements. Usually, the manufacturer states the values of the input and output impedances or admittances at the nominal operation point on the data sheet for the device. For example, the above requirements can be realized by an *n-p-n* silicon transistor operating at 300 MHz with $Z_{in} = (1.3 + j0.9)\,\Omega$ and $Y_{out} = (150 - j70)\,\text{mS}$, which is intended for transmitting applications in class AB with nominal supply voltages up to 13.5 V.

In this case, Z_{in} is expressed as a series combination of an input transistor resistance and an inductive reactance. Y_{out} is represented by a parallel combination of an output resistance and an inductive reactance. This means that, for a chosen operating frequency, an influence of the series parasitic collector lead inductance exceeds the influence of the parallel collector capacitance, which gives a net inductive reactance to the equivalent output circuit of an active device. To match the series input inductive impedance to the standard 50 Ω input source impedance,

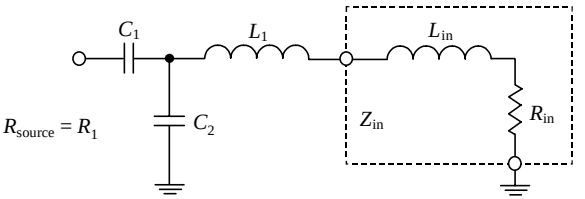


Figure 4.15 Complete input network circuit.

we use a matching circuit in the form of the T-transformer shown in Fig. 4.14(b). Figure 4.15 shows the complete input network including input device impedance and a matching circuit. At the operating frequency of 300 MHz the input inductance will be equal approximately to 0.5 nH.

We first calculate the quality factor Q_2, which is needed to determine the parameters of the matching circuit:

$$Q_2 > \sqrt{R_1/R_{in} - 1} = 6.1$$

The value of Q_2 must be larger than 6.1. For example, $Q_2 = 6.5$ provides the 3-dB bandwidth of 300 MHz/6.5 = 46 MHz. As a result, a value of Q_1 will be equal to 0.35. The values of the input matching circuit parameters are as follows:

$$C_1 = 1/(\omega Q_1 R_1) = 30\,\text{pF}$$

$$L_1 + L_{in} = Q_2 R_{in}/\omega = 4.5\,\text{nH} \Rightarrow L_1 = 4.0\,\text{nH}$$

$$C_2 = (Q_2 - Q_1)/\omega R_{in}\left(1 + Q_2^2\right) = 59\,\text{pF}$$

This type of a T-transformer is used widely in practical matching circuit design because of its simplicity. In addition, a small value of series capacitance C_1 contributes to the elimination of the low-frequency parasitic oscillations in the case of a multistage power amplifier. The function of each element can be traced on the Smith chart, as shown in Fig. 4.16. The easiest and most convenient way to plot the traces of the matching circuit elements is by plotting initially the traces of $Q_2 = 6.5$ and $Q_1 = 0.35$. The circle of equal Q is plotted, taking into account that, for each point located at this circle, a ratio of X/R or B/G must be the same. The trace of the series inductance L_1 must be plotted as far as the intersection point with Q_2-circle. This means that, beginning at Z_{in}, a curve of increasing inductive reactance must be plotted up to the Q_2-circle. The value of L_1 is determined from the normalized inductive impedance at this intersection point. Then, due to 50 Ω normalization, the chart value must be multiplied by factor of 50. The trace of the parallel capacitance C_2 must be plotted using admittance circles.

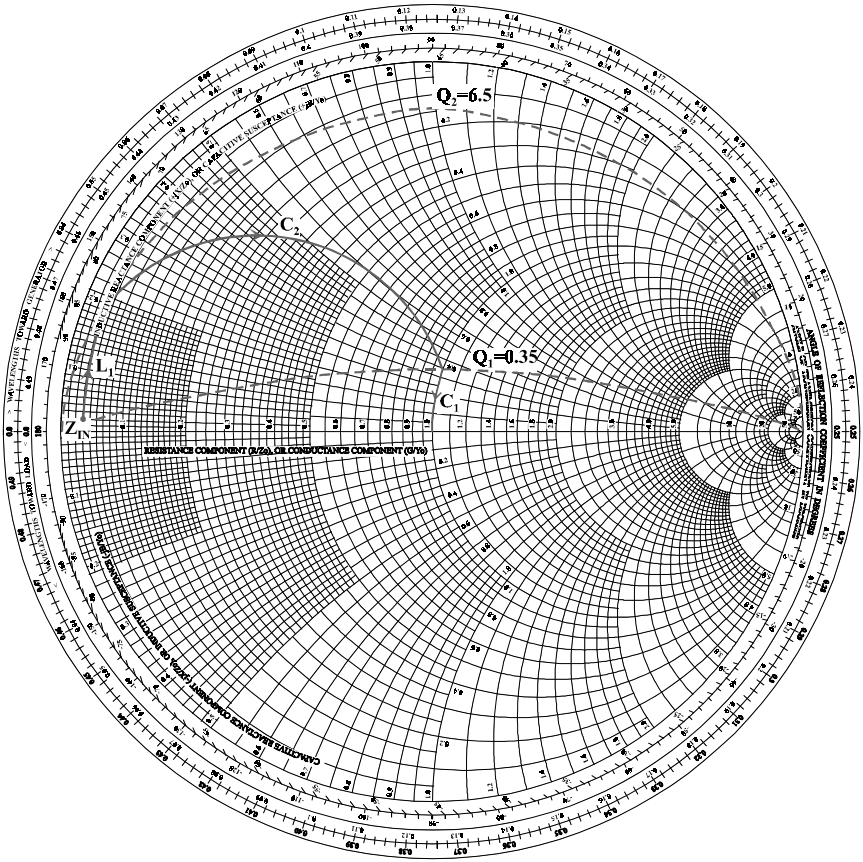


Figure 4.16 Smith chart with elements from Fig. 4.15.

The previous impedance point located at the Q_2-circle is converted to its appropriate admittance one. This point is symmetrical to the impedance point regarding the center point and is located on a straight line from the intersection point drawn through the center of the Smith chart into its lower half at the same distance from the center point. A curve from this point with constant conductance and increasing capacitive susceptance is plotted. These points are transformed to appropriate impedances using a line through the center point extended at an equal distance on the other side and stop when the transformed curve reaches the $Q_1 = 0.35$ circle. In other words, it is necessary to transform mentally or to use a transparent admittance Smith chart (impedance Smith chart rotated on 180°) to plot a curve for C_2 on the upper half of the impedance Smith chart. The difference between the susceptances at the beginning and the end of this curve determines the value of C_2.

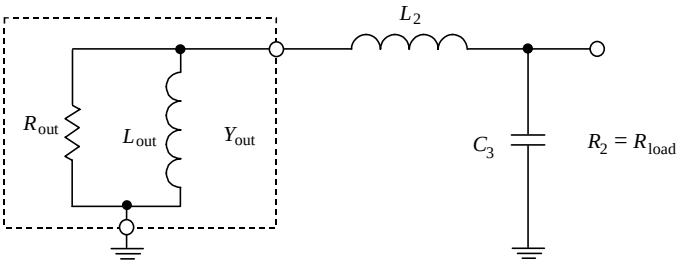


Figure 4.17 Complete output network circuit.

Then, a curve of reducing inductive reactance is plotted down to the center point to determine a value for the series capacitance C_1.

A similar design philosophy can be applied to the design of the output matching circuit shown in Fig. 4.17. However, taking into account the presence of the parallel output inductance, it is advisable to use a matching circuit such as the π-transformer shown in Fig. 4.13(c). The output resistance, collector capacitance, and lead inductance (its influence becomes significant at the higher frequencies) can represent the device output impedance in a common case. The output resistance can be analytically evaluated by

$$R_{\text{out}} = \frac{[V_{\text{cc}} - V_{\text{cc(sat)}}]^2}{2P_{\text{out}}} \cong \frac{(0.9V_{\text{cc}})^2}{2P_{\text{out}}} \cong 6.3\ \Omega$$

where V_{cc} is the supply voltage, $V_{\text{cc(sat)}}$ is the saturation voltage, and P_{out} is the output power, and is practically the same as from the measurement results: $R_{\text{out}} = 1/0.15 = 6.7$ Ohm. A value of L_{out} is approximately equal to 7.6 nH.

The quality factor Q_2 necessary to calculate the parameters of the matching circuit is

$$Q_2 > \sqrt{R_2/R_{\text{out}} - 1} = 2.5$$

The quality factor Q_1 of the device output circuit is

$$Q_1 = R_{\text{out}}/\omega L_{\text{out}} = 0.47$$

This value of L_{out} allows matching to the 50 Ω load impedance with the chosen output matching circuit because

$$Q_2 = \sqrt{\frac{R_2}{R_{\text{out}}}(1 + Q_1^2) - 1} = 2.8 > 2.5$$

As a result, the values of the other two elements of the output

matching circuit are

$$C_3 = Q_2/\omega R_2 = 31 \text{ pF}$$

$$L_2 = R_2(Q_2 - Q_1)/\omega(1 + Q_2^2) = 6.8 \text{ nH}$$

A blocking capacitor that performs dc supply decoupling can be connected after the π-transformer with sufficiently high value of its capacitance to avoid any negative influence on the matching circuit. Alternatively, it can be used in series with the inductance L_2 in order to form a series resonant circuit, as shown in Fig. 4.11. The design of the output circuit using the Smith chart is presented in Fig. 4.18. Initially, it is necessary to transform the output admittance Y_{out} to the output impedance Z_{out} using the straight line of the Smith chart, putting the Z_{out} point at the same distance from the center point as for the Y_{out} point. Then, the effect of increasing series inductance L_2—by moving from the Z_{out} point along the curve of the constant R and increasing X

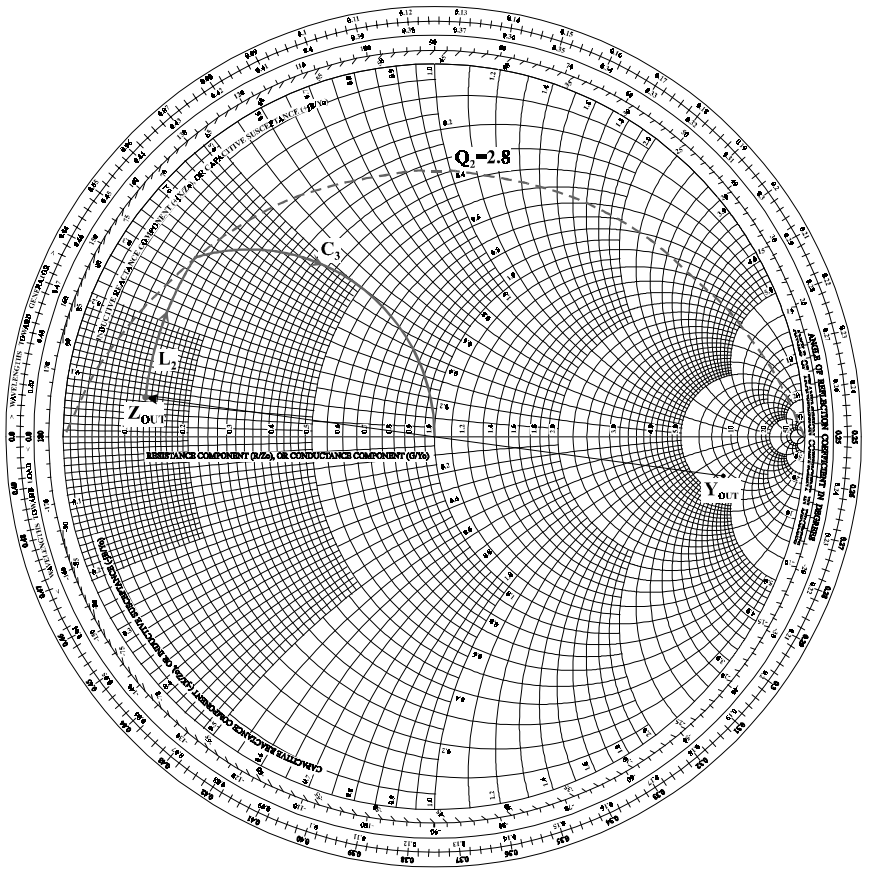


Figure 4.18 Smith chart with elements from Fig. 4.17.

until intersection with the $Q_2 = 2.8$ circle—is plotted. To determine the parallel capacitance C_3, we transform this point to the corresponding admittance one and plot the curve of the constant G and increasing B, which must intersect the center point of the Smith chart.

MOSFET VHF high-power amplifier

A lumped matching circuit technique will be demonstrated by designing a 150 W MOSFET power amplifier with supply voltage 50 V operating in a frequency bandwidth of 132–174 MHz and providing a power gain more than 10 dB. These requirements can be satisfied using a silicon n-channel enhancement mode VDMOS transistor designed for large-signal amplifier applications in the VHF frequency range. The center bandwidth frequency $f_c = \sqrt{132 \cdot 174} = 152$ MHz. For this frequency, the manufacturer states the following values of the input and output impedances: $Z_{in} = (0.9 - j1.2)\,\Omega$ and $Z_{out} = (1.8 + j2.1)\,\Omega$. Both Z_{in} and Z_{out} are expressed as the series combination of input or output resistance and the capacitive or inductive reactance, respectively. To realize the required frequency bandwidth, low-Q matching circuits should be used that allow reduction of the in-band amplitude ripple and improvement to the input *VSWR*. The value of a quality factor for 3-dB level bandwidth must be less than $Q = 152/(174 - 132) = 3.6$. As a result, it is very convenient to design the input and output matching circuits using the simple L-transformers in the form of low-pass and high-pass filter sections with a constant value of Q [5].

To match series input capacitive impedance to the standard 50 Ω source impedance with adequate bandwidth, we use three filter sections (see Fig. 4.19). At the operating frequency of 152 MHz, the input capacitance is equal to approximately 873 pF. To compensate at the center frequency this capacitive reactance, it is enough to connect in series to it an inductance with a value of 1.3 nH. Now, when the device input capacitive reactance is compensated, the design of the input matching circuit can proceed. To simplify the matching design procedure, we cascade L-transformers with equal values of Q. Although equal Q values are not absolutely necessary, this provides a convenient guide for both

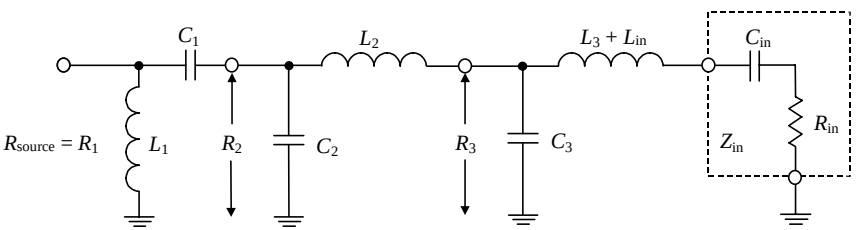


Figure 4.19 Complete broadband input network circuit.

the analytical calculation of matching circuit parameters and the Smith chart graphic design.

In this case, the following ratio can be written for the input matching circuit:

$$\frac{R_1}{R_2} = \frac{R_2}{R_3} = \frac{R_3}{R_{\text{in}}} \tag{4.33}$$

from which we obtain $R_2 = 13\ \Omega$ and $R_3 = 3.5\ \Omega$ for $R_{\text{source}} = R_1 = 50\ \Omega$ and $R_{\text{in}} = 0.9\ \Omega$. Consequently, a quality factor of each L-transformer is equal to a value of $Q = 1.7$. The elements of the input matching circuit using the formulas given in Fig. 4.8 can be calculated as $L_1 = 31$ nH, $C_1 = 47$ pF, $L_2 = 6.2$ nH, $C_2 = 137$ pF, $L_3 = 1.6$ nH, and $C_3 = 509$ pF.

This equal Q approach significantly simplifies the matching circuit design using the Smith chart. When calculating a value of Q, it is necessary to plot a circle of equal Q values on the Smith chart. Then, each element of the input matching circuit can be readily determined, as it is shown in Fig. 4.20. Each trace for the series inductance must be plotted until the intersection point with Q-circle, whereas each trace for the parallel capacitance should be plotted until intersection with the horizontal real axis.

To match series output inductive impedance to the standard 50 Ω load impedance, we use two filter sections, as shown in Fig. 4.21. At the operating frequency of 152 MHz, the transistor output lead inductance will be equal approximately to 2.2 nH. This inductance can be used as a part of L-transformer in the form of low-pass filter section. For an output matching circuit, the condition of equal Q values gives the following ratio:

$$\frac{R_2}{R_1} = \frac{R_1}{R_{\text{out}}} \tag{4.34}$$

with the value of $R_1 = 9.5\ \Omega$ for $R_{\text{load}} = R_2 = 50\ \Omega$ and $R_{\text{out}} = 1.8\ \Omega$. Consequently, a quality factor of each L-transformer is equal to $Q = 2.1$, which is substantially smaller than a value of Q for 3-dB level bandwidth. Now it is necessary to check a value of a series inductance of the low-pass section, which must exceed the value of 2.2 nH for correct matching procedure. The appropriate calculation gives a value of total series inductance $L_4 + L_{\text{out}}$ of approximately 4 nH. As a result, the values of the elements of the output matching circuit are $L_4 = 1.8$ nH, $C_4 = 231$ pF, $C_5 = 52$ pF, and $L_5 = 25$ nH.

The output matching circuit design using the Smith chart with constant Q-circle is shown in Fig. 4.22. For the final high-pass section, a trace for the series capacitance C_5 must be plotted until it intersects the $Q = 2.1$ circle, whereas a trace for the parallel inductance L_5 should be plotted until it intersects the center point of the Smith chart.

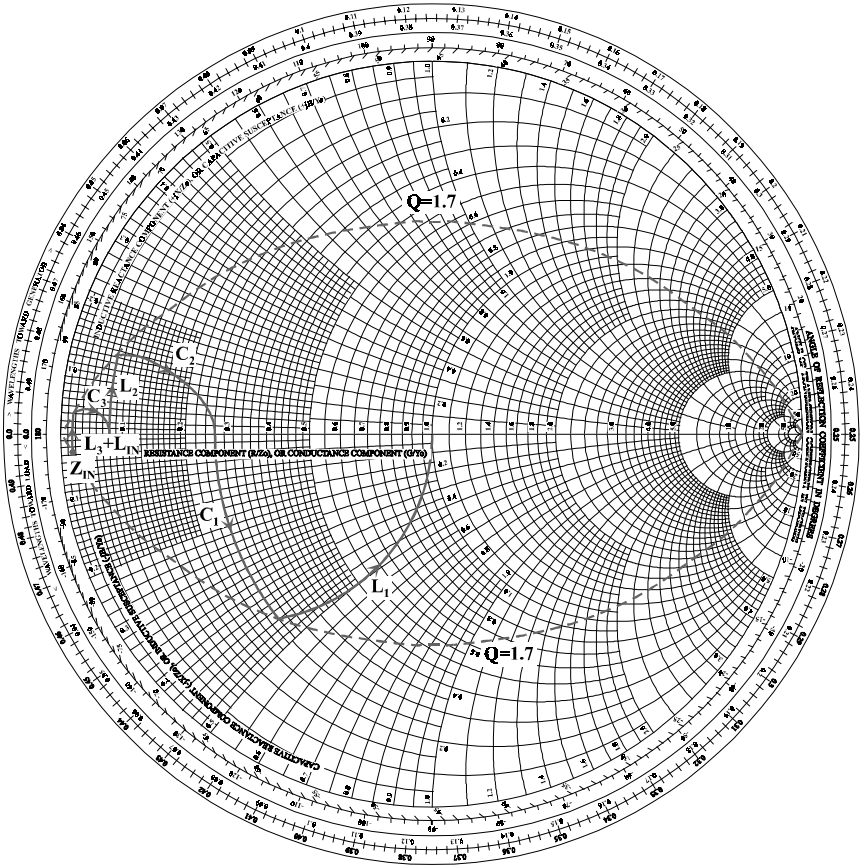


Figure 4.20 Smith chart with elements from Fig. 4.19.

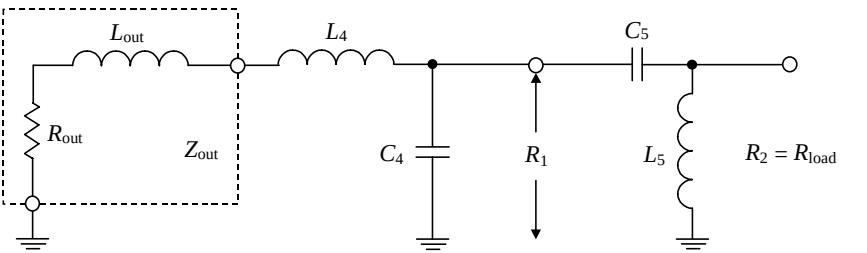


Figure 4.21 Complete broadband output network circuit.

Matching with Transmission Lines [6]

Figure 4.23 shows an impedance matching circuit in the form of a transmission line transformer between the source impedance Z_S and load impedance Z_L. The input impedance as a function of a length of

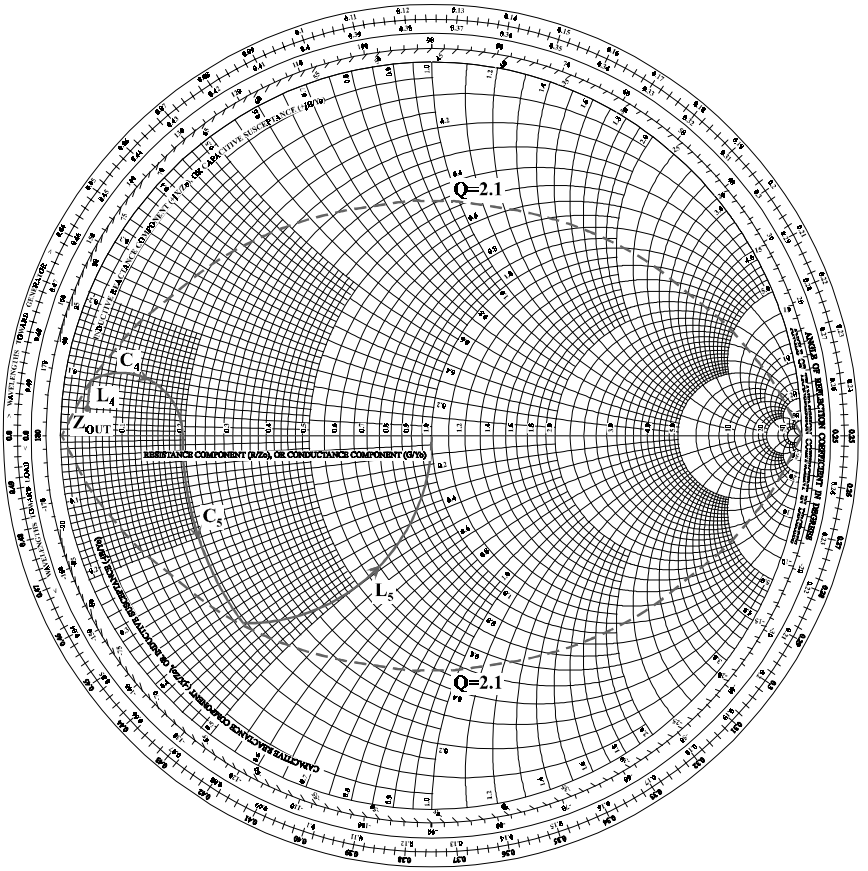


Figure 4.22 Smith chart with elements from Fig. 4.21.

transmission line with arbitrary load impedance is

$$Z_{\text{in}} = Z_0 \frac{Z_{\text{L}} + jZ_0 \tan\theta}{Z_0 + jZ_{\text{L}} \tan\theta} \tag{4.35}$$

where Z_0 is the characteristic impedance, $\theta = \beta l$ is the electrical length of transmission line, $\beta = \frac{\omega}{c}\sqrt{\mu_{\text{r}}\varepsilon_{\text{r}}}$ is the phase constant, c is the speed of

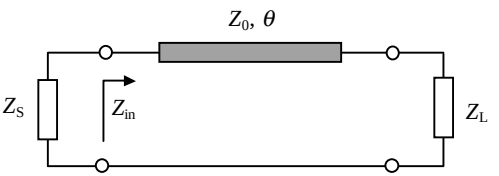


Figure 4.23 Transmission line impedance transformer.

light in free space, μ_r is the substrate permeability, ε_r is the substrate permittivity, ω is the radial frequency, and l is the geometrical length of the transmission line [1, 7].

For a quarter-wavelength transmission line when $\theta = \pi/2$, the expression for Z_{in} is simplified to

$$Z_{in} = Z_0^2/Z_L \tag{4.36}$$

Usually, such a quarter-wavelength impedance transformer is used for impedance matching in a narrow frequency bandwidth of 10 to 20 percent, and its length is chosen at the bandwidth center frequency. However, using a multi-section quarterwave transformer widens the bandwidth and expands the choice of substrate to include materials with high dielectric permittivity, which reduces the transformer's size. For example, consider the case of a 15 W GaAs MESFET power amplifier [8]. It uses a transformer composed of seven quarter-wavelength transmission lines of different characteristic impedances, whose lengths are selected at the highest bandwidth frequency. This design achieved a gain flatness of ±1 dB over 5 to 10 GHz.

To provide a conjugate matching of the input transmission line impedance Z_{in} with the source impedance $Z_S = R_S + jX_S$ when $R_S = \mathrm{Re}Z_{in}$ and $X_S = -\mathrm{Im}Z_{in}$, Eq. (4.35) can be rewritten in the following form:

$$R_S - jX_S = Z_0 \frac{R_L + j(X_L + Z_0 \tan\theta)}{Z_0 - X_L \tan\theta + jR_L \tan\theta} \tag{4.37}$$

For a quarter-wavelength transformer, Eq. (4.37) can be divided into two equations representing the real and imaginary parts of source impedance Z_S:

$$R_S = Z_0^2 \frac{R_L}{R_L^2 + X_L^2} \qquad X_S = -Z_0^2 \frac{X_L}{R_L^2 + X_L^2} \tag{4.38}$$

For a purely active load with $X_L = 0$, a quarter-wavelength transmission line with characteristic impedance Z_0 can provide impedance matching for a purely active source and load only in accordance with

$$Z_0 = \sqrt{R_S R_L} \tag{4.39}$$

Equation (4.37) can be divided into two equations representing the real and imaginary parts as follows:

$$\begin{cases} R_S(Z_0 - X_L \tan\theta) - R_L(Z_0 - X_S \tan\theta) = 0 \\ X_S(X_L \tan\theta - Z_0) - Z_0(X_L + Z_0 \tan\theta) + R_S R_L \tan\theta = 0 \end{cases} \tag{4.40}$$

Solving the system (4.40) for the two independent variables Z_0 and θ yields

$$Z_0 = \sqrt{\frac{R_S(R_L^2 + X_L^2) - R_L(R_S^2 + X_S^2)}{R_L - R_S}} \tag{4.41}$$

$$\theta = \tan^{-1}\left(Z_0 \frac{R_S - R_L}{R_S X_L - X_S R_L}\right) \tag{4.42}$$

As a result, the transmission line with the characteristic impedance Z_0 and electrical length θ, determined by Eqs. (4.41) and (4.42), respectively, can match any source and load impedances when the impedance ratio gives a positive value under the square root expression in Eq. (4.41).

For a purely active source when $Z_S = R_S$, the ratio between the parameters of load and transmission line derived from system (4.40) can be expressed by

$$X_L Z_0(1 - \tan^2\theta) + (Z_0^2 - X_L^2 - R_L^2)\tan\theta = 0 \tag{4.43}$$

Then, for the electrical length of the transmission line having $\theta = \pi/4$, the expression for Z_0 can be simplified to

$$Z_0 = |Z_L| = \sqrt{R_L^2 + X_L^2} \tag{4.44}$$

whereas the required active source impedance R_S should be equal to

$$R_S = R_L \frac{Z_0}{Z_0 - X_L} \tag{4.45}$$

Consequently, any load impedance can be transformed to a real source impedance defined by Eq. (4.45) using a $\lambda/8$ transformer whose characteristic impedance is equal to the magnitude of the load impedance [9].

Applying the same approach to match pure active load with source impedance, the total matching circuit that includes two $\lambda/8$ transformers and a $\lambda/4$ transformer can provide impedance matching between any source impedance Z_S and load impedance Z_L (see Fig. 4.24).

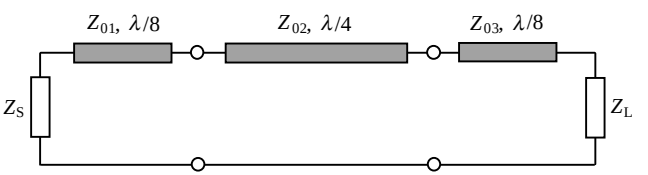


Figure 4.24 Transmission line transformer for any source and load impedances.

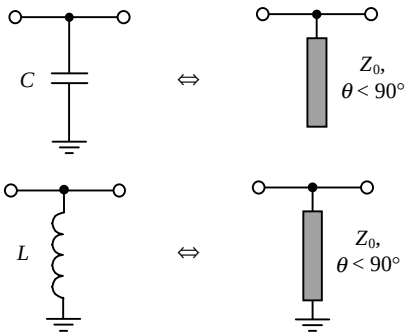


Figure 4.25 Lumped and transmission line single frequency equivalence.

The input impedance of the transmission line at a particular frequency can be expressed as that of a lumped element, as shown in Fig. 4.25. When $Z_L = 0$, it follows that

$$Z_{in} = jZ_0 \tan\theta \tag{4.46}$$

which corresponds to the inductive input impedance for $\theta < \pi/2$. The equivalent inductance at the frequency ω is calculated from

$$L = \frac{X_{in}}{\omega} = \frac{Z_0 \tan\theta}{\omega} \tag{4.47}$$

Similarly, when $Z_L = \infty$,

$$Z_{in} = -jZ_0 \cot\theta \tag{4.48}$$

which corresponds to the capacitive input impedance for $\theta < \pi/2$. The equivalent capacitance at the frequency ω is determined from

$$C = -\frac{1}{\omega X_{in}} = \frac{\tan\theta}{\omega Z_0} \tag{4.49}$$

To calculate the parameters of parallel open-circuited or short-circuited stubs, we use the matching circuit technique with lumped elements. The Smith chart is particularly useful for graphical impedance or admittance solutions. Once the appropriate parallel capacitance or inductance has been determined analytically or by Smith chart, the parameters of parallel open-circuited or short-circuited stubs, the characteristic impedance Z_0, and the electrical length θ, can be directly calculated from Eq. (4.47) for inductance and Eq. (4.49) for capacitance.

Microwave power amplifier design often employs a simple matching circuit such as an L-transformer with a series transmission line as the basic matching section. It is convenient to analyze the transforming properties of this matching circuit by substituting the equivalent transformation of the parallel RX circuit for the series one. For example,

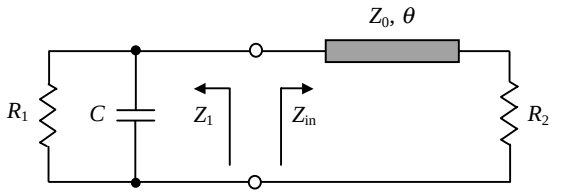


Figure 4.26 L-transformer with series transmission line.

R_1 and $X_1 = -1/\omega C$ are the resistance and reactance of the impedance $Z_1 = jR_1X_1/(R_1 + jX_1)$ for parallel capacitive circuits, and $R_{in} = \mathrm{Re}Z_{in}$ and $X_{in} = \mathrm{Im}Z_{in}$ are the real and imaginary parts of the impedance $Z_{in} = R_{in} + jX_{in}$ for the series circuits presented in Fig. 4.26. For conjugate matching at some frequencies when $Z_1 = Z_{in}^*$, we obtain

$$R_{in} - jX_{in} = \frac{R_1X_1^2}{R_1^2 + X_1^2} + j\frac{R_1^2X_1}{R_1^2 + X_1^2} \tag{4.50}$$

The solution of Eq. (4.50) can be written in the form of two expressions by

$$R_1 = R_{in}(1 + Q^2) \tag{4.51}$$

$$X_1 = -X_{in}(1 + Q^{-2}) \tag{4.52}$$

where $Q = R_1/|X_1| = X_{in}/R_{in}$ is a quality factor that is equal for both parallel capacitive and series transmission line circuits. From Eq. (4.35), the real and imaginary parts of the input impedance Z_{in} can be written as

$$R_{in} = Z_0^2R_2\frac{1 + \tan^2\theta}{Z_0^2 + (R_2\tan\theta)^2} \tag{4.53}$$

$$X_{in} = Z_0\tan\theta\frac{Z_0^2 - R_2^2}{Z_0^2 + (R_2\tan\theta)^2} \tag{4.54}$$

From Eq. (4.54) it follows that an inductive input impedance (necessary to compensate for the capacitive parallel component) is provided when $Z_0 > R_2$ for $\theta < \pi/2$ and $Z_0 < R_2$ for $\pi/2 < \theta < \pi$. As a result, to transform resistance R_1 into another resistance R_2 at the given frequency, it is necessary to connect a two-port L-transformer (including a parallel capacitance and a series transmission line) between them. When one parameter (usually the characteristic impedance Z_0) is known, the matching circuit parameters can be calculated from

the following two equations:

$$C = \frac{Q}{\omega R_1} \tag{4.55}$$

$$\sin 2\theta = \frac{2Q}{\left(\frac{Z_0}{R_2} - \frac{R_2}{Z_0}\right)} \tag{4.56}$$

where Q is defined as a function of resistances R_1 and R_2 as well as the parameters of the transmission line, the characteristic impedance Z_0 and electrical length θ, by the following equation:

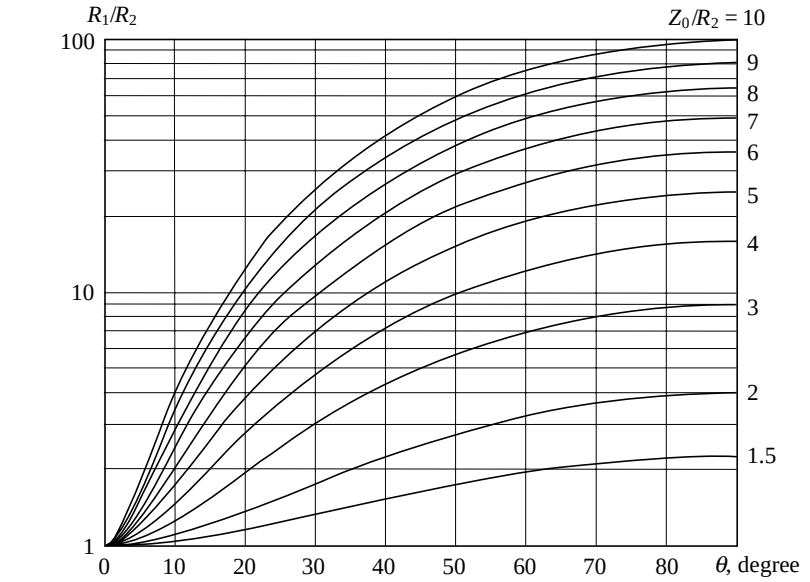
$$Q = \sqrt{\frac{R_1}{R_2}\left[\cos^2\theta + \left(\frac{R_2}{Z_0}\right)^2 \sin^2\theta\right] - 1} \tag{4.57}$$

It follows from Eqs. (4.56) and (4.57) that the calculation of θ is a result of the numerical solution of a transcendental equation with one unknown parameter. However, it is more convenient to combine these two equations and to rewrite them in the form of

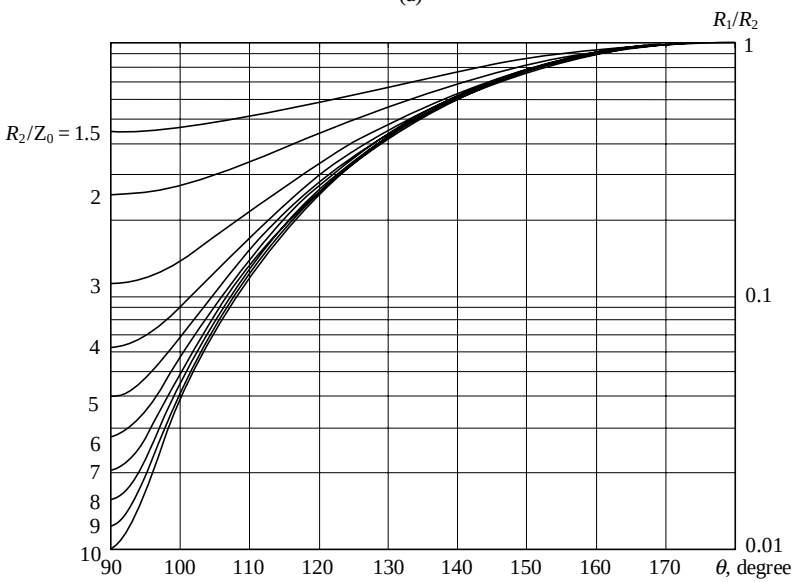
$$\frac{R_1}{R_2} = \frac{1 + \left(\frac{Z_0}{R_2} - \frac{R_2}{Z_0}\right)^2 \sin^2\theta \cos^2\theta}{\cos^2\theta + \left(\frac{R_2}{Z_0}\right)^2 \sin^2\theta} \tag{4.58}$$

Figure 4.27 shows the resistance ratio of R_1/R_2 as a function of the parameter Z_0/R_2 and electrical length θ in the form of two nomographs: (a) one for the case of $Z_0/R_2 > 1$ and (b) another for the case of $Z_0/R_2 < 1$. When input resistance R_1 and output resistance R_2 are known in advance, and when the value of the transmission line characteristic impedance Z_0 is chosen, it is easy to evaluate the required value of θ using these nomographs. The graphical results show that, in contrast to a lumped L-transformer, a simple L-transformer with a transmission line can match a purely resistive source and load impedance with any values of the ratio R_1/R_2.

A π-transformer can be realized by connecting two L-transformers when resistances R_1 and R_2 are transformed to some intermediate resistance R_0 as shown in Fig. 4.28(a). In this case, to minimize the length of transmission line, the value of R_0 should be smaller than that of both R_1 and R_2, i.e., $R_0 < (R_1, R_2)$. The same procedure for a T-transformer shown in Fig. 4.28(b) gives a value of R_0 that is larger than that of both R_1 and R_2, i.e., $R_0 > (R_1, R_2)$. Then, for a T-transformer, two parallel adjacent capacitances are combined. For a π-transformer, two adjacent series transmission lines are combined into one transmission line with total electrical length.



(a)



(b)

Figure 4.27 Nomographs for calculating L-transformer.

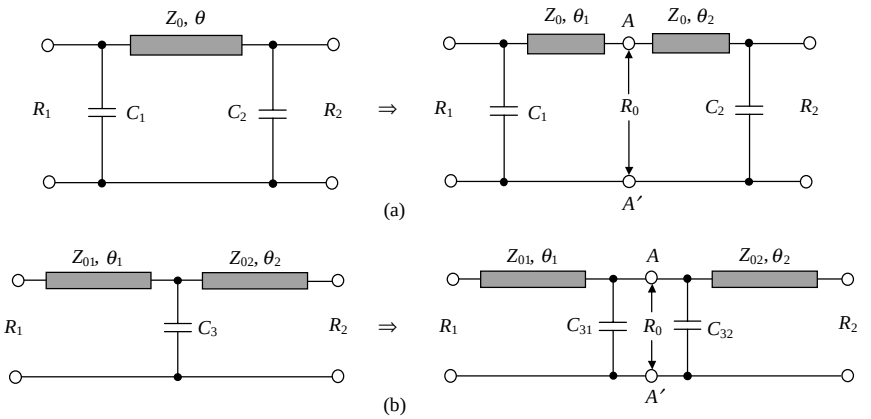


Figure 4.28 T- and π-transformers with transmission lines.

For a π-transformer, the lengths of each part of the combined transmission line can be calculated by equating the imaginary parts of the impedances from both sides at the reference plane A–A' to zero, which means that the intermediate impedance R_0 is real. This leads to two quadratic equations for each electrical length of the combined series transmission lines as variables in the form of

$$\tan^2\theta_1 - \frac{R_1}{Z_0 Q_1}\left[1 - \left(1 + Q_1^2\right)\left(\frac{Z_0}{R_1}\right)^2\right]\tan\theta_1 - 1 = 0 \qquad (4.59)$$

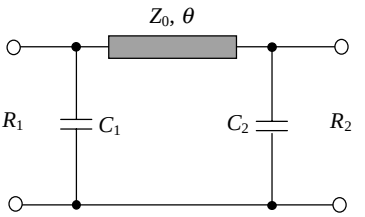
$$\tan^2\theta_2 - \frac{R_2}{Z_0 Q_2}\left[1 - \left(1 + Q_2^2\right)\left(\frac{Z_0}{R_2}\right)^2\right]\tan\theta_2 - 1 = 0 \qquad (4.60)$$

where $Q_1 = \omega C_1 R_1$, $Q_2 = \omega C_2 R_2$.

To simplify this analytical calculation procedure, it is best to use the nomographs shown in Fig. 4.27. If the values of R_1 and R_2 are selected in advance to set the intermediate resistance R_0, and the characteristic impedance of the transmission line Z_0 is known, the values of θ_1 and θ_2 can be easily determined from one of these nomographs.

A widely used two-port π-transformer, along with its design formulas, is presented in Fig. 4.29. Such a transformer is used as the output matching circuit of high power amplifiers in class B operation to provide sinusoidal voltage drain or collector waveform by appropriate harmonic suppression. Moreover, it is convenient to use this transformer as an input matching circuit in high power push–pull amplifiers where capacitances can be connected between series transmission lines.

A two-port T-transformer with series transmission line and two capacitances, along with the design formulas, is given in Fig. 4.30.



$$\omega C_1 = Q_1/R_1 \qquad \omega C_2 = Q_2/R_2 \qquad \theta = \theta_1 + \theta_2$$

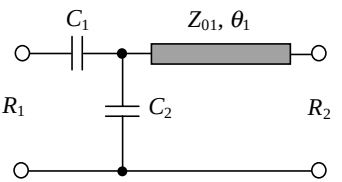
$$Q_2 = \sqrt{\frac{R_2}{R_1}\left(1 + Q_1^2\right) - 1} \qquad Q_1 > \sqrt{\frac{R_1}{R_2} - 1}$$

Figure 4.29 Transmission-line π-transformer and equations.

Narrow-band power amplifier design

This example illustrates a transmission line matching circuit technique through the design of an output matching circuit for a 5 W 1.6 GHz bipolar power amplifier that operates from a 24 V supply voltage and provides about 10 dB power gain. These requirements can be provided with an *n-p-n* silicon microwave transistor intended for transmitting applications in class AB operation for a frequency range of 1.5 to 1.7 GHz. At the operating frequency of 1.6 GHz, let $Z_{\text{out}} = (5.5 - j6.5)\ \Omega$, which corresponds to a series combination of the transistor output resistance and capacitance. To match this capacitive impedance to the standard 50 Ω load resistance, we use a matching circuit in the form of a T-transformer shown in Fig. 4.30. Figure 4.31 shows the complete two-port network including output device impedance and matching circuit.

The circuit should compensate for the series capacitance inherent in the output impedance. For a small electrical length where $\tan\theta \cong \theta$ and the characteristic impedance $Z_0 >> R_{\text{out}}$, we can deduce from Eqs. (4.53)



$$\omega C_1 = 1/(R_1 Q_1) \qquad \sin 2\theta_1 = 2Q_2/\left(\frac{Z_{01}}{R_2} - \frac{R_2}{Z_{01}}\right) \qquad \omega C_2 = (Q_2 - Q_1)/\left[R_1\left(1 + Q_1^2\right)\right]$$

$$Q_1 = \sqrt{\frac{R_2}{R_1}\frac{1 + Q_2^2}{\cos^2\theta_1 + (R_2/Z_{01})\sin^2\theta_1} - 1} \qquad Q_2 > \sqrt{\frac{R_1}{R_2} - 1}$$

Figure 4.30 Transmission-line T-transformer and equations.

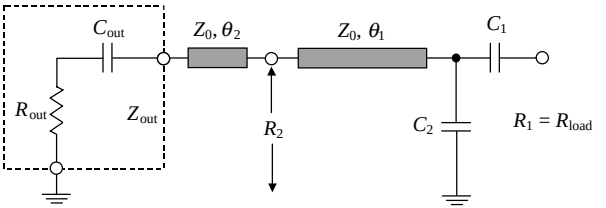


Figure 4.31 Complete output two-port network circuit.

and (4.54) that

$$\begin{cases} R_{\text{out}} \cong R_2 \\ \theta_2 \cong -X_{\text{out}}/Z_0 = 1/\omega C_{\text{out}} Z_0 \end{cases} \tag{4.61}$$

where θ_2 is a part of the total transmission line that is required to compensate for the output capacitance reactance. If Z_0 is chosen to be 50 Ω, then $\theta_2 = 6.5/50 = 0.13$ radians, which is equal to approximately 7.5° of electrical length. Then, the value of quality factor Q_2 is defined by

$$Q_2 > \sqrt{R_1/R_2 - 1} = 2.84$$

The value of Q_2 must be larger than 2.84. For example, a value of $Q_2 = 3$ can be chosen to yield a 3-dB bandwidth of 1.6 GHz/3 = 533 MHz. The values of the output matching circuit parameters are

$$\theta_1 = \frac{1}{2}\sin^{-1}\left[2Q_2/\left(\frac{Z_0}{R_2} - \frac{R_2}{Z_0}\right)\right] = 21^\circ$$

$$Q_1 = \sqrt{\frac{R_2}{R_1}\frac{1+Q_2^2}{\cos^2\theta_1 + (R_2/Z_0)^2\sin^2\theta_1} - 1} = 0.5$$

$$C_1 = 1/(\omega Q_1 R_1) = 4\,\text{pF}$$

$$C_2 = (Q_2 - Q_1)/\omega R_1\left(1 + Q_1^2\right) = 4\,\text{pF}$$

The function of each element for visual effect can be traced on the Smith chart (see Fig. 4.32). The easiest and most convenient way to plot the traces of the matching circuit elements is to first plot the traces of Q_1 and Q_2, then plot the trace of the series transmission line as far as the intersection point with the Q_2-circle, and plot the trace of capacitance C_2 as far as the intersection point with the Q_1-circle. The plot of the series transmission line represents an arc of the circle with center point at the center of the Smith chart.

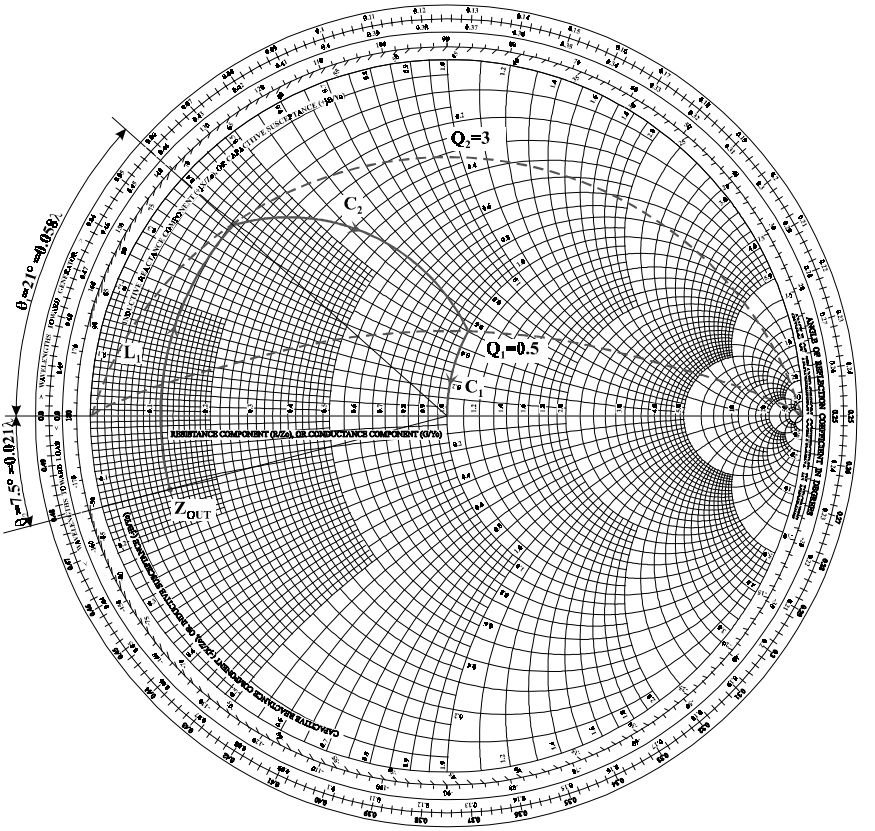


Figure 4.32 Smith chart with elements from Fig. 4.31.

Broadband high-power amplifier design

This example shows the design of a 150 W broadband power amplifier that operates over a frequency bandwidth of 470 to 860 MHz, uses a 28 V supply voltage and provides a power gain of more than 10 dB. A typical application for such a circuit is a high-power balanced LDMOS transistor designed for UHF TV transmitters. The center bandwidth frequency f_c is $f_c = \sqrt{470 \cdot 860} = 635$ MHz. For this operating frequency, assume that the manufacturer states the value of input impedance for each transistor-balanced part of $Z_{in} = (1.7 + j1.3)\,\Omega$. The input impedance Z_{in} is expressed as a series combination of input resistance and inductive reactance. To realize the required frequency bandwidth, low-Q matching circuits should be used to reduce in-band amplitude ripple and improve input *VSWR*. To achieve a 3-dB bandwidth, the value of a quality factor must be less than $Q = 635/(860 - 470) = 1.63$. Since the device input quality factor is smaller, that is, $Q_{in} = 1.3/1.7 = 0.76$,

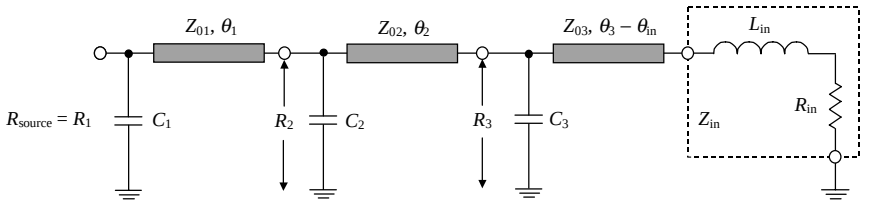


Figure 4.33 Complete broadband input two-port network circuit.

it is possible to cover the entire frequency range using a multistage matching circuit. It is very convenient to design the input and output matching circuits by using simple L-transformers in the form of series transmission lines and parallel capacitances with a constant value of Q for each balanced part of the active device. The two matching circuits are then combined by inserting capacitances, the values of which are reduced twice, between the two series transmission lines.

To match the series input inductive impedance to the standard 50 Ω source impedance, we use three L-transformers, as shown in Fig. 4.33. At the center frequency of 635 MHz, the input inductance is equal approximately to 0.3 nH. Taking this inductance into account, we subtract the appropriate value of electrical length θ_{in} from the total electrical length θ_3. Due to the short size of this transmission line, a value of θ_{in} can be easily calculated in accordance with

$$\theta_{in} \cong X_{in}/Z_0 = \omega L_{in}/Z_0 \tag{4.62}$$

In this case, the input resistance R_{in} can be assumed to be constant.

According to Eq. (4.57), there are two simple possibilities to provide matching using equal quality factors of L-transformers. One option is to use the same values of characteristic impedance for all transmission lines; the other is to use the same electrical lengths for all transmission lines. Consider the first approach, which also allows direct use of Smith chart, and choose the value of the characteristic impedance $Z_0 = Z_{01} = Z_{02} = Z_{03} = 50$ Ω. The ratio of input and output resistances can be written as

$$\frac{R_1}{R_2} = \frac{R_2}{R_3} = \frac{R_3}{R_{in}} \tag{4.63}$$

which gives the values of $R_2 = 16.2$ Ω and $R_3 = 5.25$ Ω for $R_{source} = R_1 = 50$ Ω and $R_{in} = 1.7$ Ω. The values of the electrical lengths are determined from the nomograph shown in Fig. 4.27(a) as $\theta_1 = 30^\circ$, $\theta_2 = 7.5^\circ$, and $\theta_3 = 2.4^\circ$.

To calculate the quality factor Q from Eq. (4.57), it is enough to know the electrical length θ_1 of the first L-transformer The remaining two electrical lengths can be directly obtained from Eq. (4.56). As a result,

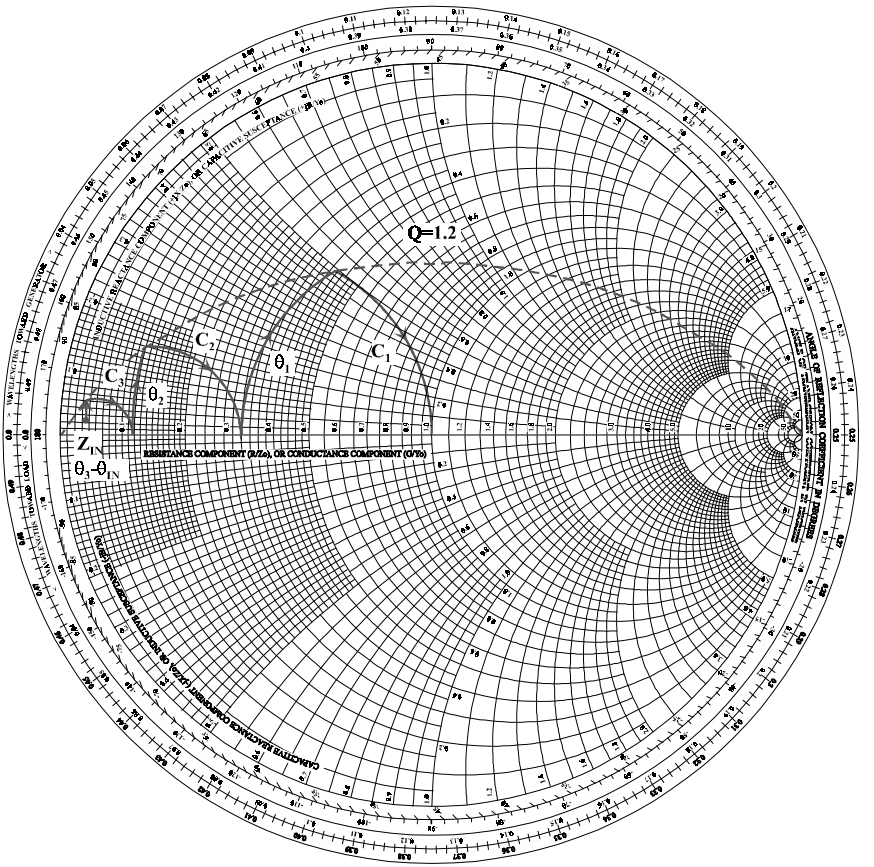


Figure 4.34 Smith chart with elements from Fig. 4.33.

the quality factor of each L-transformer is $Q = 1.2$. The values of the parallel capacitances are $C_1 = 6$ pF, $C_2 = 19$ pF, and $C_3 = 57$ pF.

For a constant Q, we can simplify significantly the design of the matching circuit by using the Smith chart. After calculating the value of Q, we plot a constant Q-circle on the Smith chart. Figure 4.34 shows the matching circuit design using the Smith chart with a constant Q-circle, where the curves for the series transmission lines represent the arcs of the circles with center points at the center of the Smith chart. The capacitive traces are moved along the circles with increasing susceptances and constant conductances.

Another approach assumes the same values of electrical lengths $\theta = \theta_1 = \theta_2 = \theta_3$ and calculates the characteristic impedances of transmission lines from Eq. (4.57) at equal ratios of the input and output resistances according to Eq. (4.63). Such an approach is more convenient

in practical design, because, when using the transmission lines with standard characteristic impedance $Z_0 = 50\ \Omega$, the electrical length of the transmission line adjacent to the active device input terminal is too short. In this case, it is advisable to set the characteristic impedance of the first series transmission line to $Z_{01} = 50\ \Omega$. Then, a value of θ should be calculated directly from the nomograph shown in Fig. 4.27(a). Subsequent calculation of Q from Eq. (4.56) yields $\theta = 30^\circ$ and $Q = 1.2$. The characteristic impedances of the remaining two transmission lines are calculated easily from Eq. (4.56) or Eq. (4.57). The values are $Z_{02} = 15.7\ \Omega$ and $Z_{03} = 5.1\ \Omega$.

Types of Transmission Line

Several types of transmission line are available when designing RF and microwave power amplifiers. Coaxial lines have very high bandwidth and high power-handling capabilities and are widely used for transformers and power combiners. Planar transmission lines are compact, can be easily integrated with active devices and are usually used as matching circuit elements and for hybrids and directional couplers.

Coaxial line

A main type of wave propagated along a coaxial line shown in Fig. 4.35 is the *transverse electromagnetic* (TEM) wave. When the transverse fields of a TEM wave are the same as the static fields that can exist between the conductors, the electromagnetic properties of a coaxial line can be characterized by the following parameters [7, 10]:

The shunt capacitance per unit length, F/m,

$$C = 2\pi\varepsilon / \ln\left(\frac{b}{a}\right) \tag{4.64}$$

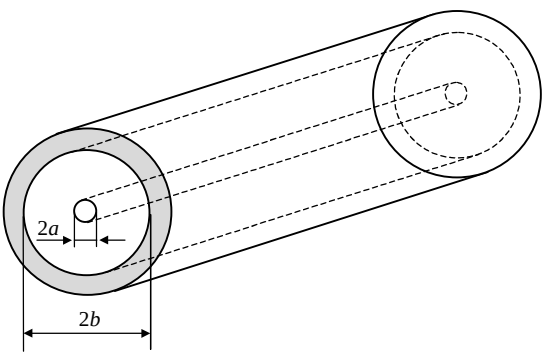


Figure 4.35 Coaxial line schematic.

where $\varepsilon = \varepsilon_o \varepsilon_r$, $\varepsilon_o = 8.854 \times 10^{-12}$ F/m is the permittivity of free-space, ε_r is the relative dielectric constant or substrate permittivity, a is a radius of inner conductor, and b is the inner radius of the outer conductor:

The series inductance per unit length, H/m,

$$L = \frac{\mu}{2\pi} \ln\left(\frac{b}{a}\right) \tag{4.65}$$

where $\mu = \mu_o \mu_r$, $\mu_o = 4\pi \times 10^{-7}$ H/m is the permeability of free space, and μ_r is the relative magnetic constant or substrate permeability.

The series resistance per unit length, Ω/m,

$$R = \frac{R_s}{2\pi}\left(\frac{1}{b} + \frac{1}{a}\right) \tag{4.66}$$

where $R_s = \rho/\Delta(f) = \sqrt{\pi \mu_o \rho f}$ is the surface resistivity, ρ is the metallization electrical resistivity, $\Delta(f)$ is the penetration depth, and f is the frequency.

The shunt conductance per unit length, S/m,

$$G = 2\pi\sigma / \ln\left(\frac{b}{a}\right) = 2\pi\omega\varepsilon_o\varepsilon_r \tan\delta / \ln\left(\frac{b}{a}\right) \tag{4.67}$$

where σ is the dielectric conductivity, $\tan\delta$ is the dielectric loss tangent.

The characteristic impedance in Ω,

$$Z_0 = \frac{\eta}{2\pi} \ln\left(\frac{b}{a}\right) \tag{4.68}$$

where $\eta = \sqrt{\mu/\varepsilon}$ is the wave impedance of the lossless coaxial line identical to the intrinsic impedance of the medium.

The conductor loss factor can be presented by

$$\alpha_c = R/2Z_0 \text{ N/m} \tag{4.69}$$

and the dielectric loss factor by

$$\alpha_d = GZ_0/2 = \sigma\eta/2 = \pi\sqrt{\varepsilon_r}\tan\delta/\lambda_0 \text{ N/m} \tag{4.70}$$

where λ_0 is the free-space wavelength.

The total loss factor α expressed through decibel per meter (dB/m) can be calculated as

$$\alpha = 8.686(\alpha_c + \alpha_d) \tag{4.71}$$

Stripline

The geometry of a commonly used stripline is shown in Fig. 4.36. The strip conductor of width W is placed between two flat dielectric

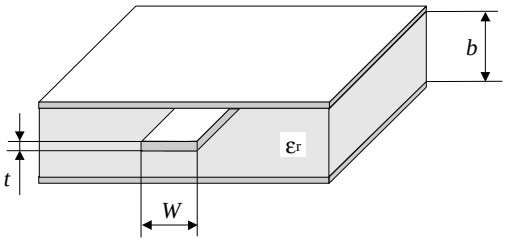


Figure 4.36 Stripline schematic.

substrates with the same dielectric constant. The outer surfaces of these substrates are metallized and serve as ground conductor. In practice, the strip conductor is etched on one of the dielectric substrates by a photolithography process. Since the stripline has two conductors and a homogeneous dielectric, it can support a pure TEM propagation mode, which is the usual mode of operation.

The exact expression for the characteristic impedance of a lossless stripline of zero thickness is [11, 12]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{K(k)}{K(k')} \tag{4.72}$$

where $k = \operatorname{sech}(\pi W/2b)$, $k' = \sqrt{1-k^2}$, and K is the complete elliptic integral of the first kind,

$$K(k) = \int_0^{\pi/2} \frac{d\varphi}{\sqrt{1-k^2\sin^2\varphi}} \tag{4.73}$$

An approximate expression for the ratio $K(k)/K(k')$ with the relative error lower than $3 \cdot 10^{-6}$ is given by [13]

$$\frac{K(k)}{K(k')} = \begin{cases} \pi / \ln\left(2\dfrac{1+\sqrt{k'}}{1-\sqrt{k'}}\right) & \text{for} \quad 0 \le k \le \dfrac{1}{\sqrt{2}} \\ \dfrac{1}{\pi} \ln\left(2\dfrac{1+\sqrt{k}}{1-\sqrt{k}}\right) & \text{for} \quad \dfrac{1}{\sqrt{2}} \le k \le 1 \end{cases} \tag{4.74}$$

In practice, it is advisable to use a sufficiently simple formula without complicated special functions. So, the formula for Z_0 within 1 percent of the exact results can be simplified to [7, 14]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{b}{W_e + 0.441b} \tag{4.75}$$

where W_e is the effective width of the center conductor defined by

$$\frac{W_e}{b} = \frac{W}{b} - \begin{cases} 0 & \text{for} \quad \dfrac{W}{b} > 0.35b \\ \left(0.35 - \dfrac{W}{b}\right)^2 & \text{for} \quad \dfrac{W}{b} \le 0.35b \end{cases} \tag{4.76}$$

For a stripline with a TEM propagation mode, the dielectric loss factor α_d is the same as for coaxial line, which is determined by Eq. (4.70). An approximation result for the conductor loss factor α_c, in dB/m, can be presented by [7]

$$\alpha_c = \begin{cases} A\dfrac{2.7 \times 10^{-3} R_s \varepsilon_r Z_0}{30\pi(b-t)} & \text{for} \quad Z_0\sqrt{\varepsilon_r} \le 120 \\ B\dfrac{0.16 R_s}{Z_0 b\pi} & \text{for} \quad Z_0\sqrt{\varepsilon_r} \ge 120 \end{cases} \tag{4.77}$$

where t is the thickness of the strip,

$$A = 1 + \frac{2W}{b-t} + \frac{1}{\pi}\frac{b+t}{b-t}\ln\frac{2b-t}{t}$$

$$B = 1 + \frac{b}{0.5W + 0.7t}\left(0.5 + \frac{0.414t}{W} + \frac{1}{2\pi}\ln\frac{4\pi W}{t}\right)$$

Figure 4.37 illustrates the characteristic impedance Z_0 of a stripline as a function of the normalized strip width W/b for various values of ε_r according to Eqs. (4.75) and (4.76).

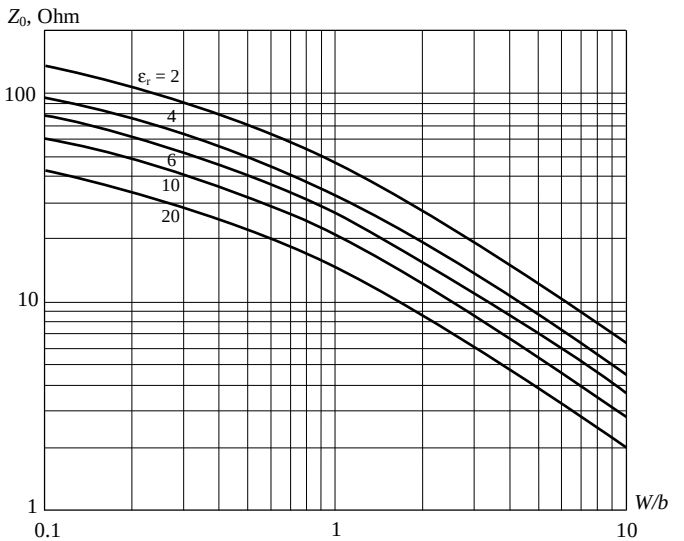


Figure 4.37 Stripline characteristic impedance versus W/b.

TABLE 4.1 Electrical and Thermal Properties of Substrate Materials

Typical substrate	Dielectric constant, ε_r @ 10 GHz	Loss tangent, $\tan\delta$ @ 10 GHz	Coefficient of thermal expension (CTE), ppm/°C
Alumina 99.5%	9.8	0.0003	6.7
Aluminum nitride	8.7	0.001	4.5
Barium tetratitanade	37	0.0002	8.3
Beryllia 99.5%	6.6	0.0003	7.5
Epoxy glass FR-4	4.7	0.01	3.0
Fused quartz	3.78	0.0001	0.5
Gallium arsenide	13.1	0.0006	6.5
Silicon	11.7	0.004	4.2
Teflon	2.5	0.0008	12

Typical values of the main electrical and thermal properties of some substrate materials are presented in Table 4.1.

Microstrip line

In a microstrip line, the grounded metallization surface covers only one side of the dielectric substrate, as shown in Fig. 4.38. In this case, the electric and magnetic field lines are located in both the dielectric region between the strip conductor and the ground plane and in the air region above the substrate. As a result, the electromagnetic wave propagated along a microstrip line is not a pure TEM, since the phase velocities in these two regions are not the same. But in a quasistatic approximation, which gives sufficiently accurate results as long as the height of the dielectric substrate is very small compared with the wavelength, it is possible to obtain the analytical expressions for the electrical characteristics.

The exact expression for the characteristic impedance of a lossless microstrip line with finite strip thickness is [15]

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_{re}}} \ln\left(\dfrac{8h}{W_e} + \dfrac{W_e}{4h}\right) & \text{for} \quad \dfrac{W}{h} \le 1 \\ \dfrac{120\pi}{\sqrt{\varepsilon_{re}}} \left[\dfrac{W_e}{h} + 1.393 + 0.667 \ln\left(\dfrac{W_e}{h} + 1.444\right)\right]^{-1} & \text{for} \quad \dfrac{W}{h} \ge 1 \end{cases} \tag{4.78}$$

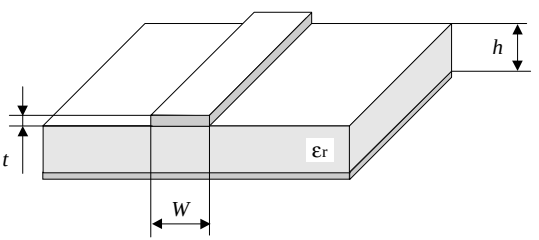


Figure 4.38 Microstrip line schematic.

where

$$\frac{W_e}{h} = \frac{W}{h} + \frac{\Delta W}{h}$$

$$\frac{\Delta W}{h} = \begin{cases} \dfrac{1.25}{\pi}\dfrac{t}{h}\left(1 + \ln\dfrac{4\pi W}{t}\right) & \text{for} \quad \dfrac{W}{h} \le 1/2\pi \\ \dfrac{1.25}{\pi}\dfrac{t}{h}\left(1 + \ln\dfrac{2h}{t}\right) & \text{for} \quad \dfrac{W}{h} \ge 1/2\pi \end{cases}$$

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + 12h/W}} - \frac{\varepsilon_r - 1}{4.6}\frac{t}{h}\sqrt{\frac{h}{W}}$$

Figure 4.39 shows the characteristic impedance Z_0 of a microstrip line with zero strip thickness as a function of the normalized strip width W/h for various values of ε_r according to Eq. (4.78).

In practice, it can be possible to use a sufficiently simple formula to calculate the characteristic impedance Z_0 of a microstrip line with zero strip thickness in the form of [1]

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_r}}\frac{h}{W}\frac{1}{1 + 1.735\varepsilon_r^{-0.0724}(W/h)^{-0.836}} \tag{4.79}$$

For a microstrip line in a quasi-TEM approximation, the conductor loss factor α_c in dB/m as a function of the microstrip line geometry can

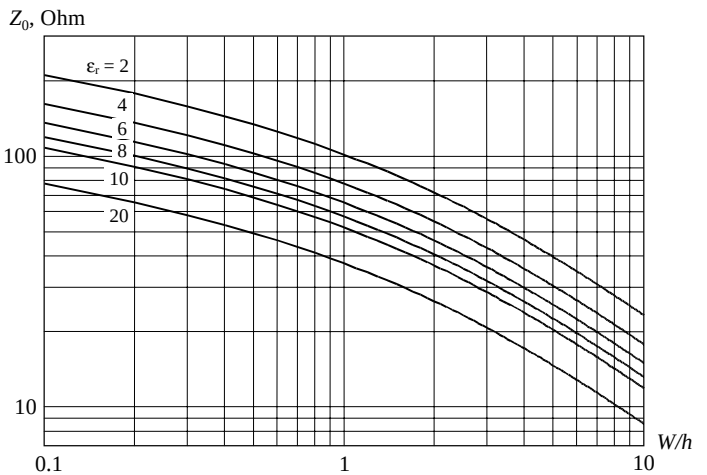


Figure 4.39 Microstrip characteristic impedance versus W/h.

TABLE 4.2 Electrical Resistivity of Conductor Materials

Material	Symbol	Electrical resistivity, μΩ · cm	Material	Symbol	Electrical resistivity, μΩ · cm
Aluminum	Al	2.65	Palladium	Pd	10.69
Copper	Cu	1.67	Platinum	Pt	10.62
Gold	Au	2.44	Silver	Ag	1.59
Indium	In	15.52	Tantalum	Ta	15.52
Iron	Fe	9.66	Tin	Sn	11.55
Lead	Pb	21.0	Titanium	Ti	55.0
Molybdenum	Mo	5.69	Tungsten	W	5.6
Nickel	Ni	8.71	Zink	Zn	5.68

be determined by [16]

$$\alpha_c = \begin{cases} 1.38A\dfrac{R_s}{hZ_0}\dfrac{32-(W_e/h)^2}{32+(W_e/h)^2} & \text{for} \quad \dfrac{W}{h} \le 1 \\ 6.1\cdot 10^{-5}A\dfrac{R_s Z_0 \varepsilon_{re}}{h}\left(\dfrac{W_e}{h}+\dfrac{0.667W_e/h}{1.444+W_e/h}\right) & \text{for} \quad \dfrac{W}{h} \ge 1 \end{cases} \tag{4.80}$$

where W_e/h is defined from Eq. (4.78),

$$A = 1+\frac{h}{W_e}\left(1+\frac{1}{\pi}\ln\frac{2B}{t}\right)$$

$$B = \begin{cases} 2\pi W & \text{for} \quad \dfrac{W}{h} \le 1/2\pi \\ h & \text{for} \quad \dfrac{W}{h} \ge 1/2\pi \end{cases}$$

The dielectric loss factor α_d in dB/m can be calculated by

$$\alpha_d = 27.3\frac{\varepsilon_r}{\varepsilon_r-1}\frac{\varepsilon_{re}-1}{\sqrt{\varepsilon_{re}}}\frac{\tan\delta}{\lambda_0} \tag{4.81}$$

For most microstrip lines (except some kinds of semiconductor substrates), the conductor loss is much more significant than the dielectric loss. The electrical resistivity of some conductor materials is shown in Table 4.2.

Slotline

Slotlines are usually used when it is necessary to realize a high value of the characteristic impedance Z_0. A slotline is dual to a microstrip line and represents a narrow slot between two conductive surfaces, one of which is grounded. Changing the width of the slot can easily change

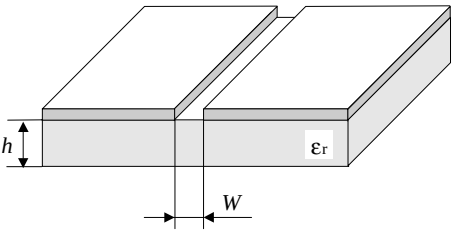


Figure 4.40 Slotline schematic.

the characteristic impedance of the slotline. The transverse electric H mode wave propagates along the slotline. The geometry of a slotline is shown in Fig. 4.40.

It is difficult to provide exact analytical expressions to calculate the slotline parameters. However, an equation for Z_0 can be obtained for a quasi-TEM approximation with zero conductor thickness and infinite width of the entire slotline system [17]:

For $0.02 \le W/h \le 0.2$

$$Z_0 = 72.62 - 15.283 \ln \varepsilon_r + 50\left(1 - 0.02\frac{h}{W}\right)\left(\frac{W}{h} - 0.1\right) + (19.23 - 3.693 \ln \varepsilon_r) \ln\left(10^2 \frac{W}{h}\right) - \left(11.4 - 2.636 \ln \varepsilon_r - 10^2 \frac{h}{\lambda_0}\right)^2 \times \left[0.139 \ln \varepsilon_r - 0.11 + \frac{W}{h}(0.465 \ln \varepsilon_r + 1.44)\right] \tag{4.82}$$

For $0.2 \le W/h \le 1.0$

$$Z_0 = 113.19 - 23.257 \ln \varepsilon_r + 1.25\frac{W}{h}(114.59 - 22.531 \ln \varepsilon_r) + 20\left(1 - \frac{W}{h}\right)\left(\frac{W}{h} - 0.2\right) - \left[0.15 + 0.1 \ln \varepsilon_r + \frac{W}{h}(0.899 \ln \varepsilon_r - 0.79)\right] \times \left[10.25 - 2.171 \ln \varepsilon_r + \frac{W}{h}(2.1 - 0.617 \ln \varepsilon_r) - 10^2 \frac{h}{\lambda_0}\right]^2 \tag{4.83}$$

where $0.01 \le h/\lambda_0 \le 0.25/\sqrt{\varepsilon_r - 1}$.

In Fig. 4.41, the characteristic impedance Z_0 of a slotline within the error of 2 percent as a function of normalized slot width W/h for $h/\lambda_0 = 0.02$ and various values of $\varepsilon_r = 9.7, 11, 12, \ldots, 20$ calculated by Eqs. (4.82) and (4.83) is shown.

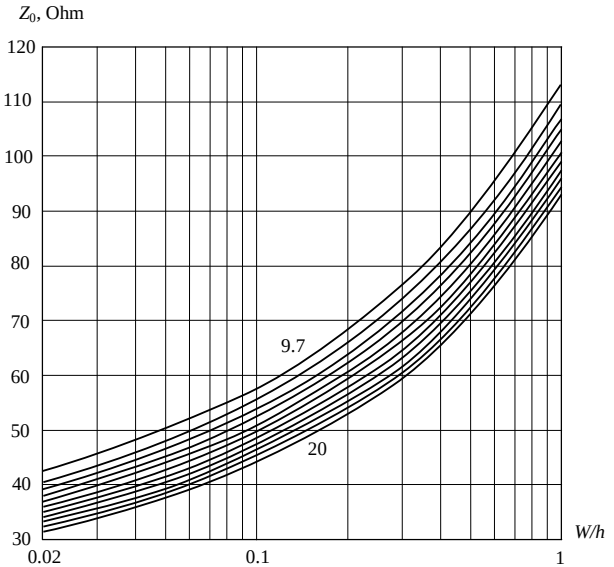


Figure 4.41 Slotline characteristic impedance versus W/h.

Coplanar waveguide

A coplanar waveguide is similar in structure to a slotline, the only difference being a third conductor centered in the slot region. The center strip conductor and two outer grounded conductors lie in the same plane, as shown in Fig. 4.42. A coplanar configuration has some advantages, which makes a coplanar waveguide suitable for hybrid and monolithic integrated circuits, including active devices. A coplanar waveguide can be also described by a quasi-TEM approximation for both numerical and analytical calculations.

The approximate expression of the characteristic impedance Z_0 for zero metal thickness and infinite width of the dielectric substrate

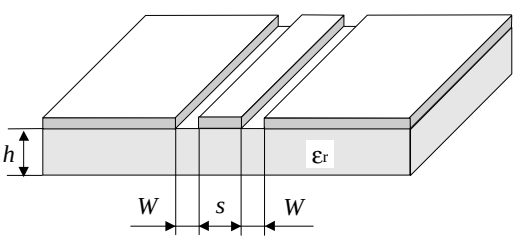


Figure 4.42 Coplanar waveguide schematic.

is [18]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{K(k')}{K(k)} \tag{4.84}$$

$$\varepsilon_{re} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')} \tag{4.85}$$

where $k = \frac{s}{s+2W}$, $k_1 = \frac{\sinh \pi s}{4h} / \sinh \frac{\pi(s+2W)}{4h}$, $k' = \sqrt{1-k^2}$, $k_1' = \sqrt{1-k_1^2}$, and K is the complete elliptic integral of the first kind. The values of the ratios $K(k)/K(k')$ and $K(k_1)/K(k_1')$ can be defined from Eq. (4.74).

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Chapter

5

Power Combiners, Impedance Transformers and Directional Couplers

It is critical, particularly at higher frequencies, that special types of combiner and divider are used to avoid insufficient power performance of the individual active devices. The method of configuration for combiners and dividers differs depending on the operating frequency, frequency bandwidth, output power, and size requirements. Coaxial cable combiners with ferrite cores are used to combine the output powers of RF power amplifiers intended for wideband applications. The device output impedance is usually too small for high power levels so to match this impedance with a standard 50-Ω load coaxial line transformers with specified impedance transformation are used. For narrow-band applications, the *N*-way Wilkinson combiners are widely used due to their simple practical realization. For microwaves, the size of the combiners should be very small and, therefore, the hybrid microstrip combiners (including different types of the microwaves hybrids and directional couplers) are commonly used to combine the output powers of power amplifiers. In this chapter, the basic properties of three-port and four-port networks are presented, as well as a variety of different combiners, transformers and directional couplers for RF and microwave power applications.

Basic Properties

Basic three-port or four-port networks can be used to divide the output power of a single power source or to combine the output powers of two or more power amplifiers. Generally, the multiport network required to

combine the output powers of N identical power amplifiers is based on these basic networks. If this is the case, it is very important to match all power amplifiers with the load to provide an overall output power that is N times larger than the output power of single power amplifier. Changes in the operation condition of one power amplifier should not affect the operation conditions of the remaining power amplifiers. To satisfy this requirement, all of the input ports of the combiner should be decoupled (mutually independent). When one of the power amplifiers is eliminated, the total output power must decrease by as little as possible. In addition, the combiners can be used for both narrow-band and broadband transmitters, in the latter case requiring that their electrical characteristics are provided for a wide frequency bandwidth.

Three-Port Networks

The simplest devices used for power division and combination are the three-port networks having one input and two outputs in the power divider shown in Fig. 5.1(a) and two inputs and one output in the power combiner shown in Fig. 5.1(b). The scattering S-matrix of an arbitrary three-port network can be written by

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{5.1}$$

where $S_{ij} = S_{ji}$ for the symmetric scattering S-matrix when all components are passive and reciprocal. In this case, if all ports are appropriately matched (when $S_{ii} = 0$) the scattering, S-matrix is reduced to

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & S_{23} \\ S_{13} & S_{23} & 0 \end{bmatrix} \tag{5.2}$$

A lossless condition applied to a fully matched S-matrix given in Eq. (5.2) requires it to be a unitary matrix when

$$[S]^* [S] = 1 \tag{5.3}$$

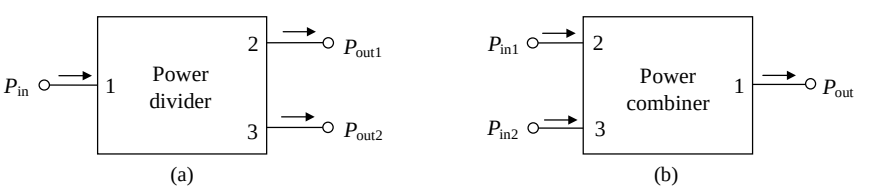


Figure 5.1 Schematic diagrams of (a) power divider and (b) power combiner.

where $[S]^*$ is the matrix complex conjugated to the original S-matrix [1, 2]. As a result of multiplying two matrices, it follows that

$$|S_{12}|^2 + |S_{13}|^2 = |S_{12}|^2 + |S_{23}|^2 = |S_{13}|^2 + |S_{23}|^2 = 1 \tag{5.4}$$

$$S_{13}^* S_{23} = S_{23}^* S_{12} = S_{12}^* S_{13} = 0 \tag{5.5}$$

From Eq. (5.5) it follows that at least two of the three available parameters S_{12}, S_{13} and S_{23} should be zero, which is inconsistent with at least one condition given by Eq. (5.4). This means that a three-port network cannot be lossless, reciprocal and matched at all ports. However, if any one of these three conditions is not fulfilled, a physically realizable device is possible for practical implementation. A lossless and reciprocal three-port network can be realized if only two of its ports are matched, or, in the case of the resistive divider, if the three-port network is reciprocal and fully matched at all three ports but it is lossy.

If a reciprocal three-port network represents the 3-dB power divider when, for a given input power at port 1, the output powers at ports 2 and 3 are equal, then according to Eq. (5.4)

$$|S_{12}| = |S_{13}| = \frac{1}{\sqrt{2}} \tag{5.6}$$

Four-Port Networks

The four-port networks are used for directional power coupling when, for a given input signal at port 1, the output signals are delivered to ports 2 and 3 and no power is delivered to port 4 (ideal case), as shown in Fig. 5.2. The scattering S-matrix of a reciprocal four-port network matched at all its ports is given by

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} & S_{14} \\ S_{12} & 0 & S_{23} & S_{24} \\ S_{13} & S_{23} & 0 & S_{34} \\ S_{14} & S_{24} & S_{34} & 0 \end{bmatrix} \tag{5.7}$$

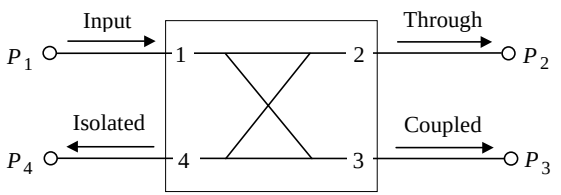


Figure 5.2 Schematic diagram of directional coupler.

where $S_{ij} = S_{ji}$ for the symmetric scattering S-matrix when all components are passive and reciprocal. In this case, the power supplied to the input port 1 is coupled to the coupled port 3 with coupling factor $|S_{13}|^2$, whereas the remainder of the input power is delivered to the through port 2 with coefficient $|S_{12}|^2$.

For a lossless four-port network, the unitary condition of the fully matched S-matrix given by Eq. (5.7) results in

$$|S_{12}|^2 + |S_{13}|^2 = |S_{12}|^2 + |S_{24}|^2 = |S_{13}|^2 + |S_{34}|^2 = |S_{24}|^2 + |S_{34}|^2 = 1 \quad (5.8)$$

which implies a full isolation between ports 2 and 3 and ports 1 and 4, respectively, when

$$S_{14} = S_{41} = S_{23} = S_{32} = 0 \quad (5.9)$$

and that

$$|S_{13}| = |S_{24}| \qquad |S_{12}| = |S_{34}| \quad (5.10)$$

The scattering S-matrix of such a directional coupler, matched at all its ports with two decoupled two-port networks, reduces to

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} & 0 \\ S_{12} & 0 & 0 & S_{24} \\ S_{13} & 0 & 0 & S_{34} \\ 0 & S_{24} & S_{34} & 0 \end{bmatrix} \quad (5.11)$$

The directional coupler can be classified according to the phase shift ϕ between two output ports 2 and 3 as the in-phase coupler with $\phi = 0$, quadrature coupler with $\phi = \pi/2$ and out-of-phase coupler with $\phi = \pi$. The following important quantities are used to characterize the directional coupler:

- The power-split ratio or power division ratio K^2, which is calculated as the ratio of power at the output ports when all ports are nominally (reflectionless) terminated

$$K^2 = \frac{P_2}{P_3}$$

- The insertion loss C_{12}, which is calculated as the ratio of power at the output port 2 relative to the input port 1

$$C_{12} = 10 \log_{10} \frac{P_1}{P_2} = -20 \log_{10} |S_{12}|$$

- The coupling C_{13}, which is calculated as the ratio of power at the output port 3 relative to the input port 1

$$C_{13} = 10\log_{10}\frac{P_1}{P_3} = -20\log_{10}|S_{13}|$$

- The directivity C_{34}, which is calculated as the ratio of power at the output port 3 relative to the isolated port 4

$$C_{34} = 10\log_{10}\frac{P_3}{P_4} = 20\log_{10}\frac{|S_{13}|}{|S_{14}|}$$

- The isolations C_{14} and C_{23}, which are calculated as the ratio of power at the input port 1 relative to the isolated port 4 and between the two output ports (output port 2 is considered as an input port), respectively,

$$C_{14} = 10\log_{10}\frac{P_1}{P_4} = -20\log_{10}|S_{14}|$$

$$C_{23} = 10\log_{10}\frac{P_2}{P_3} = -20\log_{10}|S_{23}|$$

- The voltage standing wave ratio at each port or $VSWR_{\rm i}$, where $i = 1$, 2, 3, 4, calculated as

$$VSWR_{\rm i} = \frac{1+|S_{\rm ii}|}{1-|S_{\rm ii}|}$$

In an ideal case, the directional coupler would have $VSWR_{\rm i} = 1$ at each port, insertion loss $C_{12} = 3$ dB, coupling $C_{13} = 3$ dB, infinite isolation and directivity $C_{14} = C_{23} = C_{34} = \infty$.

Coaxial Cable Transformers and Combiners

The coaxial cable transformers and combiners provide the wideband frequency operation of the RF power amplifiers [3, 4]. Figure 5.3(a) shows the schematic configuration of a coaxial cable transformer, which consists of the coaxial line arranged inside the ferrite core or wound around the ferrite core. A coaxial cable transformer, whose equivalent circuit is shown in Fig. 5.3(b), is commonly called a *balun*. Due to its practical configuration, the coaxial cable transformer takes a position between the lumped and distributed systems. Therefore, at lower frequencies its equivalent circuit represents a conventional low-frequency transformer [see Fig.5.3(c)], while at higher frequencies it is a transmission line with the characteristic impedance Z_0 shown in Fig. 5.3(d). The advantage of such a transformer is that the parasitic interturn capacitance determines its characteristic impedance, whereas in the conventional wire-wound

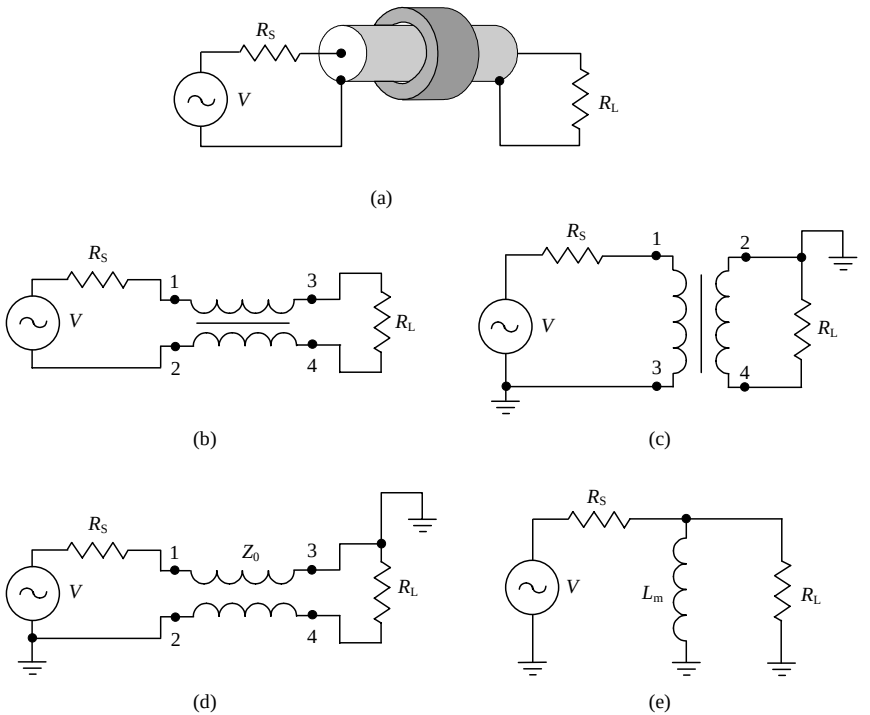


Figure 5.3 Schematic configurations of coaxial cable transformer.

transformer with discrete windings this parasitic capacitance negatively contributes to the transformer's frequency performance.

When $R_S = R_L = Z_0$, the transmission line can considered to be a transformer with 1:1 impedance transformation. To avoid any resonant phenomena, especially for complex loads, which can contribute substantially to the amplitude ripple increase, the length of the transmission line should be chosen from the condition of

$$l \leq \frac{\lambda_{\min}}{8} \tag{5.12}$$

where $\lambda_{\min}$ is the minimum wavelength in the transmission line corresponding to the high bandwidth frequency $f_{\max}$.

The low-frequency response of a transformer at lower frequencies is degraded by a shunt susceptance between the inner and outer conductors shown in Fig. 5.3(e) due to the magnetizing inductance L_m, which is given by

$$L_m = 4\pi n^2 \mu \frac{A_e}{L_e} \tag{5.13}$$

where

n = number of turns
μ = core permeability
A_e = effective area of the core
L_e = average magnetic path length [3]

Considering the equivalent circuit shown in Fig. 5.3(e), the ratio between the power delivered to the load P_L and power available at the source $P_S = V^2/8R_S$ when $R_S = R_L$ can be obtained from

$$\frac{P_L}{P_S} = \frac{4(\omega L_m)^2}{R_S^2 + 4(\omega L_m)^2} \tag{5.14}$$

which gives the minimum operating frequency f_{min} for a given magnetizing inductance L_m, taking into account the maximum decrease of the output power by 3 dB, as

$$f_{min} \geq \frac{R_S}{4\pi L_m} \tag{5.15}$$

To choose the appropriate ferrite core commonly used in RF transformers, it is necessary to know the flux level for core saturation and nonlinearity. So, the maximum flux density determined at the lowest operation frequency can be calculated from

$$B = \frac{V_{rms}}{4.44 f n A_e} \cdot 10^8, \text{ gauss} \tag{5.16}$$

where

V_{rms} = rms voltage on the winding
n = number of turns
f = operating frequency
A_e = effective area of the core in square centimeters [3]

Figure 5.4 shows the two 2:1 transformer configurations using coaxial lines, which can provide a 4:1 impedance transformation. A current I driven into the inner conductor of the upper line in Fig. 5.4(a) produces a current I that flows in the outer conductor of the upper line, resulting in a current $2I$ flowing into the load R_L. Because the voltage $2V$ from the input voltage source is divided into two equal parts between coaxial line and the load, such a transformer provides an impedance transformation from $R_S = 2Z_0$ into $R_L = Z_0/2$, where Z_0 is the characteristic impedance of each coaxial line. A ferrite core is necessary only for the upper line because the outer conductor of the lower line is grounded at both ends and no current is flowing through it. Since all points of the inner conductor of the lower line have the same potentials, it is advisable to connect directly the left point of the outer conductor to the right point of the inner conductor of the upper line.

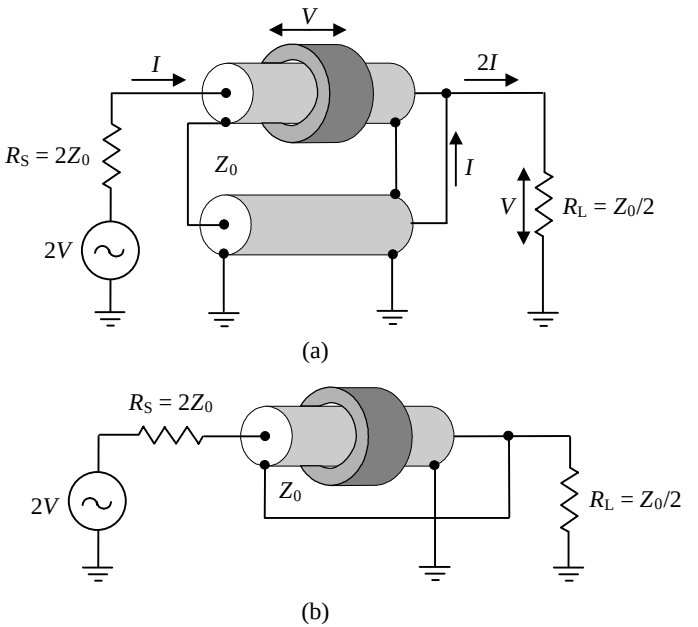


Figure 5.4 Schematic configuration of 2:1 cable transformer.

Thus the lower coaxial line can be removed and a 2:1 coaxial line transformer can be put in place, as shown in Fig. 5.4(b). At lower frequencies, such a transformer can be considered to be an ordinary 1:2 autotransformer. However, at higher frequencies, the lower line provides an in-phase combination of output voltages and is called a *phase-compensating line*.

Figure 5.5 shows similar arrangements for the 3:1 coaxial line transformers, which produce 9:1 impedance transformations. A current I driven into the inner conductor of the upper line in Fig. 5.5(a) will cause a current I to flow in the outer conductor of the upper line. This current then produces a current I in the outer conductor of the lower line, resulting in a current $3I$ flowing into the load R_L. The lowest coaxial line can be removed, resulting in a 3:1 coaxial line transformer shown in Fig. 5.5(b). The characteristic impedance of each transmission line is specified by the voltage applied to the end of the line and the current flowing through the line.

By using the coaxial line transformers with different integer transformation ratios in certain connections, we can obtain the fractional transformation ratio [4]. For example, for the overall 1:3/2-transformer configuration, it is necessary to provide the cascade connection of a 1:3 transformer to increase impedance by 9 times, and a 2:1 transformer to decrease the impedance by 4 times, as shown schematically

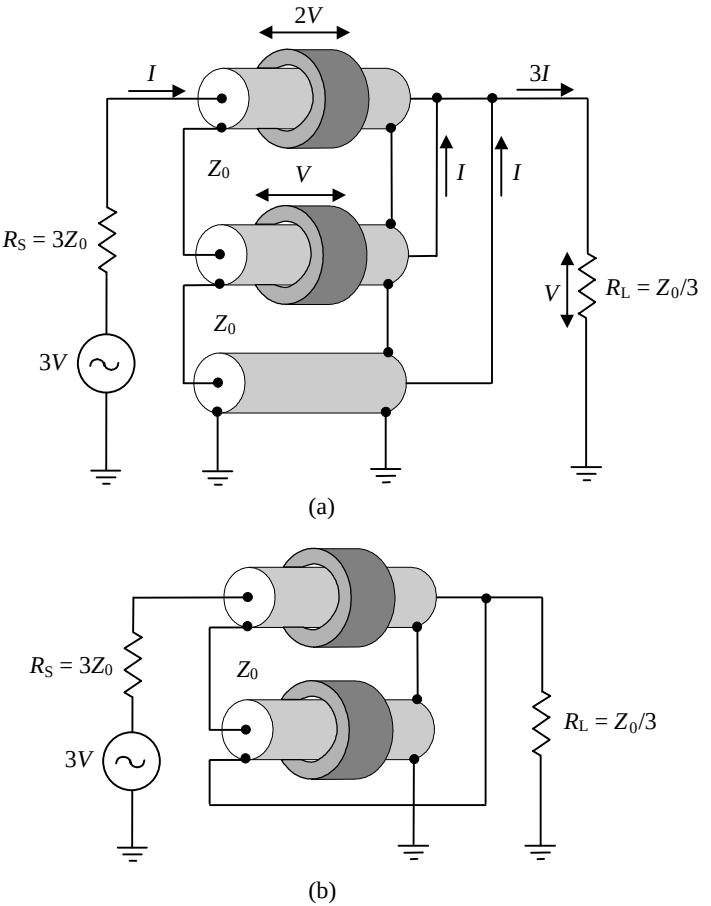
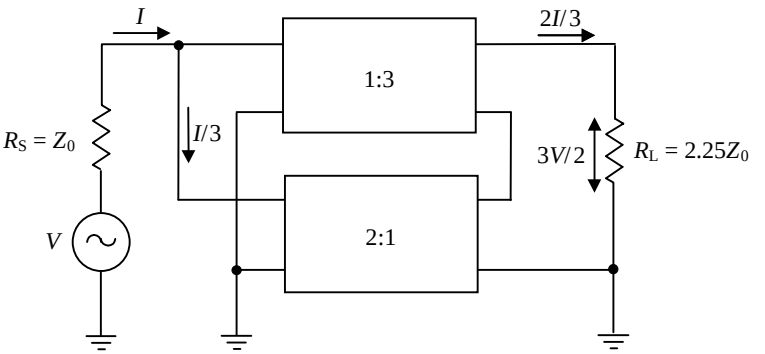


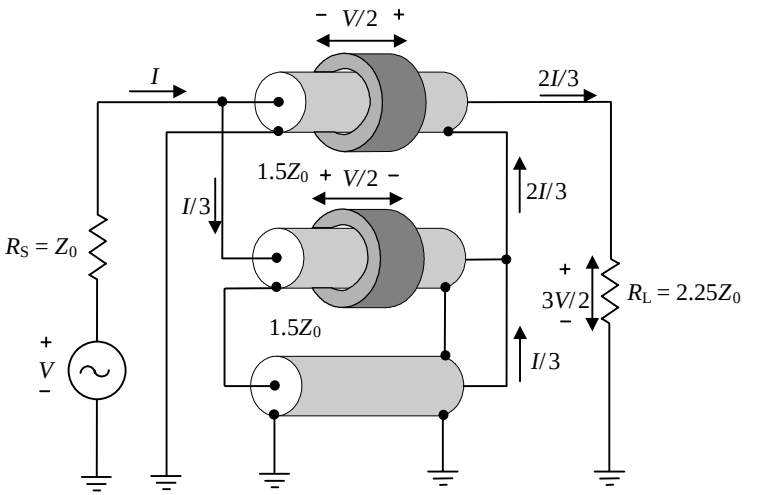
Figure 5.5 Schematic configurations of 3:1 cable transformer.

in Fig. 5.6(a). The practical configuration using coaxial cables with ferrite cores is shown in Fig. 5.6(b). The lowest line also can be eliminated with direct connection of the points at both ends of its inner conductor, as in the case of the 2:1 or 3:1 transformers shown in Figs. 5.4 and 5.5. Here, the currents $I/3$ in the inner conductors of the two lower lines cause an overall current $2I/3$ in the outer conductor of the upper line, resulting in a current $2I/3$ flowing into the load R_L. A load voltage $3V/2$ is out of phase with a longitudinal voltage $V/2$ along the upper line, resulting in a source voltage V.

Figure 5.7 shows the circuit arrangement with two coaxial line transformers combined to provide push-pull operation of the power amplifiers. Ideally, the out-of-phase RF signals from both active devices will have pure half-sinusoidal waveforms, which contain, according to the



(a)



(b)

Figure 5.6 Schematic configurations of fractional 1:1.5 cable transformer.

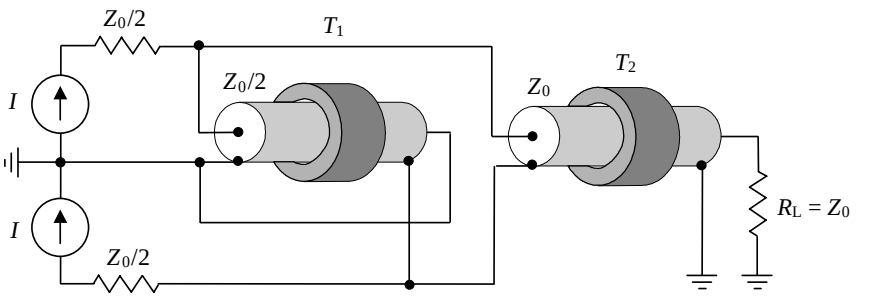


Figure 5.7 Circuit arrangement with two cable transformers for push–pull operation.

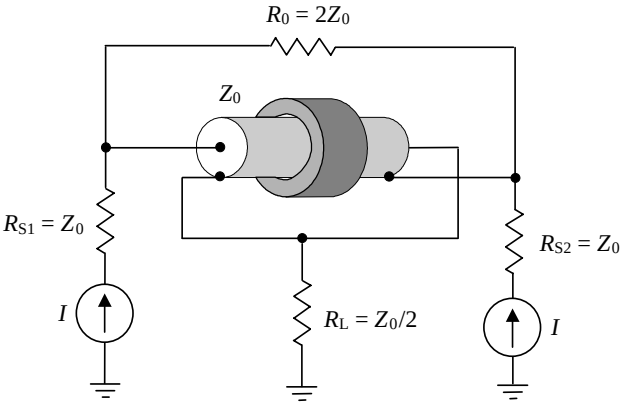


Figure 5.8 Coaxial cable combiner.

Fourier series expansion, only fundamental and even harmonic components. This means a 180-degree shift for fundamental and in-phase conditions for the remaining even harmonics. In this case, the transformer T_1, commonly called a *hybrid*, operates as a filter for even harmonics because currents flow through its inner and outer conductors in opposite directions. For each fundamental flowing through its inner and outer conductors in the same direction, it works as RF choke, the impedance of which depends on the core permeability. Consequently, since the transformer T_2 is a 1:1 balanced-to-unbalanced transformer, to provide maximum power delivery to the load R_L, the output resistance of each device should be two times smaller.

Coaxial cable transformers allow us to combine the output powers from two or more power amplifiers. Figure 5.8 shows an example of such a transformer combining two in-phase signals when both signals are delivered to the load R_L and no signal will be dissipated in the ballast resistor R_0 if their amplitudes are equal [5]. The main advantage of this transformer is the zero longitudinal voltage along the line for equal input powers; as a result, no losses occur in the ferrite core. When one input signal source (for example a power amplifier) defaults or disconnects, the longitudinal voltage becomes equal to half the voltage of another input source. Using this transformer, it is possible to combine two out-of-phase signals when the ballast resistor is considered as the load and the load resistor in turn is considered as the ballast resistor. Another hybrid combiner using two coaxial cable transformers is shown in Fig. 5.9. Here two independent signal sources operate with the same load R_L and the ballast resistor R_0 can be grounded. These transformer-based combiners can also be used for the power division when the output power from a single source is divided into two independent loads. In this case, the original load and the two signal sources should be switched.

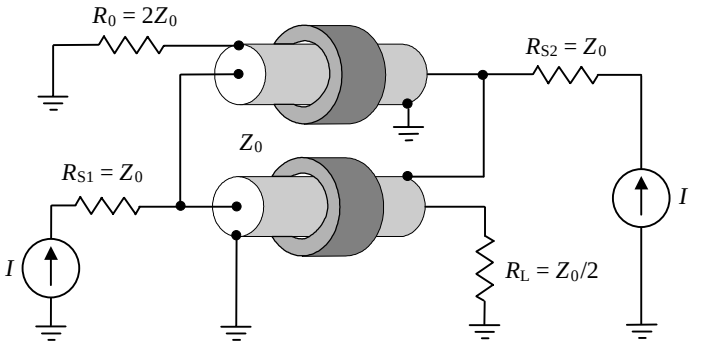
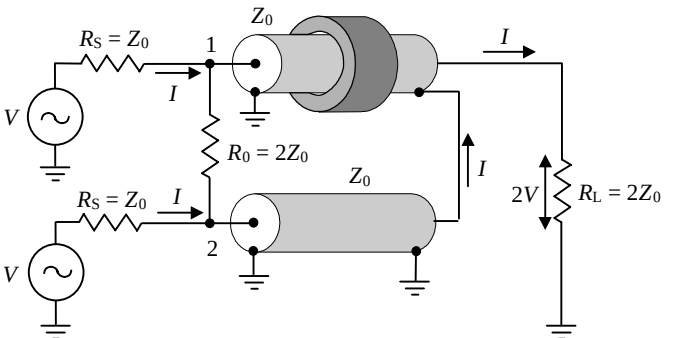
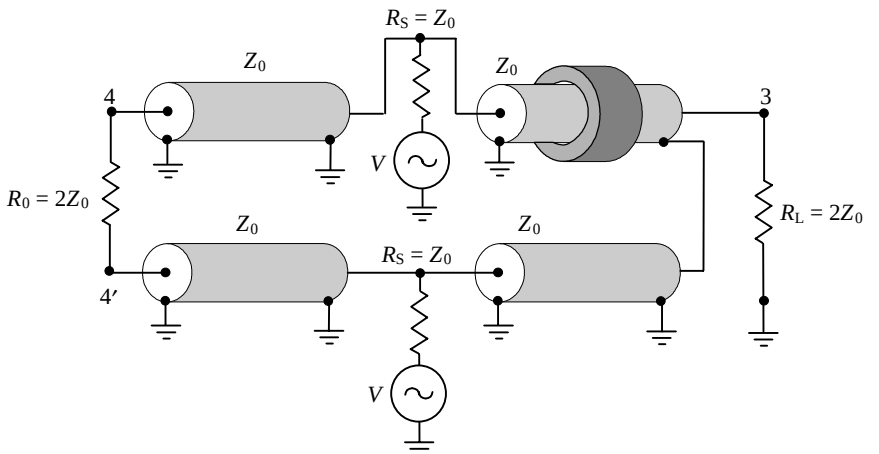


Figure 5.9 Two-cable hybrid combiner.



(a)



(b)

Figure 5.10 Two-cable combiners with increased isolation.

Figure 5.10(a) shows a coaxial line two-way combiner where the input signals having the same amplitudes and phases at ports 1 and 2 are matched at higher frequencies when all lines are of the same length and $R_S = Z_0 = R_L/2 = R_0/2$ [4]. In this case, the isolation between these input ports can be calculated by

$$C_{23} = 10 \log_{10}[4(1 + 4 \cot^2 \theta)], \text{ dB} \tag{5.17}$$

where θ is the electrical length of each transmission line. In order to improve the isolation, the symmetrical ballast resistor R_0 should connect through two identical additional lines, as shown in Fig. 5.10(b), which gives the minimum reflection coefficient magnitude at ports 3 and 4 of

$$|\Gamma|_{\min} = (1 + 2 \cot^2 \theta)^{-1} \tag{5.18}$$

Using two ferrite cores it is possible to realize the coaxial cable combiners fully matched and isolated in pairs as shown in Fig. 5.11 [4]. Such combiners can be effectively used in high-power broadcasting VHF FM and VHF–UHF TV transmitters. In this case, for power amplifiers with output impedances of $R_{S1} = R_{S2} = Z_0/2$, it is necessary to provide the ballast resistor and load with $R_0 = R_L = Z_0$, where Z_0 is the characteristic impedance of the coaxial cables of equal lengths.

In the case when wide frequency bandwidth is not as crucial, it is convenient to use a simple ring hybrid, as shown in Fig. 5.12 [4, 6]. Due to the crisscross arrangement of the inner and outer conductors of two adjacent lines, its overall length can be reduced to the wavelength λ. The isolation between the input signal sources will be independent of frequency and will exceed 20 dB in a frequency range of 30 percent. For the 50-Ω source and load impedances, the hybrid ring can be arranged using four quarterwave coaxial lines with the characteristic impedances of 75 Ω.

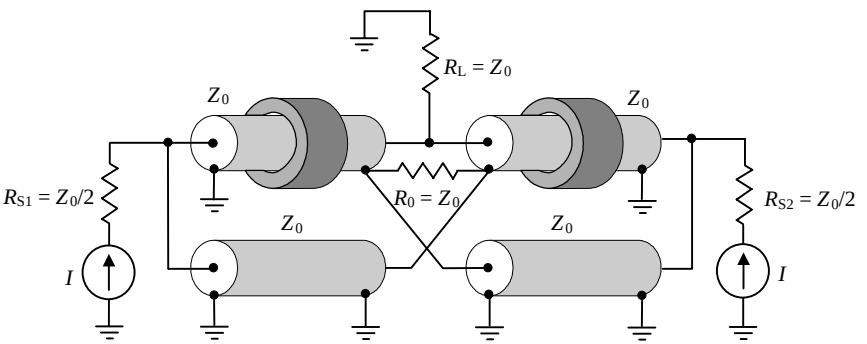


Figure 5.11 Fully matched and isolated cable combiner.

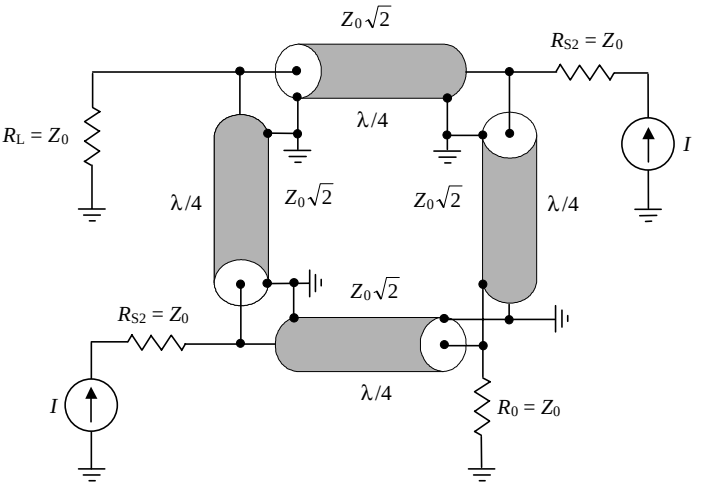


Figure 5.12 Cable-based ring hybrid schematic.

Wilkinson Power Divider

Figure 5.13(a) shows the basic parallel beam N-way divider/combiner, which provides a combination of powers from the N signal sources, where the input impedance of the N transmission lines with the characteristic impedance of Z_0 (each connected in parallel and equal to Z_0/N) is

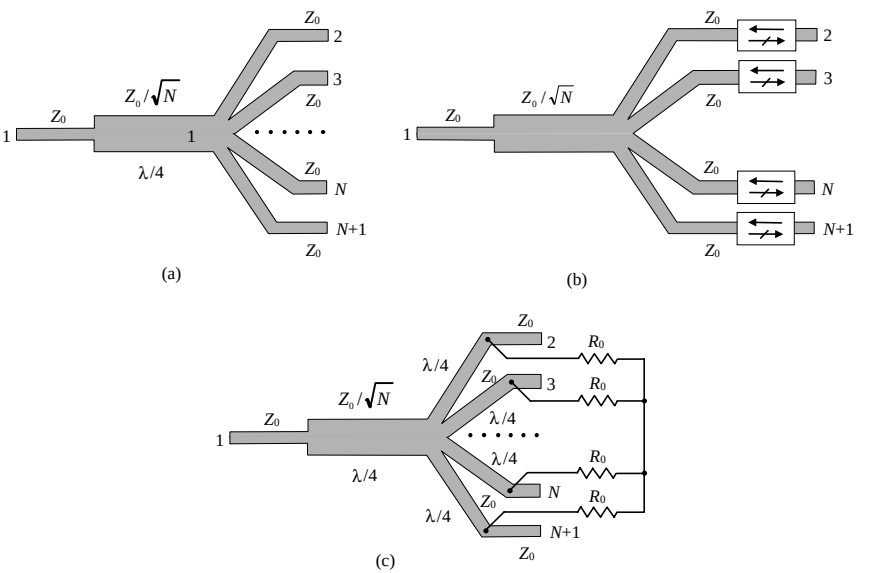


Figure 5.13 Circuit schematic of N-way beam combiners/dividers.

converted by a quarterwave transformer. This N-way divider/combiner cannot provide sufficient isolation between inputs. The input impedances are matched only when all input signals have the same magnitudes and phases at any combiner input. The effect of any input on the remaining ones becomes smaller for combiners with a greater number of inputs. For example, if the input signal is delivered into the input 2 and all other inputs and output 1 are matched, then the power dissipated at any load connected to the matched inputs will be decreased by $(1 - 1/N^2)/(2N - 1)$ times, and the isolation between any two inputs expressed through S-parameters is obtained by

$$S_{ij} = -10 \log_{10}\left(\frac{1}{N^2}\frac{N^2 - 1}{2N - 1}\right) \tag{5.19}$$

In most cases, better isolation is required than can be obtained from Eq. (5.19). The simplest way to provide full isolation between the inputs and output of the combiner is to connect the ferrite isolators (circulators) at the inputs $2, 3, \ldots, N, N + 1$, as shown in Fig. 5.13(b). For the N-way divider, the ferrite isolators must be connected in the reverse direction. In this case, the lengths of the transmission lines connected between the ferrite isolators and the quarterwave transformer should be equal. Although the ferrite isolators increase the overall weight and dimensions of the combiner and contribute to additional insertion losses, nevertheless they provide a very simple combiner realization and protect the connected power amplifiers from the load changes. Using a 12-way parallel beam combiner, the continuous output power of 1 kW for the L-band transmitter was obtained at the operating frequency of 1.25 GHz [7].

When one or more power amplifiers are eliminated, the overall output power P_{out} and efficiency η_c of the combiner can be calculated, respectively, by

$$P_{out} = \frac{(N - M)^2}{N} P_1 \tag{5.20}$$

$$\eta_c = \frac{P_{out}}{P_{in}} = 1 - \frac{M}{N} \tag{5.21}$$

where

$P_{in} = (N - M)P_1$
$P_1 =$ output power from single power amplifier
$N =$ number of the inputs
$M =$ number of destroyed power amplifiers

Part of the output powers of the remaining power amplifiers will be dissipated within the ferrite isolators (in ballast resistors of circulators). For each ferrite isolator connected to the operating power amplifier, the

dissipated power P_{do} can be defined as

$$P_{do} = \left(\frac{M}{N}\right)^2 P_1 \tag{5.22}$$

For each isolator connected to the destroyed power amplifier, the dissipated power P_{dd} is

$$P_{dd} = \left(\frac{N-M}{N}\right)^2 P_1 \tag{5.23}$$

The Wilkinson N-way power combiner/divider provides matching of all ports, low loss and high isolation between input and output ports due to the additional ballast resistors $R_0 = Z_0$. As shown in Fig. 5.13(c), one terminal of each ballast resistor is connected to the transmission line in each direction at the quarter-wavelength distance from the quarterwave transformer and all other terminals are combined together [8]. However, hybrid power division can also exist when the source resistance R_S is different from Z_0, provided the characteristic impedance of the quarterwave transmission line adjacent to the source is equal to $\sqrt{R_S Z_0/N}$. The frequency dependence of the input $VSWR_{in}$ of such a combiner/divider, depending on the number of the power division ports N, is shown in Fig. 5.14 [9].

The main problem with adequately implementing the Wilkinson combiners/dividers is the provision of a common connection of the ballast resistors with minimum lead lengths, because ideally this connection should represent a point connection. In order to solve this problem, it

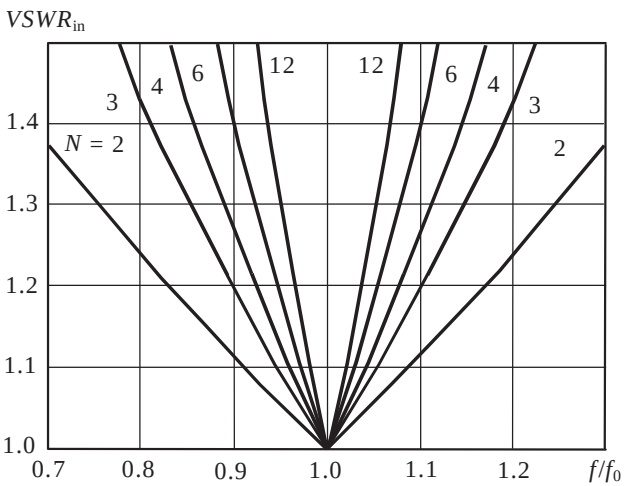


Figure 5.14 Frequency performance of N-way Wilkinson divider [9].

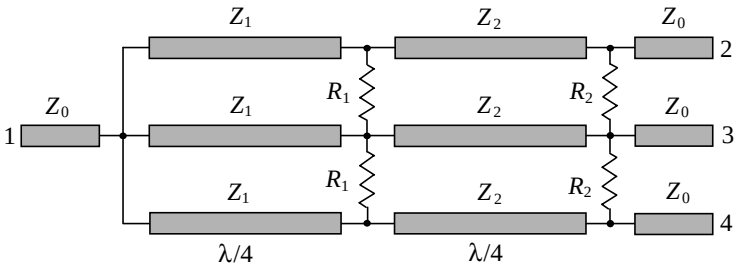


Figure 5.15 Microstrip three-way divider with improved isolation.

is advisable to realize a combiner as a multisection providing sufficient isolation and matching. Such a 3-way divider is shown in Fig. 5.15, where the characteristic impedances of the quarterwave transmission lines are chosen to maximize the operating frequency bandwidth, so that $Z_1 = 114\ \Omega$ and $Z_2 = 65.8\ \Omega$ with $Z_0 = 50\ \Omega$, $R_1 = 64.95\ \Omega$ and $R_2 = 200\ \Omega$ [10]. This two-step 3-way divider provides an octave frequency bandwidth.

However, high characteristic impedance values (more than 100 Ω) for the transmission lines can create a problem in their practical microstrip implementation, since their narrow widths increase the insertion loss. In this case, using a recombinant power divider, shown in Fig. 5.16, provides 20-dB isolation in a frequency range of 72 percent for a maximum line impedance of 80 Ω and requires only three isolation resistors [11]. This three-way recombinant divider has insertion losses of about 1 dB and return losses of more than 12 dB in a frequency range of 6–14 GHz, fabricated in 25-mil thick 99.6 percent alumina substrate. The design values for the quarterwave transmission lines were $Z_1 = 36\ \Omega$, $Z_2 = 40\ \Omega$, $Z_3 = 40\ \Omega$, $Z_4 = 80\ \Omega$, and $Z_5 = 40\ \Omega$ with the ballast resistors $R_1 = 50\ \Omega$ and $R_2 = 100\ \Omega$.

The hybrid microstrip realization of the simplest two-way Wilkinson divider is shown in Fig. 5.17(a). Despite its small dimensions and

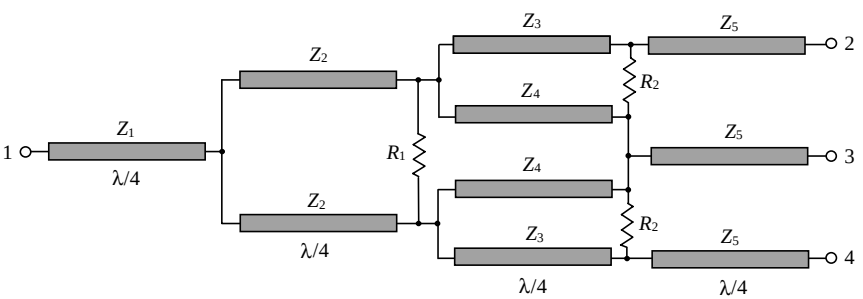


Figure 5.16 Modified microstrip three-way divider with improved isolation.

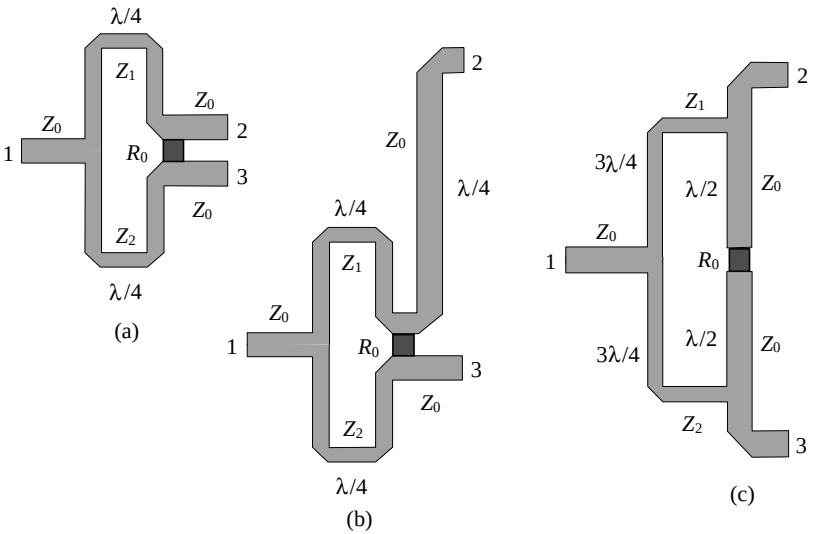


Figure 5.17 Microstrip realization of two-way Wilkinson dividers.

simple construction, such a divider possesses a sufficiently wide frequency bandwidth when, due to a symmetrical configuration when $R_0 = 2Z_0$ and $Z_1 = Z_2 = Z_0\sqrt{2}$, equal power division with $S_{21} = S_{31}$ is performed at all frequencies. However, in practice, it is necessary to take into account the distributed RC structure of the ballast resistor, when its size is sufficiently large, as well as manufacturing tolerances and discontinuities. As a result, in a frequency bandwidth of 30 percent with $VSWR_{\text{in}} = 1.2$ and $VSWR_{\text{out}} = 1.03$, the isolation between the divider outputs can be better than 20 dB [12].

The scattering S-matrix of the ideally matched two-way Wilkinson divider at the center frequency is obtained by

$$[S] = -\frac{j}{\sqrt{2}}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \tag{5.24}$$

The unequal power–split ratio for two-way Wilkinson divider with K that differs from unity can be realized when [1]

$$Z_2 = \frac{Z_0}{K}\sqrt{\frac{1+K^2}{K}} \tag{5.25}$$

$$Z_1 = Z_0\sqrt{K(1+K^2)} \tag{5.26}$$

$$R_0 = Z_0\left(K + \frac{1}{K}\right) \tag{5.27}$$

On the basis of a symmetrical two-way divider, the quadrature one can be designed using an additional quarterwave microstrip line connected to one of the outputs, as shown in Fig. 5.17(b). This divider has the same properties as the basic one at the center frequency. The narrower frequency bandwidth is the result of the deviation of the electrical length of this additional microstrip line from a quarterwave one with the change of the operating frequency. However, the broadband properties can be improved by using the more complicated phase-shift circuit instead of a simple microstrip line. The phase shift between two output ports 2 and 3 will be close to 90° in an octave frequency range if a Schiffman's element based on the coupled microstrip lines is connected to one port [13]. At the same time, an additional microstrip line with the electrical length of $3\lambda/4$ at the center bandwidth frequency should be connected to the second port.

This microstrip design of a two-way Wilkinson power divider is usually used at *X*-band frequencies and below, especially when the desired power-split ratio is significantly different from unity. At higher frequencies, in order to increase a chip-resistor resonant frequency, the overall chip dimensions must be very small: approximately 1 mm × 0.5 mm. This means that the two branches of the power divider are very close to each other, which leads to strong mutual coupling between the output microstrip lines and, as a result, upsets the desired power-split ratio. A possible solution is to use the branches with the electrical lengths of $3\lambda/4$ instead of $\lambda/4$ and include two additional branches into a semicircle, as shown in Fig. 5.17(c) [14]. These additional branches should be of $\lambda/2$ electrical lengths with the characteristic impedances equal to Z_0. At the operating frequency of 30.4 GHz, such a modified power divider with a power-split ratio 2:1 provides better than 20 dB return losses at all ports and a better than 17 dB isolation between all ports with the insertion loss of about 1.3 dB.

The connection of two-way Wilkinson dividers allows multi-channel division or combination. The simplest practical realization is the binary divider/combiner, which is composed of n stages where each consecutive stage contains a number of two-way dividers, which increases by 2^n ($n = 1, 2, 3, \ldots$). The output power and efficiency of an N-way divider due to the destroyed power amplifiers can be calculated by Eqs. (5.20) and (5.21), respectively. For a single destroyed power amplifier, the power dissipated in the ballast resistors is

$$P_{\text{db}} = \left(1 - \frac{1}{N}\right)^2 P_1 \tag{5.28}$$

The output power of $P_1/2$ is dissipated in the ballast resistor adjacent to the destroyed power amplifier; the output power of $P_1/4$ is dissipated

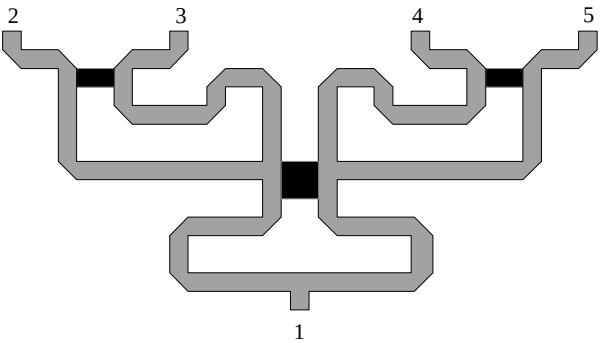


Figure 5.18 Practical UHF four-way microstrip Wilkinson divider.

in the ballast resistor of the next stage, and so on. However, the characteristic impedances of the microstrip lines are often different. A divider with a number of outputs multiple to 4^n presents the convenient case when they may be of the same impedance. In Fig. 5.18, the UHF four-way microstrip Wilkinson divider is shown, which was developed on alumina ceramics with six 50-Ω quarterwave microstrip lines and two 100-Ω and one 50-Ω integrated resistors. This microstrip Wilkinson power divider/combiner provides the insertion loss of less than 0.3 dB and isolation between any outputs of about 20 dB in the frequency bandwidth of ±10 percent [15].

Figure 5.19 shows the compact microstrip three-way Wilkinson power divider designed for operation over a frequency range of 1.7–2.1 GHz, with minimum combining efficiency of 93.8 percent, maximum amplitude imbalance of 0.35 dB and isolation better than 15 dB [16]. To avoid any amplitude and phase imbalances between the divider 50-Ω outputs, the resistor connected to its middle branch should be split into

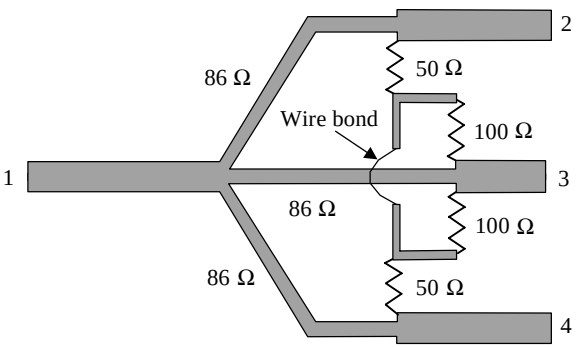


Figure 5.19 Compact microstrip three-way Wilkinson power divider.

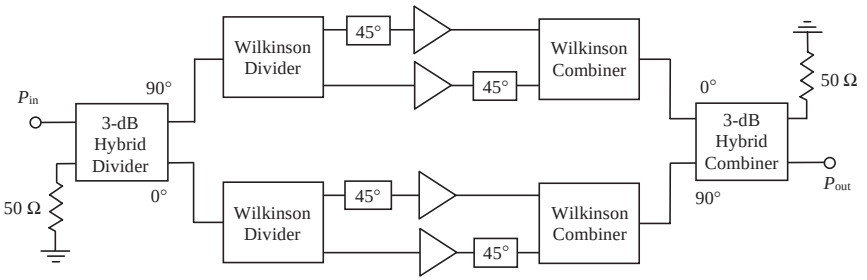


Figure 5.20 Implementation of two-way Wilkinson dividers into power amplifier design.

two equal parallel resistors. To obtain an ideal floating node, these two resistors are connected together with narrow microstrip lines that are as short as possible. Finally, to connect the resistors from both sides of the middle branch, a copper wire of diameter of 7 mil is used. The most critical parameter is the isolation between port 2 and port 4, which can be improved by shortening the wire bond length.

Addition of the Wilkinson dividers into power amplifier design can improve the overall power amplifier characteristics, which for conventional single-stage one depend significantly on load *VSWR*. For a 3.5 V 29 dBm GaAs MESFET power amplifier designed to operate in a 900-MHz digital cellular phone system, the adjacent channel leakage power ratio increases from –56 dBc to –32 dBc [17]. In addition, a large value of load *VSWR*, when increasing up to 3, leads to efficiency degradation from 52.7 to 35 percent. In this case, using the Wilkinson divider to combine the output powers from four power amplifier units with additional phase shifts provides overall high performance. Fig. 5.20 shows the configuration of such a power amplifier, combining two amplifier units in pairs using Wilkinson dividers/combiners and 45-degree delay lines, and four amplifier units using 3-dB quadrature hybrids. As a result, the overall distortion below -45 dBc with over 45 percent efficiency being obtained for load $VSWR \leq 3$.

Microwave Hybrids

The output powers from two power amplifiers at microwaves can be combined using the two-branch microstrip line 90° hybrid shown in Fig. 5.21, whose ports are connected to the standard 50-Ω source and load impedances. The characteristic impedances of the transverse branches should be 50 Ω; the longitudinal branches must have the characteristic impedance of $50/\sqrt{2} = 35.4\ \Omega$. The branch-line hybrid does not depend on the load mismatch level for equal reflected coefficients from the outputs when all reflected power is dissipated in the 50-Ω ballast resistor. However, in practice, due to the quarter-wavelength transmission

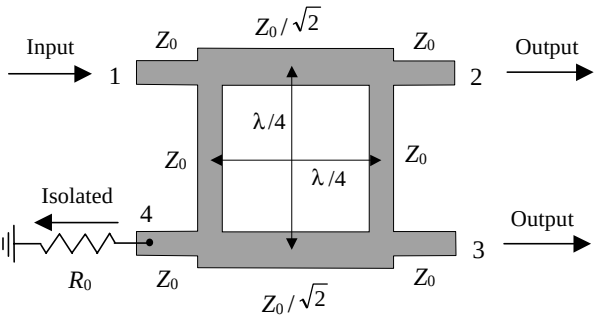


Figure 5.21 Two-branch microstrip line 90-degree quadrature hybrid.

line requirement, the bandwidth of a balanced amplifier based on such a quadrature branch-line hybrid is limited to 10 to 20 percent.

When all ports are matched, the power entering input port 1 is divided between the output ports 2 and 3 with a 90° phase shift between these outputs, and no power is delivered to the isolated port 4. The scattering S-matrix of such a quadrature hybrid branch-line coupler is given by

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{5.29}$$

Figure 5.22 shows the calculated frequency bandwidth characteristics of the two-branch line coupler matched at the center bandwidth frequency with the load impedance $Z_L = Z_0 = 50\ \Omega$ [15].

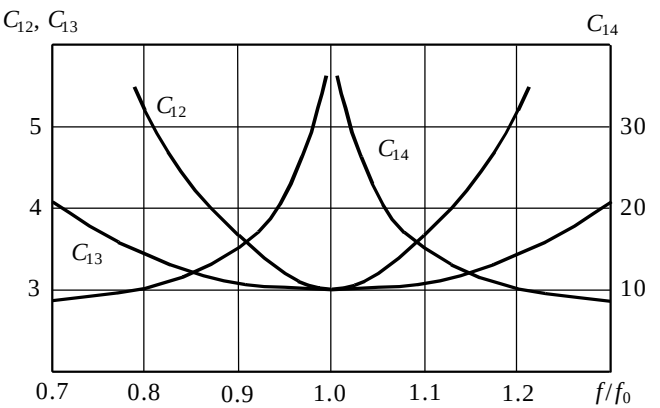


Figure 5.22 Frequency bandwidth characteristics of two-branch line coupler.

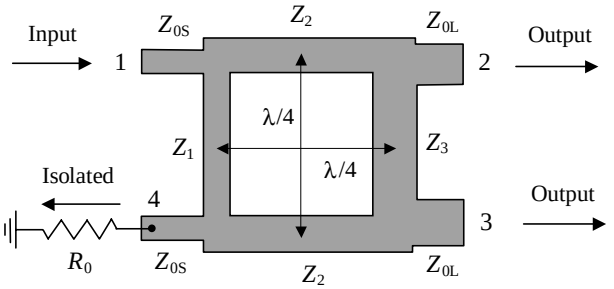


Figure 5.23 Two-branch microstrip line quadrature impedance transforming hybrid.

To simplify the requirements for the matching circuits for a balanced high-power amplifier with small values for the device impedances, it is possible to use the quadrature branch-line 90° hybrids with impedance transforming properties (see Fig. 5.23) [18]. The characteristic impedances of the quarter-wavelength branch lines related to the input impedance Z_{0S} and output impedance Z_{0L} can be calculated by

$$Z_1 = \frac{Z_{0S}}{K} \tag{5.30}$$

$$Z_2 = \sqrt{\frac{Z_{0S}Z_{0L}}{1+K^2}} \tag{5.31}$$

$$Z_3 = \frac{Z_1 Z_{0L}}{Z_{0S}} \tag{5.32}$$

where K is the voltage-split ratio between the output ports 2 and 3, and $R_0 = Z_{0S}$.

Broadband impedance transformation can be achieved when several quadrature microwave hybrids are connected in succession having the different characteristic impedances of the quarter-wavelength branch lines. A two-section branch-line quadrature hybrid is shown in Fig. 5.24. To design this hybrid with the given impedance transformation ratio r and the power-split ratio K^2, the branch-line characteristic impedances should be chosen according to [19]

$$Z_1 = Z_{0S}\sqrt{r\frac{t^2-r}{t-r}} \tag{5.33}$$

$$\frac{Z_2^2}{Z_3} = Z_{0S}\sqrt{r-\left(\frac{r}{t}\right)^2} \tag{5.34}$$

$$Z_4 = Z_{0S}\frac{\sqrt{r(t^2-r)}}{t-1} \tag{5.35}$$

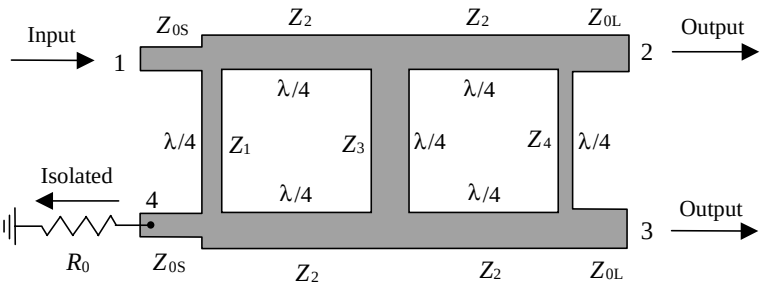


Figure 5.24 Broadband microwave branch-line quadrature hybrid.

where $t = r\sqrt{1 + K^2}$ and a condition of $Z_2 = Z_3$ gives maximum bandwidth when the best performance at the center bandwidth frequency is specified.

For an equal power division when $K = 1, t = r\sqrt{2}$ specifies a minimum value of $r = 0.5$. However, in practice, it is better to choose r in the range 0.7 to 1.3, in order to provide the physically realizable branch-line characteristic impedances for 50-Ω input impedance. For example, for the 50- to 35-Ω transformation with a two-section hybrid, $Z_1 = 72.5\ \Omega$, $Z_2 = \mathrm{Z}_3 = 29.6\ \Omega$ and $Z_4 = 191.25\ \Omega$. This gives a 0.5 dB output balance bandwidth of 25 percent with the return loss and isolation better than 20 dB for a 2-GHz hybrid. For the 50- to 25-Ω transformation with three-section hybrid, the amplitude balance of 3.7±0.68 dB and the return loss and isolation of approximately 15 dB over the frequency bandwidth of 3 to 5 GHz were realized [18].

For monolithic microwave integrated circuit (MMIC) applications, the overall dimensions of the quadrature hybrid with quarterwave branch-line are too large. Therefore, it is attractive to replace each quarterwave branch line with a combination of short transmission lines with shunt capacitances providing the same bandwidth properties [see Fig. 5.25 (a) and (b)] [20]. Consider the admittance matrices for a quarterwave transmission line $[Y_\mathrm{a}]$ and a circuit consisting of a short transmission line with two shunt capacitances $[Y_\mathrm{b}]$ given by

$$[Y_\mathrm{a}] = \frac{1}{jZ_0}\begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix} \tag{5.36}$$

$$[Y_\mathrm{b}] = \frac{1}{jZ\sin\theta}\begin{bmatrix} \cos\theta - \omega CZ\sin\theta & -1 \\ -1 & \cos\theta - \omega CZ\sin\theta \end{bmatrix} \tag{5.37}$$

where Z_0 is the characteristic impedance of a quarterwave line, Z and θ are the characteristic impedance and electrical length of a shortened line, and C is the shunt capacitance. Equating the corresponding

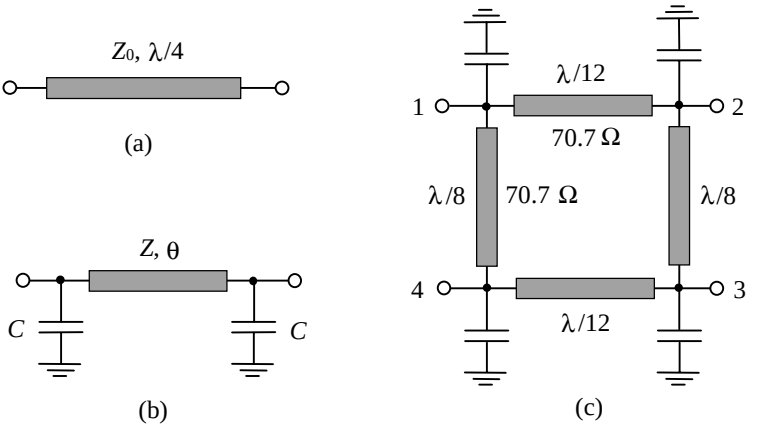


Figure 5.25 Reduced-size branch-line quadrature hybrid.

Y-parameters in Eqs. (5.36) and (5.37), we can obtain the relationships between the circuit parameters in the form of

$$Z = Z_0/\sin\theta \tag{5.38}$$

$$C = 1/\omega Z_0 \cos\theta \tag{5.39}$$

The branch-line length can be made shorter with the increase of their characteristic impedance Z and lumped capacitance C. For example, when choosing the electrical length of $\theta = 45^\circ$, the characteristic impedance of the transmission line increases by a factor of $\sqrt{2}$.

A circuit schematic of the reduced-size branch-line quadrature hybrid is shown in Fig. 5.25(c). Since, in the conventional branch-line hybrid, the characteristic impedances of the transverse and longitude lines are Z_0 and $Z_0/\sqrt{2}$, respectively, the parameters of the reduced-size hybrid are obtained from

$$\theta_1 = \sin^{-1}\left(\frac{Z_0}{Z}\right) \tag{5.40}$$

$$\theta_2 = \sin^{-1}\left(\frac{Z_0}{Z\sqrt{2}}\right) \tag{5.41}$$

$$\omega C Z_0 = \sqrt{1-\left(\frac{Z_0}{Z}\right)^2} + \sqrt{2-\left(\frac{Z_0}{Z}\right)^2} \tag{5.42}$$

where θ_1 and θ_2 are the electrical lengths of the reverse and longitude branch lines, respectively.

When $Z = Z_0\sqrt{2}$, $\theta_1 = 45^\circ$ and $\theta_2 = 30^\circ$, as shown in Fig. 5.25(c) for the characteristic impedance $Z_0 = 50\ \Omega$. Experimental results for

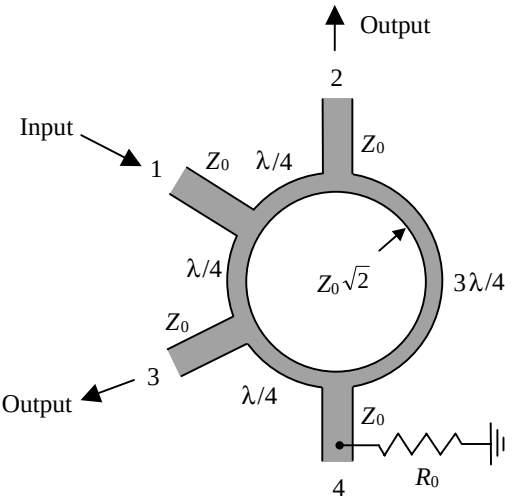


Figure 5.26 Microstrip ring hybrid.

a 25-GHz reduced-size hybrid show that its bandwidth performance is slightly narrower than that of the quarterwave one, but its overall dimension is more than 80 percent smaller.

The ring hybrid, or rate-race, whose microstrip topology is shown in Fig. 5.26, can be used to divide the output power of the single oscillator or combine the output powers from two synchronized oscillators. In the case of power division, a signal applied to port 1 will be evenly split into two in-phase components at ports 2 and 3, and port 4 will be isolated. If the input signal is applied at port 4, it will be equally split into two components with 180° difference at ports 2 and 3, and port 1 will be isolated. When operated as a combiner, with an input signal applied at ports 2 and 3, the sum of the input signals will be delivered to port 1. Their difference will flow to port 4 and be dissipated in the corresponding ballast resistor R_0. For equal signals and matched ring hybrid with $Z_0 = R_0$, there is zero power dissipation at port 4. Due to the frequency dependence of the ring lengths, the operating frequency bandwidth of the ring hybrid is 20 to 30 percent. The scattering S-matrix for the ideal 3-dB 180° ring hybrid is

$$[S] = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{bmatrix} \tag{5.43}$$

It is possible to reduce the overall dimension of the conventional ring hybrid with quarterwave transmission line sections by using the single

frequency equivalence between the circuits with the lumped and distributed parameters [21]. Consider the transmission matrices for a 270° transmission line $[ABCD_{\mathrm{a}}]$ and a π-type lumped circuit $[ABCD_{\mathrm{b}}]$, consisting of the series capacitors and two shunt inductors, given by

$$[ABCD_{\mathrm{a}}] = \left[\begin{array}{cc} \cos\theta & jZ_0\sin\theta \\ j\dfrac{\sin\theta}{Z_0} & \cos\theta \end{array}\right]\Bigg|_{\theta=3\pi/2} = \left[\begin{array}{cc} 0 & -jZ_0 \\ \dfrac{-j}{Z_0} & 0 \end{array}\right] \tag{5.44}$$

$$\begin{aligned}[ABCD_{\mathrm{b}}] &= \left[\begin{array}{cc} 1 & 0 \\ -j/\omega L & 1 \end{array}\right]\left[\begin{array}{cc} 1 & -j/\omega C \\ 0 & 1 \end{array}\right]\left[\begin{array}{cc} 1 & 0 \\ -j/\omega L & 1 \end{array}\right] \\ &= \left[\begin{array}{cc} 1-\dfrac{1}{\omega^2 LC} & -j\dfrac{1}{\omega C} \\ -j\dfrac{1}{\omega L}\left(2-\dfrac{1}{\omega^2 LC}\right) & 1-\dfrac{1}{\omega^2 LC} \end{array}\right] \end{aligned} \tag{5.45}$$

Equating the corresponding elements of both matrices obtained by Eqs. (5.44) and (5.45) yields the relationships between the circuit elements as

$$Z_0\omega C = Z_0/\omega L = 1 \tag{5.46}$$

To reduce the size of a ring hybrid, a 270° transmission line is replaced by a high-pass lumped section. Then, it is advisable to replace the quarterwave line sections by shortened ones with two shunt capacitances, as shown in Fig. 5.25(b) for a branch-line coupler. Finally, the characteristic impedance of the transmission line sections is chosen so that the shunt inductors of the high-pass section in Fig. 5.27(b) are resonant with shunt capacitors of the low-pass section at the center

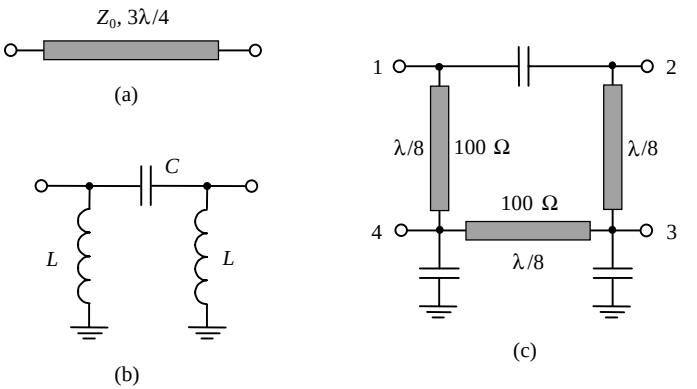


Figure 5.27 Reduced-size ring hybrid.

bandwidth frequency to remove these components. Figure 5.27(c) shows the circuit diagram of the reduced-size ring hybrid with the characteristic impedances of the transmission line sections of 100 Ω and their electrical lengths of 45° [20].

Coupled-Line Directional Couplers

A coupled-line directional coupler—its single-section schematic is shown in Fig. 5.28(a)—can be used for broadband power division or combination. Its electrical properties are described using the concept of two types of excitations for the coupled lines in TEM approximation. In this case, for the even mode, the currents flowing in the strip conductors

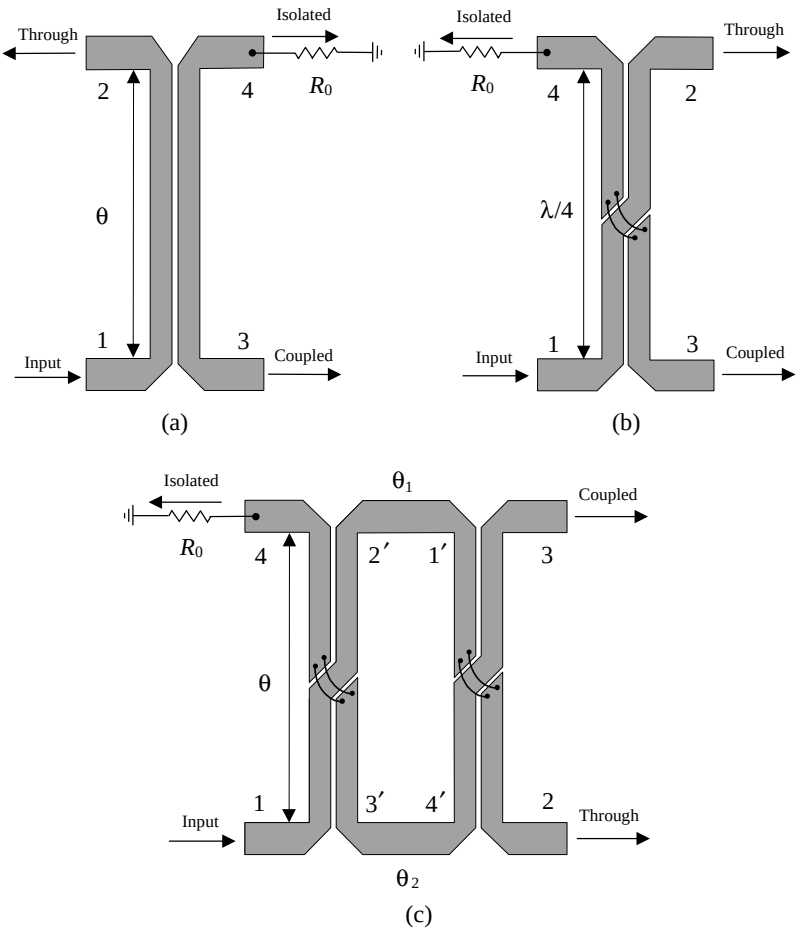


Figure 5.28 Coupled-line directional couplers.

are equal in amplitude and flow in the same direction. The electric field has even symmetry about the center line, and no current flows between the two strip conductors. For the odd mode, the currents flowing in the strip conductors are equal in amplitude but flow in opposite directions. The electric field lines have an odd symmetry about the center line, and a voltage null exists between these two strip conductors. An arbitrary excitation of the coupled lines can always be treated as a superposition of appropriate amplitudes of even and odd modes. Therefore, the characteristic impedance for the even excitation mode Z_{0e} and the characteristic impedance for the odd excitation mode Z_{0o} characterize the coupled lines. Using two coupled equal strip lines, connected to the input and output transmission lines with the characteristic impedance of Z_0, we can obtain $Z_0^2 = Z_{0e}Z_{0o}$. In this case, $S_{11} = S_{14} = 0$ for any electrical lengths of the coupled lines and the output port 4 is isolated from the matched input port 1. Changing the coupling between the lines and their widths can change the characteristic impedances Z_{0e} and Z_{0o}. The scattering parameters S_{12} and S_{13}, which characterize the power transmission to the output ports 2 and 3, depend on the coupling coefficient $C = (Z_{0e} - Z_{0o})/(Z_{0e} + Z_{0o})$ and electrical length θ by [22]

$$S_{12} = \frac{\sqrt{1 - C^2}}{\sqrt{1 - C^2}\cos\theta + j\sin\theta} \tag{5.47}$$

$$S_{13} = \frac{jC\sin\theta}{\sqrt{1 - C^2}\cos\theta + j\sin\theta} \tag{5.48}$$

The voltage-split ratio K is defined as the ratio between the voltages at port 2 and port 3 by

$$K = \left|\frac{S_{12}}{S_{13}}\right| = \frac{\sqrt{1 - C^2}}{C\sin\theta} \tag{5.49}$$

where K can be managed by changing the coupling coefficient C and electrical length θ.

For $\theta = \pi/2$ when a coupler is $\lambda/4$ long, Eqs. (5.47) and (5.48) reduce to

$$S_{12} = -j\sqrt{1 - C^2} \tag{5.50}$$

$$S_{13} = C \tag{5.51}$$

which defines C as the midband voltage coupling coefficient, where an equal voltage split between the output ports can be provided with $C = 1/\sqrt{2}$.

If it is necessary to provide the output ports 2 and 3 at one side, it is best to use a directional coupler as shown in Fig. 5.28(b). Such a 3-dB microstrip directional coupler, fabricated on alumina substrate, should have the calculated strip spacing of less than 10 μm. Such a narrow

value can explain the interest in the construction of directional couplers with larger spacing. One solution is to use a tandem connection of two equal directional couplers, which allows realizing the resulting broadband 3-dB coupling for substantially smaller coupling between microstrip lines in individual couplers. The tandem coupler shown in Fig. 5.28(c) has the electrical properties of the individual coupler when the output ports 1, 4 and 2, 3 are isolated in pairs and the phase difference between the output ports 2 and 3 is of 90° [22, 23].

Consider the signal propagation from input port 1 to output ports 2 and 3 of the tandem coupler. The signal from input port 1 to output port 2 propagates through the traces 1-2′-1′-2 and 1-3′-4′-2, whereas the signal flowing through the traces 1-2′-1′-3 and 1-3′-4′-3 is delivered to the output port 3. Then, taking into account the identity of the individual couplers and isolation property of the tandem coupler, the relationships between the incident and reflected voltages can be given by

$$V_{2r}^{T} = \left[S_{12}^{2}\exp(-j\theta_1) + S_{13}^{2}\exp(-j\theta_2)\right] V_{1i}^{T} \tag{5.52}$$

$$V_{3r}^{T} = \left[S_{12}S_{13}\exp(-j\theta_1) + S_{12}S_{13}\exp(-j\theta_2)\right] V_{1i}^{T} \tag{5.53}$$

where θ_1 and θ_2 are the electrical lengths of the traces 2′-1′ and 3′-4′, respectively. For $\theta_1 = \theta_2 = \theta$, the scattering S-matrix of a tandem coupler can be written by

$$\left[S^{T}\right] = \begin{bmatrix} 0 & S_{12}^{2}+S_{13}^{2} & 2S_{12}S_{13} & 0 \\ S_{12}^{2}+S_{13}^{2} & 0 & 0 & 2S_{12}S_{13} \\ 2S_{12}S_{13} & 0 & 0 & S_{12}^{2}+S_{13}^{2} \\ 0 & 2S_{12}S_{13} & S_{12}^{2}+S_{13}^{2} & 0 \end{bmatrix} \exp(-j\theta) \tag{5.54}$$

From Eqs. (5.47), (5.48), and (5.54), we can obtain

$$\frac{S_{12}^{T}}{S_{13}^{T}} = \frac{S_{12}^{2}+S_{13}^{2}}{2S_{12}S_{13}} = -j\frac{1-C^{2}(1+\sin^{2}\theta)}{2C\sqrt{1-C^{2}}\sin\theta} \tag{5.55}$$

As a result, the signal at output port 2 overtakes the signal at output part 3 by 90°. As for a 3-dB tandem coupler with $\theta = \pi/2$, the magnitude of Eq. (5.55) must be equal to unity. The required coupling coefficient becomes equal to

$$C = 0.5\sqrt{2-\sqrt{2}} = 0.3827$$

or

$$C_{12} = C_{13} = 8.34\,\text{dB}$$

Using a series connection of two directional couplers with their appropriate insertion loss C_{12} and coupling C_{13} of 8.34 dB, we can realize a tandem coupler with the insertion loss and coupling of 3 dB. The electrical properties of the resulting tandem coupler are the same as for an individual directional couple. An 8.34-dB directional coupler has the dimensions of $W/h = 0.77$ and $S/h = 0.18$ for an alumina substrate with $\varepsilon_r = 9.6$, where W is the strip width, S is the strip spacing, and h is the substrate thickness [15].

Another way to increase the coupling between edge-coupled lines is to use several parallel lines with the wires interconnected with each other, as shown in Fig. 5.29. For the Lange coupler shown in Fig. 5.29(a), four coupled microstrip lines are used, achieving a 3-dB coupling ratio with an octave or more bandwidth [24]. The signal at the input port 1 is distributed between output ports 2 and 3 with the phase difference of 90° so that the Lange coupler is a quadrature one. However, this structure is quite complicated for practical implementation when, for alumina substrate with $\varepsilon_r = 9.6$, the dimensions of a 3-dB Lange coupler are $W/h = 0.107$ and $S/h = 0.071$, where W is the width of each strip, and S is the strip spacing.

Figure 5.29(b) illustrates the unfolded Lange coupler with four strips of equal lengths; it offers the same electrical performance but is easier for circuit modeling [25]. The even-mode characteristic impedance Z_{e4} and odd-mode characteristic impedance Z_{o4} of the Lange coupler with $Z_0^2 = Z_{e4}Z_{o4}$, in terms of the characteristic impedances of the

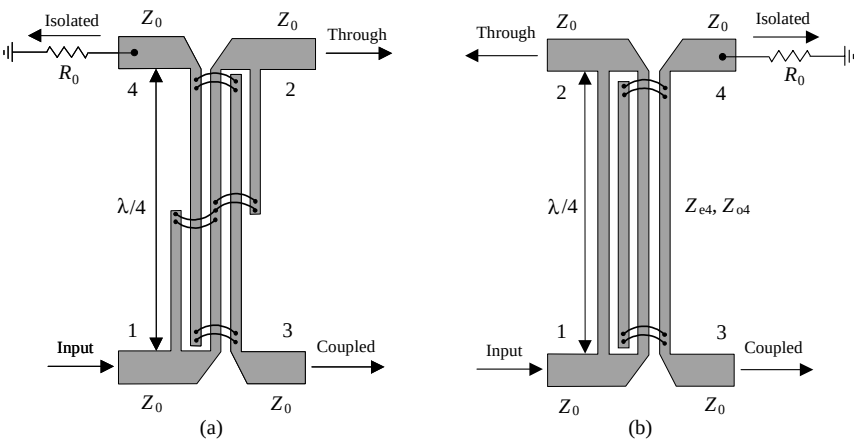


Figure 5.29 Lange directional couplers.

two-conductor line (which is identical to any pair of adjacent lines in the coupler), can be obtained by [26]

$$Z_{e4} = \frac{Z_{0o} + Z_{0e}}{3Z_{0o} + Z_{0e}} Z_{0e} \tag{5.56}$$

$$Z_{o4} = \frac{Z_{0e} + Z_{0o}}{3Z_{0e} + Z_{0o}} Z_{0o} \tag{5.57}$$

where Z_{0e} and Z_{0o} are the even- and odd-mode characteristic impedances of the two-conductor pair.

The midband voltage coupling coefficient C is given by

$$C = \frac{Z_{e4} - Z_{o4}}{Z_{e4} + Z_{o4}} = \frac{3\left(Z_{0e}^2 - Z_{0o}^2\right)}{3\left(Z_{0e}^2 + Z_{0o}^2\right) + 2Z_{0e}Z_{0o}} \tag{5.58}$$

The necessary even- and odd-mode characteristic impedances, as functions of the characteristic impedance Z_0 and coupling coefficient C, are determined by

$$Z_{0e} = \frac{4C - 3 + \sqrt{9 - 8C^2}}{2C\sqrt{(1-C)/(1+C)}} Z_0 \tag{5.59}$$

$$Z_{0o} = \frac{4C + 3 - \sqrt{9 - 8C^2}}{2C\sqrt{(1+C)/(1-C)}} Z_0 \tag{5.60}$$

and, for alumina substrate with $\varepsilon_r = 9.6$, the dimensions of such a 3-dB unfolded Lange coupler are $W/h = 0.112$ and $S/h = 0.080$, where W is the width of each strip, and S is the strip spacing.

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Chapter

6

Power Amplifier Design Fundamentals

Power amplifier design involves providing simultaneously accurate active device modeling, effective impedance matching (depending on the technical requirements and operation conditions), stability in operation and ease of practical implementation. The quality of the power amplifier design is evaluated by realizing maximum power gain under stable operating conditions with minimum amplifier stages regardless of the requirement for linearity or high efficiency. For stable operation, it is necessary to evaluate the operating frequency domains where the active device may be potentially unstable. To avoid the parasitic oscillations, the stabilization circuit technique for different frequency domains (from low frequencies up to high frequencies close to the device transition frequency) is discussed. The key parameter of the power amplifier is its linearity, which is very important for many TV and cellular applications. The relationships between the output power, 1-dB gain compression point, third-order intercept point, and intermodulation distortions of the third and higher orders are given and illustrated for different active devices. The device biasing conditions, which change when linearity is improved or efficiency is increased, depend on Classes A, AB, B, or C and the type of the active device. The biasing circuits for MOSFET device are simple due to its voltage control, because the gate dc current is equal to the gate leakage current. However, for bipolar devices with a current control, these currents differ substantially, depending on the device base current and class of operation. In view of this, several examples containing calculations of biasing circuit parameters for MOSFET and bipolar devices are presented. The basic classes of the power amplifier operation A, AB, B and C are introduced, analyzed and illustrated. The design and concept of push-pull amplifiers using

balanced transistors are given. In a final section, numerous practical examples of power amplifiers using MOSFET, MESFET, and bipolar devices in the frequency ranges from high frequencies up to microwaves, and output power from 100 mW up to 100 W, are shown and discussed.

Main Characteristics

A generalized single-stage power amplifier circuit is presented in Fig. 6.1. The two-port active device is characterized by a system of immittance W-parameters, i.e., any system of impedance Z-parameters or admittance Y-parameters, which are mainly used in practical power amplifier design. Matching circuits transform the source and load immittances, W_S and W_L, into definite values between points *1–2* and *3–4* respectively, by means of which the optimal design operation mode of the power amplifier is realized.

The given technical requirements and the convenience of the design realization (using the appropriate types of active devices and circuit schematics) determine the choice of system of Y-parameters or Z-parameters. Let, for the given input and output voltages, the active device be characterized by a matrix of Y-parameters: in this case, the source of the input signal is presented by the current source with internal admittance Y_S. A load is characterized by the load admittance Y_L as shown in Fig. 6.2(a). If a two-port active device is described by a system of Z-parameters, the source of the input signal is presented by the voltage source with an internal impedance Z_S, whereas the load is characterized by the load impedance Z_L as shown in Fig. 6.2(b). In both cases, the admittances, Y_S and Y_L, and the impedances, Z_S and Z_L, are seen looking toward the source and load through the input and output matching circuits.

To calculate the electrical characteristics of a power amplifier, consider a system of Y-parameters. The active device in this case is described by the following system of two equations:

$$\begin{cases} I_1 = Y_{11}V_1 + Y_{12}V_2 \\ I_2 = Y_{21}V_1 + Y_{22}V_2 \end{cases} \tag{6.1}$$

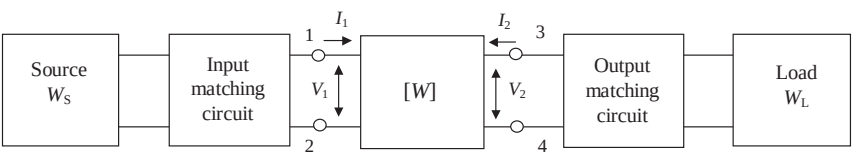

Figure 6.1 Generalized single-stage power amplifier circuit.

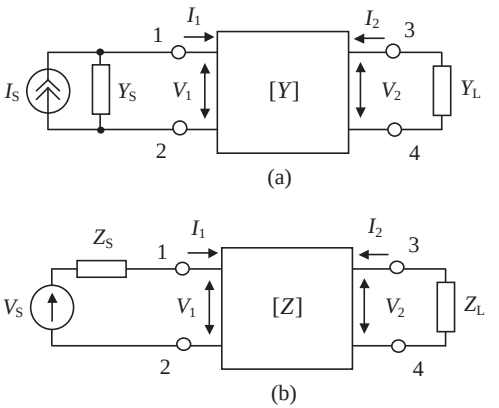

Figure 6.2 Two-port loaded amplifier networks.

Depending on impedance matching at the input and output device ports, several definitions of the amplifier power gain in terms of *Y*-parameters can be derived.

Operating power gain ($G_P = P_L/P_{in}$) is the ratio of power dissipated in the active load G_L to the power delivered to the input port of the active device with admittance Y_{in}. This gain is independent of G_S but is strongly dependent on G_L.

Available power gain ($G_A = P_{out}/P_S$) is the ratio of power available at the output port of the active device with admittance Y_{out} to the power available from the source G_S. This power gain depends on G_S but not G_L.

Transducer power gain ($G_T = P_L/P_S$) is the ratio of power dissipated in the active load G_L to the power available from the source G_S. This power gain assumes conjugate impedance matching at the input and output ports of the active device being dependent on both G_S and G_L.

Maximum available gain (*MAG*) is the theoretical power gain of the active device when its reverse transfer admittance Y_{12} is set equal to zero. It represents a theoretical limit on the gain that can be achieved with the given active device assuming conjugate impedance matching of the input and output ports of the active device with the source and load, respectively.

In practice, to characterize an amplifier circuit gain property, two types of power gain are used: operating power gain G_P and transducer power gain G_T. Operating power gain is mostly used because, in practice, it is usually required to calculate the power at the input port of

the device, which is necessary to provide the given power delivered to the load. However, to analyze the stability conditions, it is important to know the values of both the source impedance and the load impedance. Therefore, in this case it is preferable to use transducer power gain, which it is necessary to maximize within the restrictions imposed by the stability consideration.

First, consider the evaluation of G_P in terms of two-port network Y-parameters. If V_1 is the amplitude at the input port of the active device, then

$$P_{in} = 0.5V_1^2 \mathrm{Re}Y_{in} \tag{6.2}$$

where $Y_{in} = I_1/V_1$ is the input admittance of a two-port network at 1–2 loaded on the admittance Y_L. Given that $I_2 = -Y_L V_2$, the expression for Y_{in} is defined from Eq. (6.1):

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22} + Y_L} \tag{6.3}$$

The output power dissipated in a load is defined as

$$P_L = 0.5V_2^2 \mathrm{Re}Y_L \tag{6.4}$$

As a result, the operating power gain G_P can be written as follows:

$$G_P = \frac{P_L}{P_{in}} = \frac{|Y_{21}|^2 \mathrm{Re}Y_L}{|Y_{22} + Y_L|^2 \mathrm{Re}Y_{in}} \tag{6.5}$$

The operating power gain G_P does not depend on the source parameters and characterizes only the effectiveness of the power delivery from the input port of the active device to the load. This gain helps to evaluate the gain property of a multistage amplifier when the overall operating power gain $G_{P(total)}$ is equal to the product of each stage G_P.

The transducer power gain G_T includes an assumption of conjugate matching of the load and the source. This means that $Y_{in} = Y_S^*$, where Y_S^* is the source admittance conjugate matched to the input port of the active device Y_{in}. As a result, the power available from the source is

$$P_S = \frac{I_S^2}{8\mathrm{Re}Y_S} \tag{6.6}$$

If $I_S = Y_S V_1 + I_1$, then using Eq. (6.1), the expression for the source current I_S can be defined as follows:

$$I_S = \frac{(Y_{11} + Y_S)(Y_{22} + Y_L) - Y_{12}Y_{21}}{Y_{22} + Y_L} V_1 \tag{6.7}$$

Using Eqs. (6.4) and (6.7), the transducer power gain G_T can be written in the following form:

$$G_T = \frac{P_L}{P_S} = \frac{4\left|Y_{21}\right|^2 \mathrm{Re}Y_S \mathrm{Re}Y_L}{\left|(Y_{11}+Y_S)(Y_{22}+Y_L)-Y_{12}Y_{21}\right|^2} \tag{6.8}$$

Finally, the expressions for G_P and G_T and the input and output impedances have the same analytical forms for a system of Z-parameters. Thus, by using the immittance W-parameters they can be generalized as follows:

$$W_{in} = W_{11} - \frac{W_{12}W_{21}}{W_{22}+W_L} \tag{6.9}$$

$$W_{out} = W_{22} - \frac{W_{12}W_{21}}{W_{11}+W_S} \tag{6.10}$$

$$G_P = \frac{\left|W_{21}\right|^2 \mathrm{Re}W_L}{\left|W_{22}+W_L\right|^2 \mathrm{Re}W_{in}} \tag{6.11}$$

$$G_T = \frac{4\left|W_{21}\right|^2 \mathrm{Re}W_S \mathrm{Re}W_L}{\left|(W_{11}+W_S)(W_{22}+W_L)-W_{12}W_{21}\right|^2} \tag{6.12}$$

From Eqs. (6.9) and (6.10) it follows that if $W_{12}=0$, then $W_{in}=W_{11}$ and $W_{out}=W_{22}$. As a result, in the case of conjugate matching at the input and output ports of the active device, the following expression for MAG is obtained from Eq. (6.11) or (6.12):

$$MAG = \frac{\left|W_{21}\right|^2}{4\mathrm{Re}W_{11}\mathrm{Re}W_{22}} \tag{6.13}$$

the magnitude of which depends only on the active device immittance parameters.

The device simplified π-hybrid equivalent circuit shown in Fig. 6.3 provides an example for a conjugately matched BJT power amplifier. By setting the device reverse impedance equal to zero, and taking into account that it is necessary to provide $R_S = \mathrm{Re}Z_{in}$ and $L_{in} = -\mathrm{Im}Z_{in}/\omega$ for input matching and $R_L = \mathrm{Re}Z_{out}$ and $L_{out} = -\mathrm{Im}Z_{out}/\omega$ for output matching, the transducer power gain can be evaluated as

$$G_T = \left(\frac{f_T}{f}\right)^2 \frac{1}{8\pi f_T r_b C_\mu} \tag{6.14}$$

where $f_T = g_m/2\pi C_\pi$. Equation (6.14) gives a well-known expression for the maximum operating frequency of the BJT device where the

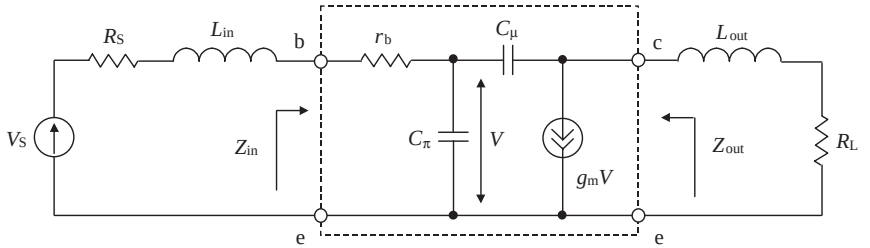

Figure 6.3 Simplified common-emitter equivalent circuit of matched bipolar power amplifier.

maximum available gain is equal to unity:

$$f_{\max} = \sqrt{\frac{f_T}{8\pi r_b C_\mu}} \tag{6.15}$$

Consider the device equivalent circuit with $C_{gd} = 0$ shown in Fig. 6.4 as an example for a conjugately matched FET power amplifier. The active device Y-parameters in this case are as follows: $Y_{11} = j\omega C_{gs}/(1+j\omega R_{gs}C_{gs})$, $Y_{12} = 0$, $Y_{21} = g_m/(1+j\omega R_{gs}C_{gs})$, and $Y_{22} = (1/R_{ds})+j\omega C_{ds}$. For input matching it is necessary to set $R_S = R_{gs}$ and $L_{in} = 1/\omega^2 C_{gs}$; for output matching $R_L = R_{ds}$ and $L_{out} = 1/\omega^2 C_{ds}$. Thus, the transducer power gain can be easily evaluated as

$$G_T(C_{gd} = 0) = MAG = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{4R_{gs}} \tag{6.16}$$

where $f_T = g_m/2\pi C_{gs}$. Equation (6.16) gives a well-known expression for the maximum operating frequency of the FET device on which the maximum available gain is equal to unity:

$$f_{\max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_{gs}}} \tag{6.17}$$

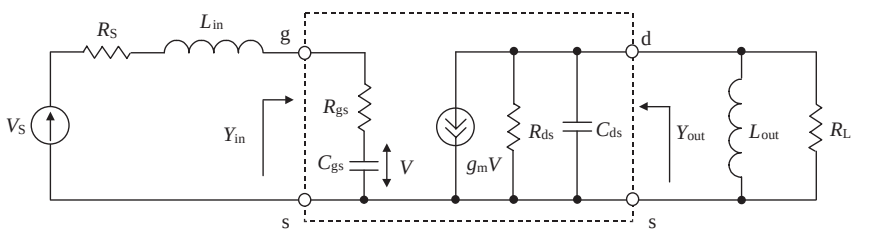

Figure 6.4 Simplified common-source equivalent circuit of matched FET power amplifier.

As a result, the gain of a conjugately matched both BJT and FET power amplifier drops off as $1/f^2$ or 6 dB per octave. Therefore $G_T(f)$ can be easily evaluated at frequency f if the gain is known at frequency f_T in the following form:

$$G_T(f) = G_T(f_T)\left(\frac{f_T}{f}\right)^2 \tag{6.18}$$

It should be noted that the previous analysis is based on the small-signal consideration when generally nonlinear device current source as a function of the input and output voltages simultaneously can be characterized by the transconductance as a function of the input voltage only and the output differential resistance as a function of the output voltage only (see Fig. 6.4). This is a result of a Taylor's series expansion of the output current as a function of the input and output voltages, maintaining only the dc and linear components. Such an approach helps us to understand and derive the maximum achievable power amplifier parameters. In a common case, for conjugate matching procedure, the device output immittance under large-signal consideration should be calculated using Fourier analysis of the output current and voltage fundamental components.

Gain and Stability

Power amplifier design aims for maximum power gain and efficiency for a given value of output power with a predictable degree of stability. Instability of the power amplifier will lead to undesired parasitic oscillations and, as a result, to the distortion of outcoming signal. One of the main reasons for amplifier instability is a positive feedback from output to input through the intrinsic active device capacitance, through the inductance of a common-grounded active device electrode and also through external circuit elements. Consequently, a stability analysis is crucial to any power amplifier design, especially at RF and microwave frequencies.

According to the immittance approach to the stability analysis of the active two-port network, it is necessary and sufficient for its unconditional stability that the following system of equations can be satisfied for the given active device with both open-circuited input and output ports:

$$\begin{cases} \mathrm{Re}[W_S(\omega) + W_{in}(\omega)] > 0 \\ \mathrm{Im}[W_S(\omega) + W_{in}(\omega)] = 0 \end{cases} \tag{6.19}$$

or

$$\begin{cases} \mathrm{Re}[W_L(\omega) + W_{out}(\omega)] > 0 \\ \mathrm{Im}[W_L(\omega) + W_{out}(\omega)] = 0 \end{cases} \tag{6.20}$$

In the case of the opposite signs in Eqs. (6.19) and (6.20) the active two-port network can be treated as unstable or potentially unstable.

When $\mathrm{Re}[W_S(\omega)] > 0$ and $\mathrm{Re}[W_L(\omega)] > 0$, the requirements of amplifier unconditional stability can be simplified to

$$\mathrm{Re}[W_{in}(\omega)] > 0 \qquad \mathrm{Re}[W_{out}(\omega)] > 0 \tag{6.21}$$

According to Eqs. (6.9) and (6.10), the value of $\mathrm{Re}W_{in}$ depends on the load immittance W_L whereas the variation of the source immittance W_S leads to the change of $\mathrm{Re}W_{out}$. Therefore, if there is a negative value of $\mathrm{Re}W_{out}$, the active two-port network will be potentially unstable in the definite limits of the values of immittance W_S. Consequently, for unconditionally stable amplifier operation mode, it is necessary to satisfy the following condition:

$$\mathrm{Re}[W_{out}(\omega)|_{min} > 0 \tag{6.22}$$

Analyzing Eq. (6.10) on extremum, we find the minimum positive value of $\mathrm{Re}W_{out}$ for a given constant value of $\mathrm{Re}W_S$ by solving the equation $\partial \mathrm{Re}W_{out}/\partial \mathrm{Im}W_S = 0$:

$$\mathrm{Re}W_{out} = \mathrm{Re}W_{22} - \frac{|W_{12}W_{21}| + \mathrm{Re}\,(W_{12}W_{21})}{2\mathrm{Re}\,(W_{11} + W_S)} \tag{6.23}$$

The fraction at the right part of Eq. (6.23) as a function of $\mathrm{Re}W_S$ can take a maximum negative value when $\mathrm{Re}W_S = 0$, resulting in

$$\mathrm{Re}W_{out} = \mathrm{Re}W_{22} - \frac{|W_{12}W_{21}| + \mathrm{Re}\,(W_{12}W_{21})}{2\mathrm{Re}W_{11}} \tag{6.24}$$

Consequently, the requirement of a positive minimum value of $\mathrm{Re}W_{out}$ expressed by Eq. (6.22) can be written as follows:

$$2\mathrm{Re}W_{11}\mathrm{Re}W_{22} - |W_{12}W_{21}| - \mathrm{Re}\,(W_{12}W_{21}) > 0 \tag{6.25}$$

This same result can be obtained by optimizing the immittance W_{in} as a function of W_L. From Eq. (6.25) it follows that under such a condition the active device is unconditionally stable at any frequencies where this condition is performed regardless of any values of the source and load immittances, W_S and W_L. Normalizing Eq. (6.25) allows us to introduce the device stability factor [1]:

$$K = \frac{2\mathrm{Re}W_{11}\mathrm{Re}W_{22} - \mathrm{Re}\,(W_{12}W_{21})}{|W_{12}W_{21}|} \tag{6.26}$$

which shows a stability margin indicating how far from zero value are the real parts in Eqs. (6.19) and (6.20) being positive.

It should be noted that the applicability of Eqs. (6.25) and (6.26) is restricted to the following requirements:

$$\mathrm{Re}[W_{11}(\omega)] > 0 \qquad \mathrm{Re}[W_{22}(\omega)] > 0 \tag{6.27}$$

A comparison of Eq. (6.25) and Eq. (6.26) shows that an active device is unconditionally stable if $K > 1$ and potentially unstable if $K < 1$. Taking into account the condition stated in Eq. (6.27) as well as the following inequality,

$$|\mathrm{Re}(W_{12}W_{21})| \le |W_{12}W_{21}| \tag{6.28}$$

the smallest possible value of the device stability factor can be defined as $K = -1$. As a result, the values of K can be arranged only in the interval $[-1, \infty)$.

When the active device is potentially unstable, an improvement of amplifier stability can be provided with the appropriate choice of source and load immittances, W_S and W_L. The circuit stability factor K_T in this case is defined in the same way as the device stability factor K, but taking into account $\mathrm{Re}W_S$ and $\mathrm{Re}W_L$ along with the device parameters. The circuit stability factor is given by

$$K_T = \frac{2\mathrm{Re}\,(W_{11} + W_S)\,\mathrm{Re}\,(W_{22} + W_L) - \mathrm{Re}\,(W_{12}W_{21})}{|W_{12}W_{21}|} \tag{6.29}$$

If the circuit stability factor $K_T \ge 1$, the amplifier is unconditionally stable. If $K_T < 1$, the amplifier is potentially unstable. The value of $K_T = 1$ corresponds to the border of the circuit unconditional stability. The values of the circuit stability factor and device stability factor are the same, i.e., $K_T = K$, if $\mathrm{Re}W_S = \mathrm{Re}W_L = 0$.

When the active device stability factor $K > 1$, the power gain G_P has to be maximized. The operating power gain G_P is defined in Eq. (6.11), which indicates that it is a function of $\mathrm{Re}W_L$ and $\mathrm{Im}W_L$. Analyzing Eq. (6.11) on extremum, it is possible to find optimum values $\mathrm{Re}W_L^\circ$ and $\mathrm{Im}W_L^\circ$, at which the operating power gain G_P is maximal by solving the following system of two equations:

$$\frac{\partial G_P}{\partial \mathrm{Re}W_L} = 0 \qquad \frac{\partial G_P}{\partial \mathrm{Im}W_L} = 0 \tag{6.30}$$

The optimum values $\mathrm{Re}W_L^\circ$ and $\mathrm{Im}W_L^\circ$ depend on the immittance parameters of the active device and the device stability factor [1, 2]:

$$\mathrm{Re}W_L^\circ = \frac{|W_{12}W_{21}|}{2\mathrm{Re}W_{11}}\sqrt{K^2 - 1} \tag{6.31}$$

$$\mathrm{Im}W_L^\circ = \frac{\mathrm{Im}(W_{12}W_{21})}{2\mathrm{Re}W_{11}} - \mathrm{Im}W_{22} \tag{6.32}$$

Substituting the obtained values of $\mathrm{Re}W_{\mathrm{L}}^{\circ}$ and $\mathrm{Im}W_{\mathrm{L}}^{\circ}$ into Eq. (6.11) yields an equation for calculating the maximum value of G_{Pmax}:

$$G_{\mathrm{Pmax}} = \left|\frac{W_{21}}{W_{12}}\right| / \left(K + \sqrt{K^2 - 1}\right) \tag{6.33}$$

G_{Pmax} can be achieved only if $K > 1$ and $G_{\mathrm{Pmax}}^{\mathrm{A}} = |W_{21}/W_{12}|$ when $K = 1$.

If the source is conjugately matched with the input of the active device, the following conditions must be satisfied:

$$\mathrm{Re}W_{\mathrm{S}} = \mathrm{Re}W_{\mathrm{in}} \qquad \mathrm{Im}W_{\mathrm{S}} + \mathrm{Im}W_{\mathrm{in}} = 0 \tag{6.34}$$

Then, by substituting these expressions into Eq. (6.9), the optimum values $\mathrm{Re}W_{\mathrm{S}}^{\circ}$ and $\mathrm{Im}W_{\mathrm{S}}^{\circ}$ can be obtained as functions of the immittance parameters of the active device and the device stability factor:

$$\mathrm{Re}W_{\mathrm{S}}^{\circ} = \frac{|W_{12}W_{21}|}{2\mathrm{Re}W_{22}}\sqrt{K^2 - 1} \tag{6.35}$$

$$\mathrm{Im}W_{\mathrm{S}}^{\circ} = \frac{\mathrm{Im}(W_{12}W_{21})}{2\mathrm{Re}W_{22}} - \mathrm{Im}W_{11} \tag{6.36}$$

A comparison of Eqs. (6.35) and (6.36) with Eqs. (6.31) and (6.32) shows that these expressions are identical. Consequently, the power amplifier with an unconditionally stable active device realizes a maximum power gain operation only if the input and output of the active device are conjugately matched with the source and load, respectively. As a result, for the lossless input matching circuit when the power available at the source is equal to the power delivered to the input ports of the active device, i.e., $P_{\mathrm{S}} = P_{\mathrm{in}}$, the maximum operating power gain is equal to the maximum transducer power gain, i.e., $G_{\mathrm{Pmax}} = G_{\mathrm{Tmax}}$.

Stabilization Circuit Technique

Frequency domains of BJT potential instability

Domains of potential instability include the operating frequency ranges where the active device stability factor is equal to $K < 1$. Within the bandwidth of such a frequency domain, parasitic oscillations can occur, defined by the internal positive feedback and operating conditions of the active device. Therefore, it is very important to determine the influence of the feedback parameters of the transistor equivalent circuit on the origin of the self-oscillation conditions and to establish possible circuit configurations of the parasitic oscillators.

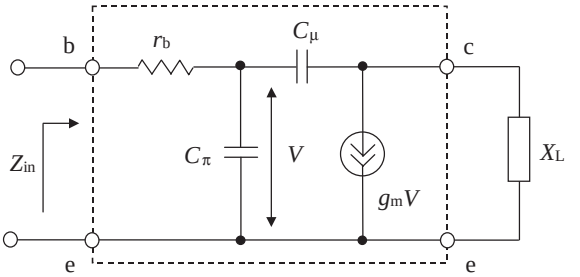

Figure 6.5 Simplified π-hybrid equivalent circuit of loaded bipolar transistor.

The BJT stability factor expressed through Z-parameters can be written in the following form:

$$K = \frac{2R_{11}R_{22} - \mathrm{Re}(Z_{12}Z_{21})}{|Z_{12}Z_{21}|} \tag{6.37}$$

where $R_{11} = \mathrm{Re}Z_{11}$, and $R_{22} = \mathrm{Re}Z_{22}$.

Consider the simplified π-hybrid equivalent circuit of the bipolar transistor shown in Fig. 6.5. The only feedback element that influences the transistor stability factor is the collector-base capacitance C_μ. Such a simplification of the equivalent circuit leads to negligible errors at the frequency range of $f \le 0.3f_T$. At higher frequencies, an influence of the parasitic reactive parameters, including the emitter lead inductance L_e, must be taken into account.

The impedance Z-parameters of this two-port network equivalent circuit are:

$$\begin{aligned}
Z_{11} &= r_b + \frac{1}{g_m} \Big/ \left(1 + j\frac{\omega}{\omega_T}\right) \\
Z_{12} &= \frac{1}{g_m} \Big/ \left(1 + j\frac{\omega}{\omega_T}\right) \\
Z_{21} &= \left(\frac{1}{g_m} - \frac{1}{j\omega C_\mu}\right) \Big/ \left(1 + j\frac{\omega}{\omega_T}\right) \\
Z_{22} &= \left(\frac{1}{g_m} + \frac{1}{\omega_T C_\mu}\right) \Big/ \left(1 + j\frac{\omega}{\omega_T}\right)
\end{aligned} \tag{6.38}$$

where $\omega_T = 2\pi f_T$.

By using the ratios for Z-parameters presented in Eq. (6.38), the BJT stability factor expressed through the parameters of the transistor

equivalent circuit can be written as

$$K = 2r_b g_m \frac{1 + \frac{g_m}{\omega_T C_\mu}}{\sqrt{1 + \left(\frac{g_m}{\omega C_\mu}\right)^2}} \tag{6.39}$$

The device stability factor increases almost proportionally with the frequency at low frequencies and achieves its maximum value of

$$K = 2r_b g_m \left(1 + \frac{g_m}{\omega_T C_\mu}\right) \tag{6.40}$$

at higher frequencies.

Equation (6.40) shows a ratio between the maximum device stability factor K and feedback capacitance C_μ, and analytically demonstrates the effect of the increase in the BJT stability factor with the decrease in the collector-base feedback capacitance.

At very low frequencies, the BJT transistors are potentially stable and the fact that $K \to 0$ as $f \to 0$ can be explained by simplifying the BJT equivalent circuit. In practice, at low frequencies, it is necessary to take into account the dynamic base-emitter resistance r_π and Early collector-emitter resistance r_{ce}, the presence of which substantially increases the value of the device stability factor. This means that—initially with the increase of the frequency—the magnitude of K decreases and then begins to increase according to Eq. (6.39). This gives the only one unstable frequency domain with $K < 1$ and low boundary frequency f_{p1}. Its bandwidth depends on the parameters of the BJT equivalent circuit.

Equating the device stability factor K with unity allows us to determine the high boundary frequency of a frequency domain of the BJT potential instability as follows:

$$f_{p2} = \frac{g_m}{2\pi C_\mu} \Big/ \sqrt{(2r_b g_m)^2 \left(1 + \frac{g_m}{\omega_T C_\mu}\right)^2 - 1} \tag{6.41}$$

For conditions when $r_b g_m > 1$ and $g_m > \omega_T C_\mu$, the expression for the high boundary frequency f_{p2} is simplified to

$$f_{p2} \cong \frac{1}{4\pi r_b C_\pi} \tag{6.42}$$

At higher frequencies, the presence of the parasitic reactive intrinsic transistor parameters and package parasitics can be of great importance to the power amplifier stability. The parasitic emitter lead inductance L_e shown in Fig. 6.6 has a major effect upon the device stability factor.

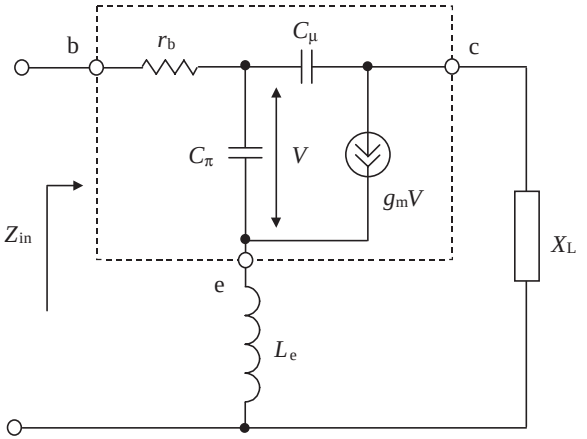

Figure 6.6 Simplified bipolar π-hybrid equivalent circuit with emitter lead inductance.

The presence of L_e leads to the appearance of the second frequency domain of potential instability at higher frequencies. The analytical calculations using Z-parameters are complicated, and for our purposes it is sufficient to present only the final expression needed to calculate the low and high boundary frequencies, f_{p3} and f_{p4}, of the second frequency domain of the BJT potential instability [3]:

$$f_{p3,4} = f_T \sqrt{\frac{1 - 4\omega_T r_b C_\mu}{8\omega_T r_b C_\mu} \mp \sqrt{\left(\frac{1 - 4\omega_T r_b C_\mu}{8\omega_T r_b C_\mu}\right)^2 - \frac{1 + \kappa}{\omega_T r_b C_\mu \kappa^2}}} \qquad (6.43)$$

where $\kappa = \omega_T L_e / r_b$.

It follows that the second frequency domain of potential instability can be realized only under the definite ratios between the factors κ and $\omega_T r_b C_\mu$. For example, for sufficiently small values of $\omega_T r_b C_\mu$, the second domain cannot be realized even under the large values of L_e. With the decrease of L_e, the second frequency domain of potential instability narrows and disappears at some certain value of κ. The further decrease of L_e leads only to widening of the first frequency domain of potential instability and to an increase of the magnitude of the device stability factor K.

A condition to calculate the optimum value of κ_o (when the second frequency domain of the device potential instability disappears) is found by equating the expression under the second radical sign in Eq. (6.43)

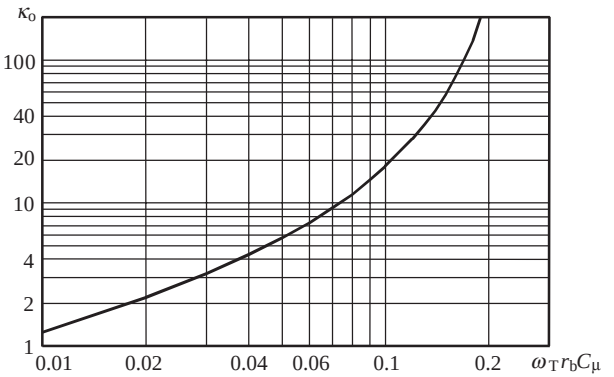

Figure 6.7 Generalized dependence of κ_o versus factor of $\omega_T r_b C_\mu$.

with zero:

$$\kappa_o = \frac{32\omega_T r_b C_\mu}{(1 - 4\omega_T r_b C_\mu)^2}\left[1 + \sqrt{1 + \frac{(1 - 4\omega_T r_b C_\mu)^2}{16\omega_T r_b C_\mu}}\right] \tag{6.44}$$

Figure 6.7 shows the generalized dependence of κ_o as a function of the factor of $\omega_T r_b C_\mu$ in accordance with Eq. (6.44). By using the curve plotted in Fig. 6.7, it is very convenient to define the presence or absence of the second domain of the device potential instability when the value of $\omega_T r_b C_\mu$ is known. As a result, the second domain is lacking for all values of L_e when $\omega_T r_b C_\mu \geq 0.25$. The same situation occurs when $\omega_T r_b C_\mu < 0.25$ but for values of L_e at which $\kappa < \kappa_o$. It should be noted that the value of L_e, which corresponds to the condition of $\kappa = \kappa_o$, represents the best case scenario from the viewpoint of the frequency stability conditions. The first domain of the device instability is narrower than when $L_e = 0$. The second domain of the device instability is not realized yet because of the sufficiently small value of L_e.

An appearance of the second frequency domain of the device potential instability is the result of the appropriate change in the device feedback phase conditions and takes place only under a simultaneous effect of the collector-base capacitance C_μ and emitter lead inductance L_e. If the effect of one of these factors is lacking, the active device is characterized by only the first domain of its potential instability.

To find the equivalent circuit of parasitic oscillators, we first consider the input impedance Z_{in} of the bipolar transistor loaded on reactive impedance X_L for the simplified case when $L_e = 0$, as shown in Fig. 6.5. Using the Z-parameters of the bipolar transistor from Eq. (6.38) and

Eq. (6.9), the input impedance Z_{in} can be expressed as

$$Z_{\text{in}} = r_{\text{b}} + \frac{1}{g_{\text{m}}} \frac{1}{1 + j\dfrac{\omega}{\omega_{\text{T}}}} \frac{1 + \dfrac{g_{\text{m}}}{\omega C_{\mu}}}{1 + \dfrac{g_{\text{m}}}{\omega_{\text{T}} C_{\mu}}(1 - \omega C_{\mu} X_{\text{L}}) + j g_{\text{m}} X_{\text{L}}} \tag{6.45}$$

The parasitic oscillations occur only if the values of the source and load reactive impedances are $\text{Im}Z_{\text{in}} < 0$ and $X_{\text{L}} > 0$. Consequently, the equivalent circuit of the parasitic oscillator represents the inductive oscillatory circuit, where inductive elements L_{S} and L_{L} in combination with the collector-base capacitance C_{μ} may form a Hartley oscillator. The equivalent circuit of such an oscillator is shown in Fig. 6.8(a). The ratio of the boundary values of the source and load inductances, L_{S} and L_{L}, which correspond to the high frequency boundary of first potential instability domain, can be approximately evaluated as [3]

$$\frac{L_{\text{L}}}{L_{\text{S}}} \approx \frac{1}{\omega_{\text{T}} r_{\text{b}} C_{\mu}} \tag{6.46}$$

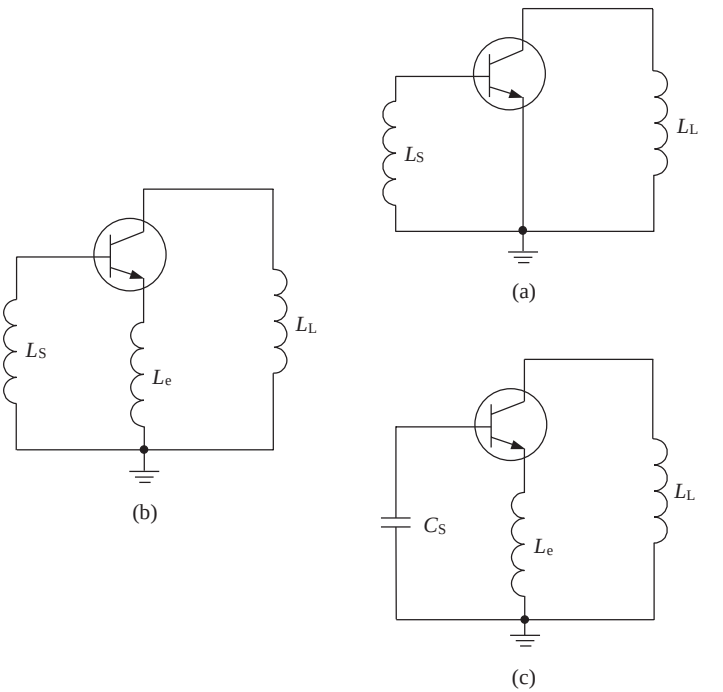

Figure 6.8 Equivalent circuits of parasitic oscillators.

An analysis of Eq. (6.46) for bipolar transistor results in a very important practical recommendation: the more a value of the collector choke inductance exceeds a value of the base choke inductance, the more likely are low frequency parasitic oscillators. Therefore, it is advisable to increase a value of the base choke inductance and to decrease a value of the collector one.

The presence of the emitter lead inductance L_e leads to the narrowing of the first frequency domain of the potential instability, which is limited to the high boundary frequency f_{p2}, and can contribute to the appearance of the second one at higher frequencies. The analytical calculation of the input and output impedances in this case is quite complicated. The final conclusions are:

- The parasitic oscillator that corresponds to the first frequency domain of the device potential instability can be realized only if the source and load reactances are inductive, i.e., $\mathrm{Im}Z_S > 0$ and $\mathrm{Im}Z_L > 0$, with the equivalent circuit of such a parasitic oscillator shown in Fig. 6.8(*b*).
- The parasitic oscillator corresponding to the second frequency domain of the device potential instability can be realized only if the source reactance is capacitive, i.e., $\mathrm{Im}Z_S < 0$; the load reactance must be inductive, i.e., $\mathrm{Im}Z_L > 0$. The equivalent circuit is shown in Fig. 6.8(*c*).

The emitter lead inductance L_e is an element of fundamental importance for the parasitic oscillator that corresponds to the second frequency domain of the device potential instability. It changes the phase conditions so that it becomes possible to perform the phase balance condition at high frequencies. Therefore, decreasing the value of L_e is the most effective way to prevent the parasitic self-oscillation in the frequency range of $f > f_{p3}$.

Frequency domains of MOSFET potential instability

It is convenient to represent the MOSFET stability factor through *Y*-parameters:

$$K = \frac{2G_{11}G_{22} - \mathrm{Re}\,(G_{12}G_{21})}{|Y_{12}Y_{21}|} \tag{6.47}$$

where $G_{11} = \mathrm{Re}Y_{11}$, $G_{22} = \mathrm{Re}Y_{22}$.

To determine the frequency domain of MOSFET potential instability provided with internal feedback elements, it is necessary to consider the equivalent circuit of the active device (without parasitic lead inductances) shown in Fig. 6.9. The only feedback element is the gate-drain capacitance C_{gd}. Negligible errors occur at the frequency range of

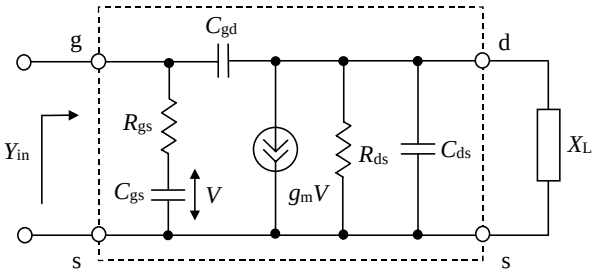

Figure 6.9 Simplified MOSFET equivalent circuit.

$f \leq 0.3 f_T$ for such a simplification. At higher frequencies, the influence of the parasitic reactive parameters (including, first of all, the source inductance L_S) should be taken into account.

The admittance Y-parameters of this two-port network equivalent circuit can be expressed as follows:

$$\begin{aligned} Y_{11} &= \frac{j\omega C_{gs}}{1 + j\omega R_{gs} C_{gs}} + j\omega C_{gd} \qquad Y_{12} = -j\omega C_{gd} \\ Y_{21} &= \frac{g_m}{1 + j\omega R_{gs} C_{gs}} - j\omega C_{gd} \quad Y_{22} = \frac{1}{R_{ds}} + j\omega (C_{ds} + C_{gd}) \end{aligned} \tag{6.48}$$

By using the ratios for Y-parameters presented in Eq. (6.48), the MOSFET stability factor expressed through the parameters of the transistor equivalent circuit can be given by

$$K = \left[1 + \frac{2}{g_m R_{ds}} \left(1 + \frac{C_{gs}}{C_{gd}}\right)\right] \frac{\omega R_{gs} C_{gs}}{\sqrt{1 + \left(\omega R_{gs} C_{gs}\right)^2}} \tag{6.49}$$

The device stability factor increases linearly from zero frequency and achieves its maximum constant value of

$$K = \left[1 + \frac{2}{g_m R_{ds}} \left(1 + \frac{C_{gs}}{C_{gd}}\right)\right] \tag{6.50}$$

at higher frequencies. Equation (6.50) determines the influence of feedback capacitance C_{gd} and transconductance g_m on the maximum device stability factor K, which increases with the decrease of both these parameters.

For MOSFET transistors, the fact that $K \to 0$ when $f \to 0$ can be explained by simplifying its equivalent circuit. At very low frequencies, it is necessary to take into account the gate leakage resistance R_{leak}. This means that, initially, with the increase of the frequency, the magnitude of K decreases and then increases according to Eq. (6.49). Consequently,

this gives the only one unstable frequency domain, with $K < 1$ and low boundary frequency f_{p1}, the bandwidth of which depends on the parameters of the MOSFET equivalent circuit. Due to the very small ratio of R_{gs}/R_{leak}, of about 10^{-6}, the value of the low boundary frequency f_{p1} is sufficiently small:

$$f_{p1} \approx 10^{-6}/2\pi R_{gs}C_{gs} \tag{6.51}$$

By equating the stability factor K with unity in Eq. (6.49), it is possible to determine the high boundary frequency of a frequency domain of the MOSFET potential instability as follows [4]:

$$f_{p2} = \frac{1}{4\pi R_{gs}C_{gs}} \frac{g_m R_{ds}}{\sqrt{1+\frac{C_{gs}}{C_{gd}}}} \frac{1}{\sqrt{1+\frac{C_{gs}}{C_{gd}}+g_m R_{ds}}} \tag{6.52}$$

For usually available conditions (for power MOSFET devices) when $g_m R_{ds} = 10 \div 30$ and $C_{gd}/C_{gs} = 0.1 \div 0.2$, the expression to evaluate the high boundary frequency f_{p2} can be simplified to approximately

$$f_{p2} \approx \frac{1}{4\pi R_{gs}C_{gs}} \tag{6.53}$$

It should be noted that power MOSFET devices have a substantially higher value of $g_m R_{ds}$ at small values of drain current than at high values. Consequently, at small values of drain current, the MOSFET device is characterized by a wider domain of potential instability. This domain is significantly wider than the same first domain of the potential instability of the bipolar transistor.

The parasitic source inductance L_s (shown in Fig. 6.10) creates a second frequency domain of potential instability at higher frequencies. By using numerical calculations, the low and high boundary frequencies, f_{p3} and f_{p4}, of the second frequency domain of the MOSFET potential instability can be predicted. Calculations are performed for typical values of the following MOSFET equivalent circuit parameters: $C_{ds}/C_{gs} = 0.5$, $R_d/R_{gs} = 0.75$, $g_m R_{gs} = 2$, and $C_{gd}/C_{gs} = 0.1$. Figure 6.11 presents the dependencies of the device stability factor K on the normalized frequency $\omega R_{gs}C_{gs}$ for different values of $\kappa = \omega_T L_s/R_{gs}$ [4].

It follows that the second frequency domain of potential instability can be realized only under the definite values of κ. For example, with the decrease of L_s, the second frequency domain of potential instability becomes narrow, disappearing at $\kappa \cong 3.5$. The further decrease of L_s leads to a widening of the first frequency domain of potential instability and an increase in the magnitude of the device stability factor K.

In addition, an analysis of the influence of the source and load conductances, G_S and G_L, on the amplifier stability shows that the first

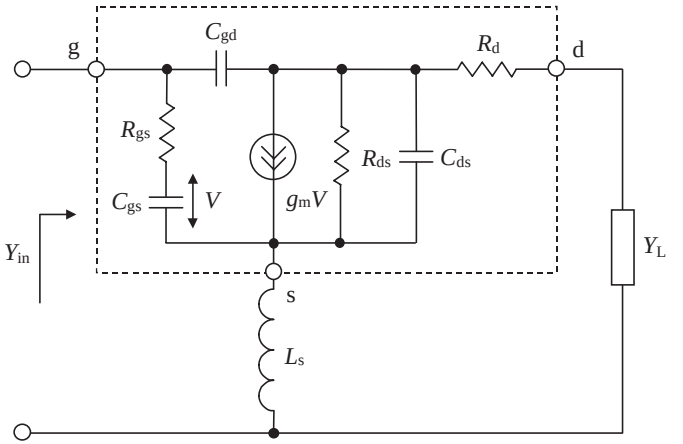

Figure 6.10 Simplified MOSFET equivalent circuit with source lead inductance.

frequency domain of the potential instability disappears when $1/(G_S R_{gs}) = 2 \div 5$ and $g_m/G_L = 5 \div 10$. The second frequency domain of potential instability can disappear when $1/(G_S R_{gs}) \approx 2$ and $g_m/G_L \approx 2$.

To define the equivalent circuit of parasitic oscillators, we have to consider the input admittance Y_{in} of the MOSFET device loaded on reactive admittance $B_L = \mathrm{Re}Y_L$, firstly for the simplified case when $L_s = 0$ as shown in Fig. 6.9. Using the device Y-parameters from Eq. (6.48) and Eq. (6.9), the input admittance Y_{in} can be presented as follows:

$$Y_{in} = \frac{j\omega C_{gs}}{1 + j\omega R_{gs} C_{gs}} \times \left[1 + g_m R_{ds} \frac{1 - j\frac{\omega}{\omega_T}(1 + j\omega R_{gs} C_{gs})}{1 + j\omega R_{ds} C_{ds} \left(1 + \frac{C_{gd}}{C_{ds}} + \frac{B_L}{\omega C_{ds}} \right)} \right] \tag{6.54}$$

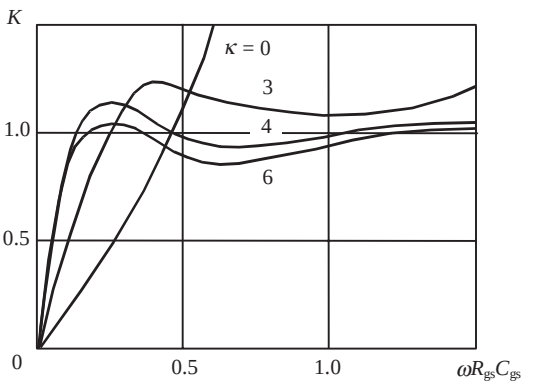

Figure 6.11 Device stability factor K versus factor of $\omega R_{gs} C_{gs}$.

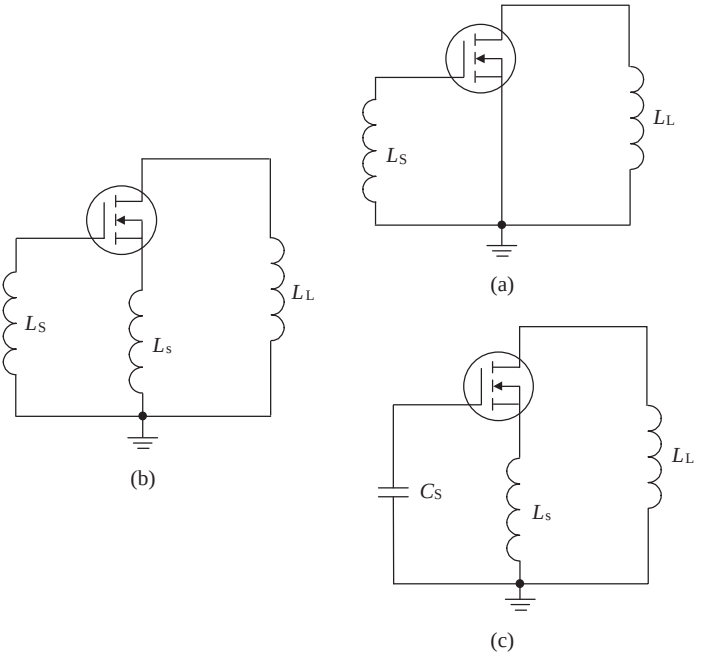

Figure 6.12 Equivalent circuits of parasitic oscillators.

The parasitic oscillations can arise only when $\mathrm{Im}Y_{\mathrm{in}} > 0$ and $B_{\mathrm{L}} < 0$. Consequently, the equivalent circuit of the parasitic oscillator represents the inductive oscillatory circuit, where inductive elements L_{S} and L_{L} in combination with the gate-drain capacitance C_{gd} may form a Hartley oscillator. The equivalent circuit of such an oscillator is shown in Fig. 6.12(a). The presence of a source lead inductance L_{s} leads to the appearance of a second frequency domain of the potential instability at higher frequencies. As a result, the parasitic oscillator corresponding to the first frequency domain of the device potential instability can be realized only if the source and load reactances are inductive, i.e., $\mathrm{Im}B_{\mathrm{S}} < 0$ and $\mathrm{Im}B_{\mathrm{L}} < 0$, with the equivalent circuit of such a parasitic oscillator shown in Fig. 6.12(b). The parasitic oscillator corresponding to the second frequency domain of the device potential instability can be realized only if the source reactance is capacitive, i.e., $\mathrm{Im}B_{\mathrm{S}} > 0$, and if the load reactance is inductive, i.e., $\mathrm{Im}B_{\mathrm{L}} < 0$, with the equivalent circuit shown in Fig. 6.12(c).

Some examples of stabilization circuits

To prevent parasitic oscillations and to provide a stable operation mode of the power amplifier, it is necessary to take into consideration the following common requirements:

- To use an active device with stability factor $K > 1$.
- If it is impossible to choose an active device with $K > 1$, it is necessary to provide the circuit stability factor $K_T > 1$ by the appropriate choice of the real parts of the source and load immittances.
- To disrupt the equivalent circuits of the possible parasitic oscillators.
- To choose such reactive parameters of the matching circuit elements adjacent to the input and output of the active device as are necessary to avoid the self-oscillation conditions.

In theory, the parasitic oscillations can arise on any frequency within the potential instability domains under the definite values of the source and load immittances, W_S and W_L. The frequency dependencies of W_S and W_L are very complicated and very often cannot be predicted exactly, especially in multistage amplifiers. In addition, any significant influence of the stabilization circuit technique on the electrical characteristics of the power amplifier must be avoided. Therefore, it is very difficult to propose a unified approach to provide a stable operation mode for the different power amplifiers. In practice, the parasitic oscillations due to the intrinsic positive feedback in an active device can arise either close to operating frequencies (if they are within the domains of the device potential instability) or at frequencies sufficiently far from the operating frequencies. As a result, the stability analysis of the power amplifier must include the methods to prevent the parasitic oscillations in different frequency ranges:

- At lower frequencies when the frequency of the parasitic oscillation f_p is significantly less than the operating frequency f_0 (i.e., $f_p \ll f_0$)
- At higher frequencies when $f_p \gg f_0$
- Finally, at the operating frequencies when $f_p \approx f_0$

Examples of the bias circuit configurations that can prevent the parasitic oscillations at lower frequencies are given in Fig. 6.13. The main idea in this case is to use a stabilizing resistor R_1 connected either in parallel to a radio-frequency choke L_1 (Fig. 6.13(a)) or together with a series bypass capacitance C_2 in parallel to the power supply (Fig. 6.13(c)). To avoid worsening the electrical characteristics of the power amplifier when the value of R_1 is sufficiently small and comparable with the output immittance of the transistor, it is advisable to use an additional series inductance L_2, as shown in Fig. 6.13(b). The value of L_2 in this case should be approximately equal to $L_2 \cong (5 \div 10)R_1/\pi f_0$. The value of the shunt capacitor C_2 for the bias circuit presented in Fig. 6.13(c) can be chosen from the following condition: $(1/2\pi R_1 f_0) \ll C_2 \ll (1/2\pi R_1 f_p)$, where f_p corresponds to the high boundary frequency f_{p2} of the first

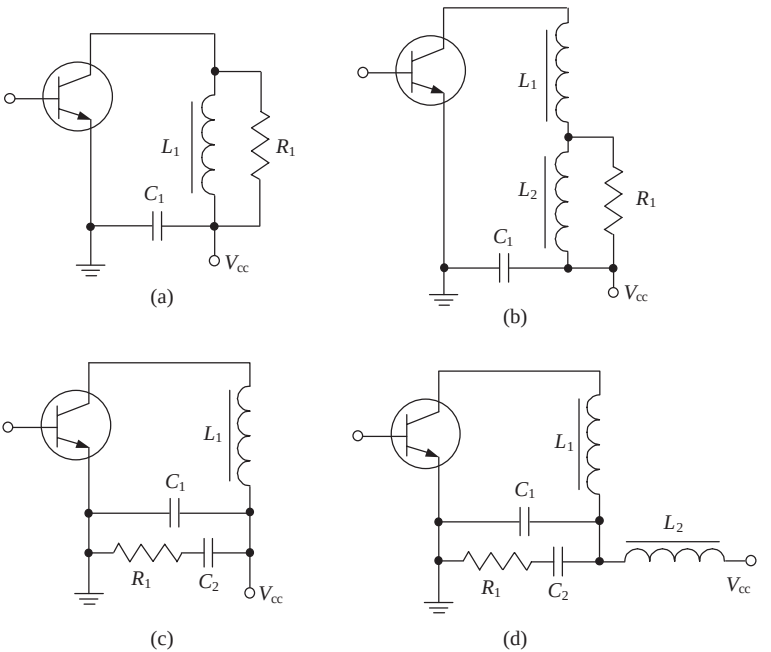

Figure 6.13 Bias circuit configurations preventing low frequency oscillations.

frequency domain of the device potential instability if $f_0 \gg f_{p2}$. When the impedance of the series circuit R_1C_2 is sufficiently high compared with the external power supply impedance, it is advisable to use an additional RF choke L_2 with the following value: $L_2 \gg R_1/2\pi f_p$, as shown in Fig. 6.13(*d*).

The equivalent circuit of the parasitic oscillator at higher frequencies is realized by means of the parasitic reactive parameters of the transistor and power amplifier circuit. The only possible equivalent circuit of such a parasitic oscillator at these frequencies is shown in Fig. 6.8(*c*). It can only be realized if the series emitter lead inductance is present. Consequently, the electrical length of the emitter lead should be reduced as much as possible, or, alternatively, the appropriate reactive immittances at the input and output electrodes of the active device should be provided. For example, it is possible to avoid the parasitic oscillations at these frequencies if the inductive immittance is provided at the input of the transistor. The equivalent circuit of such a power amplifier is shown in Fig. 6.14, where the appropriate choice of input and output matching circuits allows realizing the inductive immittance at the input of the transistor and the capacitive immittance at the output of the transistor at higher frequencies.

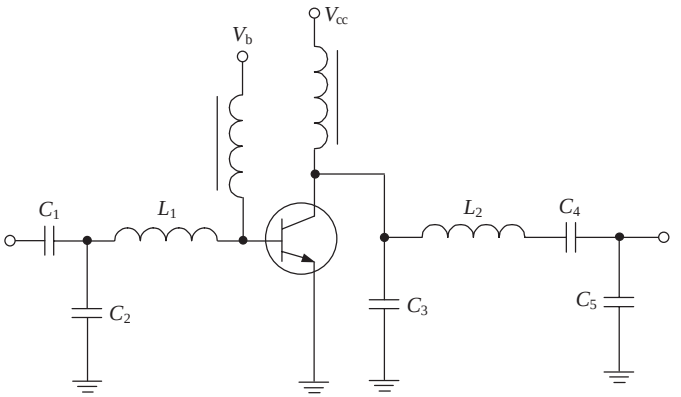

Figure 6.14 Power amplifier circuit schematic preventing high frequency oscillations.

To increase the power amplifier stability, it is possible to use special stabilizing *RLC* circuits, shown in Fig. 6.15. These stabilizing circuits are usually connected between the transistor and matching circuit, where they can be connected in parallel (Fig. 6.15(*a*)) or in series (Fig. 6.15(*b*)) to the transistor output. In both cases the resonant circuit

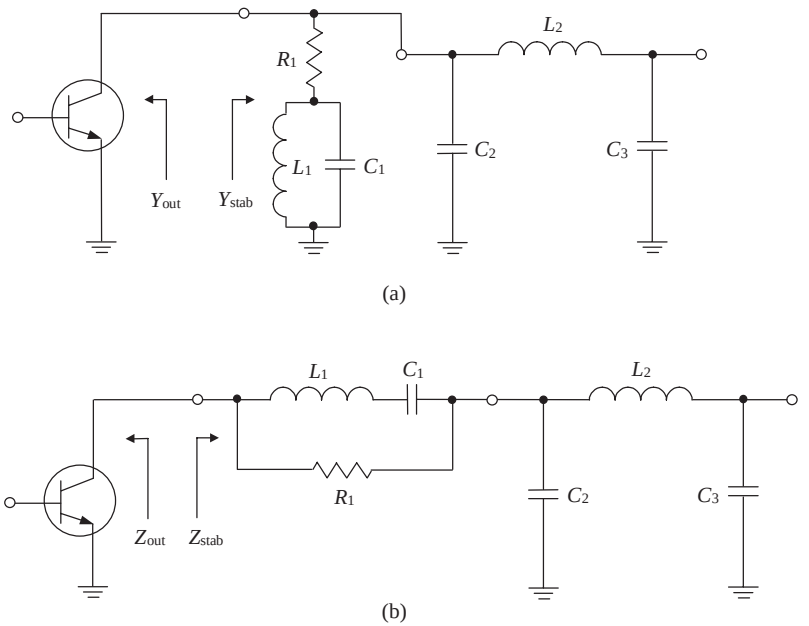

Figure 6.15 Power amplifier schematic with output stabilized *RLC* circuits.

L_1C_1 is tuned to the operating frequency f_0. As a result, the resistor R_1 provides a stabilizing effect beyond the operating frequency bandwidth. The chosen minimum value of R_1 must satisfy the amplifier stability condition $\mathrm{Re}(W_{\mathrm{out}} + W_{\mathrm{stab}}) > 0$. Such stabilizing circuits can be connected at the input of the transistor as well. However, the use of these circuits leads to some changes in the frequency bandwidth: narrowing in the case of the parallel circuit configuration and widening in the case of the series one.

Linearity

To evaluate the nonlinear properties of the power amplifier, first it is necessary to consider the transfer function of the active device in the form of

$$i = f(v) \tag{6.55}$$

where $i(t)$ is the output collector or drain current and $v(t)$ is the input gate-source or base-emitter voltage.

It is convenient to apply a power-series analysis, which is relatively easy to use and which gives a good intuitive sense of the nonlinear behavior of the active device. Assume that the nonlinearity is weak enough that a power series converges. Then, the transfer function $f(v)$ can be approximated by its expansion around a bias voltage V_0 in a Taylor series as follows:

$$f(v) = f(V_0) + \sum_{n=1}^{\infty} \frac{1}{n!} \frac{\partial^{(\mathrm{n})} f(v)}{\partial v^{\mathrm{n}}}\bigg|_{v=V_{\mathrm{o}}} (v - V_0)^{\mathrm{n}} \tag{6.56}$$

The nonlinear properties are determined by a two-tone excitation test signal with components separated slightly in frequency, which can be presented in a common case of unequal amplitudes as

$$v = V_0 + V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \tag{6.57}$$

For first three derivatives, the output signal can be represented by a Taylor series expansion with the appropriate equating of the frequency component terms by

$$i = f(V_0) + \frac{1}{4} \frac{\partial^2 f(v)}{\partial v^2}\bigg|_{v=V_{\mathrm{o}}} \left(V_1^2 + V_2^2\right) + \left[f'(V_0) + \frac{1}{4} \frac{\partial^3 f(v)}{\partial v^3}\bigg|_{v=V_{\mathrm{o}}} \left(\frac{1}{2} V_1^2 + V_2^2\right) \right] V_1 \cos \omega_1 t$$

$$+\left[f'(V_0)+\frac{1}{4}\left.\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_0}\left(V_1^2+\frac{1}{2}V_2^2\right)\right]V_2\cos\omega_2 t$$
$$+\frac{1}{4}\left.\frac{\partial^2 f(v)}{\partial v^2}\right|_{v=V_0}\left(V_1^2\cos 2\omega_1 t+V_2^2\cos 2\omega_2 t\right)$$
$$+\frac{1}{24}\left.\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_0}\left(V_1^3\cos 3\omega_1 t+V_2^3\cos 3\omega_2 t\right)$$
$$+\frac{1}{2}\left.\frac{\partial^2 f(v)}{\partial v^2}\right|_{v=V_0}V_1V_2\cos(\omega_1\pm\omega_2)t$$
$$+\frac{1}{8}\left.\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_0}\left[V_1^2V_2\cos(2\omega_1\pm\omega_2)t+V_1V_2^2\cos(\omega_1\pm 2\omega_2)t\right]\ldots \tag{6.58}$$

The following conclusions can be drawn from the above Taylor series expansion of the active device transfer function:

- A variation of the device bias point is directly proportional to the second derivative (in a common case, the even derivatives) of the transfer function.
- The device transfer function will be linear only if the third derivative (in a common case, the odd derivatives) is equal to zero.
- The even harmonic components are the result of the even derivatives of the device transfer function, whereas the odd harmonic components are the result of the odd derivatives of the device transfer function.
- The first-order mixing products (total and differential) are conditional upon the even derivatives of the device transfer function.
- The mixing products of the third and higher orders are mainly determined by the odd derivatives of the device transfer function.
- The distortions, which are determined by the second derivative (second amplitude degree) or by the third derivative (third amplitude degree) of the device transfer function, are called the *second-order intermodulation distortions* or the *third-order intermodulation distortions*, respectively.

From Eq. (6.58) it follows that the output current amplitude of the fundamental, second and third harmonic or intermodulation components depends on the first, second and third degree of the input voltage amplitude, respectively. Consequently, the output power levels of the linear, second-order and third-order frequency components show a straight-line behavior and vary by 1 dB, 2 dB and 3 dB, respectively,

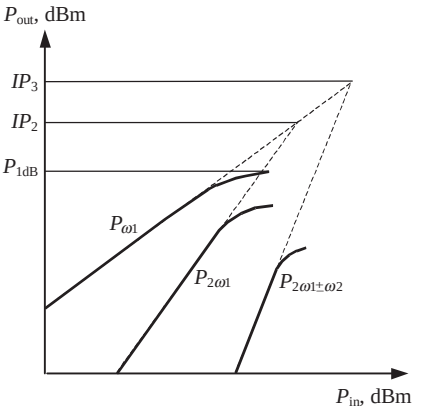

Figure 6.16 Straight-line dependencies for fundamental, second harmonic and third-order intermodulation components with the appropriate intercept points.

with an input power level of 1 dB variation. Further analysis of Eq. (6.58) would show that n-order components also vary by n dB with an input power level of 1 dB variation. As a result, these straight lines in terms of dBm intersect at the intercept points. Each point is different for each order of intermodulation products. Consequently, if the intercept point is determined, for example experimentally for a given type of the transistor, it is easy to evaluate the harmonic and n-order intermodulation output power levels at an arbitrary level of input power. In Fig. 6.16, the straight-line dependencies for fundamental, second harmonic and third-order intermodulation components with the appropriate intercept points are presented.

For any straight line, we can write the following equation:

$$P_{\mathrm{IM_n}} = nP_{\mathrm{in}} + P_{\mathrm{n0}}\,(\mathrm{dBm}) \tag{6.59}$$

where P_{n0} is a constant that will be evaluated. The linear fundamental output power is equal to

$$P_{\omega_1} = 10\log_{10}\left(G_{\mathrm{p}}P_{\mathrm{in}}\right) = P_{\mathrm{in}} + G_{\mathrm{p}}\,(\mathrm{dBm}) \tag{6.60}$$

Equation (6.59) can be rewritten as

$$P_{\mathrm{IM_n}} = nP_{\omega_1} + P_{\mathrm{n0}} - nG_{\mathrm{p}}\,(\mathrm{dBm}) \tag{6.61}$$

At the intercept point IP_{n}

$$P_{\mathrm{IM_n}} = P_{\omega_1} = IP_{\mathrm{n}} \tag{6.62}$$

which yields a ratio

$$(1-n)IP_{\mathrm{n}} = P_{\mathrm{no}} - nG_{\mathrm{p}}\,(\mathrm{dBm}) \tag{6.63}$$

Then,

$$P_{\mathrm{IM_n}} = nP_{\omega_1} - (n-1)IP_{\mathrm{n}}\,(\mathrm{dBm}) \tag{6.64}$$

Equation (6.64) can be used to evaluate the relationship between the fundamental output power P_{ω_1}, the output power corresponding to the n-order components P_{IMn}, and the n-order intercept point IP_{n} at the input level below saturation. For example, the second harmonic component $P_{2\omega_1}$ and the third-order intermodulation component $P_{2\omega_1-\omega_2}$ can be easily evaluated by the following equations:

$$P_{2\omega_1} = 2P_{\omega_1} - IP_2\,(\mathrm{dBm}) \tag{6.65}$$

$$P_{2\omega_1-\omega_2} = 3P_{\omega_1} - 2IP_3\,(\mathrm{dBm}) \tag{6.66}$$

The 1-dB compression level of output power, at which a value of the power gain decreases by 1 dB compared to its small-signal value at the linear region of operation, is determined by

$$P_{1\mathrm{dB}} = IP_3 - 9\,(\mathrm{dBm}) \tag{6.67}$$

Equations (6.66) and (6.67) give a convenient and simple qualitative evaluation of the main nonlinear characteristics of the real power amplifier. For example, if $IP_3 = 50$ dBm, then $P_{1\mathrm{db}} = 41$ dBm with the third-order nonlinear component of $P_{2\omega_1-\omega_2} = 23$ dBm. To improve the linearity of the power amplifier, it is necessary to reduce the output power level for a given value of the intercept point. The level of -30 dB, relatively fundamental for the third-order intermodulation component $P_{2\omega_1-\omega_1}$, can be achieved only in the case of $P_{\omega_1} = 35$ dBm, i.e., need to reduce significantly the output power by 6 dB (or four times).

It is well known that setting the dc drain current of a GaAs MESFET device to approximately $0.5I_{\mathrm{dss}}$ maximizes not only its gain but also its intermodulation intercept points. There are two explanations for this. First, the transfer $I_{\mathrm{ds}}(V_{\mathrm{gs}})$ curve is clearly more linear near its sweet spot of $0.5I_{\mathrm{dss}}$ where its slope, i.e., the device transconductance, is maximal, and thus mainly influenced by the first-degree coefficient of its Taylor series expansion. Second, the nonlinearity of the $C_{\mathrm{gs}}(V_{\mathrm{gs}})$ curve significantly decreases with the bias shift at higher values. To provide the high-efficiency operation mode of the MESFET power amplifier, it is necessary to use a value for the gate-source bias voltage quite close to the pinch-off voltage, with the appropriate worsening of its linear properties. However, in this case it is possible to choose the bias point with drain quiescent current I_{dq} in limits of $0.1 \div 0.15I_{\mathrm{dss}}$, when the carrier to third-order intermodulation ratio, IM_3, can be minimized at a sufficiently high level of the output power, as shown in Fig. 6.17. This effect can be explained by the following circumstances. First, the dependence

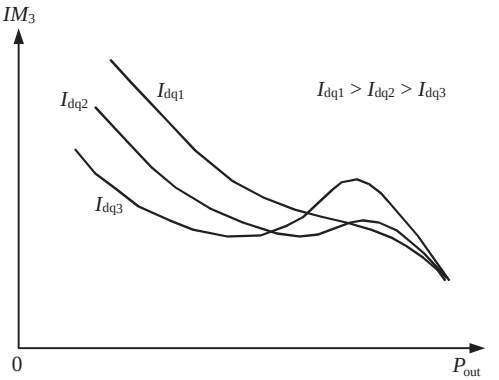

Figure 6.17 MESFET power amplifier intermodulation distortions versus output power of different quiescent currents.

of the drain current I_{ds} on the gate voltage V_{gs} has a quadratic law near the pinch-off point. Second, given a certain value of gate-source bias voltage, the third-order components and the components that are the results of an interaction of the second harmonic, $2\omega_1$ and $2\omega_2$, and differential, $\omega_2 - \omega_1$, components with fundamental components, ω_1 and ω_2, cancel each other. Since this cancellation depends on the load and source impedances at the frequencies far from the operating frequency bandwidth, it is necessary to provide an additional tuning of the input and output matching circuits in order to minimize intermodulation distortion.

Figure 6.18 shows an output power spectrum containing only n-order intermodulation components, which are the result of the effect of two-tone input excitation. The amplitude of the higher-order intermodulation components decreases significantly when frequency increases.

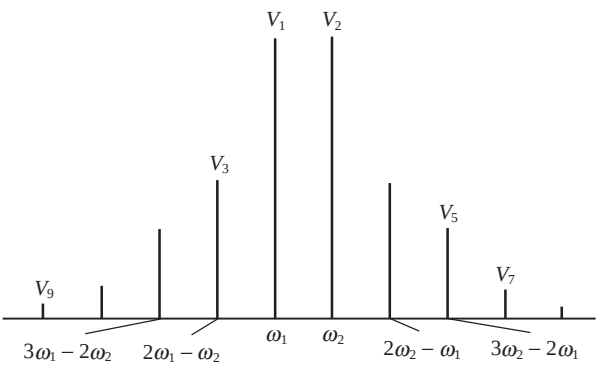

Figure 6.18 Typical output power spectrum for two-tone excitation.

To evaluate the linear properties of the transistor, it is sufficient to measure the amplitudes of the largest intermodulation components, i.e., the third-order and the fifth-order components. The carrier to third-order intermodulation ratio or the third-order intermodulation coefficient IM_3 and the fifth-order intermodulation coefficient IM_5 are defined as follows:

$$IM_3 = 10\log_{10}(P_{2\omega_1-\omega_2}/P) = P_{2\omega_1-\omega_2} - P \text{ (dBc)} \tag{6.68}$$

$$IM_5 = 10\log_{10}(P_{3\omega_1-2\omega_2}/P) = P_{3\omega_1-2\omega_2} - P \text{ (dBc)} \tag{6.69}$$

where $P = P_{\omega_1} = P_{\omega_2}$ for equal two-tone signal amplitudes. On the other hand, the third-order intermodulation coefficient IM_3 can be directly represented from Eq. (6.66) as

$$IM_3 = P_{2\omega_1-\omega_2} - P_{\omega_1} = 2P_{\omega_1} - 2IP_3 \text{ (dBc)} \tag{6.70}$$

and, for example, for the power amplifier with $IP_3 = 50$ dBm and $P_{1\text{db}} = 41$ dBm, the third-order intermodulation coefficient IM_3 is equal to -18 dBc.

The linearity properties of the MOSFET power amplifiers are also strongly sensitive to quiescent biasing conditions when a choice of the optimum bias value in Class AB operation allows improving the third-order intermodulation distortion by more than 10 dB [5]. This is a result of the quadratic character of a sufficiently long section of the device transfer dependence $I_{\text{ds}}(V_{\text{gs}})$. Minimum power gain flatness over the dynamic power range, P_{out} versus P_{in}, corresponds to the best linearity condition.

For bipolar transistors, a similar approach can be used, when an improved intermodulation distortion is achieved by varying the collector quiescent current. In this case, for Class AB operation, the minimum level of the third-order intermodulation components is a function of the values of both the output power P_{out} and the collector quiescent current I_{cq}. Low values of I_{cq} give better linearity at higher power levels, whereas higher values of I_{cq} give better linearity at lower power levels. Since the sweet point moves when different I_{cq} are used, minimum gain flatness over the total dynamic range corresponds to the best linearity that can be achieved by adding a series resistor R with optimum value in the base bias circuit [6]. The series resistor is connected after the base bypass circuit, which usually consists of a quarterwave microstrip line and bypass capacitor (see Fig. 6.19).

The use of a series resistor allows the gain flatness to be minimized and the level of third-order intermodulation components to be stabilized over the dynamic range. An increase in RF output power causes the appropriate increase in the dc collector current. This leads to an

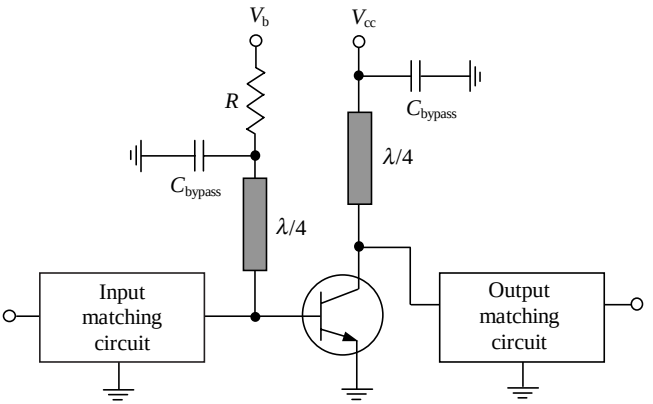

Figure 6.19 Bipolar power amplifier schematic with linearizing bias resistor.

increase in the dc base current with an increase in the voltage drop across the resistor R and a decrease in the base bias voltage. To determine the value of R, it is advisable to set a goal for the level of the intermodulation components at both high and low output power levels. Then, the value of R can be calculated in accordance with

$$R = \frac{V_{b1} - V_{b2}}{I_{b2} - I_{b1}} \tag{6.71}$$

where V_{b1} is the dc voltage at low power level, V_{b2} is the dc voltage at high power level, I_{b1} is the dc base current at low power level, and I_{b2} is the dc base current at high power level.

In practice, the level of n-order intermodulation component is frequently given relative to the peak envelope power P_{PEP} calculated from two-tone excitation signal measurements. The waveform of the signal dissipated in the load will be significantly different from sinusoidal and can be written for two-tone signal of equal amplitudes $V_1 = V_2 = V$ as

$$v_L = V_1 \sin\omega_1 t + V_2 \sin\omega_2 t = 2V \cos\Omega t \sin\omega t \tag{6.72}$$

where $\omega = (\omega_1 + \omega_2)/2$ is the center RF signal frequency and $\Omega = (\omega_1 - \omega_2)/2$ is the low intercarrier frequency.

A waveform of such a two-tone excitation signal with equal amplitudes is shown in Fig. 6.20, where $T = 2\pi/\Omega$. The peak envelope power P_{PEP} that corresponds to the output power with maximum amplitude $2V$ is equal to

$$P_{PEP} = (2V)^2/2R_L \tag{6.73}$$

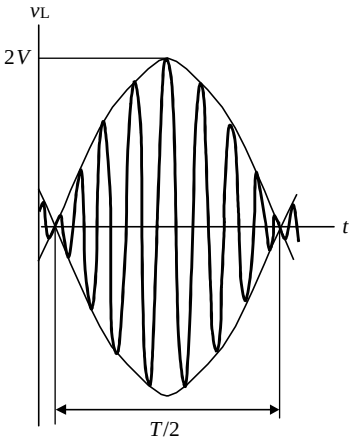

Figure 6.20 Two-tone excitation signal.

where R_L is the load resistance. The total output power provided by each sinusoidal tone of two-tone excitation signal with equal amplitudes is

$$P_{out} = P_{\omega 1} + P_{\omega 2} = V^2/R_L \tag{6.74}$$

Comparing Eqs. (6.73) and (6.74) yields

$$P_{PEP} = 2P_{out} = 4P \tag{6.75}$$

where $P = P_{\omega 1} = P_{\omega 2}$.

Basic Classes of Operation: A, AB, B and C

To determine the operation classes of the power amplifier, consider a simple resistive stage shown in Fig. 6.21, where *RFC* is the ideal RF choke with zero series resistance and infinite reactance at the operating frequency, and C_b is the dc-blocking capacitance with infinite value having zero reactance at the operating frequency. The active device behaves as an ideal voltage-controlled current source having zero saturation resistance. The input cosinusoidal voltage is defined as

$$v_{in} = V_b + V_{in} \cos \omega t \tag{6.76}$$

where V_b is the base bias voltage.

For $V_b - V_p \geq V_{in}$ and piecewise-linear approximation of the active device transfer function, the output current is cosinusoidal too:

$$i = I_q + I \cos \omega t \tag{6.77}$$

with the quiescent current I_q greater or equal to the amplitude I of the collector cosinusoidal signal. In this case, the output collector current

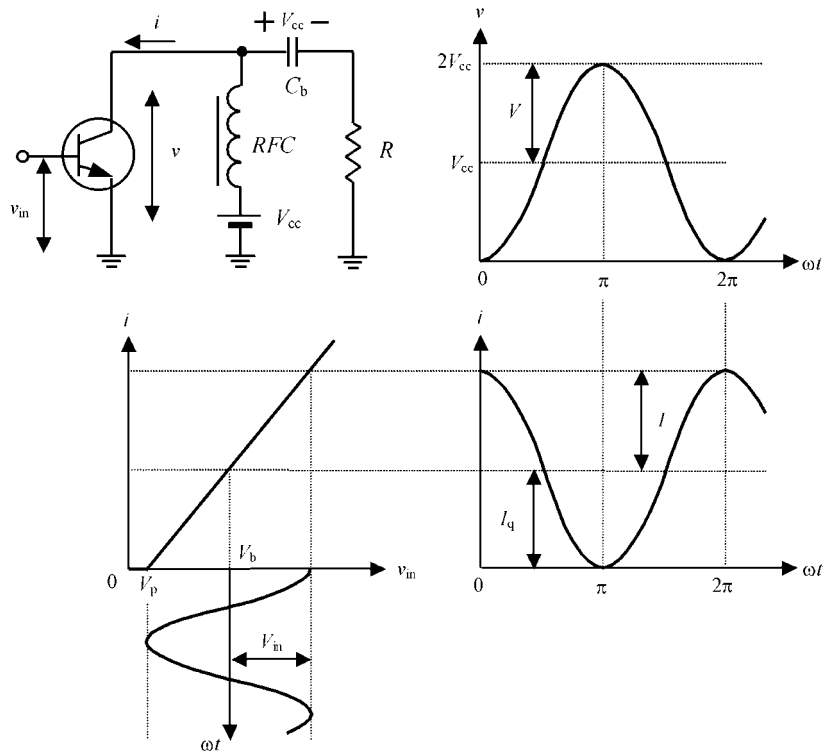

Figure 6.21 Voltage and current waveforms in Class A operation.

contains only two components—constant and cosinusoidal—and the averaged current magnitude is equal to the quiescent current I_q. For pure active load when $Z_L = R$, the collector voltage can be written by

$$v = V_{cc} - (i - I_q)R \tag{6.78}$$

Equation (6.78) can be rewritten in the form of

$$i = \left(I_q + \frac{V_{cc}}{R}\right) - \frac{v}{R} \tag{6.79}$$

which determines the changes of the collector current versus the collector voltage and represents a straight line function. Substituting Eq. (6.77) into Eq. (6.78) results in the cosinusoidal collector voltage with the opposite phase conditions:

$$v = V_{cc} - V\cos\omega t \tag{6.80}$$

which corresponds to its minimum value when the output current is maximum. Such a combination of the cosinusoidal collector voltage and current waveforms is known as a *Class A* operation mode. In real practice, because of the device nonlinearities, it is necessary to connect a parallel *LC*-circuit with resonant frequency equal to the operating frequency to suppress any possible harmonic components.

Circuit theory prescribes that the dc output power P_0, alternating current output power P, and collector efficiency η can be written, respectively, as

$$P_0 = I_q V_{cc} \tag{6.81}$$

$$P = 0.5IV \tag{6.82}$$

$$\eta = \frac{P}{P_0} = \frac{1}{2}\frac{I}{I_q}\frac{V}{V_{cc}} = \frac{1}{2}\frac{I}{I_q}\xi \tag{6.83}$$

where $\xi = V/V_{cc}$ is the collector voltage peak factor.

Then, assuming the ideal conditions of zero saturation voltage when $\xi = 1$ and maximum output current amplitude when $I/I_q = 1$, from Eq. (6.83) it follows that maximum collector efficiency in Class A operation mode is equal to only

$$\eta = 0.5 \tag{6.84}$$

However, increasing the value of I/I_q can increase the collector efficiency. This leads to a step-by-step transformation of the current cosinusoidal waveform to its pulsed waveform when the magnitude of the collector current exceeds zero value during only a part of the entire signal natural period. In this case, an active device operates in the active region followed by the operation in the pinch-off region, respectively, as shown in Fig. 6.22. Because the parallel resonant *LC*-circuit has a high quality factor, only fundamental frequency signal is flowing into the load, whereas, for higher-order harmonic components, the short-circuited conditions are performed.

Analytically such an operation can be written as

$$i = \begin{cases} I_q + I\cos\omega t, & -\theta \le \omega t < \theta \\ 0, & \theta \le \omega t < 2\pi - \theta \end{cases} \tag{6.85}$$

where the conduction angle 2θ indicates the part of the RF current cycle for which device conduction occurs and determines the moment when output current i takes a zero value. At this moment

$$i = 0 = I_q + I\cos\theta \tag{6.86}$$

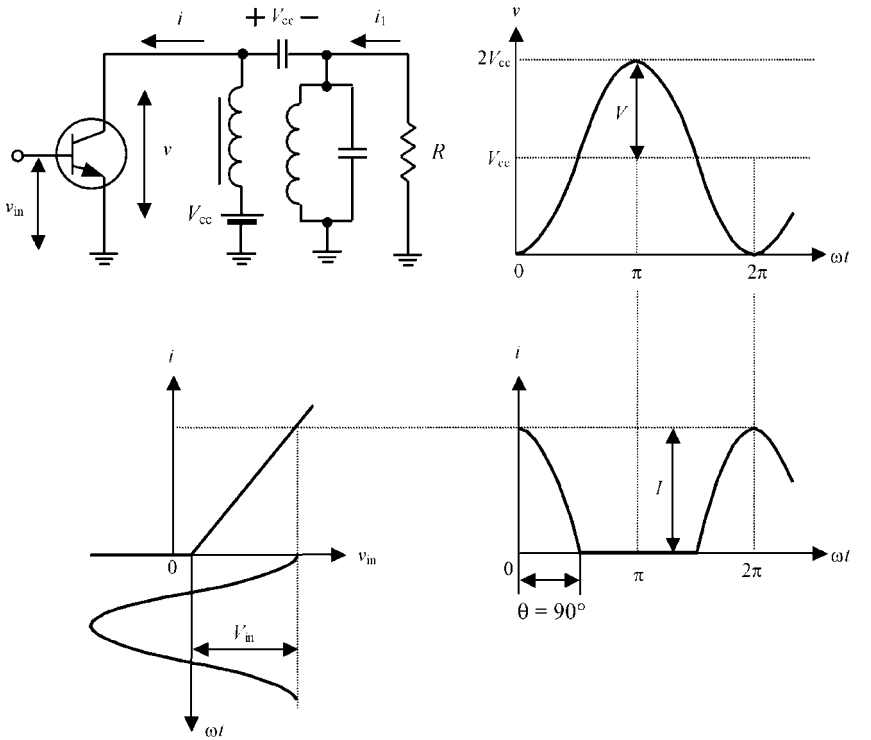

Figure 6.22 Voltage and current waveforms for the device operating in active and pinch-off regions.

and θ can be calculated from

$$\cos\theta = -\frac{I_q}{I} \tag{6.87}$$

Consequently, in a common case,

$$i = I(\cos\omega t - \cos\theta) \tag{6.88}$$

When $\omega t = 0$, the output collector current has maximum amplitude of

$$i = I_{max} = I(1 - \cos\theta) \tag{6.89}$$

From Eq. (6.87), the basic definitions are derived:

- When $\theta > 90°$, then $\cos\theta < 0, I_q > 0$ corresponding to Class AB operation.
- When $\theta = 90°$, then $\cos\theta = 0$, $I_q = 0$ corresponding to Class B operation.

- When $\theta < 90^\circ$, then $\cos\theta > 0$, $I_q < 0$ corresponding to Class C operation.

As a result, the periodic half-cosinusoidal output current i can be represented as a Fourier-series expansion

$$i = I_0 + I_1\cos\omega t + I_2\cos 2\omega t + I_3\cos 3\omega t + \ldots \tag{6.90}$$

where the dc and fundamental components can be obtained from

$$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta)d(\omega t) = I\gamma_0 \tag{6.91}$$

$$I_1 = \frac{1}{\pi}\int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta)\cos\omega t d(\omega t) = I\gamma_1 \tag{6.92}$$

where $\gamma_0 = \frac{1}{\pi}(\sin\theta - \theta\cos\theta)$, $\gamma_1 = \frac{1}{\pi}(\theta - \sin\theta\cos\theta)$.

From Eq. (6.91) it follows that, in contrast to Class A operation mode where $\theta = 180^\circ$ and the dc current is equal to quiescent current during all natural period, the dc current component is a function of θ in operation modes with $\theta < 180^\circ$.

The collector efficiency of a power amplifier with a resonant circuit can be obtained from

$$\eta = \frac{P_1}{P_0} = \frac{1}{2}\frac{I_1}{I_0}\xi = \frac{1}{2}\frac{\gamma_1}{\gamma_0}\xi \tag{6.93}$$

If $\xi = 1$ and $\theta = 90^\circ$, then from Eqs. (6.91) and (6.92) it follows that the maximum collector efficiency in Class B operation mode is equal to

$$\eta = \frac{\pi}{4} \cong 0.785 \tag{6.94}$$

Since the parallel LC-circuit is tuned to the fundamental frequency, the voltage across the load R can be considered as cosinusoidal. Then, using Eqs. (6.80), (6.85) and (6.87), the relationship between the collector current i and voltage v during a time period of $-\theta \le \omega t < \theta$ can be expressed by

$$i = \left(I_q + \frac{V_{cc}}{\gamma_1 R}\right) - \frac{v}{\gamma_1 R} \tag{6.95}$$

where the fundamental current coefficient γ_1 as a function of θ is determined by Eq. (6.92). The load resistance is equal to $R = V/I_1$ where I_1 is the fundamental current amplitude. Equation (6.95), which determines the dependence of the collector current on the collector voltage for any values of conduction angle and represents a straight line function, is

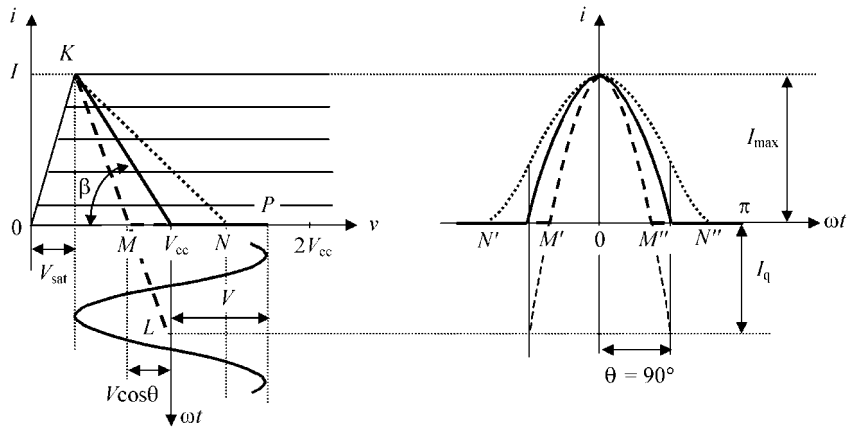

Figure 6.23 Collector voltage and current waveforms for the device operating in active and pinch-off regions.

the dynamic characteristic of the power amplifier and is called the *load line*. For Class A operation with $\theta = 180^\circ$ when $\gamma_1 = 1$, Eq. (6.95) is identical to Eq. (6.79).

Figure 6.23 shows the idealized active device static *I-V* curves and load lines for different conduction angles according to Eq. (6.95) with corresponding collector and current waveforms. From Fig. 6.23, it follows that the maximum collector current amplitude I_{max} corresponds to the minimum collector voltage V_{sat} when $\omega t = 0$, and is the same for any conduction angle. The slope of the load line is different for the different conduction angles and values of the load resistance, and it can be obtained by

$$\tan\beta = \frac{I}{V(1-\cos\theta)} = \frac{1}{\gamma_1 R} \tag{6.96}$$

from which it follows that, for the same conduction angle 2θ, the greater the slope angle β of the load line, the smaller the value of the load resistance R.

The load line moves from point K, which determines the active device saturation voltage V_{sat}, through the point of intersection with a horizontal axis v where $i = 0$ and $\omega t = \theta$. For Class AB operation (dotted line), the intersection occurs in a point N resulting in the conduction angle between points N' and N'' of $2\theta > 180^\circ$ for the collector current pulse. For Class C operation (dashed line), this is a point M with conduction angle between points M' and M'' of $2\theta < 180^\circ$ for the collector current pulse. Then, for Class C mode, the load line keeps moving down

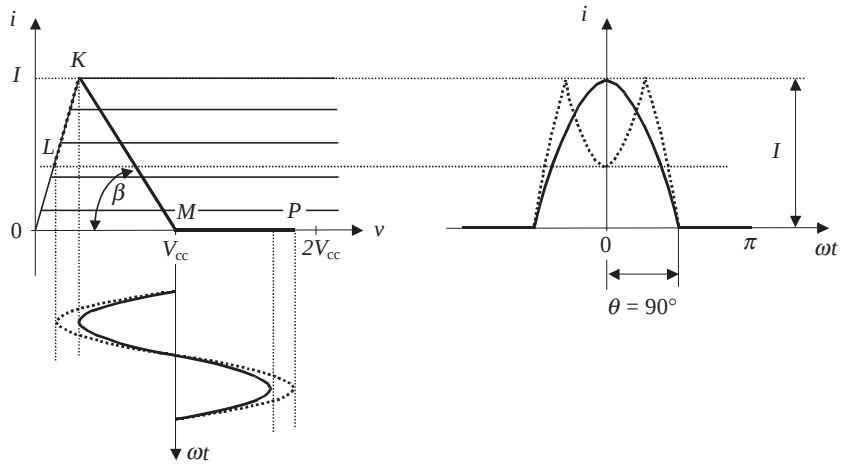

Figure 6.24 Collector voltage and current waveforms for the device operating in saturation, active and pinch-off regions.

to a point L where $\theta = 90^\circ$ and $I_q < 0$. As a result, generally the load line represents a broken line with the first section moving according to the slope angle β and another horizontal section with zero current i moving as far as the point P where $\theta = 180^\circ$. Consequently, in Class B mode, the collector current represents half-cosinusoidal pulses (solid line) with the conduction angle of $2\theta = 180^\circ$ and $I_q = 0$.

Now let us consider a Class B operation with an increased amplitude of the cosinusoidal collector voltage. In this case, as follows from Fig. 6.24, an active device operates in saturation, active and pinch-off regions and the load line represents a broken line *LKMP* with three linear sections (*LK*, *KM*, and *MP*). The new section *KL* corresponds to the saturation region resulting in the half-cosinusoidal collector current waveform with a depression in the top part. With further increase of the collector voltage amplitude, the collector current pulse can be even-split into two symmetrical pulses containing a significant level of the higher-order harmonic components. The same result can be achieved by increasing a value of the load resistance R that results in the smaller slope angle β of the load line.

The collector current waveform becomes asymmetrical for the complex load in which impedance is represented by the load resistance and capacitive or inductive reactances. For example, for the inductive load impedance, the depression in the collector current waveform reduces and moves to the left side of the waveform, whereas the capacitive load impedance causes the depression to deepen and shift to the right side of

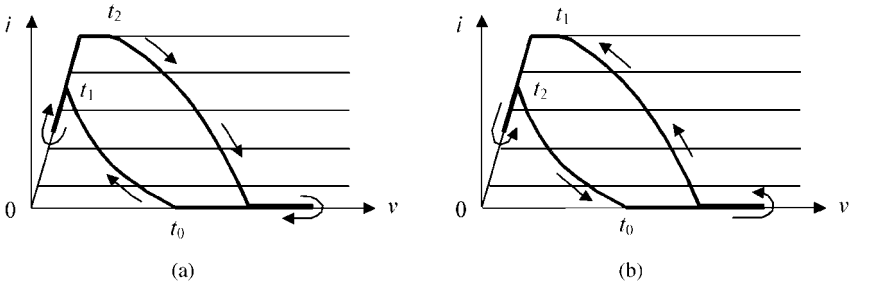

Figure 6.25 Load lines for (*a*) inductive and (*b*) capacitive load impedances.

the collector current waveform [7]. This effect can be explained by the different phase conditions for the higher-order harmonic components that compose the collector current waveform, and is illustrated by the different load lines for (*a*) inductive and (*b*) capacitive load impedances shown in Fig. 6.25.

Generally, the dependence of the device collector capacitance on collector voltage in the large-signal operation can lead to parametric effects. To evaluate the influence of the nonlinear collector capacitance on the electrical behavior of the power amplifier, consider the power amplifier circuit with series resonant L_0C_0-circuit tuned to the fundamental frequency that provides open circuit conditions for higher-order collector current harmonic components and L-type matching circuit with series inductance L and shunt capacitance C as shown in Fig. 6.26(*a*). The matching circuit is necessary to match the output active device resistance R, corresponding to the required output power level, with the load resistance $R_{\rm L}$. The simplified equivalent circuit of the power amplifier is shown in Fig. 6.26(*b*).

The total collector current can be written as

$$i = I_0 + \sum_{n=1}^{\infty} I_{\rm n} \cos(n\omega t + \phi_{\rm n}) \tag{6.97}$$

Because of the series resonant circuit only the fundamental collector current component dissipates in the load:

$$i_{\rm L} = I_{\rm L} \cos(\omega t + \phi_{\rm L}) \tag{6.98}$$

The current flowing through the nonlinear collector capacitance consists of fundamental and higher harmonic components:

$$i_{\rm C} = I_{\rm C1} \cos(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_{\rm n} \cos(n\omega t + \phi_{\rm n}) \tag{6.99}$$

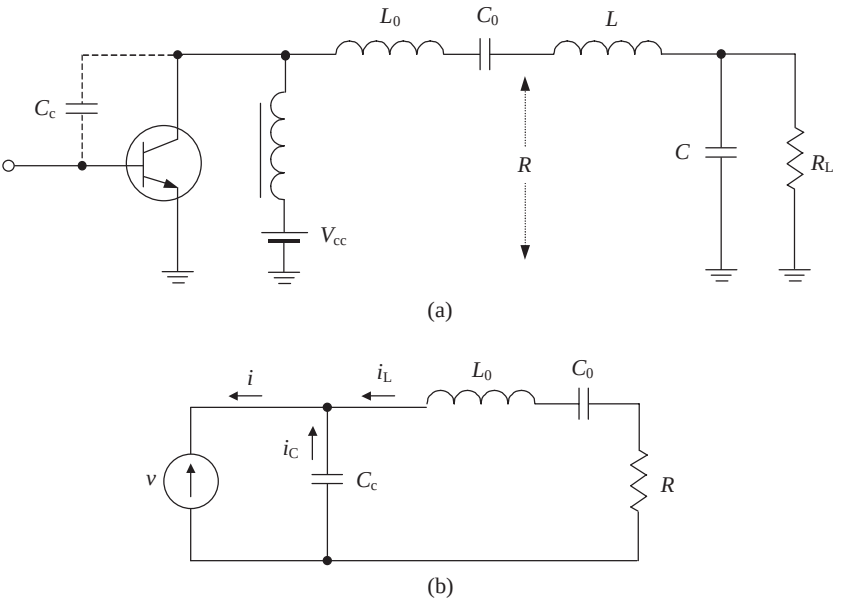

Figure 6.26 Resonant power amplifier circuit schematics.

The collector voltage-capacitance dependence is written as

$$C_c = C_{co}\left(\frac{\varphi + V_{cc}}{\varphi + v}\right)^{\gamma} \tag{6.100}$$

where C_{co} is the small-signal collector capacitance at $v = V_{cc}$, V_{cc} is the supply voltage, φ is the contact potential and γ is the junction sensitivity.

From the result of charge consideration and the first three terms of the Taylor's series expansion it follows that—because of the parametric transformation due to the nonlinearity of the collector capacitance—the fundamental collector voltage amplitude V_1 increases by σ_p times according to

$$\sigma_p = 1 + \frac{1}{4}\frac{I_2\gamma}{\omega C_{co}V_{cc}}\cos(90^\circ + \phi_2 - 2\phi_1) + \frac{1}{12}\frac{I_2 I_3\gamma}{(\omega C_{co})^2 V_1 V_{cc}}\cos(90^\circ + \phi_3 - \phi_2 - \phi_1) \tag{6.101}$$

where $\sigma_p = \xi_p/\xi$, ξ_p is collector voltage peak factor with parametric effect [7].

To maximize the collector voltage and, consequently, the collector efficiency for given value of the supply voltage V_{cc}, from Eq. (6.101)

the following phase conditions are realized: $\phi_2 = 2\phi_1 - 90^\circ$ and $\phi_3 = 3\phi_1 - 180^\circ$. Then, for $\gamma = 0.5$,

$$\sigma_p = 1 + \frac{1}{8}\frac{I_2}{\omega C_{co} V_{cc}} + \frac{1}{24}\frac{I_2 I_3}{(\omega C_{co})^2 V_1 V_{cc}} \tag{6.102}$$

Equation (6.102) shows the theoretical possibility of realizing an increase in collector peak factor of $\sigma_p = 1.1$–1.2 times, which achieves a collector efficiency of 85 to 90 percent. Physically, the improved efficiency can be explained by the transformation of the higher harmonic component power into the fundamental one because of the nonlinearity of the collector capacitance.

DC Biasing

The simplest way to provide a biasing condition for a power MOSFET device in Class A or Class AB operation is to use the potentiometer-type voltage divider for gate bias and inductance or an RF choke in the drain circuit, as shown in Fig. 6.27(a). In this case, any influence of the ambient temperature in a wide range or bias voltage variations leads to the variations of quiescent current and, as a result, to appropriate variations of the output power, linearity, efficiency and gain of the power amplifier. The threshold voltage of the MOSFET transistor V_{th} varies versus temperature T linearly with the approximate velocity of $\Delta V_{th}/\Delta T \cong 2$ mV/°C. The simple addition of a diode in series to the variable resistor allows the quiescent current variation to be reduced substantially over temperature. A bias circuit corresponding to this stabilizing condition is presented in Fig. 6.27(b). For a high value of V_{th}, several diodes are connected in series. Such a simple bias circuit configuration for power MOSFET transistors is possible when an extremely small value of the dc gate current, which is restricted to a value of the gate-source leakage current, is present.

In contrast to MOSFET devices—where it can be possible to choose the optimum operating point with practically zero temperature coefficient or to be limited to connection of an additional diode only—the bipolar transistors require the more complicated approach of dc biasing depending on the class of operation. So, in Class A operation, to obtain maximum linear power gain with minimum changes in a wide temperature range, a bias circuit can be designed as shown in Fig. 6.28 [8]. Here, due to the large negative feedback by means of the resistor R_3, the operating point of the RF power bipolar transistor is extremely stabilized for wide variations in ambient temperature. For instance, if the dc collector current of the RF power transistor rises, due to an increase in ambient temperature, the collector voltage of this transistor will fall in accordance with the voltage drop across the feedback

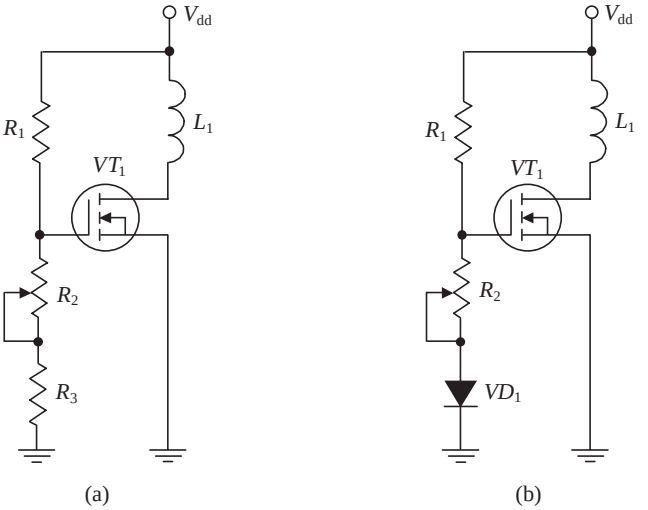

Figure 6.27 Typical MOSFET bias circuits.

resistor R_3 causing an appropriate decrease in the transistor collector current. The diode is used to compensate the temperature coefficient of the base-emitter junction voltage of the *p-n-p* power transistor. The variable resistor R_1 in series with this diode serves to adjust the dc collector current of the RF transistor in its operating point at the desired value. The resistor R_5 is necessary to reduce the variation in collector current of the *p-n-p* transistor, whereas the resistor R_4 is included to protect the RF power transistor and to reduce the dissipation in the *p-n-p* transistor. The parameters of this bias circuit are given for a

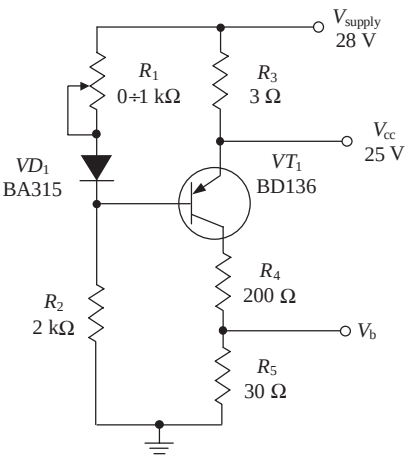

Figure 6.28 Typical bipolar bias circuit for Class A operation.

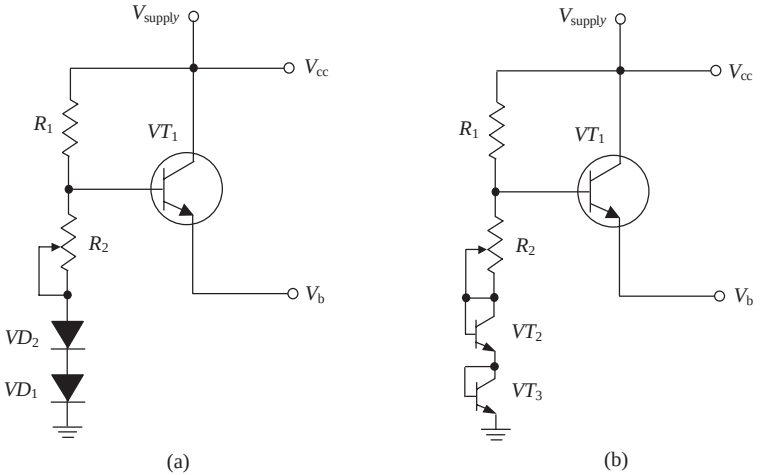

Figure 6.29 Simple bipolar bias circuits for Class AB operation.

collector current of RF power transistor of 0.9 A with collector voltage of 25 V for supply voltage of 28 V.

In a Class AB operation, the bias circuit has to deliver a constant voltage, slightly adjustable approximately within limits of 0.7 to 0.8 V, with a wide range of current values. Besides, it is necessary to provide an operation mode for the power amplifier with temperature compensation and minimum possible current consumption. One of the simplest versions of such a bias circuit with silicon diode temperature compensation is presented in Fig. 6.29(*a*). Using the emitter follower on the *n-p-n* power transistor VT_1, it is possible to increase the base current of the RF power transistor for high-power operation. In this bias circuit, the silicon diode can be replaced by the *n-p-n* diode-connected transistor, the collector and base of which are directly connected between each other, as shown in Fig. 6.29(*b*). A better temperature compensating result can be achieved using the same devices as for the RF power transistor for each bias circuit transistor, but with reduced area size. Such an approach is usually used in monolithic integrated circuit design when transistor cells with different area sizes are used for both RF power device and bias circuit transistors.

Figure 6.30 shows a more complicated bias circuit that is commonly used for biasing the high power RF transistors to provide their temperature-stable and reliable operation mode [8]. The temperature stabilization is provided by the parallel connection of the base-emitter diode junction of the transistor VT_1, whereas high value of the bias drive current for the RF power transistor is delivered by the transistor VT_2. If the dc collector current of an RF power transistor is 5 A and a value of

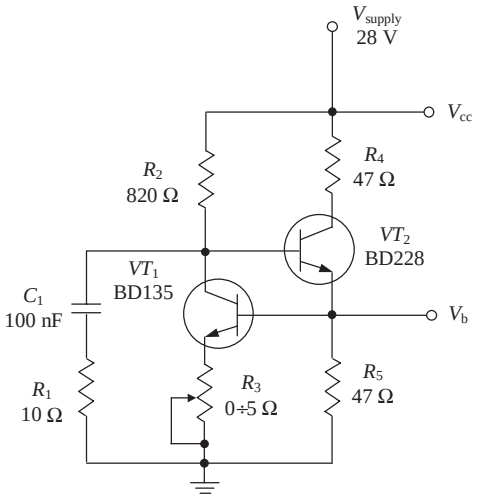

Figure 6.30 Typical bipolar bias circuit for Class AB operation [8].

β_F is approximately equal to 10, then the maximum base current of the RF power transistor can be 0.5 A. In this bias circuit the resistor R_5 is used to reduce the base current variations. At $V_b = 0.7$ V, for a current of 15 mA the value of R_5 should be equal to 0.7 V/15 mA = 47 Ω. Suppose that a value of the collector current of VT_1 is 30 mA. Then, if the base-emitter junction voltage of VT_2 is equal to 0.8 V with a voltage across the resistor R_2 of 28 – 1.5 = 26.5 V, its value is 26.5 V/30 mA ≅ 820 Ω. The variable resistor R_3 serves to adjust the output voltage in limits of 0.1 V. To limit the maximum collector current of VT_2 by a value of 0.5 A, it is advisable to use the resistor R_4. Since VT_2 has a value for the saturation voltage of 0.8 V, it follows that the maximum value of R_4 is 26.5 V/0.5 A = 53 Ω. It is sufficient to use its value of 47 Ω with a power dissipation of $(0.5\text{ A})^2 \times 47\ \Omega = 11.75$ W. Such a bias circuit can develop the parasitic oscillations near 1 MHz with highly capacitive loads. Therefore, to prevent these oscillations, it is necessary to connect the *RC*-circuit between the collector of VT_1 and ground.

In most wireless telecommunication systems it is preferable that the power amplifier operates with high efficiency, maintaining an acceptable linearity over the desired supply voltage range. However, there is a tradeoff between efficiency and linearity with improvement in one coming at the expense of the other. This means that it is necessary to provide an optimum stable bias point over wide temperature range and process variations. As a current-controlled device, the bipolar transistor in RF operation requires a dc base driving current, the value of which depends on the output power and device parameters. Because technologically the bipolar device represents a parallel connection

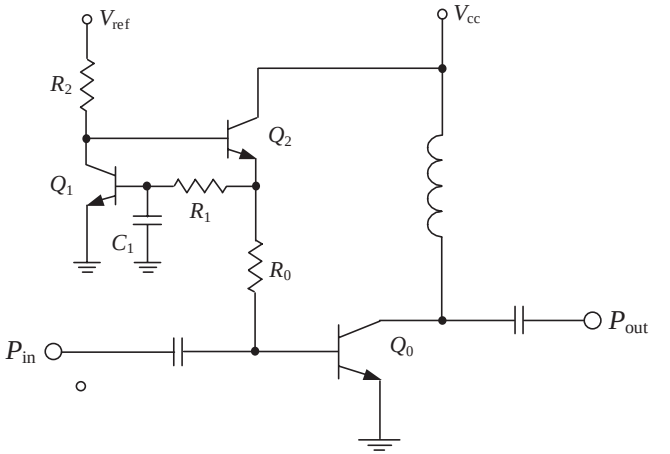

Figure 6.31 Typical bipolar bias circuit for wireless handset linear power amplifier.

of the basic cells, it is important to use the ballasting series resistors to avoid current imbalance and possible device collapse at higher current-density levels. Another important aspect is to keep the dc base-emitter bias point constant over any RF input power variations to prevent the linearity worsening at the maximum output power for power amplifiers with a variable envelope signal (such as WCDMA or CDMA2000).

The typical temperature-compensation current mirror bias circuit with one reference transistor Q_1 and one driving transistor Q_2 is shown in Fig. 6.31. This circuit keeps the quiescent current for the RF device Q_0 more or less constant over temperature variations, and the current flowing through resistor R_2 is sufficiently small. It is very important to provide the proper ratio between the ballasting resistors R_1 and R_0, equal to the ratio of the device areas Q_0/Q_1. This can minimize the overall performance variation with temperature as well as stabilize the dc bias point. The latter case is very important for the variable envelope signals, as the dc bias voltage V_{be0} establishes the conduction angle and operation class for the RF device. If the dc base-emitter bias voltage reduces with the increase of RF input power, the Class AB mode required for linear operation changes to nonlinear Class C operation.

Figure 6.32 shows the dependence of the dc base-emitter bias voltage V_{be0} versus RF input power P_{in} for the second stage of a WCDMA InGaP/GaAs HBT power amplifier for three cases, with ballasting resistor $R_1 = 0$ (curve 1) and optimum ballast resistor R_1 (curve 2). From Fig. 6.32, it follows that including the ballast resistor with an optimum value results in a more constant base-emitter dc bias voltage over a

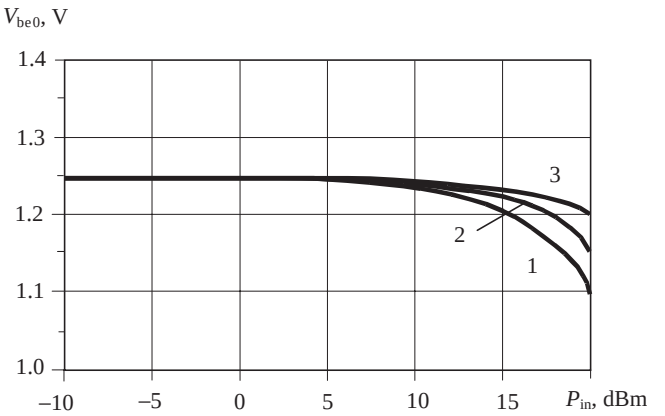

Figure 6.32 DC bias voltage over input power.

wider range of input powers, improving the linearity performance of the power amplifier at high power levels. In addition, it is best to use a shunt capacitance C_1 connected to the base of the device Q_1 to form a low-pass RC filter, which provides better isolation of the bias circuit from the RF signal, with a more constant base-emitter dc bias voltage (curve 3).

Figure 6.33 shows the emitter follower bias circuit that provides temperature compensation and minimizing reference current requirements [9]. The emitter follower bias circuit requires only several tens of

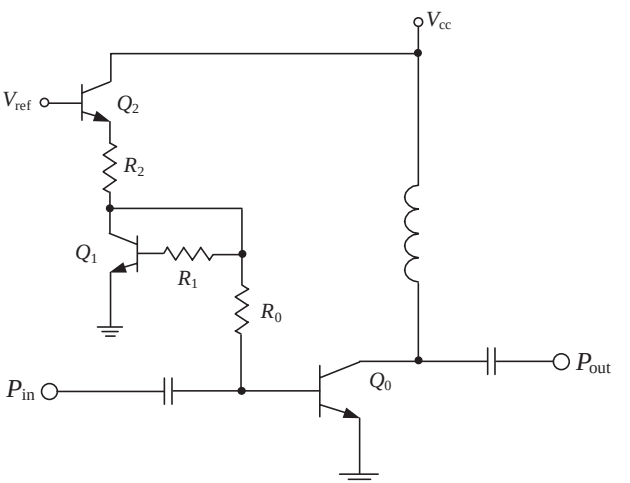

Figure 6.33 Bipolar power amplifier stage with emitter follower bias circuit.

microamperes of reference current, whereas the current mirror bias circuit (see Fig. 6.31) requires a few milliamperes of reference current. Both the current mirror and emitter follower bias circuits have the same current-voltage behavior but, for the same circuit parameters (R_0, R_1 and R_2) and device areas for Q_0, Q_1 and Q_2, the emitter follower circuit is the less sensitive to the reference voltage variations. Variations of the collector supply voltage V_{cc} in limits of 3.0 V to 5.0 V have no effect on the quiescent current set by the reference voltage V_{ref}.

Push-Pull Amplifiers

Common-source or common-emitter push-pull operation using balanced MOSFET or bipolar devices, respectively, helps to increase the values of the input and output impedances. For the same output level, input impedance Z_{in} and output impedance Z_{out} under a push-pull operation mode is approximately four times as high as a parallel connection of these parts. But, at the same time, the quality factor of the input or output circuits remains unchanged because both the real parts and reactive parts of Z_{in} or Z_{out} are increased by the factor of four. The basic concept of push-pull operation can be analyzed by using the equivalent circuit presented in Fig. 6.34 [10].

It is most convenient to consider an ideal Class B operation, which means that each transistor conducts exactly half a 180° cycle with zero quiescent current. Suppose further that a number of turns of both primary and secondary windings of the output transformer are equal, i.e., $n_1 = n_2$. Assume also that the collector current of each transistor can be presented in the following half-sinusoidal form:

For the first transistor

$$i_{c1} = \begin{cases} +I_c \sin\theta, & 0 \le \theta < \pi \\ 0, & \pi \le \theta < 2\pi \end{cases} \tag{6.103}$$

For the second transistor

$$i_{c2} = \begin{cases} 0, & 0 \le \theta < \pi \\ -I_c \sin\theta, & \pi \le \theta < 2\pi \end{cases} \tag{6.104}$$

Being transformed through the output transformer T_2 with the appropriate phase conditions, the total current flowing across the load R_L is defined as

$$i_L(\theta) = i_{c1}(\theta) - i_{c2}(\theta) = I_c \sin(\theta) \tag{6.105}$$

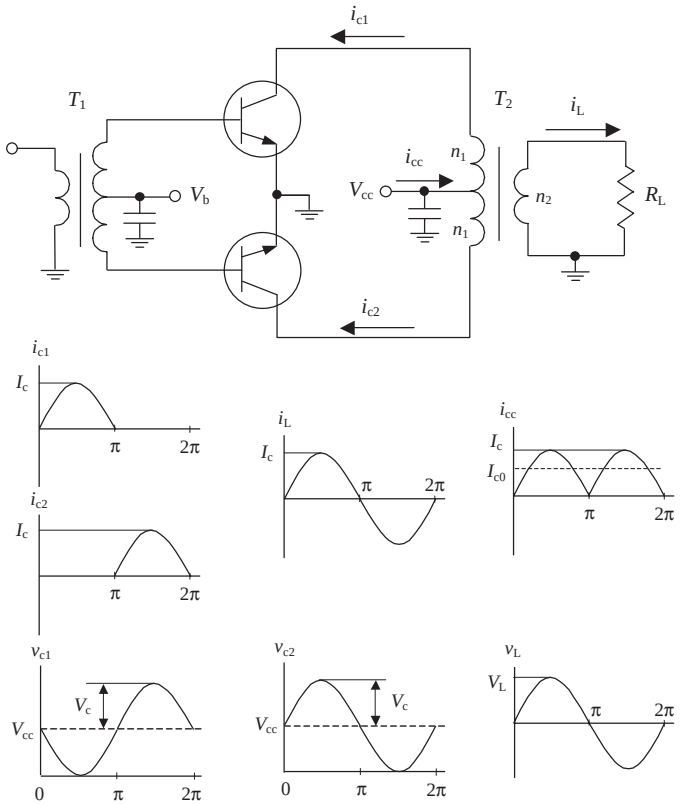

Figure 6.34 Basic concept of push-pull operation.

The current flowing in the center tap of the primary windings of this transformer is the sum of the collector currents:

$$i_{cc}(\theta) = i_{c1}(\theta) + i_{c2}(\theta) = I_c|\sin(\theta)| \tag{6.106}$$

Ideally, even-order harmonics are canceled out and should not appear at the load. In practice a level of the second harmonic of 30 to 40 dB below the fundamental is allowable. It is necessary to connect a bypass capacitor to the center tap of the primary winding in order to exclude power losses due to even-order harmonics. The current $i_L(\theta)$ produces the following output voltage onto the load R_L:

$$v_L(\theta) = I_c R_L \sin(\theta) = V_L \sin(\theta) \tag{6.107}$$

The total dc collector current can be defined as the average value of $i_{cc}(\theta)$:

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i_{cc}(\theta)d\theta = \frac{2}{\pi}I_c \tag{6.108}$$

The total dc power P_0 and RF fundamental output power P_{out}, for the ideal case of zero saturation voltage for both transistors when $V_c = V_{cc}$ and taking into account that $V_L = V_c$ for equal turns of windings when $n_1 = n_2$, are:

$$P_0 = \frac{2}{\pi}I_c V_{cc} \qquad P_{out} = \frac{1}{2}I_c V_{cc} \tag{6.109}$$

The maximum theoretical collector efficiency that can be achieved in push-pull Class B operation is equal to

$$\eta = \frac{P_{out}}{P_0} = \frac{\pi}{4} \cong 78.5\% \tag{6.110}$$

In a balanced circuit, identical sides carry 180° out-of-phase signals of equal magnitude. If perfect balance is maintained on both sides of the circuit, there is a midpoint where the signal magnitude is zero. For absolutely identical circuits in each balanced side, the difference between signal magnitudes becomes equal to zero in each midpoint, as shown in Fig. 6.35. This is called a *virtual grounding*, and this point is referred to as *virtual ground*. The virtual ground, being actually inside the device package, reduces common-mode inductance and results in better stability and usually higher gain.

For a balanced transistor, new possibilities for both internal and external impedance matching emerge. It is necessary to provide reliable grounding for the push-pull operation mode of two single-ended transistors with input and output matching circuits for each device, as shown

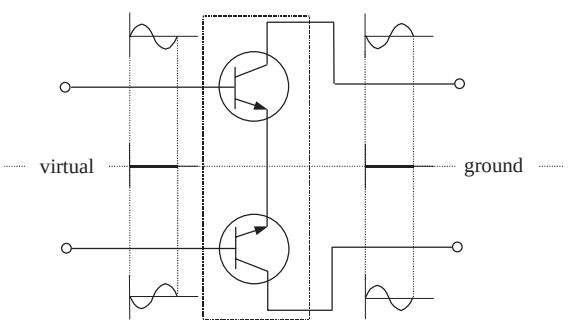

Figure 6.35 Basic concept of balanced transistor.

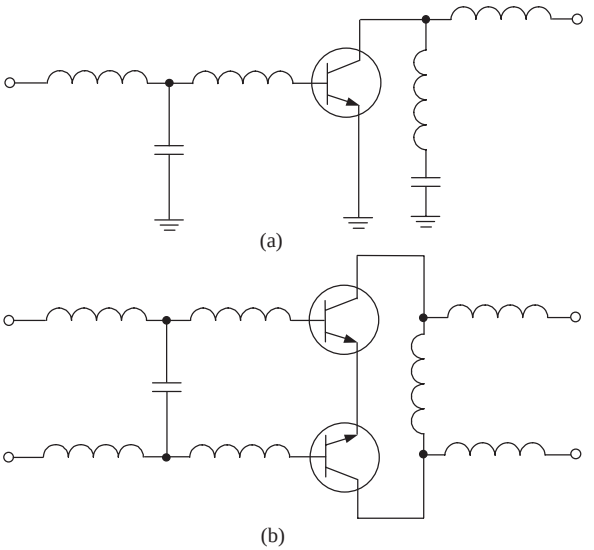

Figure 6.36 Matching technique for (*a*) single-ended and (*b*) balanced transistors.

in Fig. 6.36(*a*). An application of the balanced transistors simplifies significantly the matching circuit configuration technique by using the parallel capacitances and inductances, as shown in Fig. 6.36(*b*), when dc blocking capacitors are not required.

For push-pull operation of the power amplifier with a balanced transistor, it is necessary to provide the unbalance-to-balance transformation referenced to the ground both at the input and at the output of the amplifier. The most suitable approach to solving this problem in the best possible manner at RF and microwaves is to use the transmission-line transformers shown in Fig. 6.37. If the characteristic impedance Z_0 of the coaxial transmission line is equal to the input impedance Z_{in} applied at one end of the transformer, the impedance seen at the

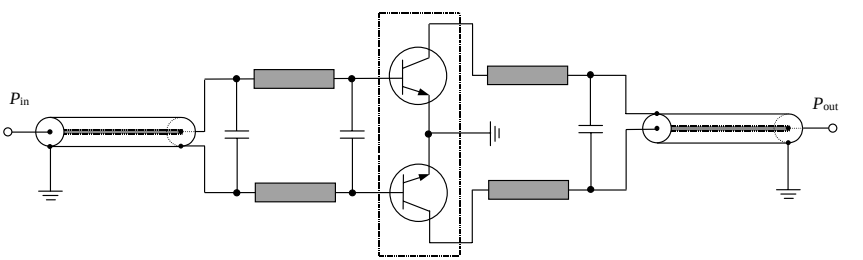

Figure 6.37 Push-pull power amplifier with balanced-unbalanced transformers.

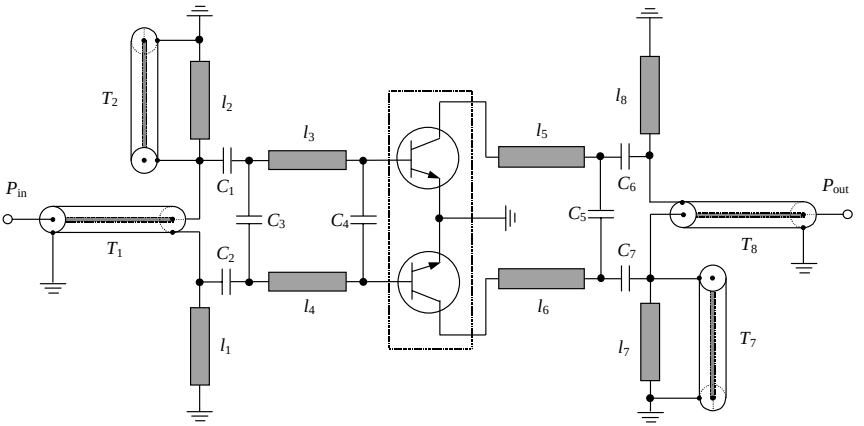

Figure 6.38 Push-pull power amplifier with compact balanced-unbalanced transformers.

other end of the transformer will be equal to the input impedance. As a result, such a transmission-line transformer can be used as a 1:1 unbalanced-to-balanced transformer. If $Z_0 = 50\,\Omega$, for the standard input impedance of 50 Ω, the impedance seen at the each balanced part is equal to 25 Ω, which is necessary to match with the appropriate input impedance of each part of a balanced transistor. The input and output matching circuits are easily realized by using the series microstrip lines with parallel capacitances.

The miniaturized compact input unbalanced-to-balanced transformers cover the frequency bandwidth up to octave with well-defined rejection-mode impedances (see Fig. 6.38) [11]. To avoid the parasitic capacitance between the outer conductor and the ground, the coaxial semirigid transformer T_1 is mounted on top of the microstrip shorted stub l_1 and soldered continuously along its length. The electrical length of this stub is usually chosen from the condition of $\theta \leq \pi/2$ on the high bandwidth frequency depending on the matching requirements. To maintain circuit symmetry on the balanced side of the transformer network, another semirigid coaxial section T_2 with unconnected center conductor is soldered continuously along the microstrip shorted stub l_2. The lengths of T_2 and l_2 are equal to the lengths of T_1 and l_1, respectively. Because the input short-circuited microstrip stubs provide inductive impedance, for matching purposes, two series capacitors of the same value, C_1 and C_2, are used, thereby forming the first high-pass matching section and providing dc blocking at the same time. The practical circuit realization of the output matching circuit and balanced-to-unbalanced transformer can be the same as for the input matching circuit.

Practical Aspect of RF and Microwave Power Amplifiers

The typical topology of a microwave linear power bipolar or GaAs MESFET amplifier, with input and output matching circuit substrates and packaged active device, usually designed for Class A operation, is shown in Fig. 6.39. Here, the matching circuits (L-transformers) are presented where the electrical lengths of the microstrip lines depend on active device impedances. The microstrip open stubs, l_1 and l_4, represent the capacitive matching impedances, the series microstrip lines, l_2 and l_3, provide the required inductive impedances, and C_1 and C_2 are the blocking capacitors. Bias circuit isolation is usually performed by quarter-wavelength microstrip open and shorted stubs of different characteristic impedances.

The electric circuit of a microwave linear power GaAs MESFET amplifier designed for 2.5 to 2.7 GHz frequency bandwidth in Class AB operation is shown in Fig. 6.40. To match device input and output inductive impedances of $Z_{\text{in}} = (1.2 + j\,20)\ \Omega$ and $Z_{\text{out}} = (4.2 + j\,25)\ \Omega$, measured at a 5-W output power level with source and load 50-Ω resistances, respectively, we combine microstrip quarter-wavelength transformers and L-transformers. Instead of open microstrip stubs, the variable capacitances in limits of 1 to 5 pF are used for fine matching tuning. A series RC circuit connected in parallel to the drain supply circuit prevents parasitic oscillations at high frequencies. To avoid the low frequency oscillations, it is necessary to use a bypass capacitor with sufficiently large capacitance in parallel to the power supply.

Figure 6.41 shows the equivalent matching circuit topology of a microwave GaAs MESFET high-power amplifier designed for S-band application. A 38.4-mm gate width device was designed in order to achieve output power of 20 W in a frequency bandwidth of 3.0 to 3.5 GHz with

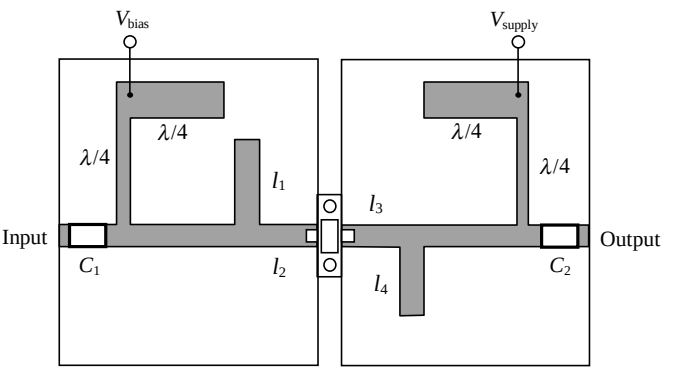

Figure 6.39 Typical topology of a microwave power amplifier.

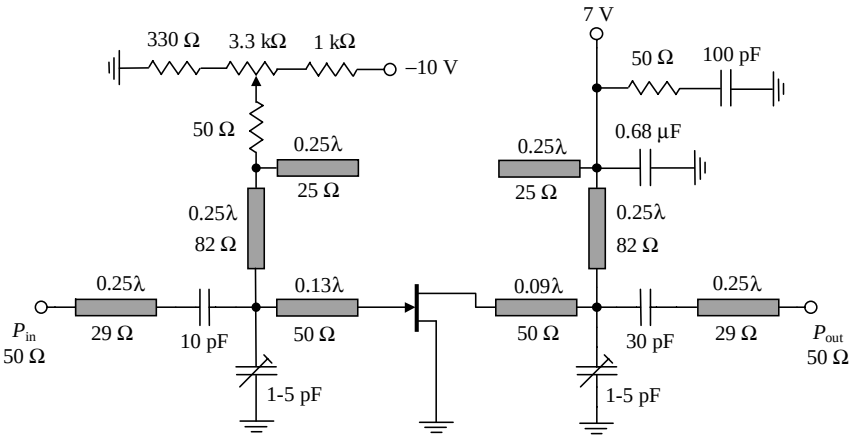

Figure 6.40 Circuit schematic of 2.5 to 2.7 GHz GaAs MESFET power amplifier.

7-dB power gain and power-added efficiency of 34 percent [12]. At the center frequency, resistance of approximately 0.2 Ω connected in series with 50-pF capacitance can represent the input device impedance, whereas the output impedance is the parallel connection of 2.5-Ω resistance and 9-pF capacitance. The input quarter-wavelength microstrip line provides an impedance transformation from 50 Ω to a quite small impedance of $(12.5 \times 12.5/50)\,\Omega = 3.125\,\Omega$. For the subsequent impedance matching with input and output device impedances, T-type lumped transformers are used with chip capacitors connected in parallel and lumped inductances realized by gold bond wires.

Figure 6.42 shows the bipolar VHF linear power amplifier using a TRW TPV-376 device. An amplifier was developed to transmit the composite TV video and audio signal in Class A operation in a frequency range of 174 to 230 MHz with at least 10-dB power gain and 30-W peak output power. The input matching circuit consists of both lumped elements composing a π-transformer and microstrip lines performed on FR-4 substrate with a dielectric permittivity of $\varepsilon_r = 4.7$. A three-turn air-core inductor realizes the lumped inductance L. The output

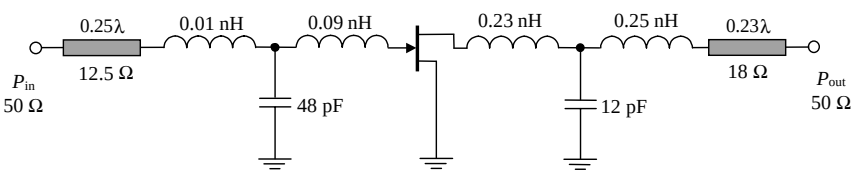

Figure 6.41 Circuit schematic of 3.0 to 3.5 GHz GaAs MESFET power amplifier [12].

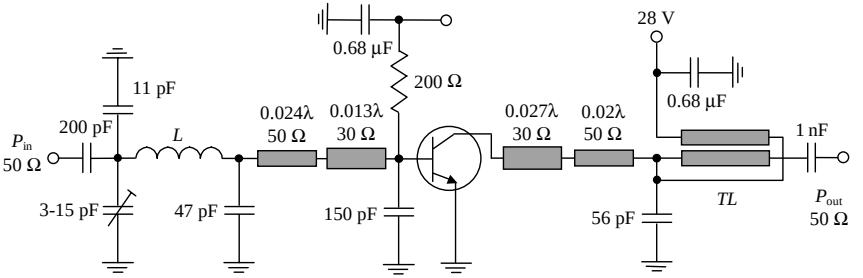

Figure 6.42 Bipolar VHF power amplifier for TV applications.

matching circuit includes a 1:2 coaxial transformer *TL* with the characteristic impedance of 25 Ω and wavelength of $\lambda/8$ in order to provide 12.5-Ω to 50-Ω final matching.

To combine the output power from two or more transistors at microwaves, we can use the branch-line 90° microstrip line hybrids, as shown in Fig. 6.43 for two power amplifiers with standard 50-Ω input and output impedances. In this case, the characteristic impedances of the transverse branches should be 50 Ω, whereas the longitudinal branches must have the characteristic impedance of $50/\sqrt{2} = 35.4\,\Omega$. In practice, due to the quarter-wavelength transmission line requirement, the bandwidth of such a balanced amplifier based on this quadrature branch-line hybrid is limited to 10–20 percent. However, a quadrature hybrid has an important advantage in comparison with *T*-junction: at equal values of reflection coefficients from loads connected to the output terminals, the reflection wave is lacking at the input terminal and, consequently, input VSWR of a branch-line hybrid does not depend on

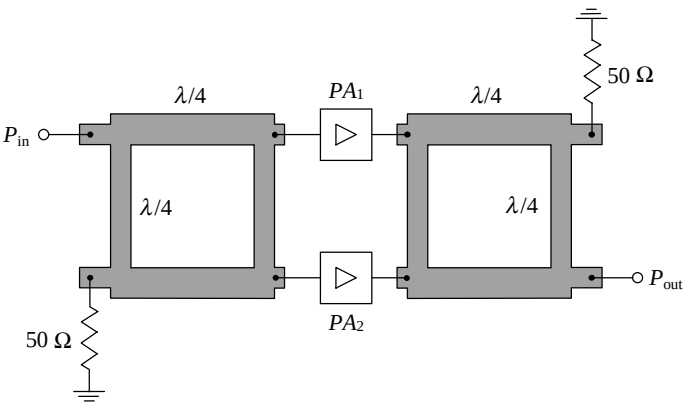

Figure 6.43 Power amplifier topology with branch-line hybrids.

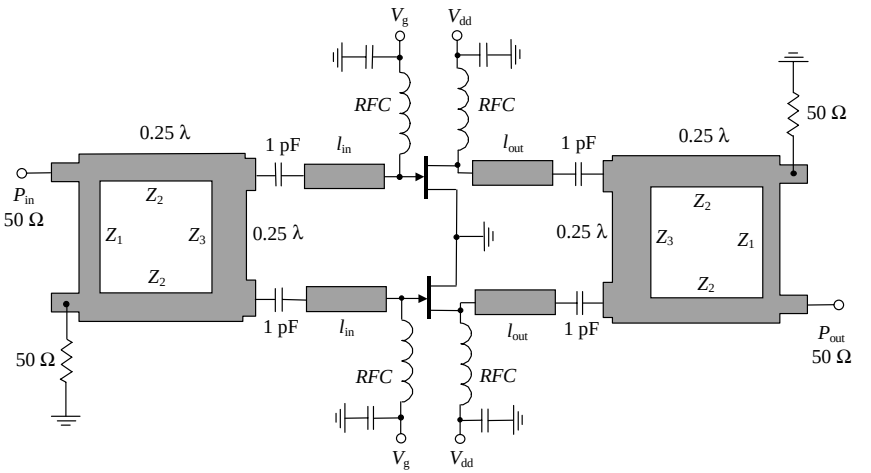

Figure 6.44 Balanced high power GaAs MESFET amplifier with branch-line impedance-transforming hybrids [13].

the equal load mismatch level, and all reflected power is dissipated in 50-Ω ballast resistor.

To simplify the requirements of the matching circuits for balanced high power amplifiers with small values of the device impedances, we can use the quadrature branch-line 90° hybrids with impedance-transforming properties [13]. An example of such a balanced GaAs MESFET amplifier with 18-W output power and 8.5-dB power gain at 1.7 GHz using NEC NE345-20 devices is shown in Fig. 6.44. The characteristic impedances of quarter-wavelength branch lines can be calculated by

$$Z_1 = Z_{\text{in}} \quad Z_2 = \sqrt{\frac{Z_{\text{in}} Z_{\text{out}}}{2}} \quad Z_3 = Z_{\text{out}} \tag{6.111}$$

Consequently, for a 50 Ω-to-20 Ω coupler, 50-Ω to 20-Ω the characteristic impedances of each branch line are $Z_1 = 50\ \Omega$, $Z_2 = 22.4\ \Omega$ and $Z_3 = 20\ \Omega$. The input and output matching circuits for each transistor can be simplified to the only series microstrip line with characteristic impedance of 20 Ω followed by a series capacitor, where $l_{\text{in}} = 7.47$ mm and $l_{\text{out}} = 6.67$ mm for alumina substrate.

In monolithic microwave applications, it is possible to increase the output power of the amplifier by connecting several active devices in parallel. In Fig. 6.45, the equivalent circuit of the monolithic 5.5 GHz power amplifier is presented, where two 4-mm gate width GaAs MESFET devices are used in order to realize a maximum output power of 34 dBm with a peak power-added efficiency of 40 percent in Class B operation [14]. The input matching circuits are T-transformers with series

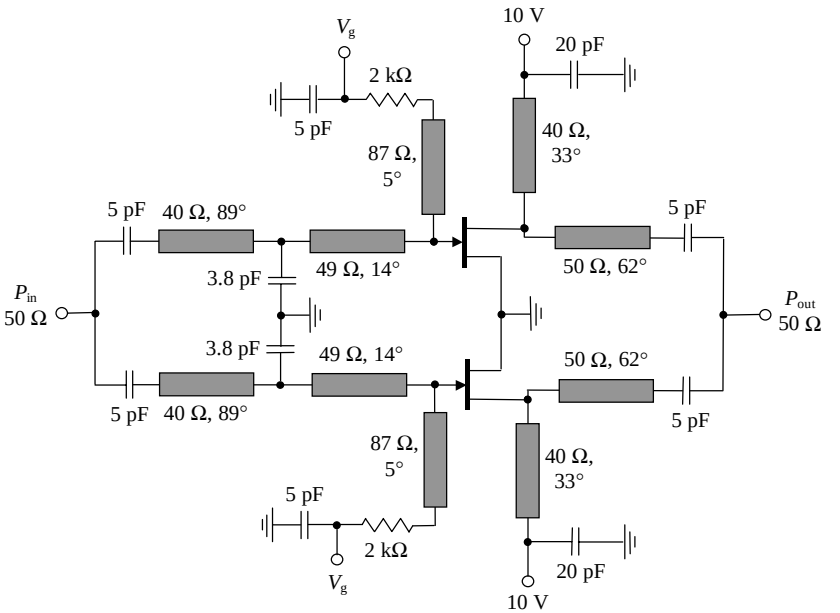

Figure 6.45 Circuit schematic of monolithic 5.5 GHz GaAs MESFET power amplifier [14].

microstrip lines, whereas two microstrip lines (parallel and series) provide output matching when it is necessary to compensate the device output reactance and to match the real part of its output impedance with a load resistance, respectively.

High-power RF amplifiers with operating frequencies of up to several gigahertz are very often designed in order to provide push-pull operation mode. For example, the high-power UHF amplifier shown in Fig. 6.46 using PTF10120 (which is an enhancement mode Ericsson's balanced LDMOSFET device) has a 120 W output power at 1-dB small-signal gain compression in the 1.93 to 1.99 GHz frequency range [15]. Typical power gain is 11 dB with drain efficiency of about 40 percent for a quiescent current of 600 mA at Class AB operation. For a push-pull operation mode, the 1:1 input coaxial transformer T_1 and 1:1 output coaxial transformer T_2 are used to provide the unbalanced-to-balanced transformation. These baluns transform the single-ended input into two signals of equal amplitudes 180° out of phase, and perform the opposite function in the output. Matching networks combine distributed and lumped elements in the low-pass configuration.

A high-power RF push-pull amplifier can be designed by using a symmetrical mirror-image connected pair of MOSFETs with the same electrical characteristics. Such an amplifier with 300-W output power

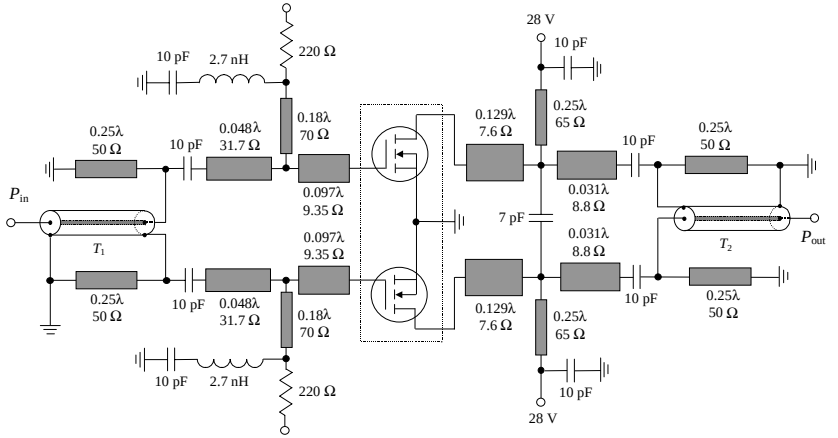

Figure 6.46 High power UHF LDMOSFET push-pull amplifier [15].

and 75 percent efficiency for the operating frequency of 81.36 MHz is shown in Fig. 6.47 [16]. The input ferrite transformer provides the 2:1 unbalanced-to-balanced transformation. Consequently, the gate impedance of each transistor, which was determined to be $(0.3 + j2.75)\ \Omega$, should be matched to the 6.25-Ω transformer secondary winding impedance. The input matching circuit for each device represents a low-pass

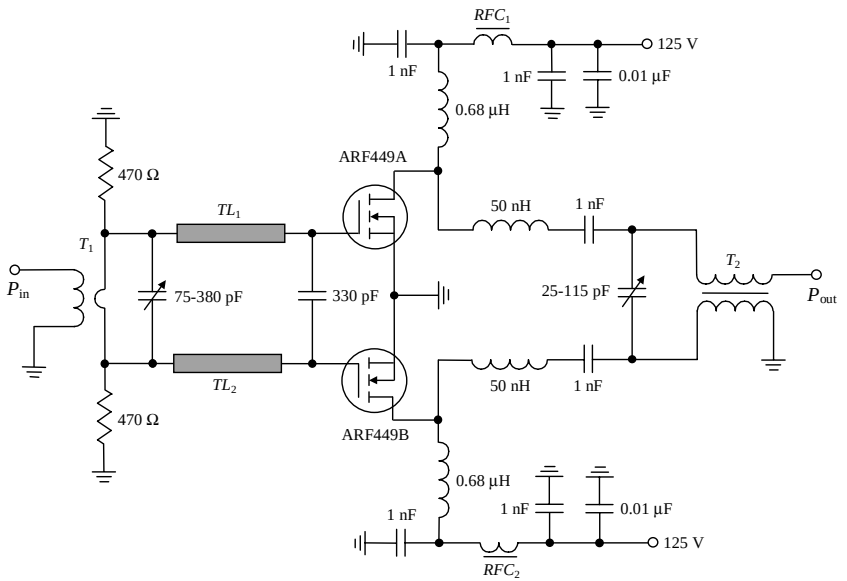

Figure 6.47 300 W VHF MOSFET power amplifier [16].

π-type section with parallel capacitances and series microstrip printed line; both TL_1 and TL_2 are 0.2 in wide, 1.80 in long, and of 35 Ω. The gates of both MOSFETs are connected to ground through the resistors on each side of the transformer secondary winding, although a single resistor at the secondary center tap would work as well. To match the output device impedance of $(9.14 - j12.6)$ Ω with the output coaxial transformer impedance of 25 Ω, it is sufficient to use a simple L-type matching section with series inductance and parallel tuning capacitance.

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Chapter

7

High-Efficiency Power Amplifier Design

Highly efficient power amplifiers can be obtained by using overdriven Class B, Class F or Class E operation modes, depending on the technical requirements. In all cases, an efficiency improvement is achieved by providing the nonlinear operation conditions when an active device can simultaneously operate in pinch-off, active and saturation regions resulting in nonsinusoidal collector current and voltage waveforms, symmetrical for Class F and asymmetrical for Class E operation modes. In Class F amplifiers analyzed in the frequency domain, the fundamental and harmonic load impedances are optimized by short-circuit termination and open-circuit peaking in order to control the voltage and current waveforms at the collector (or drain) of the device to obtain maximum efficiency. In Class E amplifiers analyzed in the time domain, an efficiency improvement is achieved by realizing the on/off active device switching operation (the pinch-off and saturation modes) with special current and voltage waveforms so that high voltage and high current do not concur at the same time.

Overdriven Class B

The idealized overdriven Class B collector current and voltage waveforms are presented in Fig. 7.1 (solid curves). The amplitudes of both the current and voltage waveforms increase, but their truncated peak values remain the same as in conventional Class B and are equal to the value of the supply voltage V_{cc} and current peak value I_s, respectively.

A Fourier analysis of the current and voltage waveforms as functions of the angular parameter θ_1 gives the following values for the voltage and current components [1]:

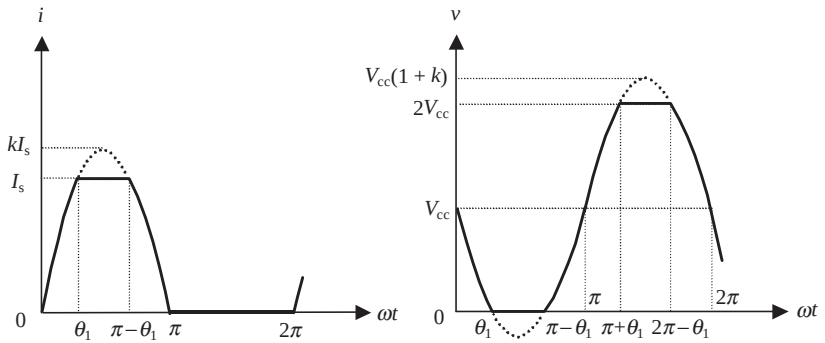


Figure 7.1 Overdriven Class B collector current and voltage waveforms.

For the dc voltage component

$$V_0 = V_{cc} \tag{7.1}$$

For the fundamental voltage component

$$V_1 = \frac{2V_{cc}}{\pi}\left(\frac{\theta_1}{\sin\theta_1} + \cos\theta_1\right) \tag{7.2}$$

For the odd voltage components

$$V_n = \frac{2V_{cc}}{\pi}\left[\frac{\sin(\theta_1 - n\theta_1)}{(1-n)\sin\theta_1} - \frac{\sin(\theta_1 + n\theta_1)}{(1+n)\sin\theta_1} + \frac{2\cos n\theta_1}{n}\right] \tag{7.3}$$

where $n = 3, 5, \ldots$

For the dc current component

$$I_0 = \frac{I_s}{\pi}\left(\frac{\pi}{2} - \theta_1 + \tan\frac{\theta_1}{2}\right) \tag{7.4}$$

For the fundamental current component

$$I_1 = \frac{I_s}{\pi}\left(\frac{\theta_1}{\sin\theta_1} + \cos\theta_1\right) \tag{7.5}$$

For the odd current components

$$I_n = \frac{I_s}{\pi}\left[\frac{\sin(\theta_1 - n\theta_1)}{(1-n)\sin\theta_1} - \frac{\sin(\theta_1 + n\theta_1)}{(1+n)\sin\theta_1} + \frac{2\cos n\theta_1}{n}\right] \tag{7.6}$$

The output power on the fundamental frequency $P_1 = V_1 I_1/2$ can be calculated as a function of the angular parameter θ_1 from

$$P_1 = \frac{V_{cc} I_s}{\pi^2}\left(\frac{\theta_1}{\sin\theta_1} + \cos\theta_1\right)^2 \tag{7.7}$$

The dc power $P_0 = V_0 I_0$ is also a function of the angular parameter θ_1, so that

$$P_0 = \frac{V_{cc} I_s}{\pi} \left(\frac{\pi}{2} - \theta_1 + \tan \frac{\theta_1}{2} \right) \tag{7.8}$$

and the out-of-band impedances are equal to

$$Z_n = \frac{2V_{cc}}{I_s} = R_L \quad \text{for odd } n \tag{7.9}$$

$$Z_n = 0 \quad \text{for even } n \tag{7.10}$$

where R_L is the load resistance. Consequently, the total power is dissipated on the load resistance not only at the fundamental (as in conventional Class B operation) but also at odd harmonic frequency components.

From expressions for the fundamental output power and dc power, the collector efficiency η can be written as

$$\eta = \frac{1}{\pi} \frac{\left(\frac{\theta_1}{\sin \theta_1} + \cos \theta_1 \right)^2}{\frac{\pi}{2} - \theta_1 + \tan \frac{\theta_1}{2}} \tag{7.11}$$

For the extreme case of the square voltage and current waveforms when θ_1 approaches zero, the collector efficiency η approaches

$$\eta = \frac{8}{\pi^2} = 81\% \tag{7.12}$$

This value is higher than in conventional Class B operation with maximum collector efficiency $\eta = 78.5\%$ that follows from Eq. (7.11) when $\theta_1 = 90^\circ$. However, analyzing Eq. (7.11) as a function of θ_1 (on extremum) results in overdriven Class B operation mode with maximum value of the collector efficiency $\eta = 88.6\%$ for angular parameter $\theta_1 = 32.4^\circ$.

To evaluate the power-added efficiency (*PAE*), it is necessary to calculate the effective operating power gain G_{Peff} in overdriven operation. If it is assumed that the overdriven effect is lacking, from Fig. 7.1 (dotted curves) it follows that in this case, a conventional Class B operation, both the current and voltage amplitudes are k times larger than the same ones in overdriven Class B operation, where $k = 1/\sin \theta_1$. Consequently, in the case of the same input power P_{in}, the output fundamental power in conventional Class B operation P_1 will be larger than that in the overdriven operation P_{1e} by k^2 times. Further, the effective

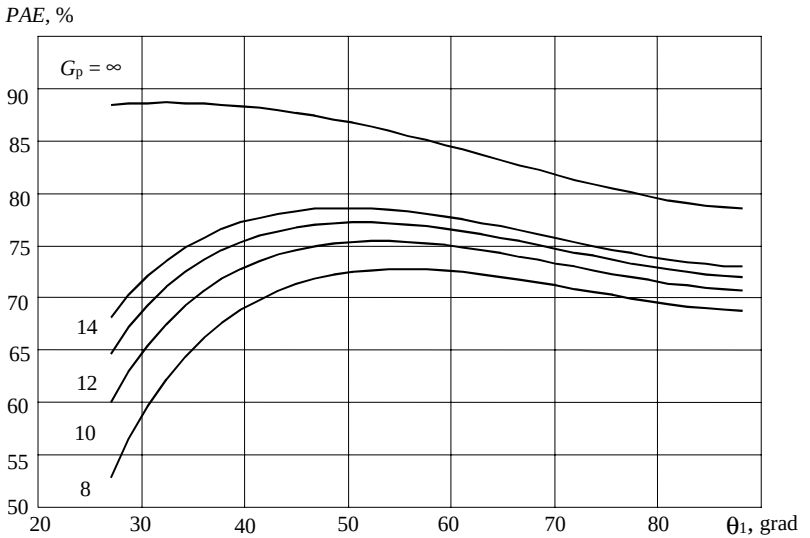


Figure 7.2 Power-added efficiency for different values of power gain.

operating power gain G_{Peff} will be smaller than the operating power gain without the overdriven effect G_{P}. This is defined by the following expression:

$$G_{\text{Peff}} = \frac{G_{\text{P}}}{k^2} \cdot \frac{P_{1e}}{P_1} = G_{\text{P}} \left(\frac{2 \sin \theta_1}{\pi} \right)^2 \left(\frac{\theta_1}{\sin \theta_1} + \cos \theta_1 \right)^2 \tag{7.13}$$

Then, the power-added efficiency as a function of the angular parameter θ_1 can be calculated according to

$$PAE = \frac{P_1 - P_{\text{in}}}{P_0} = \frac{P_1}{P_0} \left(1 - \frac{1}{G_{\text{Peff}}} \right) \tag{7.14}$$

In Fig. 7.2 the dependencies of *PAE* versus θ_1 for different values of G_{P} are shown. So, for a typical value of $G_{\text{P}} = 12$ dB in conventional Class B operation, the power-added efficiency in overdriven operation mode achieves a value of $PAE = 77.2$ percent with an optimum angular parameter of $\theta_1 = 51.4^\circ$. But in this case it is necessary to consider an excess of voltage collector amplitude V_1 in $k = 1.28$ times over supply voltage V_{cc}.

Class F Circuit Design

To increase the efficiency in overdriven Class B operation, it is advisable to use a constant value of angular parameter equal to $\theta_1 = 90^\circ$

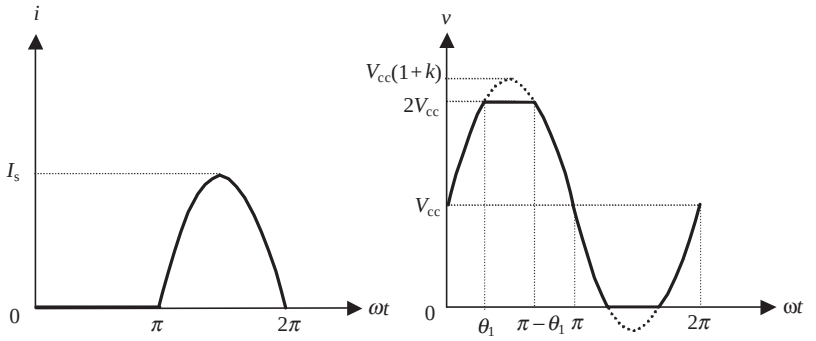


Figure 7.3 Optimum efficiency Class B collector current and voltage waveforms.

for collector current, i.e., to remain a half-sinusoidal collector current waveform, and to approach θ_1 to zero for collector voltage waveform as shown in Fig. 7.3.

In the extreme case of $\theta_1 = 0$ the collector voltage approaches a square waveform. Then, the fundamental current and voltage components will be

$$I_1 = \frac{I_s}{2} \tag{7.15}$$

$$V_1 = \frac{4V_{cc}}{\pi} \tag{7.16}$$

respectively, giving an output power at the fundamental frequency of

$$P_1 = \frac{V_{cc} I_s}{\pi} \tag{7.17}$$

Taking into account Eq. (7.1) for the dc voltage component, and Eq. (7.4) for the dc current component when $\theta_1 = 90^\circ$, gives the same value for dc output power of

$$P_0 = \frac{V_{cc} I_s}{\pi} \tag{7.18}$$

As a result, the theoretical collector efficiency achieves a maximum value of

$$\eta = \frac{P_1}{P_0} = 100\% \tag{7.19}$$

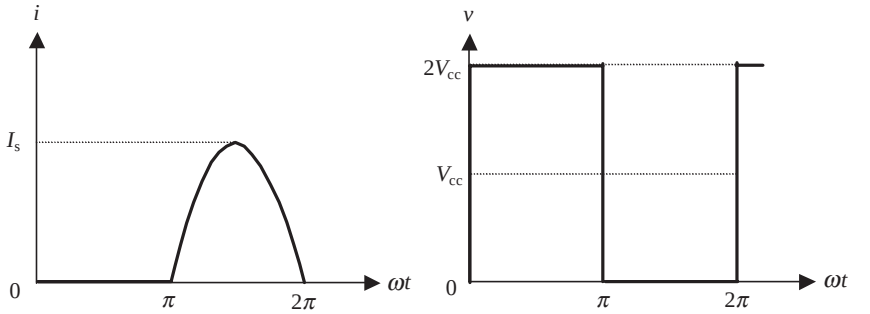


Figure 7.4 Ideal Class F current and voltage waveforms.

The impedance conditions at the device collector for 100 percent idealized collector efficiency must be

$$\begin{cases} Z_1 = R_1 = \dfrac{8}{\pi}\dfrac{V_{cc}}{I_s} \\ Z_n = 0 \quad \text{for even } n \\ Z_n = \infty \quad \text{for odd } n \end{cases} \tag{7.20}$$

The impedance conditions given by Eq. (7.20) correspond to ideal Class F operation with voltage and current waveforms shown in Fig. 7.4 [2]. Here, a sum of odd harmonics gives a square voltage waveform and a sum of fundamental and even harmonics approximates a half-sinusoidal current shape. Such a condition with symmetrical collector voltage and current waveforms, corresponding to ideal Class F operation mode with 100 percent collector efficiency, can be realized using a load network with a lossless quarterwave transmission line and a series resonant circuit with infinite quality factor (see Figs. 2.7 and 2.8 in Chap. 2).

Although it is impossible to realize the ideal harmonic impedance conditions in real hardware, the peaking of at least several current and voltage harmonic components should be provided to achieve high-efficiency operation of the power amplifier. The more the voltage waveform provided by the high-order harmonic components can be flattened, the less power dissipation due to flowing of the output current (when the output voltage is extremely small) occurs. To understand common design principles and to numerically calculate power amplifier efficiency according to the appropriate number of the frequency harmonic components of voltage and current waveforms, use a design technique applied to Class F approximation with maximally flattened waveforms [3]. The output network is assumed to be ideal, to deliver only the fundamental frequency power to the load without loss. The active device represents

an ideal current source for providing an ideal switching between saturation and pinch-off operation regions, with the saturation voltage and the output capacitance equal to zero. Flattening of the voltage and current waveforms to realize Class F operation can be accomplished by using odd harmonic components to approximate a square voltage waveform and even harmonic components to approximate a half-sinusoidal current waveform given by

$$v(\theta) = V_{cc} + V_1 \sin\theta + \sum_{n=3,5,7,\ldots}^{\infty} V_n \sin n\theta \tag{7.21}$$

$$i(\theta) = I_0 - I_1 \sin\theta - \sum_{n=2,4,6,\ldots}^{\infty} I_n \cos n\theta \tag{7.22}$$

where $\theta = \omega_0 t$, $\omega_0 = 2\pi f_0$, f_0 is the fundamental frequency.

It follows from Fig. 7.4 that the medium points where the voltage waveform reaches its maximum and minimum values are at $\theta = \pi/2$ and $\theta = 3\pi/2$, respectively. Maximum flatness at the minimum voltage requires the even derivatives to be zero at $\theta = 3\pi/2$. Since the odd-order derivatives are equal to zero due to $\cos(n\pi/2) = 0$ for odd n, it is necessary to define the even-order derivatives of the voltage waveform given in Eq. (7.21).

For third harmonic peaking, when only the third harmonic component together with the fundamental one is present, their optimum amplitudes are defined by

$$V_1 = \frac{9}{8}V_{cc} \qquad V_3 = \frac{1}{8}V_{cc} \tag{7.23}$$

The voltage waveforms for third harmonic peaking ($n = 1, 3$), fifth harmonic peaking ($n = 1, 3, 5$), and seventh harmonic peaking ($n = 1, 3, 5, 7$) are presented in Fig. 7.5.

From Fig. 7.4 it follows that the medium points where the current waveform reaches its minimum and maximum values are at $\theta = \pi/2$ and $\theta = 3\pi/2$, respectively. Since the odd-order derivatives are equal to zero due to $\cos(\pi/2) = 0$ and $\sin(n\pi/2) = 0$ for even n, defining the even-order derivatives of the current waveform given in Eq. (7.22) is necessary. Maximum flatness at the minimum current requires the even derivatives to be zero at $\theta = \pi/2$.

For second harmonic peaking, when only the second harmonic component together with the fundamental one is present, their optimum amplitudes are defined by

$$I_1 = \frac{4}{3}I_0 \qquad I_2 = \frac{1}{3}I_0 \tag{7.24}$$

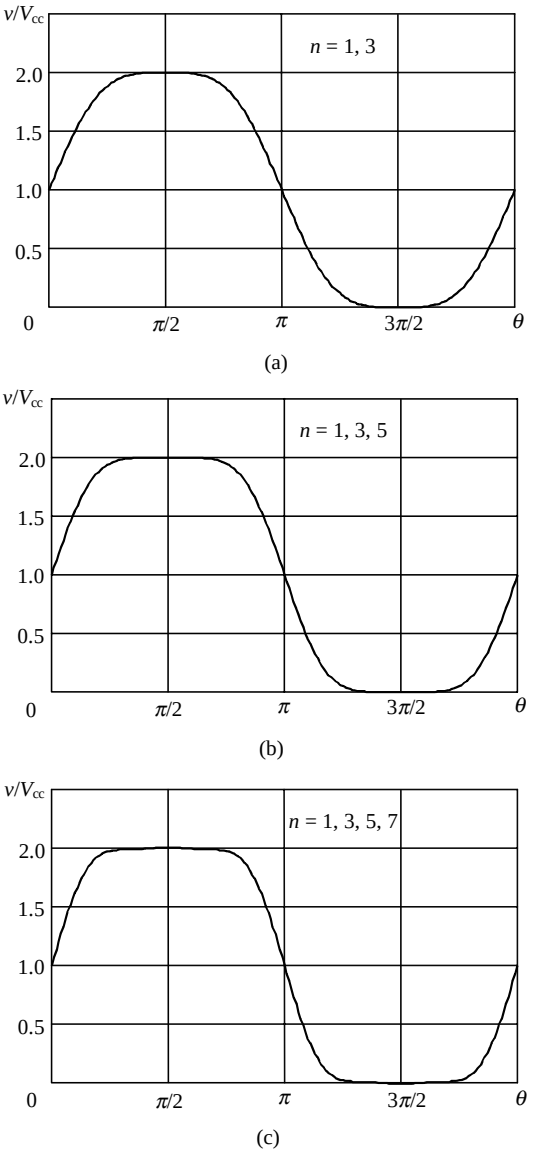
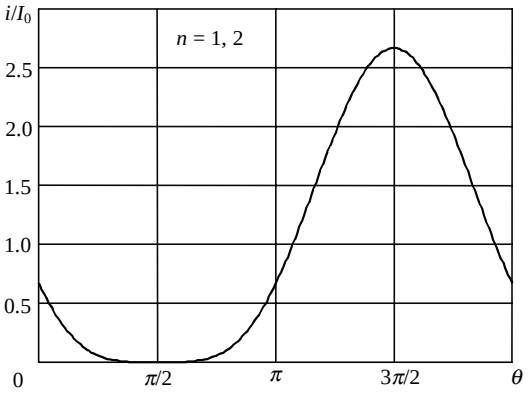


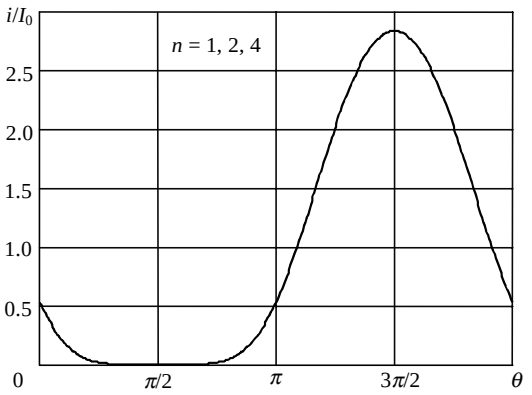
Figure 7.5 Voltage waveforms for n harmonic peaking.

The current waveforms for second harmonic peaking ($n = 1, 2$), fourth harmonic peaking ($n = 1, 2, 4$), and sixth harmonic peaking ($n = 1, 2, 4, 6$) are shown in Fig. 7.6.

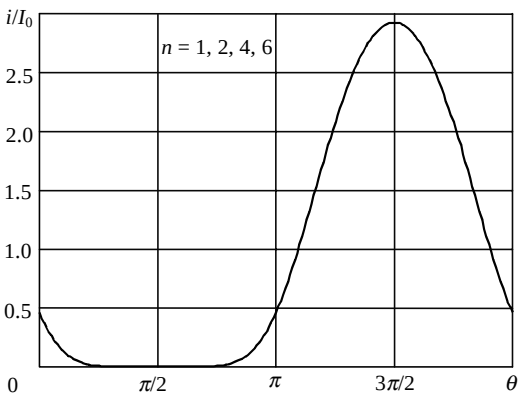
To compare the effectiveness of the operation modes with different voltage and current harmonic peaking, calculate the efficiency η of each



(a)



(b)



(c)

Figure 7.6 Current waveforms for n harmonic peaking.

operation mode in accordance with

$$\eta = \frac{P_1}{P_0} = 0.5\frac{I_1 V_1}{I_0 V_0} \tag{7.25}$$

The resultant efficiencies for various combinations of voltage and current harmonic components are presented in Table 7.1, which shows that the efficiency increases with an increase of the number of voltage and current harmonic components. To increase efficiency, it is more advisable to provide harmonic peaking in consecutive numerical order—both for voltage and current harmonic components—than it is to increase the number of the harmonic component into only voltage or current waveforms. Class F operation becomes mostly effective in comparison with Class B operation if at least third voltage harmonic peaking and fourth current harmonic peaking are realized. An inclusion of fifth voltage harmonic component increases the efficiency to 83.3 percent. Additional inclusion of a sixth harmonic component into the current waveform and a seventh harmonic component into the voltage waveform leads to efficiencies of up to 94 percent.

In practice, both extrinsic and intrinsic transistor parasitic elements have a substantial effect on the efficiency, especially at high frequencies: the influence of the output active device capacitance C_{out}, the collector capacitance C_c (in the case of the bipolar transistor) or the drain-source capacitance plus gate-drain capacitance $C_{\text{ds}} + C_{\text{gd}}$ (in the case of the FET device). At higher frequencies the influence of the output lead inductance L_{out} should be considered.

The ideal Class F amplifier with second harmonic short-circuit termination and third harmonic peaking allows maximum drain efficiency of 75 percent to be realized. For a lumped-circuit amplifier, use an additional parallel or series resonant circuits in order to approximate an ideal Class F amplifier, with harmonic impedance conditions of $Z_1 = Z_3 = \infty\,\Omega$ and $Z_2 = 0\,\Omega$ at the collector or drain, by compensating for the influence of C_{out}. Output impedance-peaking circuits with additional lumped (a) parallel and (b) series resonant circuits are shown in Fig. 7.7 [4, 5].

The reactive part of the output admittance Y_{out}, including the impedance peaking circuit that is presented in Fig. 7.7(a), can be given by

$$\text{Im}Y_{\text{out}} = \omega C_{\text{out}} - \frac{1 - \omega^2 L_2 C_2}{\omega L_1(1 - \omega^2 L_2 C_2) + \omega L_2} \tag{7.26}$$

As a result, applying three harmonic impedance conditions, open-circuited for fundamental and third harmonic and short-circuited for second harmonic, the values of the elements of this impedance-peaking

TABLE 7.1 Resultant Efficiencies for Various Combinations of Voltage and Current Harmonic Components

Current harmonic components	Voltage harmonic components				
	1	1, 3	1, 3, 5	1, 3, 5, 7	1, 3, 5, $\ldots$, ∞
1	$1/2 = 0.500$	$9/16 = 0.563$	$75/128 = 0.586$	$1225/2048 = 0.598$	$2/\pi = 0.637$
1, 2	$2/3 = 0.667$	$3/4 = 0.750$	$25/32 = 0.781$	$1225/1536 = 0.798$	$8/3\pi = 0.849$
1, 2, 4	$32/45 = 0.711$	$4/5 = 0.800$	$5/6 = 0.833$	$245/288 = 0.851$	$128/45\pi = 0.905$
1, 2, 4, 6	$128/175 = 0.731$	$144/175 = 0.823$	$6/7 = 0.857$	$7/8 = 0.875$	$512/175\pi = 0.931$
1, 2, 4, $\ldots$, ∞	$\pi/4 = 0.785$	$9\pi/32 = 0.884$	$75\pi/256 = 0.920$	$1225\pi/4096 = 0.940$	$1 = 1.000$

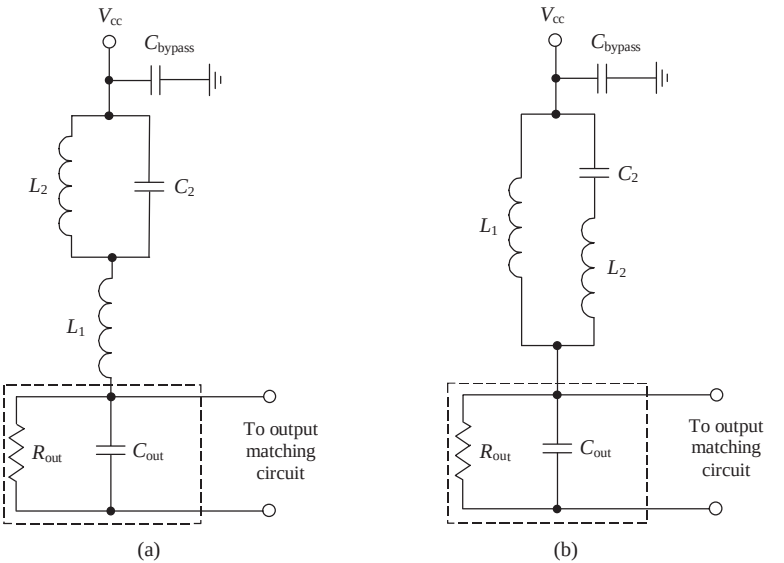


Figure 7.7 Output impedance-peaking circuits with additional lumped (*a*) parallel and (*b*) series resonant circuits.

circuit are

$$L_1 = \frac{1}{6\omega_0^2 C_{\text{out}}} \qquad L_2 = \frac{5}{3}L_1 \qquad C_2 = \frac{12}{5}C_{\text{out}} \tag{7.27}$$

Applying the same conditions for the output circuit that is shown in Fig. 7.7(*b*) obtains the following values for the elements of such an impedance-peaking circuit [6]:

$$L_1 = \frac{4}{9\omega_0^2 C_{\text{out}}} \qquad L_2 = \frac{9}{15}L_1 \qquad C_2 = \frac{15}{16}C_{\text{out}} \tag{7.28}$$

where L_2, C_2 creates a short-circuit condition at the second harmonic, and all elements create the parallel resonant tanks for fundamental and third harmonic components.

As an example, the frequency-response characteristic for the lumped impedance-peaking circuit in Fig. 7.7(*a*), whose parameters are calculated based on the fundamental frequency $f_0 = 0.5$ GHz, is given in Fig. 7.8. The circuit parameters are as follows: $L_1 = 7.7$ nH, $L_2 = 12.8$ nH, inductance quality factor $Q = 20$, $C_2 = 5.3$ pF, $R_{\text{out}} = 200\,\Omega$, and $C_{\text{out}} = 2.2$ pF. To increase the power amplifier efficiency, the element of the output matching circuit adjacent to the drain or collector of the transistor must be series and inductive to provide the high impedance on odd harmonic components. As a first approximation for numerical calculation, the output device resistance R_{out} can be

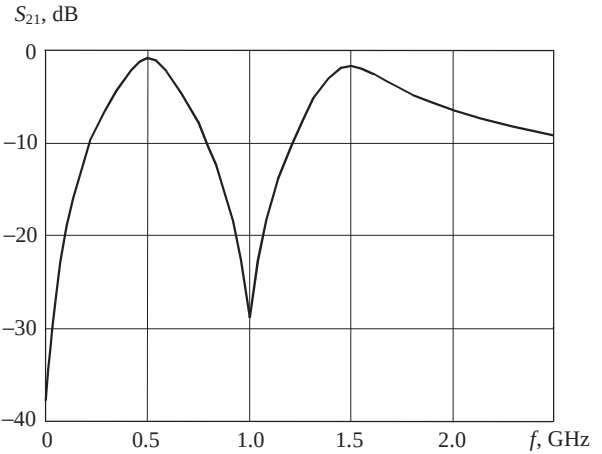


Figure 7.8 Frequency response of impedance-peaking circuit.

estimated as the equivalent resistance determined on the fundamental frequency for ideal Class F operation, $R_{\text{out}} = R_1^{(\text{F})} = V_1/I_1$. Taking into account a zero saturation voltage and using Eqs. (7.15), (7.16) and (7.20) yields

$$R_1^{(\text{F})} = \frac{4}{\pi}\frac{V_{\text{cc}}}{I_1} = \frac{4}{\pi}R_1^{(\text{B})} \tag{7.29}$$

where $R_1^{(\text{B})} = V_{\text{cc}}/I_1$ is the fundamental output resistance in Class B.

The ideal Class F amplifier with all-even harmonic short-circuit termination and third harmonic peaking achieves a maximum drain efficiency of 88.4 percent. Such an operation mode is easy to realize by using the transmission lines in the output circuit. The equivalent output impedance-peaking circuit of such a microstrip amplifier is shown in Fig. 7.9.

For the microstrip power amplifier, it is sufficient to provide the following electrical lengths of the transmission lines on fundamental frequency:

$$\theta_1 = \frac{\pi}{2} \qquad \theta_2 = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{\text{out}}}\right) \qquad \theta_3 = \frac{\pi}{6} \tag{7.30}$$

where Z_0 is the characteristic impedance of the microstrip line. As an example, the frequency-response characteristic of the microstrip impedance-peaking circuit on the alumina substrate for the device output resistance $R_{\text{out}} = 50\ \Omega$ and output capacitance $C_{\text{out}} = 2.2$ pF, characteristic impedance of microstrip lines $Z_0 = 50\ \Omega$ and electrical length $\theta_2 = 15^\circ$ is given in Fig. 7.10. From Fig. 7.10 it follows that, for the

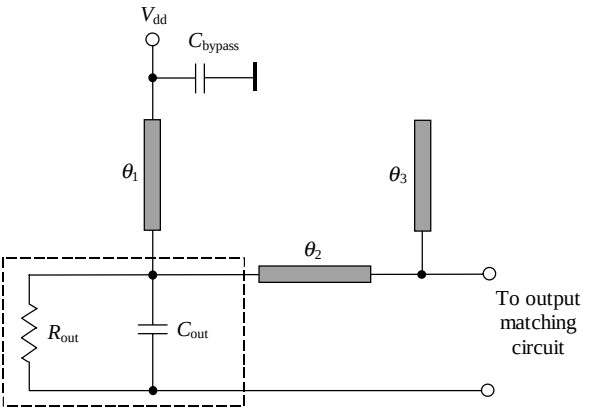


Figure 7.9 Transmission-line impedance-peaking circuit.

short-circuited conditions for all-even harmonics and third harmonic peaking, an additional output matching on the fundamental frequency $f_0 = 0.5$ GHz—taking into account the reactance due to the impedance peaking circuit—is required.

The effectiveness of the circuit design technique is demonstrated on the example of a high-power LDMOSFET amplifier. The small-signal equivalent circuit of the LDMOS device cell with channel length $L = 1.25$ μm and channel width $W = 1.44$ mm is presented in Fig. 7.11. The device model parameters were extracted from pulsed $I-V$ and S-parameter measurements. The parameters of the equivalent circuit

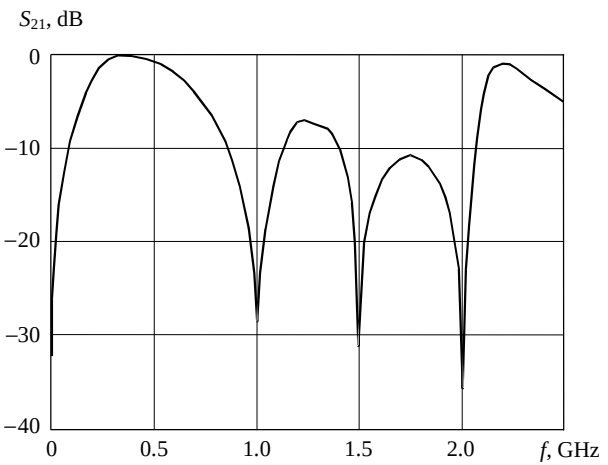


Figure 7.10 Frequency response of microstrip impedance-peaking circuit.

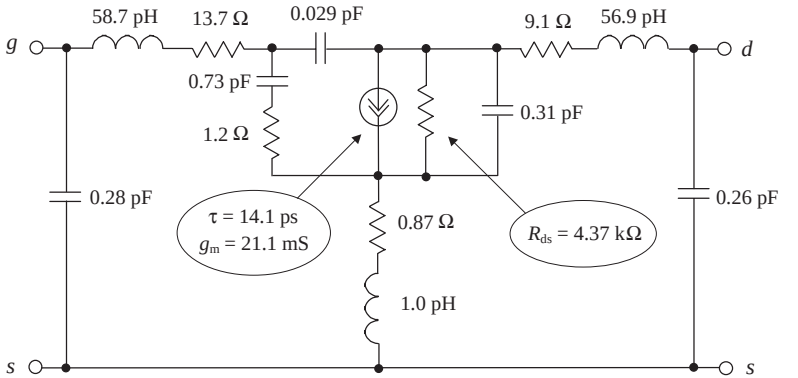


Figure 7.11 Small-signal LDMOSFET equivalent circuit.

are given at a bias voltage for Class AB operation with quiescent current $I_q = 15$ mA at $V_{dd} = 28$ V.

The equivalent circuit of the simulated 500 MHz single-stage lumped power amplifier is shown in Fig. 7.12. The total channel width of a high-voltage LDMOSFET is 7×1.44 mm. The drain efficiency and power gain versus input power P_{in} for the case of ideal circuit inductances are presented in Fig. 7.13. The values obtained for the drain efficiency greater than 75 percent (curve 2) are due to an additional harmonic peaking on higher components. This shortens the switching time from pinch-off region to saturation region by better approximating the drain voltage square waveform (Fig. 7.14, solid line). And, in this

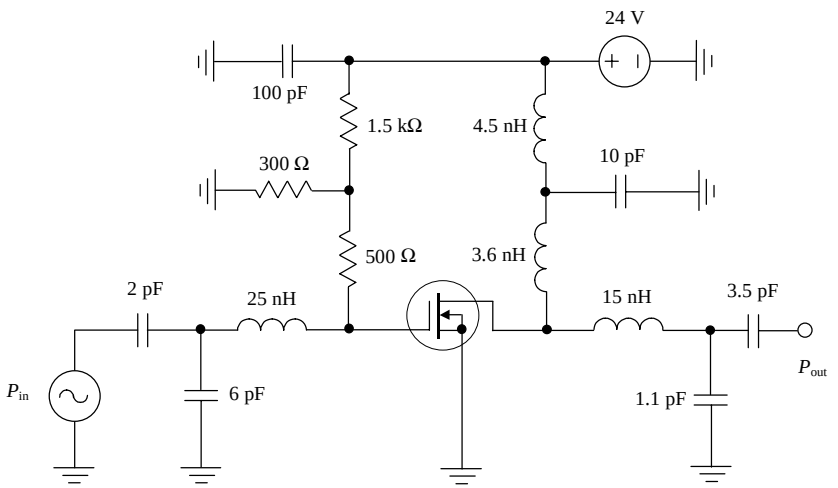


Figure 7.12 Simulated lumped LDMOSFET Class F power amplifier.

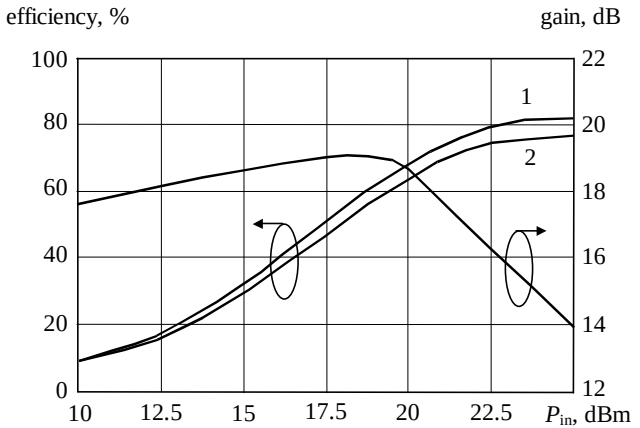


Figure 7.13 Drain efficiency and power gain versus input power.

case, the drain current waveform differs from a half-sinusoidal one because it includes higher-order odd harmonic components together with current flowing through the device internal equivalent circuit capacitances (Fig. 7.14, dotted line). The drain efficiency becomes higher than 80 percent (curve 1) if we ignore the effect of the device series drain resistance. However, the amplifier drain efficiency, as well as the power gain, can be significantly reduced with sufficiently small values in the quality factor of the circuit inductances. For example, the maximum value of the drain efficiency can be only 71 percent when a quality factor of the inductances on the fundamental frequency is $Q_{ind} = 30$, as shown in Fig. 7.15.

Therefore, for high-level output power, it is preferable to use matching circuits that employ microstrip lines. The equivalent circuit of the

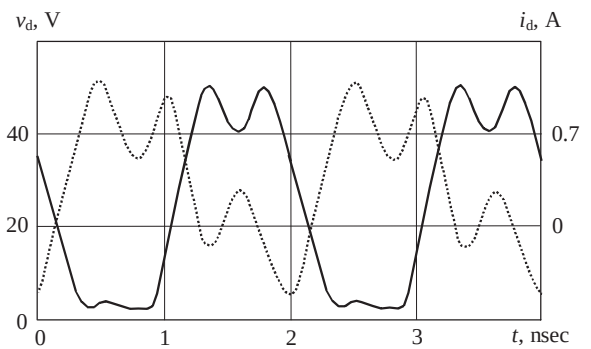


Figure 7.14 Drain voltage and current waveforms.

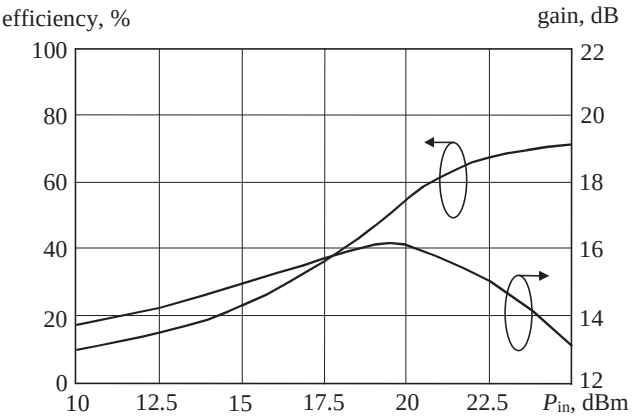


Figure 7.15 Drain efficiency and power gain versus input power.

simulated 500 MHz single-stage microstrip power amplifier is shown in Fig. 7.16. The input and output matching circuits represent T-section matching circuits, and each of them consists of a series microstrip line, parallel open-circuit stub and series capacitance. To provide even harmonic termination and third harmonic peaking for Class F operation, the RF short-circuited quarterwave microstrip line and a combination of series microstrip line and open-circuit stub of $\lambda/12$ electrical length are used. Such an output circuit configuration approximates the square drain voltage waveform (Fig. 7.17, solid line) and realizes a high drain efficiency of more than 75 percent with maximum output power $P_{out} = 8$ W (Fig. 7.18). The smaller value of the drain efficiency, in comparison with the theoretical value, can be explained by the additional

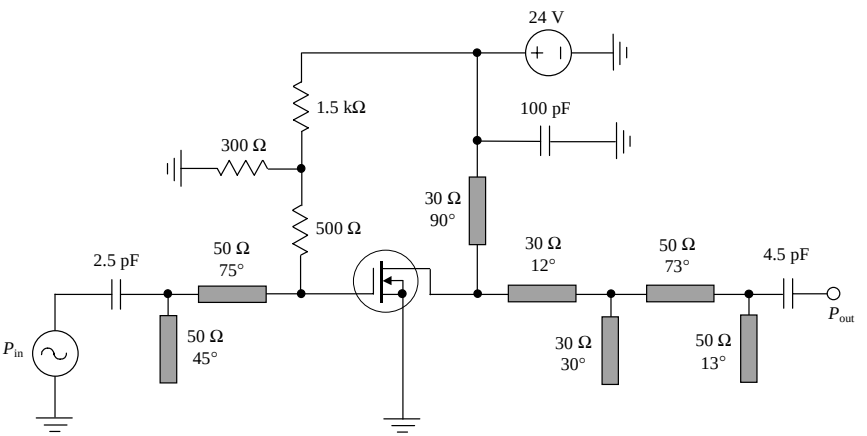


Figure 7.16 Simulated microstrip LDMOSFET Class F power amplifier.

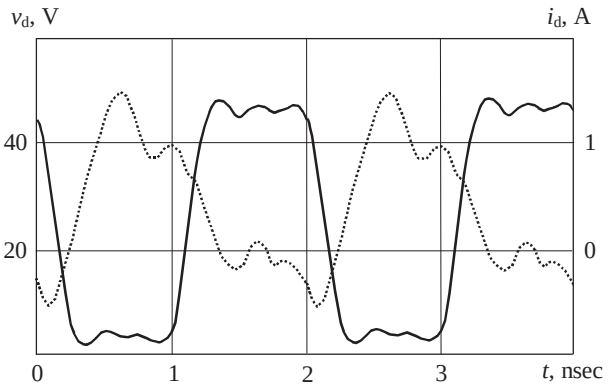


Figure 7.17 Drain voltage and current waveforms.

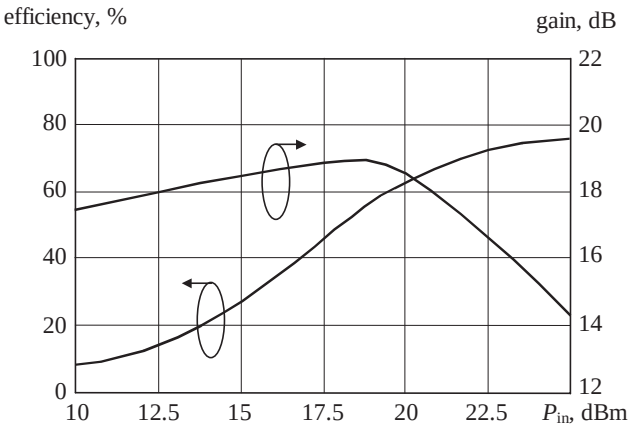


Figure 7.18 Drain efficiency and power gain versus input power.

power loss due to the saturation resistance and the parasitic drain series resistance. Also, as seen in Fig. 7.17, the drain current waveform (dotted line) differs from half-sinusoidal because the nonoptimal magnitudes of the odd harmonic components flow through the drain terminal.

Inverse Class F

The concept of inverse Class F mode was introduced mostly for low-voltage power amplifiers designed for monolithic applications [7, 8]. The inverse Class F is dual to the conventional Class F mode with the collector voltage and current waveforms being mutually interchanged. In this case, the maximum amplitude of the output current waveform

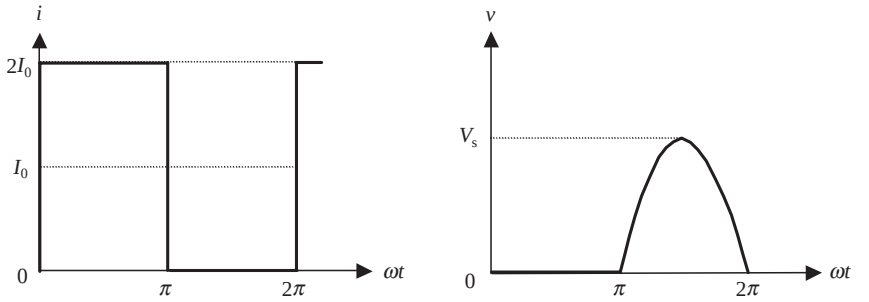


Figure 7.19 Ideal voltage and current waveforms corresponding to inverse Class F operation.

is smaller, which can contribute to reducing loss in the lumped inductances due to lower voltage drop across their parasitic resistances. The ideal voltage and current waveforms corresponding to inverse Class F operation are shown in Fig. 7.19. Here, a sum of odd harmonics gives a square current waveform and a sum of fundamental and even harmonics approximates a half-sinusoidal voltage shape.

Taking into account Eqs. (7.15) and (7.16) for ideal Class F operation mode, the fundamental current and voltage components for inverse Class F operation mode are determined by

$$V_1 = \frac{V_s}{2} = \frac{\pi}{2} V_{cc} \tag{7.31}$$

$$I_1 = \frac{4I_0}{\pi} \tag{7.32}$$

respectively, giving an output power at the fundamental frequency of

$$P_1 = \frac{V_s I_0}{\pi} = V_{cc} I_0 = P_0 \tag{7.33}$$

In this case, as well as for conventional Class F one, the theoretical collector (or drain) efficiency achieves a maximum value of 100 percent because there are no intersections between current and voltage waveforms. The impedance conditions at the device collector for 100 percent idealized collector efficiency must be

$$\begin{cases} Z_1 = R_1 = \dfrac{\pi}{8} \dfrac{V_s}{I_0} \\ Z_n = 0 \quad \text{for odd } n \\ Z_n = \infty \quad \text{for even } n \end{cases} \tag{7.34}$$

The ideal inverse Class F power amplifier cannot provide all of the voltage third-order and higher-order odd harmonic short-circuit

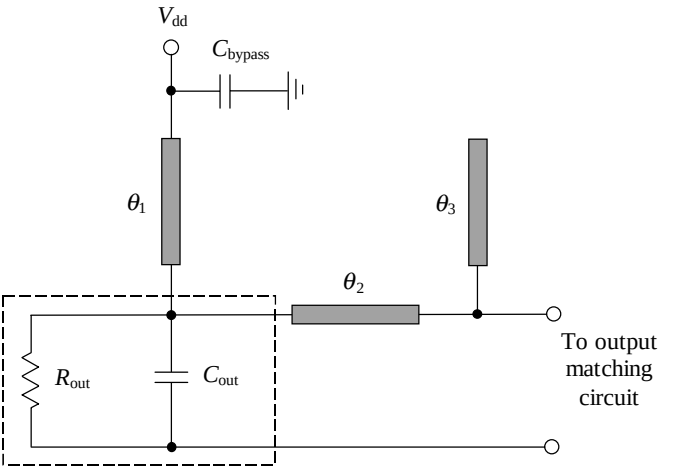


Figure 7.20 Equivalent transmission line output impedance-peaking circuit.

termination by the use of only a transmission line, as can be easily realized by quarterwave transmission line for even harmonics in the conventional Class F power amplifier. In this case, with a sufficiently simple circuit schematic convenient for practical realization, only the current second harmonic peaking and voltage third harmonic termination can be realized, with a maximum drain efficiency of 75 percent. The equivalent output impedance-peaking circuit of such a microstrip power amplifier is presented in Fig. 7.20. This circuit schematic is similar to that found in Class F operation mode. As a first approximation for numerical calculation, the output device resistance R_{out} can be estimated as equivalent resistance determined on the fundamental frequency for ideal inverse Class F operation, $R_{out} = R_1^{(invF)} = V_1/I_1$. Then, taking into account a zero saturation voltage and using Eq. (7.31) yields

$$R_1^{(invF)} = \frac{\pi}{2}\frac{V_{cc}}{I_1} = \frac{\pi^2}{8}R_1^{(F)} = \frac{\pi}{2}R_1^{(B)} \tag{7.35}$$

From Eq. (7.35) it follows that the equivalent output resistance for ideal inverse Class F is higher by more than 1.5 times than for conventional Class B operation. Therefore, using an inverse Class F operation mode simplifies the output matching circuit design. This is very important for a high-output power level when the output resistance is sufficiently small. However, the maximum amplitude of the output voltage waveform is higher than the supply voltage by about three times. In an ideal case, maximum amplitude requires that the device breakdown voltage be increased or the supply voltage be reduced.

The latter is not desirable because of a decrease in power gain and efficiency.

For such an inverse Class F microstrip power amplifier, it is necessary to provide the following electrical lengths for the transmission lines at the fundamental component:

$$\theta_1 = \frac{\pi}{3} \qquad \theta_2 = \frac{1}{2}\tan^{-1}\left[\left(2Z_0\omega_0 C_{\text{out}} - \frac{1}{\sqrt{3}}\right)^{-1}\right] \qquad \theta_3 = \frac{\pi}{4} \tag{7.36}$$

where Z_0 is the characteristic impedance of the microstrip lines. A transmission line with $\theta_1 = \pi/3$ provides a short circuit condition for the third harmonic, whereas the remaining two transmission lines, together with the device output capacitance, forms a parallel resonant circuit to realize an open circuit condition for the second harmonic at the drain terminal. As an example, the frequency-response characteristic of the microstrip impedance-peaking circuit on the alumina substrate for the device output resistance $R_{\text{out}} = 50\ \Omega$ and output capacitance $C_{\text{out}} = 2.2$ pF, characteristic impedance of microstrip lines $Z_0 = 50\ \Omega$ and electrical length $\theta_2 = 42^\circ$ is given in Fig. 7.21. From Fig. 7.21 it follows that, for the second harmonic peaking and third harmonic short-circuit termination, an additional output matching on the fundamental frequency $f_0 = 0.5$ GHz—taking into account the reactance introduced by the impedance-peaking circuit—is required.

The effectiveness of the circuit design technique for inverse Class F application is demonstrated by the example of a high-power LDMOSFET amplifier with a device of the same geometry as for conventional Class F mode. The equivalent circuit of the simulated 500 MHz

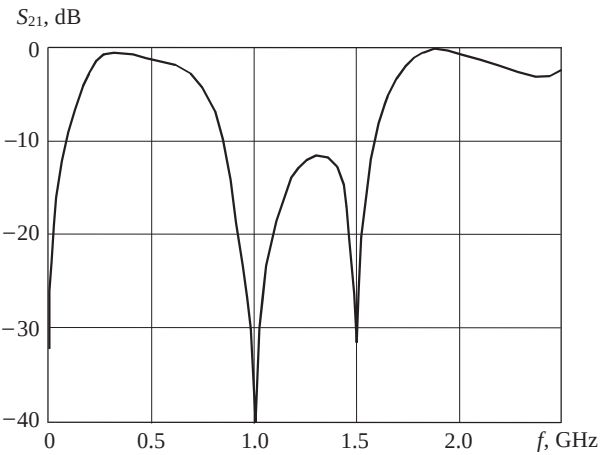


Figure 7.21 Frequency response of the microstrip impedance peaking circuit.

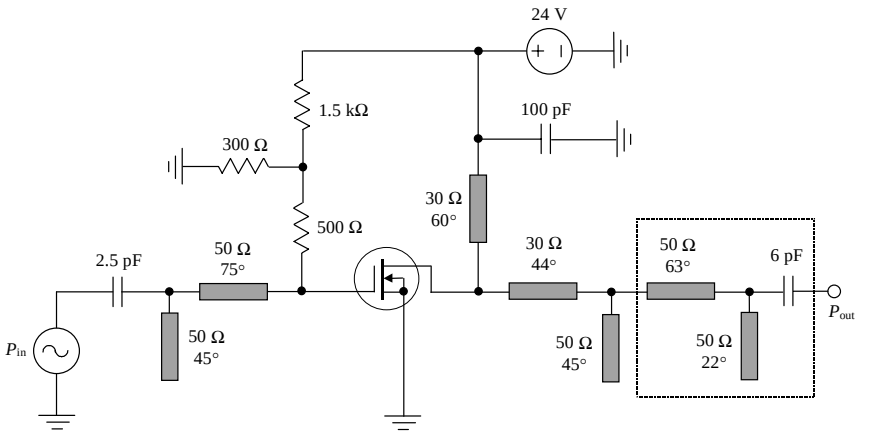


Figure 7.22 Simulated 500 MHz single-stage microstrip power amplifier.

single-stage microstrip power amplifier is shown in Fig. 7.22. The schematic of input and output matching circuits also represents a *T*-section matching circuit with a series microstrip line, parallel open-circuit stub and series capacitance. To provide the third harmonic termination and second harmonic peaking for inverse Class F operation, we use the RF short-circuited $\lambda/6$-microstrip line together with a combination of series microstrip line and open-circuit stub of $\lambda/8$ electrical length for the second harmonic termination. Figure 7.23 shows the drain voltage waveform close to the half-sinusoidal one (solid line) and the drain current waveform, which differs slightly from the ideal

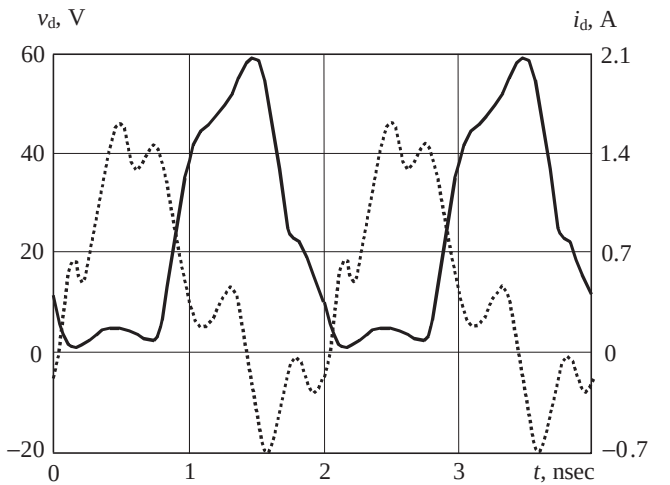


Figure 7.23 Drain voltage and current waveforms.

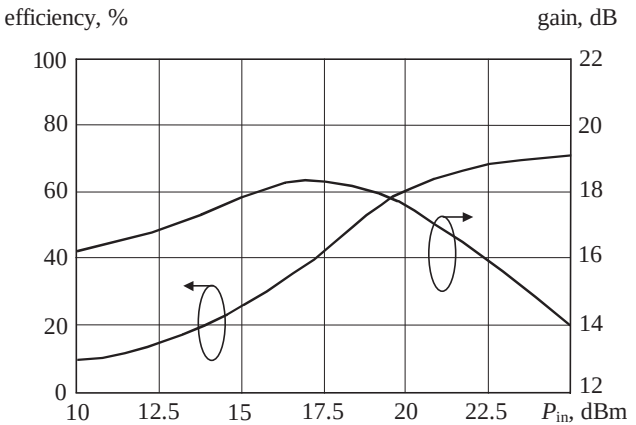


Figure 7.24 Drain efficiency and power gain versus input power.

(dotted line). In this case, the maximum value of the drain voltage is larger by 2.4 times the drain supply voltage of 24 V. Nevertheless, a drain efficiency of up to 71 percent with maximum output power $P_{out} = 8$ W is achieved (Fig. 7.24).

To minimize the number of circuit elements, the output matching circuit of such a power amplifier can also be realized in the form of a high-pass L-transformer, as shown in Fig. 7.25. Simulation results indicate that the length of the short-circuited parallel stub can approach $\lambda/4$. For particular cases, the load network designed to provide the second and third harmonic control can also perform the function of a matching circuit, together with the series capacitance required for dc

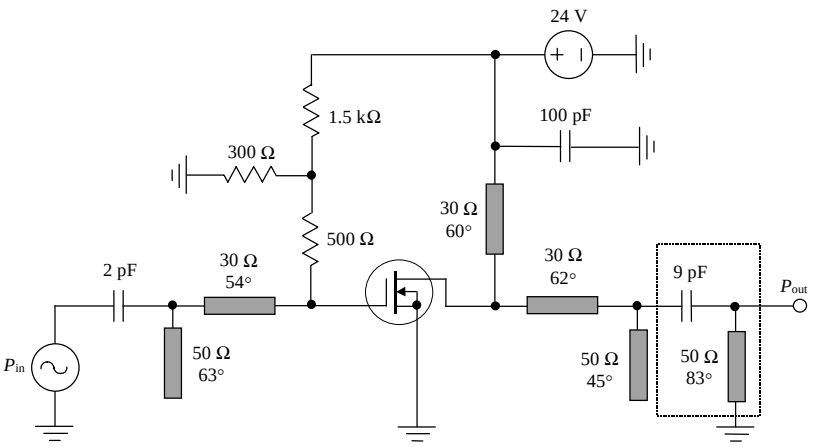


Figure 7.25 Simulated 500 MHz microstrip power amplifier with L-transformer.

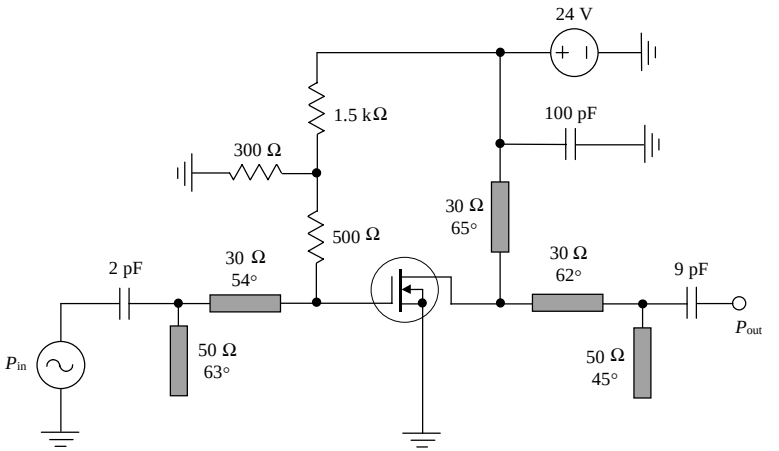


Figure 7.26 Simulated 500 MHz single-stage microstrip high-power amplifier.

blocking. The equivalent circuit of the simulated 500 MHz single-stage microstrip high-power amplifier with total LDMOSFET channel width $W = 28 \times 1.44$ mm is shown in Fig. 7.26. In this case, drain efficiency of up to 78 percent for output power of about 25 W with 14 dB power gain can be realized, as follows from Fig. 7.27. An analysis of the drain voltage and current waveforms shown in Fig. 7.28 indicates that the operation mode obtained is close to inverse Class F operation mode where the current waveform is close to the square one (dotted line) whereas the voltage waveform looks half-sinusoidal. The only difference is a small phase shift between the voltage and current waveforms. In this case, the maximum voltage magnitude does not reach even a value of 60 V.

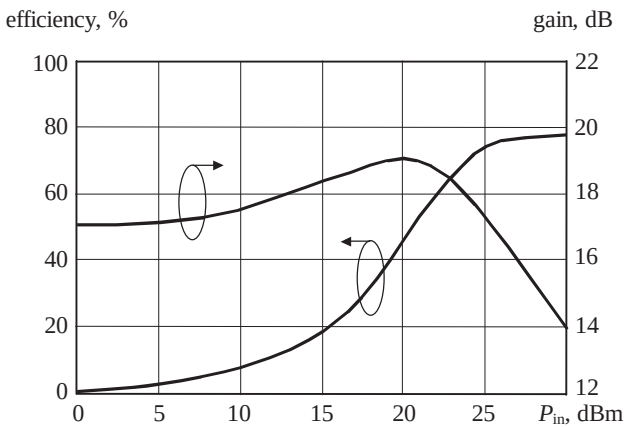


Figure 7.27 Drain efficiency and power gain versus input power.

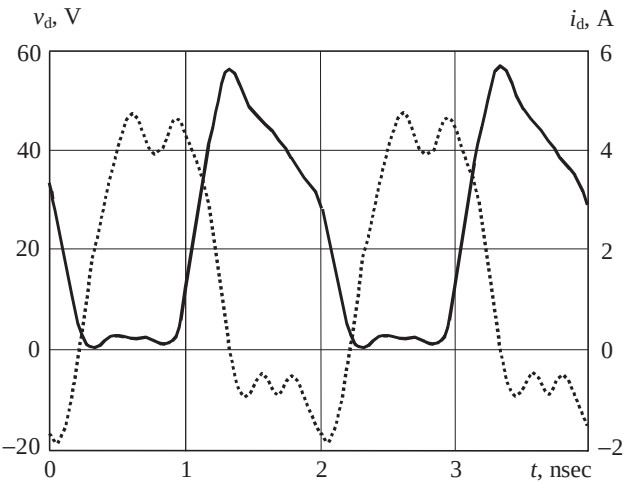


Figure 7.28 Drain voltage and current waveforms.

It is also possible to use chip capacitances instead of open circuit stubs to minimize the overall size of the power amplifier [4, 5].

Class E with Shunt Capacitance

The switched-mode tuned Class E power amplifiers with a shunt capacitance have found widespread application due to their design simplicity and high efficiency. These power amplifiers are widely used in different frequency ranges and provide output power levels ranging from several kilowatts at low RF frequencies up to about one watt at microwave frequencies. In the Class E power amplifier, the transistor operates as an on-to-off switch and the shapes of the current and voltage waveforms provide a condition where the high current and high voltage do not overlap simultaneously. This minimizes the power dissipation and maximizes the power amplifier efficiency. The possibility of increasing the efficiency of the single-ended power amplifier by mistuning the output matching circuit was found quite long ago [9]. However, the single-ended switched-mode power amplifier with a shunt capacitance as a Class E power amplifier was first introduced only in 1975 [10].

The characteristics of a Class E power amplifier can be determined by finding its steady-state collector voltage and current waveforms. The basic circuit of a Class E power amplifier with a shunt capacitance is shown in Fig. 7.29(a), where the load network consists of a capacitance C shunting the transistor, a series inductance L, a series fundamentally tuned L_0C_0-circuit and a load resistance R. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and

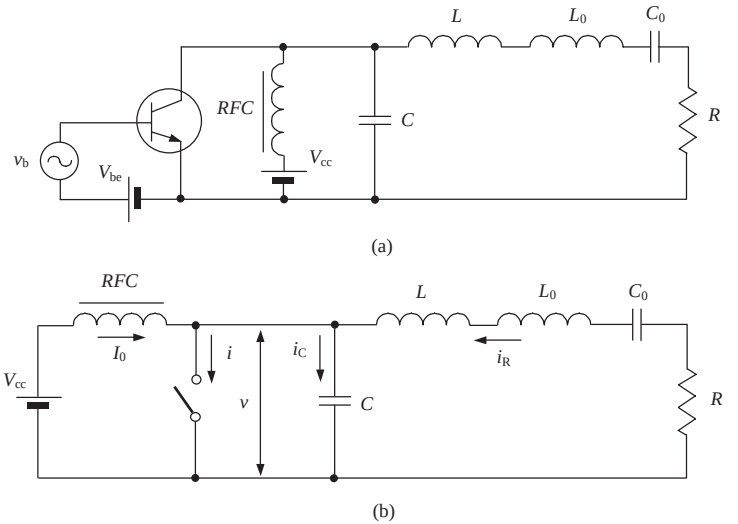


Figure 7.29 Basic circuits of a Class E power amplifier with shunt capacitance.

external circuit capacitance added by the load network. The collector of the transistor is connected to the supply voltage by an RF choke with high reactance at the fundamental frequency. The active device is considered to be an ideal switch that is driven in such a way as to switch the device between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the switch when it is turned on and by the transient response of the load network when the switch is turned off.

In order to simplify an analysis of a Class E power amplifier, a simple equivalent circuit of which is shown in Fig. 7.29(*b*), the following several assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The total shunt capacitance is independent of the collector and is assumed to be linear.
- The RF choke allows only a constant dc current and has no resistance.
- The loaded quality factor Q_L of the series resonant L_0C_0-circuit tuned on the fundamental frequency $\omega_0 = 1/\sqrt{L_0C_0}$ is high enough for the output current to be sinusoidal at the switching frequency.
- There are no losses in the circuit except only into the load R.
- For optimum operation mode a 50 percent duty cycle is used.

For the lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch just prior to the start of switch-on at the moment $t = 2\pi$, when transistor is saturated:

$$v(\omega t)|_{\omega t=2\pi} = 0 \tag{7.37}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0 \tag{7.38}$$

where v is the voltage across the switch.

The detailed theoretical analysis of a Class E power amplifier with shunt capacitance for any duty cycle is given in [11], where the output current is assumed to be sinusoidal as

$$i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi) \tag{7.39}$$

where φ is the initial phase shift.

When the switch is on for $0 \leq \omega t < \pi$, the current through the capacitance $i_{\mathrm{C}}(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0$ and, consequently,

$$i(\omega t) = I_0 + I_{\mathrm{R}} \sin(\omega t + \varphi) \tag{7.40}$$

under the initial on-state condition $i\left(0\right) = 0$. Hence, the dc current can be defined as

$$I_0 = -I_{\mathrm{R}} \sin\varphi \tag{7.41}$$

and the current through the switch can be rewritten by

$$i(\omega t) = I_{\mathrm{R}}[\sin(\omega t + \varphi) - \sin\varphi] \tag{7.42}$$

When the switch is off for $\pi \leq \omega t < 2\pi$, the current through the switch $i(\omega t) = 0$ and the current flowing through the capacitance C can be written as

$$i_{\mathrm{C}}(\omega t) = I_0 + I_{\mathrm{R}} \sin(\omega t + \varphi) \tag{7.43}$$

whereas the voltage across the switch is produced by the charging of this capacitance according to

$$v(\omega t) = \frac{1}{\omega C} \int_{\pi}^{\omega t} i_{\mathrm{C}}(\omega t) d\omega t = -\frac{I_{\mathrm{R}}}{\omega C}[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi] \tag{7.44}$$

Applying the first optimum condition given by Eq. (7.37) allows the phase angle φ to be defined as

$$\varphi = \tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482^{\circ} \tag{7.45}$$

Consideration of trigonometric relationships shows that

$$\sin\varphi = \frac{-2}{\sqrt{\pi^2+4}} \qquad \cos\varphi = \frac{\pi}{\sqrt{\pi^2+4}} \tag{7.46}$$

As a result, the steady-state voltage waveform across the switch using Eqs. (7.41) and (7.46) can be obtained in the form of

$$v(\omega t) = \frac{I_0}{\omega C}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{7.47}$$

Using Fourier-series expansion, the expression to determine the supply voltage V_{cc} can be written as

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)d\omega t = \frac{I_0}{\pi\omega C} \tag{7.48}$$

As a result, the normalized steady-state collector voltage waveform for $\pi \le \omega t < 2\pi$ and current waveform for period of $0 \le \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = \pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{7.49}$$

$$\frac{i(\omega t)}{I_0} = \omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t \tag{7.50}$$

Figure 7.30 shows the normalized (*a*) load current, (*b*) collector voltage waveform, and (*c*) collector current waveforms for idealized optimum Class E with shunt capacitance. From the collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch, and the current i consisting of the load sinusoidal current and dc current flows through the device. However, when the transistor is turned off, this current flows through the parallel capacitance C.

As a result, there is no nonzero voltage and current simultaneously, which means a lack of the power losses and gives an idealized collector efficiency of 100 percent. This implies that the dc power and fundamental output power are equal, that is

$$I_0 V_{cc} = \frac{I_R^2}{2}R \tag{7.51}$$

Consequently, the amplitude of the supply current I_0 can be determined using Eqs. (7.41) and (7.46) by

$$I_0 = \frac{V_{cc}}{R}\frac{8}{\pi^2+4} = 0.577\frac{V_{cc}}{R} \tag{7.52}$$

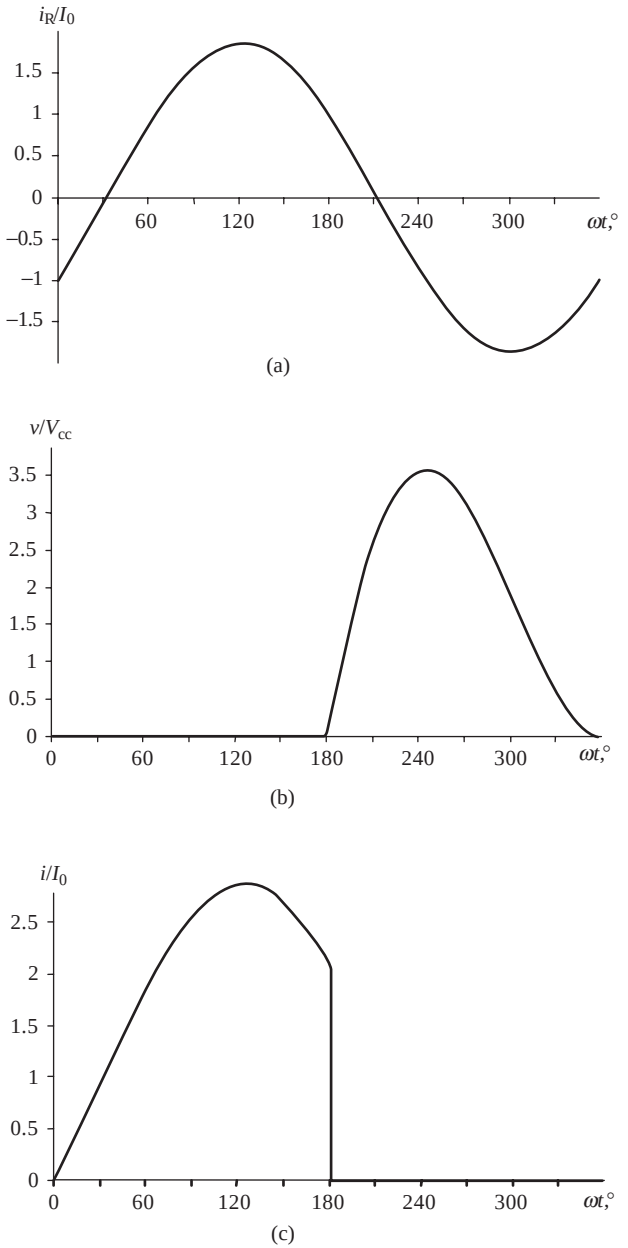


Figure 7.30 Normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum Class E with shunt capacitance.

Then, the amplitude of the output voltage $V_R = I_R R$ can be found by

$$V_R = \frac{4V_{cc}}{\sqrt{\pi^2 + 4}} = 1.074V_{cc} \tag{7.53}$$

The peak collector voltage V_s and current I_s can be determined by differentiating the appropriate waveforms given by Eqs. (7.49) and (7.50), respectively, and setting the results equal to zero, which gives

$$V_s = -2\pi\varphi V_{cc} = 3.562V_{cc} \tag{7.54}$$

and

$$I_s = \left(\frac{\sqrt{\pi^2 + 4}}{2} + 1\right) I_0 = 2.8621\, I_0 \tag{7.55}$$

The fundamental-frequency voltage $v_1(\omega t)$ across the switch consists of two quadrature components as shown in Fig. 7.31, the amplitudes of which can be found using Fourier formulas and Eq. (7.49) by

$$V_R = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin(\omega t + \varphi)d(\omega t) = \frac{I_R}{\pi\omega C}\left(\frac{\pi}{2}\sin 2\varphi + 2\cos 2\varphi\right) \tag{7.56}$$

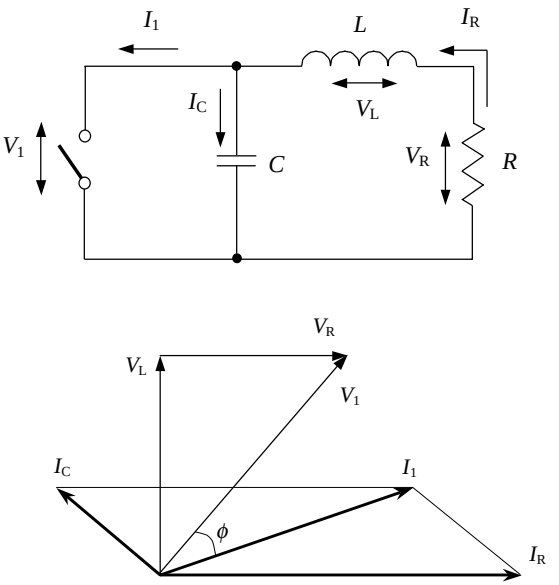


Figure 7.31 Fundamental voltage and current phasors for equivalent circuit diagram corresponding to Class E power amplifier with shunt capacitance.

$$V_{\mathrm{L}} = -\frac{1}{\pi}\int_{0}^{2\pi} v(\omega t)\cos(\omega t+\varphi)d\omega t = -\frac{I_{\mathrm{R}}}{\pi\omega C}\left(\frac{\pi}{2}+\pi\sin^2\varphi+2\sin 2\varphi\right) \tag{7.57}$$

As a result, the optimum series inductance L and shunt capacitance C can be found from

$$\frac{\omega L}{R} = \frac{V_{\mathrm{L}}}{V_{\mathrm{R}}} = 1.1525 \tag{7.58}$$

$$\omega CR = \frac{\omega C}{I_{\mathrm{R}}}V_{\mathrm{R}} = 0.1836 \tag{7.59}$$

The optimum load resistance R can be obtained using Eqs. (7.51) and (7.53) for the supply voltage V_{cc} and the output power P_{out} as

$$R = \frac{8}{\pi^2+4}\frac{V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} = 0.5768\frac{V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} \tag{7.60}$$

Finally, the phase angle of the load network at fundamental seen by the switch, and required for idealized optimum Class E with shunt capacitance, can be determined through the circuit parameters using Eqs. (7.58) and (7.59) by

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1-\frac{\omega L}{R}\omega CR}\right) = 35.945^{\circ} \tag{7.61}$$

The high-Q_{L} assumption for the series resonant L_0C_0-circuit can lead to considerable errors if its value is very small in real circuits [12]. For example, for a 50 percent duty cycle, the values of the load network parameters for a loaded quality factor less than unity can differ by several tens of percents. At the same time, for $Q_{\mathrm{L}} \geq 7$, the errors are found to be less than 10 percent and they become less than 5 percent for $Q_{\mathrm{L}} \geq 10$. Also, it is necessary to take into account the finite value of the RF choke inductance, and, when it can be observed, the increase of the output power for low inductance values [13, 14]. A detailed overview of Class E power amplifiers with shunt capacitance including explicit design equations, applicable frequency range, optimization principles and experimental results is given in [15].

These analytical results for idealized Class E operation conditions do not take into account the possible losses caused by nonideal active device properties, for example, due to the finite value of the saturation resistance r_{sat} and finite time between *on* and *off* operation conditions. The second effect can be explained by the device inertia when the base charge changes to zero with some finite time delay τ_{a}. As a

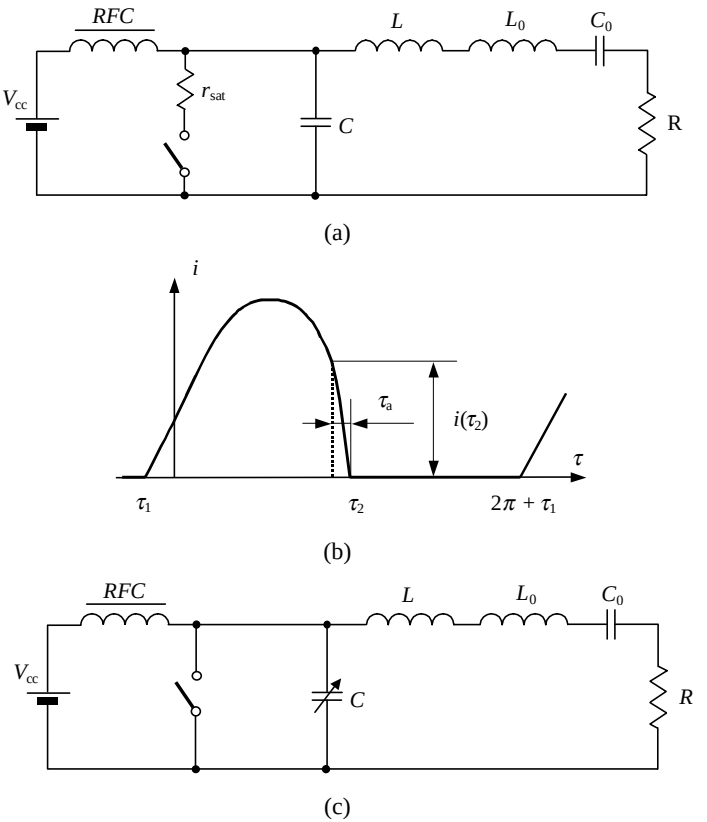


Figure 7.32 Equivalent Class E load networks (*a*) with saturation resistance and (*c*) nonlinear capacitance and (*b*) current waveform with finite time delay.

result, the base charge process determines the collector current waveform behaviour during this time delay period. So, for the equivalent circuit shown in Fig. 7.32(*a*), the average dissipated power P_{sat} can be evaluated by [9]

$$P_{\text{sat}} \cong \frac{8}{3}\frac{r_{\text{sat}}P_{\text{out}}^2}{V_{\text{cc}}^2} \tag{7.62}$$

whereas the losses due to the finite time between *on* and *off* operation conditions described by the normalized loss power P_{a} can be approximately calculated by [2, 9]

$$P_{\text{a}} \cong \frac{\tau_{\text{a}}^2}{12} \tag{7.63}$$

where τ_{a} is shown in Fig. 7.32(*b*). In this case, the losses are sufficiently small and, for example, for $\tau_{\text{a}} = 0.35$ or 20° they are only 1 percent.

In a common case, the intrinsic output device capacitance is nonlinear as shown in Fig. 7.32(*c*) and, if its contribution to the overall shunt capacitance is quite large, it is necessary to take into account the nonlinear nature of this capacitance when specifying the breakdown voltage. So, the collector voltage waveform will rise in the case of the output capacitance described by the abrupt junction in comparison to the linear one, and its maximum voltage can be greater by about 20 percent [16]. The nonlinear nature of this capacitance should also be taken into consideration when obtaining the optimum value of the series inductance.

The idealized switching conditions given by Eqs. (7.37) and (7.38) are optimum for yielding high efficiency in the case of a switch with negligibly small series resistance. However, if the switch has appreciable resistance, the higher efficiency can be achieved by moving slightly from the idealized optimum waveforms [15]. No analytical optimization procedure yet exists, but the load network parameters can be optimized numerically.

Class E with Parallel Circuit

The switched-mode tuned Class E power amplifiers with a parallel circuit are an alternative to the Class E tuned power amplifiers with a shunt capacitance realizing the high-efficiency operation mode [9, 17, 18]. In the parallel-circuit Class E power amplifier, the transistor also operates as an on-to-off switch and the shapes of the current and voltage waveforms provide a condition, when the high current and high voltage do not overlap simultaneously, that minimizes the power dissipation and maximizes the power amplifier efficiency. Such an operation mode can be achieved by an appropriate choice of the values for the reactive elements in its load network, which should be mistuned at the fundamental frequency. For the parallel-circuit Class E power amplifiers, the circuit schematic, required waveforms, phase angles and values of the circuit elements differ from those of the Class E power amplifier with shunt capacitance.

The basic circuit of a switched-mode parallel-circuit Class E power amplifier is shown in Fig. 7.33(*a*). The load network consists of a parallel inductance L, a parallel capacitance C, a series L_0C_0-resonant circuit tuned on the fundamental, and a load R. In a common case, a parallel capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network.

Let us introduce the same idealized assumptions to analyze the parallel-circuit Class E power amplifier with the optimum conditions given by Eqs. (7.37) and (7.38) that were applied to analyze the Class E power amplifier with a shunt capacitance. For the idealized theoretical

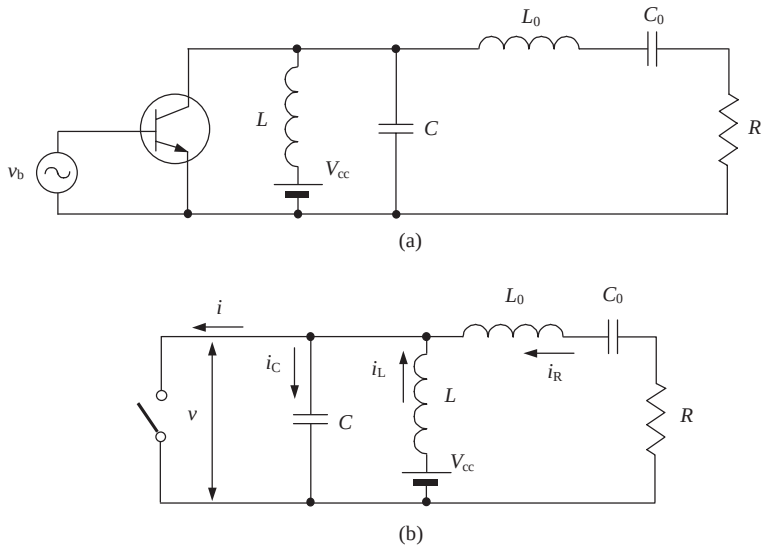


Figure 7.33 Equivalent circuits of Class E power amplifiers with parallel circuit.

analysis, it is advisable to replace the active device by the ideal switch, as shown in Fig. 7.33(*b*). Also, let the output current flowing through the load be sinusoidal with the initial phase shift φ.

When the switch is on for $0 \le \omega t < \pi$, the voltage $v(\omega t) = V_{cc} - v_L(\omega t) = 0$, the current flowing through the capacitance $i_C(\omega t) = \omega C \frac{dv(\omega t)}{d(\omega t)} = 0$ and, consequently,

$$i(\omega t) = i_L(\omega t) + i_R(\omega t) = \frac{V_{cc}}{\omega L}\omega t + I_R[\sin(\omega t + \varphi) - \sin\varphi] \tag{7.64}$$

When the switch is off for $\pi \le \omega t < 2\pi$, the current $i(\omega t) = 0$ and the current $i_C(\omega t) = i_L(\omega t) + i_R(\omega t)$ flowing through the capacitance C can be rewritten as

$$\omega C \frac{dv(\omega t)}{d(\omega t)} = \frac{1}{\omega L}\int_{\pi}^{\omega t} [V_{cc} - v(\omega t)]d(\omega t) + i_L(\pi) + I_R \sin(\omega t + \varphi) \tag{7.65}$$

under the initial off-state conditions $v(\pi) = 0$ and $i_L(\pi) = \frac{V_{cc}\pi}{\omega L} - I_R \sin\varphi$.

Equation (7.65) can be represented in the form of the linear nonhomogeneous second-order differential equation given by

$$\omega^2 LC \frac{d^2 v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{cc} - \omega L I_R \cos(\omega t + \varphi) = 0 \tag{7.66}$$

the general solution for which can be obtained in the form of

$$v(\omega t) = C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + V_{cc} - \frac{q^2}{1-q^2}\omega L I_R \cos(\omega t + \varphi) \tag{7.67}$$

where $q = 1/\omega\sqrt{LC}$ and the coefficients C_1 and C_2 are determined from the initial off-state conditions.

To solve Eq. (7.67) with regard to the three unknown parameters, it is necessary to use the two optimum conditions given by Eqs. (7.37) and (7.38) and to add an additional equation defining the supply voltage V_{cc} from a Fourier-series expansion as

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t) d\omega t \tag{7.68}$$

As a result, the following exact values can be obtained numerically for the unknown parameters:

$$q = 1.412 \tag{7.69}$$

$$\varphi = 15.155^\circ \tag{7.70}$$

$$\omega L I_R = 1.21\ V_{cc} \tag{7.71}$$

The dc supply current I_0 can be found using the Fourier formula by

$$\begin{aligned} I_0 &= \frac{1}{2\pi}\int_0^{2\pi} i(\omega t) d(\omega t) \\ &= \frac{I_R}{2\pi}\left(\frac{V_{cc}}{\omega L I_R}\frac{\pi^2}{2} + 2\cos\varphi - \pi\sin\varphi\right) = 0.826 I_R \end{aligned} \tag{7.72}$$

Figure 7.34 shows the normalized (a) load current and collector (b) voltage and (c) current waveforms for idealized optimum parallel-circuit Class E operation. From the collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch and current i—consisting of the load sinusoidal and inductive currents—flows through the device. However, when the transistor is turned off, this current now flows through the parallel capacitance C. As a result, there is no nonzero voltage and current simultaneously. When this happens, no power loss occurs and an idealized collector efficiency of 100 percent is achieved. The normalized currents flowing through the load network parallel (a) capacitance C and (b) inductance L for idealized optimum parallel-circuit Class E operation mode are shown in Fig. 7.35.

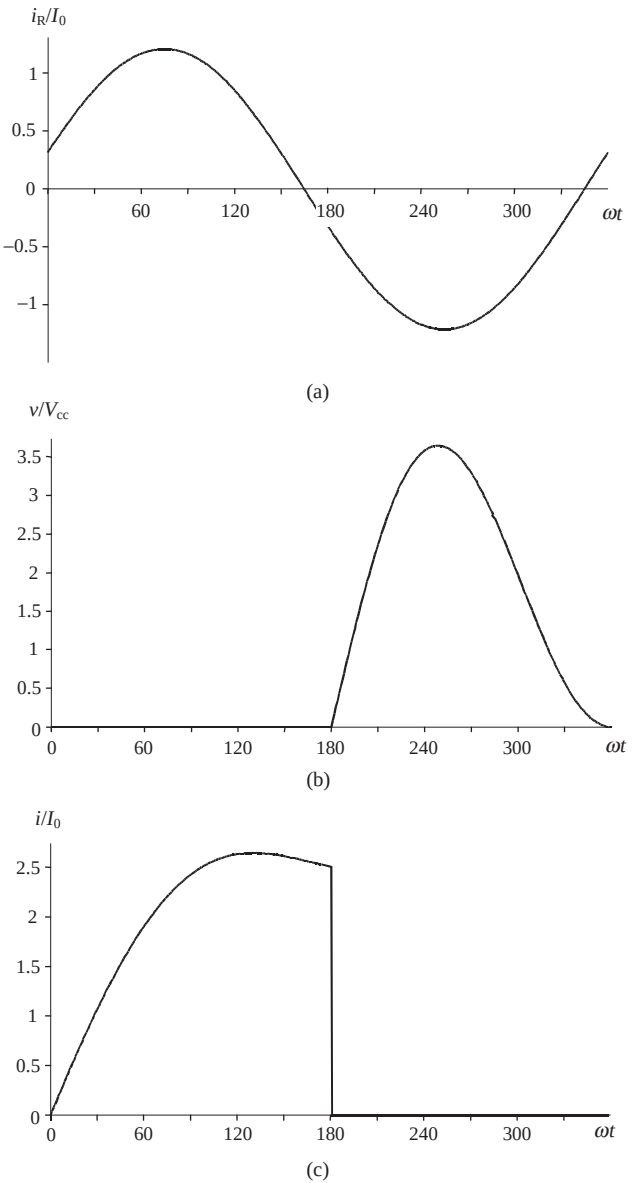


Figure 7.34 Normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum parallel-circuit Class E.

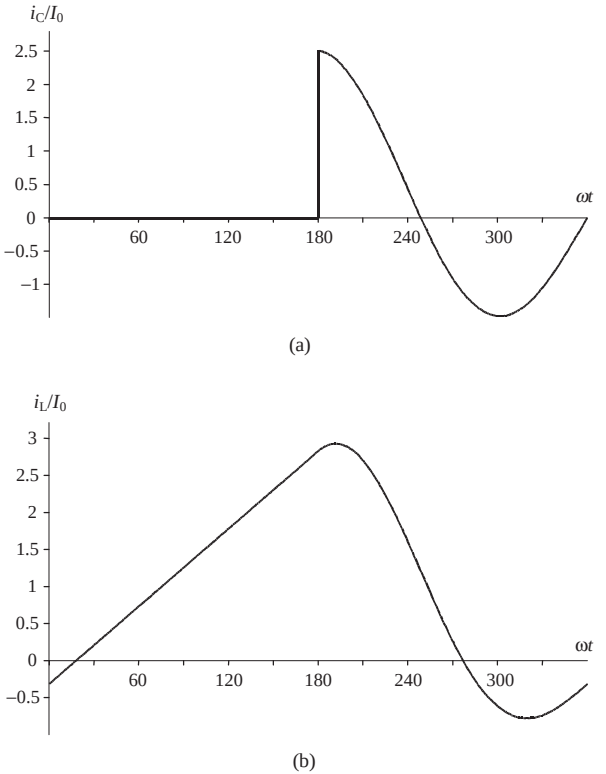


Figure 7.35 Normalized currents flowing through load network parallel (*a*) capacitance and (*b*) inductance for idealized optimum parallel-circuit Class E.

The fundamental-frequency current $i_1(\omega t)$ flowing through the switch consists of the two quadrature components shown in Fig. 7.36, the amplitudes of which can be found using Fourier formulas and Eq. (7.64) by

$$I_R = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\sin(\omega t+\varphi)d(\omega t)$$

$$= \frac{I_R}{\pi}\left[\frac{V_{cc}}{\omega L I_R}(\pi\cos\varphi - 2\sin\varphi) + \frac{\pi}{2} - \sin 2\varphi\right] \tag{7.73}$$

$$I_X = -\frac{1}{\pi}\int_0^{2\pi} i(\omega t)\cos(\omega t+\varphi)d(\omega t)$$

$$= \frac{I_R}{\pi}\left[\frac{V_{cc}}{\omega L I_R}(\pi\sin\varphi + 2\cos\varphi) - 2\sin^2\varphi\right] \tag{7.74}$$

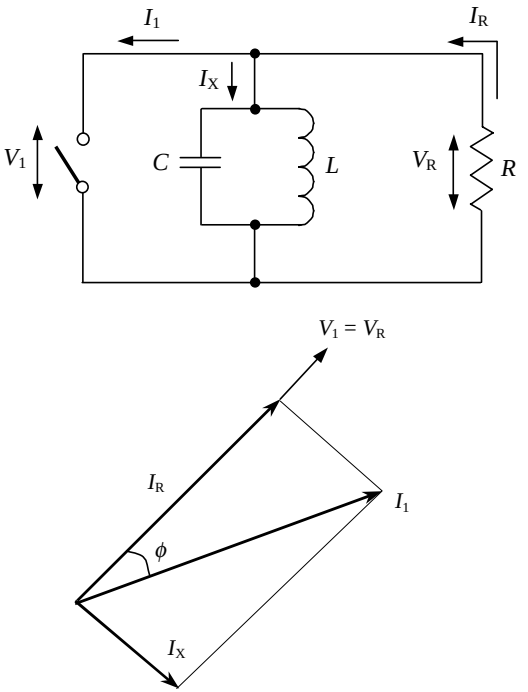


Figure 7.36 Phasor diagram corresponding to Class E power amplifier with parallel circuit.

Consequently, the phase angle ϕ between the fundamental-frequency voltage $v_1(\omega t)$ and current $i_1(\omega t)$ applied to the switch terminal is equal to

$$\phi = \tan^{-1}\left(\frac{I_X}{I_R}\right) = 34.244^\circ \tag{7.75}$$

Alternatively, the phase angle ϕ can be represented as a function of load network elements as

$$\tan\phi = \frac{R}{\omega L} - \omega RC \tag{7.76}$$

Hence, the normalized load network parameters can be obtained by

$$\frac{\omega L}{R} = \frac{q^2 - 1}{q^2 \tan\phi} \tag{7.77}$$

$$\omega RC = \frac{\tan\phi}{q^2 - 1} \tag{7.78}$$

As a result, using Eqs. (7.69) and (7.75) the optimum parallel inductance L and parallel capacitance C can be determined by

$$L = 0.732\frac{R}{\omega} \tag{7.79}$$

$$C = \frac{0.685}{\omega R} \tag{7.80}$$

The optimum load resistance R for the specified values of supply voltage V_{cc} and output power P_{out} can be obtained from Eq. (7.71), taking into account that $R = V_R^2/2P_{out}$, by

$$R = 1.365\frac{V_{cc}^2}{P_{out}} \tag{7.81}$$

The parameters of the series resonant circuit as functions of the loaded quality factor Q_L (whose value should be as high as possible) are calculated by

$$C_0 = \frac{1}{\omega R Q_L} \tag{7.82}$$

$$L_0 = \frac{1}{\omega^2 C_0} \tag{7.83}$$

If the calculated value of the resistance R for the optimum Class E power amplifier is too small or differs significantly from the required load impedance, it is necessary to use an additional matching circuit to deliver maximum output power to the load. In this case, the first series element of such matching circuits should be the inductance to provide high impedance conditions for harmonics, as shown in Fig. 7.37.

The peak collector current I_s and peak collector voltage V_s can be determined from Eqs. (7.64) and (7.67) as

$$I_s = 2.647 I_0 \tag{7.84}$$

$$V_s = 3.647 V_{cc} \tag{7.85}$$

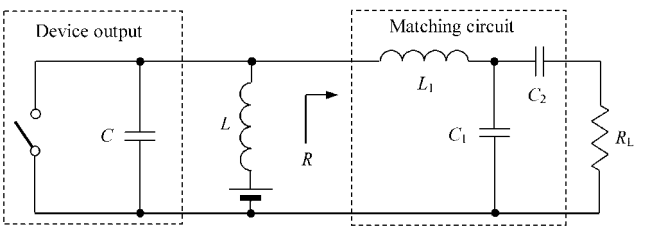


Figure 7.37 Parallel-circuit Class E power amplifier with lumped matching circuit.

When realizing the optimum Class E operation mode, it is important to know the maximum frequency that such an efficient operation mode can achieve. In this case, it is advisable to establish a relationship between the maximum frequency $f_{\max}$, device output capacitance C_{out} and supply voltage V_{cc}. The device output capacitance C_{out} gives the main limitation of the maximum operation frequency, as it is an intrinsic device parameter and cannot be reduced for a given active device. So, using Eqs. (7.80) and (7.81) when $C = C_{\text{out}}$ gives the value of maximum operation frequency of

$$f_{\max} = 0.0798 \frac{P_{\text{out}}}{C_{\text{out}} V_{\text{cc}}^2} \tag{7.86}$$

which is 1.4 times higher than maximum operation frequency for an optimum Class E power amplifier with shunt capacitance [19].

Class E with Transmission Lines

At microwave frequencies, to minimize the insertion losses, the transmission lines should replace any lumped inductances in the output matching circuit. For example, the matching circuit can be composed of any type of transmission lines—including open-circuited or short-circuited stubs—to provide the required matching and harmonic suppression conditions. As a result, to approximate the idealized Class E with shunt capacitance, it is necessary to design the transmission-line load network to satisfy the required idealized optimum impedance at the fundamental given by

$$Z_{\text{net1}} = R\,(1 + j \tan 49.052^\circ) \tag{7.87}$$

which can be obtained from Eqs. (7.58) and (7.59) [11]. At the same time, the open-circuited conditions should be realized for all higher-order harmonics. However, as it turned out from the Fourier analysis, a good approximation to Class E mode may be obtained with only two harmonics (fundamental and second) of the voltage waveform across the switch [20]. In Fig. 7.38(a), the voltage waveform containing these two harmonic components (dotted line) is plotted along with the ideal one (solid line). In this case, the load network for Class E with shunt capacitance designed for microwave applications includes the series microstrip line l_1 and open-circuited stub l_2, as shown in Fig. 7.38(b). The electrical lengths of lines l_1 and l_2 are chosen to be of about 45° at the fundamental to provide an open circuit condition at the second harmonic, whereas their characteristic impedances are calculated to satisfy the required inductive impedance condition at the fundamental.

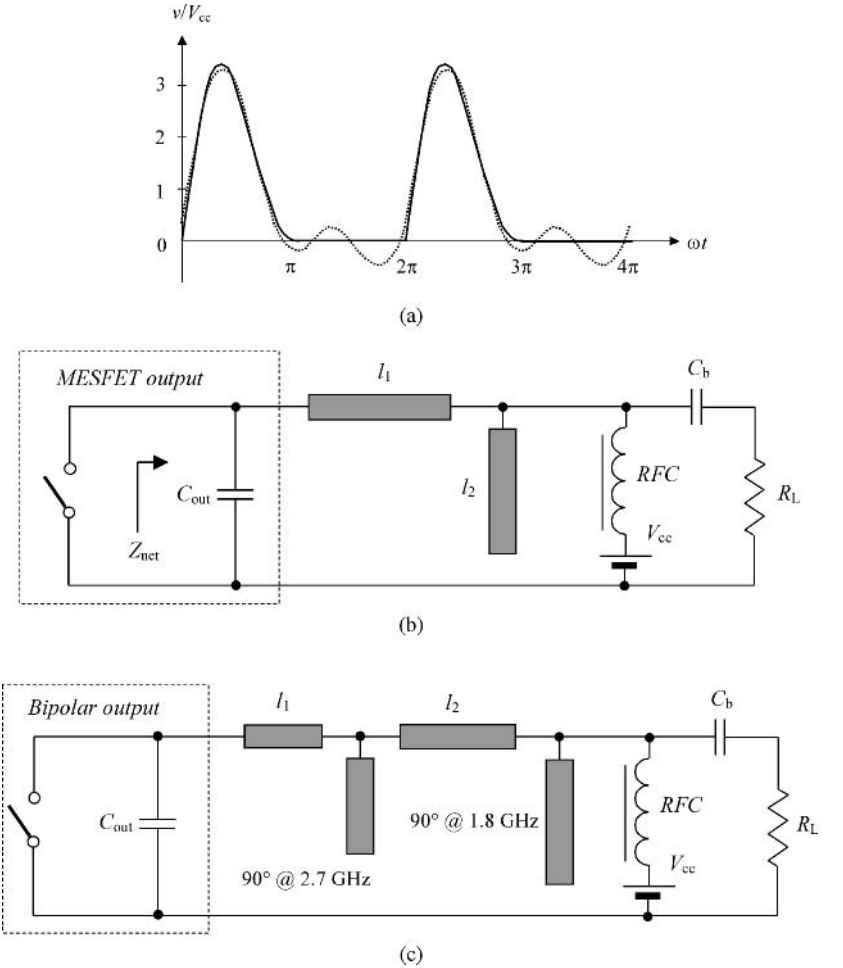


Figure 7.38 Two-harmonic voltage waveform and equivalent circuits of Class E power amplifiers with transmission lines.

The output lead inductance of the packaged device can be accounted for by shortening the length of l_1.

An additional increase of the collector efficiency can be provided by the load impedance control at both the second and third harmonics [21]. Such a harmonic control network consists of the open-circuited quarterwave stubs both at the second harmonic and third one separately, as shown in Fig. 7.38(c), where the third harmonic quarterwave stub is located before the second harmonic one. It is possible to achieve very high collector efficiency even with values of the device output capacitance higher than is conventionally required, as long as the load at the

second and third harmonics is kept strictly inductive. As a result, maximum collector efficiency over 90 percent for a power amplifier with an output power of 1.5 W can be realized at 900 MHz.

The same Fourier analysis can be applied to the parallel-circuit Class E power amplifier, when a good approximation to the idealized voltage and current collector waveforms can also be obtained with only the first and second harmonics. Here, as a first step, the parallel inductance L at microwaves should be replaced by the short-length short-circuited transmission line TL, as shown in Fig. 7.39(a), according to

$$Z_0 \tan\theta = \omega L \tag{7.88}$$

where Z_0 and θ are the characteristic impedance and electrical length of the transmission line TL, respectively. To approximate the idealized parallel-circuit Class E operation conditions for a microwave power amplifier, it is necessary to design the transmission-line load network to satisfy the required idealized optimum impedance at the fundamental given by

$$Z_{\text{net1}} = R/(1 - j\tan 34.244^\circ) \tag{7.89}$$

which can be obtained using Eqs. (7.79) and (7.80).

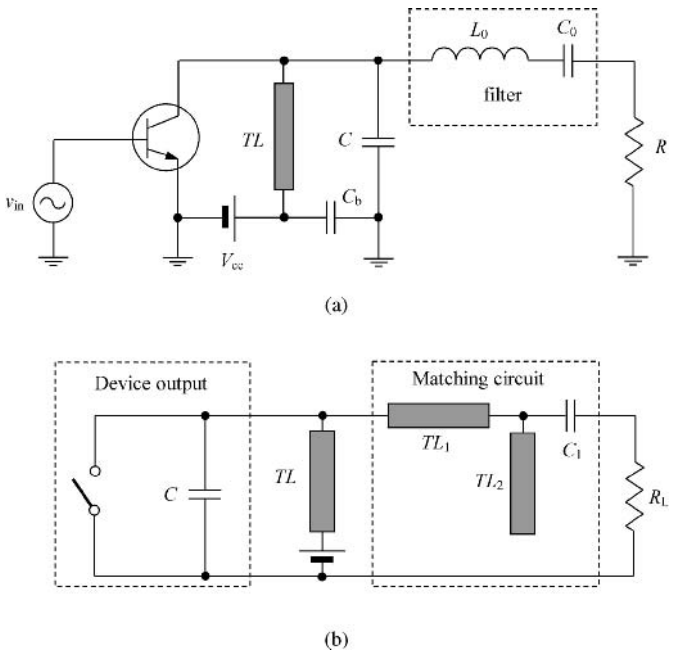


Figure 7.39 Schematics of parallel-circuit Class E power amplifier with transmission line.

As a result, using Eq. (7.79) to determine the parallel inductance L for optimum switched-mode operation, the ratio between the transmission line parameters and the load resistance for idealized 50 percent duty cycle switched-mode operation can be obtained by [22]

$$\tan\theta = 0.732\frac{R}{Z_0} \tag{7.90}$$

In a practical circuit, the L_0C_0-filter should be replaced by the output matching circuit, the input impedance of which needs to be sufficiently high at the harmonics. This means that, for the T-type matching circuit shown in Fig. 7.39(b), the length of the parallel open-circuited stub TL_2 should be chosen as 45° to realize a short circuit condition for the second harmonic across the load. Then, the values of the characteristic impedances and the electrical lengths of all transmission lines using Eq. (7.90) are analytically calculated to provide the required inductive impedance at the fundamental and capacitive reactance at the second harmonic. However, to simplify the matching procedure, it is easier to simply realize the conjugate matching with the load using the transmission-line output matching circuit, whereas the length of the parallel transmission line is chosen to realize the required phase angle for the given device output capacitance.

Another possible transmission-line load network—shown in Fig. 7.40(a)—was developed for a monolithic cellular handset power

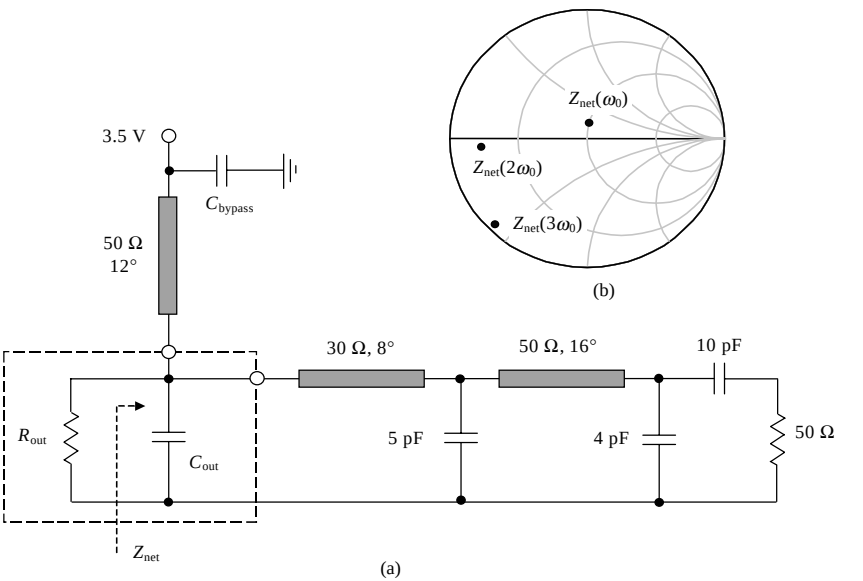


Figure 7.40 Schematics of parallel-circuit Class E power amplifier with transmission line.

amplifier, and includes a series transmission line with parallel capacitances. However, because of the finite electrical length of the transmission line, it is impossible to realize simultaneously the required inductive impedance at the fundamental with the purely capacitive reactance at the higher-order harmonics. For example, at the second harmonic, the real part of the load network input impedance is too high, as shown in Fig. 7.40(*b*). However, even for this approximation the results of circuit simulation for the handset two-stage InGaP/GaAs HBT power amplifier demonstrates a collector efficiency of 71 percent, power-added efficiency of 61 percent at a frequency of 1.75 GHz with a supply voltage $V_{cc} = 3.5$ V and output power of $P_{out} = 34$ dBm [17].

These transmission-line load networks cannot provide 100 percent efficiency, even ideally, as the optimum conditions are realized only for the fundamental and a few higher-order harmonic components. Therefore, a special case is a load network with a quarterwave transmission line, when the lossless dc-to-RF power transformation can be realized for particular values of the load network parameters. In practice, the idealized rectangular collector voltage and half-sinusoidal current waveforms corresponding to Class F operation, provided by using a quarterwave transmission line in the load network, can be realized at low frequencies when the effect of the device collector capacitance is negligibly small. At higher frequencies, the effect of the device collector capacitance contributes to a finite switching time, which results in the time periods when the collector voltage and collector current exist at the same time, i.e., $v > 0$ and $i > 0$ simultaneously. As a result, such a load network with the quarterwave transmission line and shunt capacitance cannot provide the switched-mode operation with an instantaneous transition from the device pinch-off mode to saturation mode and vice versa. Therefore, during a finite time interval, the device operates in the active region as a current source with a reverse-biased collector-base junction and the collector current is provided by this current source.

However, the collector efficiency can be increased, and the effect of the collector capacitance can be compensated, by including a series inductance between the shunt capacitance and quarterwave transmission line, realizing Class E operation conditions. The possibility of including a quarterwave transmission line into the Class E load network (see Fig. 7.29) instead of an RF choke was first considered in [23]. However, such a location for a quarterwave transmission line with a straight connection to the device collector violates the required capacitive reactance conditions at even harmonics by providing simply their shortening. As a result, an optimum Class E operation mode—when the shapes of the collector current and voltage waveforms provide a condition at which the high current and high voltage do not overlap simultaneously—cannot

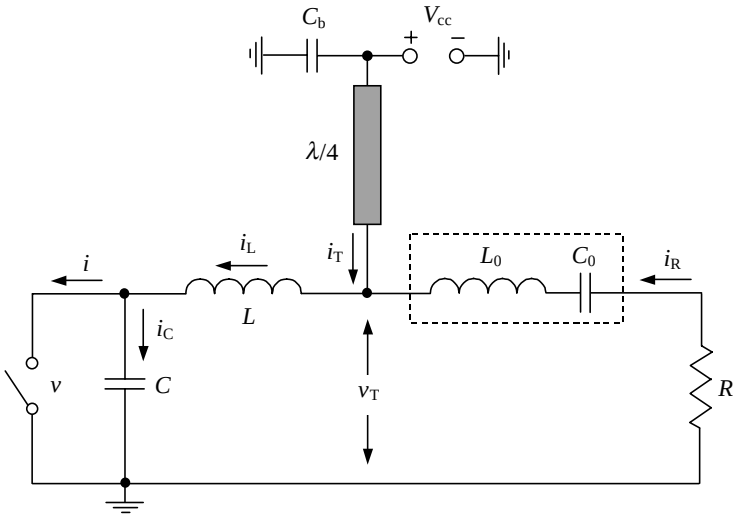


Figure 7.41 Equivalent circuit of Class E power amplifier with quarterwave transmission line.

be realized. Moreover, the larger the value of the shunt capacitance, the smaller the collector efficiency that can be achieved.

Consider the idealized Class E load network with a shunt capacitance where a quarterwave transmission line is connected between the series inductance and the fundamentally tuned series L_0C_0-circuit, as shown in Fig. 7.41. Let the output current flowing into the load be sinusoidal given by Eq. (7.39) where the phase shift φ is due to the shunt capacitance and series inductance.

When the switch is on for $0 \leq \omega t < \pi$, the current flowing through the shunt capacitance $i_C(\omega t) = 0$ and, consequently,

$$i(\omega t) = i_L(\omega t) = i_T(\omega t) + i_R(\omega t) \tag{7.91}$$

When the switch is off for $\pi \leq \omega t < 2\pi$, there is no current flowing through the switch, i.e., $i(\omega t) = 0$, and the current flowing through the shunt capacitance C is

$$i_C(\omega t) = i_L(\omega t) = i_T(\omega t) + i_R(\omega t) \tag{7.92}$$

Using Eqs. (2.58) and (7.39) for currents flowing into the transmission line and load, an important expression can be derived from Eqs. (7.91) and (7.92):

$$i_L(\omega t) - i_L(\omega t + \pi) = 2i_R(\omega t) \tag{7.93}$$

The current $i_L(\omega t + \pi)$ can be expressed through the voltages v_T and $v_L(\omega t) = \omega L \frac{di_L(\omega t)}{d(\omega t)}$ as

$$i_L(\omega t + \pi) = \omega C \frac{d}{d(\omega t)} \left[v_T(\omega t + \pi) - \omega L \frac{di_L(\omega t + \pi)}{d(\omega t)} \right] \tag{7.94}$$

Hence, using Eq. (2.57) for the switch-on condition when it yields

$$v_T(\omega t + \pi) = 2V_{cc} - \omega L \frac{di_L(\omega t)}{d(\omega \mathrm{t})} \tag{7.95}$$

the resulting second-order differential equation can be obtained from Eqs. (7.93) and (7.94) when switch is turned off for $\pi \leq \omega t < 2\pi$ and $i_L = i_C$:

$$\frac{d^2 i_C(\omega t)}{d(\omega t)^2} + \frac{q^2}{2} i_C(\omega t) + I_R \sin(\omega t + \varphi) = 0 \tag{7.96}$$

the general solution for which can be obtained in the form of

$$i_C(\omega t) = C_1 \cos\left(\frac{q}{\sqrt{2}} \omega t \right) + C_2 \sin\left(\frac{q}{\sqrt{2}} \omega t \right) + \frac{2I_R}{2 - q^2} \sin(\omega t + \varphi) \tag{7.97}$$

where $q = 1/\omega\sqrt{LC}$ and the coefficients C_1 and C_2 are calculated using the following initial off-state conditions:

$$i_C(\omega t)|_{\omega t = \pi} = 2i_R(\pi) \tag{7.98}$$

$$\left. \frac{di_C(\omega t)}{d(\omega t)} \right|_{\omega t = \pi} = \frac{V_{cc}}{\omega L} - I_R \cos(\varphi) \tag{7.99}$$

The voltage across the switch during off-state operation is produced by the charging of the shunt capacitance C according to

$$v(\omega t) = \frac{1}{\omega C} \int_{\pi}^{\omega t} i_C(\omega t) d\omega t \tag{7.100}$$

As a result, the three unknown parameters q, $p = \omega L I_R / V_{cc}$ and φ can be found from Eq. (7.100) using Eq. (7.97), the two optimum conditions given by Eqs. (7.37) and (7.38) and an additional equation defining the supply voltage V_{cc} from Fourier-series expansion as

$$q = 1.649 \tag{7.101}$$

$$p = 1.302 \tag{7.102}$$

$$\varphi = -40.8^\circ \tag{7.103}$$

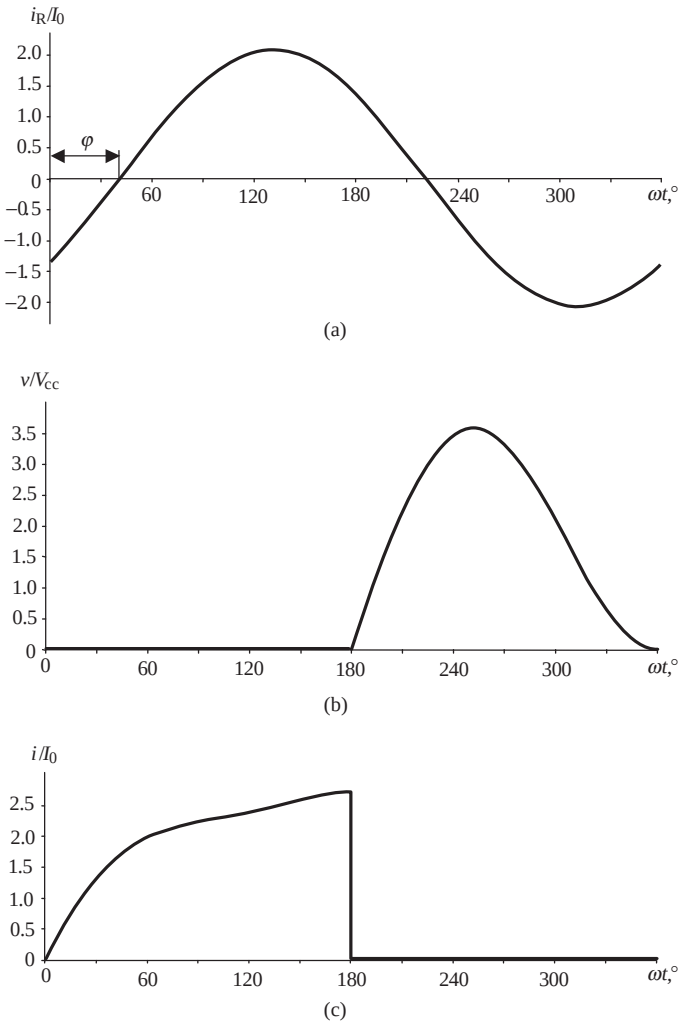


Figure 7.42 Voltage and current waveforms of a Class E power amplifier with quarterwave transmission line.

Figure 7.42 shows the normalized (*a*) load current, (*b*) collector voltage and (*c*) current waveforms for idealized optimum Class E mode with a quarterwave transmission line. From the collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch and the current i—consisting of the load sinusoidal current and transmission line current (see Fig. 7.43(*b*))—flows through the switch. However, when the transistor is turned off, this current flows through the shunt capacitance C (see Fig. 7.43(*a*)).

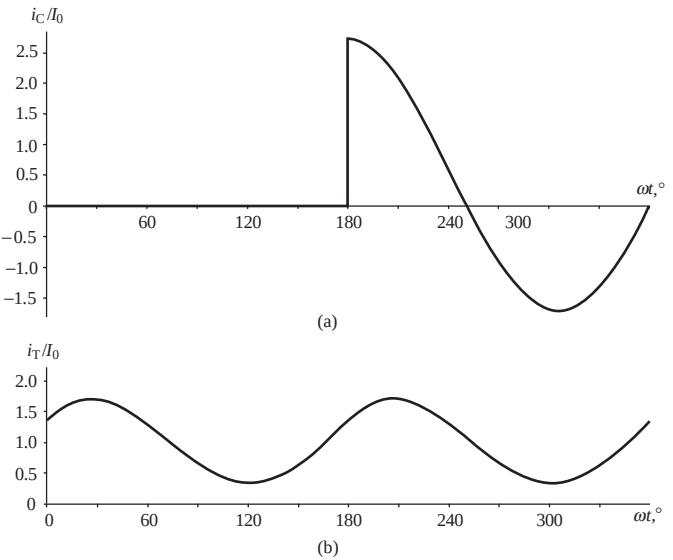


Figure 7.43 Current waveforms of a Class E power amplifier with quarterwave transmission line.

The optimum series inductance L, shunt capacitance C and load resistance R can be obtained by

$$L = 1.349\frac{R}{\omega} \tag{7.104}$$

$$C = \frac{0.2725}{\omega R} \tag{7.105}$$

$$R = 0.465\frac{V_{cc}^2}{P_{out}} \tag{7.106}$$

The peak collector current I_s, peak collector voltage V_s and maximum operation frequency f_{max} can be determined directly from numerical calculation and Eq. (7.105), respectively, giving

$$I_s = 2.714I_0 \tag{7.107}$$

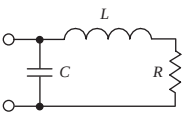
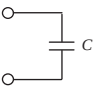
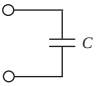
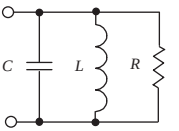
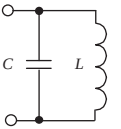
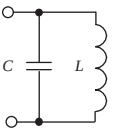
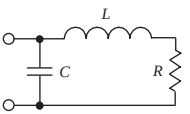
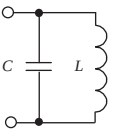
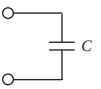
$$V_s = 3.589V_{cc} \tag{7.108}$$

$$f_{max} = 0.093\frac{P_{out}}{C_{out}V_{cc}^2} \tag{7.109}$$

which is 1.63 times higher than maximum operation frequency for the optimum Class E power amplifier with a shunt capacitance [19].

In Table 7.2, the optimum impedances seen from the device collector at the fundamental and higher-order harmonic components are

TABLE 7.2 Optimum Impedances at Fundamental and Harmonics for Different Class E Load Networks

Class E load network	f_0 (fundamental)	$2nf_0$ (even harmonics)	$(2n+1)f_0$ (odd harmonics)
Class E with shunt capacitance			
Class E with parallel circuit			
Class E with quarterwave transmission line			

illustrated by the appropriate circuit configurations. It can be seen that Class E mode with a quarterwave transmission line shows different impedance properties at even and odd harmonics. At odd harmonics, the optimum impedances can be established by the shunt capacitance as it is required for all harmonics in Class E with a shunt capacitance. At even harmonics, the optimum impedances are realized using a parallel *LC*-circuit as it is required for all harmonics in Class E with a parallel circuit. Thus, the frequency properties of a grounded quarterwave transmission line with its open-circuit conditions at odd harmonics and short-circuit conditions at even harmonics allow Class E with a quarterwave transmission line to combine simultaneously the harmonic impedance conditions typical for both Class E with a shunt capacitance and Class E with a parallel circuit.

The theoretical results obtained for Class E mode with a quarterwave transmission line show that it is enough to use a very simple load network to realize the optimum impedance conditions even for four harmonics. In this case, as the shunt capacitance C and series inductance L provide optimum inductive impedance at the fundamental, and the quarterwave transmission line realizes the shortening of even harmonics, it is only necessary to provide an open-circuit condition at the third harmonic component. In addition, as follows from Fig. 7.43(*b*), the current flowing into the transmission line is very closed to the sinusoidal second harmonic current, which means that the level of fourth and higher-order harmonics is negligible because of the significant shunting effect of the capacitance C. Consequently, when the ideal series

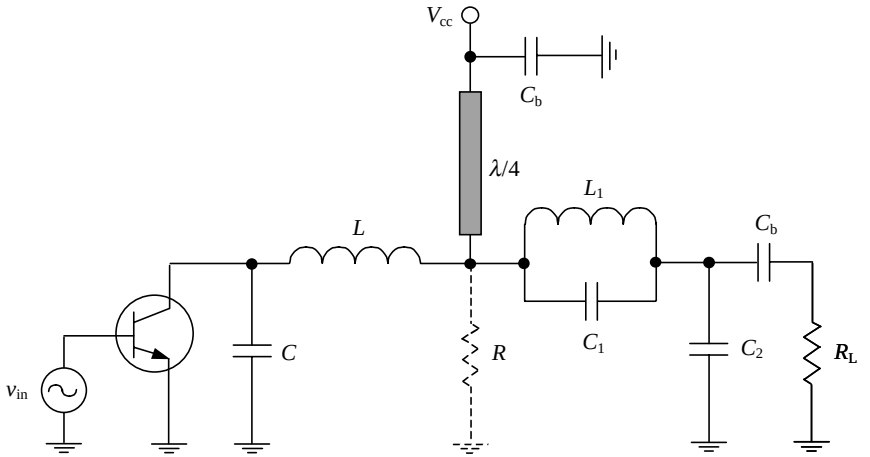


Figure 7.44 Schematic of Class E power amplifier with lumped load network.

L_0C_0-circuit is replaced by the output matching circuit, the optimum impedance conditions for Class E load network with a quarterwave transmission line can be practically fully realized by simply providing an open-circuit condition at the third harmonic component.

Figure 7.44 shows the circuit schematic of a lumped Class E power amplifier with a quarterwave transmission line, where the parallel resonant L_1C_1-circuit tuned on the third harmonic is used and C_b is the blocking capacitance. Since at the fundamental the reactance of this circuit is inductive, it is enough to use the shunt capacitance C_2 to compose the L-type matching circuit that provides the required impedance matching of optimum Class E load resistance R with the standard load impedance of $R_L = 50\ \Omega$. To calculate the parameters of the circuit elements, consider the loaded quality factor $Q_L = \omega C_2 R_L$, which also can be written as

$$Q_L = \sqrt{\left(\frac{R_L}{R}\right) - 1} \tag{7.110}$$

As a result, the matching circuit parameters can be calculated from

$$C_2 = \frac{Q_L}{\omega R_L} \tag{7.111}$$

$$L_1 = \frac{8}{9}\frac{Q_L R}{\omega} \tag{7.112}$$

$$C_1 = \frac{1}{9\omega^2 L_1} \tag{7.113}$$

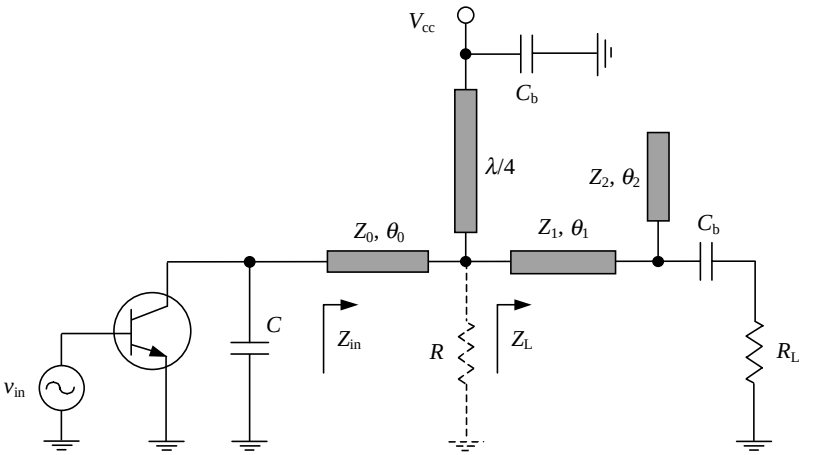


Figure 7.45 Schematic of a transmission-line Class E power amplifier.

At microwaves, the series lumped inductance L should be replaced by the short-length series transmission line. In this case, when the shunt capacitance C represents a fully internal active device output capacitance, the bondwire and lead inductances can also be taken into account, to provide the required inductive reactance and make the series transmission line shorter. Figure 7.45 shows the circuit schematic of a transmission-line Class E power amplifier with a quarterwave transmission line.

Usually the transmission line characteristic impedance Z_0 (in most cases equal to 50 Ω) is much higher than the required optimum load network resistance R. Consequently, the input impedance of the series transmission line with characteristic impedance Z_0 and electrical length θ_0 under the condition of $(R\tan\theta_0/Z_0) \ll 1$, and having a sufficiently short transmission line with an electrical length of less than 45°, is determined by

$$Z_{\text{in}} = Z_0\frac{R + jZ_0\tan\theta_0}{Z_0 + jR\tan\theta_0} = Z_0\frac{\frac{R}{Z_0} + j\tan\theta_0}{1 + j\frac{R}{Z_0}\tan\theta_0} \cong R + jZ_0\tan\theta_0 \quad (7.114)$$

Using Eq. (7.114), the required optimum value of θ_0 for Class E mode using Eq. (7.104) is obtained from

$$\theta_0 = \tan^{-1}\left(1.349\frac{R}{Z_0}\right) \quad (7.115)$$

The output matching circuit is necessary to match the required optimum resistance R calculated in accordance with Eq. (7.106) to the 50 Ω load and also to provide an open-circuit condition at the third harmonic component. This can be easily done using the output matching

topology in the form of an L-type transformer with a series transmission line and open-circuit stub. In this case, the electrical lengths of the series transmission line and open-circuit stub should be chosen to be 30° each. The load impedance Z_L seen by a quarterwave transmission line can be written by

$$Z_L = Z_1 \frac{R_L(Z_2 - Z_1 \tan^2\theta) + jZ_1Z_2 \tan\theta}{Z_1Z_2 + j(Z_1 + Z_2)R_L \tan\theta} \tag{7.116}$$

where $\theta = \theta_1 = \theta_2 = 30^\circ$, Z_1 and θ_1 are the characteristic impedance and electrical length of the series transmission line, and Z_2 and θ_2 are the characteristic impedance and electrical length of the open-circuit stub.

Hence, the conjugate matching with the load can be provided by proper choice of the characteristic impedances Z_1 and Z_2. Separating Eq. (7.116) into real and imaginary parts, the following system of two equations with two unknown parameters is obtained:

$$\begin{cases} Z_1^2Z_2^2 - R_L^2(Z_1 + Z_2)(Z_2 - Z_1 \tan^2\theta) = 0 \\ (Z_1 + Z_2)^2R_L^2R \tan^2\theta - Z_1^2Z_2^2[R_L(1 + \tan^2\theta) - R] = 0 \end{cases} \tag{7.117}$$

which allows calculation of the characteristic impedances Z_1 and Z_2. This system of two equations can be explicitly solved as a function of the parameter $r = R_L/R$ resulting in

$$\frac{Z_1}{R_L} = \frac{\sqrt{4r - 3}}{r} \tag{7.118}$$

$$\frac{Z_1}{Z_2} = 3\left(\frac{r - 1}{r}\right) \tag{7.119}$$

Consequently, for the specified value of the parameter r with the required Class E optimum load resistance R and standard load $R_L = 50\ \Omega$, the characteristic impedance Z_1 is calculated from Eq. (7.118) and the characteristic impedance Z_2 is calculated from Eq. (7.119). For example, if the required optimum load resistance is equal to $R = 12.5\ \Omega$ resulting in $r = 4$, the characteristic impedance of the series transmission line is equal to $Z_1 = 45\ \Omega$ and the characteristic impedance of the open-circuit stub is equal to $Z_2 = 20\ \Omega$.

Unlike the transmission-line Class E load networks shown in Fig. 7.41(b) with two-harmonic control [20] and in Fig. 7.41(c) with three-harmonic control [21], the Class E load network with a quarterwave transmission line, which can provide the optimum impedance conditions for at least four harmonics, is very simple in circuit implementation and doesn't require an additional lumped RF choke element. In addition, there is no need to use the special computer simulation

tools required to calculate the parameters of the existing Class E transmission-line load-network topologies [21, 24, 25], since all parameters of the Class E load network with a quarterwave transmission line, as well as the output matching circuit parameters, are easily calculated explicitly from simple analytical equations. Besides, such a Class E load network with a quarterwave transmission line is very useful in practical design providing simultaneously significant higher-order harmonic suppression.

Broadband Class E Circuit Design

The conventional design of a high-efficiency switched-mode tuned Class E power amplifier requires a high Q_L-factor to satisfy the necessary harmonic impedance conditions at the output device terminal. However, if a sufficiently small value of the quality factor Q_L can be chosen, a high-efficiency broadband operation of the Class E power amplifier can be realized. For example, a simple network consisting of a series resonant LC-circuit tuned to the fundamental and a parallel inductance provides a constant load phase angle of 50° in a frequency range of about 50 percent [26]. For the first time, such a reactance compensation technique using single-resonant circuit has been applied to the varactor tuned Gunn oscillator and parametric amplifier [27]. Moreover, it is possible to increase the tuning range of an oscillator by adding more stages of reactance compensation. So, for circuit having a 50 Ω load, an improvement of 4 percent in the tuning range can theoretically be achieved as a result of applying double-resonant circuit reactance compensation, whereas for a circuit operating into 100 Ω load the increase in tuning range is 17 percent [28]. This reactance compensation circuit technique can also be applied to microwave transistor amplifier design because the input and output transistor impedances generally are simulated by series or shunt RLC-circuits. For compensating the reactive part and transforming the active part of the output transistor impedance to the conventional load impedance, quarter- or half-wavelength transmission lines can be used successfully. Transmission-line matching technique achieves for GaAs MESFET amplifiers a frequency range of 3.7 to 4.2 GHz with a gain ripple in limits of ± 0.1 dB and return loss of about 20 dB [29].

Computer-aided design of broadband microwave transistor amplifiers normally requires considerable time and can be quite tedious. Therefore the analytical approach, which can define common regularities and express in explicit and simple form the ratios between circuit elements, can be useful in substantially reducing the calculation required. Combined with this analytical approach, computer optimization technique yields the fastest and most accurate results.

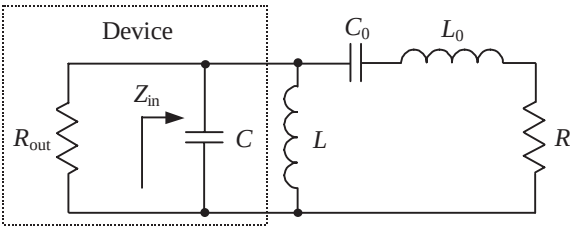


Figure 7.46 Single reactance compensation circuit.

The reactance compensation circuit technique will be demonstrated using the simplified equivalent load network with a series resonant L_0C_0-circuit tuned on the fundamental and a shunt LC-circuit providing a constant load phase angle relative to the device output terminals, as shown in Fig. 7.46. The reactances of the series and shunt resonant circuits vary with frequency, increasing in the case of the series circuit and reducing in the case of the loaded parallel circuit near the resonant frequency ω_0, as shown in Fig. 7.47 by curve 1 and curve 2, respectively. Near the resonant frequency ω_0 of the series circuit with positive slope of its reactance, the slope of the shunt circuit reactance is negative. This reduces the overall reactance slope of the load network (dotted line). With a proper choice of the circuit elements, a constant load angle over a very large frequency bandwidth is established.

This technique can be easily applied to the switched-mode Class E power amplifier with a parallel circuit because its circuit configuration is exactly the same. The parallel circuit configuration is directly applied

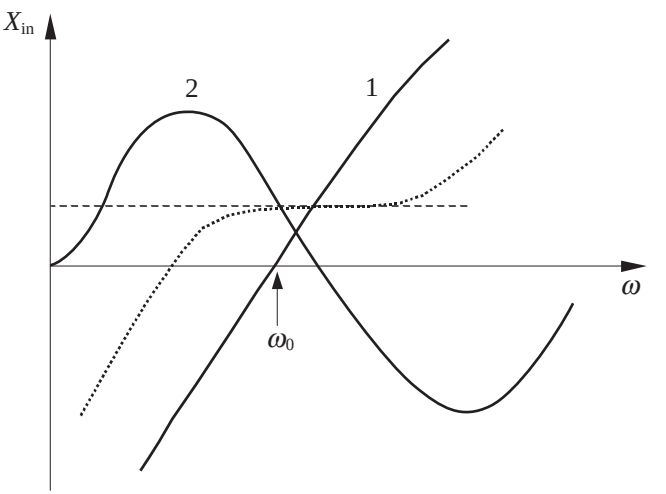


Figure 7.47 Reactance compensation principle.

for broadband operation conditions, unlike the Class E circuit configuration with shunt capacitance and series inductance. In this case, the optimum phase angle ϕ and load resistance R of the load network can be obtained from Eqs. (7.75) and (7.81), respectively.

The load network input admittance $Y_{\text{in}} = 1/Z_{\text{in}}$ can be written by

$$Y_{\text{in}} = \left(j\omega C + \frac{1}{j\omega L} + \frac{1}{R + j\omega' L_0} \right) \tag{7.120}$$

where $\omega' = \omega(1 - \frac{\omega_0^2}{\omega^2})$, and $\omega_0 = 1/\sqrt{L_0 C_0}$ is the resonant frequency.

At the resonant frequency the normalized input admittance can be rewritten by

$$Y_{\text{in}} = \left(j\omega C + \frac{1}{j\omega L} + \frac{1}{R} \right) \tag{7.121}$$

The parallel inductance L and capacitance C required for optimum switched-mode operation are calculated as the functions of the load resistance R and frequency ω from Eqs. (7.79) and (7.80), respectively. The parameters of the series resonant L_0C_0-circuit must be chosen to provide a constant phase angle of the load network over broadband frequency bandwidth.

The frequency bandwidth will be maximized if at resonant frequency ω_0

$$\left. \frac{dB(\omega)}{d\omega} \right|_{\omega=\omega_0} = 0 \tag{7.122}$$

where $B(\omega) = \text{Im}Y_{\text{in}} = -(1 - \omega^2 LC)/\omega L$ is the load network susceptance. In this case, the concept of the susceptance compensation technique, which is similar to the reactance compensation technique, is used to simplify the calculation. An additional equation can be written:

$$C + \frac{1}{\omega^2 L} - \frac{2L_0}{R^2} = 0 \tag{7.123}$$

As a result, the series capacitance C_0 and inductance L_0 can be calculated by

$$L_0 = 1.026\frac{R}{\omega} \tag{7.124}$$

$$C_0 = 1/\omega^2 L_0 \tag{7.125}$$

Wider frequency bandwidth can be achieved using the double-resonant reactance compensation circuit shown in Fig. 7.48, where L_0C_0 and L_1C_1 are the series and parallel resonant circuit, respectively.

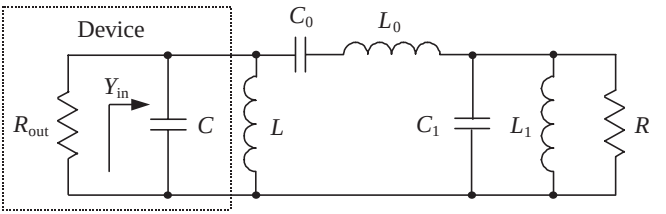


Figure 7.48 Double reactance compensation circuit.

In this case, a system of two equations can be solved according to

$$\left.\frac{dB}{d\omega}\right|_{\omega=\omega_0} = \left.\frac{d^3B}{d\omega^3}\right|_{\omega=\omega_0} = 0 \tag{7.126}$$

as the second derivative cannot provide an appropriate analytical expression.

To determine the circuit parameters for double-resonant circuit reactance compensation with overall circuit susceptance given by

$$B(\omega') = \omega C - \frac{1}{\omega L} + \omega' \frac{C_1 R^2 [1 - (\omega')^2 L_0 C_1] - L_0}{R^2 [1 - (\omega')^2 L_0 C_1]^2 + (\omega' L_0)^2} \tag{7.127}$$

it is necessary to solve simultaneously the following two equations:

$$C + \frac{1}{\omega^2 L} - 2\frac{C_1 R^2 - L_0}{R^2} = 0 \tag{7.128}$$

$$\frac{1}{\omega^2 L} + \frac{C_1 R^2 - L_0}{R^2} - 8\omega^2 L_0 \left[C_1^2 + \frac{(C_1 R^2 - L_0)(L_0 - 2C_1 R^2)}{R^4} \right] = 0 \tag{7.129}$$

As a result, the parameters of the series and shunt resonant circuits with quality factors $Q_0 = \omega L_0/R$ and $Q_1 = \omega C_1 R$ close to unity and greater—as a starting point for circuit optimization—can be calculated from

$$L_0 = \frac{R}{\omega}\frac{2}{\sqrt{5}-1} \qquad C_0 = \frac{1}{\omega^2 L_0} \tag{7.130}$$

$$C_1 = \frac{L_0}{R^2}\frac{3-\sqrt{5}}{2} \qquad L_1 = \frac{1}{\omega^2 C_1} \tag{7.131}$$

The circuit simulation for these two types of reactance compensation load networks was performed at resonant frequency $f_0 = 150$ MHz for load $R = 50\ \Omega$. In Fig. 7.49, the frequency dependencies of the load network phase angle ϕ for the single reactance (curve 1) and double

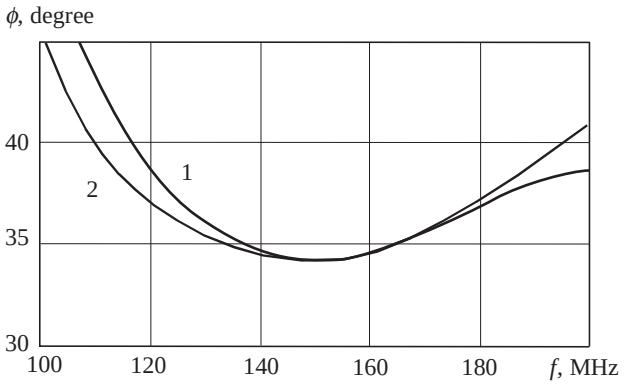


Figure 7.49 Reactance compensation load network broadband performance.

reactance (curve 2) compensation circuits are plotted. It is apparent that the reactance compensation technique realizes the very broadband operation conditions. Using just a single reactance load network yields a significant widening of the operating frequency bandwidth with minimum deviation of the magnitude and phase of load network input impedance. A double reactance compensation load network obtains maximum deviation from the optimum value of about 34° by only 3° in a frequency range of 120 to 180 MHz.

To achieve the high efficiency broadband operation mode with high power gain, it is best to design the power amplifier based on LDMOS transistors. It is easy to provide a very broadband input matching using a lossy matching circuit, especially at frequencies about ten times lower than the device transition frequency f_T. For example, using a high voltage LDMOSFET device for a Class E power amplifier a drain efficiency of 88 percent at 144 MHz with an output power level of 14 W was achieved with high-Q inductor in the output series resonant circuit [30]. In Fig. 7.50, the schematic of the LDMOSFET power amplifier, designed for operation in a frequency bandwidth of 100 to 200 MHz and using a double resonant load network, is shown. The input matching circuit includes a simple L-transformer connected in parallel to a series circuit with the inductance and 50 Ω resistance. This provides a minimum return loss at 200 MHz of about 15 dB and $VSWR$ less than 1.4 over all frequency bandwidth. Figure 7.51 shows that, for such an octave-band power amplifier with the input power of 1 W, the power gain of 10 dB with deviation of only ±0.5 dB (curve 2) can be achieved with a drain efficiency of about 70 percent and higher (curve 1).

An analysis of the drain voltage and current waveforms at the center bandwidth frequency of 150 MHz, shown in Fig. 7.52, demonstrates that

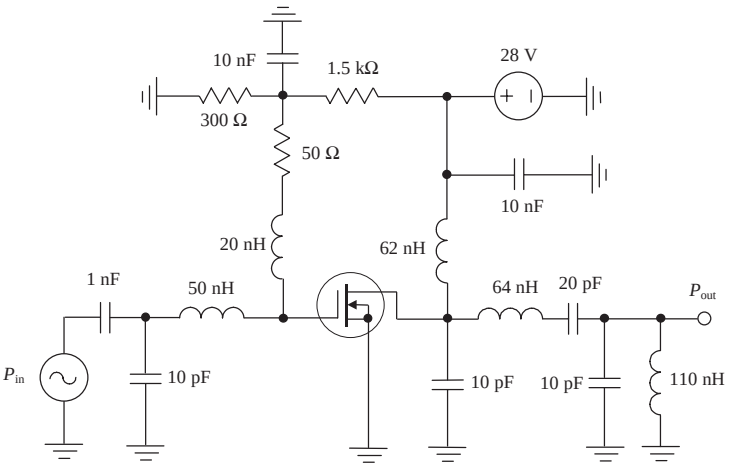


Figure 7.50 Simulated broadband switched-mode LDMOSFET power amplifier.

the operating broadband mode is very close to optimum parallel-circuit Class E operation mode, although the impedance conditions at higher harmonics are not controlled properly. As seen from the plot, when the transistor is turned on, there is practically no voltage when the drain current achieves its maximum value. On the other hand, when the transistor is turned off, the drain current continues to flow, but instead through the device drain-source capacitance C_{ds}.

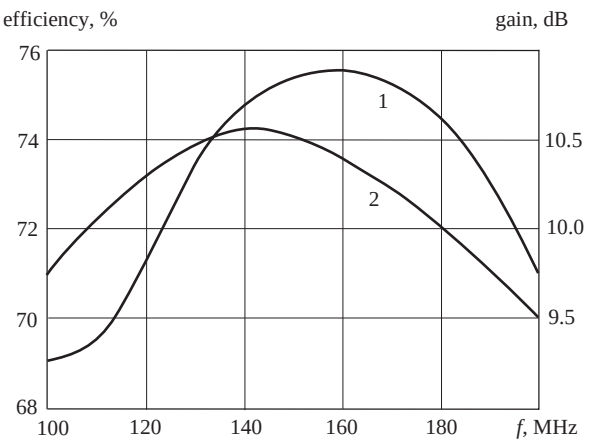


Figure 7.51 Broadband switched-mode LDMOSFET power amplifier performance.

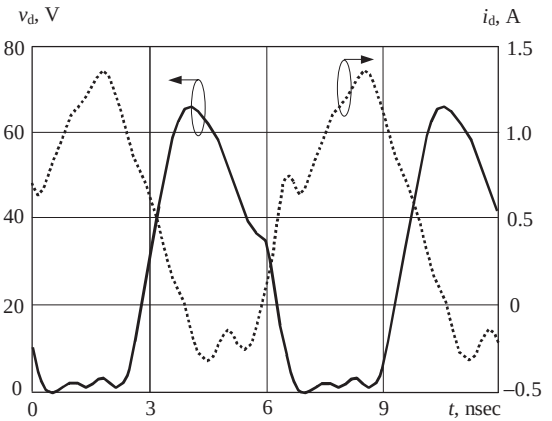


Figure 7.52 Drain voltage and current waveforms.

Practical High-Efficiency RF and Microwave Power Amplifiers

Figure 7.53 shows a typical VHF high-efficiency bipolar power amplifier that can provide output power of about 10 W with power-added efficiency of about 60 percent in a zero-bias Class C operation. Using T-type output matching transformer with the series inductance creates high impedance conditions for the second and higher-order harmonic components at the collector terminal, thereby improving the collector efficiency. In this case, the collector current waveform is close to sinusoidal, whereas the collector voltage waveform is characterized by a high value in the peak factor. To provide a reliable transistor operation when the maximum collector voltage amplitude should be less than

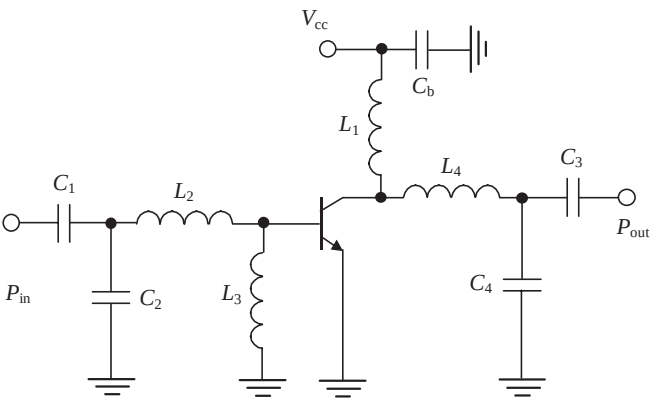


Figure 7.53 Typical VHF high-efficiency bipolar power amplifier.

the collector-emitter breakdown voltage, it is necessary to reduce the collector supply voltage. Due to the small value of the transistor input impedance of about 1 Ω, the frequency bandwidth of such an amplifier is sufficiently narrow and does not exceed several percents at the −3-dB output power level. The inductance L_3 is required to provide zero base-emitter biasing, whereas the inductance L_1 is necessary to protect the dc power supply from the RF signal. Their values are sufficiently large to influence the amplifier matching conditions. So, for example, such an amplifier in slightly overdriven Class B operation can provide 10-W output power with a power gain of 8 dB and a power-added efficiency close to 70 percent at an operating frequency of 250 MHz [1].

However, to improve the power amplifier reliability by reducing a peak factor to a theoretical maximum value of 2, it is best to use the quarterwave transmission line instead of the RF choke. This method realizes short circuit conditions for even collector voltage harmonics, resulting in the square voltage and half-sinusoidal current waveform approximations typical for Class F operation mode. To increase the impedance conditions for higher harmonic components, use the series high-Q resonant circuit tuned to the fundamental together with an output matching circuit. The typical electrical schematic of such a high-efficiency Class F VHF power amplifier is shown in Fig. 7.54. This design offers the possibility of achieving a collector efficiency approaching 90 percent for a 10-W hybrid power amplifier at 250 MHz.

A Class F operation mode can also be realized with a monolithic power amplifier design. Figure 7.55 shows a circuit configuration for a 1 W one-chip GaAs MESFET power amplifier that operates at the low supply voltage of 3.3 V in a frequency range of 925 to 990 MHz [31]. To increase power amplifier drain efficiency, the drain bias circuit

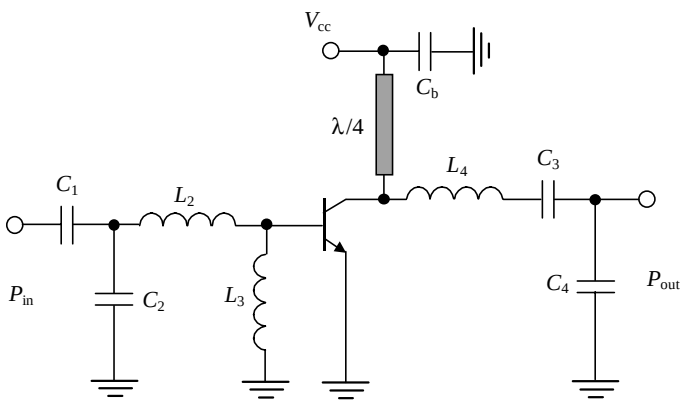


Figure 7.54 High-efficiency Class F VHF power amplifier with transmission line.

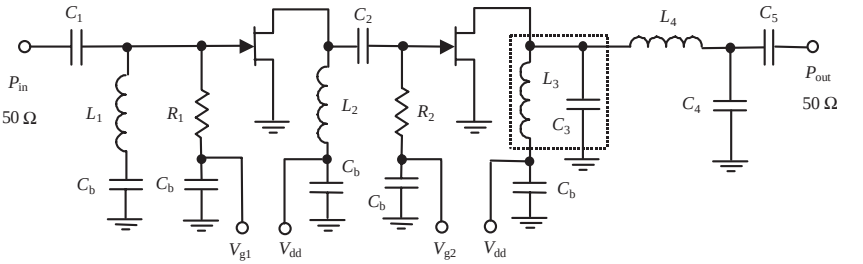


Figure 7.55 Monolithic Class F power amplifier with second harmonic control.

is realized in the form of the parallel resonant circuit (dotted box). This provides the required reflection coefficient for the second harmonic and also achieves high impedance at the fundamental frequency. Simple *L*- and *T*-transformers are used as input, interstage and output matching circuits, respectively. Using a resistor with low value in the interstage matching circuit contributes to a stable operation condition. To minimize the chip size, all circuit elements are lumped elements consisting of spiral inductors, metal-insulator-metal (MIM) capacitors and epitaxial layered resistors. The spiral inductors in the output circuit are 100 μm wide and 9 μm thick to reduce dc and RF losses. As a result, using a MESFET device for the second stage with geometry of 0.5 μm $\times$7.56 mm achieves a power-added efficiency of 43 percent with chip size of 2.5 mm $\times$3.48 mm.

However, a hybrid or multichip power amplifier achieves substantially higher efficiency than a monolithic one because using a microstrip line may provide minimal dc and RF losses. The simplified circuit topology of a microstrip two-stage 900 MHz band GaAs MESFET power amplifier is shown in Fig. 7.56 [32]. The microstrip line between the MESFET and open-circuit stub of $\lambda_2/4$ electrical length, where λ_2 is a second harmonic wavelength, is a compensation line for the equivalent device output reactance. The *T*-transformer—which consists of the series microstrip line, open-circuit microstrip stub and series capacitance—provides an output matching with load. The input and

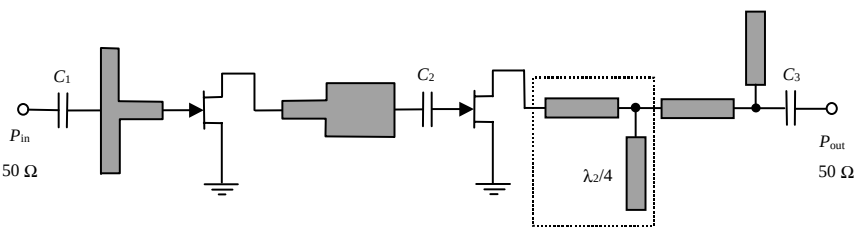


Figure 7.56 Simplified schematic of microstrip Class F power amplifier.

interstage matching circuits at the fundamental frequency were designed using microstrip lines. As a result, with second harmonic control by series microstrip line and microstrip stub (dotted box), such a power amplifier demonstrates a drain efficiency of more than 80 percent, power-added efficiency of 71 percent and output power of 2 W at the supply voltage of 6 V.

One of the most important factors for high-efficiency operation mode is the value of the device saturation resistance r_{sat} (or on-resistance r_{on}), especially for low supply voltage. Here, r_{on} is the ratio of the drain-source voltage at the saturated drain current to the saturated drain current itself. It is difficult to improve the efficiency of a small-scale MESFET with a narrow gate width when, in low voltage operation, the ratio r_{on}/R_{out} (where R_{out} is the device output resistance) is not small enough. To realize a high-efficiency operation mode for the power amplifier, this ratio must be increased as much as possible. So, by decreasing r_{on} by half, the efficiency can be improved by about 10 percent. A MESFET, which has an on-resistance r_{on} of about 1 Ω, can demonstrate a drain efficiency of 90 percent at a supply voltage of 6 V in a 900-MHz frequency bandwidth in Class F power amplifiers [32].

By inputting a quasisquare voltage wave into the MESFET gate, the efficiency of the Class F power amplifier can be increased. This quasisquare gate voltage contributes to the reduction of the voltage/current switching time at the drain and reduces power dissipation. Dissipation occurs when the drain voltage and current exist simultaneously. Figure 7.57 shows the circuit diagram of a single-stage power amplifier with optimally terminated source and drain second harmonic

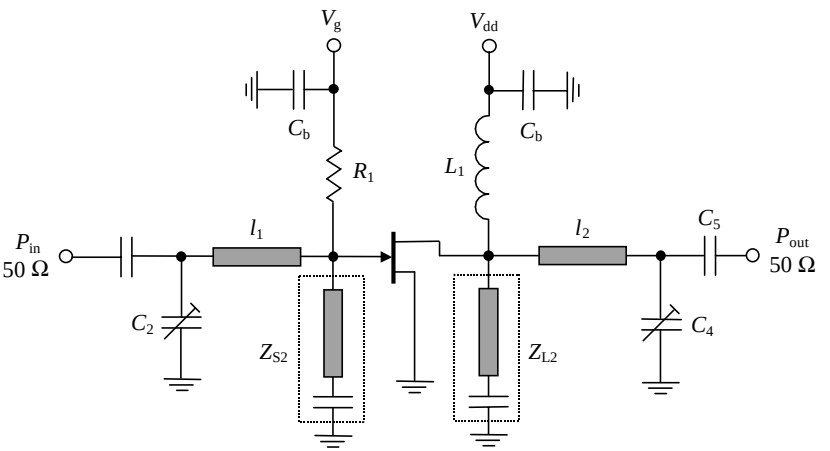


Figure 7.57 Circuit diagram of Class F power amplifier with optimally terminated source and drain second harmonic impedances.

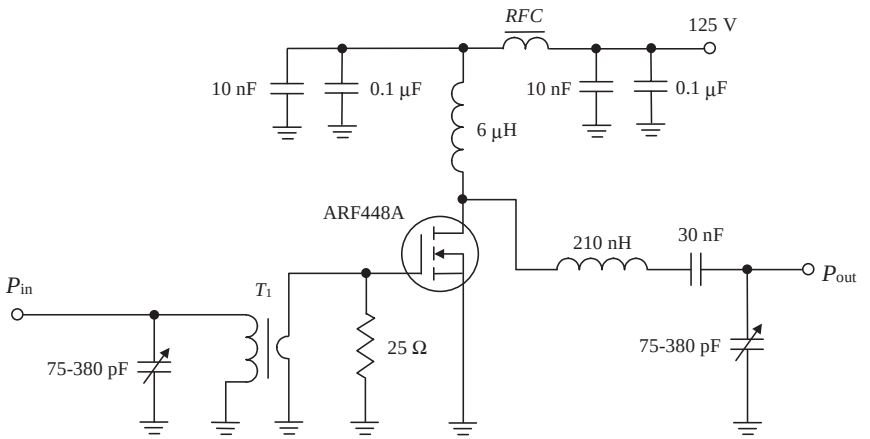


Figure 7.58 High-power Class E MOSFET power amplifier [34].

impedances Z_{S2} and Z_{L2}, each of which is provided by a series 50-Ω microstrip line and a shunt capacitor [33]. This approach achieves power-added efficiency of 74 percent with output power of 31.4 dBm (1.4 W) at the operating frequency of 930 MHz and supply voltage of 3.5 V using a GaAs MESFET device of 12-mm gate width. In this case, applying the input second harmonic control circuit improves the power-added efficiency by 5 percent.

High output power can be achieved in Class E operation by using high voltage MOSFET devices. Such an amplifier, with 500 W output power and 83 percent efficiency for the operating frequency of 27.12 MHz, is shown in Fig. 7.58 [34]. The input ferrite transformer provides the 2:1 transformation voltage ratio to match the gate impedance, which is represented by the parallel equivalent circuit of 2200-pF capacitance and 210-Ω resistance. Use of the external parallel resistor of 25 Ω simplifies the matching procedure and improves the amplifier stability conditions. The transformer secondary winding provides an inductance of 19 nH, which is required to compensate the device input capacitance at the operating frequency. High quality passive components are necessary to use in the *L*-type output network. The quality factor of the bare copper wire inductance was 375. The series blocking capacitor consists of three parallel disc ceramic capacitors. To realize Class E operation with shunt capacitance, it is sufficient to be limited to only the output device capacitance with a value of 125 pF. This is just slightly larger than that required for optimum drain voltage and current waveforms.

Silicon LDMOSFET devices made it possible in Class E operation to achieve a high output power level with sufficiently high efficiency at

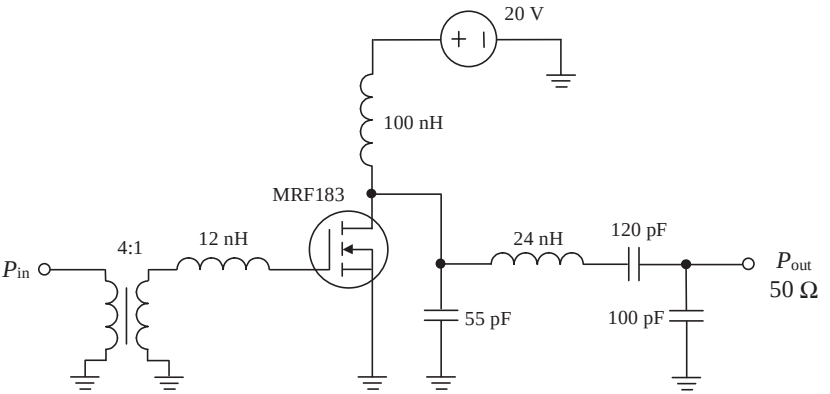


Figure 7.59 High-power Class E LDMOSFET power amplifier [30].

higher frequencies. Using a Motorola MRF183 device, it is possible to achieve a drain efficiency of 70 percent for maximum output power of 54 W, at operating frequency of 144 MHz when the input power is set to 5 W [30]. The drain efficiency can be increased to 88 percent if the output power level is reduced to 14 W by an appropriate increase of the series inductance in the output network. The simplified circuit schematic of such a high-power LDMOSFET amplifier is shown in Fig. 7.59. The input device impedance is quite low; therefore a ferrite transformer and a series inductance are used at the input. At the output, the 50-Ω load impedance is transformed to the 1.5-Ω device output resistance by a lumped L-transformer with a series inductance and a series capacitance. The series inductance is included with the output series resonant LC-circuit. The required value of a parallel switching capacitance is provided by the values of the intrinsic device output capacitance of 38 pF and external capacitance of 55 pF. The quality factor—of about 5—of the resonant circuit was chosen to be sufficiently low to provide some frequency bandwidth operation and to reduce the sensitivity of amplifier performance to the value of resonant circuit elements. To reduce the loss in the output network, the inductor was fabricated by using a 5-mm copper ribbon that provides the inductor quality factor of 150 to 250, depending on the distance to the ground plane. By inserting a piece of conductor between the ribbon and the ground plane the inductance can be tuned at least twice.

The transmission-line Class E power amplifier topology is shown in Fig. 7.60. The electrical lengths of microstrip line l_3 and l_4 should be close to 45° so that an approximate open circuit at the second harmonic will be presented to the switch capacitor, which is the equivalent output device capacitance. The characteristic impedances of all microstrip

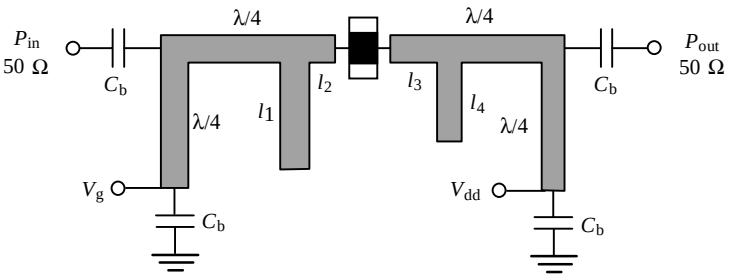


Figure 7.60 Transmission-line Class E power amplifier topology.

lines are 50 Ω, and the substrate is 2.54-mm-thick Duroid with dielectric permittivity $\varepsilon_r = 10.5$. For the Siemens CLY5 MESFET device, with the drain-source capacitance $C_{ds} = 2.4$ pF, a power-added efficiency of 80 percent was achieved at 0.5 GHz with the output power of 0.55 W [24]. In this case, the electrical lengths of the microstrip lines are $l_1 = 73^\circ$, $l_2 = 79^\circ$, $l_3 = 58^\circ$, and $l_4 = 46^\circ$. The power-added efficiency remains above 75 percent over a 10 percent bandwidth, and above 50 percent over a 26 percent bandwidth. Moreover, the power-added efficiency of 73 percent can be realized at 1.0 GHz with the output power of 0.94 W. Using the Fujitsu FLK052WG MESFET device makes possible a Class E power amplifier for higher frequencies [20]. Such a power amplifier demonstrates an output power of 0.61 W, 1-dB compressed gain of 7.6 dB, drain efficiency of 81 percent and power-added efficiency of 72 percent at 5 GHz. The power amplifier was fabricated on Duroid substrate with thickness of 0.508 mm and $\varepsilon_r = 2.2$. As a result, the lengths of 50-Ω (1.6-mm wide) microstrip lines are 9 mm for l_1, 1.8 mm for l_2, 5.3 mm for l_3, and 6.2 mm for l_4, respectively. The power-added efficiency is greater than 70 percent over a 5 percent bandwidth and greater than 60 percent over a 10 percent bandwidth.

Figure 7.61 shows a fully integrated high-efficiency low voltage two-stage Class E power amplifier for mobile communications [35]. In this amplifier, to avoid long transition times from one switching state to the other, the first driver stage is operated in Class F mode with harmonic control from two parallel-tuned resonant circuits. These *LC*-resonant circuits are connected to the drain terminal of the first device, one tuned to the fundamental harmonic and the other one tuned to the third harmonic. These circuits generate a drain voltage waveform, with the necessary first and third harmonic content, approximate to the required square waveform in ideal Class F operation. The final stage is designed to operate in Class E mode when the device output capacitance is accounted for in the required parallel switching capacitance to turn the transistor from on-state to off-state operation conditions.

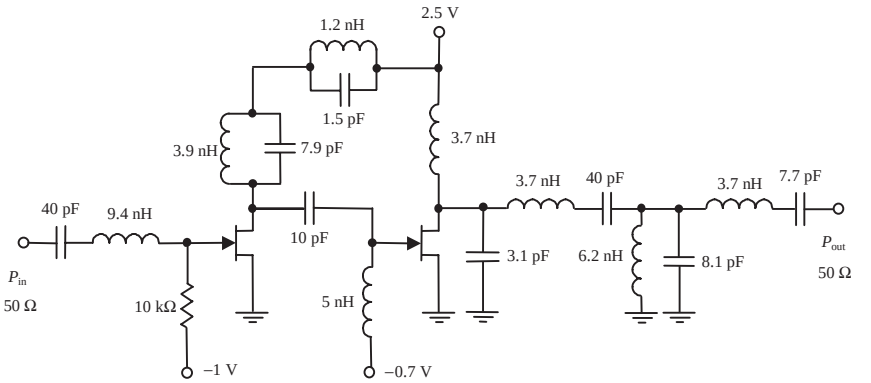


Figure 7.61 Fully integrated high efficiency low voltage Class E power amplifier.

The series resonant circuit is included with the *T*-type output matching circuit. As a result, by using two 0.8-μm GaAs MESFETs with gate widths of 400 μm and 4000 μm, respectively, the power amplifier provides an output power of 24 dBm with a power-added efficiency greater than 50 percent at a supply voltage of 2.5 V over frequency range of 800 to 870 MHz.

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Chapter

8

Broadband Power Amplifiers

In many telecommunication, radar or testing systems, the transmitters operate in a very wide frequency range, for example, 1.5 to 30 MHz in high-frequency transceivers, 225 to 400 MHz in military frequency-agility systems, 470 to 860 MHz in UHF TV transmitters, and 2 to 8 GHz or 6 to 18 GHz in microwave applications. The power amplifier design based on a broadband concept provides some advantages when there is no need to tune resonant circuits, and it is possible to realize fast frequency agility or to transmit a wide multimode signal spectrum. However, there are many factors that restrict the frequency bandwidth depending on the active device parameters. So, it is quite easy to provide multioctave amplification from very low frequencies up to the ultra high-frequency band using the power MOSFET devices when lossy gain compensation is easily provided. This can be possible due to some margin in power gain at lower frequencies for these devices, since its value decreases with frequency by approximately 6 dB per octave. Besides, lossy gain-compensating networks can provide lower input reflection coefficients, smaller gain ripple, more predictable amplifier design and can contribute to amplifier stability factors that are superior to those of lossless match networks. At higher frequencies when the device input impedance is significantly smaller, and influence of its internal feedback and parasitic parameters is substantially higher, it is necessary to use multisection matching networks with lumped and distributed elements. Also it is advisable in some cases to apply the negative feedback technique, which improves the power amplifier linearity.

Generally, the matching design procedure is based on the methods of circuit analysis and synthesis. According to the first method, the circuit

parameters are calculated at one frequency chosen in advance (usually the center or high bandwidth), and then the power amplifier properties are analyzed across the overall frequency bandwidth. In order to synthesize the broadband-matching network, it is necessary to choose the maximum attenuation level or reflection coefficient magnitude in the operating frequency bandwidth and then to obtain the parameters of the matching networks by using special tables and formulas to convert the lumped elements into distributed ones. For push-pull power amplifiers, it is very convenient to use both lumped and distributed parameters when lumped capacitors are connected in parallel to the microstrip lines due to the effect of virtual ground.

Bode-Fano Criterion

The design for a broadband matching circuit should solve a problem with contradictory requirements: wider matching bandwidth with minimum reflection coefficient, or how to minimize the number of the matching network sections for a given wideband specification. The necessary requirements are determined by the Bode-Fano criterion [1, 2], which gives, for certain canonical types of load impedances, a theoretical limit on the minimum reflection coefficient magnitude that can be obtained with an arbitrary matching network. So, for the lossless network with a parallel RC load impedance shown in Fig. 8.1(a) and with a series LR load impedance shown in Fig. 8.1(b) the Bode-Fano criterion states that

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|} d\omega \le \frac{\pi}{\tau} \tag{8.1}$$

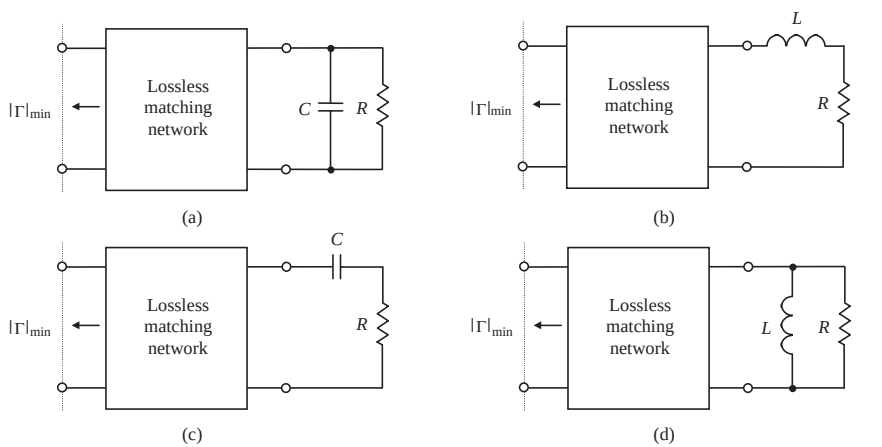

Figure 8.1 Loaded lossless matching circuits.

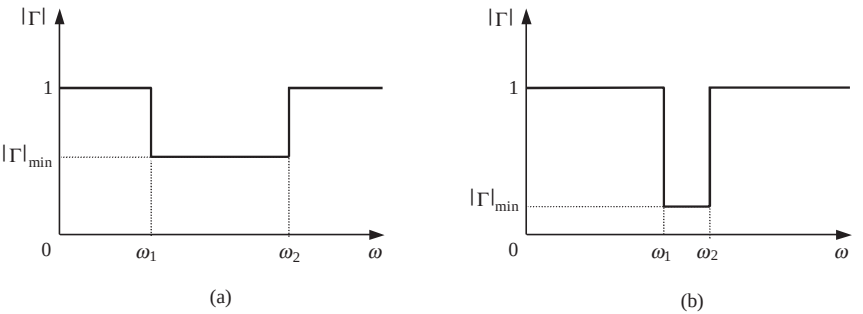

Figure 8.2 Ideal filter flat responses.

where $\tau = RC = L/R$, $\Gamma(\omega)$ is the reflection coefficient seen looking into the arbitrary lossless matching network. For the lossless network with a series RC load impedance shown in Fig. 8.1(c) and with a parallel LR load impedance shown in Fig. 8.1(d), the Bode-Fano integral is

$$\int_0^\infty \omega^{-2} \ln \frac{1}{|\Gamma(\omega)|} d\omega \leq \pi\tau \tag{8.2}$$

The mathematical relationship expressed by Eq. (8.1) or Eq. (8.2) is shown in Fig. 8.2 when two plots reflect an ideal filter with a flat response over the required frequency bandwidth. For the same load, both plots illustrate the important tradeoff: the wider the matching network bandwidth, the worse the reflection coefficient magnitude. And applying Eq. (8.1) for this frequency bandwidth, with $|\Gamma|$ constant within the frequency bandwidth and $|\Gamma| = 1$ otherwise, yields

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|} d\omega = \int_{\omega_1}^{\omega_2} \ln \frac{1}{|\Gamma(\omega)|} d\omega = \Delta\omega \ln \frac{1}{|\Gamma|} \leq \frac{\pi}{\tau} \tag{8.3}$$

Then,

$$|\Gamma|_{\min} = \exp\left(\frac{-\pi}{\Delta\omega\tau}\right) \tag{8.4}$$

where $\Delta\omega = \omega_2 - \omega_1$.

Similarly, for the lossless network with a series RC load impedance and with a parallel LR load impedance,

$$|\Gamma|_{\min} = \exp\left(\frac{-\pi\omega_0^2\tau}{\Delta\omega}\right) \tag{8.5}$$

where $\omega_0 = \sqrt{\omega_1\omega_2}$ is the center bandwidth frequency. It should be noted that the theoretical bandwidth limits can be realized only with an in-

finite number of matching network sections. And the frequency bandwidth with minimum reflection coefficient magnitude is determined by a loaded quality factor $Q_L = \omega_0 \tau$ for the series RL or parallel RC circuit and $Q_L = 1/\omega_0 \tau$ for the parallel RL or series RC circuits. The Chebyshev matching transformer with a finite number of sections can be considered as a close approximation to the ideal passband network when the ripple of the Chebyshev response is made equal to $|\Gamma|_{\min}$. Equations (8.4) and (8.5) can be rewritten in a general simplified form of

$$|\Gamma|_{\min} = \exp\left(-\pi \frac{Q_0}{Q_L}\right) \tag{8.6}$$

where $Q_0 = \omega_0/\Delta\omega$.

Matching Networks with Lumped Elements

When designing broadband matching circuits for power amplifiers it is necessary to transform and to match the device complex impedances with the source and load impedances, which are usually resistive and equal to 50 Ω. For high-power or low-supply voltage cases, the device impedances may be small enough, and it needs to include an ideal transformer IT together with a matching circuit, as shown in Fig. 8.3. Such an ideal transformer provides only a transformation between the resistances applied to its input and output, respectively, and does not have any effect on the circuit frequency characteristics.

To implement such an ideal transformer to the impedance-transforming circuit design, it is useful to apply the Norton transform. An ideal transformer with two capacitors, C_1 and C_2 in Fig. 8.4(a), is replaced by three capacitances connected in the form of a π-transformer, C_I, C_{II} and C_{III} (see Fig. 8.4(b)). Their values are determined by

$$C_I = n_T(n_T - 1)C_1 \tag{8.7}$$

$$C_{II} = n_T C_1 \tag{8.8}$$

$$C_{III} = C_2 - (n_T - 1)C_1 \tag{8.9}$$

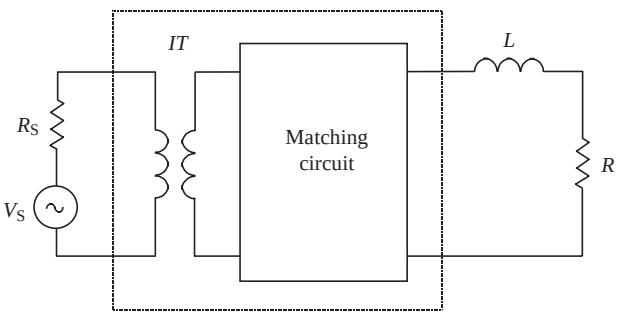

Figure 8.3 Matching circuit with ideal transformer.

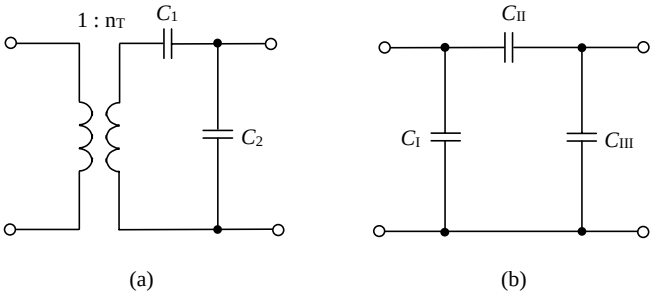

Figure 8.4 Capacitive impedance transforming circuits.

where n_T is the transformation coefficient. In this case, all of the parameters of these two-port networks are identical at any frequency. However, such a replacement is possible only if the capacitance C_{III} obtained by Eq. (8.9) is positive and, consequently, physically realizable.

At the same time, an ideal transformer with two inductors, L_1 and L_2 (see Fig. 8.5(a)) can be replaced by three inductors connected in the form of a T-transformer, L_I, L_{II} and L_{III} in Fig. 8.5(b), with values determined by

$$L_I = n_T(n_T - 1)L_2 \tag{8.10}$$

$$L_{II} = n_T L_2 \tag{8.11}$$

$$L_{III} = L_1 - (n_T - 1)L_2 \tag{8.12}$$

Again, the replacement is possible only if the inductance L_{III} defined by Eq. (8.12) is positive and, consequently, physically realizable.

The broadband impedance-transforming circuits represent the transforming bandpass filters when the in-band matching requirements with specified ripple must be satisfied. The out-of-band mismatching can be very significant. One of the design methods for such matching circuits is based on the theory of transforming low-pass filters of a ladder

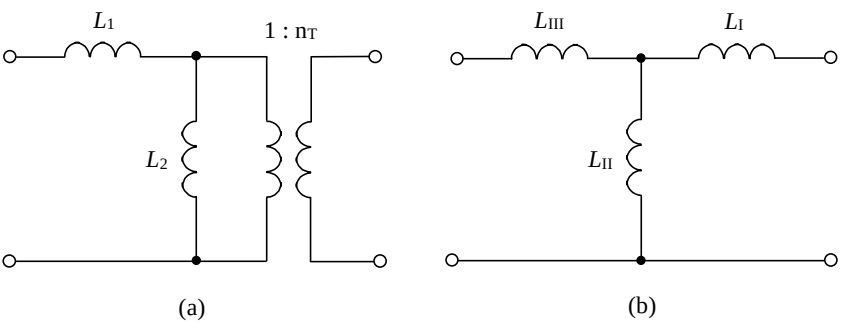

Figure 8.5 Inductive impedance transforming circuits.

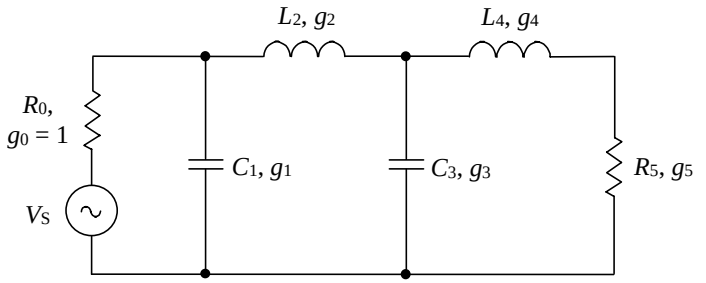

Figure 8.6 Two-section impedance-transforming circuit.

configuration of series inductances alternating with shunt capacitances, whose two-section equivalent representation is shown in Fig. 8.6. For a large ratio of R_0/R_5, mismatching at zero frequency is too high and such a matching circuit can be treated as a bandpass impedance-transforming filter.

Table 8.1 gives the maximum passband ripples and coefficients g_1 and g_2 needed to calculate the parameters of a two-section low-pass Chebyshev filter for different transformation ratios $r = R_0/R_5$, and frequency bandwidths $w = 2(f_2 - f_1)/(f_2 + f_1)$, where f_2 and f_1 are the high- and low-bandwidth frequencies, respectively [3]. The coefficients g_3 and g_4 are calculated according to $g_3 = rg_2$ and $g_4 = g_1/r$, respectively, and the circuit elements can be obtained by

$$C_1 = g_1/\omega_0 R_0 \qquad C_3 = g_3/\omega_0 R_0 \tag{8.13}$$

$$L_2 = g_2 R_0/\omega_0 \qquad L_4 = g_4 R_0/\omega_0 \tag{8.14}$$

TABLE 8.1 Two-Section Low-Pass Chebyshev Filter Parameters [3]

r	w	ripple, dB	g_1	g_2
5	0.1	0.000087	1.26113	0.709217
	0.2	0.001389	1.27034	0.704050
	0.3	0.007023	1.28561	0.695548
	0.4	0.022109	1.30687	0.638859
10	0.1	0.000220	1.60350	0.591627
	0.2	0.003516	1.62135	0.585091
	0.3	0.017754	1.65115	0.574412
	0.4	0.055746	1.69304	0.559894
25	0.1	0.000625	2.11734	0.462747
	0.2	0.009993	2.15623	0.454380
	0.3	0.050312	2.22189	0.440863
	0.4	0.156725	2.31517	0.422868
50	0.1	0.001303	2.57580	0.384325
	0.2	0.020801	2.64380	0.374422
	0.3	0.104210	2.75961	0.358638
	0.4	0.320490	2.92539	0.338129

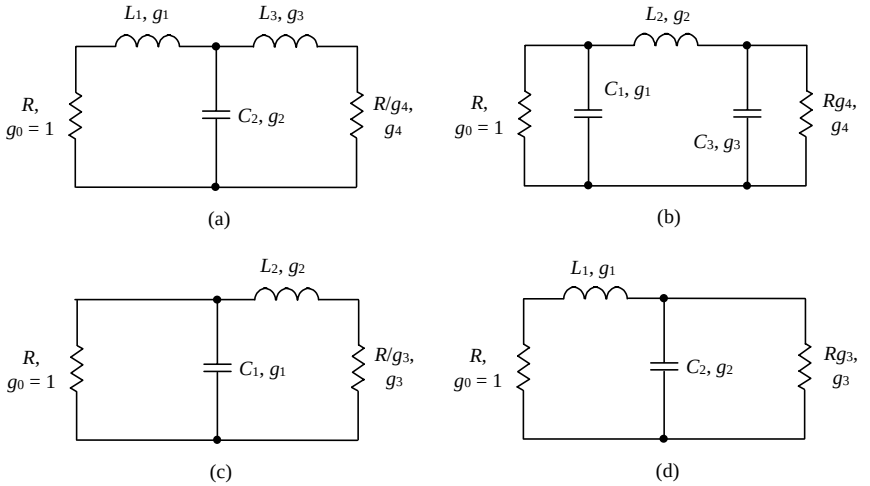

Figure 8.7 Lumped L-, π- and T-type impedance-transforming circuits.

Another approach is based on the transform from the low-pass prototype filters, whose simple L-, T- and π-type equivalent circuits are shown in Fig. 8.7, to the bandpass filters. Table 8.2 gives the parameters of the low-pass Chebyshev filter prototypes for different maximum in-band ripples and number of sections $n = 1, 2, 3$ [4]. The transformation from the low-pass to bandpass prototype filters can be obtained using frequency substitution in the form of

$$\omega \to \frac{\omega_0}{\Delta\omega}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \tag{8.15}$$

where $\omega_0 = \sqrt{\omega_1\omega_2}$, $\Delta\omega = \omega_2 - \omega_1$, ω_1 and ω_2 are the low and high edges of the passband. As a result, a series inductance L_k is transformed into

TABLE 8.2 Parameters of Low-Pass Chebyshev Filters-Prototypes [4]

ripple, dB	n	g_1	g_2	g_3	g_4
0.01	1	0.0960	1.0000		
	2	0.4488	0.4077	1.1007	
	3	0.6291	0.9702	0.6291	1.0000
0.1	1	0.3052	1.0000		
	2	0.8430	0.6220	1.3554	
	3	1.0315	1.1474	1.0315	1.0000
0.2	1	0.4342	1.0000		
	2	1.0378	0.6745	1.5386	
	3	1.2275	1.1525	1.2275	1.0000
0.5	1	0.6986	1.0000		
	2	1.4029	0.7071	1.9841	
	3	1.5963	1.0967	1.5963	1.0000

a series LC circuit according to

$$\omega L_{\mathrm{k}} = \frac{\omega_0}{\Delta\omega}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)L_{\mathrm{k}} = \omega L'_{\mathrm{k}} - \frac{1}{\omega C'_{\mathrm{k}}} \tag{8.16}$$

where

$$L'_{\mathrm{k}} = \frac{L_{\mathrm{k}}}{\Delta\omega} \qquad C'_{\mathrm{k}} = \frac{\Delta\omega}{\omega_0^2 L_{\mathrm{k}}}$$

Similarly, a shunt capacitance C_{k} is transformed into a shunt LC circuit

$$\omega C_{\mathrm{k}} = \frac{\omega_0}{\Delta\omega}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)C_{\mathrm{k}} = \omega C'_{\mathrm{k}} - \frac{1}{\omega L'_{\mathrm{k}}} \tag{8.17}$$

where

$$C'_{\mathrm{k}} = \frac{C_{\mathrm{k}}}{\Delta\omega} \qquad L'_{\mathrm{k}} = \frac{\Delta\omega}{\omega_0^2 C_{\mathrm{k}}}$$

The low-pass prototype filter will be transformed to the bandpass one when all its series elements are replaced by series resonant circuits, all its parallel elements are replaced by parallel resonant circuits, and each of them is tuned on a resonant frequency ω_0. The bandpass filter elements can be calculated from

$$\Delta\omega C_{\mathrm{k}} = g_{\mathrm{k}}/R \tag{8.18}$$

$$\Delta\omega L_{\mathrm{k}} = g_{\mathrm{k}} R \tag{8.19}$$

where k is an element serial number for a low-pass prototype filter, and g_{k} are the appropriate coefficients given by Table 8.2.

Consider the design of the low-pass prototype filter for a given maximum ripple level, in a frequency range up to $\omega_{2(2)}$ for a two-element filter, and up to $\omega_{2(3)}$ for three elements, as shown in Fig. 8.8(a). Then, an arbitrary frequency ω_0 is chosen and a series capacitance is added to each inductance, and a parallel inductance is added to each capacitance on the assumption that all these resonant circuits are tuned on the arbitrary frequency ω_0. As a result, a new bandpass filter will be realized with the same ripple shown in Fig. 8.8(b) for $n = 2$ and $n = 3$ with the passbands $\Delta\omega_{(2)}$ and $\Delta\omega_{(3)}$, respectively. Their elements are calculated according to Eqs. (8.18) and (8.19).

The maximum ripple level shown in Fig. 8.8 determines the insertion loss IL or power loss ratio P_{LR} through the magnitude of the reflection coefficient Γ by

$$IL = 10\log_{10} P_{\mathrm{LR}} = -10\log_{10}(1 - |\Gamma(\omega)|^2) \tag{8.20}$$

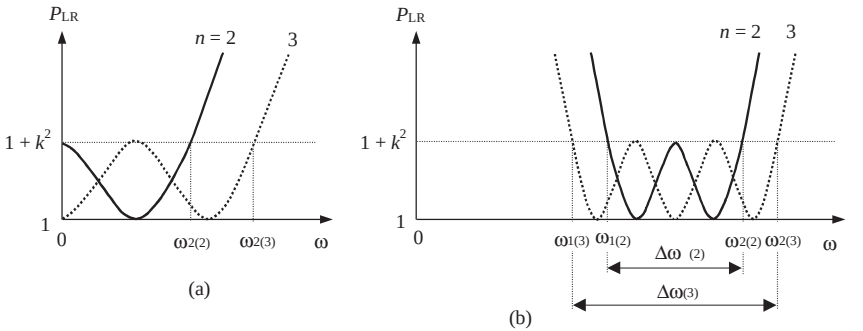

Figure 8.8 Maximum ripple level versus frequency bandwidth.

For an n-order Chebyshev low-pass filter, P_{LR} can be obtained from

$$P_{LR} = 1 + k^2 T_n^2 \left(\frac{\omega}{\omega_c} \right) \tag{8.21}$$

where ω_c is the cutoff frequency. The passband response has equal ripples of amplitude $1 + k^2$, and the n-order Chebyshev polynomials are

$$T_1(x) = x \tag{8.22}$$

$$T_2(x) = 2x^2 - 1 \tag{8.23}$$

$$T_3(x) = 4x^3 - 3x \tag{8.24}$$

$$T_4(x) = 8x^4 - 8x^2 + 1 \tag{8.25}$$

Higher-order polynomials can be found using recurrence in the form of

$$T_n(x) = 2xT_{n-1}(x) - T_{n-2}(x) \tag{8.26}$$

where $x = \omega/\omega_c$.

Generally, the low-pass prototype filters, as well as bandpass filters obtained on their basis, do not perform an impedance transformation. The input and output resistances are either equal for the symmetric T- or π-type filters shown in Fig. 8.7(a, b) where $g_4 = 1$ or their ratio is too small for L-type filters as those shown in Fig. 8.7(c, d) where $g_3 < 2$. Therefore, in this case, it is necessary to use the concept of an ideal transformer. This approach is also attractive due to the existence of tables from which the parameters of such impedance-transforming networks can be easily calculated for a given quality factor of device input or output circuit.

Consider the design example of the matching transformer based on the bandpass filter with a maximum in-band ripple of 0.5 dB, input device impedance with $R_{in} = 1\,\Omega$ and $L_{in} = 1$ nH at the operating

frequency of 1.5 GHz. For the two-section low-pass filter shown in Fig. 8.6 with $R_0 = 50\,\Omega$ and $r = 50$, $g_1 = g_4 r = \omega_0 L_{\text{in}} r/R_0 = 9.4$, which is too large to use Table 8.1. For $n = 2$, $R = R_{\text{in}}$ and $L_1 = L_{\text{in}}$, from Table 8.2 and Eq. (8.19), we can obtain the coefficients $g_1 = 1.4029$, $g_2 = 0.7071$ and $g_3 = 1.9841$ for the relative frequency bandwidth determined by

$$\frac{\Delta\omega}{\omega_0} = g_1 \frac{R}{\omega_0 L_1} \tag{8.27}$$

which yields $\Delta\omega/\omega_0 \cong 0.17$ and the frequency bandwidth of 223 MHz. Equation (8.27) is a function of the coefficient g_1 and the quality factor $Q_1 = \omega_0 L_1/R$, and allows us to evaluate the frequency bandwidth

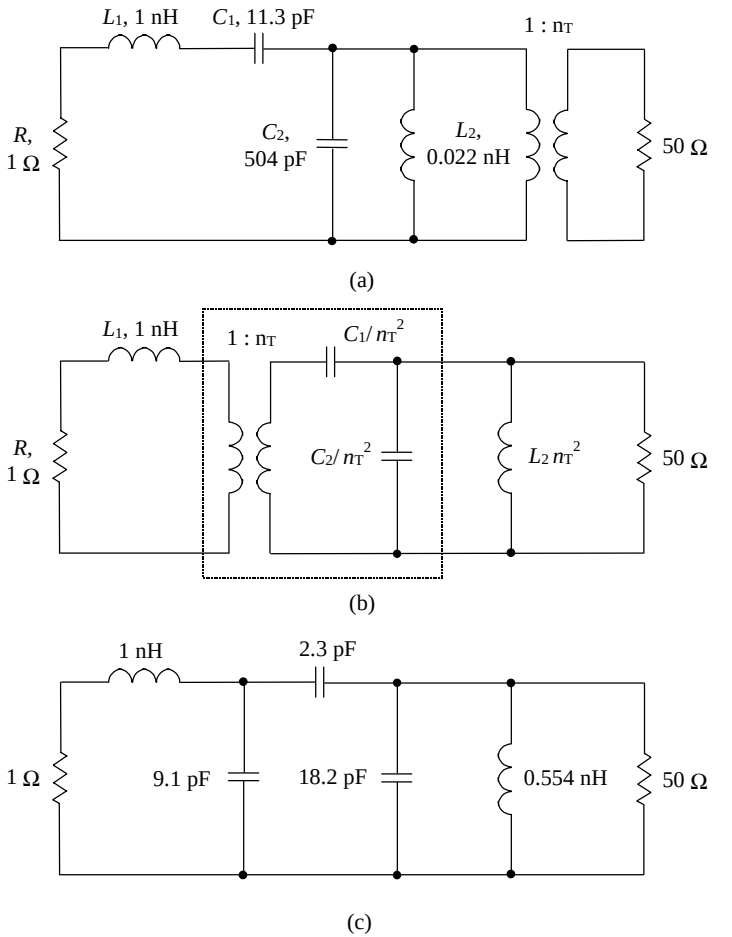

Figure 8.9 Matching transformer design procedure using passband filter.

with a specified maximum ripple when the number of filter sections is increased. For our case, increasing the number of filter sections up to $n = 10$ when $g_1 = 1.7543$ yields a wider frequency bandwidth of $1.7543/1.4029 = 1.2505$ or approximately 25 percent. However, the circuit realization becomes too complicated. The capacitance C_2 is determined from Eq. (8.18) as equal to $C_2 = g_2/R\Delta\omega = 504$ pF. To convert the low-pass filter to its bandpass prototype, it is necessary to connect the capacitance C_1 in series with the inductance L_1, and the inductance L_2 in parallel with the capacitance C_2, as shown in Fig. 8.9(a). The resonant frequency of these series and parallel circuits should be equal to $\omega_0 = 1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_2}$. Such a bandpass filter has the required bandwidth properties for the source resistance of $Rg_3 = 1.9841\ \Omega$ that it requires the connection of an ideal transformer IT with $n_\mathrm{T} = \sqrt{50/1.9841} = 5.02$. To exclude this transformer in accordance with Fig. 8.4, move the elements C_1, C_2 and L_2 to the right from IT, as shown in Fig. 8.9(b). Then, by taking into account Eqs. (8.7) to (8.9), we can obtain the circuit shown in Fig. 8.9(c).

When designing an interstage impedance-transforming circuit, it is necessary to take into account the parasitic capacitance and inductance of the device output, together with the parasitic inductance of the device input, as shown in Fig. 8.10(a). Consider the design procedure for an impedance-transforming circuit described in [5], at the center operating frequency of 1 GHz for a T-type low-pass prototype filter shown in Fig. 8.7(a). Initially, the parallel connection of the device output resistance R_out and capacitance C_out should be converted to the appropriate series one at the center frequency ω_0 according to

$$R'_\mathrm{out} = \frac{R_\mathrm{out}}{1 + (\omega_0 R_\mathrm{out} C_\mathrm{out})^2} \tag{8.28}$$

$$C'_\mathrm{out} = \frac{1 + (\omega_0 R_\mathrm{out} C_\mathrm{out})^2}{(\omega_0 R_\mathrm{out})^2 C_\mathrm{out}} \tag{8.29}$$

as shown in Fig. 8.10(b).

Suppose the maximum ripple is equal to 0.1 dB; from Table 8.2 we then can obtain $g_1 = g_3 = 1.0315, g_2 = 1.1474, g_4 = 1$ and IT transformation coefficient $n_\mathrm{T} = \sqrt{9.8/1.5}$, which give the impedance-transforming circuit in the form shown in Fig. 8.10(c). Here, the reactances for each series element are equal to 9.42 Ω. The reactances for each parallel element are 0.215 Ω. Moving the ideal transformer IT to the right part in order to apply a Norton transform gives the circuit shown in Fig. 8.10(d), where the required series elements with reactances of $9.42n_\mathrm{T}^2\ \Omega$ are realized by the existing device output capacitance C'_out and inductance L_out and additional elements L' and C'.

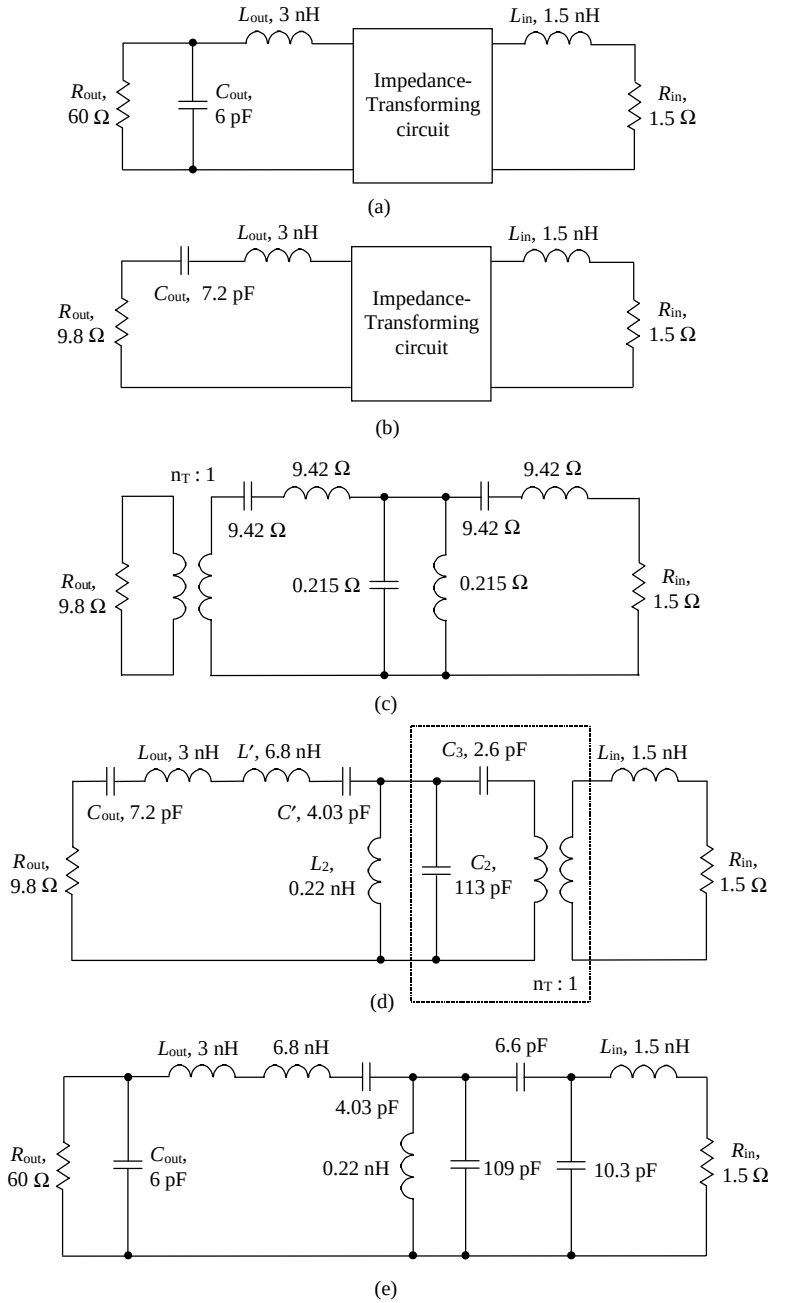

Figure 8.10 Matching transformer design procedure using low-pass filter-prototype.

According to Eq. (8.27) the relative frequency bandwidth in this case is $\Delta\omega/\omega_0 = g_1 R_{\text{in}}/\omega_0 L_{\text{in}} = 16.5$ percent. Using a Norton transform for an ideal transformer and two capacitances leads to the final circuit shown in Fig. 8.10(e).

Matching Networks with Mixed Lumped and Distributed Elements

The matching circuits, which incorporate mixed lumped and transmission line elements, are widely used both in hybrid and monolithic design technique. Such matching circuits are very convenient when designing the push-pull power amplifiers, where the parallel capacitances are simply connected between two series microstrip lines. A basic two-stage design procedure consists of an appropriate topology resulting in near-maximum gain, which is chosen by calculating the parameters, and then the application of an optimization technique to minimize power ripple over the operation frequency bandwidth [6].

A periodic LC structure in the form of the low-pass ladder π-network is used as a basis for the lumped matching prototype. Then, the lumped prototype should be split up into individual π-type sections with equal capacitances—by the consecutive step-by-step process—and replaced by their equivalent distributed network counterparts. Finally, the complete mixed matching structure is optimized to improve the overall performance by employing standard nonlinear optimization routines on the element values.

For a single frequency equivalence between lumped and distributed elements, the low-pass lumped π-type ladder section can be made equivalent to a symmetrically loaded transmission line at the single frequency, as shown in Fig. 8.11(a). The transfer $ABCD$-matrices of these lumped and distributed ladder sections can be given by

$$[ABCD]_{\text{L}} = \begin{bmatrix} 1 - \omega_0^2 LC & j\omega_0 L \\ j\omega_0 C\,(2 - \omega_0^2 LC) & 1 - \omega_0^2 LC \end{bmatrix} \tag{8.30}$$

$$[ABCD]_{\text{T}} = \begin{bmatrix} \cos\theta_0 - \omega_0 C_{\text{T}} Z_0 \sin\theta_0 & jZ_0 \sin\theta_0 \\ \dfrac{j}{Z_0}\left(2\omega_0 C_{\text{T}} Z_0 \cos\theta_0 + \sin\theta_0 - \omega_0^2 C_{\text{T}}^2 Z_0^2 \sin\theta_0\right) & \cos\theta_0 - \omega_0 C_{\text{T}} Z_0 \sin\theta_0 \end{bmatrix} \tag{8.31}$$

where θ_0 is the electrical length of a transmission line at the center bandwidth frequency ω_0.

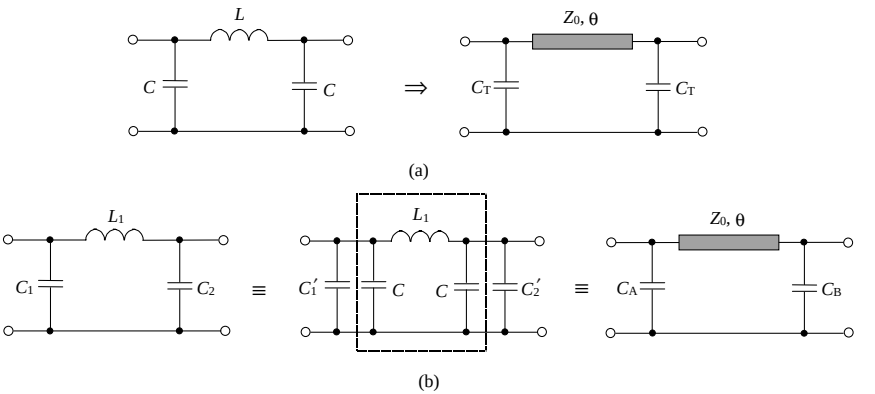

Figure 8.11 Transforming design procedure for lumped and distributed matching circuits.

Consequently, as these two circuits are equivalent, having equal matrix elements of $A_L = A_T$ and $B_L = B_T$, one can obtain

$$1 - \omega_0^2 LC = \cos\theta_0 - \omega_0 C_T Z_0 \sin\theta_0 \tag{8.32}$$

$$j\omega_0 L = jZ_0 \sin\theta_0 \tag{8.33}$$

After solving Eqs. (8.32) and (8.33), the characteristic impedance Z_0 and parallel capacitance C_T can be directly calculated as

$$Z_0 = \frac{\omega_0 L}{\sin\theta_0} \tag{8.34}$$

$$C_T = \frac{\cos\theta_0 + \omega_0^2 LC - 1}{\omega_0^2 L} \tag{8.35}$$

To provide a design method using a single frequency equivalent technique, the following consecutive design steps are performed [6]:

- Designate the lumped π-type C_1-L_1-C_2 section to be replaced.
- From the chosen π-type C_1-L_1-C_2 section, form the symmetrical C-L-C ladder section with equal capacitances C (shown in Fig. 8.11(b)). The choice is arbitrary but the values cannot exceed the minimum of (C_1, C_2).
- Calculate the parameters of the symmetrical C_T-TL-C_T using the parameters of the lumped equivalent π-section by setting the electrical length θ_0 of a transmission line according to Eqs. (8.34) and (8.35). Here, it is presumed that the minimum of the capacitances C_1 and C_2 should be greater or equal than C_T so that C_T can be readily embedded in the new C_T-TL-C_T section.

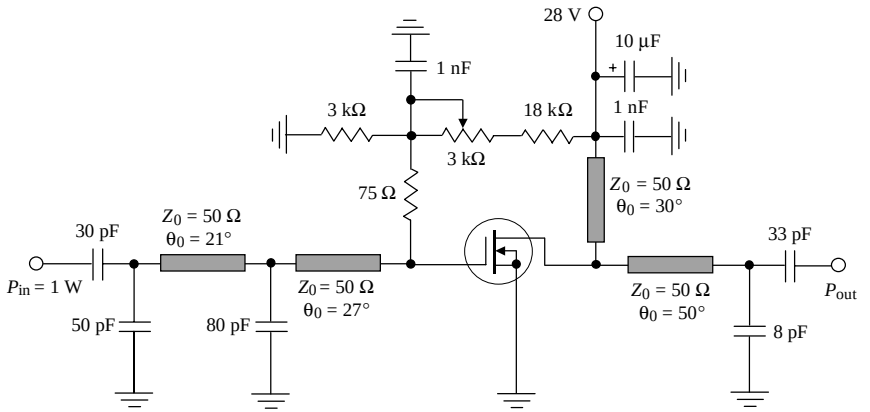

Figure 8.12 Circuit schematic of broadband LDMOSFET power amplifier.

- Finally, replace the π-type C_1-L_1-C_2 ladder section by the equivalent symmetrical C_T-TL-C_T section as shown in Fig. 8.11(*b*) where the loaded parallel capacitances C_A and C_B are given as $C_A = C_1' + C_T$ and $C_B = C_2' + C_T$.

Figure 8.12 shows the electrical schematic of a broadband RF high-power LDMOSFET amplifier intended for wireless applications. To provide about 15 W output power with power gain of more than 10 dB in a frequency range of 225 to 400 MHz, a device with a gate geometry of 1.25 μm × 40 mm and supply voltage of 28 V was chosen. In this case, the matching design technique is based on using multisection low-pass networks, two π-type sections for input matching circuit, and one π-type section for output matching circuit, with series microstrip lines and parallel capacitances. The sections adjacent to the device input and output terminals incorporate the corresponding internal input and output device capacitances. Since a ratio between the device output resistance for several tens of watts of output power and load resistance of 50 Ω is not significant, it is sufficient to be limited to only one section for the output matching network. Once a matching network structure is chosen, based on the requirements for the electrical performance and frequency bandwidth, the simplest and fastest way is to apply an optimization procedure using CAD simulators to satisfy certain criteria. For such a broadband power amplifier, these criteria can be the minimum output power ripple and input return loss with maximum power gain and efficiency. To minimize the overall dimensions of the amplifier circuit realization, the parallel microstrip line in the drain circuit was treated as an element of the output matching circuit and its electrical length was considered as a variable to be optimized. Applying a nonlinear broadband optimization technique (incorporated, for example,

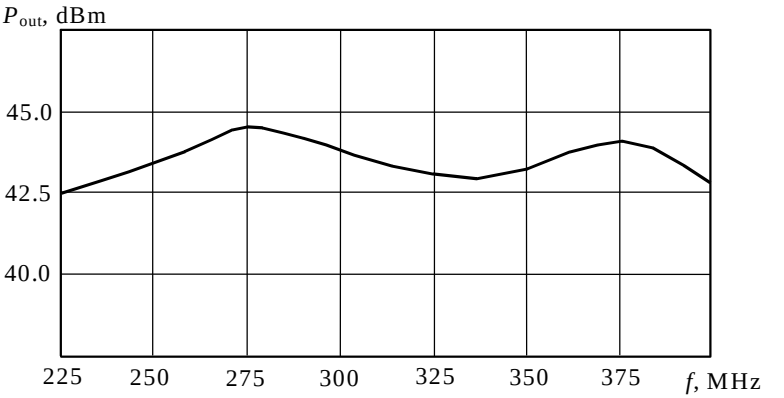

Figure 8.13 Output power versus bandwidth frequency.

into the circuit simulator Ansoft's Serenade or ADS) and setting the ranges of electrical length of the transmission lines between 0° and 90° and parallel capacitances from 0 to 100 pF, we obtain the parameters of the input and output matching circuits. However, to speed up this procedure, it is best to optimize circuit parameters separately for the input and output matching circuits with the device equivalent input and output impedances: a series *RC* circuit for the device input and a parallel *RC* circuit for the device output. It is sufficient to use a fast linear optimization process, which will take only a few minutes to complete the matching circuit design. Then, the resulting optimized values are incorporated into the overall power amplifier circuit for each element and final optimization is performed using a large-signal active device model. In this case, the optimization process is finalized by choosing the nominal level of input power with optimizing elements in narrower ranges of their values of about 10 to 20 percent for most critical elements. For practical convenience, all transmission lines have the characteristic impedances of 50 Ω. Figure 8.13 illustrates the simulated broadband power amplifier performance where the output power is in the range 42.5 to 44.5 dBm, with a power gain of 13.5 ± 1 dB, in a frequency bandwidth of 225 to 400 MHz.

Matching Networks with Transmission Lines

The lumped or mixed matching networks generally work well at sufficiently low frequencies (up to several gigahertz). However, the lumped elements such as inductors and capacitors are difficult to implement at microwave frequencies where they can be treated as distributed elements. In addition, the quality factors for inductors are sufficiently small that they contribute to additional losses. To convert lumped

elements to transmission line sections, a Richards's transformation is used, which is written as

$$s = j \tan\theta \tag{8.36}$$

where $s = j\omega$ is the frequency variable, $\theta = 2\pi l/\lambda$ is the electrical length of transmission line, and l is its length [7]. This transformation is necessary to synthesize an LC network using open-circuited and short-circuited transmission lines. For inductive short-circuited stub impedance

$$Z_{\mathrm{L}} = sL = j\omega L = jL \tan\theta \tag{8.37}$$

For the capacitive open-circuited stub admittance,

$$Y_{\mathrm{C}} = sC = j\omega C = jC \tan\theta \tag{8.38}$$

Cutoff occurs at unit frequency for a low-pass filter prototype, which yields the result when an inductor can be replaced with a short-circuited stub of $l = \lambda/8$, while a capacitor can be replaced with an open-circuited stub of the same length, as shown in Fig. 8.14.

As an example, consider the design of the broadband input matching circuit in the form of a two-section low-pass transforming filter shown in Fig. 8.6, with a center bandwidth frequency of $\omega_0 = 3$ GHz to match 50-Ω source impedance with the device input impedance $Z_{\mathrm{in}} = R_{\mathrm{in}} + j\omega_0 L_{\mathrm{in}}$, where $R_{\mathrm{in}} = 2\ \Omega$ and $L_{\mathrm{in}} = 0.223$ nH. The value of the series input device inductance is chosen to satisfy Table 8.1 when, for $n = 4$, $w = 0.4$, maximum ripple of 0.156725, $r = 25$ and $g_1 = 2.31517$, from Eq. (8.14) it follows that

$$L_4 = \frac{g_4 R_0}{\omega_0} = \frac{g_1 R_0}{\omega_0 r} = 0.223 \text{ nH}$$

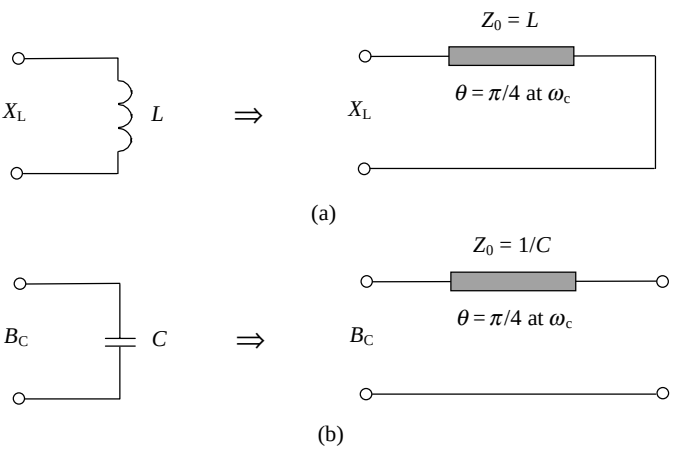

Figure 8.14 Single frequency equivalence between lumped elements and transmission lines.

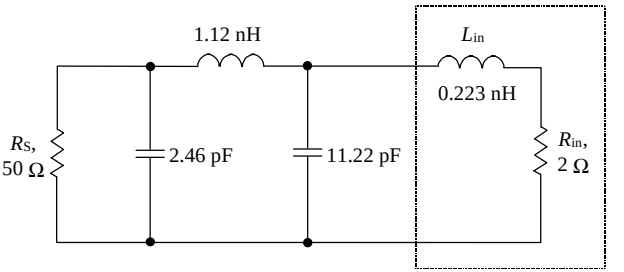

Figure 8.15 Two-section broadband matching circuit.

From Table 8.1, we obtain $g_2 = 0.422868$, which gives (using Eqs. (8.13) and (8.14)) the circuit parameters shown in Fig. 8.15. The inductance value is chosen for design convenience. If this value differs from the required value, it means that it is necessary to change the maximum frequency bandwidth, the power ripple or the number of ladder sections.

The application of a Richards's transformation provides a sequence of short-circuited and open-circuited stubs, which are converted to a more practical circuit implementation. This can be done using four Kuroda identities, which allows these stubs to be physically separated, transforming the series stub into the shunt and changing impractical characteristic impedances into more realizable ones [8]. The Kuroda identities use redundant transmission line sections, which are called *unit elements* and are $\lambda/8$ long at ω_c. These unit elements are thus commensurate with the stubs used to implement inductors and the capacitors of the prototype design. The unit elements should connect only the transforming two-port network and the load. In this case, connecting the unit element with characteristic impedance of Z_0 to the same load impedance Z_0 does not change the input impedance. The four Kuroda identities are illustrated in Fig. 8.16, where the combinations of unit elements with the characteristic impedance Z_0 and length $l = \lambda/8$, the reactive elements, and the relationships between them are given. To prove the equivalence, consider two circuits of identity at the first row in Fig. 8.16(a) when the *ABCD*-matrix for the entire left circuit can be written as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{L}} = \frac{1}{\sqrt{1-s^2}} \begin{bmatrix} 1 & 0 \\ sC & 1 \end{bmatrix} \begin{bmatrix} 1 & sZ_1 \\ \dfrac{s}{Z_1} & 1 \end{bmatrix}$$

$$= \frac{1}{\sqrt{1-s^2}} \begin{bmatrix} 1 & sZ_1 \\ s\left(C + \dfrac{1}{Z_1}\right) & 1 + s^2 Z_1 C \end{bmatrix} \tag{8.39}$$

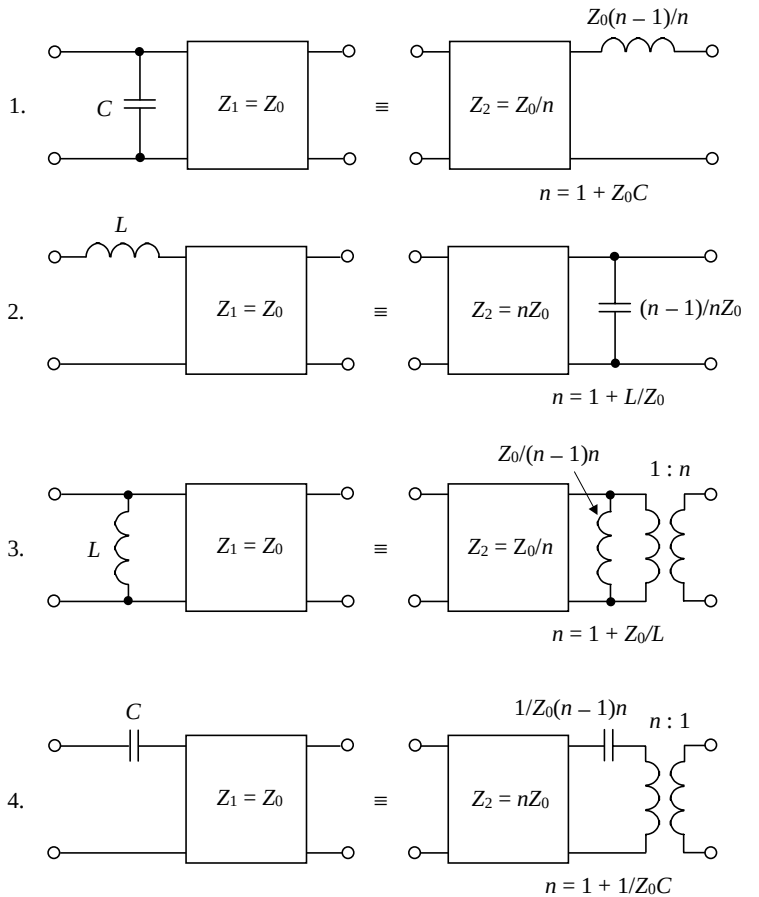

Figure 8.16 Four Kuroda identities.

For the right circuit

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{R}} = \frac{1}{\sqrt{1-s^2}} \begin{bmatrix} 1 & sZ_2 \\ \dfrac{s}{Z_2} & 1 \end{bmatrix} \begin{bmatrix} 1 & sL \\ 0 & 1 \end{bmatrix}$$

$$= \frac{1}{\sqrt{1-s^2}} \begin{bmatrix} 1 & s(Z_2+L) \\ \dfrac{s}{Z_2} & 1+\dfrac{s^2L}{Z_2} \end{bmatrix} \tag{8.40}$$

where Z_1 and Z_2 are the characteristic impedances of the left unit element and right one, respectively. The results in Eqs. (8.39) and (8.40)

are identical if

$$Z_1 = Z_2 + L \qquad \frac{1}{Z_1} + C = \frac{1}{Z_2} \qquad \frac{L}{Z_2} = Z_1 C$$

or

$$Z_2 = \frac{Z_1}{n} \qquad L = \frac{n-1}{n} Z_1 \tag{8.41}$$

where $n = 1 + Z_1 C$.

Figure 8.17 shows the design transformation of a lumped low-pass transforming filter to a microstrip one using the Kuroda identities. The first step (shown in Fig. 8.17(a)) is to add a 50-Ω unit element at the end of the circuit and convert a shunt capacitor to a series inductor—as shown in Fig. 8.17(b)—using the first Kuroda identity. Then, adding another unit element and applying the second Kuroda identity (see Fig. 8.17(c)) leads to the circuit with two unit elements and three parallel capacitors shown in Fig. 8.17(d). To keep the same physical dimensions during the calculation of the circuit parameters, the inductance should be taken in nanohenri. The capacitance is measured in nanofarad if the operating frequency is measured in gigahertz. Finally, a Richards's transformation is used to convert the parallel capacitors to shunt stubs. According to Eq. (8.38), the normalized characteristic impedance of a shunt stub is $1/C$, which it is necessary to multiply by 50 Ω.

Figure 8.17(e) shows the microstrip layout of the final low-pass transforming circuit. The lengths of the shunt stubs are $\lambda/8$ at the cutoff frequency f_c, as well as the length of each unit element representing the series stubs. If the normalized frequency bandwidth and center bandwidth frequency are chosen to be $w = 0.4$ and $f_0 = 3$ GHz, the cutoff frequency is

$$f_c = f_0 \left(1 + \frac{w}{2}\right) = 3.6 \text{ GHz}$$

An alternative impedance matching technique depends on using the multisection matching transformers consisting of stepped transmission-line sections with different characteristic impedances. These transformers, in contrast to the continuously tapered transmission-line transformers, are significantly shorter and find broader performance. Figure 8.18(a) shows a stepped transmission-line transformer, which consists of a cascaded connection of n uniform sections of equal lengths $l = \lambda_0/4$, where λ_0 is the wavelength corresponding to the central bandwidth frequency ω_0. Such a transformer may be constructed using any type of transmission lines. In Fig. 8.19, as an example, the minimum possible *VSWR* is plotted as a function of the step spacing for a five-step transformer having a total characteristic

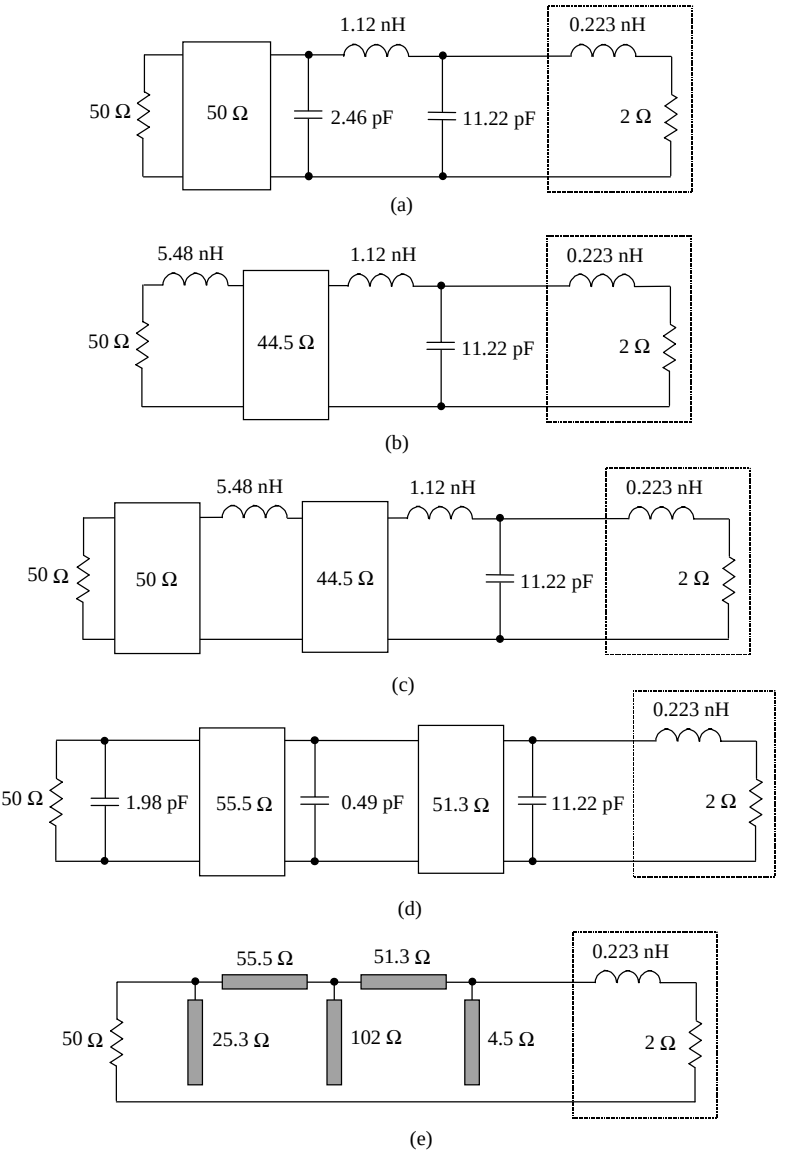

Figure 8.17 Design transform from lumped low-pass to microstrip transforming filter.

impedance change ratio of 8:1 designed for maximum *VSWR* of 1.021 in an octave frequency bandwidth where each section is of quarterwave electrical length [9].

The stepped transmission-line transformer shown in Fig. 8.18(*a*) represents an antimetric structure, for which the relationship between the

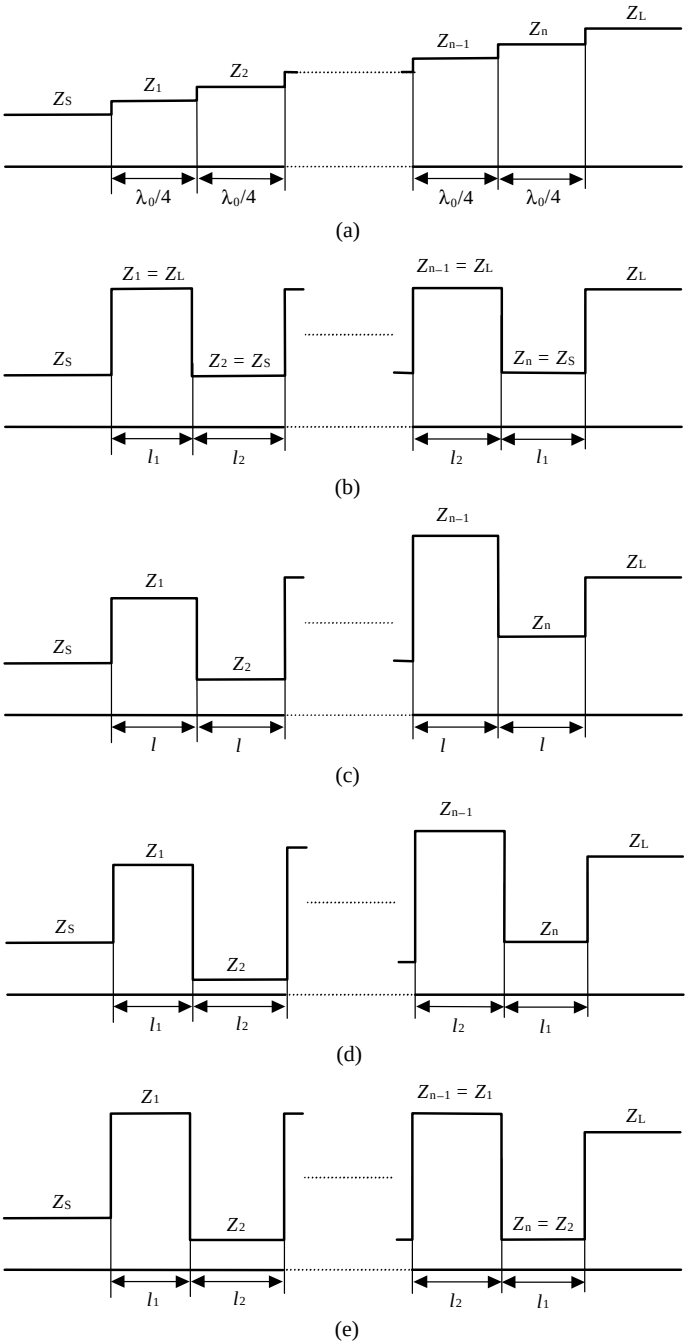

Figure 8.18 Schematic structures of different stepped transmission-line transformers.

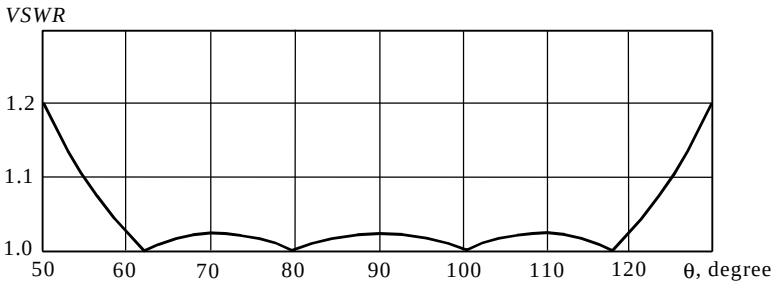

Figure 8.19 Theoretical frequency bandwidth of five-step transformer [9].

characteristic impedances of its sections may be written in the form of [10]

$$Z_{\mathrm{i}} Z_{\mathrm{n+1-i}} = Z_{\mathrm{S}} Z_{\mathrm{L}} \quad i = 1, 2, \ldots, n \tag{8.42}$$

The main drawback of such transformers is their significant total length of $L = n\lambda_0/4$. However, it is possible to reduce the transformer length by applying other profiles of its structure. The stepped transformers using n cascaded uniform transmission line sections of various lengths with alternating impedances are shorter by 1.5 to 2 [11]. In this case, the number of sections n is always an even number and the section impedances may be equal to the source and load impedances to be matched, as shown in Fig. 8.18(b). To define the unknown section lengths, the optimization approach to achieve the global minimum of the objective function $|\Gamma(\theta, A)|$ was used, written in the form of

$$\min_{\mathrm{A}} \max_{\theta \in [\theta_1, \theta_2]} |\Gamma(\theta, A)| \tag{8.43}$$

where θ_1 and θ_2 are the electrical lengths at the low- and high-frequency bandwidth edges, respectively, and the vector $A = (A_1, A_2, \ldots, A_{\mathrm{n}})$ consists of the normalized section lengths $L_{\mathrm{i}} = l_{\mathrm{i}}/\lambda_0$ as components. Solving Eq. (8.43) numerically, we find that the optimum Chebyshev characteristics can be provided by the transmission line structure with [11]

$$l_{\mathrm{i}} = l_{\mathrm{n+1-i}} \quad i = 1, 2, \ldots, n/2 \tag{8.44}$$

The total length of such a stepped transmission-line transformer can be further reduced by using the structure representing the cascade connection of n transmission line sections (where n is an even number) of the same length $l < \lambda_0/4$ with [12]

$$\begin{matrix} Z_1 < Z_3 < \cdots < Z_{\mathrm{n-1}} \\ Z_2 < Z_4 < \cdots < Z_{\mathrm{n}} \end{matrix} \qquad (Z_1 > Z_{\mathrm{n}} \text{ when } Z_{\mathrm{S}} < Z_{\mathrm{L}}) \tag{8.45}$$

In Fig. 8.18(c), the total transformer length is shorter by a factor of 2 to 4 compared to the basic structure with quarterwave sections shown

in Fig. 8.18(a). However, it requires the use of a high impedance ratio for its sections reaching 30 to 50.

To reduce the high impedance ratio of transformers with a short total length, it is advisable to use the generalized structure shown in Fig. 8.18(d), representing cascaded even n sections of different lengths l_i and impedances Z_i. The optimum Chebyshev characteristics for this structure can be provided with the relationships between the lengths and characteristic impedances of its sections, in the form of [11]

$$\begin{aligned} l_i &= l_{n+1-i} \\ Z_i Z_{n+1-i} &= Z_S Z_L \end{aligned} \qquad i = 1, 2, \ldots, n/2 \tag{8.46}$$

and

$$Z_{n-1} > Z_{n-3} > \cdots > Z_1 > Z_n > Z_{n-2} > \cdots > Z_2 \tag{8.47}$$

where, in the direction from higher impedance Z_L to lower impedance Z_S, the impedances of both even and odd sections decrease, with the impedance of any odd section being always larger that that of any even section. The lengths of even sections decrease in the direction from the transmission line of smaller impedance, whereas the lengths of odd sections increase in the same direction.

Another structure for the stepped transmission-line transformer is shown in Fig. 8.18(e), for which Eq. (8.44) can be applied and for which

TABLE 8.3 Optimum Parameters for Different Four-Section Transformers

	Generalized structure, Fig. 8.18(c)					
$\lvert\Gamma\rvert_{min}$	$L_{1,2,3,4}$	Z_1, Ω	Z_2, Ω	Z_3, Ω	Z_4, Ω	L
0.065	0.0833	42.38	19.80	63.13	29.49	0.3330
0.071	0.0625	55.75	13.58	92.03	22.42	0.2500
0.074	0.0418	82.58	8.45	148.01	12.14	0.1670
0.076	0.0313	109.64	6.17	202.48	11.40	0.1250
	Equal-length structure, Fig. 8.18(d)					
	$L_{1,2}$	$L_{3,4}$	Z_1, Ω	Z_2, Ω	Z_3, Ω	Z_4, Ω	L
0.068	0.0625	0.0833	51.75	18.20	68.73	24.15	0.2916
0.070	0.0525	0.0725	62.00	15.28	81.85	20.15	0.2500
0.075	0.0320	0.0510	103.00	10.13	123.39	12.14	0.1660
0.076	0.0205	0.0420	152.90	7.78	160.95	8.18	0.1250
	New structure, Fig. 8.18(e)					
	$L_{1,2}$	$L_{3,4}$	Z_1, Ω	Z_2, Ω	L	
0.064	0.0479	0.1171	52.38	23.36	0.3330	
0.070	0.0405	0.0841	72.91	17.14	0.2500	
0.074	0.0282	0.0553	114.55	10.91	0.1670	
0.075	0.0213	0.0412	155.67	8.03	0.1250	

the same characteristic impedances for odd and even sections differ from the source and load impedances according to

$$\begin{aligned} Z_1 &= Z_3 = \cdots = Z_{n-1} \\ Z_2 &= Z_4 = \cdots = Z_n \end{aligned} \tag{8.48}$$

where $Z_1 Z_2 = Z_S Z_L$, $Z_n < Z_S$, and $Z_{n-1} > Z_L$ can reduce the total transformer length [11].

Table 8.3 gives the optimum parameters for different four-section transformers ($n = 4$) designed to match the transmission lines with impedances $Z_S = 25\ \Omega$ and $Z_L = 50\ \Omega$ in an octave frequency range, where the section lengths L_i and total length L are normalized to λ_0.

Lossy Matching Circuits

Dissipative or lossy gain compensation matching circuits can achieve the important tradeoffs between gain, reflection coefficient and bandwidth. Moreover, the resistive nature of such a matching circuit may also improve amplifier stability, and reduce its size and cost because it has a simple lossy matching circuit schematic. In many practical cases, to provide broadband matching with minimum gain flatness and input reflection coefficient, it is sufficient to use the resistive shunt element at the transistor input. An additional matching improvement with reference to upper frequencies can be achieved by employing inductive reactive elements in series to the resistor. For a broadband lossy match MOSFET high-power amplifier, it is advisable to use a series lumped inductance [13]; for the same type of a GaAs MESFET amplifier it is very convenient to use a short-circuited transmission line [14]. In addition, at higher frequencies it is possible to provide a pure resistive device input impedance with higher power gain by using an additional capacitance in parallel with the lumped inductance for monolithic application [15]. In this case, it is very important to optimize the elements of the lossy matching circuit in order to achieve minimum gain flatness over maximum frequency bandwidth. Consider such an approach for the example of the silicon MOSFET high-power amplifier.

The small-signal silicon MOSFET equivalent circuit is shown in Fig. 8.20. When the load resistance R_L is connected to the drain and source terminals, we can readily obtain an expression for the input device impedance in the form of

$$\begin{aligned} Z_{in} = R_g + \left(R_{gs} + \frac{1}{j\omega C_{gs}}\right) \Big/ \Bigg[1 + \frac{C_{gd}}{C_{gs}} \\ \times \frac{(1 + j\omega\tau_g)(1 + j\omega C_{ds} R_{L0}) + g_m R_{L0}}{1 + j\omega R_{L0}(C_{ds} + C_{gd})}\Bigg] \end{aligned} \tag{8.49}$$

where $R_{L0} = (R_L + R_d) / \left[1 + (R_L + R_d)/R_{ds}\right]$, $\tau_g = R_{gs} C_{gs}$.

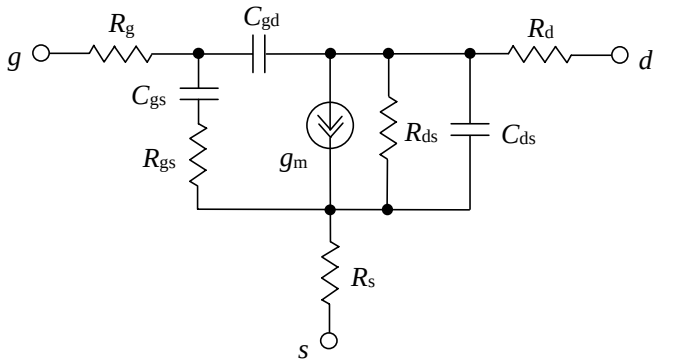

Figure 8.20 Small-signal silicon MOSFET equivalent circuit.

The circuit shown in Fig. 8.21(a) describes adequately the frequency behavior of such an input impedance. In Eq. (8.49), the series source resistance R_s and transit time τ are not taken into account due to their too small values for high-power MOSFETs in a frequency range of

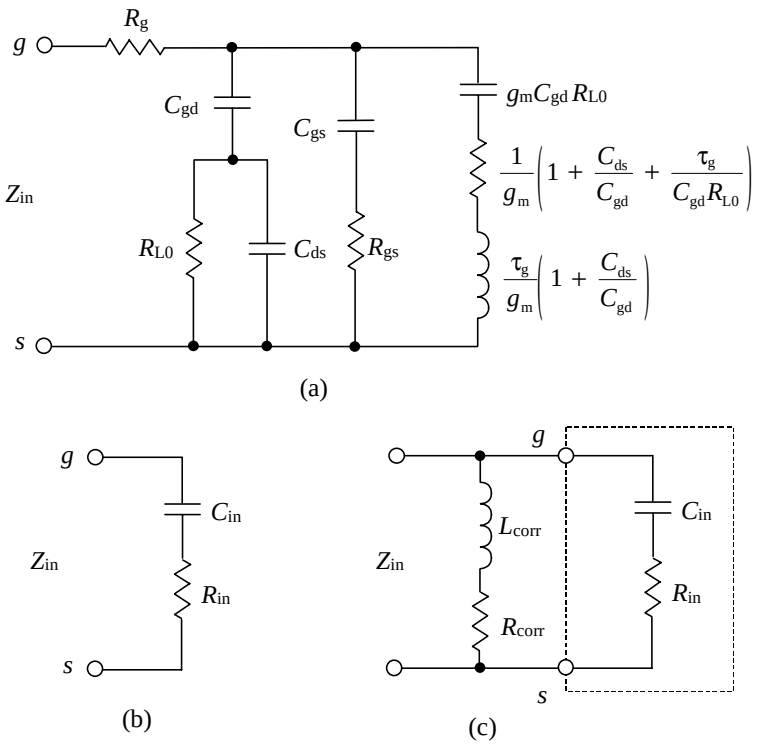

Figure 8.21 Equivalent circuits characterizing device input impedance.

$\omega \le 0.3\omega_T$, where $\omega_T = g_m/C_{gs}$. When $\omega\tau_g \le 0.3$ and the device output capacitive impedance is inductively compensated, the input equivalent circuit simplifies significantly and can represent a capacitance and a resistance connected in series (see Fig. 8.21(b)) with values of

$$R_{in} \cong R_g + R_{gs} \tag{8.50}$$

$$C_{in} \cong C_{gs} + C_{gd}\left[1 + g_m \frac{R_L + R_d}{1 + R_L/(R_{ds} + R_d)}\right] \tag{8.51}$$

To provide a constant real part of input impedance in a frequency range up to $0.1 f_T$, it is enough to use a simple lossy matching circuit. Such a series compensating input circuit, consisting of an inductance L_{corr} and a resistance R_{corr}, is shown in Fig. 8.21(c).

The total input impedance of both the lossy matching circuit and device input circuit is written as

$$Z_{in} = \frac{R_{corr} - \omega^2 C_{in} R_{in} L_{corr} + j\omega(L_{corr} + C_{in} R_{in} R_{corr})}{1 - \omega^2 L_{corr} C_{in} + j\omega C_{in}(R_{corr} + R_{in})} \tag{8.52}$$

Under the condition $R = R_{corr} = R_{in}$, the reactive part of the input impedance Z_{in} becomes zero, i.e., $X_{in} = 0$, when

$$L_{corr} = C_{in} R^2 \tag{8.53}$$

This leads to a pure active input impedance Z_{in} obtained by

$$Z_{in} = R = R_{in} \tag{8.54}$$

At microwaves, the short-circuited transmission line can be included instead of the inductance L_{corr} with the same input inductive reactance.

The low-frequency power gain G_P in dB is calculated using

$$G_P \cong 20 \log_{10}\left(\frac{g_m \sqrt{R_{corr} R_L}}{1 + (R_L + R_d)/R_{ds}}\right) \tag{8.55}$$

However, when the frequency increases, the voltage amplitude applied to the input capacitance C_{in} decreases. This leads to the appropriate decrease of the power gain G_P at higher bandwidth frequencies. Due to the rather small values of R_{in} for high-power MOSFETs, the value of G_P may not be high enough. Therefore, it should provide an additional impedance matching with lossless matching circuits in order to match with standard source impedance of 50 Ω or quite a high output impedance of the active device of the previous power amplifier stage.

Figure 8.22 shows the circuit schematic of the broadband LDMOSFET high-power amplifier with device geometry of 1.25 μm × 40 mm. The optimized input three-element lossy matching circuit allows a very

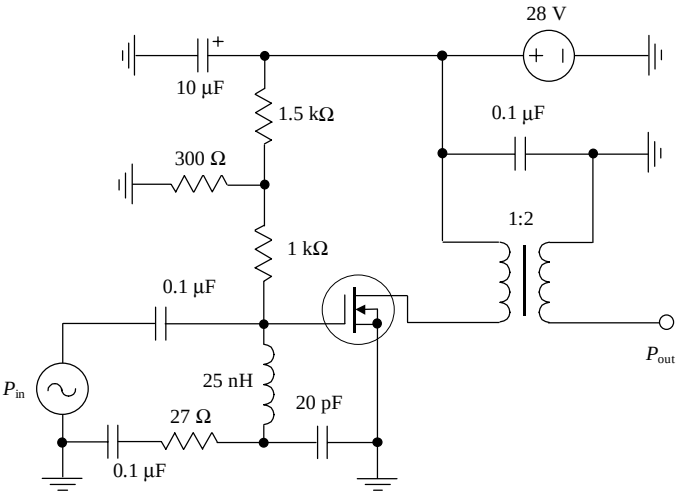

Figure 8.22 Circuit schematic of broadband LDMOSFET high-power amplifier.

broadband operation to be provided with minimum power gain flatness; the 1:2 output transformer contributes to an increase in the output power level. The capacitance of 20 pF connected in parallel with the resistance of 27 Ω provides an additional increase of power gain at higher bandwidth frequencies.

The simulation results are illustrated in Fig. 8.23, where the output power of 22 to 25 W with power gain of 13.7 ± 0.3 dB in a frequency

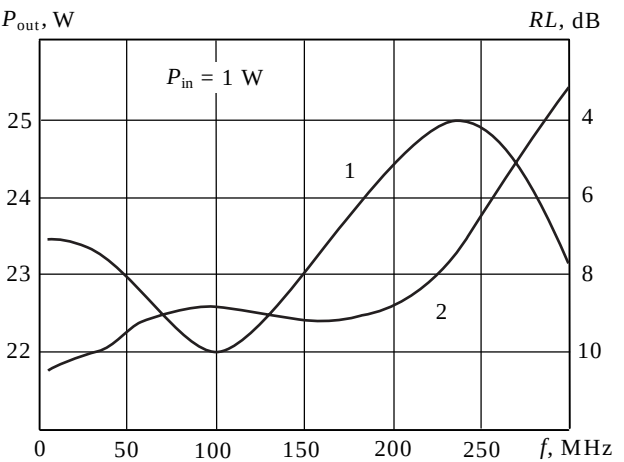

Figure 8.23 Output power and return losses versus bandwidth frequency.

range of 5 to 300 MHz can be realized (curve 1). The return losses are greater than 8 dB up to 225 MHz (curve 2). The direct connection of the standard 50-Ω load to the device drain terminal through the bypass capacitance gives the output power level in the range 6 to 7 W.

Practical Design Aspect

Multisection bandpass networks for input and output matching circuits provide wide frequency bandwidth with minimum power gain ripple and better harmonic suppression. Such a matching circuit configuration using lumped elements was applied for the design of a 60 W power amplifier operating in the frequency bandwidth of 140 to 180 MHz (see Fig. 8.24) [16]. To realize such technical requirements, the bipolar transistor BM100-28 (an internally matched device for VHF applications, which provides a 100 W output power level at a supply voltage of 28 V) was used. The input device impedance at the center frequency $f_c = \sqrt{140 \times 180} = 159$ MHz is $Z_{in} = (0.9 + j1.8)$ Ω. Therefore, the input matching circuit was designed as a three-section network with two low-pass sections and one high-pass section to minimize its quality factor Q. In this case, the device input lead inductance of $1.8/2\pi 0.159 = 1.8$ nH was considered as a series inductive element of the first low-pass section.

A similar design philosophy was used to design the output matching circuit when the three-section network maintains a value of the quality factor close to unity or within the $Q = 1$ circle on a Smith chart. The output device impedance is practically resistive of 1.65 Ω because the output device capacitive reactance is compensated by the device lead inductance. The series inductance of the first matching low-pass section

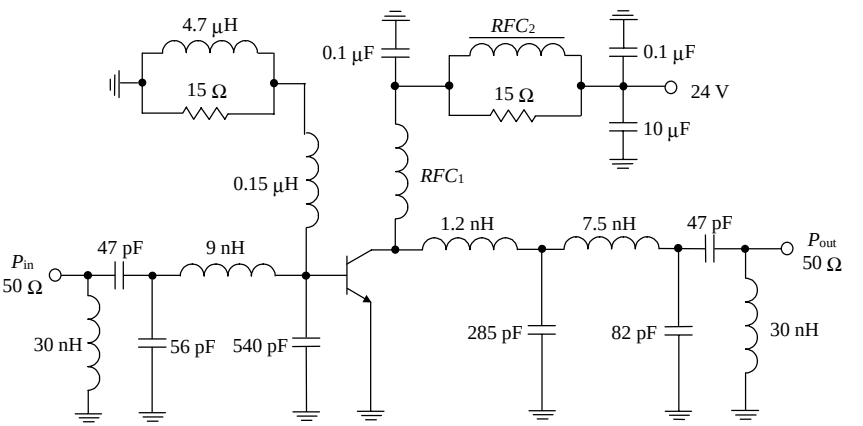

Figure 8.24 Bipolar 140–180 MHz high-power amplifier [16].

adjacent to the collector terminal, according to the Smith chart, can be realized as a section of 50-Ω microstrip line with electrical length of 0.011λ, where λ is the wavelength on the center bandwidth frequency. The physical length of this microstrip line for 1/16 inch Teflon fiberglass with a dielectric permittivity $\varepsilon_r = 2.55$ must be 0.51 inch whereas its width is 0.4 inch. As a result, the designed amplifier provides a power gain of at least 8 dB, gain ripple of less than 3 dB, more than 50 percent efficiency and input *VSWR* below 3:1.

At microwave frequencies, an increase of the number of transmission line transformer sections also improves the amplifier bandwidth characteristic. For example, with the use of a multisection transformer with seven quarter-wavelength transmission lines of different characteristic impedances, a power gain of 9 ± 1 dB and power-added efficiency (PAE) of 37.5 ± 7.5 percent over 5 to 10 GHz was achieved for a 15 W GaAs MESFET power amplifier [17]. The simplified schematic diagram of such an amplifier is shown in Fig. 8.25. To achieve minimum output power flatness, the number of sections of the output matching circuit is determined to compensate for the frequency-dependent device power gain based on load-pull measurements. At the same time, the number of sections of the input matching circuit compensates for the frequency-dependent gain based on small-signal *S*-parameter measurements. For the 5.25 mm GaAs MESFET device, the values of the input and output impedances derived from its large-signal model were assumed resistive and equal to $Z_{in} = 0.075\ \Omega$ and $Z_{out} = 1.32\ \Omega$, respectively. To achieve minimum gain flatness, the length of each microstrip section was initially chosen as a quarter wavelength at the highest frequency of 10 GHz. However, because the input and output device impedances are not pure resistive in reality, the final optimized length of each microstrip section was reduced to be a quarter wavelength at around 15 GHz. The microstrip transformer sections L_1-L_6 and L_9-L_{14} were fabricated on alumina substrate with dielectric permittivity $\varepsilon_r = 9.8$ and thickness of 0.635 mm for L_1 and L_2, 0.2 mm for L_3-L_6 and L_{10}-L_{12}, and 0.38 mm for L_{13}-L_{14}. Microstrip section L_7 was realized on high dielectric substrate

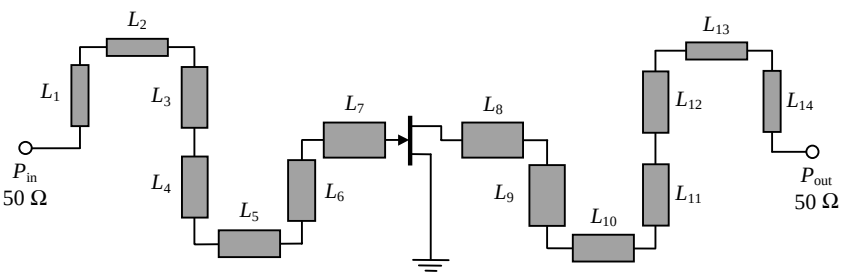

Figure 8.25 Microstrip 5–10 GHz 15 W GaAs MESFET power amplifier.

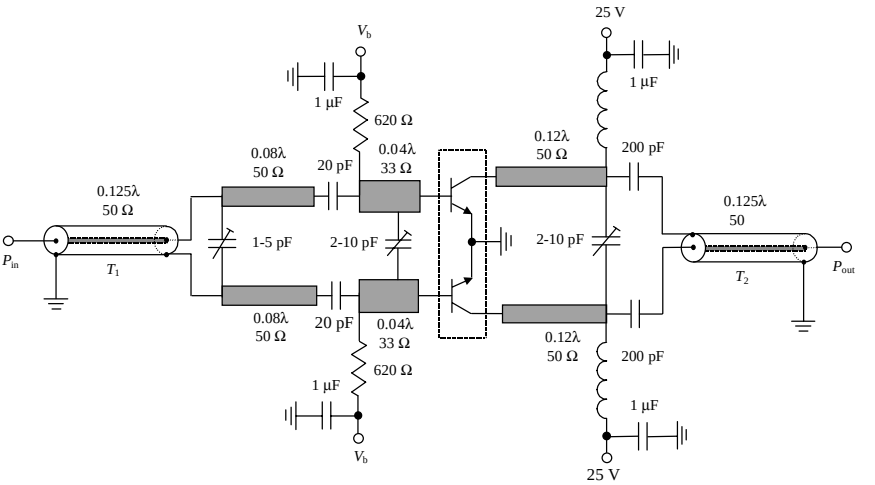

Figure 8.26 Circuit schematic of bipolar UHF power amplifier for TV applications.

with $\varepsilon_r = 38$ and a thickness of 0.18 mm, whereas microstrip sections L_8 and L_9 were fabricated on the high dielectric substrate with $\varepsilon_r = 89$ and thickness of 0.15 mm. The final power amplifier represents a balanced configuration of two 5.25 mm GaAs MESFETs with quadrature couplers.

The broadband power amplifier shown in Fig. 8.26 is intended for TV transponders with complex video and audio TV signal amplification in the frequency bandwidth of 470 to 790 MHz. The power amplifier is practically realized on copper-clad epoxy glass laminate with $\varepsilon_r = 4.7$ of 1.5 mm thickness. The lengths of the microstrip lines are given in terms of their lengths on the high-bandwidth frequency, and the *RFC* chokes represent three-wire air inductors. The device input and output impedances measured at the base and collector terminals at 600 MHz are $Z_{in} = (6 + j4)\ \Omega$ and $Z_{out} = (15 + j17.5)\ \Omega$, respectively, which allows the use of a two-section input matching circuit and single-section output matching circuit. In Class A operation, such a power amplifier using a balanced TPV-595A bipolar transistor provides a linear output power of 7 W, and a power gain of about 12 dB for a quiescent collector current of 1.3 A.

The high-power amplifier intended for applications in TV transmitters, using the balanced bipolar transistor BLV861, is shown in Fig. 8.27 [18]. In Class AB operation with a quiescent current of 100 mA, it covers the frequency bandwidth of 470 to 860 MHz with an output power of 100 W, a power gain of about 9.5 dB with a gain ripple of ± 0.5 dB and an efficiency of 55 percent. The device input and output impedances at 663 MHz are $Z_{in} = (4.4 + j7.9)\ \Omega$ and $Z_{out} = (8.8 - j3.65)\ \Omega$, respectively, for the three-section input matching circuit and two-section output

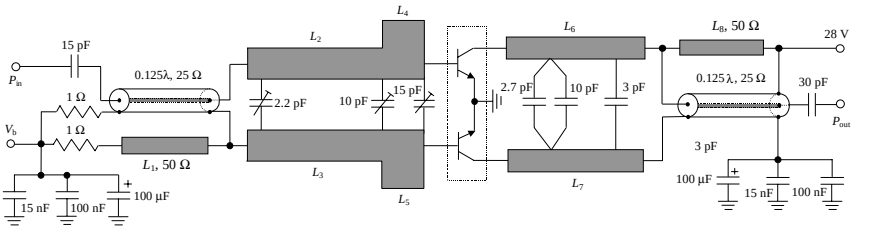

Figure 8.27 Bipolar high-power UHF amplifier intended for TV transmitters [18].

matching circuit that are used. The unbalanced-to-balanced transformation to 50 Ω is realized by 1:2 balun transformers, each of which is represented by a 25-Ω semirigid coax cable with an electrical length of 45° at the midband and a diameter of 1.8 mm, soldered over the whole length on top of the same length microstrip line. For low-frequency stability enhancements, the input balun stubs are connected to the bias point by means of 1-Ω series resistors. Large value electrolytic capacitors are added at the input and output biasing points to improve the amplifier video response. The amplifier is fabricated by using printed circuit board laminate PTFE glass with $\varepsilon_r = 2.55$ and a thickness of 0.51 mm (20 mils).

Figure 8.28 presents the schematic diagram of a two-octave wideband high-power amplifier covering both the civil and military airbands in a frequency range of 100 to 450 MHz [19]. The BLF548 device is a balanced *n*-channel enhancement mode VDMOS transistor designed for use in broadband amplifiers with an output power of 150 W and a power gain of more than 10 dB in a frequency range of up to 500 MHz. In a frequency range of 100 to 500 MHz, the real part of the input impedance

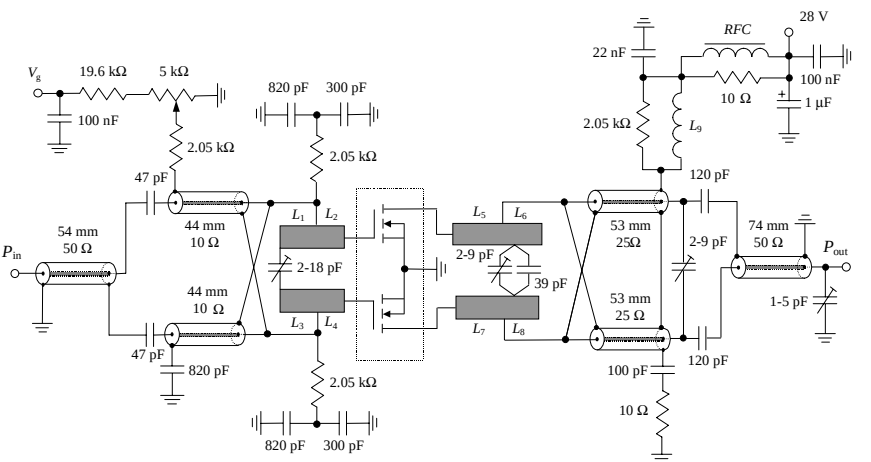

Figure 8.28 Schematical diagram of wideband high-power VHF MOSFET amplifier [19].

is practically constant and equal to $\mathrm{Re}Z_{\mathrm{in}} = 0.43\ \Omega$, whereas the imaginary part of the input impedance changes its capacitive impedance $\mathrm{Im}Z_{\mathrm{in}} = -4.1\ \Omega$ at 100 MHz to the inductive impedance $\mathrm{Im}Z_{\mathrm{in}} = 0.5\ \Omega$ at 500 MHz. The output impedance is capacitive and equal to $Z_{\mathrm{out}} = (1.1 - j0.8)\ \Omega$ at the high bandwidth frequency of 500 MHz. Coaxial semirigid baluns are used to transform the unbalanced 50 Ω source and load into two opposite 180° phase 25 Ω sections, respectively, followed by coaxial transformers, with the characteristic impedance of 10 Ω for input matching and of 25 Ω for output matching. This yields the lower impedance $R_{\mathrm{in}} = \sqrt{25 \times 10}/4 = 3.9\ \Omega$, which is necessary to transform to the device input resistance of 0.43 Ω, and the higher impedance $R_{\mathrm{out}} = \sqrt{25 \times 25}/4 = 6.2\ \Omega$, which is necessary to transform to the device output resistance of 2.8 Ω. Final matching is provided by simple L-transformers with series microstrip lines and parallel variable capacitors. The microstrip lines were realized on a double copper-clad fiberglass PCB with dielectric permittivity $\varepsilon_{\mathrm{r}} = 2.2$ and a thickness of 1/32 inch. In this case, the dimensions of each microstrip line with characteristic impedance of 20 Ω are as follows: L_1 and L_3 are 5 × 8 mm, L_2 and L_4 are 2.5 × 8 mm, L_5 and L_7 are 11.5 × 8 mm, and L_6 and L_8 are 4 × 8 mm. In order to compensate for the 6 dB/octave slope, conjugate matching is achieved at 450 MHz since at lower frequencies a mismatch gives the required decrease of power gain necessary to provide an acceptable broadband power gain flatness. As a result, in the frequency range of 100 to 450 MHz, the gain ripple is smaller than 1 dB at the output power level of 150 W. At the same time the input return loss is better than 12 dB.

Figure 8.29 shows the circuit schematic of a linear MOSFET power amplifier designed for a multioctave frequency bandwidth of 1.5 to 60 MHz with a 50-W output power and a power gain within 23 ± 1 dB.

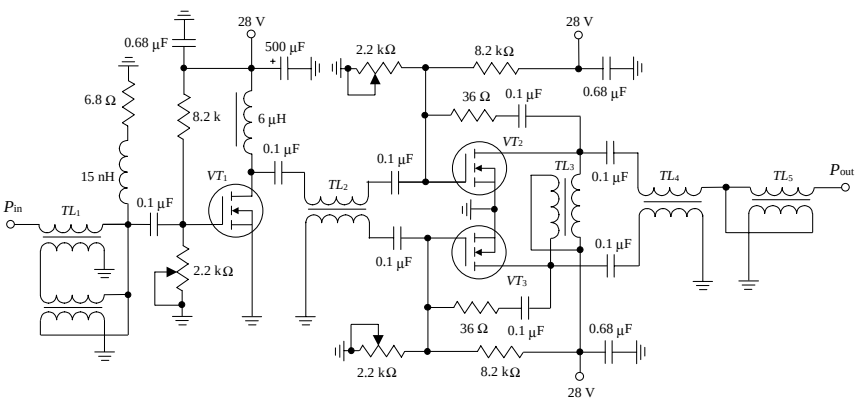

Figure 8.29 Circuit schematic of multioctave linear MOSFET HF-VHF power amplifier.

Using negative feedback resistors of 36 Ω in the final stage allows the power amplifier nonlinearity to be improved and reduces the level of the third-order intermodulation components down to −45 dBc. An asymmetrical 3:1 transformer using a 17-Ω stripline and a ferrite core with permeability $\mu = 400$ provides the input impedance transformation. An increased value of the ferrite core permeability is necessary to reduce the cable length to about 10 to 15 cm, providing a significantly higher inductive impedance of the transformer primary winding, of about 10 times the standard source 50-Ω impedance, at a low bandwidth frequency. Due to the 36-Ω resistive feedback, the input impedance of each device should be 6.25 Ω. In this case, it is sufficient to use an unbalanced-to-balanced 1:1 transformer with a 12.5-Ω stripline characteristic impedance, and provide a load for the driver stage MOSFET device of 12.5 Ω. Using a transformer TL_3 contributes to the effective push-pull operation with even harmonic suppression. In addition, from a viewpoint of the circuit simplicity, it is convenient to use its common terminal for the drain voltage supply. The output transformation is achieved by using a balanced-to-unbalanced 1:1 transformer TL_4 that converts an output impedance of each MOSFET device designed for push-pull operation to 12.5 Ω, and an asymmetrical 1:2 transformer TL_5 to transform 12.5 Ω to the standard load 50-Ω impedance.

Figure 8.30 shows a bipolar VHF broadband high-power amplifier designed for broadcast FM transmitters in a frequency range of 66 to

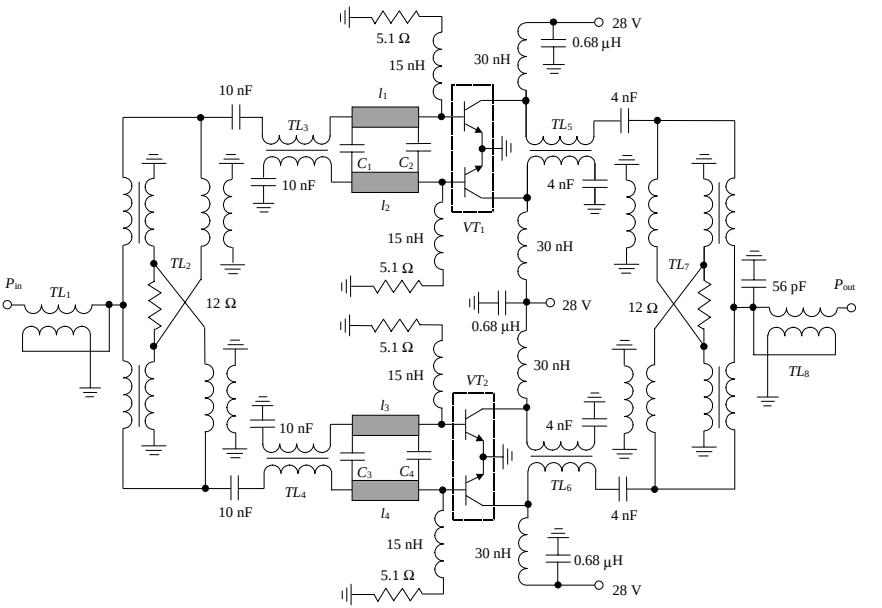

Figure 8.30 Bipolar VHF broadband high-power amplifier for broadcast FM transmitters.

108 MHz. When using the NEC 2SC3812 or Thomson SD1483 bipolar balanced transistors in a Class C operation, an output power of 350 W with a power gain within 11 ± 1 dB and power-added efficiency of about 60 percent can be realized in a whole frequency bandwidth. An appropriate negative biasing in a Class C operation is achieved by using the series resistors of 5.1 Ω in the base-emitter bias circuit together with the series inductances of about 15 nH, which is necessary to realize minimum gain ripple. The asymmetrical 2:1 input TL_1 and 1:2 output TL_8 transformers with the coaxial cable characteristic impedance of 25 Ω are used to convert 12.5 Ω to standard source and load 50-Ω impedance, respectively. The unbalanced-to-balanced transformers TL_3–TL_6 with the stripline characteristic impedances of 6 Ω are necessary to provide the 3-Ω source and load impedances for each part of the balanced bipolar transistors. Due to the small value of the device single-ended input impedance of about 1 Ω with the inductive component, the additional input two-section *L*-type impedance matching circuits are used. Here, the series microstrip lines l_1–l_4 are the inductive elements for the fist section, and the device lead inductances are the inductive elements for the second section. Power-dividing at the input as well as power-combining at the output of the high-power amplifier is realized by hybrid power splitters/combiners TL_2 and TL_7, each with 12-Ω ballast resistors and striplines with the characteristic impedances of 12.5 Ω. Such a hybrid power splitter/combiner provides excellent device–device isolation isolation and contributes to stable amplifier operation.

The circuit schematic of the input, interstage and output networks intended for microwave broadband power amplifiers are presented in Fig. 8.31. The constant-resistance input network shown in Fig. 8.31(*a*) provides the input device impedance pure resistive and equal to $Z_{\text{in}} = R_{\text{in}}$, when $L_1 = C_{\text{gs}}R_{\text{in}}^2$, $C_1 = L_{\text{g}}/R_{\text{in}}^2$ and $R_1 = R_{\text{in}}$, that makes wideband transformation of the input resistance to the source resistance much easier. In the output network presented in Fig. 8.31(*b*), a value of the drain inductance is chosen to compensate for the capacitive device output reactance at the center bandwidth frequency. Then, a resonant frequency of the parallel resonant circuit is set to be equal to the same center bandwidth frequency. In this case, for the frequencies where device output impedance Z_{d} is capacitive, the impedance of the parallel resonant circuit is inductive. On the other hand, for the frequencies where impedance Z_{d} is inductive, the impedance of the parallel resonant circuit is capacitive. As a result, the wideband reactance compensation is realized when the reactive part of the impedance Z_{d} becomes smaller over a wide frequency bandwidth. For microwave applications, such a parallel resonant circuit is fabricated by using a quarterwave short-circuited stub. The interstage network, the schematic diagram

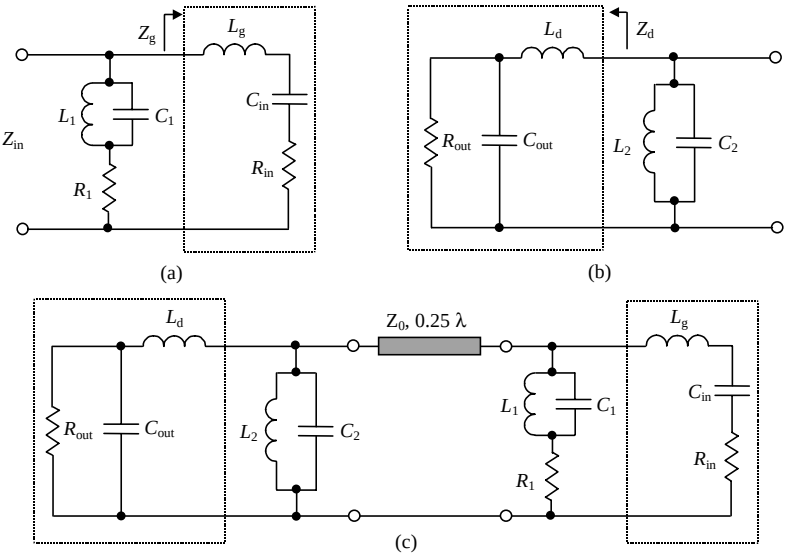

Figure 8.31 Schematic of (*a*) input, (*b*) output, and (*c*) interstage broadband matching circuits.

for which is shown in Fig. 8.31(*c*), is comprised of the input and output networks described above and a quarterwave microstrip transformer with the characteristic impedance $Z_0 = \sqrt{R_{in}L_d/R_{out}C_{out}}$.

A schematic diagram of the two-stage lossy match MESFET power amplifier is shown in Fig. 8.32 [15]. By using a 1.05-mm device in the driver stage and two 1.35-mm devices in the final stage, saturated output power was 27.7 ± 2.7 dBm, linear power gain was 8.3 ± 2.8 dB and a drain efficiency of 15.3 ± 8.3 percent was realized in a frequency range of 4 to 25 GHz. The input and interstage constant-resistance networks are each represented by the series connections of a resistance and an inductance, which is fabricated by using a high-impedance microstrip line. In Fig. 8.32, two such networks connected in parallel provide input pure resistive impedance, where l_4 and l_5 are the series microstrip lines, and R_1 and R_2 are the series resistances. The short-circuited microstrip lines—l_7 and l_8 in the interstage network and l_{19} and l_{21} in the output network—with quarterwave electrical lengths at the center frequency realize the parallel resonant circuits connected at the device output terminals. The microstrip lines l_{10} and l_{14} in the interstage network are the quarterwave impedance transformers, which provide matching between the output impedance of the driver-stage device and the input impedance of the second-stage devices connected in parallel. The input and output matching circuits are realized in the form of *T*-transformers, where a series microstrip line and parallel open-circuited

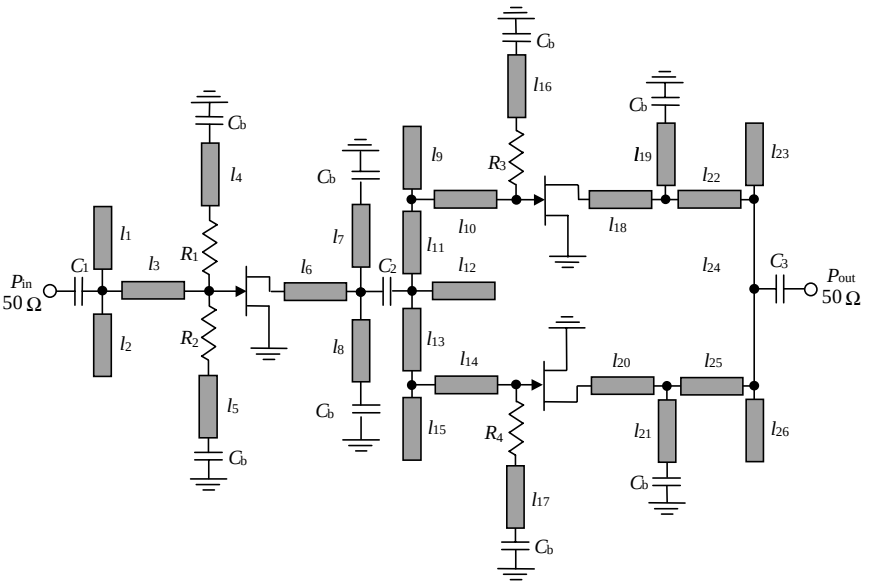

Figure 8.32 Microstrip two-stage lossy match MESFET power amplifier.

microstrip stub replace a series inductance and a parallel capacitance, respectively.

The output matching circuit can be also represented as a series combination of the impedance π-type matching network and a lossy gain network, as shown in Fig. 8.33 [20]. For both bipolar and MESFET broadband amplifiers, the parallel capacitances for a π-type network are the device output capacitance and open-circuited microstrip stub, which are connected to each side of a series lumped inductance, respectively. The output network for lossy gain compensation is connected between the impedance matching circuit and the load. This configuration is usually used for medium power, very broadband amplifiers. For example, the two-stage cascade of the *L*-band broadband bipolar amplifier shown in Fig. 8.33(*a*) was designed for a minimum input reflection coefficient with 1.78:1 *VSWR* and a maximum gain variation of ± 1.2 dB, around 16.5-dB power gain over the 1.0-to 2.0-GHz frequency range. The two-stage cascade of the microwave MESFET amplifier shown in Fig. 8.33(*b*) was designed for maximum flat gain in a frequency range of 4.0 to 6.0 GHz when the power gain varies within 15.4 ± 0.5 dB. To provide minimum losses at high bandwidth frequency, the short-circuited microstrip line in the output lossy gain circuit was chosen to be of a quarter wavelength for each amplifier.

Figure 8.34 shows the circuit schematic of the broadband GaN HEMT microwave power amplifier with the device geometry of 0.7 μm × 1 mm,

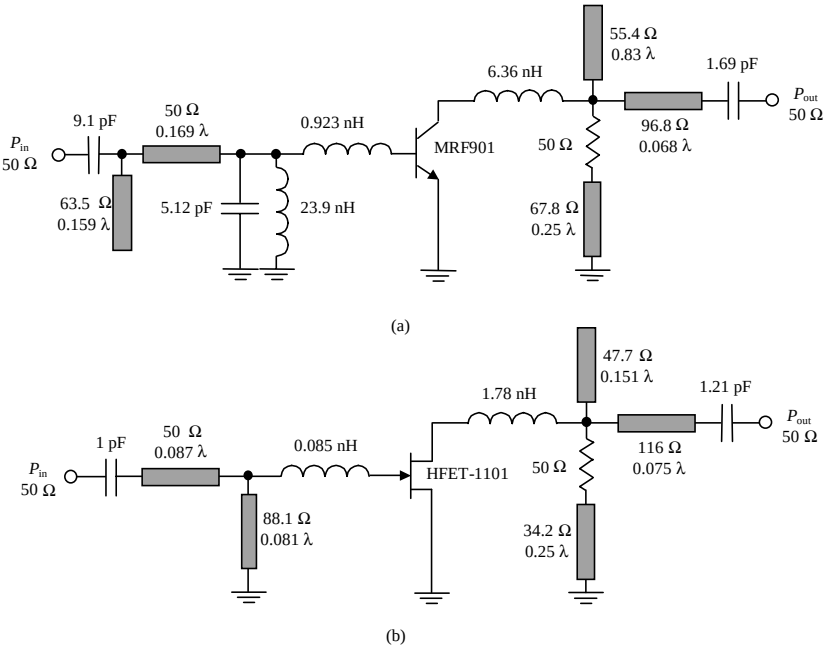

Figure 8.33 Broadband microstrip lossy match (*a*) bipolar and (*b*) MESFET power amplifiers [20].

transition frequency $f_T = 18$ GHz and maximum frequency $f_{max} = 35$ Hz. The optimized input three-element lossy *LCR* matching circuit provides a power gain up to 11.5 dB and low input reflection less than –10 dB over a frequency range of 3 to 9 GHz [21]. As the impedance at the input of the lossy matching circuit is only about 10 Ω, this

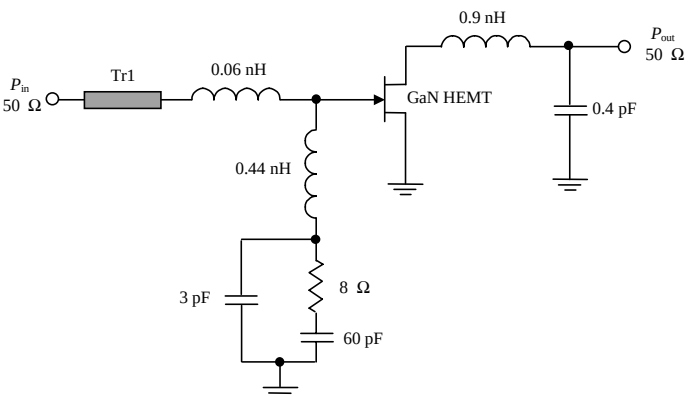

Figure 8.34 Schematic of 3 to 9 GHz GaN HEMT broadband power amplifier [21].

necessitates an additional 50 Ω to 10 Ω broadband impedance transformation (Tr1), which was realized using a few sections of quarterwave coplanar transmission lines with decreasing impedance. The output network incorporates an *LC* circuit to compensate the output device capacitance such that the intrinsic device sees approximately a real load within the frequency bandwidth. As the optimum load for this 1-mm device with supply voltage of 20 V is of about 50 Ω, no output impedance transformation is needed. The output power was of about 1.6 W, with the power-added efficiency within the range of 14 to 24 percent in a 4-to 8-GHz bandwidth.

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Chapter

9

Power Amplifier Design for Communication Systems

In modern telecommunication systems, it is very important to realize both high-efficiency and linear operation of the power amplifiers. This chapter describes a variety of techniques and approaches that can improve the power amplifier performance. To increase efficiency, the Kahn envelope elimination and restoration and envelope tracking techniques, Doherty and outphasing power amplifier architectures as well as switched-mode and dual-path power amplifier configurations are discussed and analyzed. There are several linearization techniques that provide linearization of both entire transmitter systems and handset power amplifiers. Feedforward correction is a technology for satellite and cellular base station applications to achieve the high linearity levels of -75 dBc and better. The practical realization of such a technique is quite complicated and very sensitive to the feedback loop imbalance as well as to the parameters of its separate components. Predistortion technique is the simplest form of power amplifier linearization and can be used for handset application, although significant linearity improvement is difficult to realize. The choice of a proper high-efficiency approach or linearity correction scheme depends on performance tradeoffs as well as manufacturing capabilities. Finally, the design and implementation of the monolithic integrated circuits of HBT and CMOS power amplifiers for handset application are considered and illustrated.

Kahn Envelope Elimination and Restoration Technique

Modern wireless communication systems require that the signal is fed with a nonconstant envelope through the power amplifier. In this case, there is a tradeoff between power amplifier efficiency and linearity, with improvement in one coming at the expense of the other. In a traditional analog envelope elimination and restoration (EER) approach, where special devices are required to separate the amplitude (envelope) and RF phase-modulated signals, one type of power amplifier is responsible for envelope signal amplification, while another type of power amplifier is fed by a constant-envelope RF signal as shown in Fig. 9.1(*a*). The constant-envelope RF signal can be amplified efficiently by a nonlinear power amplifier (PA) using Class B, Class E or Class F operation mode. Amplitude modulation of the final stage of the power amplifier restores the envelope to the phase-modulated carrier signal creating an amplitude replica of the input signal. This technique was first developed by

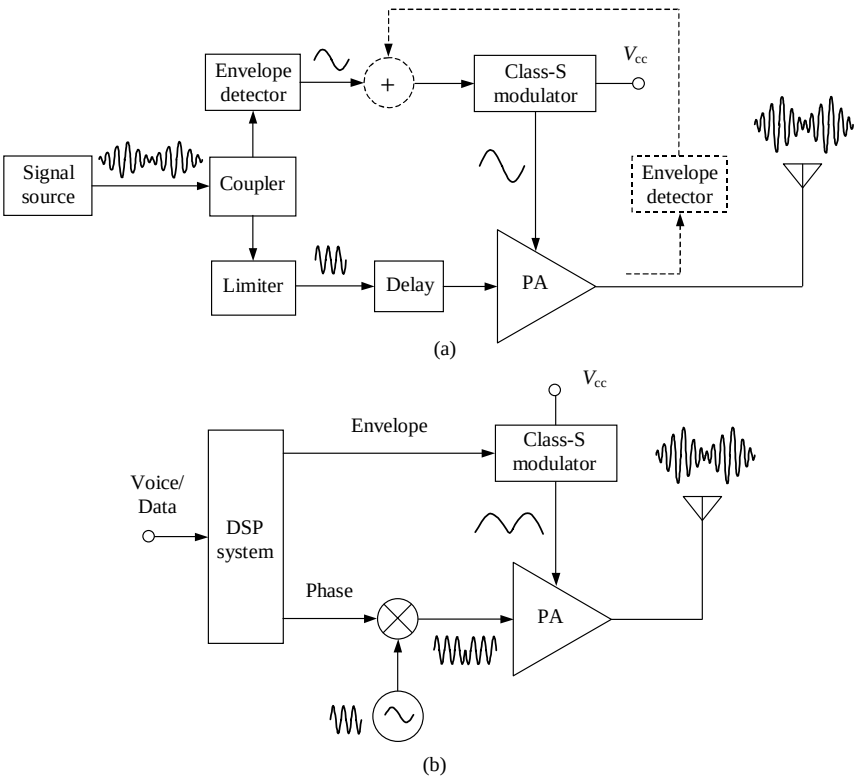

Figure 9.1 Block diagrams of Kahn EER transmitters.

Kahn in the 1950s to improve the efficiency of short-wave broadcast transmitters [1]. In contrast to linear power amplifiers, a Kahn EER transmitter operates with high efficiency over a wide dynamic range of backoff output power levels and, therefore, produces an average efficiency that is three to five times higher [2, 3]. To minimize misalignment between phase and amplitude, a delay line is required. Adding the output envelope feedback circuit allows the intermodulation distortion to be reduced [4]. In modern transmitters for wireless applications, both the envelope and phase-modulated signals can be easily generated separately using the digital signal processing (DSP) technique shown in Fig. 9.1(*b*). Then, the phase-modulated signal with constant envelope is upconverted to the desired output RF frequency using a direct or double conversion scheme. For a direct conversion scheme, the baseband signal containing the phase information directly modulates the RF carrier.

A Class-S modulator is a high-efficiency low-frequency power amplifier based on pulse-width modulation, and its output is a baseband envelope signal including a dc component [3, 4]. Such a modulator produces only positive output current and therefore requires only a single transistor and a single diode, which is required to provide a suitable reverse-direction path, as shown in Fig. 9.2. The output voltage can have any value between nearly zero voltage and the supply voltage V_{cc}. The low-pass filter (LPF) should have a high impedance to the switching frequency and its harmonics to provide a high level of spectral purity of the output RF signal. Usually, it is preferable to use a first-order LPF, since further increasing the number of its elements improves the modulator performance insignificantly but significantly increases the size and complexity of a Class-S modulator. When the transistor is open, the supply voltage V_{cc} is connected to the input of the LPF and the load current flows through the device. When the transistor is closed, the load current flows through the diode and the voltage at the LPF

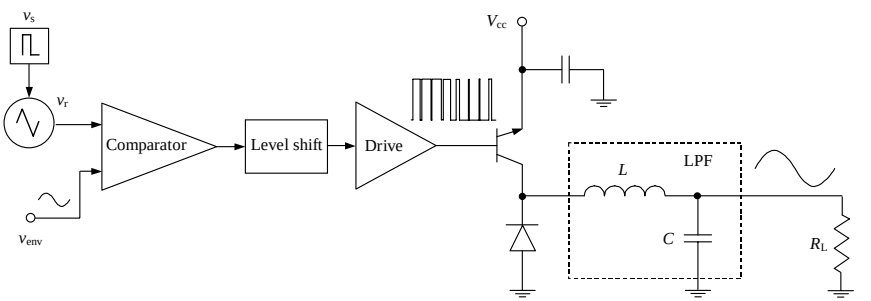

Figure 9.2 Schematic of class-S modulator.

input is equal to the voltage across the open diode. For an ideal operation, the active device never experiences simultaneous nonzero voltage and nonzero current, resulting in 100 percent efficiency. However, in practice the losses in the diode and transistor, due to the finite values of their on-saturation resistances and finite time between on- and off-operation modes, degrade efficiency, especially at higher operation frequencies. To minimize the intermodulation distortion of the envelope signal, it is necessary to choose correctly the LPF parameters providing a maximally flat frequency response, which can be calculated by

$$L = 0.7\frac{R_{\mathrm{L}}}{\pi f_{\mathrm{c}}} \qquad C = \frac{1}{2.8\pi f_{\mathrm{c}} R_{\mathrm{L}}} \tag{9.1}$$

where f_{c} is the cutoff frequency of the low-pass filter.

The pulse-width modulated (PWM) signal can be accomplished by several techniques, the most popular of which is a comparator method (see Fig. 9.2). Comparison of the envelope input to a triangular reference wave shown in Fig. 9.3(*b*) by a comparator produces a PWM switching signal, the width of which varies with envelope amplitude, as shown in Fig. 9.3(*c*). The comparator produces maximum output when the input signal is larger than the triangular wave and zero output when the input signal is smaller than triangular wave. The triangular wave can be supplied directly from a function-generator circuit or obtained by integration of the output of a square-wave switching generator (see Fig. 9.3(*a*)). The maximum modulation frequency depends strongly on the switching (clock) frequency required for a PWM process. To keep the spurious products in the output spectrum at least 30 or 40 dB below the carrier, the switching frequency must four or five times exceed the highest modulation frequency; in practice, to restore the input envelope with the minimum level of intermodulation components using an LPF (see Fig. 9.3(*d*)), it is better to use a factor of 10. An efficiency of about 90 percent can be achieved for a Class-S modulator with an envelope bandwidth up to 150 kHz [4, 5]. However, a PWM is an inherently nonlinear process that generates intermodulation components with as higher level as wider RF signal bandwidth [6].

Therefore, for the EER systems with wider bandwidths and stronger requirements for the intermodulation distortion levels, it is preferable to use a Class-S modulator based on the delta-sigma modulation scheme. For the same switching frequency (or oversampling ratio), a system based on delta-sigma modulation can provide wider bandwidth and lower distortion than a PWM system. The signal in a delta-sigma modulator is digitized by a quantizer (single-bit comparator), the output of which is subtracted from the input signal through a digital feedback loop acting as a bandpass filter, and quantization noise is forced outside the pass band. The degree of suppression of the quantization noise

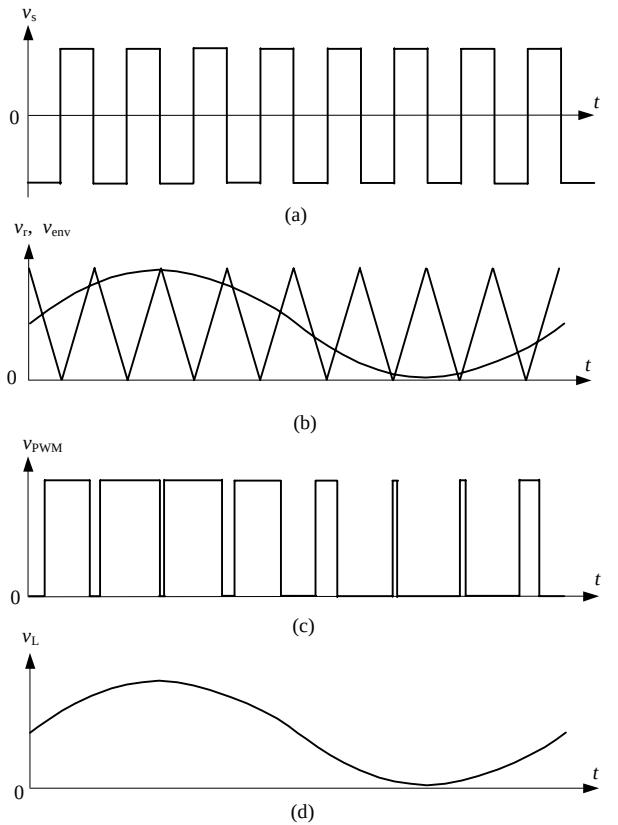

Figure 9.3 Waveforms of pulse-width modulation of envelope signal.

depends on the oversampling ratio, which is the ratio of the digital clock frequency to the RF bandwidth. Applying a 0.8-μm CMOS technology can provide a sufficiently high efficiency over a wide range of backoff output powers, with overall efficiency of 33 percent at 28 dBm of linear output power using an RF CMOS power amplifier (designed for cellular handset applications) having a maximum power of 1 W and power-added efficiency of 42 percent [7].

There are several limitations of a traditional Kahn EER architecture for practical implementation. The transfer characteristic of the RF power transistor should be linear enough to restore accurately the input envelope. However, in practice this is not the case, especially for high-power devices. Besides, the size of a Class-S modulator is sufficiently large for microwave monolithic integrated circuit (MMIC) implementation, and it becomes too inefficient at high frequencies. Also, a high degree of amplitude and phase tracking is required in order to achieve a

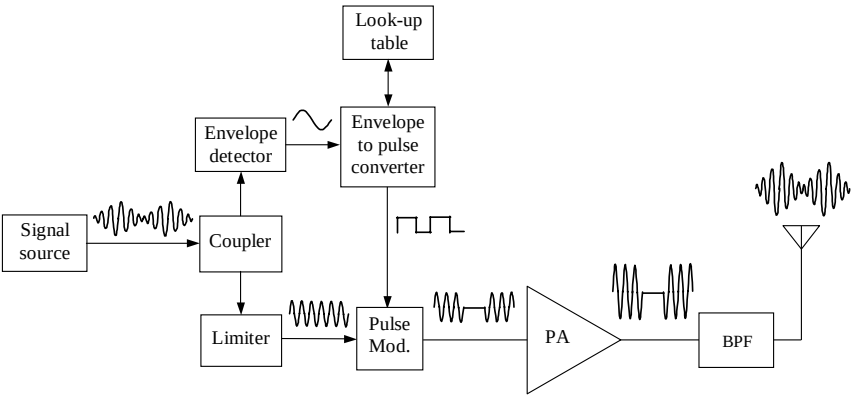

Figure 9.4 Transmitter architecture with pulse-width carrier modulation.

high depth of modulation. For instance, a combination of 0.2 dB amplitude and 3° of phase tracking error will result in a maximum modulation dynamic range of 20 dB. To obtain the carrier-to-intermodulation ratio of $C/I \geq 30$ dBc, the differential time delay (Δt) between the envelope and phase-modulated paths, measured in seconds, must be small, as defined by $\Delta t \leq 0.1/B_{\text{RF}}$, where B_{RF} is the bandwidth of the RF signal [6]. Finally, there should be a tradeoff between the switching frequency in the Class-S modulator and the order of the low-pass filter in order to minimize the intermodulation distortion.

Figure 9.4 shows an architecture with pulse-width carrier modulation, which is an alternative to a conventional Kahn EER technique [8]. The phase-modulated input signal with a nonconstant envelope is split by a coupler into separate envelope and phase-modulated components that use an envelope detector and limiter. Then, the envelope is converted to duty factor variations of pulse train, typically at a sampling rate at least an order of magnitude higher in frequency than the maximum frequency of the envelope. The pulse train is applied as pulse-width modulation onto a carrier RF phase-modulated signal using a pulse modulator. The combined signal is transmitted to a high-efficiency nonlinear power amplifier. Unwanted sidebands caused by the sampling process are rejected by bandpass filter (BPF) at the amplifier output to pass only the carrier and its modulated signal bandwidth and hence recover a linear replica of the original source signal. Use of a look-up table in the envelope to pulse modulation circuitry can be useful to maximize the envelope dynamic range by proper adjustment of the pulse width and the sampling period. Both the envelope and phase-modulated signals can also be generated separately using the DSP technique, and digitization of the envelope signal can be provided by a delta-sigma modulator with a sampling rate of ten times the RF

bandwidth [9]. The main disadvantage of such systems is the high level of insertion losses of the narrow-band BPF, the quality factor of which should be very high to minimize the switching frequency sidebands. Nevertheless, in some particular cases, it is possible to realize a compromise solution between BPF losses and switching frequency that results in a higher average efficiency for signals with nonconstant envelope than can be achieved by the systems at backoff output power levels using linear power amplifiers.

Envelope Tracking

The collector (drain) efficiency of a power amplifier can be analytically obtained from (see also Chap. 6)

$$\eta = \frac{P_1}{P_0} = \frac{1}{2}\frac{I_1}{I_0}\frac{V}{V_{cc}} \tag{9.2}$$

where $P_1 = I_1 V$ is the output power at the fundamental frequency, $P_0 = I_0 V_{cc}$ is the dc power, I_1 is the fundamental current amplitude, I_0 is the dc current, V is the fundamental collector voltage amplitude and V_{cc} is the collector supply voltage.

For the operation conditions with the same conduction angle (for example, in Class B, the conduction angle is equal to 180° regardless of the collector current amplitude I), the current ratio between the fundamental and dc components, I_1/I_0, keeps a constant value. Generally, depending on the conduction angle, the current ratio I_1/I_0 varies from 1 in Class A with 360° conduction angle to 2 for the ideal limiting case of Class C with 0° conduction angle. For Class B operation, the current ratio I_1/I_0 is equal to 1.57. Consequently, for nearly Class B operation when the value of the conduction angle deviates from 180° by not too much, the current ratio I_1/I_0 varies within a small range of 10 to 20 percent. Thus, as follows from Eq. (9.2), the main factor of collector efficiency improvement at backoff output power levels is the voltage ratio V/V_{cc}, which should be kept constant for different output power levels. This can be achieved by reducing the supply voltage V_{cc} using envelope tracking technique or increasing the load resistance (the stronger slope of the load line in Fig. 9.30).

Since the collector efficiency is proportional to the ratio of the fundamental amplitude to the dc supply voltage, it becomes extremely small already at output powers of 10 dB less than peak power, provided that the load and dc supply voltage are kept constant. However, normally for CDMA2000 or WCDMA transmitters, the output power can vary in a wide dynamic range of about 80 dB with maximum statistically averaged transmitting power required to deliver signal to the base station of about 15 to 25 dB less than the peak output power. Therefore, the

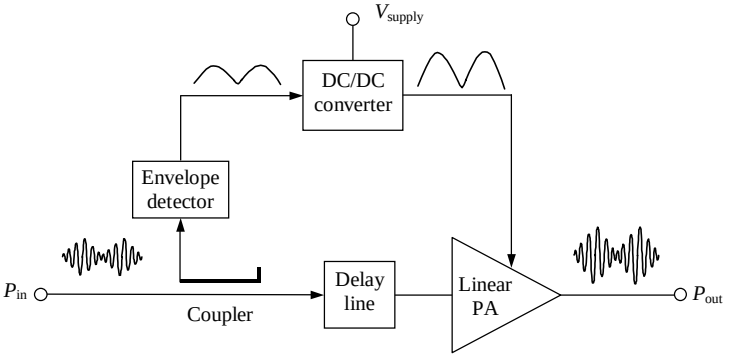

Figure 9.5 Power amplifier envelope-tracking architecture with analog control.

envelope-tracking technique can be very useful to increase power amplifier efficiency in a wide range of output powers by varying the dc supply voltage according to the RF signal envelope.

Figure 9.5 shows the power amplifier envelope-tracking architecture with analog control where the envelope detector is used at the input to detect the signal envelope [10 to 12]. Here, a dc-dc converter is used to provide the dynamically controlled supply voltage to a linear power amplifier. The delay line is necessary to compensate the phase misalignment between the envelope and the RF signal due to the envelope feedback path. Unlike the Kahn EER technique, the envelope tracking system has a linear power amplifier and no limiter.

The linearity of a power amplifier with envelope tracking is usually worse than that of a power amplifier with a fixed supply voltage because of the variation of the power gain with the supply voltage. In this case, it is possible to use a fixed predistortion to minimize the increased nonlinearity to a considerable extent. However, it is best to use a digital control of the power amplifier with envelope tracking, a schematic for which is shown in Fig. 9.6 [12]. In addition to providing a proper control voltage for the dc-dc converter according to the signal envelope, the DSP system also computes a predistorted input signal for both the in-phase (I) and quadrature (Q) channels using amplifier amplitude and phase characteristics. The practical results show that the output frequency spectrum for a IS-95 CDMA input signal can be improved by 8 dB in adjacent channel power ratio (*ACPR*) having an output power of 28 dBm. However, the *ACPR* is quite sensitive to the timing relationships between a varying supply voltage and input signal.

Figure 9.7 shows the schematic of the boost dc-dc converter without a feedback loop section implemented using the AlGaAs/GaAs HBT process [10]. The inductor value is set to 300 nH, limiting the dc output

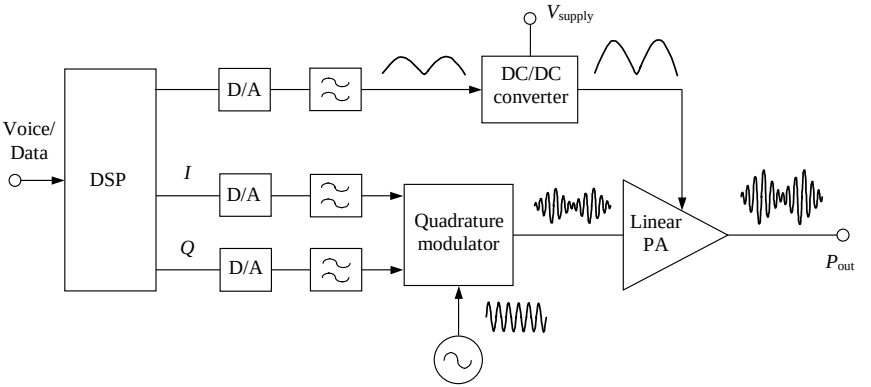

Figure 9.6 Power amplifier envelope-tracking architecture with digital control.

power maximum to 1 W. The value of the output capacitance is chosen to be 10 nF, consistent with low ripple and fast dynamic response. Such a dc-dc boost converter with 10 MHz switching (clock) frequency can provide 74 percent efficiency at maximum dc power. The ripple in the dc-dc converter output results in the spurious output signal spectrum of approximately 60 dB lower than the fundamental. For a GaAs MESFET power amplifier with boost converter operated at 950 MHz with maximum output power of 1 W, the power usage efficiency calculated in accordance with the probability distribution function (PDF) of its output power is 1.64 times higher than the one for just battery operation [11]. However, to meet CDMA IS-95 specifications for *ACPR*, a fast feedback loop regulation scheme and dynamic gate biasing are needed.

The Class-S modulator, which can provide a dynamically controlled supply voltage, is similar in form to a buck dc-dc converter where the

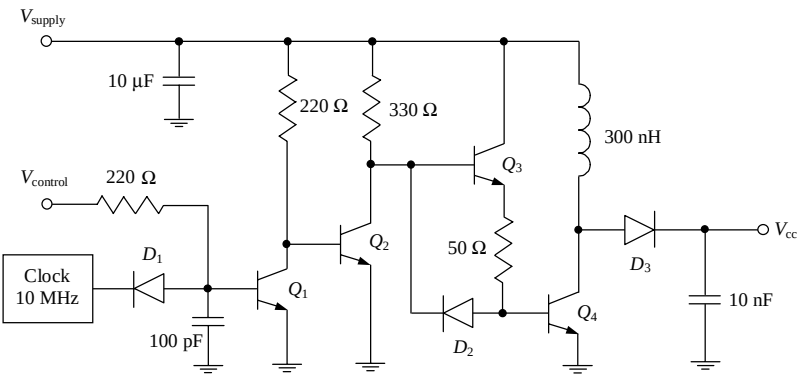

Figure 9.7 DC-to-DC converter schematic [10].

width or duty cycle of the pulses is proportional to an input control voltage. The control voltage corresponds to the amplitude of the modulated envelope signal. For most modern communication systems, the switching frequency should be as high as possible to allow rapid modulation of the supply voltage. The high switching frequency provides several advantages: reduced value and size of the low-pass filter, better suppression of the switching frequency and fast dynamic response. Maximizing the quality factors of the LPF elements and minimizing the on-resistances of the switching nMOS and pMOS transistors using larger sizes for their gate channel widths can result in a Class-S modulator efficiency of approximately 90 percent at the switching frequency of 5 MHz, and slightly less at 10 MHz [13].

Figure 9.8 shows the experimental results for 2-W envelope tracking power amplifier using a high-efficiency Class-S modulator intended for CDMA cellular handset applications in a frequency range of 824 to 849 MHz [13]. The power amplifier was designed based on AlGaAs/InGaAs heterostructure insulated-gate FET technology, which allows single supply voltage operation. The phase deviations of the output

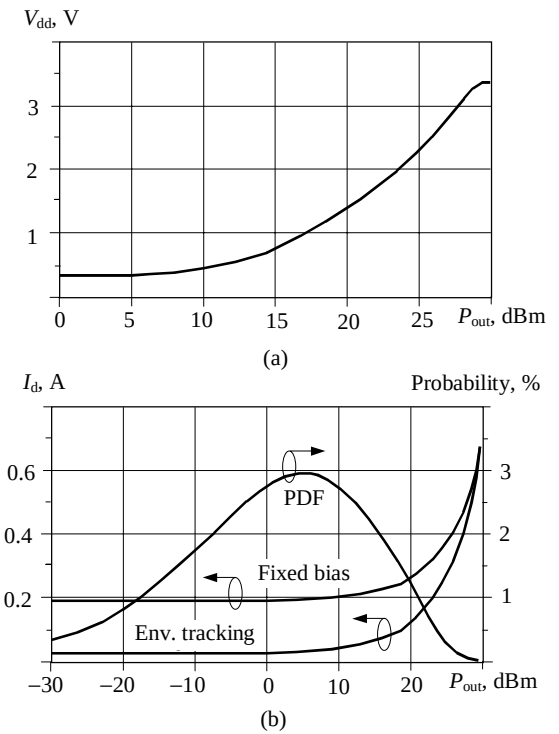

Figure 9.8 Envelope tracking power amplifier drain (*a*) supply voltage and (*b*) DC current [13].

signal across the dynamic range of the supply voltage were less than 3° up to the 2-dB gain compression point, resulting in adjacent and alternate channel power ratios of −46 dBc and −56 dBc, respectively. Each *ACPR* is measured as the ratio of power in a 30-kHz bandwidth offset from the carrier by 885 kHz for the adjacent channel and 1.98 MHz for the alternate channel. The supply voltage is dynamically stepped down via the Class-S modulator to approximately 0.3 V in deep backoff with a maximum voltage of about 3.3 V due to the small voltage drop from the battery supply voltage of 3.5 V, as shown in Fig. 9.8(*a*). More than five times improvement in power usage efficiency is obtained compared to a power amplifier with fixed bias voltage where the significant amount of the quiescent current is still kept over a wide range of output powers (see Fig. 9.8(*b*)).

In handset wireless applications, the dc-dc converters should provide high efficiency, small size, low cost, and low noise operation. One of the possibilities is to use a deep submicron SiGe BiCMOS process technology for fabrication of the monolithic supply modulated power amplifier, where the power transistor can be implemented using the SiGe HBT process [14]. The size of the passive elements can be reduced to practical values for integration by increasing the switching frequencies to the order of 100 MHz. Switches can be implemented using nMOS and pMOS devices with optimum channel widths to minimize their power losses. The filter capacitance is realized as a MOS capacitance having higher specific capacitance compared with a metal-insulator-metal (MIM) capacitance. To increase the quality factor of the filter inductance, it is implemented using a thick last metal layer far above the substrate. Such a monolithic 900 MHz power amplifier with a high speed synchronous buck dc-dc converter can provide substantially higher efficiency compared with a similar power amplifier using a constant voltage supply, especially at low power levels.

Outphasing Power Amplifiers

Outphasing power amplifier modulation technique was firstly developed in 1935 to improve both the efficiency and linearity of AM-broadcast transmitters [15]. Substantially later, its application was extended up to microwave frequencies under the name LINC (*linear amplification using nonlinear components*) [16]. An outphasing transmitter operates as a linear power amplifier system for amplitude-modulated signals, having a linear transfer function over a wide range of input signal levels by combining the outputs of two nonlinear power amplifiers, which are driven with signals of constant amplitude but different time-varying phases corresponding to the envelope of the input signal.

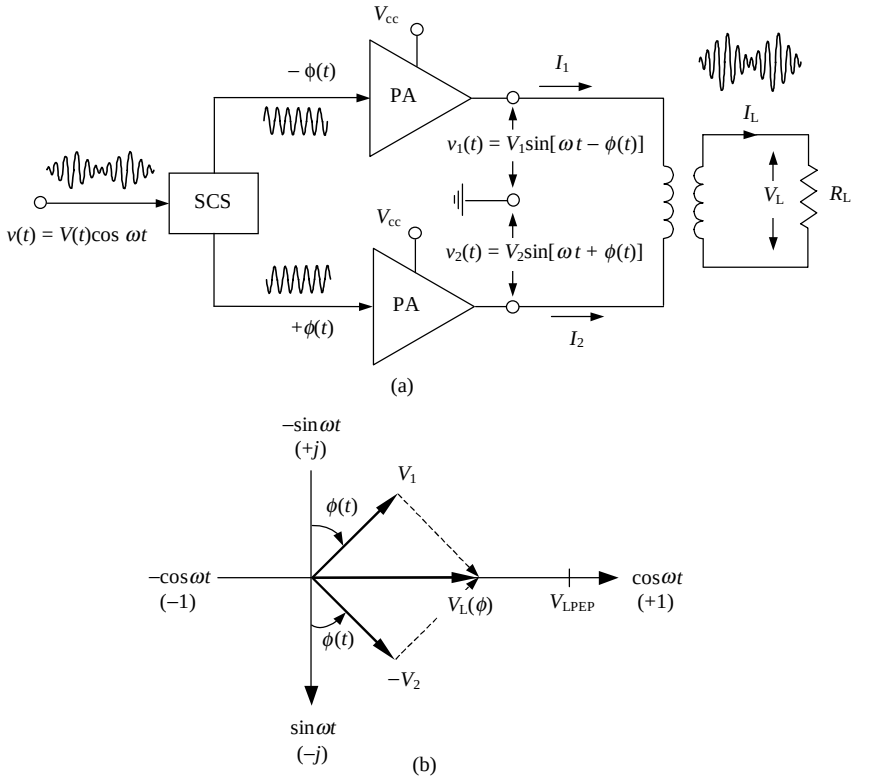

Figure 9.9 Simple outphasing power amplifier system.

A simple outphasing power amplifier system is shown in Fig. 9.9(a) [17]. The signal component separator (SCS) generates from the input amplitude-modulated signal two sine-wave signals of constant envelopes with different phases, $+\phi(t)$ and $-\phi(t)$. These two signals are then amplified by nonlinear power amplifiers and added together to produce the output amplitude-modulated signal. The peak output power is obtained with $\phi = 90^\circ$ when currents from power amplifiers with equal amplitudes $I_L = I_1 = I_2$ are added in phase, similar to push-pull operation. Zero output power corresponds to the signal with $\phi = 0^\circ$ when equal currents from power amplifiers cancel each other, i.e., $I_L = 0$. Intermediate values of phase $0^\circ < \phi < 90^\circ$ produce intermediate values of output voltage amplitude. As shown in Fig. 9.9(b), the time-varying phase ϕ can be written using the vector sum of the output voltages V_1 and V_2 by

$$\phi = \arcsin(V_L/V_{LPEP}) \tag{9.3}$$

where $V_L = I_L R_L$ is the output voltage amplitude across the load resistance R_L, and V_{LPEP} is the maximum output voltage amplitude at peak envelope power.

The instantaneous collector efficiency of a simple outphasing system with Class B power amplifiers can be calculated from

$$\eta = \frac{\pi}{4} \frac{V_L}{V_{LPEP}} \tag{9.4}$$

having maximum value of 78.5 percent under saturation when $V_L = V_{LPEP}$ with $\phi = 90^\circ$ and zero value when $V_L = 0$ with $\phi = 0^\circ$. Thus, the efficiency of a simple power amplifier outphasing system is the same as that of an ideal Class B power amplifier, reducing linearly with the output voltage amplitude.

The efficiency at lower output voltages can be significantly improved using the Chireix outphasing power amplifier system shown in Fig. 9.10(a), which includes additional quarterwave transmission lines and shunt reactances. Phasor analysis of the load network results in the

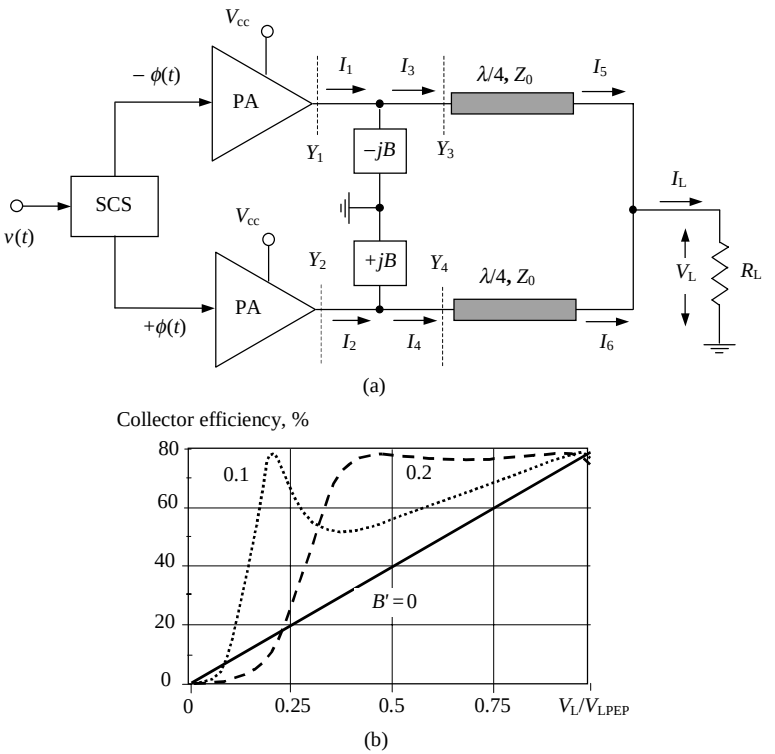

Figure 9.10 Chireix outphasing power amplifier system and instantaneous efficiencies.

following equations for admittances Y_3 and Y_4 as functions of the time-varying phase ϕ using the quarterwave transmission-line impedance transformation of $Z_3Z_5 = Z_4Z_6 = Z_0^2$ [17]:

$$Y_3 = \frac{2R_L}{Z_0^2}\frac{V_L}{V_{LPEP}}(\sin\phi + j\cos\phi) \tag{9.5}$$

$$Y_4 = \frac{2R_L}{Z_0^2}\frac{V_L}{V_{LPEP}}(\sin\phi - j\cos\phi) \tag{9.6}$$

where Z_0 is the characteristic impedance of the transmission lines.

From Eqs. (9.5) and (9.6), it follows that the admittances Y_3 and Y_4 are purely resistive only for $\phi = 90^\circ$ corresponding to the case of in-phase output currents. However, for most values of phase ϕ, the power amplifiers have highly reactive loads, which become completely reactive when $\phi = 0^\circ$ with out-of-phase output currents. The effect of the reactive loads can be partially compensated by adding the shunt susceptances $-B$ and $+B$, respectively. The susceptances of the admittances $Y_1 = Y_3 - jB$ and $Y_2 = Y_4 + jB$ can be zeroed at one specific output voltage amplitude by setting

$$B = \frac{2R_L}{Z_0^2}\frac{V_L}{V_{LPEP}}\sqrt{1 - \left(\frac{V_L}{V_{LPEP}}\right)^2} \tag{9.7}$$

which can be obtained by substituting Eq. (9.3) into Eqs. (9.5) and (9.6). As a result, for the case of a purely resistive load, the instantaneous collector efficiency of a Chireix outphasing system with ideal Class B power amplifiers can reach the maximum value of

$$\eta = \frac{\pi}{4} \tag{9.8}$$

The instantaneous efficiencies of the Chireix outphasing system for different values of the normalized shunt susceptance $B' = BZ_0^2/2R_L$ are shown in Fig. 9.10(*b*), from which it follows that the selection of a proper value of B increases efficiency at a specified level of the output voltage amplitude but it is degraded at low and high amplitudes. Using a value of $B' = 0.2$ can provide high efficiency over the upper 6 dB of the output voltage range. The case of $B' = 0$ corresponds to the collector efficiency variations of an ideal Class B power amplifier. An improvement in the average efficiency, calculated over a wide range of output voltages for various amplitude-modulated signals, of up to a factor of two over that of an ideal Class B power amplifier, can be achieved by properly selecting the shunt susceptances in the outphasing power amplifier system. On the whole, to design such an outphasing system, it is necessary to consider simultaneously such factors as the

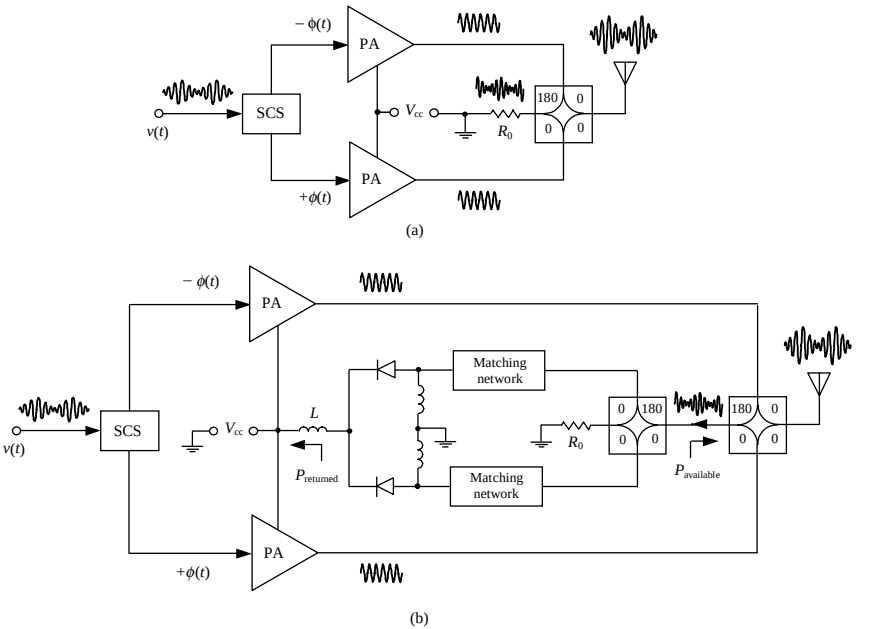

Figure 9.11 Outphasing power amplifier system with hybrid combiner [18].

complexity of the SCS circuit and sensitivity of the power amplifiers to the wide range of load impedances.

The outphasing power amplifier systems used at microwaves employ hybrid combiners to isolate the two power amplifiers from each other, allowing them to see resistive loads at all signal levels, as shown in Fig. 9.11(a). Since both power amplifiers deliver full power all of the time, the efficiency of such a hybrid-coupled microwave LINC transmitter varies with the output power, resulting in a poor efficiency at low power levels. This is because most of the output power is dissipated in the ballast resistor R_0 of the combining network when the two power amplifiers are operated substantially out-of-phase. Figure 9.11(b) shows the power recycling schematic where RF-to-dc converter is implemented with high-speed Schottky diodes and optimized matching networks [18]. To achieve better efficiency, the diodes should be switched fully having minimal series on-resistances. As a result, at the operating frequency of 1.95 GHz, the measured power reuse efficiency, which is defined as the ratio of the returned power P_{returned} to the power available from the hybrid $P_{\text{available}}$, was found to be approximately 63 percent at power levels varied with supply voltage. The amount of the overall system efficiency improvement depends on the modulation scheme and could be compromised for modulation schemes that exhibit very deep

variations in envelope power on a regular basis. In general, such a technique is very useful to improve the overall efficiency of the LINC power amplifier architecture making it much more attractive for implementation in future generations of communication systems.

Using quarterwave transmission lines in microwave LINC power amplifier systems results in a sufficiently narrow-band operation, which may not be acceptable for modern communication systems with wideband modulation techniques. At the same time, connecting the parallel resonant L_0C_0-circuit tuned on the fundamental in parallel to the load R_L, as shown in Fig. 9.12(a), allows us to approximate the ideal Class F operation mode for each power amplifier with rectangular drain voltage and half-cosinusoidal drain current waveforms increasing the operation efficiency of the power amplifiers (see Chap. 7). This is because such a parallel L_0C_0-circuit has low impedances at any harmonics, resulting in a proper shortening of the quarterwave transmission lines at their ends and low impedances for even-order harmonics at their inputs.

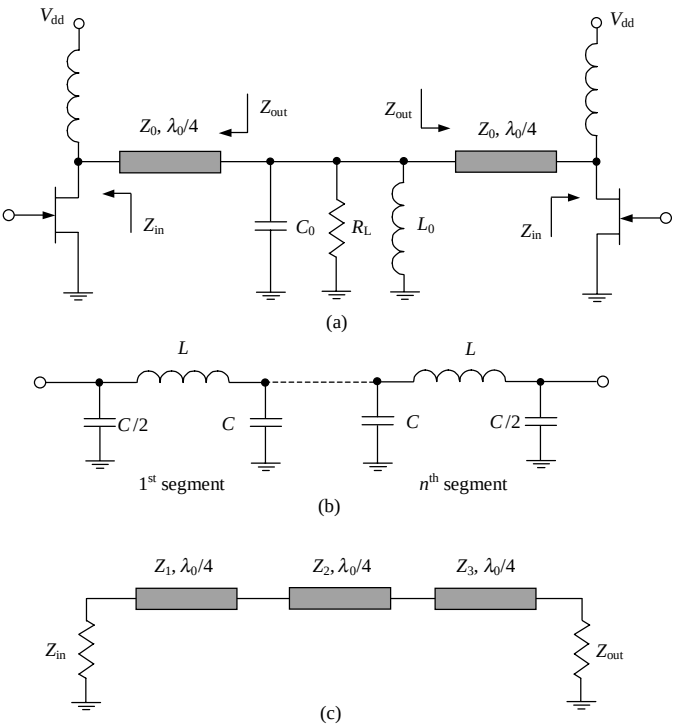

Figure 9.12 LINC transmitter load network with quarterwave transmission lines and their broadband realizations.

To apply CMOS technology (realizing low cost and compact size), it is best to replace the quarterwave transmission lines by their lumped LC ladder low-pass network equivalent shown in Fig. 9.12(b). The values of the series inductances L and shunt capacitances C can be obtained by [19]

$$L = \frac{Z_0}{4nf_0} \tag{9.9}$$

$$C = \frac{1}{4nf_0 Z_0} \tag{9.10}$$

where f_0 is the center bandwidth frequency, Z_0 is the characteristic impedance of the transmission line, and n is the number of π-type segments.

To achieve wideband operation, the single transmission line should be replaced by cascades of transmission lines, having a smaller transformation ratio for each line. For the antimetric structure of the stepped transmission-line transformer with three quarterwave transmission lines shown in Fig. 9.12(c), using the ratios between their characteristic impedances Eq. (8.42) can be calculated by

$$Z_0 = Z_2 \tag{9.11}$$

$$Z_2^2 = Z_1 Z_3 \tag{9.12}$$

where $Z_S = Z_{in}$, $Z_L = Z_{out}$, $n = 3$ and $Z_{in} < Z_1 < Z_2 < Z_3 < Z_{out}$.

Finally, to provide wideband matching of the input impedance of $Z_{in} = 0.55\,\Omega$ to the output impedance $Z_{out} = 100\,\Omega$ in a 50 percent bandwidth with the center bandwidth frequency of 8 GHz, the six π-type LC ladder segments were used. The overall size of the combiner using 0.18-μm CMOS technology to realize the six strip octagonal inductances and seven MIM capacitances was $400 \times 1400\ \mu m^2$ providing a delivery of 1.5-W output power from both power amplifiers to the antenna [19].

However, the practical implementation of the entire LINC power amplifier system is quite difficult because of its inherent sensitivity to the phase errors caused by the difference in electrical lengths between the two power amplifier branches. A block diagram of the LINC power amplifier architecture, incorporating a feedback loop to compensate for phase errors, is shown in Fig. 9.13 [20]. The phase difference between the two branches is detected by a multiplier, which allows the phase control of one branch by adding or subtracting a certain phase increment. At the operating frequency of 900 MHz, the output power of 7.5 W with power amplifier efficiency of 21 percent (including hybrid and isolator losses) was achieved. This method also allows the out-of-band spectral components to be effectively suppressed. To provide a high amplitude

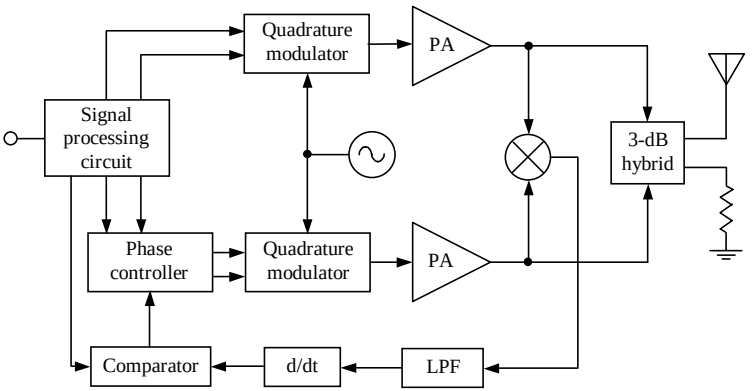

Figure 9.13 LINC transmitter with phase error compensating loop [20].

and phase accuracy of the LINC system (0.5-dB amplitude and 0.3° phase), a DSP-based architecture can be developed where the compensation of the amplitude and phase imbalances is accomplished using calibration schemes [21].

Doherty Power Amplifier Architecture

The Doherty power amplifier technique was introduced in 1936 as a more efficient alternative to the conventional amplitude-modulation techniques having low average efficiency [22]. The classical two-stage Doherty power amplifier architecture shown in Fig. 9.14 incorporates two power amplifiers, normally called the *main* (*carrier*) and *auxiliary* (*peaking*) amplifiers, separated by a quarterwave transmission line. The quarterwave transmission line on the input is required to compensate for the 90° phase shift caused by the quarterwave transmission line at

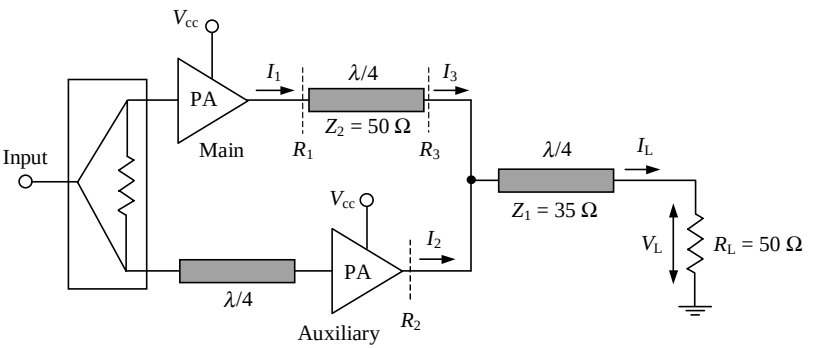

Figure 9.14 Classical two-stage Doherty power amplifier architecture.

the output of the main amplifier. The main amplifier is biased in Class B mode, while the auxiliary amplifier is biased in Class C mode.

The condition of power conservation for a lossless output transmission line results in

$$I_3 = I_1\sqrt{\frac{R_1}{R_3}} \tag{9.13}$$

The current division ratio is defined by

$$S = \frac{I_3}{I_2 + I_3} \tag{9.14}$$

As a result, the overall output power P_{out} is the sum of the main amplifier output power $P_1 = SP_{\text{out}}$ and auxiliary amplifier output power $P_2 = (1 - S)P_{\text{out}}$. The impedance seen at the output of the 50 Ω transmission line is

$$R_3 = \frac{I_2 + I_3}{I_3}\frac{Z_1^2}{R_{\text{L}}} = \frac{Z_1^2}{SR_{\text{L}}} \tag{9.15}$$

whereas the impedance seen by the auxiliary power amplifier is

$$R_2 = \frac{I_2 + I_3}{I_2}\frac{Z_1^2}{R_{\text{L}}} = \frac{Z_1^2}{(1 - S)R_{\text{L}}} \tag{9.16}$$

The basic operation principle of the Doherty power amplifier architecture is analyzed for low, medium and peak output power regions [23]. At peak output power P_{PEP} when both power amplifiers are saturated, for ideal Class B operation, the resultant collector efficiency is equal to the maximum achievable efficiency of $\eta = \pi/4$. For the classical Doherty power amplifier architecture shown in Fig. 9.14 with the current and power division ratios of $S = \alpha = 0.5$ when both the main and auxiliary amplifiers produce equal output powers, their load impedances are equal to $R_1 = R_3 = R_2 = Z_2 = 2Z_1^2/R_{\text{L}}$. If the characteristic impedance of the output transmission line is chosen equal to $Z_1 = 35\,\Omega$, then $R_1 = R_3 = R_2 = Z_2 = R_{\text{L}} = 50\,\Omega$.

At lower power levels, the auxiliary amplifier is turned off while the main amplifier operates in the active region. In this case, the load impedance seen by the main amplifier is

$$R_1 = \left(\frac{Z_2}{Z_1}\right)^2 R_{\text{L}} \tag{9.17}$$

and equal to $R_1 = 2R_{\text{L}} = 100\,\Omega$ when $Z_1 = 35\,\Omega$ and $Z_2 = R_{\text{L}} = 50\,\Omega$. Because the output power of the main amplifier in saturation is four times less than the peak output power P_{PEP}, the collector efficiency of

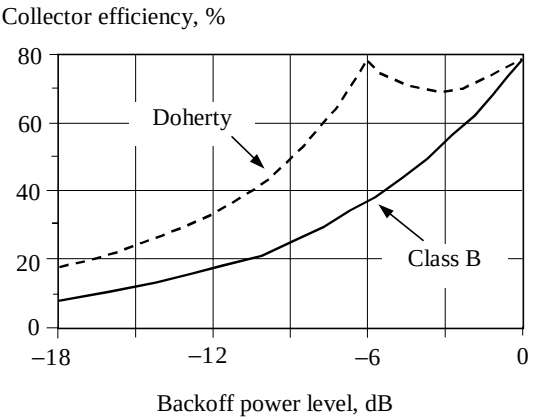

Figure 9.15 Collector efficiency of ideal two-stage Doherty architecture and Class B power amplifier.

the main amplifier in an ideal Class B mode will be twice that of a conventional Class B power amplifier, achieving a maximum of 78.5 percent at the backoff power level of −6 dB, as shown in Fig. 9.15.

At medium power levels, the main amplifier is saturated, whereas the auxiliary amplifier is turned on and operates in the active region. Since the output voltage of the main amplifier $V_1 = I_1 R_1$ is constant under saturation conditions, from Eq. (9.13) it follows that the current I_3 is constant in the medium power region too. The collector efficiency of the main amplifier remains at its maximum value. The collector efficiency of the auxiliary amplifier increases to its maximum value for Class B operation at peak output power P_{PEP}. As a result, the Doherty power amplifier architecture achieves maximum efficiency at both the transition point and peak output power, and remains relatively high in between (see Fig. 9.15).

There is a possibility to extend the collector efficiency over a wider range of output powers if we choose the main and auxiliary amplifiers with different output power capabilities, smaller for the main amplifier and larger for the auxiliary amplifier. For example, for a power ratio $\alpha = 0.25$, the transition point with maximum collector efficiency corresponds to the backoff power level of −12 dB from peak output power [23]. At peak output power when the main and auxiliary amplifiers are saturated, from consideration of their output powers it follows that $R_1 = Z_2 = R_3 = 3R_2$. As a result, $I_2 = 3I_3$ and $S = 0.25$. The output impedances R_2 and R_3 as functions of the load impedance R_{L} and characteristic impedance Z_1 can be obtained from Eqs. (9.15) and (9.16). For example, if we choose the characteristic impedance of the output transmission line $Z_1 = 15\,\Omega$ and $R_{\text{L}} = 50\,\Omega$, then the characteristic impedance of the quarterwave transformer and output impedance of

the main amplifier are $Z_2 = R_1 = 18\,\Omega$ while the output impedance of the auxiliary amplifier is $R_2 = R_1/3 = 6\,\Omega$.

From Eqs. (9.15) and (9.17) it follows that

$$R_1 = \frac{Z_2^2}{SR_3} \tag{9.18}$$

Hence, at lower power levels when the auxiliary amplifier is turned off, the output impedance R_1 is four times higher than that at the peak output power where $R_1 = Z_2 = R_3$.

Implementation of the extended Doherty technique into the InGaP/GaAs HBT power amplifier developed for CDMA handset applications increased the efficiency at the backoff power levels, satisfying the linearity requirements at the same time. The scaling ratio of 4:1 was used for HBT devices with total emitter areas of 3360 and 840 μm^2 for the auxiliary and main amplifiers, respectively. As a result, the power-added efficiency of 45 percent was measured at a highest maximum output power of 25 dBm with the adjacent and alternate channel power ratios of -42 dBc and -54 dBc, respectively [24]. At the 10-dB backoff level, the power-added efficiency remains high enough, at 23 percent, while the conventional Class AB power amplifiers designed for the same application normally have power-added efficiencies about four times lower.

An asymmetrical Doherty architecture exhibits a significant drop in efficiency in the region between the power at the transition point and the peak output power. However, it is possible to use more than two power amplifiers in order to maintain the efficiency without significant dropping at the backoff output power levels. The multistage Doherty power amplifier architecture shown in Fig. 9.16 uses more than one auxiliary amplifier, with quarterwave transmission lines to combine their output powers [25].

Figure 9.17 shows the instantaneous collector efficiencies of the multistage Doherty power amplifer (DPA) architectures for two, three and

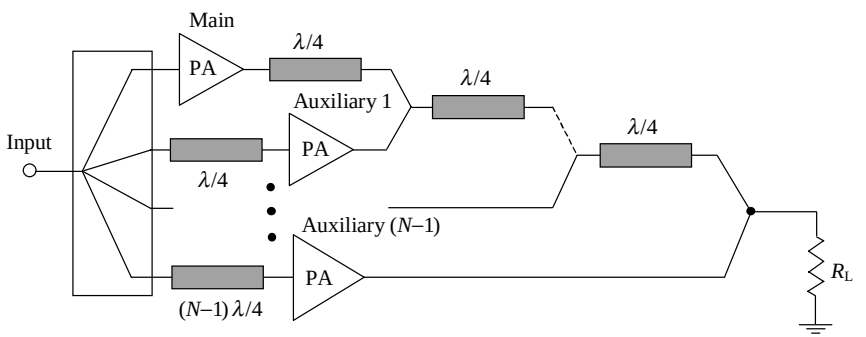

Figure 9.16 Multistage Doherty power amplifier architecture.

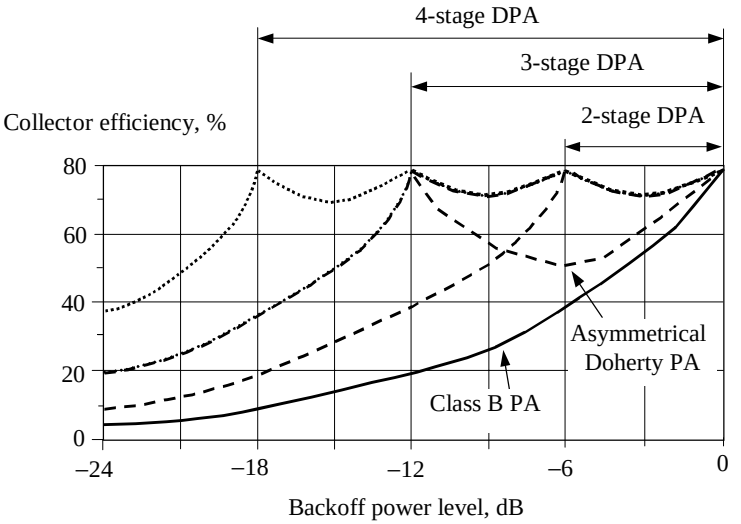

Figure 9.17 Efficiencies of the different Doherty power amplifier architectures.

four stages having maximum efficiency at the transition points of −6 dB, −12 dB and −18 dB backoff output power levels, respectively. As follows from Fig. 9.17, the multistage architecture provides higher efficiencies at backoff levels in between the efficiency peaking points compared with asymmetrical Doherty architecture and significantly higher efficiency at all backoff output power levels compared with the conventional Class B power amplifiers. For 1.95-GHz WCDMA application, such a three-stage Doherty power amplifier structure—using GaAs MESFET devices and microstrip-based power combining elements on FR-4 substrate—provides the power-added efficiency of 46 percent and power gain of 8.5 dB at $P_{1dB} = 29.7$ dBm. The peak power-added efficiencies of 34.5 percent and 16.9 percent were measured at −6 dBc and −12 dBc backoff conditions. The WCDMA linearity requirements were met at all output power levels up to 28.6 dBm [25].

It is difficult to apply directly the Doherty technique to the design of the power amplifier integrated circuits with a high level of integration, since the physical size of the quarterwave transmission lines is too large. For example, for a FR-4 substrate with effective dielectric permittivity of $\varepsilon_r = 3.48$, the geometrical lengths of the quarterwave transmission lines are 48 mm, 19 mm and 8.7 mm at the operating frequencies of 900 MHz, 2.4 GHz and 5.2 GHz, respectively [26]. Therefore, the best solution in this situation is to replace the quarterwave transmission lines with lumped elements using a single-frequency equivalence.

Consider the transmission matrix $[ABCD_a]$ for a quarterwave transmission line (see Fig. 9.18(a)) and transmission matrix $[ABCD_b]$ for a

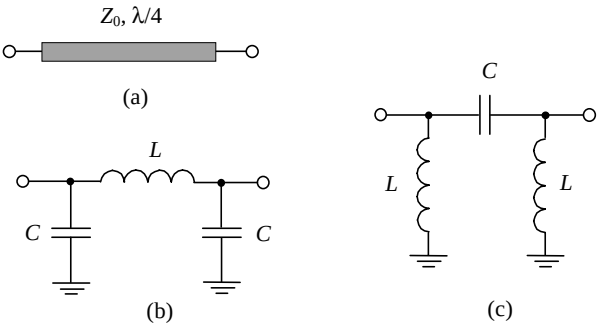

Figure 9.18 Quarterwave transmission line and its single-frequency lumped equivalent circuits.

π-type lumped circuit, consisting of the series inductance and two shunt capacitances (see Fig. 9.18(b)) given by

$$[ABCD_{\mathrm{a}}] = \begin{bmatrix} \cos\theta & jZ_0 \sin\theta \\ j\dfrac{\sin\theta}{Z_0} & \cos\theta \end{bmatrix}\Bigg|_{\theta=\pi/2} = \begin{bmatrix} 0 & jZ_0 \\ \dfrac{j}{Z_0} & 0 \end{bmatrix} \tag{9.19}$$

$$\begin{aligned}[ABCD_{\mathrm{b}}] &= \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1-\omega^2 LC & j\omega L \\ j\omega L\left(2-\dfrac{1}{\omega^2 LC}\right) & 1-\omega^2 LC \end{bmatrix} \end{aligned} \tag{9.20}$$

Equating the corresponding elements of both matrices obtained by Eqs. (9.19) and (9.20) yields the following relationships between the circuit elements:

$$Z_0\omega C = Z_0/\omega L = 1 \tag{9.21}$$

The same relationships can be established between the characteristic impedance of the quarterwave transmission line and π-type lumped circuit consisting of the series capacitance and two shunt inductances shown in Fig. 9.18(c) using Eqs. (5.44) and (5.45) (see Chap. 5).

Figure 9.19 shows a 900-MHz GaAs MESFET lumped two-stage Doherty power amplifier architecture where the output quarterwave transmission line connected to the main amplifier is replaced by a low-pass π-type lumped circuit and the input quarterwave transmission line (providing phase shifting) connected to the auxiliary amplifier is replaced by a high-pass π-type lumped circuit [26]. In addition, the output quarterwave transformer connected to the load is replaced by

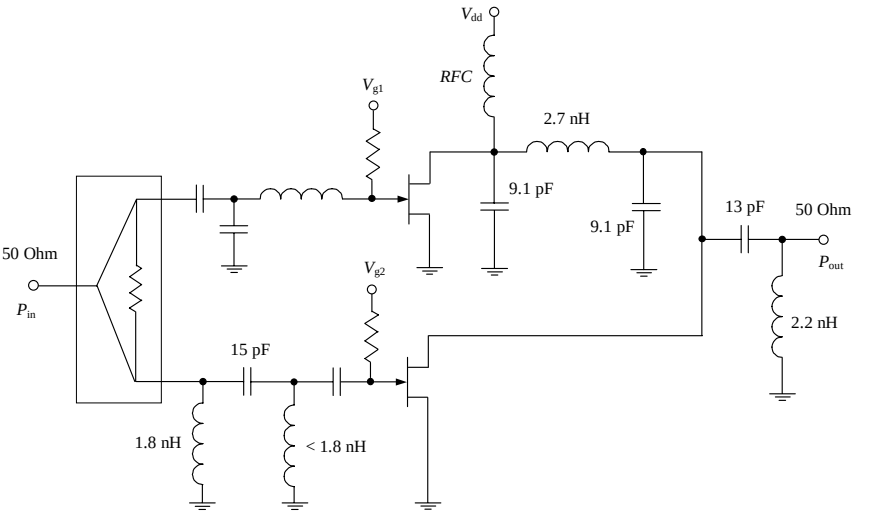

Figure 9.19 A 900-MHz Doherty amplifier implemented with lumped elements [26].

a high-pass *L*-type matching circuit, whereas the two low-pass *L*-type matching circuits are used to provide the input matching of the main and auxiliary amplifiers. In the case of the auxiliary amplifier, the parallel inductance corresponding to the equivalent quarterwave phase shifter, and parallel capacitance corresponding to the input matching circuit, can be combined into a single parallel inductance.

As a result, the size reduction achieved by using lumped elements is dramatic, and such a lumped Doherty power amplifier can be implemented in a hybrid module. The overall performance of the lumped and transmission-line architectures is similar, with slightly narrower bandwidth (of about 15 percent) for the lumped Doherty power amplifier. Using such a lumped Doherty power amplifier with a power-added efficiency of about 52 percent at peak output power, the power usage efficiency according to a PDF for the CDMA signal is 14.1 percent, which is more than three times higher than the conventional Class AB power amplifier having an efficiency of 4.4 percent.

However, the nonideal power gain and phase in a high-power region can cause a linearity problem when, for a CDMA signal, the *ACPR* may not be good enough to satisfy the IS-95 specification requirements. To solve this problem, an improved Doherty power amplifier architecture can be used, which employs an envelope-tracking technique to control the gate bias voltage of the auxiliary amplifier in accordance with the input signal envelope. Such an approach can provide also higher efficiency, realizing a lower bias voltage for higher output power. This compromises both high efficiency and good linearity requirements over a wide range of output powers.

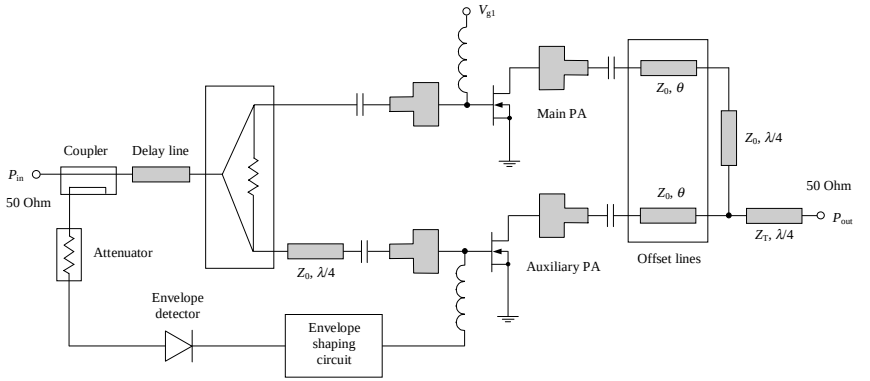

Figure 9.20 Block diagram of LDMOSFET microstrip Doherty power amplifier with adaptive gate bias control [27].

Figure 9.20 shows a block diagram of a 2.14-GHz LDMOSFET microstrip Doherty power amplifier with adaptive gate bias control [27]. The electrical lengths of the 50-Ω offset microstrip lines of 0.535 λ were used for both the main and auxiliary amplifiers. The output impedance transformed by the bottom offset line becomes high enough to block the output power leakage of the auxiliary amplifier at low-power operation. Having the same output powers of 32.7 dBm, such a Doherty power amplifier demonstrates an improvement in power-added efficiency of 15.2 percent compared with the Class AB power amplifier, which is achieved using Class AB biasing for both the main and auxiliary amplifiers with quiescent current of 20 mA each. In the case of the Doherty power amplifier, the same quiescent current is kept only for the main amplifier, while the bias point of the auxiliary amplifier is changed according to the input signal envelope.

The linearity of the power amplifier can be improved by using DSP to provide more accurate gate bias control, combined with digital predistortion to correct simultaneously the gain and phase characteristics in a high-power region. Figure 9.21 shows an 840-MHz MESFET Doherty power amplifier architecture realized using hybrid technology with DSP implemented externally via a board controlled by a personal computer [28]. The DSP generates the baseband I and Q signals (which are then up-converted to an RF signal using the quadrature modulator), as well as another voltage signal V_{g2}, which is applied to the gate bias of the auxiliary amplifier. DSP control results in an efficiency improvement because of the dynamic gate biasing of the auxiliary amplifier according to the instantaneous envelope of the input signal. At the same time, the phase performance is corrected by phase predistortion at baseband level based on the dynamic gate bias voltage values from

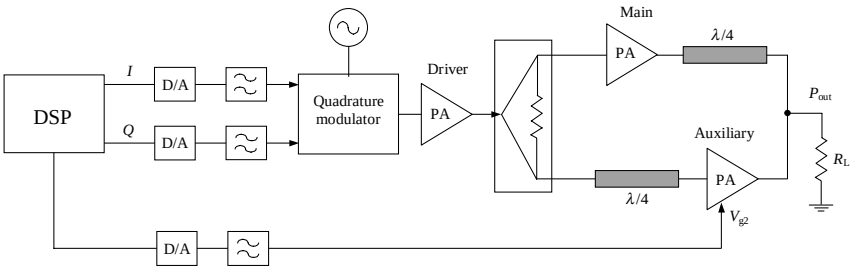

Figure 9.21 Doherty power amplifier architecture with DSP control.

the gain correction, resulting in a linearity improvement. An overall improvement in *PAE* of 3–5 percent and in *ACPR* of about 10 dB at an average output power of 23 dBm can be achieved by utilizing such a DSP technique [26, 28].

To further increase the efficiency of the Doherty amplifier at backoff output power levels for the signals with nonconstant amplitude, it is necessary to provide the proper variations of the supply bias voltage. By modulating the main amplifier supply voltage using the output of the envelope amplifier as shown in Fig. 9.22, the high-efficiency range of the Doherty power amplifier is greatly enhanced [29]. As well as in the Kahn EER approach, the envelope amplifier includes a Class-S modulator with low-pass filter to obtain high efficiency. The supply bias voltage of the main amplifier varies in such a way as to maintain continuous operation near saturation, while the auxiliary amplifier operates at fixed supply voltage. The envelope amplifier can be turned on for high-efficiency low-power level operation, or it can be turned off for a conventional Doherty power amplifier.

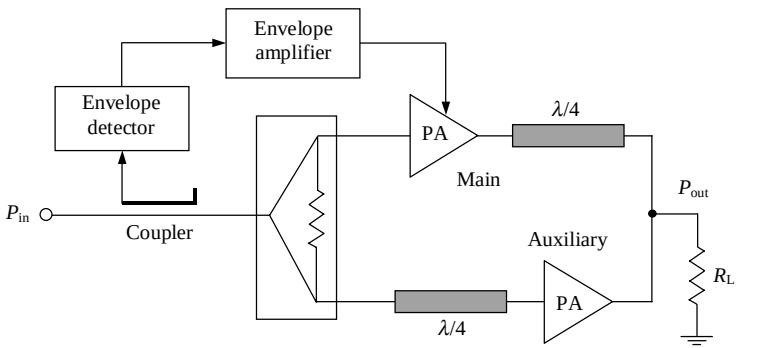

Figure 9.22 Doherty power amplifier architecture with supply voltage control.

Switched-Mode and Dual-Path Power Amplifiers

The power amplifiers in communications systems like GSM/EDGE, WCDMA or CDMA2000 are required to cover linearly a dynamic range of the transmitter output powers up to 80 dB. As a result, being designed for the highest power level with maximum achievable efficiency, the power amplifier tends to operate less efficiently at lower power levels, which leads to shortening the life of a battery. In Fig. 9.23, a transmitter architecture, including a variable gain amplifier, a power amplifier to provide a high output power level, a bypass line for bypassing the smaller output power level, and a switch between the two signal paths is shown [30]. Normally, the power amplifiers for wireless handset transmitters are designed to achieve the power gain of about 25 to 30 dB. Therefore, it is very important to provide an efficient operation condition for the maximum probable transmitting power required to deliver a signal to the base station, which is of about 15 to 25 dB less than the maximum peak power. The output power of the widely used variable gain amplifiers is usually less than 10 dBm, otherwise it is difficult to realize their linear operation. The variable gain amplifiers usually have a sufficiently high value for their noise figure. This contributes to the degradation in distortion and excessive noise level in the receiver bandwidth, which can only be improved by additional filtering, that increases the cost and size of the transmitter. Besides, it is difficult to provide an 80-dB dynamic range using a single variable gain amplifier because it can provide typically a linear gain control range of about 30 to 40 dB.

A possible solution to improve the performance of the wireless handset transmitter is to use two power amplifier paths with different output power levels and a variable gain amplifier in the low power path. This can result in a significant reduction of power consumption, because the low-power amplifier provides higher efficiency at the output power level corresponding to maximum PDF. The block schematic of such a transmitter architecture with a dual-path power amplifier is shown in Fig. 9.24. When it is required to transmit the signal with an output power between the maximum level $P_{\max}$ and the statistically averaged power P_{avg}, the low-power amplifier with variable gain is turned off.

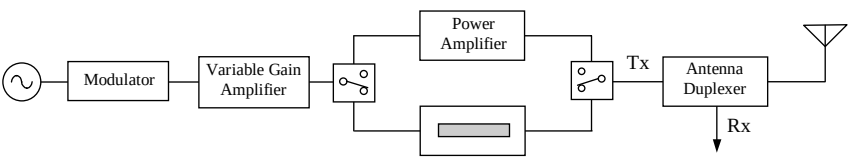

Figure 9.23 Transmitter architecture with bypass line.

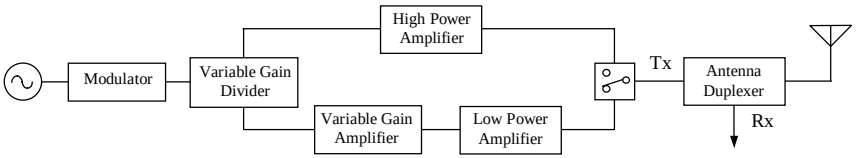

Figure 9.24 Transmitter architecture with dual-path power amplifier.

When it is sufficient to transmit a signal with output power equal or less than P_{avg}, the high-power amplifier is turned off. So, at any moment only one power amplifier is switched on. To further improve the efficiency of the transmitter, it is necessary to provide more than two power amplifier sections with different output power levels (with a variable gain amplifier for each section) connected in parallel to the multipole switch.

The variable gain amplifier can be realized in the form of the cascode amplifier, a typical circuit schematic for which is shown in Fig. 9.25. Such a cascode amplifier can operate as an attenuator with a linear power dynamic range of about 20 to 25 dB. Its current consumption is sufficiently small (less than 8 mA at maximum output power for $V_{contr} = 2.2$ V) as only the voltage supply is required for both transistors. Maximum output power with good linearity can be realized when the values of resistors R are chosen within the range of 500 to 1000 Ω.

The variable gain divider shown in Fig. 9.26 can be realized in the form of a differential amplifier with two output terminals transmitting the signal to both power amplifier paths simultaneously. The control signal, applied simultaneously to the bases of the differential pair devices, provides a sufficiently linear power dynamic range of about 15 dB. Better linearity is realized when the values of the resistors R are sufficiently high, of about 1500 to 2000 Ω. Such a differential amplifier has

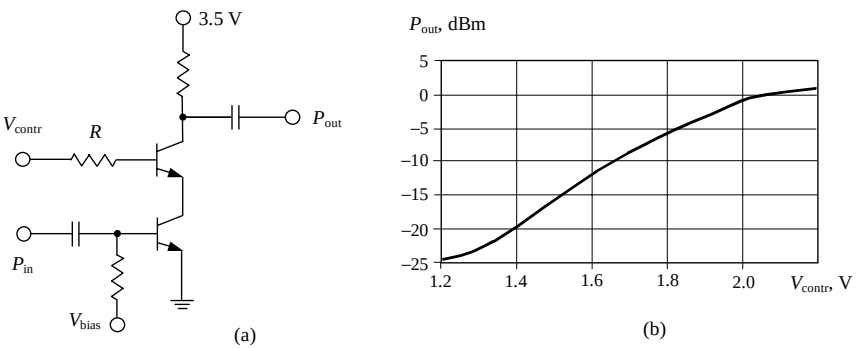

Figure 9.25 Variable gain amplifier circuit schematic and power tuning curve.

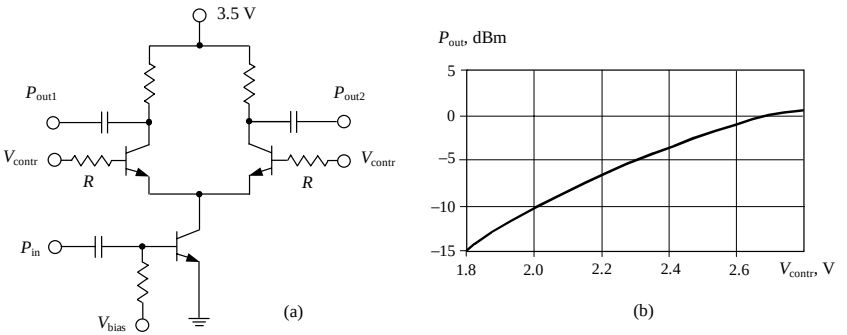

Figure 9.26 Variable gain divider circuit schematic and power tuning curve.

a good isolation between its input terminal and output terminals with equal signal levels at both output terminals.

In another approach, a mechanism for switching the output path between two or several power devices is used [31]. In this switchable path power amplifier (see Fig. 9.27), a combining network with a Schottky diode is used to switch the output path between the first active device (designed for maximum output power level) and the second active device (designed for the specified output power level with

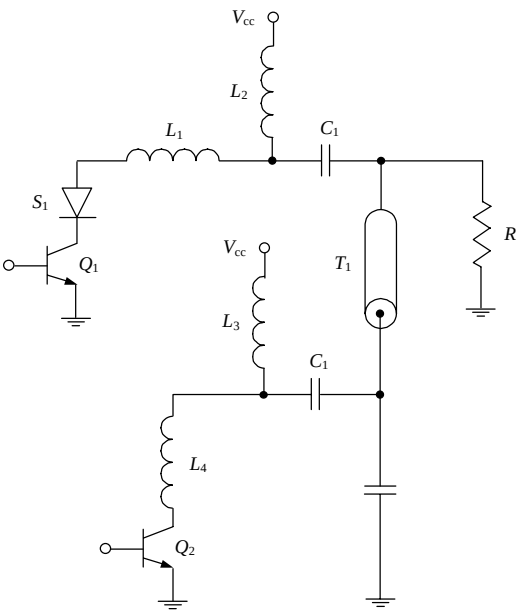

Figure 9.27 Switchable path power amplifier circuit.

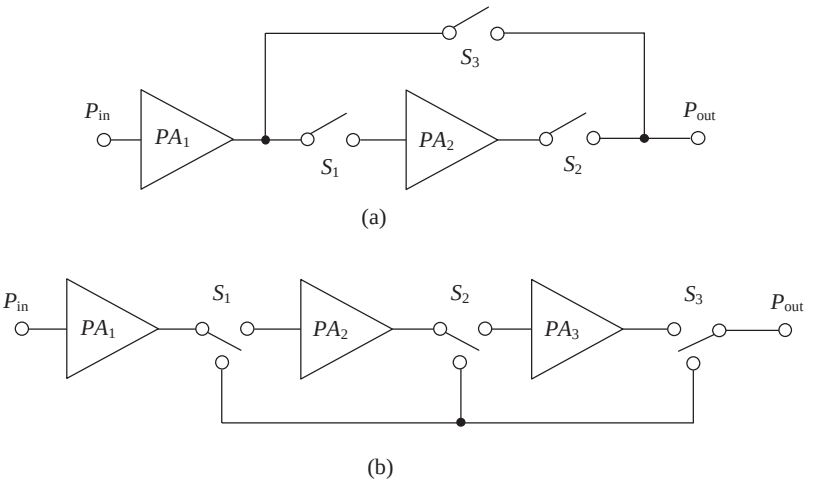

Figure 9.28 Switched-stage power amplifier configurations.

increased efficiency). As a result, the combining network is operable such that either the first power device or the second power device drives the power amplifier output.

An efficiency improvement can also be achieved by bypassing the power amplifier stages. For example, the power amplifier topology shown in Fig. 9.28(*a*) provides the possibility of bypassing the second stage [32]. At lower output power levels, the signal amplification can be achieved using only the first stage PA_1 with switch S_1 being turned on, whereas the maximum output power level is achieved using the two-stage power amplifier configuration with switches S_2 and S_3 being turned on. To eliminate any additional impedance matching, both stages should be designed to operate in a 50-Ω environment at the input and output. An improvement in average efficiency of greater than four times at backoff output power levels, compared with the conventional two-stage architecture, is realized for a CDMA power amplifier operating at 825 to 849 MHz with 29-dBm maximum output power [33].

The power amplifier schematic shown in Fig. 9.28(*b*) includes three amplifier stages with each stage having its own configuration so that a selected number of desired output power levels may be obtained directly from a selected power amplifier stage [34]. The amplifier stages also can be configured in tandem to deliver maximum output power when the output of the first stage PA_1 provides an input to the amplifier stage PA_2 and the output of the amplifier stage PA_2 provides an input to the amplifier stage PA_3. As a result, a three-stage power amplifier can provide three output power levels with maximum achievable efficiency.

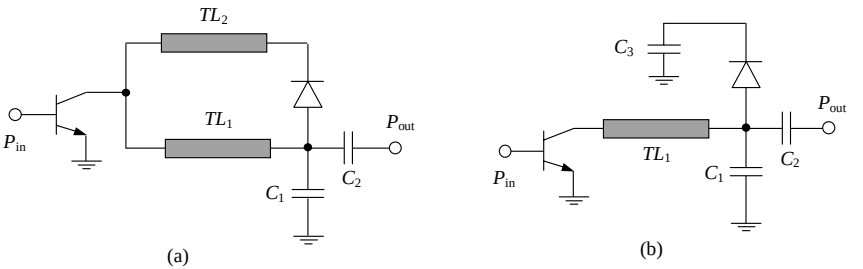

Figure 9.29 Diode-switched load network circuit configurations.

As an alternative to switching the power amplifier paths, it is possible to improve efficiency of the power amplifier operation at a fixed low output power level by providing the impedance transformation between the load and active device using switched circuit arrangements of the load network shown in Fig. 9.29 [35]. The load network shown in Fig. 9.29(a) includes the transmission line TL_1, the parallel capacitor C_1 and the series capacitor C_2 for impedance matching at the highest output power level when the p-i-n diode is switched off, and an additional transmission line TL_2 for impedance matching at the specified reduced power level when the p-i-n diode is switched on. In the latter case, the composite transmission line, consisting of two transmission lines connected in parallel, has a reduced value of characteristic impedance that contributes to an increase of the matching circuit input impedance seen by the device collector. Another circuit configuration of the load network is shown in Fig. 9.29(b). This load network includes the transmission line TL_1, the parallel capacitor C_1 and the series capacitor C_2 for impedance matching at the specified reduced output power level when the p-i-n diode is switched off, and an additional capacitor C_3 for impedance matching at the highest power level when the p-i-n diode is switched on. For practical implementation, it is necessary to choose p-i-n diodes with minimal series resistance and minimize the influence of the diode biasing circuitry on RF performance.

The operational principle of the diode-switched or variable load network configuration is illustrated in Fig. 9.30. To maximize efficiency of the power amplifier operation, the load resistance for different output power levels should be different, so as to provide a collector voltage amplitude close to the value of the supply voltage V_{cc} (see Eq. (9.2)). This means that the load line angle at lower output power levels becomes smaller, so that the smaller collector current amplitude corresponds to approximately the same collector voltage amplitude as for the higher output power level. Moreover, for lower power levels, the saturation voltage becomes smaller (see collector voltage amplitude corresponding

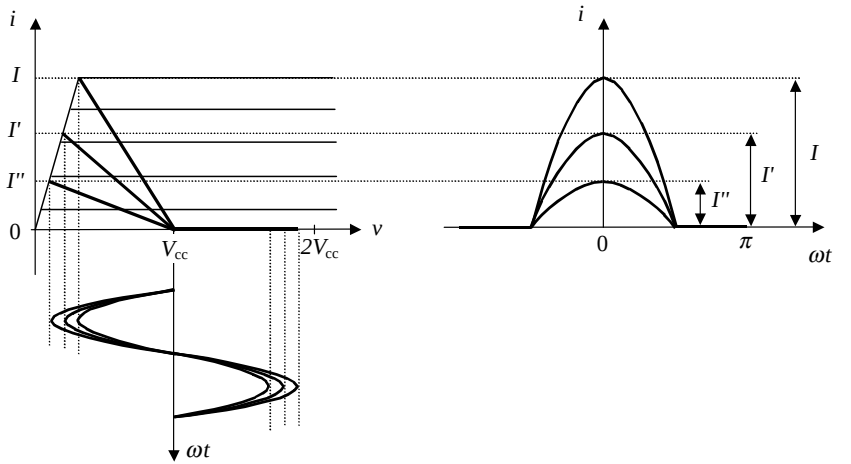

Figure 9.30 Collector voltage and current waveforms for different load lines.

to collector current amplitude I'' in Fig. 9.30) and peak collector voltage is even higher. This smaller load line angle corresponds to the higher value of the load resistance seen from the device collector.

To provide higher efficiency over a wide range of output power levels, the load network configurations with variable circuit elements can be used [36]. In Fig. 9.31(a), a load network topology with variable inductances is shown. The variable inductance can be practically implemented by means of the series connection of a quarterwave transmission line and a varactor diode, as shown in Fig. 9.31(b). The characteristic impedance of a quarterwave transmission line must be sufficiently low, so that the voltage swing across the varactor capacitance is substantially reduced. Using commercially available varactor diodes, it is possible to achieve an approximately constant value of maximum power-added efficiency over the 5-dB dynamic range and more than double improvement in efficiency at the −15 dB backoff output

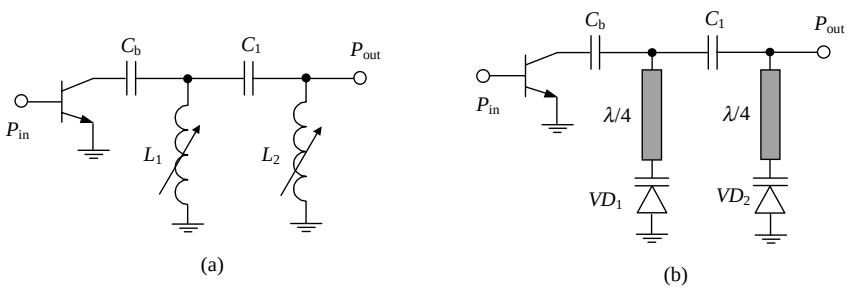

Figure 9.31 Load network configurations with variable circuit elements.

power level. The reverse-bias voltage applied to the varactor diodes should be high enough to minimize the insertion losses and parasitic phase distortion.

Using the diode switches in the load network results in increased size, cost, and circuit complexity, and additional power losses. To improve the performance of the wireless handset transmitter, it is preferable to use two power amplifier paths with different output power levels and a single three-port nonswitchable output load network [37]. Such an approach provides high-efficiency operation at low and medium output power levels with a significant reduction of the overall transmitter power consumption. The basic dual-path two-stage power amplifier schematic with a three-port output matching circuit is shown in Fig. 9.32(a), which also includes a common first stage, a common three-port interstage matching circuit and a dual-path second stage. When it is necessary to transmit a signal with output power between maximum output power $P_{\max}$ and some averaged backoff output power P_{avg}, the low-power amplifier stage with active device Q_3 is turned off. When it is enough to transmit a signal with output power equal to or less than

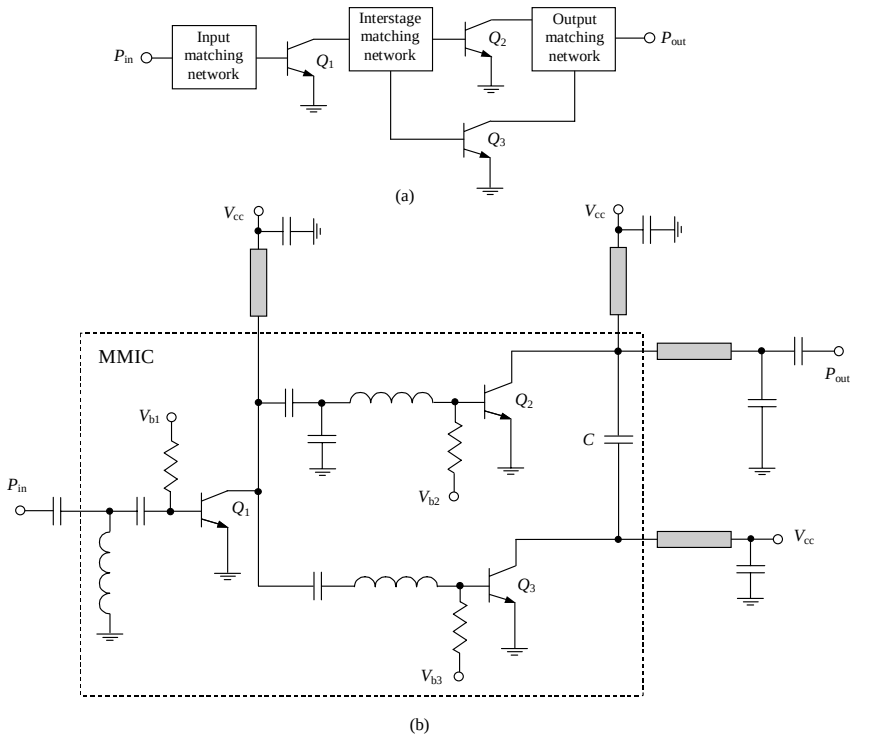

Figure 9.32 Three-port load network configurations of a dual-path power amplifier.

P_{avg}, the high-power amplifier stage with active device Q_2 is turned off. Both transistors are biased in Class AB with a small quiescent current to provide a linear operation. The area of the smaller device Q_3 corresponds to the output power P_{avr} needed by the antenna. The three-port output matching circuit should be configured so that it provides a lower load impedance seen from the collector of the transistor Q_2 to deliver maximum output power P_{max} with maximum achievable collector efficiency and higher load impedance seen from the collector of the transistor Q_3 to maximize collector efficiency at the most probable output power P_{avr}. Since such a dual-path configuration with a single three-port load network does not require additional components other than transistors, it is very practical for single-chip integration without seriously increasing manufacturing cost and size.

Figure 9.32(*b*) shows the circuit schematic of a two-stage InGaP/GaAs HBT MMIC power amplifier [37]. The emitter areas of the transistors for driver stage Q_1, power stage Q_2 and dual stage Q_3 were chosen as 480 μm^2, 1920 μm^2 and 480 μm^2, respectively. The output impedance-transforming circuit is constructed with a series capacitance C. Current mirror circuits located within the integrated circuit were used for transistor biasing. As a result, using Class AB operation with quiescent currents of 10 mA for the devices Q_1 and Q_3 and 40 mA for the device Q_2 and supply voltage of $V_{cc} = 3.3$ V, the power-added efficiency of 16.4 percent was obtained in low power mode with $P_{1dB} = 16.7$ dBm. In high-power mode with $P_{1dB} = 27.6$ dBm, the power-added efficiency was 34.2 percent. Generally, an overall efficiency improvement of at least 1.81 times over a wide power range was provided, compared with a conventional two-stage Class AB power amplifier.

Figure 9.33 shows an alternative approach to realize the dual-path power amplifier using a chain configuration of the output impedance-transforming circuit [38]. The dual-chain two-stage InGaP/GaAs HBT MMIC power amplifier with a single common input and output matching circuits intended for WCDMA handset applications is implemented by parallel integration of two amplifying chains having different output powers. Either the low-power amplifying chain with $P_{1dB} = 16$ dBm or the high-power amplifying chain with $P_{1dB} = 28$ dBm is activated through the bias selection. The matching circuit between the collectors of the output transistors, with series inductance and shunt capacitance composing a simple low-pass L-type matching circuit, allows the power-added efficiency at backoff output powers to be increased by more accurate impedance matching of the higher output impedance of the low-power device and the 50-Ω load resistance. Using such a chain power amplifier configuration, it is possible to obtain the *PAE* of 21 percent at $P_{1dB} = 16$ dBm in low-power mode and the *PAE* of 40 percent at $P_{1dB} = 28$ dBm in high-power mode.

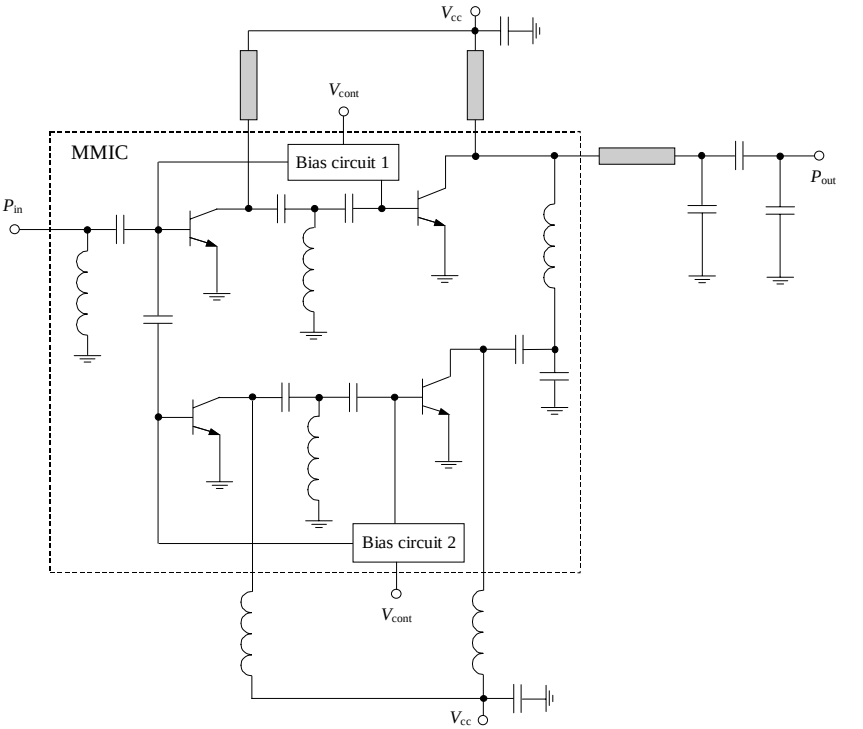

Figure 9.33 Schematic of a dual-chain MMIC power amplifier.

Feedforward Linearizing Technique

Figure 9.34 shows the basic form and principle of operation of the feedforward amplifier [39]. The feedforward system (except the main amplifier) includes three couplers, two phase shifters and an auxiliary error amplifier. The operation of the feedforward linearization circuit is based

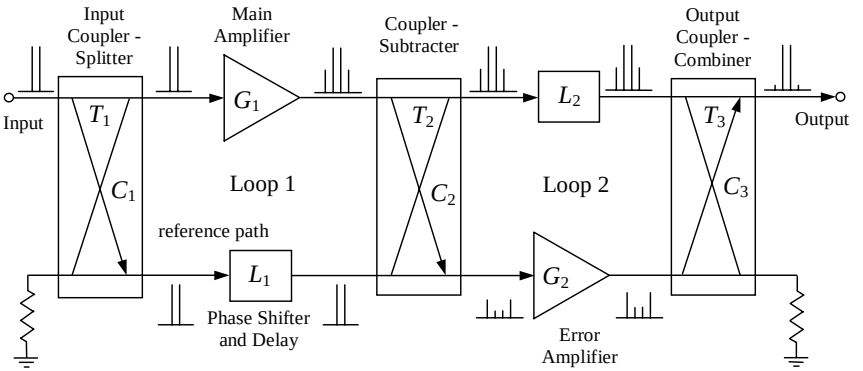

Figure 9.34 Basic operation principle of feedforward amplifier.

on the subtraction of two equal signals with subsequent cancellation of the error signal in the amplifier output spectrum. Its operation principle can be seen clearly from the two-tone test spectra at various points of the block diagram. The input signal is split to form two identical parts, although in a common case the ratio used in the splitting process does not need to be equal. The input directional coupler splits in phase the original input linear signal, which is necessary to amplify without or with minimum additional nonlinear distortion, one part of which forwards to the main amplifier input. Then, one part of the main amplifier's output signal is coupled by the coupler-subtracter, which is usually a 180° hybrid, and a time-delayed and opposite-phase portion of the origin signal are subtracted. The result of this subtraction is an error signal that essentially contains ideally only the nonlinear distortion provided by the main amplifier. The error signal is then amplified linearly to the required level in order to cancel the distortion in the main part, and is fed to the output directional coupler-combiner, on the other input of which a time-delayed and opposite-phase main-path signal is forwarded. The resultant signal at the feedforward linearization system output is error-free in the ideal case, or essentially an amplified version of the original input signal in real practice.

For an analytical evaluation of such a feedforward linearization system, define the cancellation that is achieved by each independent feedforward loop as the power ratio of the suppressed signal over the reference signal corresponding to the open loop configuration. Then, assume that the signal in each upper and lower path of the first loop is pure cosinusoidal and can be written as

$$V_1 = V_{1\mathrm{m}} \cos \omega t \tag{9.22}$$

$$V_2 = V_{2\mathrm{m}} \cos (\omega t + \phi_1) \tag{9.23}$$

where $V_{2\mathrm{m}} = V_{1\mathrm{m}} \pm \Delta V_{1\mathrm{m}}, \phi_1 = 2\pi + \theta_1, \Delta V_{1\mathrm{m}}$ is the amplitude deviation, and θ_1 is the phase imbalance.

An averaged normalized suppressed signal power at the loop output can be calculated from

$$P_{\mathrm{avg}} = \frac{V_{1\mathrm{m}}^2}{2} + \frac{(V_{1\mathrm{m}} \pm \Delta V_{1\mathrm{m}})^2}{2} + 2V_{1\mathrm{m}}(V_{1\mathrm{m}} \pm \Delta V_{1\mathrm{m}}) \cos \theta_1 \tag{9.24}$$

Thus, the cancellation performance when the reference normalized signal is defined as

$$P_{1\mathrm{avg}} = \frac{V_{1\mathrm{m}}^2}{2} \tag{9.25}$$

can be written in decibels for the first loop in the form of

$$CANC_1 = 10\log_{10}\left(1+\alpha_1^2-2\alpha_1\cos\theta_1\right) \tag{9.26}$$

where $\alpha_1 = \left(V_{1\mathrm{m}} \pm \Delta V_{1\mathrm{m}}\right)/V_{1\mathrm{m}}$ is the amplitude imbalance in the first loop.

Similarly, the cancellation in decibels achieved by the second loop can be calculated by

$$CANC_2 = 10\log_{10}\left(1+\alpha_2^2-2\alpha_2\cos\theta_2\right) \tag{9.27}$$

where α_2 and θ_2 are the amplitude and phase imbalance in the second loop, respectively.

Let us evaluate the cancellation provided by both the first and second loop through the parameters of the feedforward system, as shown in [40]. As a result, at the output of the second coupler with suppressed carrier P_{supp}, the cancellation of the first loop can be written as

$$CANC_1 = \frac{P_{\mathrm{supp}}}{C_2 P_{\mathrm{main}}} \tag{9.28}$$

where C_2 is the coupling coefficient of the second coupler-subtracter, and P_{main} is the carrier power level of the main amplifier. On the other hand, the cancellation achieved in the second loop is

$$CANC_2 = \frac{P_{\mathrm{IM3supp}}}{P_{\mathrm{IM3main}}}\frac{1}{T_2 L_2 T_3} \tag{9.29}$$

where P_{IM3main} is the power level of the third-order intermodulation component, P_{IM3supp} is the power level of the third-order intermodulation component of the main amplifier (suppressed at the linearizer output due to the corrective action of the second loop), L_2 is the delay line losses in the second loop, and T_2 and T_3 are the transmission losses in the second and output couplers, respectively.

The effective cancellation of the overall feedforward linearization system is the ratio of the power level of all intermodulation components at the system output over the power level of the intermodulation products for open-loop configuration. As a result, for in-phase addition of the intermodulation components of the main and error amplifiers, the effective cancellation in decibels can be expressed by

$$CANC_{\mathrm{eff}} = 20\log_{10}\left[\sqrt{CANC_2}+\sqrt{CANC_1^3\left(\frac{IP_{3\mathrm{main}}}{IP_{3\mathrm{error}}}\right)^2\frac{T_2^2L_2^2}{\alpha_2^3}\left(\frac{T_3}{C_3}\right)^2}\right] \tag{9.30}$$

where the amplitude imbalance α_2 is defined as the ratio of the power gain of the two paths in the form of

$$\alpha_2 = \frac{T_2 L_2 T_3}{C_2 G_2 C_3} \tag{9.31}$$

where G_2 is the gain of the error amplifier, C_3 is the coupling coefficient of the output coupler, and $IP_{3\text{main}}$ and $IP_{3\text{error}}$ are the third-order intercept points of the main and error amplifiers, respectively.

The first term in Eq. (9.30) depends on the balance level achieved in the second loop, whereas the second term defines the possible imbalance created by the first loop and some other feedforward circuit parameters. In particular, an error amplifier with too low power capabilities, with an insufficiently small value of $IP_{3\text{error}}$, or having too big a coupling coefficient C_3 of the output coupler and losses ($T_2 L_2 T_3$) through the main path, increases the effect of the amplitude and phase imbalances.

The relationship between the overall feedforward system efficiency η and the efficiencies of the two amplifiers, η_{main} for the main amplifier and η_{error} for the error amplifier, when the losses ($T_2 L_2 T_3$) through the main path are considered as negligible, can be written as [41]

$$\eta = \frac{\eta_{\text{main}} \eta_{\text{error}} C_3 (1 - C_3)}{\eta_{\text{error}} C_3 + \eta_{\text{main}} f_{\text{main}} (1 - C_3)} \tag{9.32}$$

where $\log_{10} f_{\text{main}} = -(C/I)_{\text{main}}/10$, $(C/I)_{\text{main}}$ is the carrier-to-intermodulation ratio of the main amplifier. Provided the optimum value of C_3, which maximizes the overall efficiency η when the other parameters are fixed, maximum $\eta_{\max}$ can be given by

$$\eta_{\max} = \eta_{\text{main}} \Big/ \left(1 + \sqrt{\frac{\eta_{\text{main}}}{\eta_{\text{error}}} f_{\text{main}}} \right)^2 \tag{9.33}$$

As an example, the feedforward linearization technique was applied to the 1.855 GHz power amplifier with 37-dBm output power, 37-dB power gain with 1-dB flatness and phase variations within 5° in the operating frequency bandwidth of 30 MHz [42]. Using MRF6404 device, the level of the third-order intermodulation components of the power amplifier was only –24 dBc under a two-tone test signal measurement. As a result, with cancellation performance of the first linearization loop of 45 dB, the third-order intermodulation components of the implemented feedforward power amplifier were reduced to −61 dBc.

Predistortion Linearization

To achieve simultaneously high efficiency and low distortion operation, it is possible to use a predistortion linearizer, which provides positive

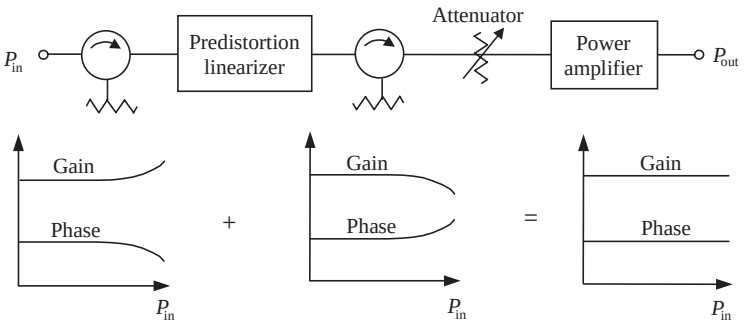

Figure 9.35 Block diagram of power amplifier with predistortion linearizer.

amplitude and negative phase deviations for the RF input signal to compensate the intrinsic active device nonlinearity. The block diagram of a power amplifier with a predistortion linearizer, with indication of the appropriate amplitude and phase performances, is shown in Fig. 9.35. A linearized power amplifier usually includes two isolators for stable operation conditions and an attenuator for adjusting the input signal level.

One of the possible configurations of the predistortion linearizer is based on splitting the input signal into two paths using a directional coupler or hybrid divider: the nonlinear path through the nonlinear active circuit and linear one with subsequent subtraction in the output coupler-subtracter [43]. A block diagram of such a predistortion linearizer is presented in Fig. 9.36. The nonlinear path contains a power amplifier that allows for the required positive shift of the phase characteristic. The appropriate length of microstrip line compensates for the additional phase shift provided by the active device, whereas the required amplitude conditions are realized by the coupling coefficient of the output coupler-subtracter to be chosen. As a result, for an *X*-band multicarrier 4.5-W power amplifier, the phase deviation of a 12-dBm signal at the linearizer output up to -10° was realized with a 22-dBm signal at the linearizer input.

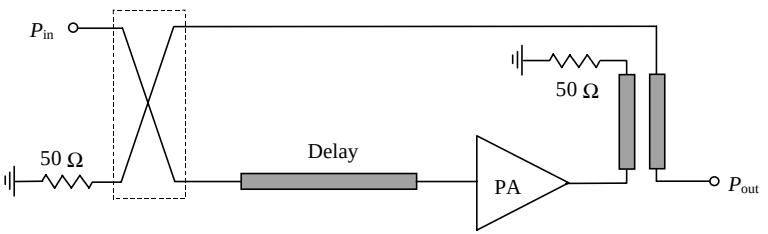

Figure 9.36 Block diagram of power amplifier with input power splitting.

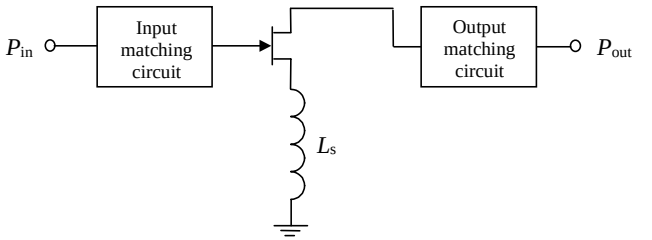

Figure 9.37 Linearizer with series feedback inductance.

Positive amplitude deviation with negative phase deviation can also be achieved using a series feedback amplifier with a large source inductance L_s, a block diagram of which (including matching circuits) is shown in Fig. 9.37 [44]. The required amplitude and phase deviations are due to the nonlinearity of the GaAs MESFET transconductance g_m, gate-source capacitance C_{gs} and drain-source conductance G_{ds}. For the device with a gate width of 1.2 mm, a nonlinearity of g_m contributes to the positive amplitude deviation for $L_s = 20$ nH. At the same time, the nonlinearities of g_m and G_{ds} contribute to a negative phase deviation for $L_s \geq 3$ nH. A nonlinearity of C_{gs} has a negligibly small effect on both the amplitude and phase deviations. As a result, for a linearizer with $L_s = 16$ nH at an operating frequency of 1.9 GHz, the positive amplitude and negative phase deviations were obtained for the input power dynamic range from 5 to 18 dBm, with amplitude deviation of 2.5 dB and phase deviation of 30° at 18-dBm input power. The GaAs MESFET device was biased under Class AB operation with drain-source supply voltage of 2 V and a quiescent current of 78 mA. Applying this technique to a 1.9 GHz MMIC power amplifier with 1-dB compressed power of 17 dBm can achieve an improvement in *ACPR* of up to 7 dB when it is used for $\pi/4$-shift quadrature phase-shift keying (QPSK) signal.

However, it is possible to achieve positive amplitude and negative phase deviations using only a source-grounded MESFET device with zero drain-source bias voltage [45]. The schematic diagram of such a linearizer is presented in Fig. 9.38. In this case, for the device with a gate width of 240 μm and saturation power of 20 mW under gate bias condition of $V_g = -0.4$ V, a 3-dB increased gain and about 30° negative phase performance were achieved due to the drain-source resistance variation. Because of its simplicity, a linearizer can operate from 2 to 12 GHz with good thermal stability. This linearizer has been adopted into a 50-W solid-state power amplifier system at 7 GHz, which allows its noise-power ratio to be improved over the 15-dB dynamic range, in particular in the 2 dB at 3-dB output backoff point.

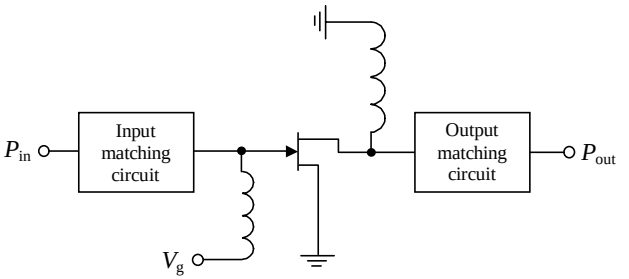

Figure 9.38 Linearizer with zero drain-source bias.

A simple diode linearizer can be used to improve the intermodulation distortion. Being composed of a series Schottky diode VD_1 and a parallel capacitor C_p with two bias chokes for dc feed and two blocking capacitors, as shown in Fig. 9.39(a), it provides positive amplitude and negative phase deviations with the increase of input power [46]. An equivalent circuit of the series diode is presented in Fig. 9.39(b), where R is the diode equivalent resistance and C_j is the junction capacitance. With the increase of incident input signal power, the forward diode current increases, which leads to a decrease of the diode resistance R. In this case, the positive amplitude and negative phase deviations can be achieved under low forward bias conditions when the diode current ranges from 0.1 to 1.0 mA; in the latter case, the phase deviations can reach a deviation of -30°. Applying such a linearizer to a 1.9-GHz MMIC power amplifier, an improvement of *ACPR* up to 5 dB was achieved for the QPSK modulated signal. The MMIC power amplifier has a linear gain of 35 dB and saturation power of 22.5 dBm. When the output power is less than 15 dBm, a 5-dB improvement can be realized.

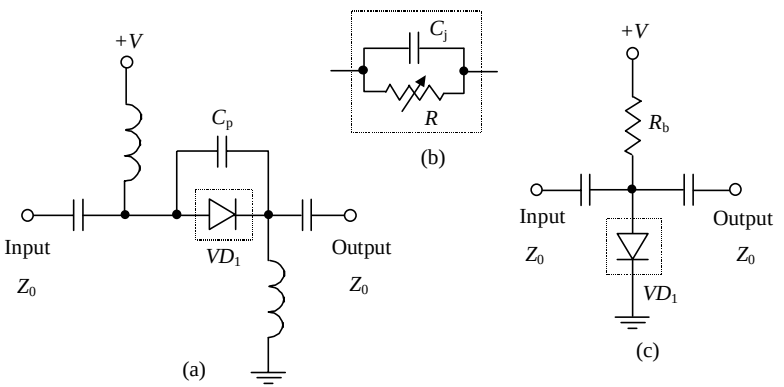

Figure 9.39 Simple diode-based linearizers.

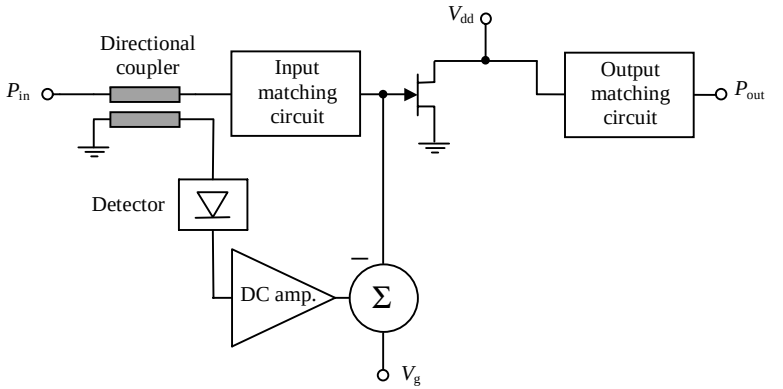

Figure 9.40 Circuit diagram of gate-bias compensation technique.

A similar improvement of *ACPR* can be achieved by a linearizer using a parallel Schottky diode VD_1 with a bias feed resistor R_b (see the simplified circuit in Fig. 9.39(*c*)) [47]. With the increase of input power, the bias point of a diode is changed due to the voltage drop across the resistor R_b caused in turn by the increased diode forward current. As a result, due to the decreased diode resistance R, the linearizer achieves positive gain and negative phase deviations. By applying such a linearizer to a 2.7-GHz power amplifier, a maximum improvement of 5 dB was achieved for low quiescent current conditions at output power of 34.1 dBm.

Another approach for improving the intermodulation distortion is based on using a transistor gate-bias compensation controlled by the input signal level of the power amplifier [48]. Figure 9.40 shows a circuit diagram of the gate-bias compensation technique for a 6-GHz MESFET amplifier including an active device with matching circuits. The detected portion of input signal from the diode detector is amplified and subtracted from the gate-bias voltage so that, when the input power increases, the gate bias becomes more negative. This results in the decrease of both the amplifier gain and the third-order intermodulation product, which reduces more rapidly than the gain. As a result, such an improvement can achieve 10 dB for large input signals in Class AB operation when the optimum bias point is chosen.

Figure 9.41 shows a power amplifier module with adaptive predistortion developed for CDMA handset application in a frequency range of 887 to 925 MHz [49]. The block diagram of the power amplifier module includes additionally a gain-controlling block, a phase-controlling block, two signal-envelope detectors and a CMOS integrated circuit that incorporates two look-up tables to linearize the amplitude-amplitude modulation (*AM/AM*) and amplitude-phase modulation

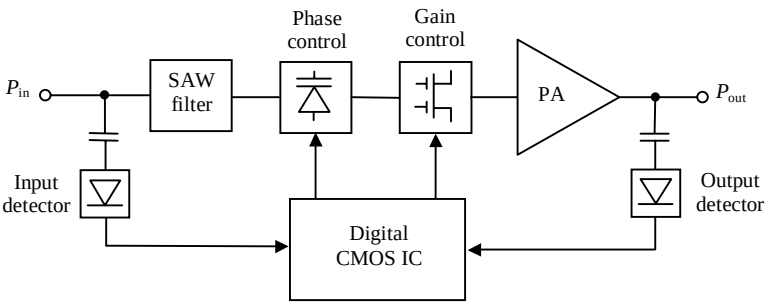

Figure 9.41 Block diagram of a power amplifier with digital adaptive predistortion.

(*AM/PM*) characteristics. A dual-gate MOSFET is used to linearize the *AM/AM* characteristic, which can easily vary the power gain by controlling its second gate-bias voltage in a range of more than 10 dB. In the phase-controlling block, a varactor diode with the phase range of more than 10° was used. By producing appropriate *AM/PM* predistortion data, including the phase characteristics of the dual-gate MOSFET and the following PA block, the total *AM/PM* can be linearized. Because the variations of phase with supply voltage and temperature were insignificant (according to the measurement results), it was sufficient to use the look-up table with modified initial data to minimize the phase variations against input power that were predictable in advance. To linearize the *AM/AM* characteristic, adaptive predistortion was used by modifying the data in the look-up table during the linearization process. It was found that the allowable time delay must be less than 40 ns for a CDMA signal. As a result, using the adaptive predistortion mechanism for only the *AM/AM* characteristic, the *PAE* was increased up to 48 percent for the output power of 27.5 dBm and *ACPR* of −49 dBc. The CMOS integrated circuit, of size 2.5×2.5 mm^2, consumed about 15 mA.

Monolithic CMOS and HBT Power Amplifiers for Handset Application

In monolithic integrated circuit design, it is very important to minimize the area in order to reduce cost. However, the design for high-power monolithic power amplifiers can take advantage of the large device area, for a large gate width for FETs or emitter area for bipolar transistors, available on a monolithic integrated circuit. The required high output power level is realized by the combination of elementary cells: for example the use of the simple parallel connection shown in Fig. 9.42(*a*), which requires too much entire geometry width, or the use of a transmission-line divider and combiner shown in Fig. 9.42(*b*),

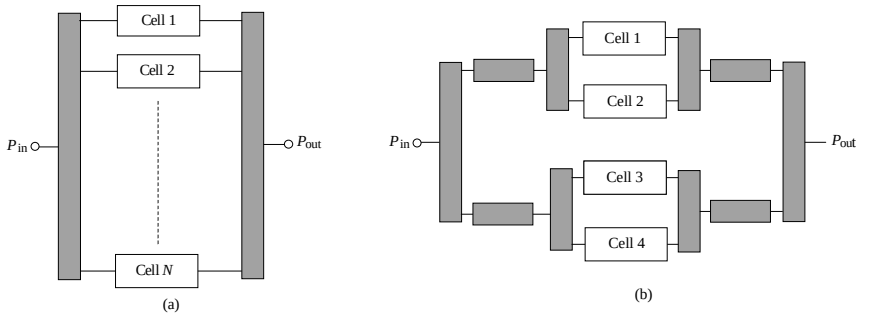

Figure 9.42 Different device cell connections for power combining.

where it is necessary to keep the same length to provide an in-phase operation of all device cells requiring additional MMIC space. The in-phase operation is very important for a high-power device, to prevent excessive heating of any device cell, provide maximum output power delivery to the load, and to realize the high-efficiency operation mode. The last issue is very important when designing the wireless handset transmitter, where the main requirement is to provide long-term operation and low cost. Such an efficient operation condition can be achieved using HBT transistors having minimum on-saturation resistance r_{sat} and high transition frequency f_T. However, in this case, it is necessary to take care about equal current distribution through each HBT cell. Even small differences in cells or their placement can cause a heating imbalance, which can lead to the cell failure causing at the same time a chain reaction failure of the other cells.

For the parallel connection of the device cells shown in Fig. 9.43(a), this problem can be eliminated by using a segmented capacitor with one layer connected to the RF input, and a segmented layer where

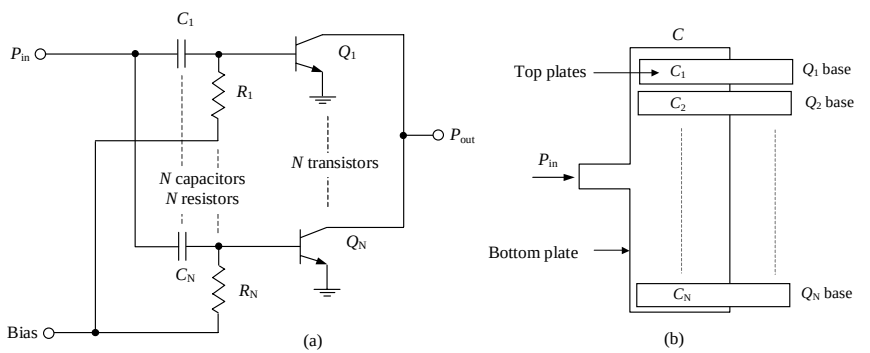

Figure 9.43 Parallel on-chip connection of device cells.

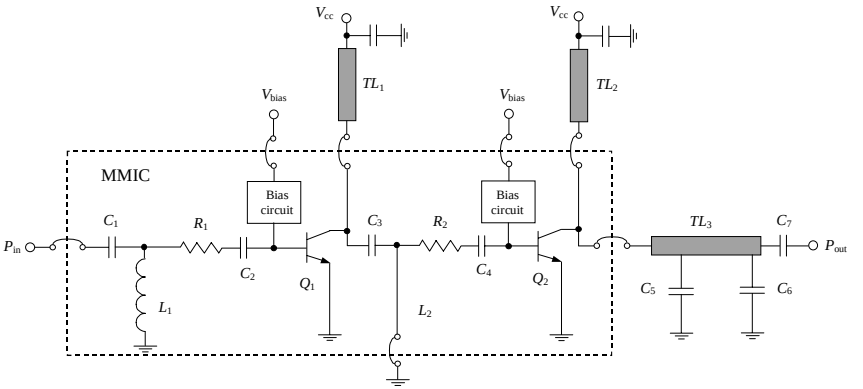

Figure 9.44 Two-stage InGaP/GaAs HBT power amplifier MMIC.

individual segments are dc isolated and connected to each HBT cell base terminal, as shown in Fig 9.43(*b*) [50]. To provide an identical dc current density for each cell, the series base resistances, the values for which are optimized over a wide temperature range, are connected to each cell.

However, when it is necessary to design a power amplifier with two or more stages, it is necessary to arrange at least additional input and interstage matching circuits, which can include, in a common case, several capacitances and inductances. Figure 9.44 shows the electrical schematic of a two-stage InGaP/GaAs HBT power amplifier MMIC designed to operate in a frequency bandwidth of 1.71 to 1.98 MHz [51]. Without any tuning, this power amplifier can provide $PAE \geq 51$ percent and $P_{\text{out}} \geq 30$ dBm over the entire frequency range for saturated mode as well as $PAE \geq 38$ percent and adjacent channel leakage power ratio $(ACLR) \leq -37$dBc at $P_{\text{out}} = 27$ dBm for WCDMA application in a frequency range of 1920 to 1980 MHz. The series resistors R_1 and R_2 are required to provide the stable (without parasitic oscillations) operation conditions. The input matching circuit, in the form of a high-pass *LC*-transformer, provides *VSWR* better than 2:1 over the entire frequency range. Using two sections of a low-pass *LC*-transformer in the interstage matching circuit provides broadband operation by minimizing the impedance sensitivity to its parameter variations. In this case, the first shunt inductance represents a series connection of the bondwire and short-length transmission line TL_1, whereas the second shunt inductance can fully be represented by the bondwire inductance shorted outside of the chip. The load network approximates the parallel-circuit Class E mode (see Fig. 7.40) including the shunt inductance consisting of the bondwire and short-length transmission line TL_2 and two-section low-pass *LC*-transformer using a series microstrip line TL_3. All microstrip lines are implemented by using FR-4 substrate.

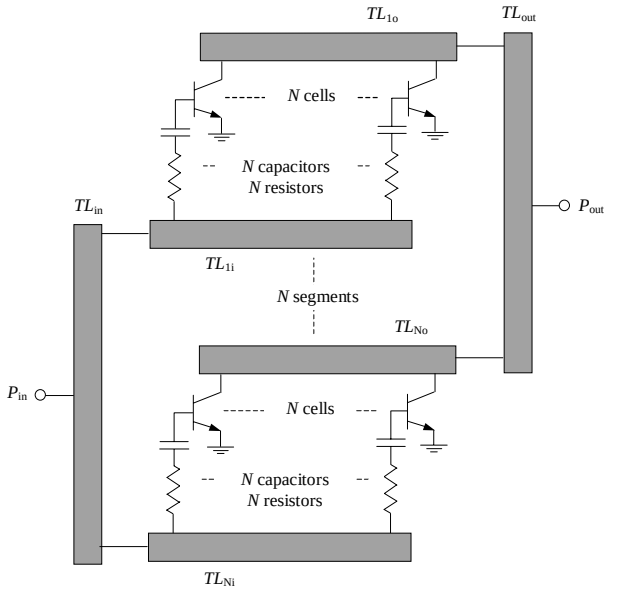

Figure 9.45 Parallel connection of device cell segments.

The emitter area of the HBT transistor is too large for output powers equal to or more than 1 W. In order to minimize the MMIC size, it is advisable to split the overall device into several segments (rows) and then to combine them. Usually the input and output terminals of the segments are connected in parallel, as shown in Fig. 9.45. However, in this case, the distances from the segment terminals to the input or output are different, which causes some phase imbalance. For output terminals, this problem is easily solved by using several bondwires connected in parallel from different points of the output transmission line TL_{out} to off-chip element of the matching circuit. But, for input segment connection, it is difficult to provide the same phase lengths, because it is necessary to incorporate the additional equal length transmission lines directly on the MMIC. Besides, in a common case, it is impossible to use the segmented realization of the interstage capacitor (capacitor C_3 in Fig. 9.44) without extending the MMIC size, as it should provide the equal segments connected to each device base. However, the capacitor profile may differ from rectangular form and the output terminal of the device from the previous stage can be located sufficiently far from the device of the output stage.

Therefore, an alternative approach (shown in Fig. 9.46) is to connect all bases of the output device directly to the second layer of the interstage capacitor C_{int} without segmentation (capacitor C_3 in Fig. 9.44).

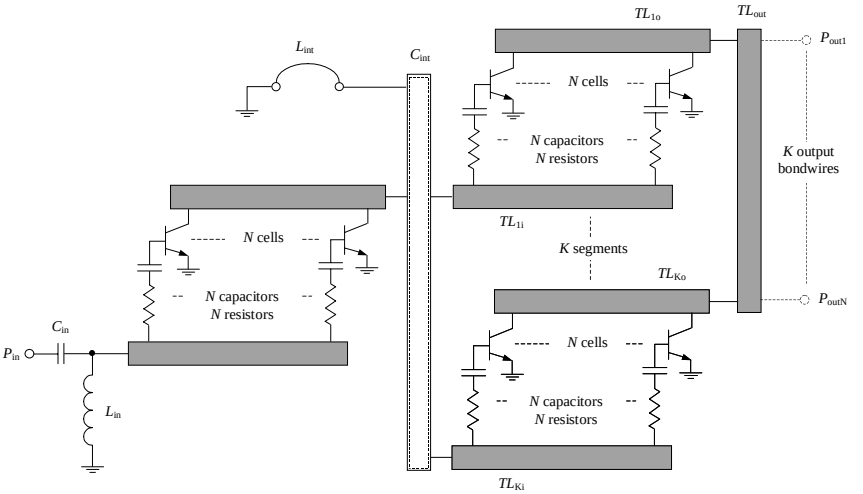

Figure 9.46 Monolithic implementation of two-stage HBT power amplifier.

This approach allows the additional transmission lines to be eliminated (the phase difference between the most far-off cells is less than 5°), to provide the equal input powers flowing into the output device cells and significantly minimize the overall MMIC size. The interstage inductance L_{int} represented by the bondwire (inductance L_2 in Fig. 9.44) can be connected to any point of the first layer of the capacitor C_{int}. The input shunt inductance L_{in} is a typical spiral inductance of square geometry having 3.5 turns. The overall die size of the two-stage power amplifier MMIC shown in Fig. 9.44 was less than 1 mm^2 with emitter areas of the first and second stage of 540 μm^2 and 3600 μm^2, respectively. Such an approach can be applied to any type of MMIC power amplifier.

The MMIC of the three-stage InGaP/GaAs HBT power amplifier shown in Fig. 9.47 contains the RF devices, input matching ciruit, two interstage matching circuits and three bias circuits on a 1.1 mm^2 die. The emitter areas of the first, second and third devices are 180 μm^2, 900 μm^2 and 5760 μm^2. The MMIC implemeted into a 3×3 mm^2 package was mounted on a FR-4 substrate, which contains the output matching circuit and short microstrip transmission lines connected to the 3.5 V voltage supply from each device collector. Standard ceramic chip capacitors were used without additional tuning under the measurement procedure. As a result, in a frequency range of 1.71 to 1.91 GHz the minimum power gain of 33 dB, output power of minimum 32.5 dBm, collector efficiency of 57 percent and *PAE* of 47 percent were obtained. Using a ceramic substrate with high-Q capacitances allowed the power amplifier

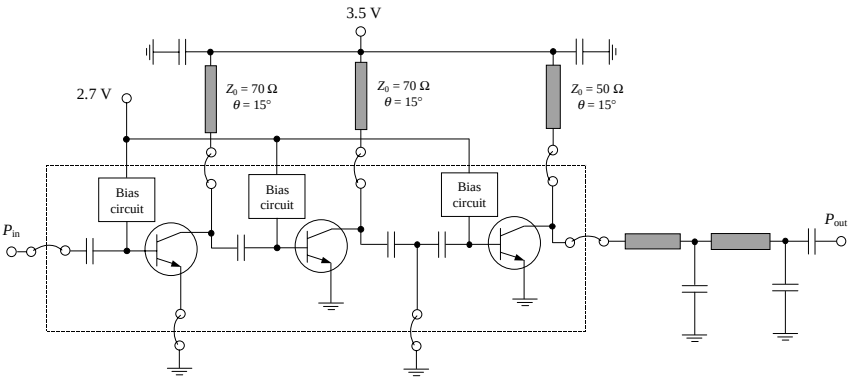

Figure 9.47 Three-stage InGaP/GaAs HBT power amplifier MMIC.

performance to be improved with the collector efficiency of 67 percent and *PAE* of 55 percent, respectively. Under a CDMA2000 test signal at the operating frequency of 1.88 GHz, the power amplifier demonstrated *PAE* of 42 percent and *ACPR* of −46 dBc at $P_{\text{out}} = 28.5$ dBm. An analysis of the simulated collector voltage and current waveforms demonstrates a close proximity to the idealized switched-mode parallel-circuit Class E mode. The collector voltage waveform is very similar to the ideal one with peak factor of about 3. The high value of the saturation voltage of about 0.5 to 0.8 V, resulting in 15 to 20 percent efficiency reduction, is the main reason for the significant efficiency degradation from the ideal 100 percent. Further decrease in efficiency can be explained by violation of the required optimum impedance conditions due to the transmission-line effect at the second and higher-order harmonics and device finite switching time and parasitics.

Implementation into a multichip module (MCM) can reduce significantly the overall size of the power amplifier. For example, using a multilayer substrate consisting of three resin and four conductor layers having thermal via holes results in the MCM size of $7 \times 7 \times 1.9\ \text{mm}^3$ [53]. All chip elements and RF lines were located on the top resin layer with a dielectric constant of 10.5. The dc bias voltage was supplied through the third conductor layer. An HBT cell with a $3 \times 20\ \mu\text{m}^2$ emitter area showed a dc current gain of about 150 at a collector current density of 104 A/cm^2 and a high collector-emitter breakdown voltage of 20 V. A two-stage InGaP/GaAs HBT power amplifier with emitter areas of the first and second devices of 480 μm^2 and 2880 μm^2 respectively exhibited WCDMA power performance with *PAE* of 46 percent and *ACLR* of −37 dBc at a measured P_{out} of 26 dBm.

Recent progress in CMOS technology has shown their promising future for RF power applications. Much progress has been achieved at the

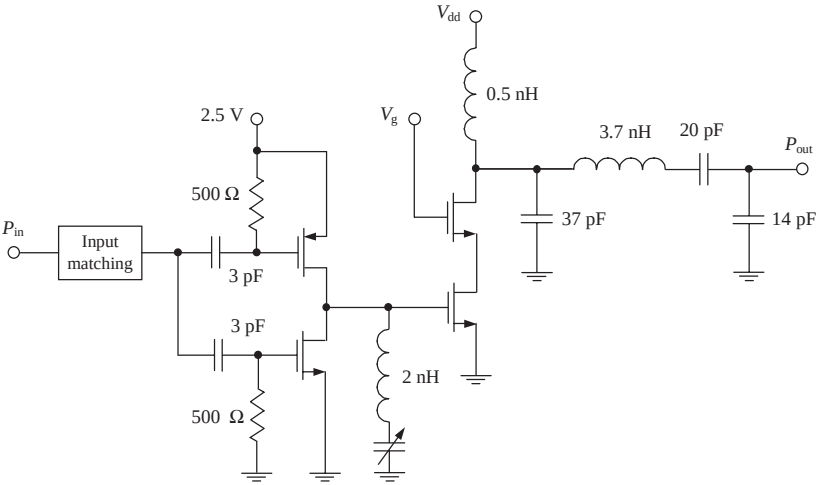

Figure 9.48 Common-gate Class E power amplifier with finite dc-feed inductance [54].

research level, and the obvious possibility to minimize the cost and size of the integrated circuits for RF handset transmitters, especially power amplifier MMICs, makes CMOS technology very feasible and brings considerable economic benefits. However, realizing high-efficiency operation of power amplifiers is limited by some technology issues, such as the high value of the device saturation resistance, low value of the breakdown voltage, and lossy silicon substrate. Therefore, it is vital to apply a high-efficiency technique into the design of the CMOS power amplifiers. For example, a 900-MHz power amplifier based on 0.25-μm CMOS technology with active die area of 2×2 mm^2 can provide an output power of 0.9 W and a power-added efficiency of 41 percent using a Class E load network with shunt capacitance and finite dc-feed inductance, the circuit schematic for which is shown in Fig. 9.48 [54]. To minimize the voltage stress on the switching transistor and maximize the allowable supply voltage, the cascode connection of two nMOS devices is used, which allows the supply voltage to be as high as 1.8 V. Since a cascode switch has higher on-resistance per unit channel width than a single common-source switch during on-state mode, wider devices of 15-mm gate widths are used. The interstage bondwire inductance of 2 nH and external capacitance is used to resonate out the gate capacitance of the cascode device. Since the quality factor of the on-chip spiral inductors in a typical CMOS device is low because of a large loss in the silicon substrate and metal layers, the bonding wires can be successfully used, having less than 5 percent inductance variation and less than 6 percent Q-factor variation as a result of the machine-bonding process.

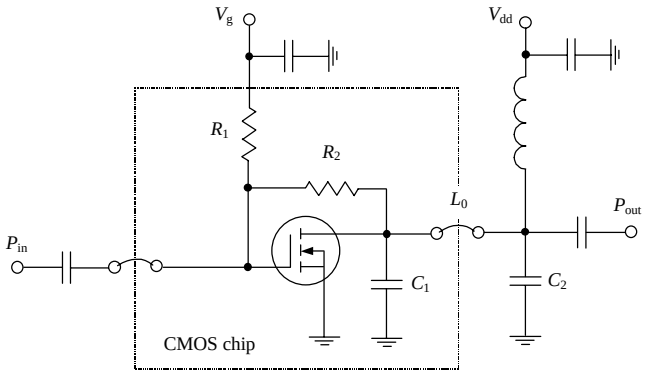

Figure 9.49 RF CMOS inverse Class F power amplifier schematic.

So, the complete power amplifier load network consists of two aluminum bondwire inductors and one on-chip (37 pF) and two off-chip (20 pF and 14 pF) capacitors. The implemented power amplifier is differential and baluns were used at both input and output to combine the two single-ended paths. Using an injection-locked oscillator technique and differential circuit topology implemented in 0.35-μm CMOS technology, the Class E power amplifier is capable of providing *PAE* of 41 percent and P_{out} of 1 W at the operating frequency of 1.98 GHz [55].

Figure 9.49 shows an inverse Class F CMOS power amplifier with second harmonic peaking implemented in a 0.6-μm CMOS standard double-poly double-metal technology [56]. The MOSFET device has a gate length of 0.6 μm and a gate width of 1200 μm. The load network consists of the shunt on-chip capacitance C_1, the series bondwire inductance L_0 and the shunt off-ship surface-mount device (SMD) capacitance C_2. At the second harmonic, the capacitance C_2 acts as a short circuit because of the self-resonance condition with series parasitic inductance. At the same time, the capacitance C_1 and bondwire inductance L_0 are tuned on the second harmonic providing a second harmonic peaking at the device drain. To stabilize the power amplifier operation, the feedback resistance R_2 is connected. As a result, at 1.9 GHz with 3-V supply voltage, the small-signal gain of 10.5 dB, saturated output power of 22.8 dBm and maximum *PAE* of 42 percent were achieved. However, the level of the third-order intermodulation component IM_3 at high output powers is sufficiently high, being approximately -20 dBc at $P_{\text{out}} = 18$ dBm. A theoretical analysis and measurements of the intermodulation distortion for Class AB operation show that, at the small-signal conditions, IM_3 follows a well-known 3-dB/dB slope. However, because of the different contribution of the device transfer function components, there are two sweet spots where IM_3

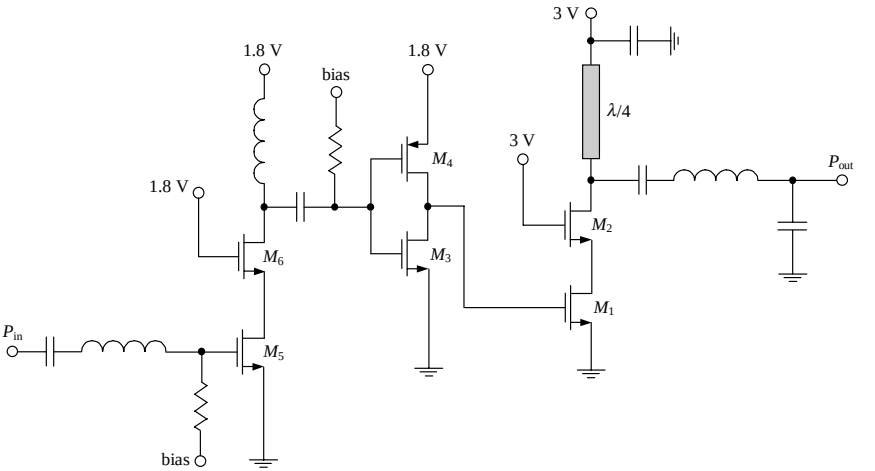

Figure 9.50 Schematic of Class F power amplifier with quarterwave transmission line.

is minimal [57]. The first sweet spot appears because of the turn-on knee region contribution, whereas the second sweet spot close to the output power compression point is due to the combined effects of the quadratic-to-linear and compression transitions of the device transfer function.

Figure 9.50 shows the circuit schematic of a Class F power amplifier implemented in a deep submicron 0.2-μm CMOS technology [58]. The advantage of using Class F operation mode is a substantially smaller drain voltage peak factor compared with Class E mode. This helps to overcome the problem of low oxide breakdown voltage limiting the maximum output power and efficiency of the CMOS power amplifier because of the lower supply voltage required for the device protection. A Class F operation is achieved by using a quarterwave transmission line together with a series resonant circuit in the load network having high impedance at the second and higher-order harmonics. In cascode configuration of the final stage, the thin gate device M_1 is protected by a thick oxide (80 Å) device M_2 with no threat to oxide breakdown under the supply voltage of 3 V. Using a pCMOS device M_4 as an inverter in the driver stage eliminates the problem of the negative voltage swing across the gate of the cascode nMOS device M_1 preventing the forward biasing of its drain junction diode. Operating at 900 MHz, such a CMOS Class F power amplifier can deliver a maximum P_{out} of 1.5 W with *PAE* of 43 percent.

Figure 9.51 shows the simplified schematic of the parallel-amplifier architecture implemented in a 0.25-μm CMOS technology and intended to provide high efficiency at backoff output power levels [59].

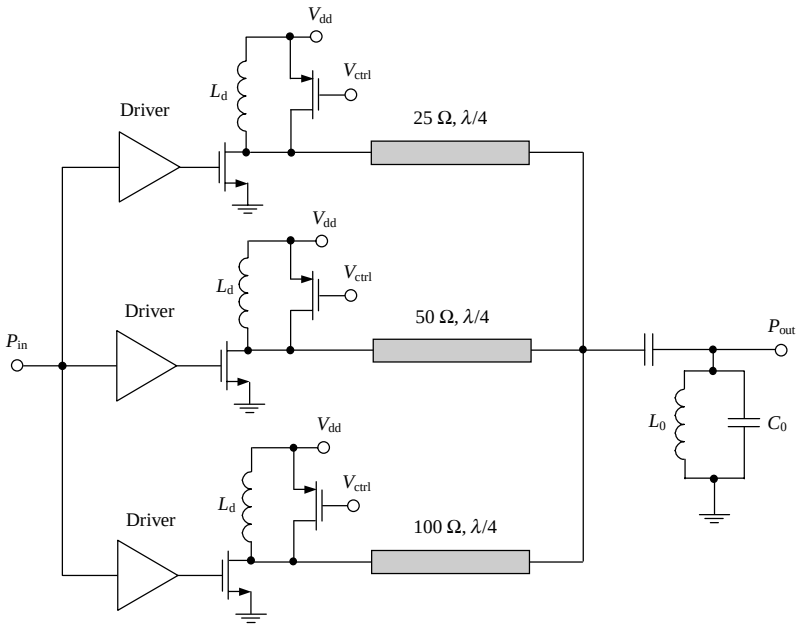

Figure 9.51 Class F parallel-power amplifier architecture.

This architecture employs three binary weighted Class F power amplifiers, the output powers of which are combined in a network based on the use of quarterwave transmission lines loaded on the parallel resonant circuit tuned on the fundamental. The capability to turn off completely each individual power amplifier without interfering with the operation of other individual power amplifiers is provided by the addition of pMOS shorting switches, which result in high impedance at the end of the corresponding transmission line. The power amplifier architecture operating at 1.4 GHz from a 1.5-V supply occupies an active die size of 0.43 mm^2 and achieves *PAE* of 49 percent at maximum P_{out} of 300 mW maintaining a *PAE* of greater than 43 percent over a lower output power range down to 100 mW. The transmission lines are implemented using PCB microstrip lines. On-chip transmission line can be fabricated in CMOS technology using *LC* ladders, making them significantly shorter. For example, the frequency response of ten sections containing a series inductance and a shunt capacitance each can approximate that of the transmission line within 5 percent occupying an area about 14 times smaller. In this case, it is enough to use a spiral inductor to implement both series inductance and shunt capacitance, which can be obtained with the bottom-plate parasitic capacitance of the spiral. However, the maximum *PAE* of the parallel on-chip power amplifier architecture degrades by 10 to 15 percent.

When implementing CMOS power amplifiers in communication systems like GSM/EDGE, WCDMA or CDMA2000 with nonconstant envelope signal when high linearity requirements need to be satisfied, some linearization techniques can be used to obtain simultaneously high efficiency and linear operation. The two main sources of CMOS device nonlinearity are the nonlinear behaviors of its gate-source capacitance and drain current source. For example, for a 0.6-μm CMOS technology, when the transistor turns on and off, the gate-source capacitance C_{gs} changes from approximately 1 pF/mm to almost 0 pF/mm, while the variation of the gate-drain capacitance C_{gd} is negligible [60]. This nonlinearity can be reduced by introducing a parallel inverse nonlinearity at the final stage of the CMOS power amplifier through the use of a pMOS device connected in parallel to the nMOS device, as shown in Fig. 9.52. In this case, no matter what state the transistor is in, the overall input capacitance is always approximately constant. By connecting the drain and source of the pMOS device together, only capacitive current flows into the pMOS device. To minimize intermodulation distortion due to the nonlinear current source, it is necessary to apply a gate bias voltage corresponding to the sweet spot where IM_3 is minimal. To keep good linearity, the driver stage can be used in Class A operation mode. As a result, this technique is capable of improving IM_3 by 10 dB and $ACPR$ by 6 dB for the Class AB power amplifier implemented in a 0.6-μm CMOS technology achieving the maximum

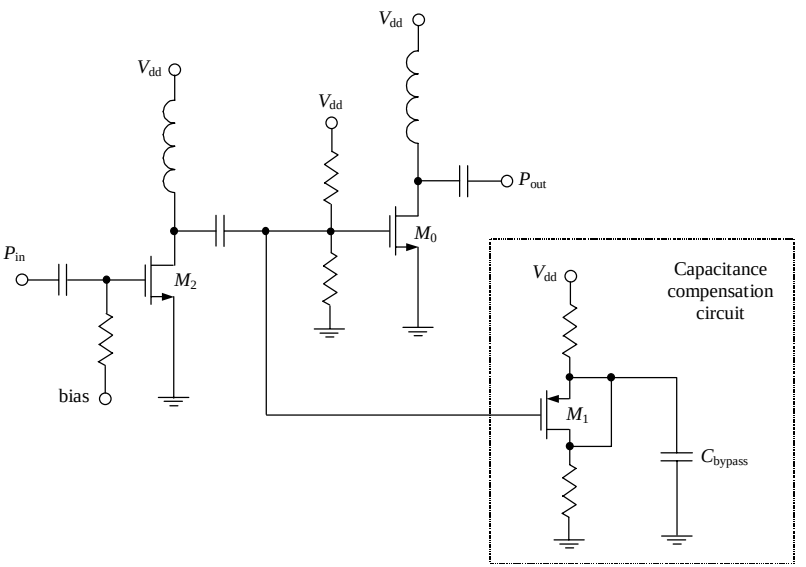

Figure 9.52 Schematic of a two-stage Class AB power amplifier.

output power of 20 dBm and drain efficiency of 40 percent at operating frequency of 1.9 GHz [60].

The gate oxide breakdown and hot-carrier effect are the two most critical issues of deep submicron CMOS device reliability. For example, for 0.18-μm and 0.25-μm CMOS technologies, the breakdown voltages are 5.7 V and 6 V respectively [61, 62]. For a thermally grown silicon dioxide (SiO_2) layer, a field of 7×10^6 V/cm generally leads to irreversible breakdown [63]; therefore, a safety margin should correspond to approximately 6 V across a 30-nm oxide. The electrical field near the corner of the silicon-silicon dioxide (Si-SiO_2) interface, where the drain junction is directly under the gate, is the largest in the device and results in hot-carrier effects: electron injection into the SiO_2 layer producing a gate current; an avalanche hole-electron pair production process, increasing the substrate potential and resulting in the built-in bipolar transistor and current source between the drain and substrate; or punchthrough for shortened channel lengths of less than 1 μm contributing to a drain-source leakage current [63, 64]. So, for high-efficiency operation modes with a large drain voltage peak factor, the device is liable to a hot carrier effect when it is turned off. On the other hand, the device is under significant gate oxide stress when it is turned on having a zero drain voltage. The results of the accelerated stress condition with $V_g = V_{dd} = 5$ V applied to a 0.18-μm nCMOS device demonstrate the significant degradation in the transition frequency f_T, transconductance g_m, third-order intermodulation distortion IM_3 and drift the gate-source capacitance C_{gs} [61]. If the gate breakdown is a catastrophic phenomenon, then the hot carrier effect contributes to a long-term power amplifier performance. Due to this hot carrier effect, the output power of the CMOS power amplifier decreases exponentially and the slope of this decrease becomes sufficiently small after about 70 to 80 h of its operation, suggesting that most of the created trap sites at the Si-SiO_2 interface have been filled by electrons. The recovery of the overall degradation in the output power of about 0.7 dB from its nominal value of 23.1 dBm can be achieved by increasing the gate-bias voltage by 0.2 V [62]. This indicates that the performance degradation is mainly due to the increase in threshold voltage.

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