An Active-Matrix OLED Driver CMOS IC With Compensation of Non-Uniform Routing-Line Resistances in Ultra-Thin Panel Bezel

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***Abstract*— This paper presents a source-driver IC that actively compensates for inter-channel charging rate mismatch in an active-matrix organic light-emitting diode (OLED) display with ultra-thin bezel panel. Due to the limitation of the physical design, the resistances of the driver-to-column routing lines in the panel bezel differ across channels. To solve the luminance non-uniformity caused by resistance mismatch, a digitally controlled g_m-degeneration technique embedded in the output buffer amplifier is proposed. Each driver channel independently compensates for different routing-line resistances, resulting in a charging rate with excellent uniformity. In addition, the bezel area can be desirably minimized without a zigzag wiring pattern. The prototype 240-channel source-driver IC was fabricated using 0.18-μm CMOS technology, and offers a 16.8M-color depth with 13-mW power consumption. With a real OLED display, the measured luminance uniformity under condition of 240-Hz frame rate was improved from $\sigma = 1.43\%$ to $\sigma = 1.01\%$ by the proposed scheme. The inter-channel output deviation was measured to be ±2.7 mV. The video play on 2.4-in OLED panel using a frame rate of 240 Hz was also successfully demonstrated with high display quality.**

***Index Terms*— Active-matrix organic light-emitting diode (AMOLED), bezel, column-driver IC, inter-channel uniformity, output buffer amplifier, *RC*-uniformization, routing lines.**

I. Introduction

TODAY, flat-panel displays utilizing liquid crystal (LC) or organic light-emitting diodes (OLEDs) are mainstream display technologies that play an important role in the information display of electronic devices, such as smart phones, tablet computers, TVs, and digital signage sets [1], [2]. In the field of flat-panel displays, one of the key technologies is the configuration of an active-matrix pixel array composed of rows and columns, fabricated on a large-area glass substrate [3]–[5]. The luminance of each RGB pixel is independently determined by an analog voltage signal supplied from an external multi-channel column (source) driver chip. Therefore, the routing lines connecting the driver IC outputs to the active-matrix column channels must be placed between the bonding pads of the driver IC and the active array [6], [7]. Fig. 1(a) shows the display panel structure with a full-HD (1920 × 1080) resolution. As shown in Fig. 1(a), the driver-to-channel routing lines are located on the top of the panel; this non-active area patterned with the routing lines is generally called the bezel, which is the outside frame area around the displayed area in the glass panel.

Due to the limited physical width of the driver IC, the distance of all routing lines cannot be the same; the length of the routing line connecting to the column channel near the driver IC is relatively short, but the routing line connecting to the channel located on the panel edge is much longer. Different lengths of routing lines induce different parasitic line resistances (R_{Routing}) from column channel to channel. In the micrograph image shown in Fig. 1(b), different lengths of the routing lines can be clearly observed. The different R_{Routing} have a significant effect on the charging rate error of the data-signal driving into the pixel, resulting in the degraded quality of the display image. The charging rate error can be defined as $\exp[-T_{\mathrm{Row}}/RC_{\mathrm{Total}}]$, where T_{Row} is the 1-row assigned driving time and RC_{Total} is the total parasitic RC delay on a driven channel line (R_{Routing} is also included in RC_{Total}). Due to different R_{Routing}, the inter-channel uniformity of the charging rate cannot be guaranteed; thus, a fixed-pattern noise tends to be detected from the display image, as shown in the gradation pattern in Fig. 1(a).

To alleviate the issue of different R_{Routing}, there is a way to reduce the display frame rate (= 1/[number of rows]/T_{Row}). However, the decreased frame rate causes motion artifacts for fast-moving video display. Furthermore, since the one-chip driver solutions have recently been introduced [8], the allowable 1-row driving time (T_{Row}) is getting shorter. To reduce the number of mounted driver ICs, the single source output of one-chip driver is responsible for driving the multiple column channels (1-to-N de-multiplexing) by dividing a traditional 1-row selection time into multiple time intervals. Moreover, the one-chip solution not only shortens the effective T_{Row}, but also severely worsens $\Delta R_{\mathrm{Routing}}$. Note that the number of used driver ICs is considerably limited owing to the one-chip solution; on the other hand, the physical size and the spatial resolution (# of columns) of the display panel continuously increase. Consequently, the non-uniform charging rate issue is likely to be more serious in flat-panel displays.

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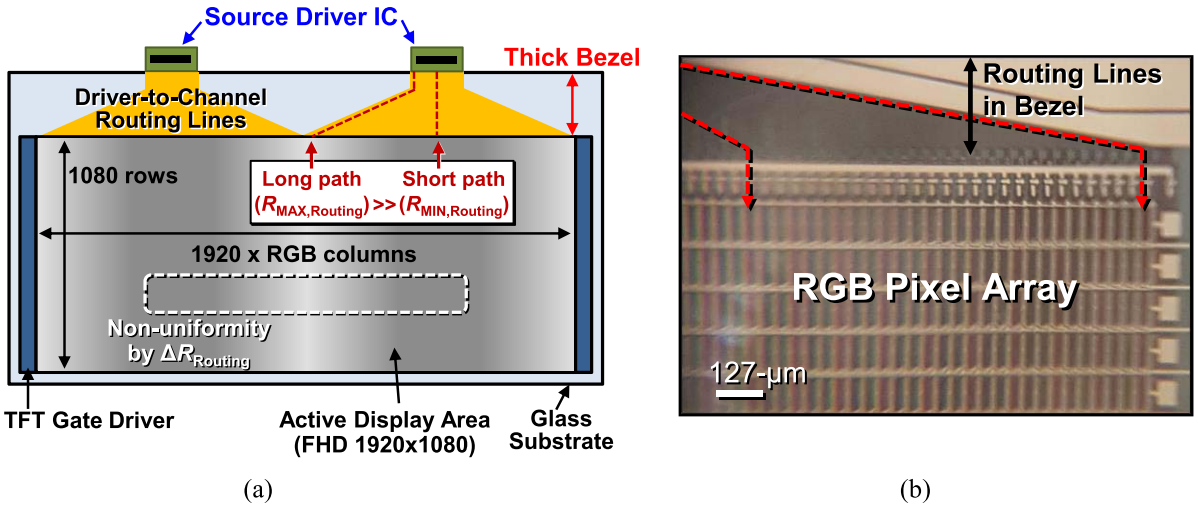


Fig. 1. Driver-to-column routing lines in display panel bezel. (a) Display panel structure with full-HD resolution. (b) Micrograph of routing lines in bezel and RGB active area.

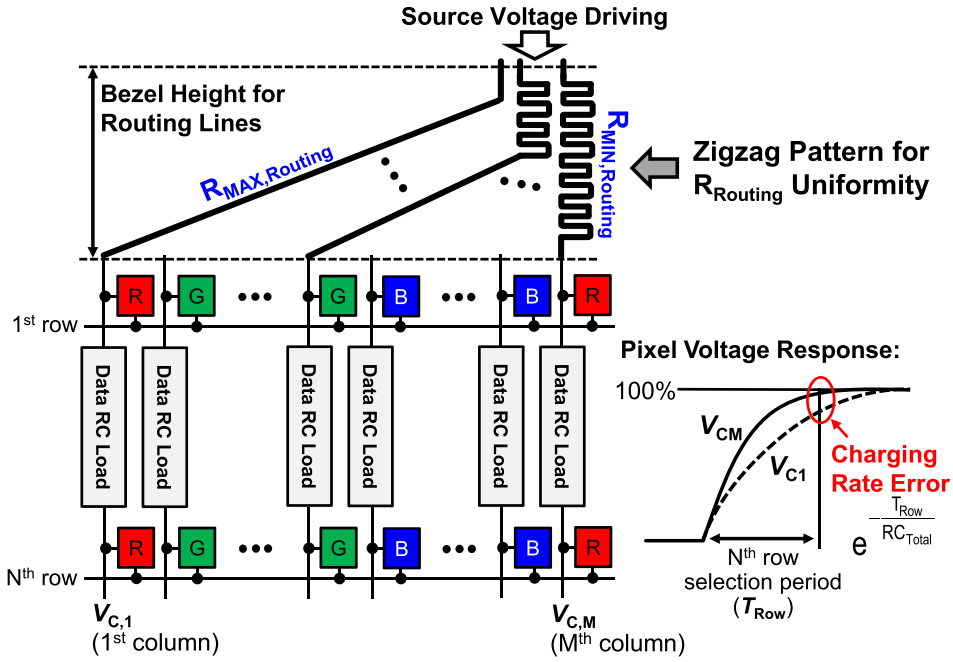


Fig. 2. Charging rate error due to different $R_{Routing}$ and zigzag wiring design to compensate for $\Delta R_{Routing}$.

For compensation of $\Delta R_{Routing}$, the conventional approach involves intentionally increasing the redundant length of the short-distance routing line by zigzag wiring design [6], [7], as shown in Fig. 2. This zigzag wiring induces a greater effective length of the routing line, so it is close to that of the longest routing line; this method improves the mismatch of $R_{Routing}$. However, a side effect of this zigzag-patterning method is that the bezel area becomes to be broadened. In commercial markets, the demand for display products with a very thin bezel is increasing; increasing the bezel thickness is thus not desirable due to the zigzag-patterning method. Actually, the effectiveness of the zigzag wiring approach could be greatly limited. Table I shows several design examples of routing lines in a bezel area and their charging rate error calculations. It should be noted that a charging rate error of $\Delta 1\%$ appears to have a luminance error of 2.56 gray levels, based on an 8-bit gray-scale resolution.

Researchers have recently proposed different LCD and OLED column-driver IC designs to improve the chip-area efficiency versus color depth [9]–[19], to improve the power efficiency versus driving speed [20]–[24], and have suggested novel OLED driving schemes [25]–[27]. Unfortunately, studies have not been reported on the display driver IC to actively compensate for the inter-channel non-uniform charging issue caused by the mismatch of driver-to-channel routing-line resistances ($R_{Routing}$).

TABLE I
DESIGN EXAMPLES OF ROUTING LINES IN BEZEL AND THEIR CHARGING RATE ERROR CALCULATIONS

	32" HD (1366×768) Flat-Panel Display	40" FHD (1920×1080) Flat-Panel Display
Number of driver chips	One chip	Two chips
Column line (S/D layer) metal material	TiCu (600nm thick)	TiCu (500nm thick)
Line width of chip-to-channel routing	6 μm	5.2 μm
Bezel height (routing-line area)	10 mm with zigzag pattern	6 mm with zigzag pattern
$R_{MAX,Routing} - R_{MIN,Routing}$	Δ1.5 kΩ (= 1.8 kΩ – 0.3 kΩ)	Δ1.6 kΩ (= 1.8 kΩ – 0.2 kΩ)
Parasitic *RC* on column line	3 kΩ // 220 pF	3 kΩ // 300 pF
1-row selection period	3.6-μs (FR 120Hz) with 1:3 DeMUX	2.6-μs (FR 120Hz) with 1:3 DeMUX
ΔCharging rate (%) (luminance difference)	$99\%_{MIN} - 97\%_{MAX} = \Delta 2\%$	$93\%_{MIN} - 83\%_{MAX} = \Delta 10\%$

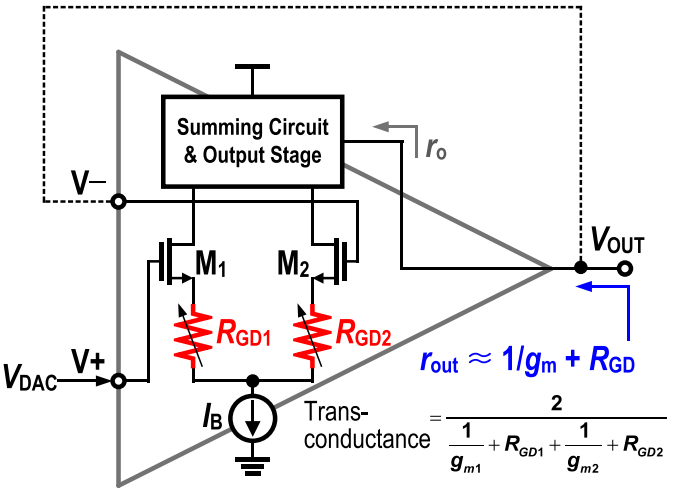


Fig. 3. Proposed technique of g_m-degenerative series resistor (R_{GD}) in input stage of output buffer for compensation of variable $R_{Routing}$.

This paper presents a column (source) driver IC design that actively compensates for non-uniform routing-line resistances ($R_{Routing}$) for an active-matrix OLED (AMOLED) display panel with an ultra-thin bezel. For this purpose, a digitally controlled g_m-degeneration technique embedded in the input stages of the output buffer amplifier is proposed in this paper. In virtue of the proposed technique, each source-driver channel independently compensates for the variable routing-line resistance, resulting in excellent uniformity of charging rate. In addition, the bezel area can be desirably minimized without a zigzag wiring pattern by the proposed driver structure. Moreover, the presented amplifier is also capable of calibrating offset voltage dispersion from channel to channel; thus, the output voltage uniformity can be significantly improved. The proposed AMOLED source-driver IC with 240-channel was designed and verified via CMOS chip fabrication, electrical measurements, and real OLED display demonstrations.

II. PROPOSED COMPENSATION OF NON-UNIFORM ROUTING-LINE RESISTANCES

In general, each source output channel of the driver IC consists of digital circuits for processing serial input data, digital-to-analog converter (DAC), and output buffer amplifier for driving the analog data voltage into a certain pixel in an active-matrix array. In this paper, for compensation of the mismatch of the routing-line resistances on the driving signal path, a transconductance (g_m) degenerative series resistor (R_{GD}) is embedded in the input stage of the output buffer amplifier, as described in Fig. 3. By inserting the $R_{GD1,2}$ in the differential input pair, the equivalent transconductance becomes to be $1/[1/g_{m1,2} + R_{GD1,2}]$ rather than $g_{m1,2}$. Assuming that the feedback-loop gain (A_{Loop}) is equal to $r_o/[1/g_{m1,2} + R_{GD}]$, where r_o is the small-signal open-loop output resistance, the equivalent closed-loop output resistance (r_{out}) of the proposed buffer amplifier can be defined as

$$r_{out} = \frac{r_o}{1 + A_{Loop}} \approx \frac{1}{g_m} + R_{GD}. \quad (1)$$

Therefore, the circuit resistance as an output buffer can be equivalently considered as $(1/g_m + R_{GD})$ on the final signal-transfer path from DAC to pixel. The additionally inserted $R_{GD1,2}$ is digitally controllable by the N-bit register, and this variable series resistor is thus used to maintain the total resistance consistency of $R_{Routing} + R_{GD}$. Fig. 4 illustrates the simplified circuit model of data-signal driving from DAC to pixel. The pixel voltage is first converted from digital data by the DAC, and is driven by the output buffer. The voltage signal is transferred to the target pixel through the driver-to-channel

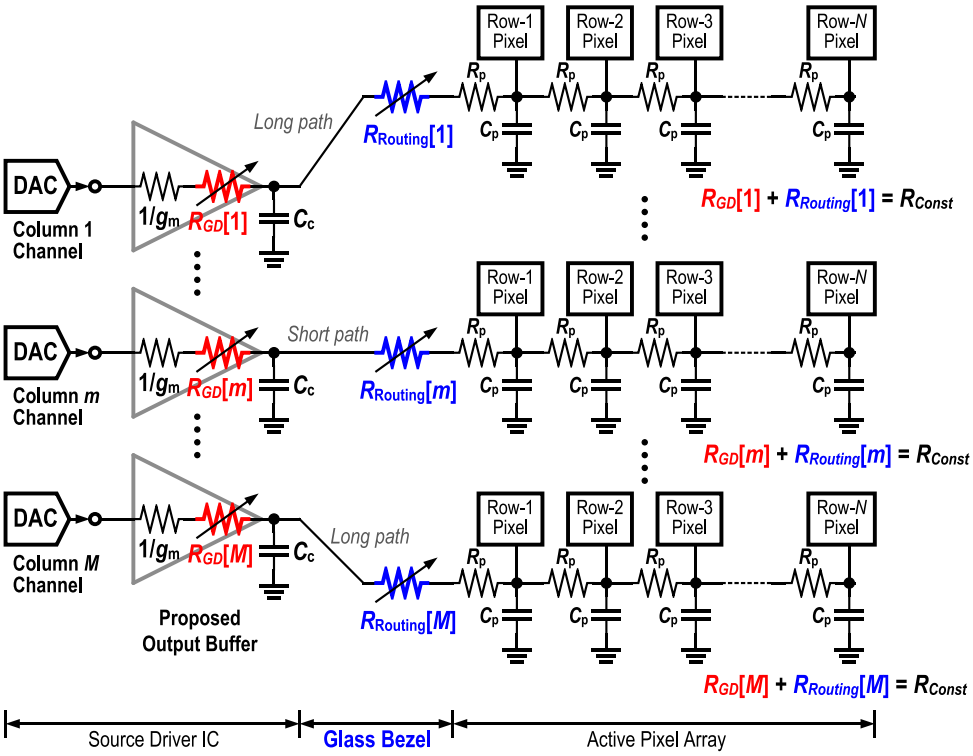


Fig. 4. Simplified circuit model of source-data driving from DAC to pixel via equivalent output buffer resistance, routing-line resistance (R_{Routing}), and data-line parasitic (R_pC_p) network.

routing line (R_{Routing}) and the parasitic R_pC_p network on the data line. The inter-channel non-uniformity of charging rate is caused from the variable R_{Routing}, depending on the effective length of the routing-line patterned on the glass bezel area. The proposed output buffer with R_{GD} compensation results in $R_{\text{GD}}[m] + R_{\text{Routing}}[m]$, which is equivalently connected in series and becomes a constant value (R_{Const}). Accordingly, the charging rate can be well-matched regardless of the R_{Routing} variation from channel to channel.

A further advantage of the proposed circuit design of Fig. 3 is the output offset cancellation. In Fig. 3, the mismatch between the input-pair MOSFETs (M_1 and M_2), that occurred due to process variation, causes the output offset dispersion. Voltages across R_{GD1} and R_{GD2}, determined by mismatched M_1 and M_2 currents, respectively, inversely create the imbalance between the M_1 and M_2 source voltages. Therefore, the independently controllable R_{GD1} and R_{GD2} in the differential input-pair contribute to stabilize the equilibrium current division by the degenerative feedback mechanism, even though M_1 and M_2 are mismatched; this results in reduction of the output offset dispersion across channels. The compensated current division in the differential pair can be expressed as

$$I_{\text{DS1}} = \frac{1}{2}k_{n1}\left(\frac{W}{L}\right)_1\left\{V_{\text{DAC}} - \left[\left(\frac{I_B}{2} + \Delta I_{\text{DS}}\right)R_{\text{GD1}} + V_B\right] - V_{\text{TH1}}\right\}^2 \tag{2}$$

$$I_{\text{DS2}} = \frac{1}{2}k_{n2}\left(\frac{W}{L}\right)_2\left\{V_{\text{DAC}} - \left[\left(\frac{I_B}{2} - \Delta I_{\text{DS}}\right)R_{\text{GD2}} + V_B\right] - V_{\text{TH2}}\right\}^2 \tag{3}$$

where ΔI_{DS} is mismatched current due to M_1 and M_2 mismatch and V_B is the top node voltage of the current source I_B. Fig. 5 shows the simulated offset voltage of our designed buffer amplifier with respect to the intentional W/L-size mismatch between the input-pair M_1 and M_2 in Fig. 3. Incorporating post-calibration, the balance control of R_{GD1} and R_{GD2} contributes to minimize the current-division mismatch of M_1 and M_2. As shown in Fig. 5, it is clearly observed that the offset voltage is significantly improved by the independent control of R_{GD1} and R_{GD2}.

To validate the compensation of $\Delta R_{\text{Routing}}$ by the proposed scheme, the theoretical response analysis in the linear settling regime is as follows. Incorporating the Elmore RC delay model [28], the time constant (τ_{Total}) of the total signal path from DAC to pixel can be defined as

$$\begin{aligned}\tau_{\text{Total}} &= \left(\frac{1}{g_m} + R_{\text{GD}}[m]\right)\cdot C_C + \sum_{i=1}^{N}\left(\frac{1}{g_m} + R_{\text{GD}}[m] + R_{\text{Routing}}[m] + i\cdot R_p\right)\cdot C_p \\ &= \left(\frac{1}{g_m} + R_{\text{GD}}[m]\right)\cdot C_C + \left(\frac{1}{g_m} + R_{\text{GD}}[m] + R_{\text{Routing}}[m]\right)\cdot N\cdot C_p \\ &\quad + \frac{N^2}{2}R_p\cdot C_p \\ &\approx \left(\frac{1}{g_m} + R_{\text{Const}}\right)\cdot N\cdot C_p + \frac{N^2}{2}R_p\cdot C_p \end{aligned} \tag{4}$$

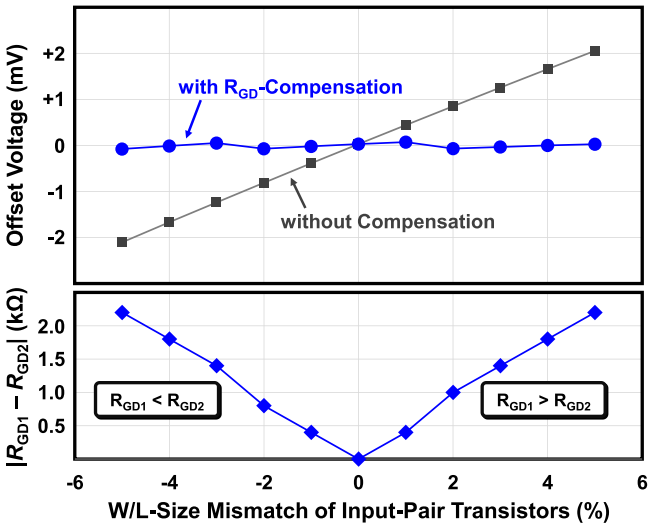


Fig. 5. Simulated offset voltage of buffer amplifier with respect to intentional W/L-size mismatch between input-pair transistors (M_1 and M_2) in Fig. 3.

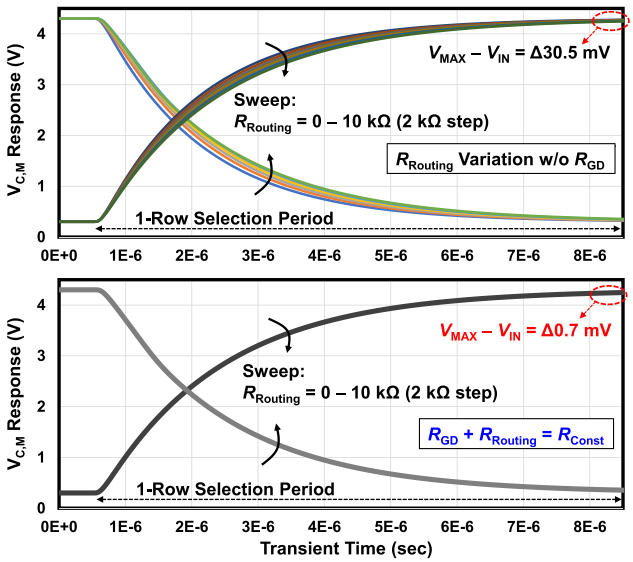


Fig. 6. Simulated transient response corresponding to a unit step input of Δ4 V with a sweep of different R_{Routing} without (top) and with (bottom) proposed compensation scheme.

where m = source channel, C_C = equivalent output capacitance of output buffer, and N = number of rows. Note that C_C is much smaller than $N \cdot C_p$. As can be seen in (4), with the proposed scheme, the variable $R_{\text{Routing}}[m]$ is replaced with the constant value (R_{Const}) by adding controllable R_{GD} in series, and the τ_{Total} dominating charge rate is thus drastically stabilized across the column lines. However, it should be noted that the equivalent output resistance of the buffer amplifier, $1/g_m + R_{\text{GD}}$, in (4) is valid only for the small-signal settling time, and the analysis of (4) can thus be an approximated expression. The signal response including large-signal domain (slewing operation) will be discussed in the next paragraph. Fig. 6 shows the simulated transient response of the pixel voltage by driving a unit step input of Δ4 V with conditions of N = 320 rows, g_m = 25 μS, C_C = 0.4 pF, R_p = 93.8 Ω, C_p = 93.8 fF, R_{Routing} = 0–10 kΩ, and T_{Row} = 8 μs. Owing to the variable routing-line resistance (R_{Routing}), the driven voltage into pixel varies within a range of Δ30.5 mV. On the other hand, the settling voltage dispersion is effectively reduced to Δ0.7 mV with R_{GD} series compensation ($R_{\text{Const}} = R_{\text{GD}} + R_{\text{Routing}}$) by the proposed output buffer amplifier.

With large input steps, the driver output displays a linear ramp having a constant slope in a realistic Op-Amp circuit. Under this condition, the amplifier experiences slewing, and the slope of the ramp is called the slew rate. In addition to the linear settling time discussed above, the slewing response should also be considered to analyze the overall response of the pixel voltage. The slew rate at the output of the buffer amplifier is mainly dominated only by I_B/C_c, where I_B and C_c are the tail current of the input stage and the Miller compensation capacitor, respectively. During that slewing period, the amplifier output signal with fixed slew rate of I_B/C_c is also transferred into the pixel via the parasitic RC loads including the routing resistance $\Delta R_{\text{Routing}}$. Therefore, the response of the pixel voltage could be varied by $\Delta R_{\text{Routing}}$

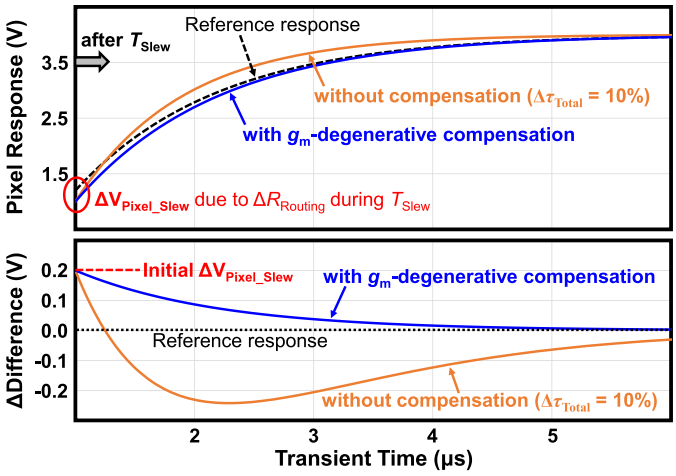


Fig. 7. Simulated transient responses of pixel voltages during linear settling time (after slewing operation) without and with proposed uniformization of τ_{Total}.

during the initial slewing period regardless of the small-signal equivalent output resistance of the buffer amplifier. In general, the slewing operation is performed until the slope of the linear settling response equals the slew rate. Thus, the slewing period (T_{Slew}) can be given by

$$\frac{I_B}{C_C} = \Delta V_{\text{Step}} \omega_{\text{GB}} \exp(-\omega_{\text{GB}} T_{\text{Slew}}) \tag{5}$$

where ω_{GB} is the unity-gain bandwidth in the feedback loop of the buffer amplifier [29]. As discussed before, the proposed circuit design of Fig. 3 improves the slew rate by the reduced C_c; this effectively shortens the T_{Slew} period (quick switch from slewing to the linear settling). By applying realistic values into (5), the slewing period (T_{Slew}) is approximately $4/\omega_{\text{GB}} (\approx 0.1\tau_{\text{Total}})$. During T_{Slew}, the difference $\Delta V_{\text{Pixel\_Slew}}$ between the pixel responses by $\Delta R_{\text{Routing}}$

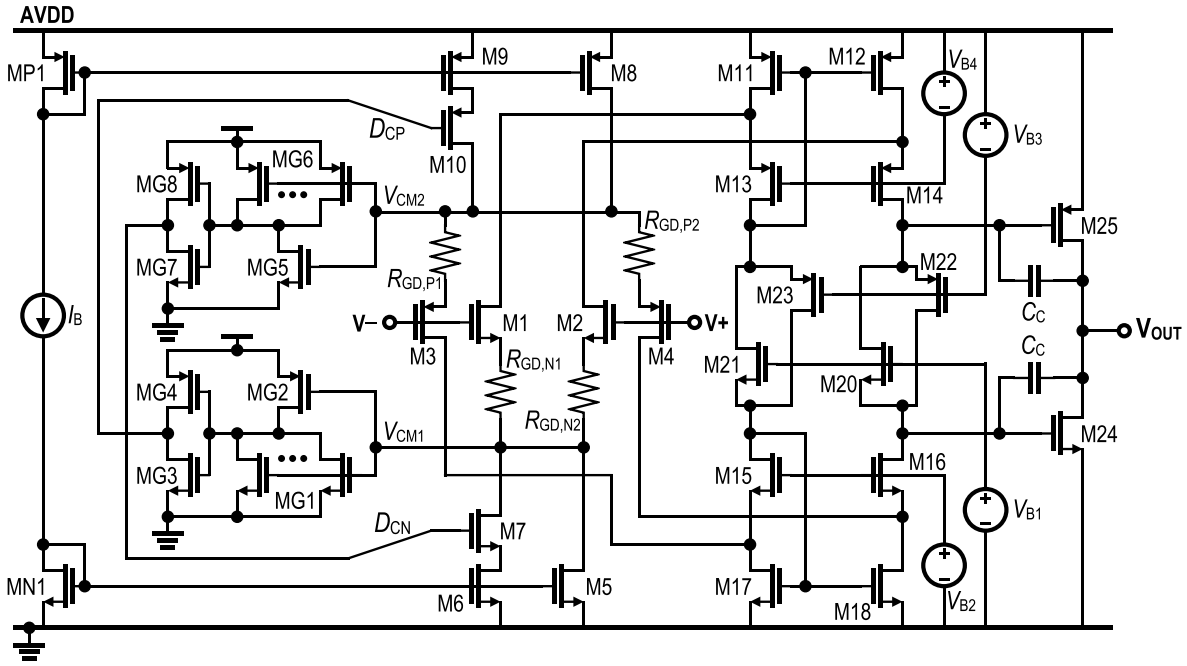


Fig. 8. Circuit schematic of rail-to-rail output buffer amplifier with g_m-degenerative resistor (R_{GD}) and constant transconductance controller.

($= R_{Routing}[m] - R_{Routing}[n]$), occurred by no effect of R_{GD} compensation, can be simplified as

$$\Delta V_{Pixel\_Slew}(\%) \approx \exp\left[-\frac{T_{Slew}}{R_{Routing}[n]\cdot NC_p + R_pC_pN^2/2}\right] - \exp\left[-\frac{T_{Slew}}{R_{Routing}[m]\cdot NC_p + R_pC_pN^2/2}\right]. \quad (6)$$

Nevertheless, the ΔV_{Pixel_Slew} will completely decay with a rate of $\exp[-t/\tau_{Total}]$ during the linear settling time (after T_{Slew}), if the τ_{Total} is well-matched by the proposed compensation scheme. Fig. 7 shows the simulated transient responses of the pixel voltages during the linear settling time (after T_{Slew}) without and with the proposed uniformization of τ_{Total}. As can be seen, in spite of initial ΔV_{Pixel_Slew} induced by no effect of R_{GD} during T_{Slew}, the proposed compensation effectively matches the charging rate in the linear settling regime.

III. Circuit Implementation

A. Output Buffer Amplifier With g_m-Degeneration

The OLED output buffer is realized by the operational transconductance amplifier in an unity-gain configuration, and is utilized to drive the parasitic R_pC_p network on the date line (column line). In addition, the output buffer should offer an almost rail-to-rail output voltage swing in order to accommodate a wide full-scale voltage range of a large number of gray levels. In this paper, considering that the ELV_{DD} (which is a source voltage of the P-type drive thin-film transistor (TFT) in the OLED pixel) is designed to be 4.6 V, the output buffer must be able to drive from 4.3 V (black) to 0.2 V (full gray level) under a 5-V power supply.

As illustrated in Fig. 8, the proposed buffer amplifier circuit is designed, based on the architecture of [30] to support

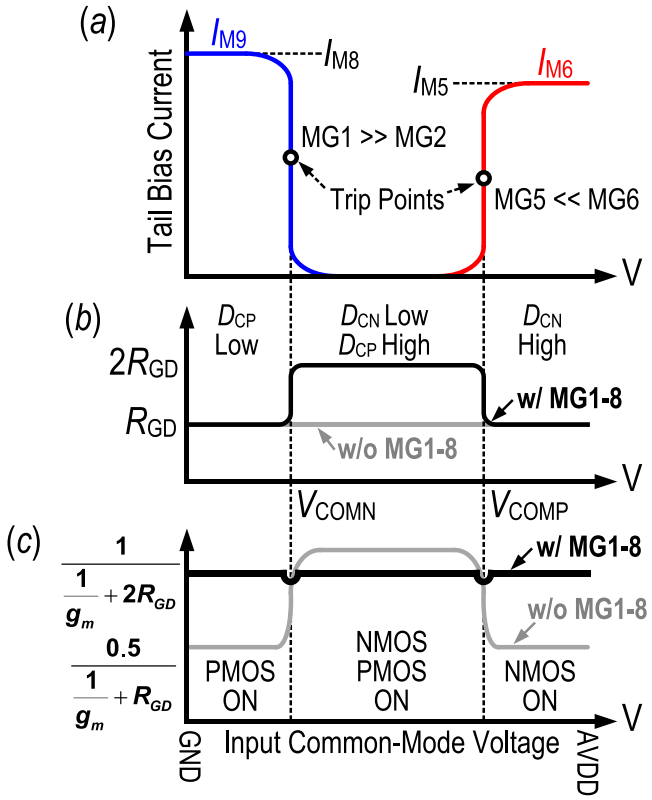


Fig. 9. Equivalent transconductance consistency by MG_1–MG_8 to cope with rail-to-rail common-mode voltages. (a) Auxiliary tail bias current for NMOS and PMOS differential input pairs. (b) Effective resistance value of series resistor R_{GD}. (c) Equivalent transconductance of proposed amplifier with respect to input common-mode voltage level.

almost rail-to-rail operations. The amplifier is composed of an input stage (M_1–M_{10}), folded-cascode summing stage (M_{11}–M_{18}), floating bias (M_{20}–M_{23}), output stage (M_{24}–M_{25}), and Miller capacitor (C_C). In addition, $R_{GD,N1}$,

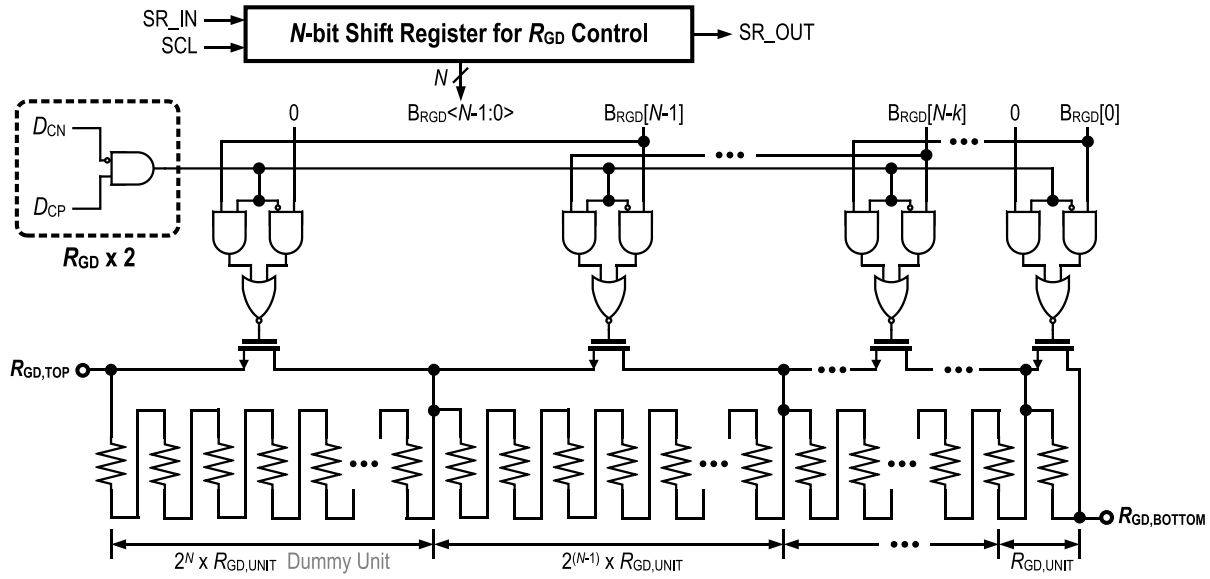


Fig. 10. Circuit implementation of g_m-degenerative series resistor (R_{GD}) controlled by N-bit digital.

$R_{GD,N2}$, $R_{GD,P1}$, and $R_{GD,P2}$ are inserted in the source of each input-pair MOS for transconductance degeneration, as described in Section II. MG_1–MG_8 are also added to enable total equivalent transconductance to be fixed without needing to consider the common-mode input voltage level.

To deal with common-mode input voltages from rail to rail, an N-channel and a P-channel differential input pair are placed in parallel. The N-channel input pair (M_1–M_2) is able to reach the positive supply rail while the P-channel input pair (M_3–M_4) is able to reach the ground rail. A drawback of the rail-to-rail input stage is that its g_m varies by a factor of 2 over the common-mode input range. This g_m variation is contrary to the intended routing-line compensation, as shown in Fig. 4. In order to obtain constant transconductance over the common-mode input range, the constant transconductance control design is also suggested in this paper, as described in Fig. 9. Fig. 9(a) shows the auxiliary tail bias current level for the NMOS and PMOS differential input pairs with respect to the input common-mode voltage. Fig. 9(b) illustrates the effective resistance value of the g_m-degenerative series resistor R_{GD} corresponding to the input common-mode voltage. Fig. 9(c) describes the equivalent transconductance of the proposed amplifier in Fig. 8 with respect to the input common-mode voltage. The g_m at the lower and upper parts of the common-mode input range must be boosted by a factor of 2. Since the input-pair MOS transistors are designed to work in weak inversion region in this design, the tail bias current could be increased by a factor of 2. This approach is realized by means of the common-mode voltage detector (MG_1–MG_8), current switches (M_7 and M_{10}), and auxiliary tail currents (I_{M6} and I_{M9}). If low common-mode input voltages are applied, only the P-channel input pair (M_3–M_4) operates. The MG_1–MG_2 detects this situation, and the D_{CP} signal then switches on the auxiliary tail current $I_{M9}(= I_{M8})$; the bias current of the PMOS input pair is consequently multiplied by a factor of 2. It is worth noting that

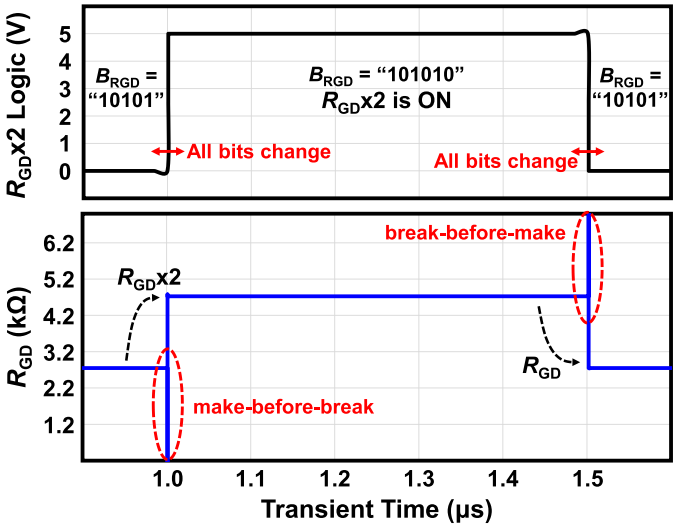


Fig. 11. Simulation of R_{GD} resistance control by $R_{GD} \times 2$ logic.

the low common-mode voltage detecting point (V_{COMN}) of MG_1–MG_2 can be designed by a ratio between $k_n(W/L)_{MG1}$ and $k_p(W/L)_{MG2}$, which is actually the tripping-point determination of the CMOS amplifier (MG_1–MG_2). If high common-mode input voltages are applied, only the N-channel input pair (M_1–M_2) operates. MG_5–MG_6 senses the high common-mode voltage, and the bias current of the NMOS input pair is then multiplied by D_{CN} activation. As previously discussed, the threshold point (V_{COMP}) of high common-mode voltage can be determined by a pre-designed tripping point of the CMOS amplifier MG_5–MG_6.

Fig. 10 shows the circuit implementation of the g_m– degenerative series resistor (R_{GD}). For variable resistance control, the binary-weighted resistors are segmented, and the switches are placed in parallel with each resistor segment. The total resistance of R_{GD} is controlled by N-bit digital data, $B_{RGD}\langle N-1:0\rangle$, connected to the gate of the MOS

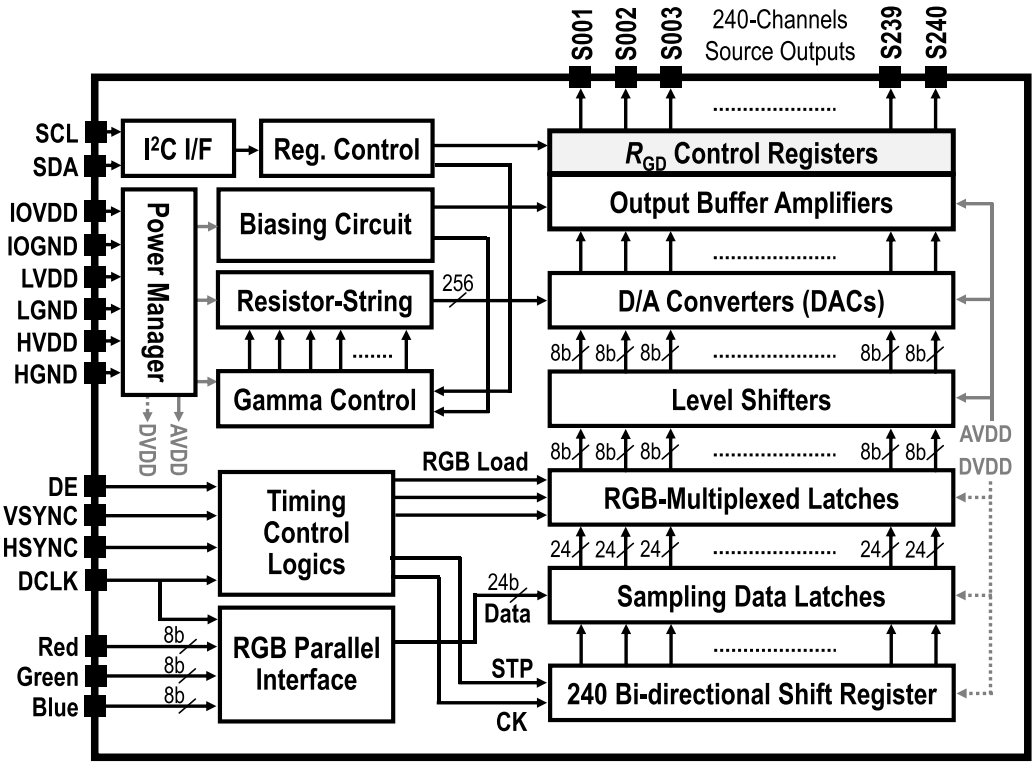


Fig. 12. Top architecture of the designed AMOLED source-driver IC.

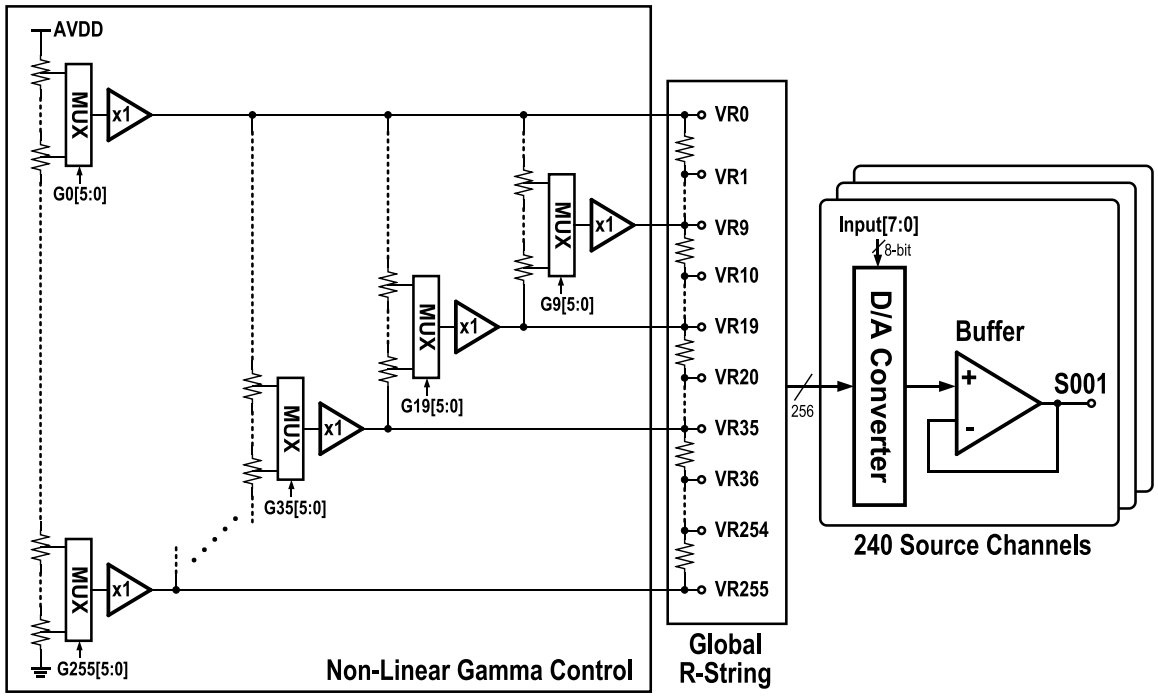


Fig. 13. 8-bit gray-level voltage generator with non-linear gamma-correction circuit.

switch, and the digital data is serially transferred from register to register, connected in series.

A number of additional circuits are shown in Fig. 10: a dummy resistor segment ($2^N \times R_{GD,UNIT}$) and a $R_{GD} \times 2$ logic block having D_{CN} and D_{CP} inputs. Due to the unique design of the g_m-degenerative R_{GD} shown in Fig. 8, the effective R_{GD} should be adjusted corresponding to the common-mode input voltage in order to realize truly constant transconductance, as described in Fig. 9. According to Fig. 9, the R_{GD} must be multiplied by a factor of 2 when the

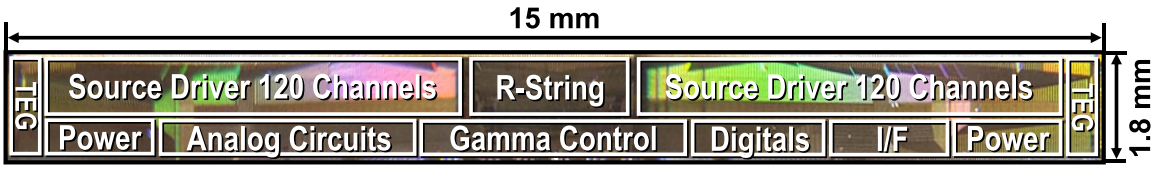


Fig. 14. Micrograph of fabricated prototype CMOS source-driver IC.

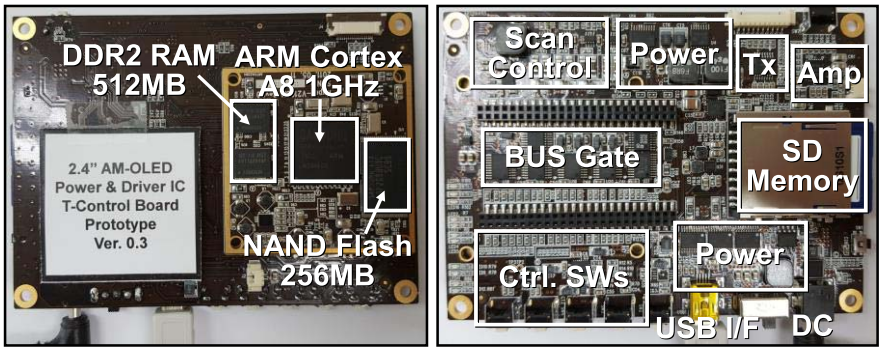
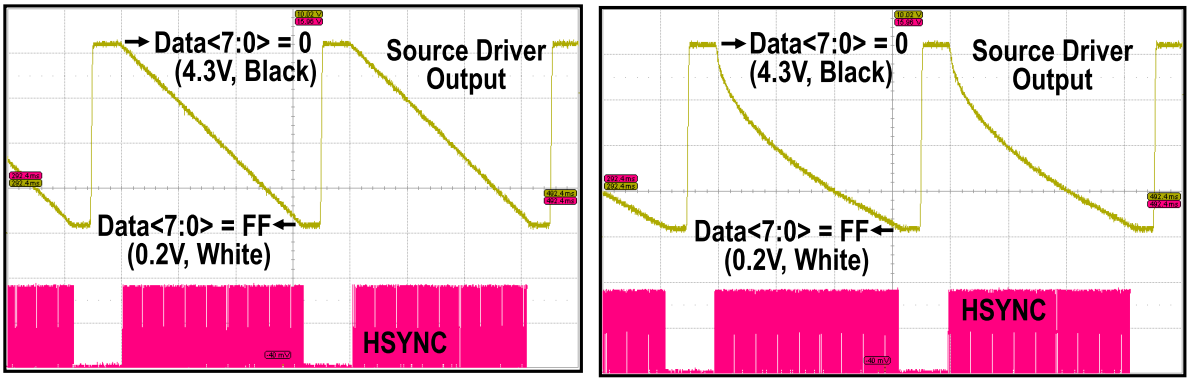


Fig. 15. Test board for driving prototype driver IC and OLED panel.



(a) (b)

Fig. 16. Measured gray-level curves from black to full brightness. (a) Without gamma correction. (b) With non-linear gamma correction.

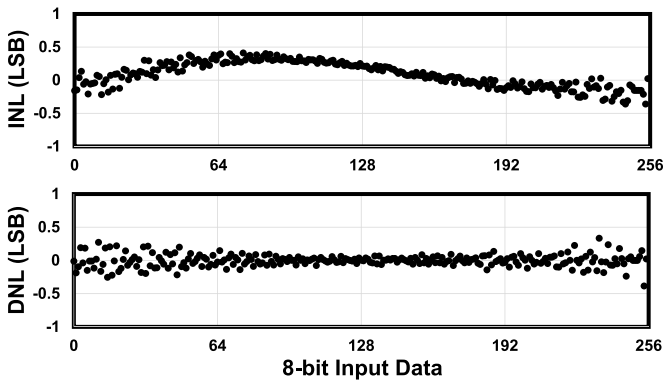


Fig. 17. Measured INL and DNL values of a linear 8-bit gray scale.

common-mode input voltage (V_{COM}) is within the middle range of $V_{\mathrm{COMN}} \leq V_{\mathrm{COM}} \leq V_{\mathrm{COMP}}$. This R_{GD} adjustment is realized by the $R_{\mathrm{GD}} \times 2$ logic block, which performs left shifting of the digital bits B_{RGD} by 1-bit when $D_{\mathrm{CP}} =$ high and $D_{\mathrm{CN}} =$ low. For an understating of Fig. 10, Fig. 11 shows the simulated operation of the $R_{\mathrm{GD}} \times 2$ logic. To consider the worst case (all bits change), the $B_{\mathrm{RGD}}\langle 4:0\rangle$ is set to be "10101," representing the R_{GD} value. If the input common-mode voltage (V_{COM}) is within the middle range of $V_{\mathrm{COMN}} \leq V_{\mathrm{COM}} \leq V_{\mathrm{COMP}}$, the $R_{\mathrm{GD}} \times 2$ logic output is activated by $D_{\mathrm{CP}} =$ high and $D_{\mathrm{CN}} =$ low. After then, the digital data connected to the switches is changed from "010101" to "101010" by the arithmetic 1-bit shift left. The bits correspond to the doubled R_{GD} value. Subsequently, the resistance value between $R_{\mathrm{GD,TOP}}$ and $R_{\mathrm{GD,BOTTOM}}$ becomes to be multiplied by two, as shown in the bottom graph of Fig. 11. By utilizing the $R_{\mathrm{GD}} \times 2$ logic block, the effective R_{GD} can be boosted by a factor of 2 in conjunction with a dummy resistor segment ($2^N \times R_{\mathrm{GD,UNIT}}$), and the truly constant transconductance is thus realized, regardless of the input common-mode voltage level.

The transition behavior of the effective resistance of R_{GD} depending on the $B_{\mathrm{RGD}}\langle N\text{–}1{:}0\rangle$ data is crucial, and should be also considered. To observe the R_{GD} variation at the transition point by the $R_{\mathrm{GD}} \times 2$ logic, the simulation is performed for the worst case (all bit change), as shown in Fig. 11. As can be seen, the switching to $R_{\mathrm{GD}} \times 2$ makes the new connection before it breaks the previous state (make-before-break),

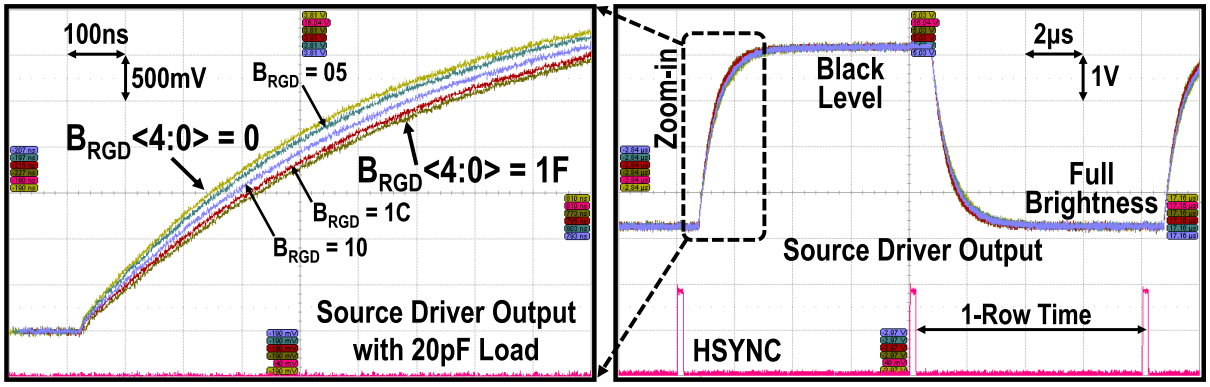


Fig. 18. Measured output waveforms with 20-pF load by sweeping the 5-bit R_{GD} control data, $B_{RGD}\langle 4{:}0\rangle$.

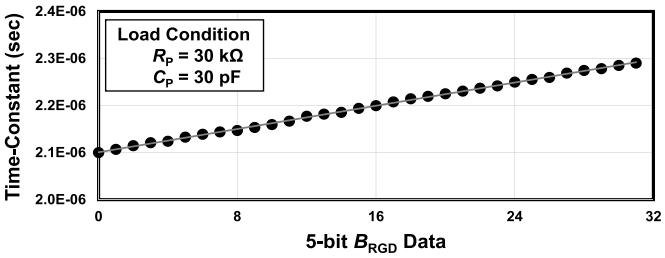


Fig. 19. Measured 1-τ settling time with g_m-degeneration control of 5-bit B_{RGD} data.

while the switching to the original value from $R_{GD} \times 2$ is the break-before-make. The glitches while the R_{GD}-changing appear only during the transition period (approximately sub-nanosecond) of the $R_{GD} \times 2$ logic output. Fortunately, they can be scarcely significant to be considered, because the feedback-loop bandwidth of the output buffer amplifier could be much more limited compared to the R_{GD} transition speed.

B. 240-Channel OLED Source-Driver IC Architecture

Fig. 12 shows the overall architecture of the designed AMOLED 240-channel source-driver IC expressing a 16.7M color depth (8-bit for each RGB signal) adopting the proposed compensation of non-uniform routing-line resistances. The sampling data latches receive one horizontal display data from the 24-bit RGB parallel interfacing block by the bidirectional shift register. Since a single source output of the driver IC is responsible for the RGB multi-channel (1:3 de-multiplexing function) in this design, each 24-bit pixel data is then multiplexed by RGB, and the multiplexed 8-bit data is stored on RGB-separate holding latches. The pixel data is transferred into a DAC via level shifters, and the DAC then selects a gray voltage from the 256 gray voltages supplied from a global resistor string, based on the pixel data. Finally, the analog gray voltage is driven to the pixel in the panel through the output buffer amplifiers. The overall operation of driver IC is under the control of the timing signals, DE, VSYNC, HSYNC, and DCLK, which are provided from an external host system.

For compensation of non-uniform routing-line resistances, the g_m-degenerative series resistance (R_{GD}) embedded in the output buffer amplifier is digitally controlled by the R_{GD} control register, and the R_{GD} control data bit flows into the control register through inter-integrated circuit serial interface protocol.

Gamma correction is the essential requirement to guarantee high-quality display. The driven voltage into pixel will be converted to the pixel current by a drive TFT in the pixel circuit, and the OLED luminance is determined by the converted pixel current. During V-to-I conversion, the TFT current could be a non-linear response to the driven voltage. Therefore, the gray-level voltages must be adjusted to compensate for this non-linearity before being displayed; this process is called gamma correction. Gamma correction is also required because of the human non-linear perception of color. Fig. 13 depicts a block diagram of 256 gray voltages generator with non-linear gamma-correction circuit. The gamma control block in the source-driver IC plays the role of gamma correction by providing voltage taps into a global resistor string, similar to a segmented piecewise linear scheme. Therefore, the non-linear curve is shaped through the control of 5-bit control registers, such as G9[5:0]–G225[5:0]. As shown in Fig. 13, the driving voltage range is determined by G0[5:0] and G225[5:0] under a supply voltage of AVDD (5 V).

IV. Chip Fabrication and Test Results

A prototype AMOLED source-driver IC with 240 output channels was fabricated in 0.18-/0.5-μm CMOS technology to validate the functionality and performance of the proposed driver architecture with non-uniform routing-line compensators. Fig. 14 shows the CMOS chip micrograph that is 15 mm (width) $\times$ 1.8 mm (height) in size. The analog and digital circuits have been designed to operate with 5 and 1.8-V power supplies, respectively. The gray voltage generator uses a supply voltage of 5 V and generates a source output range of from 4.3 V (black) to 0.2 V (full brightness), which is suitable for the voltage range of the target OLED panel ($ELV_{DD} = 4.6$ V and $ELV_{SS} = -4.4$ V) used in this paper. Fig. 15 shows the configuration of the test board for the prototype driver IC and the OLED panel. The test board provides the required power supplies, timing-control signals, and display data to the CMOS driver chip, and also gives the row-line control signals and power supplies

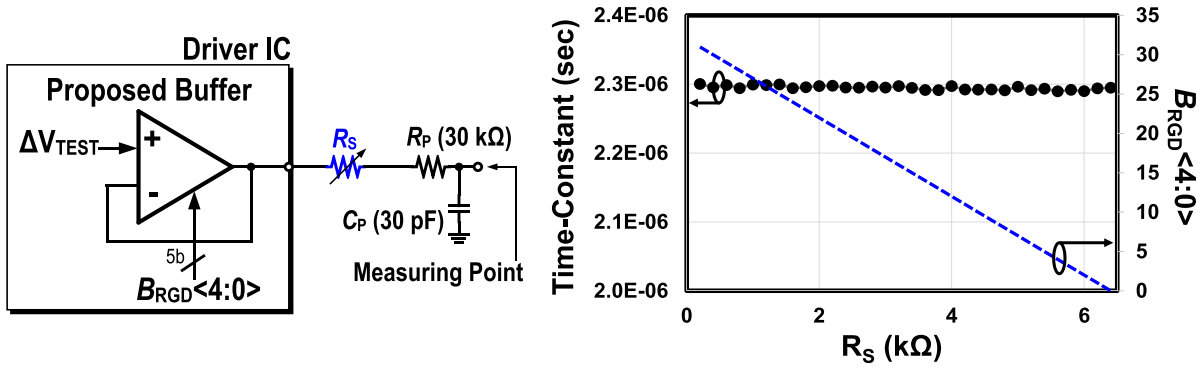
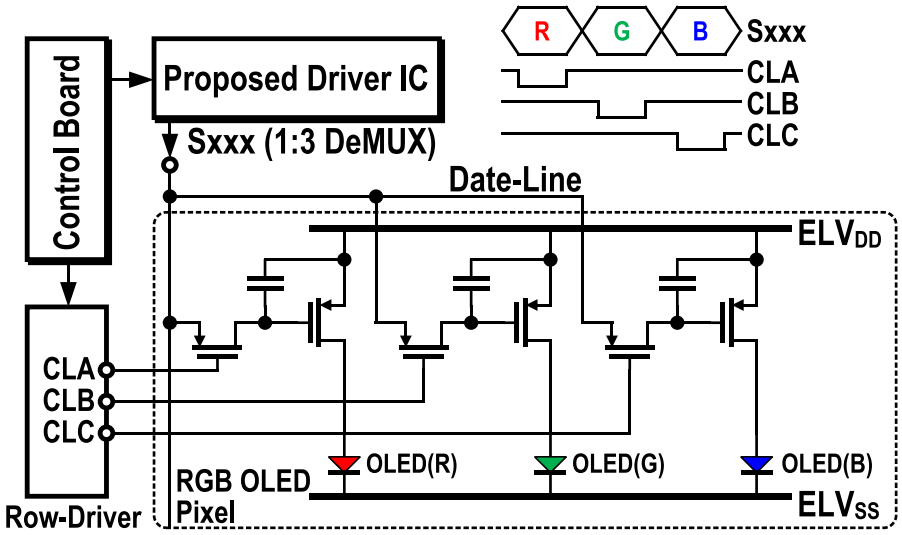
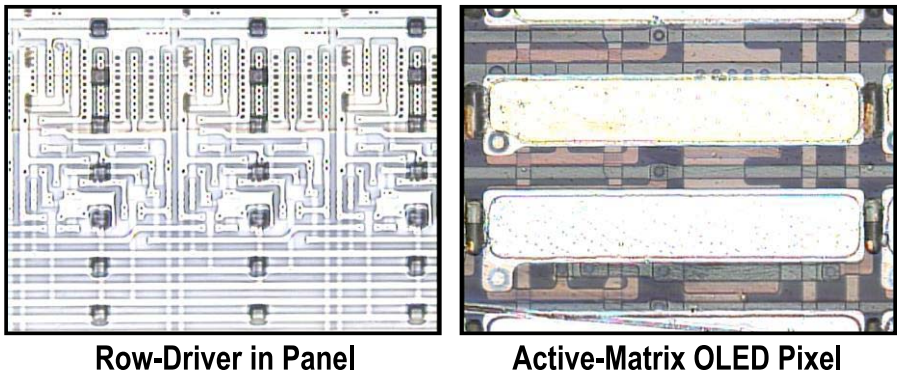


Fig. 20. Measured 1-τ settling time uniformized by g_m-degenerative compensation despite R_S variations.



(a)



(b)

Fig. 21. 2.4-in target OLED panel structure. (a) Active-matrix pixel circuit. (b) Micrograph of TFT-OLED pixel and row-driver integrated in panel.

to the OLED panel. To test the high frame rate up to 240 Hz, the high-performance CPU (1 GHz) was chosen to handle a high-frequency dot clock (DCLK) in our implementation.

A. Electrical Measurements

In order to verify the functionality of the source driver, several electrical tests were performed. Fig. 16 shows the measured waveforms of 256 gray levels based on the 8-bit input data. To measure the appropriate waveforms, input image data were increased by one gray step as the row-line number increases. As shown in Fig. 16(a), the 8-bit DAC properly generates the accurate linear 256 gray-level voltages from black (4.3 V) to full brightness (0.2 V) without gamma correction. In conjunction with non-linear gamma-correction control, it is clearly observed in Fig. 16(b) that the measured 256 gray-voltage curve shows the non-linear shape, which reflects the non-linear voltage-to-current conversion

TABLE II
SPECIFICATION OF TARGET DISPLAY PANEL

Display panel	Active-Matrix Organic Light-Emitting Diodes (AMOLED) with Low-Temperature Poly-Si Thin-Film Transistors (LTPS-TFTs)
Max. luminance	220 cd/m^2
Spatial resolution	QVGA: 240(W) × RGB × 320(H)
Panel size	2.4-inch
Power supply	ELV_{DD} = 4.6V / ELV_{SS} = -4.4V
Data-line parasitic load	(Typ.) R_p = 30 kΩ, C_p = 30 pF
Driver-to-channel routing-line resistance ($R_{Routing}$)	Shortest path: min. 3.1 kΩ Longest path: max. 8.5 kΩ (estimated values)

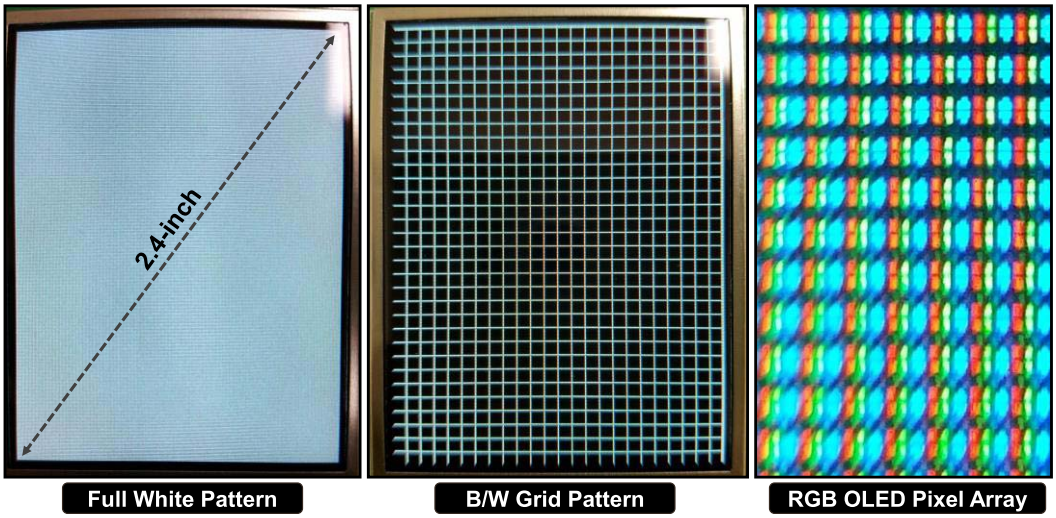


Fig. 22. Photographs of displayed picture and RGB pixels on OLED panel using the prototype source-driver IC.

characteristic of the TFT in pixel, for the linear control of OLED luminance with respect to input data. Fig. 17 shows the measured INL and DNL values of a linear 8-bit gray scale. The maximum INL and DNL values were measured to be 0.41 and 0.38 LSB, respectively, with 1 LSB = 16 mV.

The g_m-degenerative buffer amplifier was also measured to validate the compensation of the non-uniform routing-line resistances. Fig. 18 shows the measured output waveforms of a source output channel with a sweep of R_{GD} resistance. The R_{GD} is designed to be variable within a range of 0–6.4 kΩ, controlled by 5-bit digital data, $B_{RGD}\langle 4{:}0\rangle$. To observe the effect of R_{GD} on the signal charging rate, the black and white gray inputs are alternatively applied for full-range swing (Δ4.1 V) voltage output. Under the condition of $B_{RGD}\langle 4{:}0\rangle = 0$, the $1-\tau$ (63.2% accuracy) settling time was measured to be approximately 810 ns with a 20 pF load. With a $B_{RGD}\langle 4{:}0\rangle$ setting at "0x1F," the 1-τ settling time was measured to be approximately 945 ns. Fig. 19 shows the measured 1-τ settling time with g_m-degenerative control of 5-bit $B_{RGD}\langle 4{:}0\rangle$ data under load condition of $R_P = 30$ kΩ and $C_P = 30$ pF. As can be seen, the settling time can be linearly changeable through g_m-degenerative buffer amplifier. Fig. 20 shows the measured 1-τ settling time with a sweep of the series resistor (R_S). In spite of R_S variations, the settling time (charging rate) was stably uniformized by R_{GD} digital control of the proposed buffer. These measurement results demonstrate that the proposed buffer amplifier with g_m-degeneration control has sufficient ability to adjust the signal charging rate which is especially prone to vary with unfixed routing-line resistance.

B. OLED Display Demonstration

Table II summarizes the technical parameters of a target OLED display panel used in this implemented system. The active-matrix backplane of the AMOLED panel was fabricated based on low-temperature polycrystalline-silicon TFTs. The OLED panel size and the spatial resolution are 2.4-in and QVGA (240 × RGB columns and 320 rows), respectively, which are suitable for low-cost mobile electronic

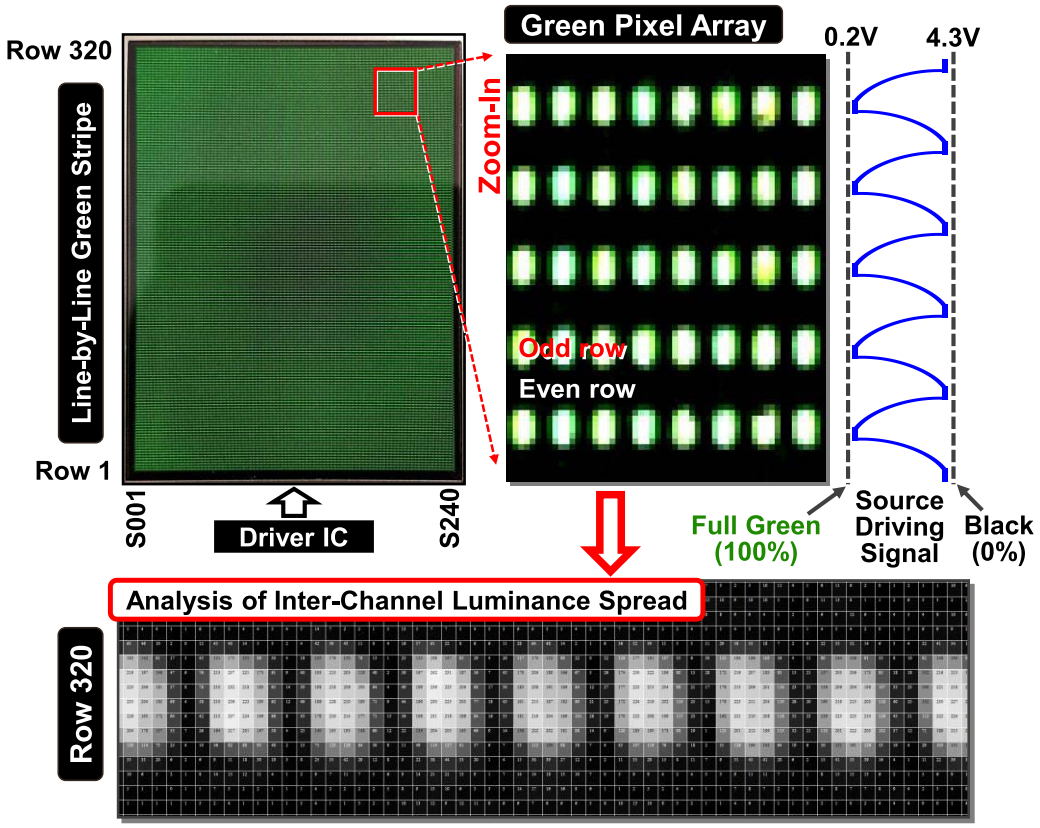


Fig. 23. Inter-channel luminance uniformity measurement depending on charging rate by driving row-by-row green stripe.

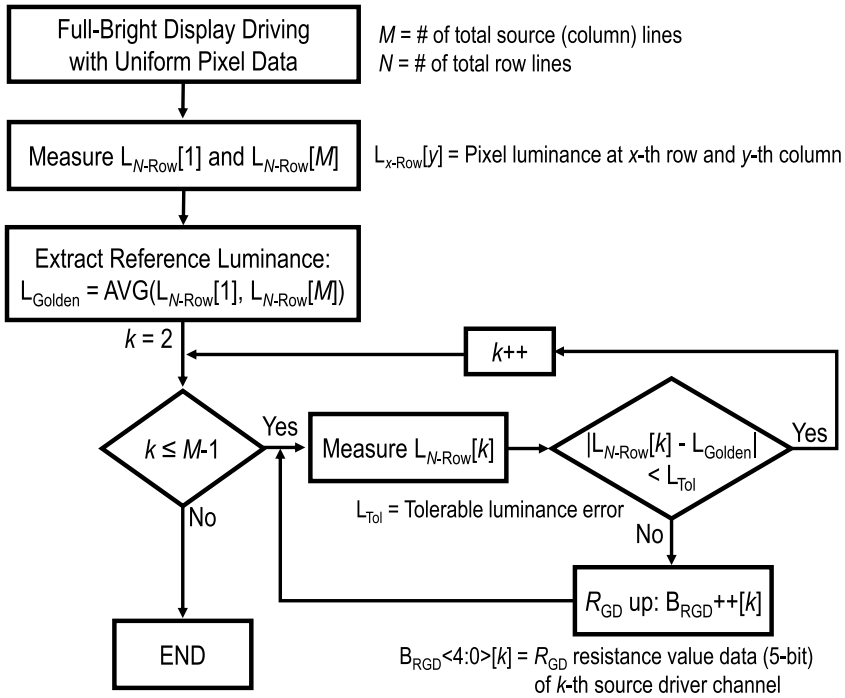


Fig. 24. Calibration process of non-uniform charging rate by R_{GD} control.

devices. Through analysis of patterned routing-line designs in bezel, the effective resistances of the shortest path routing line and the longest path routing line are estimated to be 3.1 and 8.5 kΩ, respectively. Therefore, it can be concluded that the proposed source-driver IC should compensate for $\Delta R_{\mathrm{Routing}} = 5.4$ kΩ by g_m-degeneration control to achieve

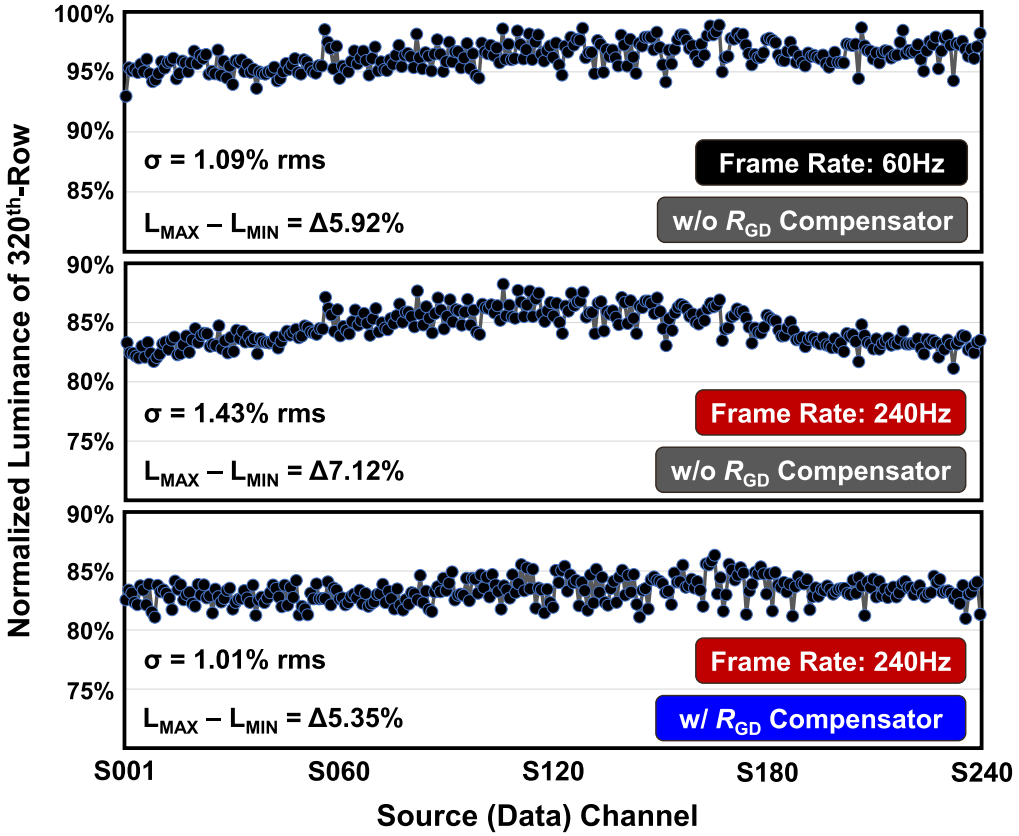


Fig. 25. Measured luminance across source channels at 320th row with frame rate of 60 Hz (top), with frame rate of 240 Hz (middle), with frame rate of 240 Hz and g_m-degenerative R_{GD} compensation (bottom).

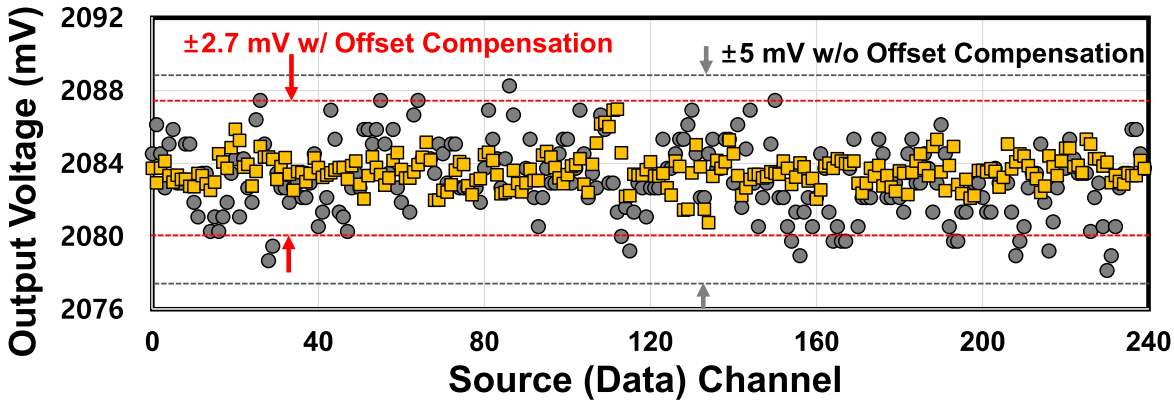


Fig. 26. Measured output voltages across source-driver channels.

a highly uniform charging rate across column channels. Fig. 21(a) describes the AMOLED pixel structure of the target OLED panel and the display driving scheme in our implementation. The unit pixel is composed of red, green, and blue sub-pixels, and they share a single data-line; thus, the proposed driver IC should support 1:3 de-multiplexing function. The TFT row-drivers integrated in panel are responsible for scanning row lines by VGH = 5 V and VGL = −7 V. Fig. 21(b) shows the micrographs of TFT-OLED pixel and row driver in target panel. By utilizing the fabricated prototype CMOS driver IC and the test board (timing control and power supply), the real display is successfully demonstrated on the 2.4-in OLED panel. Fig. 22 shows the displayed pictures (full-white pattern and line-grid pattern) and the micrograph of RGB pixel array on the OLED panel using the fabricated source-driver IC.

C. Luminance Non-Uniformity Compensation

To measure the inter-channel non-uniformity caused from the charging rate mismatch, the row-by-row green stripe image data was displayed, and the pixel-by-pixel luminance at the 320th (last) row was then measured, as shown in Fig. 23. The row-by-row stripe is driven in order to create the most

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

	This work	IEEE JSSC [11]	IEEE JSSC [19]	IEEE JSSC [27]	IEEE TCAS Video [16]
Application	AM-OLED	TFT-LCD	TFT-LCD	AM-OLED	TFT-LCD
Process technology	0.18μm 1.8/5V CMOS	0.1μm 1.5/5V CMOS	0.35μm 3.3/5V CMOS	0.18μm CMOS	0.35μm 5V CMOS
Color depth	16.8 million colors	1 billon colors	16.8 million colors	16.8 million colors	1 billon colors
# of source channels	240 channels	-	32 channels	102 channels	-
Power consumption	13 mW (chip total) while driving display	9.4 mW	-		-
Static current per buffer	1.4 μA/buffer	-	1.2 μA/buffer	63.6 μW/channel	-
Buffer area per channel	1,950 μm^2 (buffer) + 2,570 μm^2 (g_m-degenerative circuit)	1,778 μm^2	15,410 μm^2 (MUX + 2 buffers + 2 inversion-SWs)	-	-
Source output range	0.2 – 4.3 V	0 – 5 V	0.26 – 4.74 V	1.5 – 5 V	approx. 0 – 5 V
INL / DNL	0.41 LSB / 0.38 LSB	1.71 LSB / 0.37 LSB	0.79 LSB / 0.79 LSB	0.75 LSB / 0.56 LSB	2.13 LSB / 1.3 LSB
Available frame rate	240-Hz with 1:3 demultiplexing	-	-	60-Hz	-
Inter-channel deviation	±2.7 mV with offset calibration	6.35 mV	-	-	-
Inter-chip deviation	±12.3 mV	6.19 mV	17.1 – 18.5 mV	-	4.9 mV
External interface	24-bit RGB parallel	-	-	-	-
Compensation of charging rate mismatch	Available (5-bit control)	None	None	None	None
Verification level	Chip measurement + Display demonstration	Chip measurement only	Chip measurement only	Chip measurement only	Chip measurement only

Fig. 27. Demonstration of playing video with a frame rate of 240 Hz.

severe signal charging condition to be affected by routing-line resistance. After luminance measurements by using a high-performance vision camera, the calibration process of the g_m-degenerative resistance (R_{GD}) in each channel is performed for uniformizing luminance across the column channels. Fig. 24 illustrates the luminance measurement and the calibration process. In this process, the R_{GD} value of each source output is adjusted so that the measured pixel luminance reaches equal to the reference luminance (L_{Golden}), which is extracted from the edge pixels supplied via the longest routing line. The calibration process in Fig. 24 assumes that the luminance non-uniformity is only due to the $\Delta R_{Routing}$. However, it should be noted that the pixel luminance is also prone to be varied depending on the supply voltage and temperature (VT) variations. The VT variations have a significant influence on the luminance of each OLED pixel, but have little effect on the display uniformity because it affects the whole pixels evenly. However, in order to make the calibration environments (supply VT) as close as possible to real display situations, the calibration process is being conducted while driving the full-brightness display on the panel. In addition, having a sufficient thermal settling time before the luminance extraction step slightly helps matching the absolute temperature with the normal display condition. On the other hand, the process (Mura) variations [31], [32] such as a threshold voltage (V_T) shift of TFT can significantly interfere with the R_{GD} calibration process. To mitigate the Mura effect, the spatial-averaging technique is utilized in the proposed calibration steps. For higher accuracy of the R_{GD} adjustment, the Mura effects must be self-compensated in each pixel by utilizing V_T-cancellation pixel circuits.

Fig. 25 shows the measured luminance across the source channels at the 320th (last) row with frame rate variation. The upper graph of Fig. 25 is measured under the condition of a 60-Hz frame rate; the overall distortion of luminance (charging rate) uniformity cannot be observed due to sufficient T_{Row} time. Note that local (minor) non-uniformities are believed to occur due to the dispersion of source output offsets and the electrical Mura variations of TFTs and OLEDs [31], [32]. On the other hand, the overall distortion of luminance uniformity can be clearly observed when the frame

rate is increased to 240 Hz, as shown in the middle graph of Fig. 25. Due to insufficient T_{Row} time, the luminance is entirely degraded, and the luminance deviation was measured to be $\sigma = 1.43\%$. It can be observed that the charging rate is lower for pixels located at the edge of the OLED panel, since the driving signal is supplied via the longer routing-line path. The higher frame rate results in further exacerbation of the effect of different routing-line resistances (R_{Routing}) on the charging rate mismatch, due to the shortened T_{Row}. The lower graph of Fig. 25 shows the measured result after the R_{GD} calibration process of Fig. 24. As can be seen, the luminance uniformity is significantly improved; the measured luminance deviation was reduced to $\sigma = 1.01\%$, despite the high frame rate of 240 Hz, and this result is comparable to that at 60-Hz refreshing rate.

As discussed in Section II, the proposed buffer amplifier with g_m-degeneration has also ability to calibrate the output offset variation. Fig. 26 shows the measured output voltages across the source output channels of the prototype driver IC. By virtue of the offset compensation mechanism of the proposed circuit design, the measured output deviation was drastically reduced from ± 5 to ± 2.7 mV.

D. Video Display Test With 240-Hz Frame Rate

Fig. 27 shows the demonstration photograph of the playing video displayed on the OLED panel with a frame rate of 240 Hz. This result demonstrates that the proposed source-driver IC and calibration technique successfully offer a highly uniform OLED display despite the higher frame rate condition.

E. Performance Summary and Comparison

Table III summarizes the main features of the proposed driver IC compared to that proposed in prior works. The approach proposed in this paper is the only approach that actively compensates for the non-uniformities induced from the charge rate mismatch without the zigzag panel design of the driver-to-channel routing line, which broadens the bezel area thickness. In the target panel of 2.4-in QVGA OLED display, the width and pitch of the data-lines are designed to be 10 and 153 μm, respectively. Considering the design constraints, the minimum bezel height of 11 mm with zigzag wiring has to be actually required to compensate for $\Delta R_{\mathrm{Routing}}$. This bezel height corresponds to about 22% of the total height (49 mm) of the active display area. However, the bezel height of the display panel can be significantly reduced to 1 mm or less with the proposed driver IC. This paper is also successfully demonstrated by utilizing a 2.4-in AMOLED display panel with a frame rate of 240 Hz.

V. Conclusion

The 240-channel OLED source-driver IC with compensation of non-uniform routing-line resistances has been designed and verified through chip fabrication, measurements, and display demonstration. Thanks to the active compensation scheme, the luminance uniformity and the frame rate (for motion blur) can be significantly enhanced for OLED displays. Therefore, the proposed approach is highly applicable for mobile or large-area OLED/LCD display applications with ultra-thin bezel panels.

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