A Sub-1-V 15-ppm/°C CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device

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***Abstract*—A sub-1-V CMOS bandgap voltage reference requiring no low threshold voltage device is introduced in this paper. In a CMOS technology with $V_{\rm thn} \approx |V_{\rm thp}| \approx 0.9$ V at 0 °C, the minimum supply voltage of the proposed voltage reference is 0.98 V, and the maximum supply current is 18 μA. A temperature coefficient of 15 ppm/°C from 0 °C to 100 °C is recorded after trimming. The active area of the circuit is about 0.24 mm^2.**

***Index Terms*—CMOS bandgap voltage reference, low voltage, temperature.**

I. Introduction

LOW VOLTAGE and low power are two important design criteria in both the analog and digital systems. It is expected that the whole system will be able to operate down to a single 1-V supply in the near future. A voltage reference, as one of the core functional blocks in both analog and digital systems, should be able to operate from a single 1-V supply for both systems.

In CMOS technology, a parasitic vertical bipolar junction transistor (BJT) formed in a p- or n-well is commonly used to implement a bandgap reference [1]–[3]. The minimum supply voltage needs to be greater than 1 V due to two factors: 1) the reference voltage is around 1.25 V which exceeds 1-V supply [4], [5] and 2) low-voltage design of the proportional-to-absolute-temperature (PTAT) current generation loop is limited by the common-collector structure of the parasitic vertical BJT [2] and the input common-mode voltage of the amplifier [4], [6]. The first problem can be solved by resistive subdivision methods [7], [8] to scale down the 1.25-V reference voltage. The second problem can be solved by using BiCMOS process [6] or by using low threshold voltage devices [7], [8]. As shown in Fig. 1(a), the minimum input common-mode voltage of an amplifier with an nMOS input stage must be less than one $V_{\rm EB(on)}$ (i.e., $V_{\rm thn} + 2V_{\rm DS(sat)} < V_{\rm EB(on)}$), which implies that $V_{\rm thn} < 0.6$ V is required (assuming $V_{\rm EB(on)} = 0.7$ V and $V_{\rm DS(sat)} = 50$ mV). This is acceptable as nMOS transistors with $V_{\rm thn} < 0.6$ V can be easily found in many technologies. However, the temperature effect on the base–emitter voltage and threshold voltage should be considered. The temperature coefficient (TC) of the base–emitter voltage is approximately -2 mV/K [9] while that of the threshold voltage of the nMOS transistor may be greater than -2 mV/K, for example, -1.4 mV/K in AMS[1] 0.6-μm n-well CMOS technology [10]. At high temperatures, $V_{\rm EB(on)}$ may be less than $V_{\rm thn} + 2V_{\rm DS(sat)}$, and the reference circuit will not function properly. Thus, either native nMOS transistors [7] or nMOS transistors with $V_{\rm thn} < 0.5$ V [8] are required to allow the reference circuit in Fig. 1(a) to operate down to a single 1-V supply. When the reference uses an amplifier with a pMOS input stage, as shown in Fig. 1(b), the minimum supply voltage is $V_{\rm EB(on)} + |V_{\rm thp}| + 2|V_{\rm DS(sat)}|$, and so $|V_{\rm thp}|$ less than 0.2 V is required to implement a 1-V reference.

To address the above-mentioned design problems, a sub-1-V bandgap reference circuit in a standard CMOS process is presented in this paper. The key feature of the proposed reference circuit is that no low threshold voltage device is needed. The design techniques for achieving a good performance are also presented in detail.

II. Proposed Sub-1-V Bandgap Voltage Reference in CMOS Technology

The structure and the complete schematic of the proposed sub-1-V bandgap voltage reference are shown in Figs. 2 and 3, respectively. The reference core circuitry is modified from the one proposed by Banba *et al.* [7]. The main differences are that an amplifier with a pMOS input stage is used and the inputs of the amplifier are connected to nodes N_1 and N_2 instead of nodes N_3 and N_4. A self-bias approach is used in this circuit to bias the amplifier. The compensation capacitor C_B [11] is used to stabilize the reference. A larger C_B provides better stability, but the startup time will be longer.

As illustrated in Fig. 2, the amplifier enforces nodes N_1 and N_2 to have equal potential. As a result, nodes N_3 and N_4 also have the same potential when $R_{2A1} = R_{2B1}$ and $R_{2A2} = R_{2B2}$. Therefore, the loop formed by $Q1, Q2, R_1, R_{2A1}, R_{2B1}, R_{2A2}$, and R_{2B2} generates a current I given by

$$I = \frac{V_{\rm EB2}}{R_2} + \frac{V_{\rm T} \cdot \ln N}{R_1} \tag{1}$$

where N is the emitter area ratio, $V_{\rm T}$ is the thermal voltage, and $R_2 = R_{2A1} + R_{2A2} = R_{2B1} + R_{2B2}$. The current I is injected to R_3 by the current mirror formed by M1, M2, and M3, and this gives the reference voltage as follows:

$$V_{\rm ref} = \frac{R_3}{R_2} \cdot \left[V_{\rm EB2} + \left(\frac{R_2}{R_1} \ln N \right) \cdot V_{\rm T} \right]. \tag{2}$$

A scaled-down bandgap reference voltage can be obtained by an appropriate resistor ratio of R_3 to R_2. Moreover, trimming

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[1]Austria Miko Systeme Group, Austria

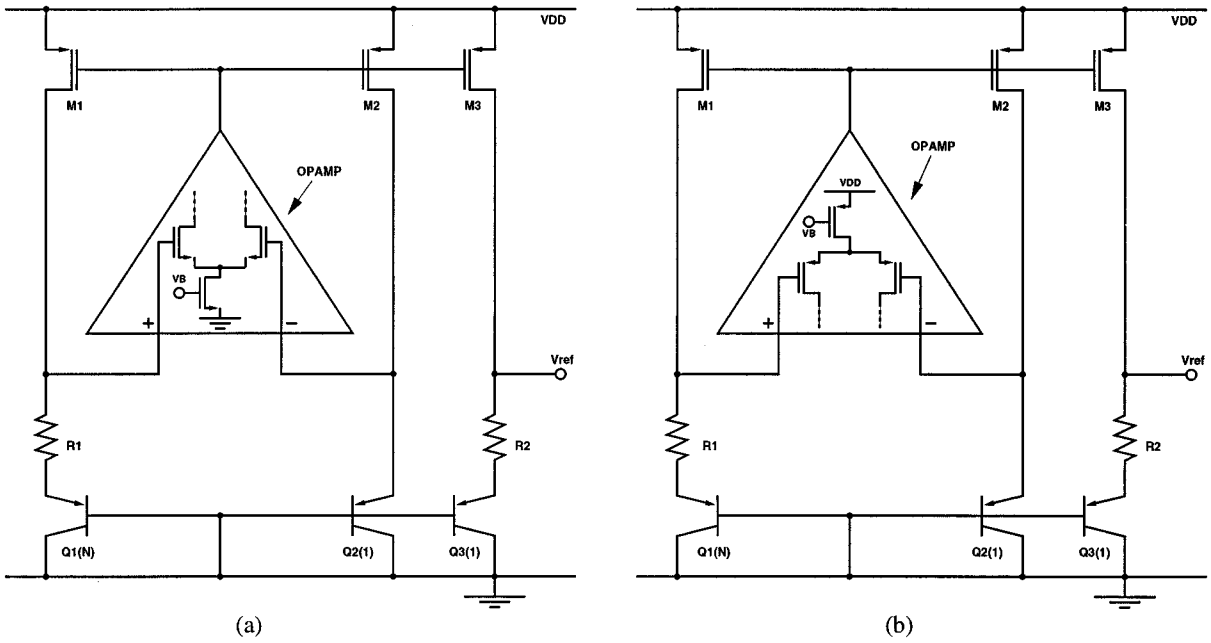

Fig. 1. Bandgap voltage references in CMOS technology using an amplifier with (a) nMOS input stage, and (b) pMOS input stage.

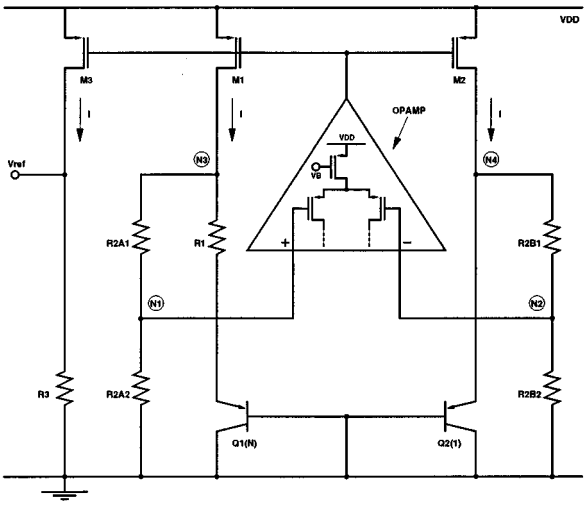

Fig. 2. Proposed sub-1-V bandgap voltage reference.

on the resistor ratio (ratio of R_2 to R_1) to achieve a good TC can be done on R_{2A1} and R_{2B1} simultaneously.

When the sum of the voltages across R_{2B1} and R_{2B2} (or R_{2A1} and R_{2A2}) is equal to $V_{\rm EB2}$, the voltage with respect to ground at N_1 and N_2 is $(R_{2B2}/(R_{2B1}+R_{2B2}))\cdot V_{\rm EB2}$. Therefore, the minimum supply voltage $V_{\rm s}$, which should be evaluated at the lowest operating temperature, is given by

$$V_{\rm s(min)} = \left(\frac{R_{2B2}}{R_{2B1}+R_{2B2}}\right)\cdot V_{\rm EB2} + |V_{\rm thp}| + 2|V_{\rm DS(sat)}|. \quad (3)$$

The minimum supply voltage is substantially reduced when $(R_{2B2}/(R_{2B1}+R_{2B2}))\cdot V_{\rm EB2}$ is set to a small value. This structure is suitable for any CMOS technology to implement low-voltage bandgap reference. Moreover, there is no increase on the total resistance compared to the one proposed by Banba *et al.*

A. Operation in High-Gain Region by Forward Biasing the Source–Bulk Junctions of pMOS Transistors

A high-gain amplifier with ultralow offset voltage is very important in the proposed bandgap reference to ensure that the nodes N_1 and N_2 in Fig. 2 have nearly the same potential. However, as the output of the amplifier is connected to the gates of pMOS transistors (M1, M2 and M3), the amplifier may not operate at the high-gain region [6]. As shown in Fig. 4, the operating point of the output of the amplifier is $V_{\rm DD} - |V_{\rm GSP}|$. If the supply voltage is low, for example, 1 V, this node voltage of the output of the amplifier may be close to the ground, and this enforces the nMOS transistor of the output stage to operate in triode region (region A in Fig. 4). As a result, the gain of the amplifier is reduced severely. A method to reduce the threshold voltage of the pMOS transistors is to forward bias the source–bulk junction [12] since the threshold voltage of a pMOS transistor is given by [9], [12]

$$|V_{\rm thp}| = |V_{\rm thpo}| + \gamma\cdot\left(\sqrt{2|\phi_f| - V_{\rm SB}} - \sqrt{2|\phi_f|}\right) \quad (4)$$

where $|V_{\rm thpo}|$ is the threshold voltage with zero biased source-bulk voltage, γ is the body bias coefficient, and $|\phi_f|$ is the bulk Fermi potential. With this technique, the gate-source voltage of a pMOS transistor is reduced from $|V_{\rm GSP}|$ to $|V_{\rm GSP}{}'|$ (region B in Fig. 4), and this allows the amplifiers to operate in the high-gain region.

In [12], the forward-biased junction is defined by the voltage drop across a Schottky diode. In order to eliminate the use of the Schottky diode and allow the reference circuit to be compatible to any CMOS process, a temperature-independent voltage across $R_{\rm SB}$, as shown in Fig. 3, is needed. This voltage is generated by drawing the current given by (1) from MSB, and the voltage across $R_{\rm SB}$ is used to forward bias the source–bulk junctions of all pMOS transistors. The temperature-dependent bulk

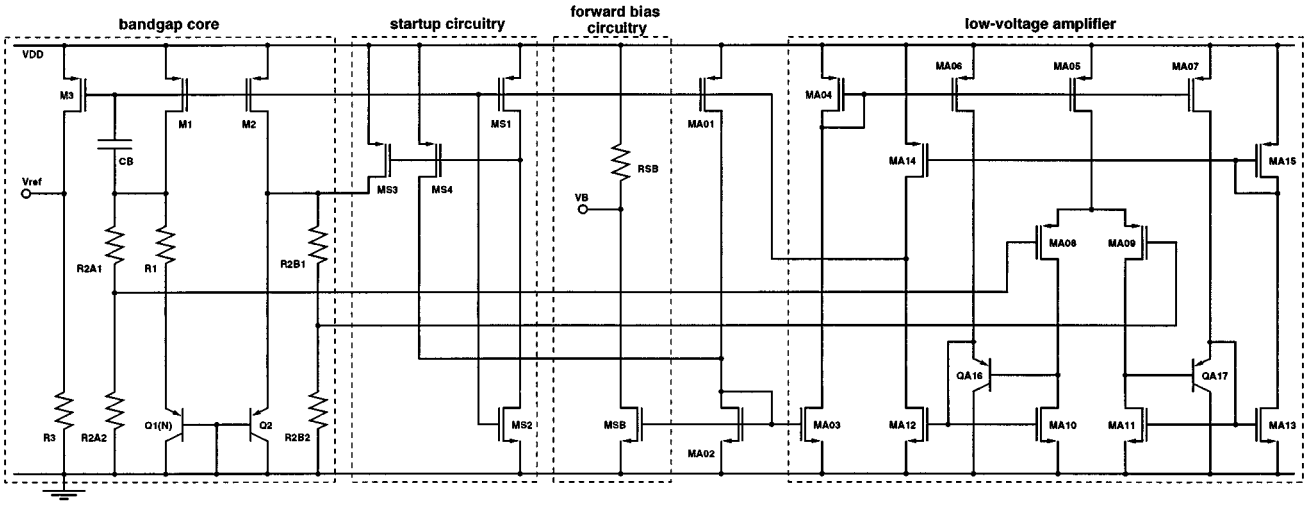

Fig. 3. Complete schematic of the proposed sub-1-V bandgap voltage reference (the source–bulk junctions of all pMOS transistors are forward biased by V_B except MA08 and MA09).

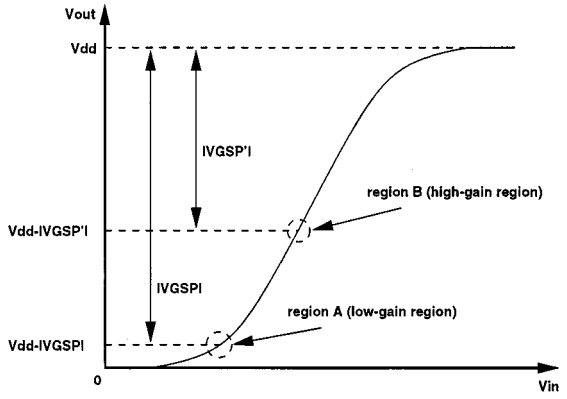

Fig. 4. Transfer characteristic of the low-voltage amplifier.

current injected to V_B is small compared with the bias current drawn from MSB. As a result, the voltage across $R_{\rm SB}$ is not exactly temperature independent but decreases slightly according to temperature. Thus, the maximum forward bias voltage is set to about 0.3 V at the lowest operating temperature to avoid turning on the p–n junction between the p-substrate and n-well.

B. Low-Voltage Amplifier With DC Level-Shifting Current Mirror

A dc level-shifting current mirror [5] must be used in order to make the low-voltage amplifier function properly, especially for some technologies with $V_{\rm thn} \geq |V_{\rm thp}|$. The circuit shown in Fig. 5(a) is part of the amplifier in Fig. 3 without dc level-shifting current mirror. The drain–source voltage of MA08 is given by $V_{\rm in+} + |V_{\rm GS8}| - V_{\rm GS10} \approx V_{\rm in+}$, assuming $|V_{\rm GS8}| \approx V_{\rm GS10}$ for $|V_{\rm thp}| \approx V_{\rm thn}$. If $V_{\rm thn} > |V_{\rm thp}|$, the drain–source voltage of MA08 is less than $V_{\rm in+}$. The drain–source voltage of MA08 may be less than the saturation voltage if $V_{\rm in+}$ is small. Since $V_{\rm in+} = (R_{2B2}/(R_{2B1} + R_{2B2})) \cdot V_{\rm EB2}$ in the proposed sub-1-V bandgap reference, MA08 may operate in triode region and this reduce the gain of the amplifier.

A dc level-shifting current mirror using the parasitic vertical BJTs, shown in Fig. 5(b), can solve this problem. The drain–source voltage of MA08 is now given by $V_{\rm in+} + |V_{\rm GS8}| + V_{\rm EB16} - V_{\rm GS10}$. This ensures that MA08 will operate in the saturation region even when $V_{\rm in+} = 0$ V, providing that $V_{\rm thn}$ is not greater than $|V_{\rm thp}|$ by more than 0.6 V.

C. Startup Circuitry

The startup circuit of the proposed reference circuit is formed by MS1–MS4. MS1 and MS2 form a function of inverter. The W/L ratio of MS2 is chosen to be much less than one, and the W and L of MS1 are the same as those of M1–M3 to eliminate the variation on the threshold voltage due to the geometry effect. When the circuit operates in zero-current state, the gate voltages of M1–M3, the same as that of MS1, are pulled high and close to $V_{\rm DD}$. The drain voltages of MS1 and MS2 are pulled low, and this turns on MS3 and MS4 to inject current to the bandgap core circuitry (by MS3) and to the amplifier (by MS4). The drain voltage of M2 increases, and the amplifier also starts to operate. Then, the amplifier forces the drain voltage of M1 to increase by pulling down the gate voltages of M1–M3 to inject current. Once the gate voltage of MS1 decreases, the drain voltages of MS1 and MS2 pull high and cut off MS3 and MS4.

The W/L ratio of MS2 is critical since the loop of the reference core is destroyed if MS3 and MS4 cannot be completely cut off after startup. To ensure a complete cutoff of MS3 and MS4, the W/L should be chosen at maximum supply voltage and operating temperature. Since accuracy is not important, it is suggested to choose 1.2 times the simulated channel length to avoid the effect of process variations.

D. Effect of Offset Voltage and Noise

Bandgap voltage reference in MOS technology suffers from the effect of MOS transistor offset due to the mismatches of transistor size and threshold voltage. This leads to drifts of the absolute value of the reference voltage and also its temperature

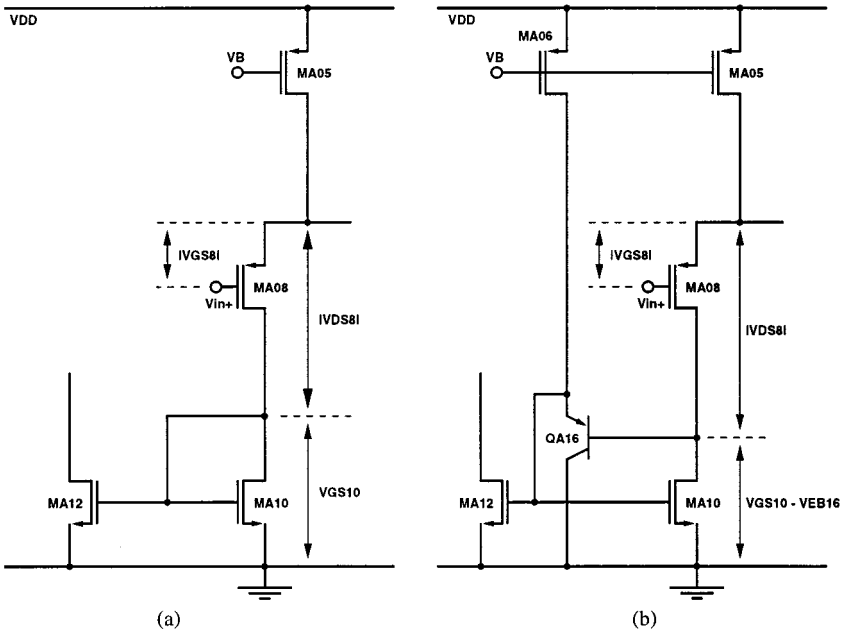

Fig. 5. Current mirror in the amplifier. (a) Without dc level shifting (b) With dc level shifting.

dependence even after trimming. In the proposed bandgap reference, the effect of the offset voltage $(V_{\rm os})$ of the amplifier can be explained by

$$V_{\rm ref} = \frac{R_3}{R_2} \cdot \left[V_{\rm EB2} + \frac{R_2}{R_1} \cdot \left(V_{\rm T} \cdot \ln N + \frac{R_2}{R_{2A2}} \cdot V_{\rm os} \right) \right]. \quad (5)$$

The effect of the $V_{\rm os}$ is amplified by the resistor ratio R_2/R_{2A2}. However, this can be reduced by increasing the emitter area ratio ($N = 64$ is used in this design), and thus the required resistor ratio of R_2 to R_1 is reduced to minimize the effect from $V_{\rm os}$ [13], [14]. Moreover, the systematic offset can be minimized by transistor size and bias current in ratio, while the random offset can be reduced by symmetrical and compact layout [3].

The noise of the proposed reference, which is similar to the offset voltage, is increased by the resistor ratio R_2/R_{2A2}. However, most of the noise is wide-band thermal noise and can be reduced by an *RC* low-pass filter.

The degradation of the noise performance and the effect of offset voltage is a tradeoff that enables the reference circuit to operate at a lower supply voltage.

III. Experimental Results

The proposed sub-1-V bandgap voltage reference shown in Fig. 3 was successfully fabricated in AMS 0.6-μm CMOS process. The micrograph of the circuit is shown in Fig. 6. Optional high resistive poly (about 1.2 kΩ/sq.) is used to reduce the chip area, and the circuit occupies 0.24 mm^2 chip area. A 4-bit trimming network is used on R_{2A1} and R_{2B1} to obtain an optimum TC.

The mean reference voltage is about 603 mV, and changes $\pm$2.2 mV at room temperature when the supply voltage changes from 0.98 to 1.5 V. The measured TCs from 0 °C to 100 °C at different supply voltages ($V_{\rm s} = 0.95, 0.98, 1.00, 1.10,$ and 1.50 V) are shown in Fig. 7. The TC at $V_{\rm s} = 0.98$ V is 15 ppm/°C and increases slightly to 25 ppm/°C at $V_{\rm s} = 1.50$ V.

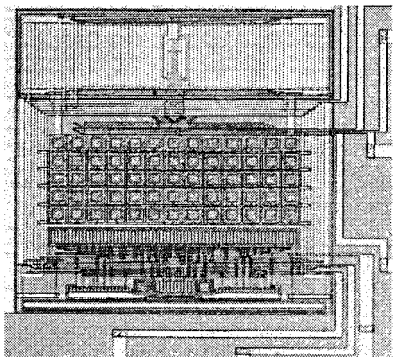

Fig. 6. Micrograph of the proposed sub-1-V bandgap voltage reference.

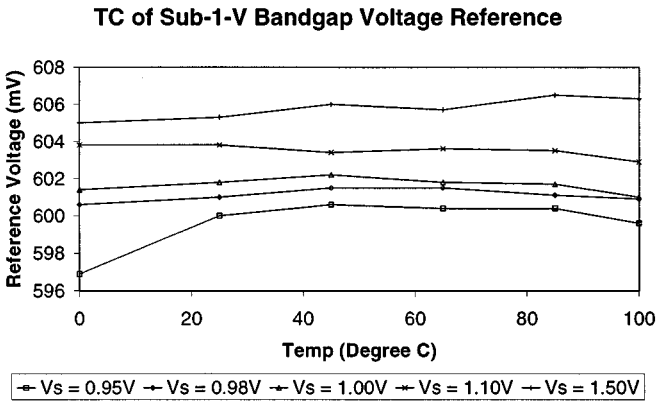

Fig. 7. Measured temperature dependence of the proposed sub-1-V bandgap reference at different supply voltages.

A maximum supply current of 18 μA is drawn when $V_{\rm s} = 1.50$ V and 100 °C. At $V_{\rm s} = 0.95$ V, the reference voltage drops rapidly at low temperatures, and the TC increases to 62 ppm/°C. This is due to larger threshold voltages at lower temperatures, thereby forcing the amplifier to operate out of the high-gain region. The reduction of the gain of amplifier causes

TABLE I
COMPARISON OF LOW-VOLTAGE BANDGAP REFERENCES

	This work	Jiang *et al.* [4]	Annema* [5]	Malcovati *et al.* [6]	Banba *et al.* [7]	Neuteboom *et al.* [8]
Technology	0.6-μm CMOS	1.2-μm CMOS	0.35-μm CMOS	0.8-μm BiCMOS	0.4-μm CMOS	0.8-μm CMOS
Threshold voltages	$V_{thp} = -0.90$ V $V_{thn} = +0.90$ V	$V_{thp} = -0.91$ V $V_{thn} = +0.53$ V	$V_{thp} = -0.65$ V $V_{thn} = +0.65$ V	-	$V_{thp} = -1.00$ V $V_{thn} = +0.70$ V $V_{thi}^{\dagger} = -0.20$ V	$V_{thp} = -0.70$ V $V_{thn} = +0.50$ V
Min. V_s	0.98 V	1.20 V	0.85 V	0.95 V	2.10 V	0.90 V
Supply current	18.0 μA	$\sim$ 500.0 μA	< 1.2 μA	< 92.0 μA	2.2 μA	-
V_{ref}	603 mV	$\sim$ 1000 mV	650 mV	536 mV	515 mV	670 mV
TC	15 ppm/°C	$\pm$100 ppm/°C (untrimmed)	57 ppm/°C	19 ppm/°C (w/o curvature compensation)	$\pm$59 ppm/°C (V_s = 2.2 V to 4 V)	-

Remarks: *DTMOST is used; †Threshold voltage of native NMOS transistor.

the rapid drop of the reference voltage at low temperatures. Therefore, the measured minimum supply voltage is 0.98 V. At the lowest supply voltage (i.e., $V_{\rm s} = 0.98$ V), the measured power-supply rejection ratio at 10 kHz is -44 dB and that at 10 MHz is -17 dB.

IV. COMPARISON WITH OTHER REPORTED LOW-VOLTAGE BANDGAP REFERENCES

A comparison with other reported low-voltage bandgap references is tabulated in Table I. From the table, technologies with low $V_{\rm thn}$ are required in [4] and [8] while native nMOS transistors are needed in [7]. DTMOST is used in [5], and BiCMOS process is used in [6]. The main reason for these approaches is to overcome the problem of the input common-mode voltage of the error amplifier in the PTAT current generation loop. However, the proposed reference can solve this problem with sub-1-V supply operation and provide comparable performance on TC.

V. CONCLUSION

A 0.98-V 15 ppm/°C CMOS bandgap voltage reference, which consumes a maximum of 18 μA at 1.5-V supply and 100 °C, has been presented. The main features are that no low threshold voltage device is needed and thus the circuit is reproducible in any CMOS technology. If low threshold voltage pMOS transistors ($|V_{\rm thp}| < 0.65$ V) are used, the minimum supply voltage can be reduced to about 0.75 V ($V_{\rm EB} + V_{\rm DS(sat)}$). In addition, techniques to achieve sub-1-V operation, such as reducing the threshold voltages by forward biasing the source–bulk junctions, improving the lower common-mode input range of the amplifier by dc level-shifting current mirrors, and low-voltage startup circuits for self-biased voltage reference, have been described.

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