An RF Receiver with an Integrated Adaptive Notch Filter for Multi-Standard Applications

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***Abstract*—This paper presents a 2.4GHz current-mode RF direct-conversion receiver implemented in a 90nm CMOS process with a novel adaptive notch filter. The notch filter uses the blocker frequency to up-convert a DC null to the pass-band, attenuating the blocker before entering the receiver. A synthesized inductor on the order of μH realizes the DC null. Blocker attenuation as large as 20dB is observed at a 40MHz offset frequency while the in-band attenuation increases by only 2dB. This proves that this technique is effective in attenuating blockers in broadband multi-standard radios without using any high-Q mechanical filters at their front-ends.**

***Index Terms*—Active inductors, current mode circuits, interference suppression, SAW filters, time varying circuits.**

I. Introduction

The quest for bandwidth has caused an exponential growth in the number of wireless standards, necessitating the deployment of multi-standard architectures in mobile devices [1], [2], [3]. Integrating multiple modules, each dedicated to certain standard, results in bulky complex designs not suitable for low cost/area/power solutions required for portable platforms. Therefore, removing the frond-end filters and adopting hardware sharing is becoming the preferred approach, particularly for receivers. The most critical challenge in these solutions is the interference issue. Eliminating front-end high-Q band-pass filters results in receiving undesired signals, orders of magnitude higher than the desired one, mandating unrealistically high dynamic range requirements for the entire receiver [4], [5]. However, once the jammer is filtered, the subsequent blocks do not need to maintain the high linearity. Hence one should use the filter as early as possible in the receiver chain to ease the design of the next stages and save power. Unfortunately, such filters have stringent requirement on the quality factor at RF frequencies (typically 100 and above) and are thus not attainable by on-silicon passives. In this paper, an adaptive on-chip notch filter is proposed capable of attenuating close-in blockers before entering the receiver, which thereby relaxes the dynamic range requirements of the core receiver. Different from the passive filters, the sharp pass-band response of the proposed notch filter is achieved in an active fashion, which incorporates a synthesized inductor at low frequencies and up-converts the null to the blocker frequency by using CMOS switches. Moreover, this technique is most suitable for the high-power unknown close-in blockers since it can be adaptively tuned to a specific blockers frequency by injection-locked oscillators or other techniques. This paper is organized as follows. In section II the general notch filter is explained together with the design trade-offs. Section III presents an integrated current-mode direct-conversion CMOS receiver, with the proposed notch filter, realized on-chip. Section IV presents the measurement results for the prototype current mode receiver, which verifies the functionality of the proposed notch filter and section V will conclude.

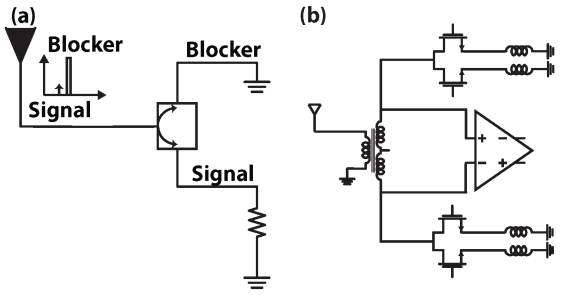

Fig. 1. (a) Conceptual schematic of the front-end notch filter. (b) The proposed blocker removal scheme of the adaptive notch filter

II. Notch Filter Concept and Design

Filter structures with high quality factors in CMOS are very desirable since the subsequent blocks in the chain can be designed without concerning the out-of-band blockers. Hence, with a specific power budget, designers can squeeze more sensitivity and/or accuracy out of their circuits. Technology scaling reduces the available voltage headroom for the CMOS blocks, hence degrades their linearity performance. Conversely, it improves the quality of CMOS switches and capacitors, allowing designers to actively synthesize desired pass-band filter characteristics through frequency translations of base-band filters. High-Q band-pass filters through up-conversion of capacitive low-pass behavior have been demonstrated in [6], [7], [8], [9], [10]. The main drawback of those structure comes from the required input signal impedance. In the previous demonstrations, for the technique to be most effective, the driving source should have a high impedance characteristic, or equivalently the input signal should be in current domain. On the other hand, in most receivers the source impedance is set by the 50Ω antenna radiation resistance, and hence the antenna is effectively a voltage-drive source. Another limitation comes from the power level of the blockers. A high power blocker causes fluctuations at the RF side of the

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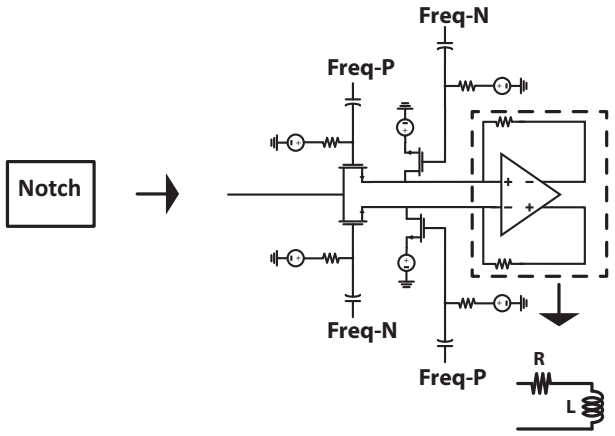

Fig. 2. Detailed circuit schematic of the dynamic notch. Freq-N/P are driven by the blocker signal

filter and degrades its performance through the nonlinearity of the switches. To alleviate these issues, we propose a notch filter. The blockers should ideally see a short circuit at the input of the filter structures, as shown in Fig. 1. and hence the RF fluctuation on the filter nodes is reduced dramatically. As such, close-by high-power blockers can be handled more easily. The main drawback of the notch is the need to have separate frequencies for each blocker. However, at any given time, the number of high power blockers at close-by frequencies should not be too many and hence a combination of notch and band-pass filters should be sufficient for many applications. The architecture in [11] uses the same concept but the notch filter block is placed before the mixer and hence the LNA should still handle the jammer. Essentially a notch filter is a short-circuit at the desired (blocker) frequency. Synthesizing a notch at RF frequencies without an inductor requires incorporating switches and a high-pass filter in the baseband. The simplest high-pass filter is an inductor. At DC it is a short-circuit and at frequencies high enough, it is basically an open-circuit. However, channel bandwidths are between a few hundred kHz to tens of MHz. A suitable inductor for rejecting close-in blockers should therefore be on the order of 1μH. Due to the large area footprint, such a large inductor is impractical for passive implementations in standard CMOS technology. Up to now it seems this idea pushed the issue of inductor design from the RF domain to DC. However, there is a key difference. One can synthesize the inductor actively in the low-frequency domain with extremely high quality-factor and low-form-factor. The architecture in Fig. 2. can emulate the inductor if the unity-gain frequency of the amplifier is low enough. The impedance looking into this structure is:

$$Z_{in} = \frac{R_F}{1 + A(s)} \tag{1}$$

for $f \ll \omega_u$

$$Z_{in} \approx \frac{R_F}{A_{DC}} + \frac{R_F}{\omega_u} s \tag{2}$$

The first term in Eq. 2 is associated with the loss and the second term can be considered as the inductive part. Clearly there is a trade-off between the size of the inductor, resistive loss and the maximum frequency at which the approximation at Eq. 2 is accurate. Setting the gain of the amplifier and the feedback resistor accordingly, the unity gain frequency will determine the magnitude and the bandwidth of the synthesized inductor. For this design, the gain of the amplifier is 70dB, the feedback resistor is 10KΩ and the unity gain is set to 1GHz to realize a 10μH inductor. This value would set the notch bandwidth to 20MHz. Due to other poles and zeros in the frequency response of the op-amp, the input impedance deviated from the inductor at around 100MHz. The sizing of the switches, which are responsible for the frequency shifting, involves a trade-off between the switch loss and the parasitic capacitance associated with the switch. The large switch size minimizes the series resistance of the filter and improves the depth of the notch. However, the parasitic capacitors deteriorate the Q of the filter. Technology scaling helps this trade-off as the $\frac{R_{on}}{C_{off}}$ ratio improves.

III. RECEIVER CIRCUIT IMPLEMENTATION

The prototype circuit, shown in Fig. 3, is implemented in 90nm CMOS, packaged in a QFN48 package and mounted on FR4 PCB. One channel is probed after the current mode filter at the base-band and the other channel is digitized by a current mode sigma-delta ADC and the outputs are 8 digital signals at 1.25GHz (half the LO frequency). The compact filter occupies the area of 800x200μm^2. since it compromises of CMOS switches and op-amps. The largest capacitor required by the op-amp is around 10pF. The LNA is common source and the matching has been achieved by a low-coupling (k-factor) on-chip transformer (Fig. 4). The current signal coming out of the passive mixer will pass through a 4$^{\text{th}}$ order current-mode biquad filter. Current-mode operation is preferred since the entire chain operates in the current-mode. The current-mode filter is more resilient to high-power blockers in low-voltage supplies. The input of the ADC is in current domain and the first integrator converts the signal to the voltage for digitization (Fig. 5). The current-mode input has a two-fold advantage. First it offers better linearity and also the baseband filter placed after the mixer can be connected directly to the ADC. The signal is converted to voltage only at the digitization time.

The switches in the notch filter are copies of the mixers' switches in the main path. The trade-off in sizing the switches is the depth of the notch versus the height of the stop-band. Wide switches have low resistances and hence their contributions to the resistance of the short-circuit seen by jammers are minimized. Conversely, the parasitic capacitances associated with them limit the highest impedance attainable in the stop-band. While incorporating an inductor to tune-out the parasitics lessens the aforementioned phenomenon, nevertheless the sharpness of the filters response would be degraded. Moreover, the effective capacitance of the switches

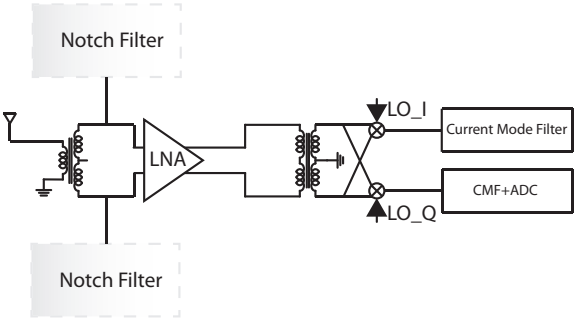

Fig. 3. System level diagram of the current mode receiver with the adaptive notches

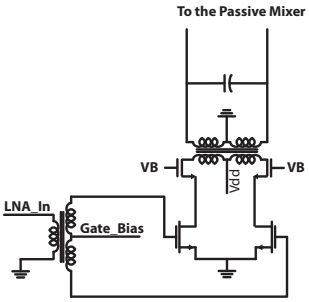

Fig. 4. Simplified schematic diagram of the on-chip transformer and the LNA

is a function of the LO-waveform that could change and exacerbate the response. The amount of attenuation of the blocker and degradation of the desired signal depend on the relative impedances of the filter and the receiver path, which are in parallel (Fig. 3). Lowering the pass-band impedance, which is the series resistances of the amplifier and the switches, improves the attenuation of the blockers. Meanwhile, the desired signal suffers more degradation from diverging to the filter due to the low stop-band impedance. The impedance of the receiver is a function of the antennas impedance due to the matching criterion. Optimum sizing of the notch filter switches depends on the technology node and the antenna impedance. One should note that the quality of switches, $\frac{R_{ON}}{C_{off}}$ improves in more advanced technology. This design, implemented in 90nm CMOS technology, deployed an step-up transformer at the input of the antenna to increase the impedance at the filer side (Fig. 3) to 450Ω and hence minimizes the attenuation of the desired signal. The value of the synthesized inductor (10μH) results in the notch bandwidth of 20MHz which can be reconfigurable by using a bank of resistors in the feedback path of the amplifier (Eq. 2). The bandpass response with comparable bandwidth would require much larger area due to the huge capacitors (on the order of nF) needed. The current consumption of the notch block can be reduced by deploying class-AB for the operational amplifier and implementing the design in more advanced technology nodes since the amplifier can contribute more to the loss due to the improvement of switches and ω_u of the amplifier.

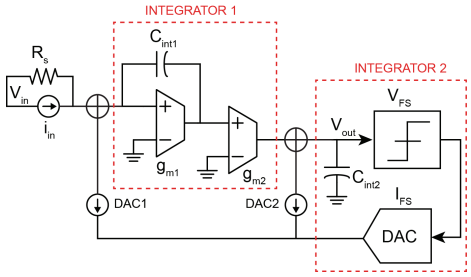

Fig. 5. Block diagram of the current-mode sigma-delta ADC

IV. MEASUREMENT RESULTS

To test the functionality of the dynamic notch (Fig. 6) a blocker signal and the desired signal are summed and injected into the front-end receiver. In the present prototype, the blocker signal is used directly to drive the notch filter, while in an actual system an injection locked oscillator can be used to automatically track and lock to the blocker. The amount of desired blocker attenuation and the amount of undesired in-band signal attenuation are both measured versus the offset frequency of the receiver's local oscillator. One potential concern about having switches in front of the antenna is the leakage of the LO signal to the antenna port. First is the issue of maximum allowable radiated emission. Second, the receiver chain can potentially amplify the signal. This issue has been addressed in the measurement by adjusting the phase of the positive and negative filter's clocks relative to each other. Deploying a bank of small capacitors at both sides and performing the tuning seems a practical solution.

The system is characterized first with the notch filter off. Then, the blocker is injected into the receiver along with the desired low-power signal. The blocker is used to drive the gates of the switches in the filter as well. By looking at the output spectrum, the desired signal as well as the attenuation of the blocker is evident. Fig. 8 and Fig. 9 show the blocker and the desired signal attenuation and increase in the figure respectively versus frequency offset with respect to the carrier frequency. As evident, blocker attenuation as large as 20dB is observed at 40MHz offset while the in-band attenuation

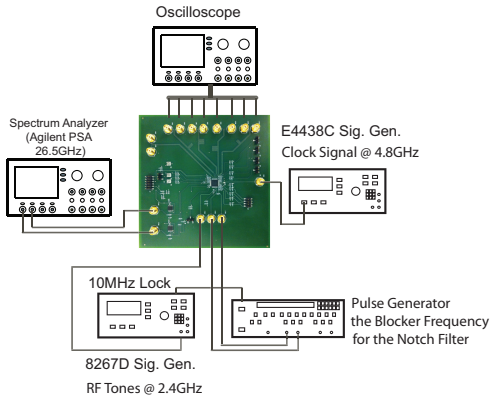

Fig. 6. Measurement setup of the packaged chip on the PCB

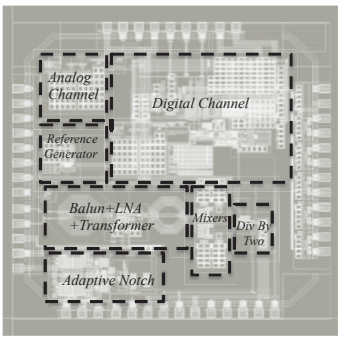

Fig. 7. Die photo of the system

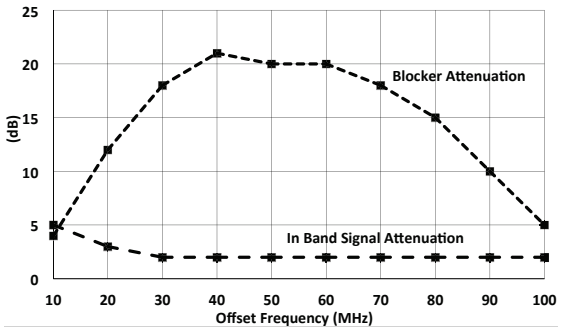

Fig. 8. Blocker and desired signal attenuation vs. offset frequency of the blocker.

increases by only 2dB for blockers as high as -15dBm. The resulting increase in noise figure due to the blocker is therefore 2dB. The noise figure increase in far offset frequencies is due to the synthesized inductor that acts as a capacitor. The receiver draws 52mA from a 1.2V supply. The notch filter consumes 25mW and can be selectively turned ON only when a high power blocker is present.

V. Conclusion

A novel RF notch filter configuration is presented in this paper. The notch filter is adaptive and can be adaptively tuned to different blocker frequencies. The filter attains a sharp frequency response by deploying the combination of frequency translation techniques and synthesizing an inductor in low frequencies. The notch filter is placed right after the antenna and attenuates the blockers by as high as 20dB in 40MHz offset from the carrier frequency while consuming only 25mW. Since the notch filter is placed before the receiver, the design constraints of RF frond-end modules can be relaxed and/or be traded for lower power and better sensitivity. The architecture is compatible with scaling as the performance improves with switch performance (on-resistance, off-capacitance).

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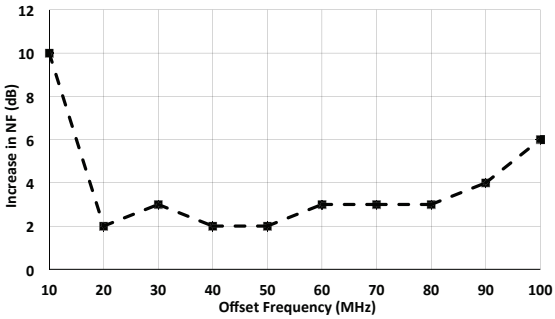

Fig. 9. Increase in the noise figure (NF) vs. offset frequency of the blocker

TABLE I
Performance Summary of the Current Mode Receiver

Frequency	2.5GHz
Gain	110mS
Channel Bandwidth	10MHz
Out-of-Band IP_3	-6dBm
Out-of-Band IP_2	55dBm
Blocker Rejection @ 40MHz	20dB
Power	52mA (Analog) + 18mA (Digital)
Supply Voltage	1.2V
Technology	90nm

References

[1] L. Van der Perre, J. Craninckx, and A. Dejonghe, *Green Software Defined Radios: Enabling seamless connectivity while saving on hardware and energy*. Springer, 2008.

[2] R. Bagheri, A. Mirzaei, M. Heidari, S. Chehrazi, M. Lee, M. Mikhemar, W. Tang, and A. Abidi, "Software-defined radio receiver: dream to reality," *Communications Magazine, IEEE*, vol. 44, no. 8, pp. 111–118, 2006.

[3] B. Razavi, "Cognitive radio design challenges and techniques," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 8, pp. 1542–1553, 2010.

[4] Z. Ru, N. A. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 12, pp. 3359–3375, 2009.

[5] H. Darabi, "Overview of front-end rf passive integration into socs," *Multi-Mode/Multi-Band RF Transceivers for Wireless Communications: Advanced Techniques, Architectures, and Trends*, pp. 113–158, 2011.

[6] D. Von Grunigen, R. Sigg, J. Schmid, G. Moschytz, and H. Melchior, "An integrated cmos switched-capacitor bandpass filter based on n-path and frequency-sampling principles," *Solid-State Circuits, IEEE Journal of*, vol. 18, no. 6, pp. 753–761, 1983.

[7] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-q bandpass filters in saw-less receivers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, no. 5, pp. 879–892, 2011.

[8] J. Borremans, G. Mandal, V. Giannini, B. Debaillie, M. Ingels, T. Sano, B. Verbruggen, and J. Craninckx, "A 40 nm cmos 0.4–6 ghz receiver resilient to out-of-band blockers," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 7, pp. 1659–1671, 2011.

[9] A. Mirzaei and H. Darabi, "Reconfigurable rf front-ends for cellular receivers," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2010 IEEE*. IEEE, 2010, pp. 1–4.

[10] J. Borremans, G. Mandal, B. Debaillie, V. Giannini, and J. Craninckx, "A sub-3db nf voltage-sampling front-end with+ 18dbm iip 3 and+ 2dbm blocker compression point," in *ESSCIRC, 2010 Proceedings of the*. IEEE, 2010, pp. 402–405.

[11] R. Vazny, W. Schelmbauer, H. Pretl, S. Herzinger, and R. Weigel, "An interstage filter-free mobile radio receiver with integrated tx leakage filtering," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*. IEEE, 2010, pp. 21–24.