TRANSIENT-INDUCED LATCHUP IN CMOS INTEGRATED CIRCUITS

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© 2009 John Wiley & Sons (Asia) Pte Ltd. ISBN: 978-0-470-82407-8

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IEEE PRESS

John Wiley & Sons (Asia) Pte Ltd

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Library of Congress Cataloging-in-Publication Data

Ker, Ming-Dou.
Transient-induced latchup in CMOS integrated circuits/Ming-Dou Ker, Sheng-Fu Hsu.
p. cm.
Includes bibliographical references and index.
ISBN 978-0-470-82407-8 (cloth)
1. Metal oxide semiconductors, Complementary–Defects. 2. Metal oxide semiconductors, Complementary–Reliability. I. Hsu, Sheng-Fu. II. Title.

TK7871.99.M44K47 2009
621.39′5–dc22

2008045600

ISBN 978-0-470-82407-8 (HB)

Typeset in 11/13pt Times by Thomson Digital, Noida, India.
Printed and bound in Singapore by Markono Print Media Pte Ltd, Singapore.
This book is printed on acid-free paper responsibly manufactured from sustainable forestry in which at least two trees are planted for each one used for paper production.

Contents

Preface

With the continual scaling of complementary metal-oxide-semiconductor (CMOS) technologies, latchup is an increasingly significant reliability issue in semiconductor technologies. Because of the parasitic silicon controlled rectifier (SCR) in CMOS, latchup can be initiated via a positive regeneration feedback if there is a large enough substrate or well current. Once latchup occurs in a powered system, huge currents can conduct through a low-impedance path from the power supply to the ground nodes. If the resulting high current is not limited, irreversible damage can occur in CMOS integrated circuits (IC) due to the latchup-generated high power. Even though the latchup current is limited to prevent permanent damage, it is highly possible that CMOS ICs will malfunction due to a "latched" power system.

Transient-induced latchup (TLU) means a latchup event initiated by a fast transient triggering mode. Several different transient triggering modes have been proven to be able to initiate TLU, such as power-on transition, transmission line reflections, supply voltage overshoots or undershoots, and cable discharge events (CDE). In addition to these transient triggering modes, the system-level electrostatic discharge (ESD) stress has been verified as a significant TLU-triggering mode, especially when modern electronic products are usually requested to satisfy the electromagnetic compatibility (EMC) regulations. The system-level ESD test is commonly used to evaluate the system-level ESD robustness of electronic products. During the system-level ESD test, the ESD-generated transient current can induce TLU in CMOS ICs within the electronic products, leading to temporary shutdown or permanent damage of the equipment under test (EUT). Such a system-level ESD stress can induce TLU much more easily than any other of the TLU-triggering sources described above, because the ESD tester (ESD gun) can carry a high charged voltage up to ± 15 kV. Once such a huge energy stresses the EUT through direct contact or indirect coupling, it can induce a large noise current to induce TLU in COMS ICs. The physical mechanism of TLU under a system-level ESD test has not been so clear until recently. Thus, this book mainly focuses on TLU induced by the system-level ESD stress.

In Chapter 1, an overview of latchup is given at first, including the introduction of latchup phenomena and characterization. The background of TLU is subsequently introduced, and the categories of several TLU-triggering modes are also summarized,

including the power-on transition, transmission line reflections, supply voltage overshoots or undershoots, cable discharge events, and system-level ESD stresses. Furthermore, the recently announced standard practice to evaluate the TLU immunity of CMOS ICs is also introduced. Compared with the conventional latchup standard commonly adopted in industry, this TLU standard practice has different test setups and latchup triggering sources. This implies that the physical mechanism of TLU is different from conventional latchup, and the foundation of the TLU test standard is necessary.

Chapter 2 focuses on clarification of the TLU physical mechanism in CMOS ICs in the system-level ESD test. An underdamped sinusoidal voltage stimulus is clarified as the realistic TLU-triggering stimulus in the system-level ESD test. With TLU characterization by device simulation and experimental verification in the time domain, the specific "sweep-back" current caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs is qualitatively proved to be the major cause of TLU. A simple 1-D analytical model of such a "sweep-back" current is also introduced. This model can qualitatively describe the sweep-back current dependency on the TLU-triggering stimulus in the system-level ESD test.

Chapter 3 introduces a component-level TLU measurement setup with a bipolar (underdamped sinusoidal) voltage trigger source. This measurement setup can evaluate the TLU immunity of a single IC by monitoring the voltage/current waveforms through an oscilloscope. Additionally, by applying the bipolar trigger voltage on the power pins of a device under test (DUT), it can accurately simulate how a CMOS IC will be disturbed by the ESD-generated noises in the system-level ESD test. With the component-level TLU measurement setup, different types of board-level noise filter networks can be evaluated to find their effectiveness for improving the TLU immunity of CMOS ICs.

Chapter 4 characterizes the TLU dependencies on the two dominant parameters of TLU-triggering transient noises, power-pin damping frequency and damping factor. In real situations, they are strongly dependent on the system shielding, board-level noise filter, chip-/board-level layout, and so on. Their impacts on the TLU immunity can be well explained in the time domain by device simulation. Based on the comprehensive simulation results and experimental verifications, board-level noise filters can be properly developed to efficiently eliminate the ESD-coupled noises for TLU prevention.

Chapter 5 introduces TLU under the electrical fast transient (EFT) test. The EFT test is used to demonstrate the immunity of electronic equipment to transient disturbances such as those originating from switching transients. During the EFT test, the EFT generator applies a number of fast pulses, coupled into the power supply, control, signal, and ground ports of electronic equipment. In the same way as the system-level ESD test, TLU can be easily initiated by a sweep-back current in the EFT test. Different types of noise filter networks are also investigated to find their effectiveness for improving the TLU immunity against EFT tests.

Chapter 6 introduces the experimental methodologies to extract area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, for

internal circuits, and for I/O and internal circuits. Through detailed investigations of latchup immunity dependencies on variations of geometrical layout parameters and temperatures, compact and safe layout rules can be established for latchup prevention in a given CMOS process. Such skills are useful for foundries to provide their customers a safe process design rule without suffering latchup issues, and are also helpful for IC designers to understand the latchup immunity dependencies on IC layout plans.

Chapter 7 introduces several special layout issues for latchup prevention. Neglecting these layout issues could draw unanticipated latchup danger, including latchup between two power domains, between power-pins and grounded N+ /N-wells, and between two adjacent I/O cells, and so on. The ESD-coupled diodes between separated power lines can also lead to unexpected latchup. Direct connection between the I/O pads and the N+ /P+ diffusions in internal circuits could easily initiate latchup in internal circuits. Additionally, if the power-rail ESD clamp circuit is very close to the I/O pads, an ESD-clamping NMOS could be unexpectedly turned on during the negative trigger current test, probably initiating the latchup in the nearby internal circuits. The corresponding solutions to these unexpected latchup issues are also introduced. By using these, IC designers could prevent possible design mistakes, eliminate the waste of masks and wafers, and decrease the time to market for products.

Chapter 8 introduces several TLU issues in power-rail ESD clamp circuits fabricated in both low-voltage (LV) and high-voltage (HV) 40-V COMS processes. In the LV CMOS process, although the TLU-free ESD-clamp circuit can be easily designed by placing double guard rings to surround each MOS devices, a specific "TLU-like" failure would still occur due to the latch-on state of the ESD-clamping NMOS in the system-level ESD test. In the HV CMOS process, the bottleneck is that the latchup holding voltage is generally much smaller than the HV nominal operating voltage, thus inevitably leading to TLU risks in HV power-rail ESD clamp circuits. In addition to the clarification of TLU-related issues in the power-rail ESD clamp circuits, the investigation and design of TLU-free power-rail ESD clamp circuits are also introduced. These TLU-free power-rail ESD clamp circuits can guarantee robust ESD immunity without suffering TLU or any TLU-like danger in both LV and HV CMOS ICs.

Chapter 9 gives a brief summary of TLU. The concepts to extract compact and safe design rules for latchup or TLU prevention are also summarized. A practical example of extracting layout rules/guidelines for latchup prevention in a 0.18-μm 1.8 V/3.3 V silicided CMOS process is given in the Appendix. The methodologies to extract all the latchup design rules/guidelines are in compliance with those presented in Chapter 6, including latchup layout rules for I/O cells, for internal circuits, and for between I/O and internal circuits. Latchup layout rules for circuits across two different power domains are also extracted to avoid the possible latchup danger between two N-wells powered by two different power supply voltages, as introduced in Chapter 7. Such skills can be further implemented in any given CMOS process to extract reliable design rules without suffering latchup danger.

1

Introduction

Due to the aggressive scaling of device feature sizes and strict demands of electromagnetic compatibility (EMC) regulations, transient-induced latchup (TLU) is increasingly a primary reliability issue in CMOS integrated circuits (IC). In this chapter, latchup overview is given at first, including the introduction of latchup phenomena and characterization. The background of TLU is subsequently introduced. It has been found that several TLU-triggering modes (rather than just one) probably initiate TLU, and the categories of these TLU-triggering modes are summarized. Furthermore, the recently announced standard practice to evaluate the TLU immunity of CMOS ICs will be also introduced.

1.1 Latchup Overview

It has been a long time since latchup was a significant reliability issue in semiconductor technologies [1–15]. Latchup originates from the parasitic silicon controlled rectifier (SCR) in CMOS technologies, which is composed of two cross-coupled parasitic bipolar junction transistors (BJT). For example, the device cross-sectional view of a basic CMOS logic circuit, an inverter, is shown in Figure 1.1 along with the two parasitic BJTs which comprise the inherent SCR. These two parasitic BJTs are a vertical PNP (Q_{pnp}) and a lateral NPN (Q_{npn}) BJT. Under normal circuit operating conditions, this CMOS logic circuit acts as an inverter, and the parasitic SCR has no adverse effect to circuit function and can be totally ignored. However, if latchup is initiated by any latchup-triggering events, the parasitic SCR will turn on and dominate the circuit function. As a result, huge current will flow through the low-impedance latchup path, leading to the circuit malfunction or even worse chip burn-out danger.

The equivalent circuit of the parasitic SCR is illustrated in Figure 1.2, and its typical latchup I–V characteristic is shown in Figure 1.3. V_{Trig} (I_{Trig}) and V_{Hold} (I_{Hold}) are referred to as the latchup trigger voltage (current) and holding voltage (current), respectively.

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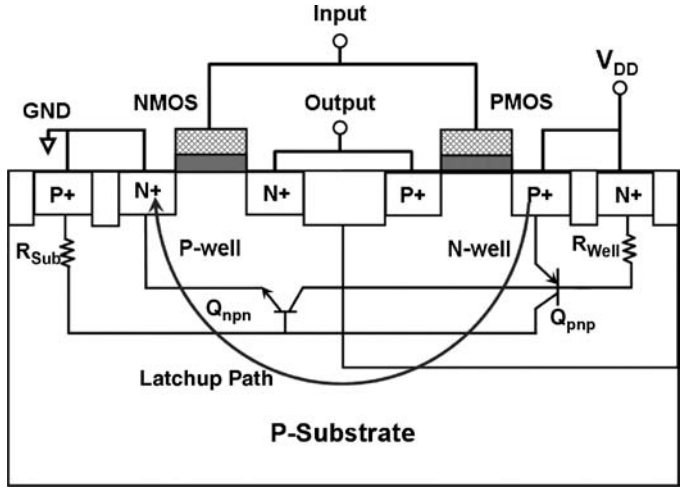


Figure 1.1 Device cross-sectional view of an inverter circuit in CMOS technologies. The two parasitic BJTs are a vertical PNP (Q_{pnp}) and a lateral NPN (Q_{npn}) BJT.

Initially at a small applied voltage ($V < V_{Trig}$), the SCR is in its high-impedance off (blocking) state, and the current flowing through from V_{DD} to the GND is negligible. Afterwards, if the applied voltage continually increases up to V_{Trig}, the reverse-biased N-well/P-substrate junction can generate a reverse junction breakdown current, which is the dominant current of I_{Trig}. Such a junction breakdown current can flow through the parasitic substrate (well) resistance of R_{Sub} (R_{Well}), turning on the Q_{npn} (Q_{pnp}) because of its forward-biased emitter-base junction. Once the Q_{npn} (Q_{pnp}) is turned on, the other Q_{pnp} (Q_{npn}) can be also turned on via the mechanism of the positive regeneration feedback. This transition region of positive regeneration feedback is unstable, and represents a negative-resistance region in the latchup *I–V* characteristic, as shown in Figure 1.3. If the product of the beta gains of these two BJTs is larger than one, this positive feedback mechanism can be maintained, leading to a large current conducting through a low-impedance path from V_{DD} (source of PMOS) to GND (source of NMOS). This phenomenon is the so-called latchup. This low-impedance on state in the latchup *I–V* curve is also referred to as the "holding region", and the minimum applied voltage (current) required to sustain this low-impedance state is V_{Hold} (I_{Hold}). If the resulting latchup current is not limited, CMOS could be burned out due to the latchup-generated high power. Even if the latchup current is limited such that no permanent damage occurs in CMOS ICs, the low-impedance path existing between V_{DD} and the GND usually causes circuit malfunction.

In CMOS technologies, latchup can occur in any parasitic SCR structures located in I/O cells or core circuits. The schematics and the layout top views of an inverter, a 2-input NAND gate, and a 2-input NOR gate are shown in Figures 1.4–1.6, respectively.

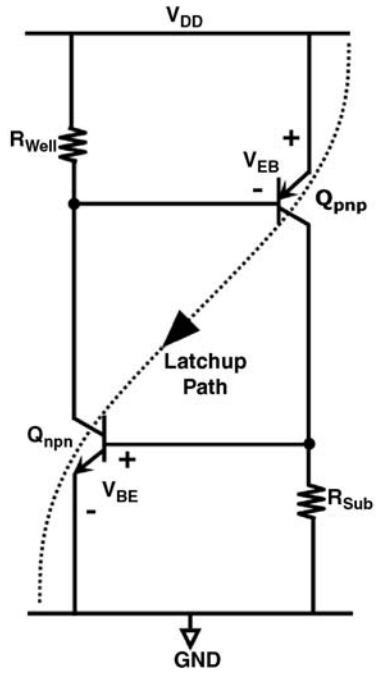


Figure 1.2 Equivalent circuit of the parasitic SCR in CMOS technologies.

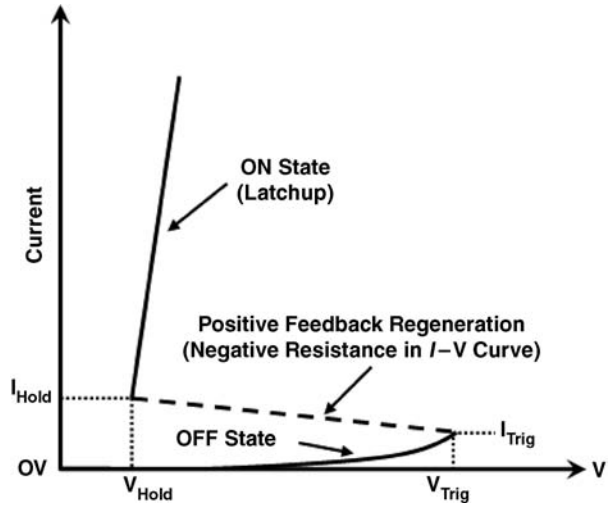


Figure 1.3 Typical latchup *I–V* characteristic in CMOS ICs.

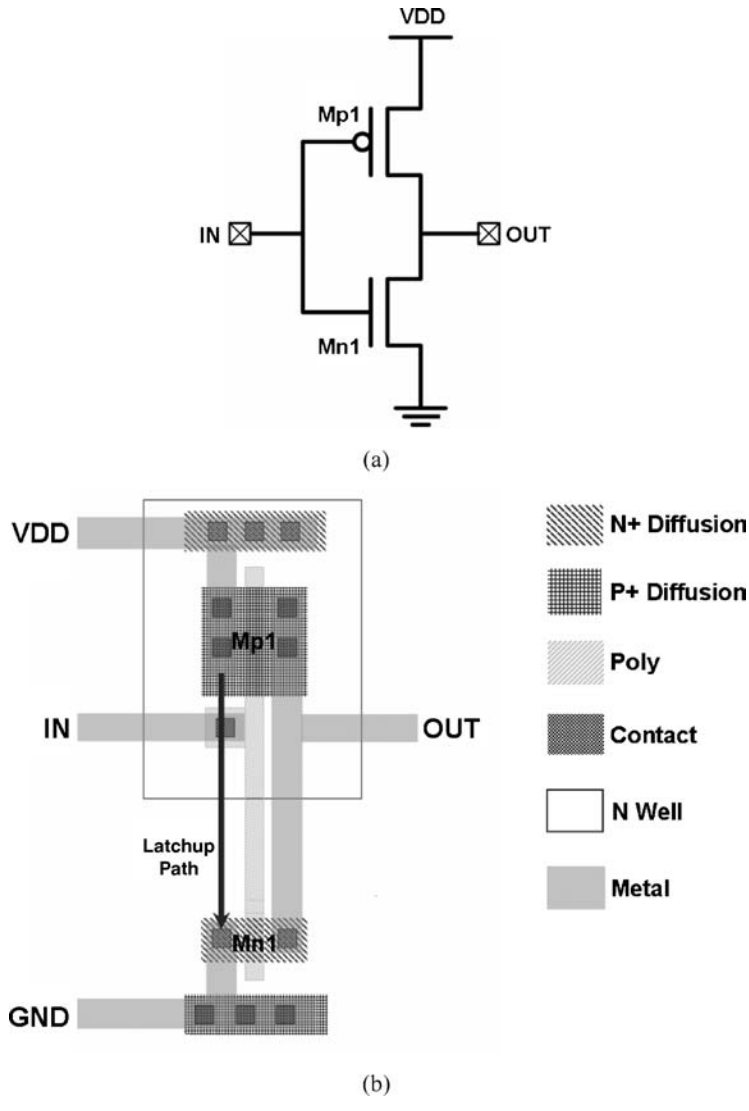


Figure 1.4 (a) Schematic, and (b) layout top view of an inverter. When latchup occurs, the latchup path goes from VDD to GND along the parasitic PNPN SCR structure.

These basic logic gates are always highly integrated in core circuits to save chip size, and therefore the guard rings are generally unallowable for latchup protection in order to save more chip layout area. Once there is an abnormal amount of noise injection current or power lines noise around the chips, latchup could be easily triggered on in such highly-integrated transistors area, as the latchup paths shown in Figures 1.4b,

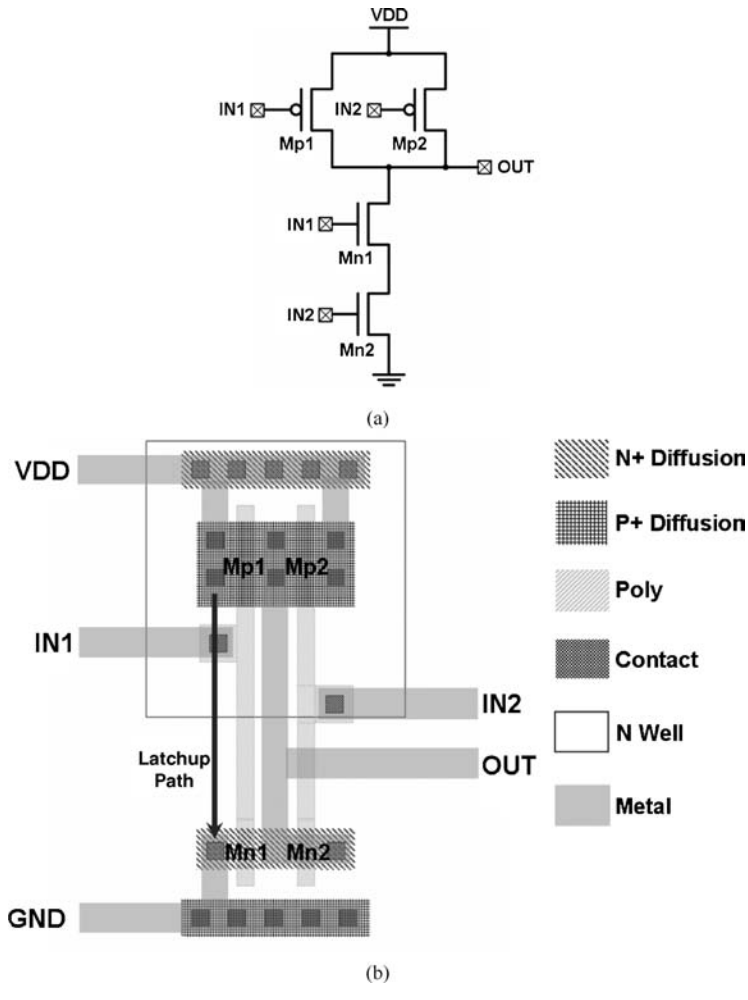


Figure 1.5 (a) Schematic, and (b) layout top view of a 2-input NAND gate. When latchup occurs, the latchup path goes from VDD to GND along the parasitic PNPN SCR structure.

1.5b, and 1.6b, respectively. Thus, proper layout rules, process techniques, and circuit design methodologies for latchup protection are necessary to ensure latchup-robust CMOS ICs.

In addition to the junction breakdown current produced by the power supply over voltage, any trigger sources that can generate substrate/well current in CMOS ICs could probably initiate TLU, such as punchthrough and transient overshoot or undershoot on the I/O pins of CMOS ICs. To achieve a robust immunity of CMOS ICs against latchup, ensuring that the V_{Hold} is greater than the V_{DD} (normal circuit operating voltage) is a simple criterion for judgment. If the V_{Hold} is greater than V_{DD},

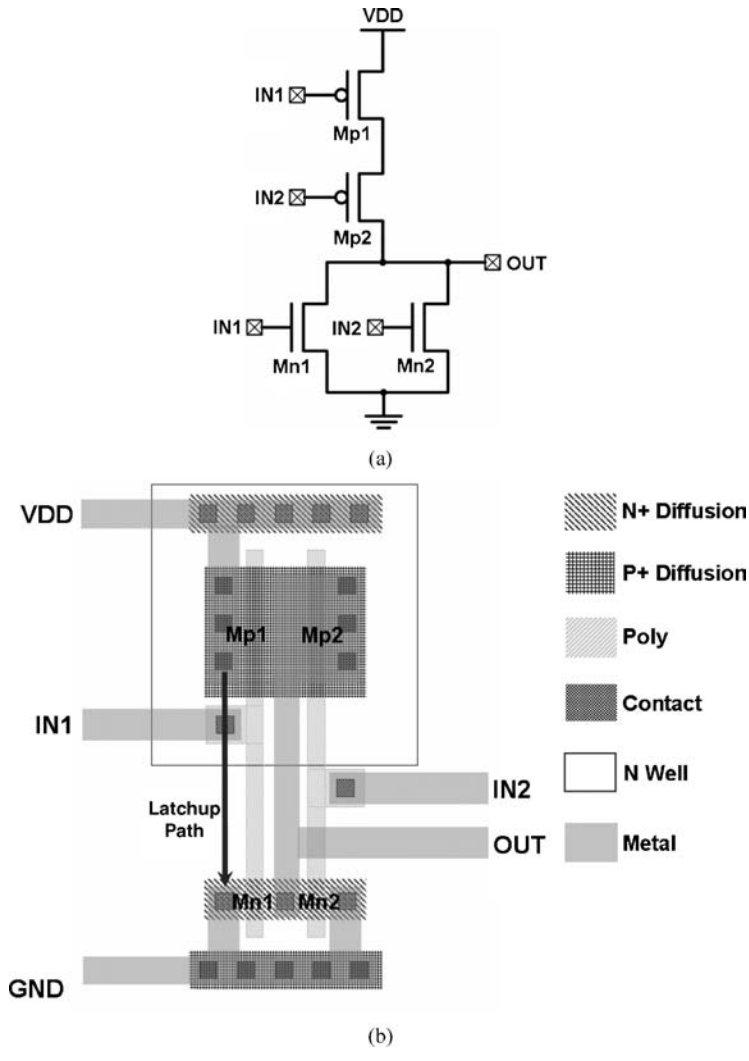


Figure 1.6 (a) Schematic, and (b) layout top view of a 2-input NOR gate. When latchup occurs, the latchup path goes from VDD to GND along the parasitic PNPN SCR structure.

the maximum power supply voltage in CMOS chips is still smaller than the voltage required to sustain latchup. As a result, latchup never occurs and the purpose of "latchup-free" can be fulfilled, regardless of whatever the latchup-triggering modes. In contrast, for a V_{Hold} lower than V_{DD}, it is still possible for latchup to be maintained after the latchup-triggering modes are removed. Thus, to raise the V_{Hold} higher than V_{DD} whenever possible, some process, layout, or circuit techniques for latchup prevention are indeed necessary.

1.2 Background of TLU

TLU means a latchup event initiated by a fast "transient" triggering mode. Once some transient triggering mode happens to generate large enough substrate or well current in CMOS ICs, TLU can be triggered on via a positive-feedback mechanism. With the continual scaling of CMOS technologies [16], the smaller device feature size enables a larger packing density of transistors in CMOS chips. However, CMOS ICs are more susceptible to TLU because the spacing from the N+ to P+ junction has been also continuously decreasing. With the increased focus on powerful functionality and low cost, state-of-the-art IC design trends or process technologies lead TLU to be a serious reliability issue, such as mixed signal products, high level integration system-on-chip (SOC), radio frequency (RF), scaling of trench isolation, usage of low-doped substrate, and so on. Also, for electronic products/equipments necessarily to meet the strict demands of EMC regulations, the CMOS ICs located with the equipment under test (EUT) are found to be very susceptible to TLU under the system-level ESD test. As a result, the reliability issue of TLU has attracted more attention recently than before in CMOS technologies [17–25]. Compared with the quasi-static latchup, TLU is much more complicated for modeling and characterization, and therefore raises the difficulties in developing the corresponding TLU-protection techniques. Furthermore, due to various TLU-triggering modes and lack of comprehensive measurement techniques, the formal test standard for TLU has not been established yet, but only "standard practice" [26] to evaluate the TLU immunity of CMOS ICs. For quasi-static latchup, however, the formal test standard [27] has been announced and widely used for evaluations of latchup immunity in the ICs industry. Therefore, in order to develop a TLU-robust IC or electronic product, it is critical to simultaneously clarify the TLU physical mechanism and develop an efficient TLU measurement setup.

1.3 Categories of TLU-Triggering Modes

Several different transient triggering modes have been proven to be able to initiate TLU [3–6, 20, 21]. These transient triggering modes include power-on transition [3, 4], transmission line reflections [5, 6], supply voltage overshoots [20], cable discharge event (CDE) [21], and system-level electrostatic discharge (ESD) event [28, 29]. In most of these transient triggering modes, their corresponding measurement setups have been also developed to evaluate the TLU immunity of CMOS ICs. These TLU-triggering modes are introduced below.

1.3.1 Power-On Transition [3, 4]

When the power-supply voltage ramps up from 0 V to its normal circuit operating voltage during the power-on transition, the displacement current will be formed due to the rapidly increasing power-supply voltage. The time-dependent power-supply

voltage during the power-on transition is shown in Figure 1.7. The ramp rate (RA) of the power-supply voltage during the power-on transition can be expressed as follows:

$$RA \equiv \frac{V_{DD}}{T_r} \tag{1.1}$$

where V_{DD} is the normal circuit operating voltage, and T_r is the rise time of the power-supply voltage.

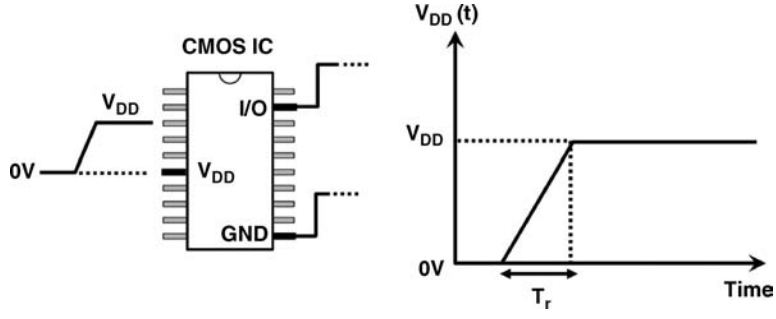


Figure 1.7 Time-dependent power-supply voltage during the power-on transition.

Once the RA is above some critical value, the TLU will be triggered on by the large enough displacement current that flows through the well/substrate junction capacitance ($C_{Well–Sub}$) of CMOS ICs, as shown in Figure 1.8. By applying different ramp rates of the power-supply voltage, the threshold ramp rate to initiate the TLU can be evaluated. The susceptibility of this TLU is strongly dependent on the ramp rate of the power-supply voltage, because TLU can occur even if the normal circuit operating voltage is far below the required latchup trigger voltage in the DC latchup *I–V* characteristic.

1.3.2 Transmission Line Reflections [5, 6]

When the transmission line reflections take place due to impedance mismatch during signal propagation, transient voltage overshoots or undershoots can occur on the I/O pins of CMOS ICs, as shown in Figure 1.9. Because the I/O pins are directly connected to the P+ (N+) diffused areas in the N-well (P-substrate), such transient voltage overshoots (undershoots) can make the emitter-base junction of the parasitic PNP (NPN) BJT momentarily forward-biased. Once the forward-biased emitter-base junction of one parasitic BJT provides enough diffusion current to turn on the other parasitic BJT, the positive-feedback regeneration mechanism can induce TLU. The techniques to simulate transient voltage overshoots and undershoots on the I/O pins of CMOS ICs are shown in Figure 1.10a and b, respectively. The transient voltage

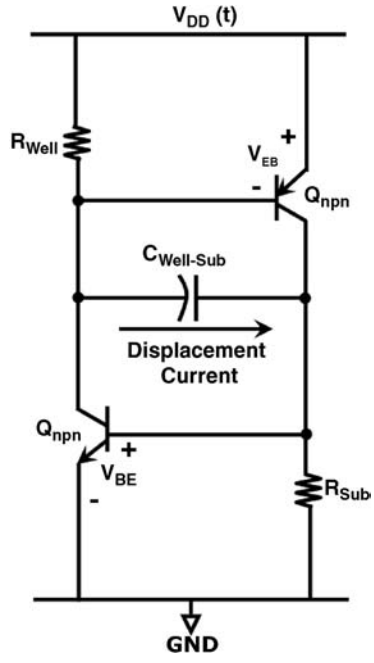


Figure 1.8 Displacement current generated by the rapidly increasing power-supply voltage on the well/substrate junction capacitance ($C_{\text{Well–Sub}}$).

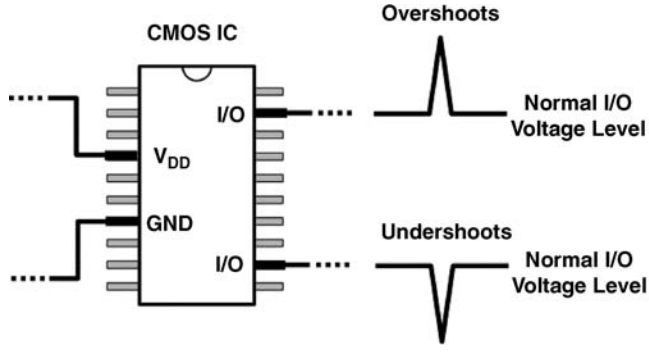
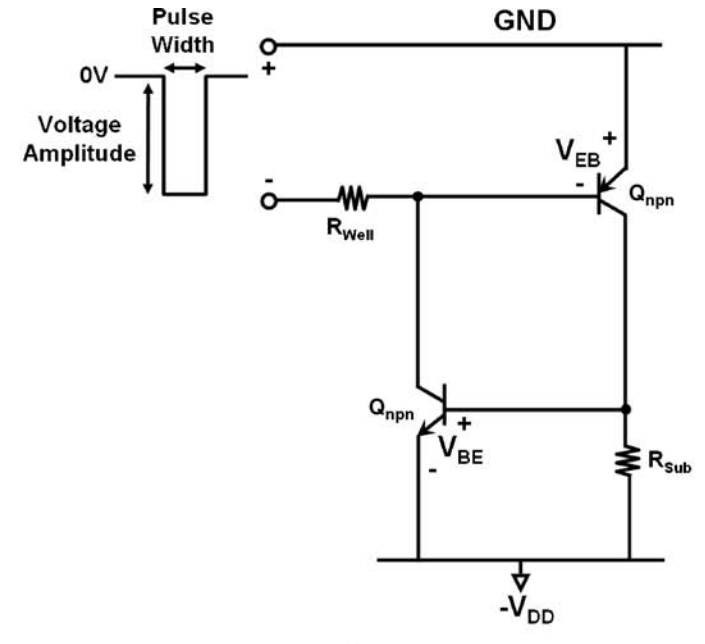
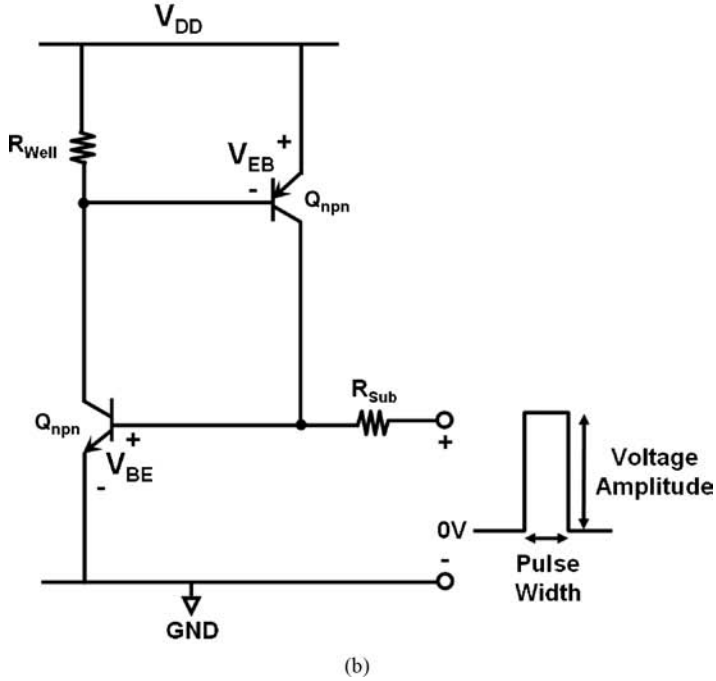


Figure 1.9 Transient voltage overshoots or undershoots on the I/O pins of CMOS ICs due to the transmission line reflections.

overshoots (undershoots) can be simulated by applying a rectangular voltage pulse on the emitter-base junction of the parasitic PNP (NPN) BJT in CMOS ICs. Thus, the threshold voltage amplitude and pulse width to initiate TLU can be determined. In general, when the pulse width decreases, the threshold voltage amplitude required to induce TLU will increase. However, when the pulse width is large enough,



(a)



(b)

Figure 1.10 Techniques to simulate the transient (a) overshoots, and (b) undershoots, on the I/O pins of CMOS ICs.

a quasi-static situation could be reached. As a result, the threshold voltage amplitude required to induce TLU is approximate to the DC bias (∼0.7 V) required to turn on the emitter-base junction of the parasitic BJT in CMOS ICs.

1.3.3 Supply Voltage Overshoots [20]

The transient overshoots on the power-supply voltage can take place due to the noise coupling under system or environment disturbance, as shown in Figure 1.11. Such transient overshoots on the power-supply voltage can induce the junction displacement or breakdown current within the CMOS ICs. If the displacement or breakdown current is large enough to activate the parasitic PNP or NPN BJT, TLU can be triggered on and sustained via the regeneration feedback. The measurement techniques to simulate the transient overshoots on power-supply voltage are shown in Figure 1.12. The power-

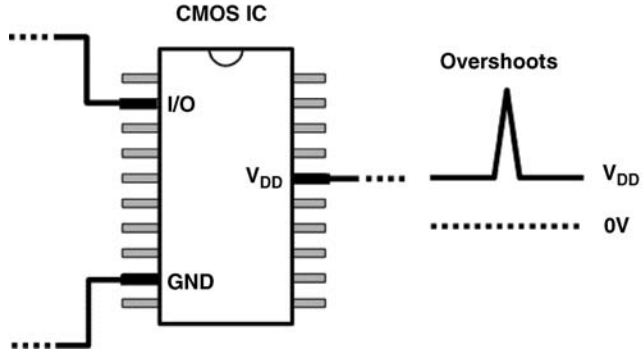


Figure 1.11 Transient overshoots on the power-supply voltage due to the noise coupling under system or environment disturbance.

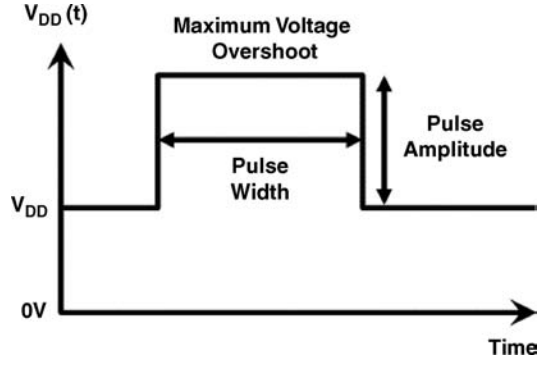


Figure 1.12 The TLU-triggering source used to simulate the supply voltage overshoots: positive-going rectangular voltage pulse applied on the power pins of CMOS ICs.

supply voltage overshoots can be simulated by applying a positive-going rectangular pulse voltage which is superposed on the normal circuit operating voltage (V_{DD}). Such a positive-going rectangular pulse voltage superposed on V_{DD} can simulate rapidly increasing overshoots on V_{DD}, leading to the excitation of displacement or a breakdown current. Related experimental results show that the minimum (threshold) voltage amplitude to initiate TLU decreases with the pulse width, regardless of positive or negative voltage pulses.

1.3.4 Cable Discharge Event [21]

A large number of charges can accumulate in cables when the unterminated cables are dragged on the floor (known as triboelectricity). The cable discharge event (CDE) is the phenomenon in which the accumulated charges in cables are discharged into another object in close proximity. An example of the CDE event occurring on the Ethernet interface of computer systems is shown in Figure 1.13. Once the accumulated static charges in cables are discharged into the I/O pins of CMOS ICs, TLU can be easily initiated within the CMOS ICs due to the injection of the transient positive or negative currents.

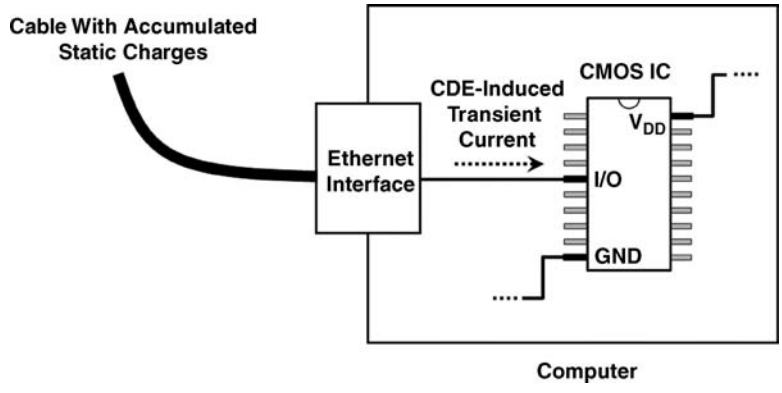


Figure 1.13 Example of the CDE event occurring on the Ethernet interface of computer systems.

CDE-induced TLU is a typical off-chip signal latchup-triggering event; injection of the CDE-induced current can induce TLU on I/O or the internal circuits of CMOS ICs. For the general off-chip signal latchup-triggering events, most CMOS IC products use the EIA/JESD78A latchup test [27] to evaluate the product robustness. Compared with the other off-chip signal latchup-triggering events, however, CDE-induced latchup is a more severe latchup condition because the injection of an CDE-induced current can possess peak current of several amps. Thus, the EIA/JESD78 latchup test standard is unsuitable for evaluations of the CDE-induced latchup robustness, and so far there

is no established component-level test standard for CDE-induced latchup. In the state-of-the-art CMOS technologies where the TLU issues are more severe, design methodologies to suppress CDE-induced TLU are needed to be developed.

1.3.5 System-Level ESD Event [28, 29]

ESD is a phenomenon due to the electrostatic charges transferring from one object to another with different electric potentials [30, 31]. Usually, a huge transient current or electromagnetic interferences (EMI) accompany the ESD phenomenon. In the real world, electronic products or systems could malfunction or be damaged when subjected to ESD events. Thus, a system-level ESD event is an important interference source to evaluate the electromagnetic sustainability (EMS) of electronic products. Thus, for electronic products to satisfy the electromagnetic compatibility (EMC) regulations, the system-level ESD test [32] is necessary to evaluate the system-level ESD robustness of electronic products.

The international standard [32], *IEC 61000-4-2*, established and issued by the *International Electrotechnical Commission* (IEC) specify the test methods and levels for electrical equipment subjected to system-level ESD events. Two major test modes are specified in this system-level ESD test – contact discharge and air discharge test modes. In the contact discharge test mode, the discharge tip of the ESD gun is held in contact with the EUT, and the discharge is actuated by the discharge switch within the ESD gun. In the air discharge test mode, in contrast, the discharge tip of the ESD gun is brought close to the EUT, and the discharge is actuated by a spark to the EUT. Moreover, either test mode has two applications – direct and indirect applications. Direct application means the discharge directly applies to the EUT. However, indirect application means the discharge applies to a coupling plane (horizontal or vertical) in the vicinity of the EUT, simulating the personnel discharge to objects which are adjacent to the EUT. An example of the system-level ESD test with a direct contact discharge test mode on an electronic product is shown in Figure 1.14. Compared with the component-level ESD tests [33–35] where the objects under test are ICs, the system-level ESD test aims to evaluate the robustness of electronic products. An illustration and the equivalent circuit of the ESD gun used in the system-level ESD test are shown in Figure 1.15a and b, respectively. The ESD gun has a charging (energy-storage) capacitor of 150 pF and a discharge resistor of 330 Ω. An illustration of the discharge tips is also depicted in Figure 1.16. Such a charging capacitor (discharge resistor) is much larger (smaller) than that in the component-level ESD test. Figure 1.17 shows, for example, the equivalent circuit for modeling the discharge from a human body to the "device under test." The charging capacitor (discharge resistor) is 100 pF (1.5 kΩ), which is 1.5 × smaller (∼5 × larger) than that in system-level ESD test. The typical waveform of the output current of the ESD gun is shown in Figure 1.18. The rise time is very small, $0.7 \sim 1$ ns, which is smaller than that of $2 \sim 10$ ns in the HBM ESD test. As a result, compared with the ESD current in the component-level

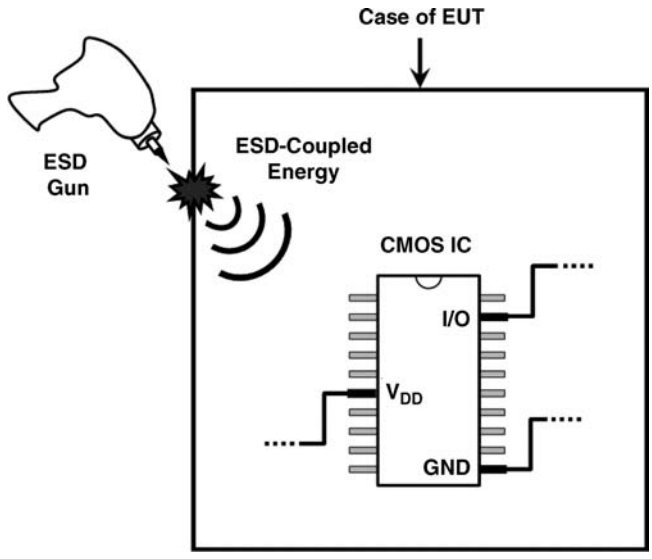


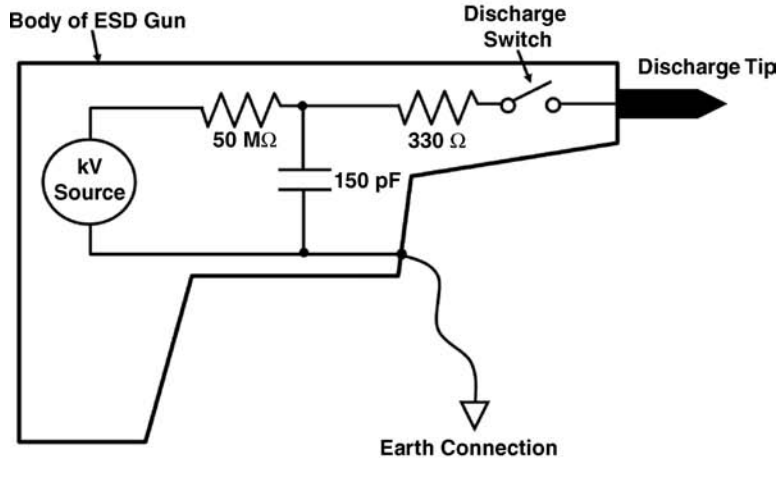
Figure 1.14 Example of the system-level ESD test with a direct contact discharge test mode on an electronic product.

ESD test, the ESD current in the system-level ESD test has a much larger peak current and a shorter rise time, leading to more severe damage for electronic products or their interior ICs.

The preferential range of the test levels for the system-level ESD test is given in Table 1.1. The failure criteria of the test results are also shown in Table 1.2. For consumer electronic products, such as LCD monitors, digital cameras, cell phones, and so on, are generally demanded to at least pass the test level of level 4 and the failure criterion of level B. That is, EUT should suffer at least 8 kV (15 kV) for contact (air) discharges without any malfunctions, or the EUT works abnormally during ESD stress but it can reset automatically. Due to the tight requirements of standard specifications, protection design techniques against the system-level ESD always draw much attention from system or IC designers. However, ESD protection designs for system- and component-level ESD tests are quite different. It has been proven [36] that a robust CMOS IC product with high component-level ESD levels could be very susceptible to the system-level ESD test. Thus, efficient ESD protection methodologies against system-level ESD events are very significant for electronic products.

During the system-level ESD test, the ESD-generated transient current can induce TLU in CMOS ICs within the electronic products, leading to temporary shutdown or permanent damage of the EUT. Thus, a clear understanding of the TLU physical mechanism is necessary to help systems or IC designers to solve TLU issues under the system-level ESD test.

(a)



(b)

Figure 1.15 (a) An illustration, and (b) the equivalent circuit, of the ESD gun used in the system-level ESD test. The ESD gun has a charging (energy-storage) capacitor of 150 pF and a discharge resistor of 330 Ω.

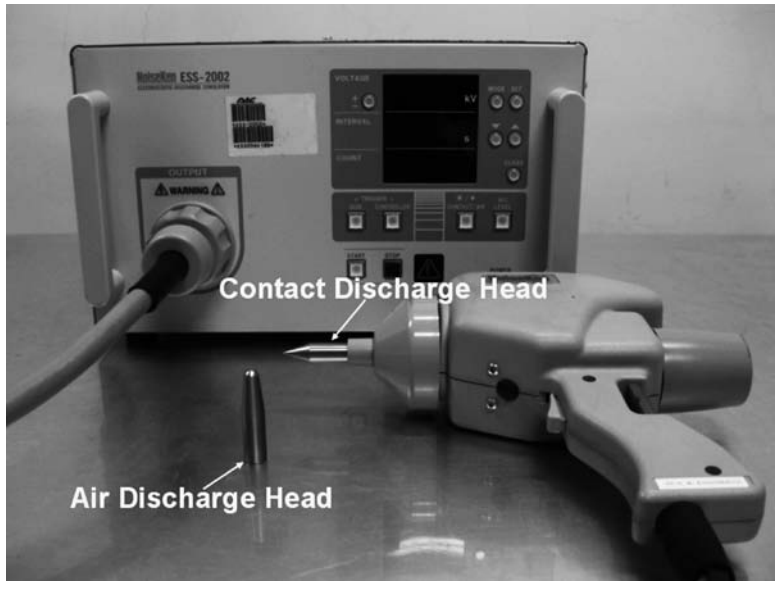


Figure 1.16 An illustration of the discharge tips.

1.4 TLU Standard Practice

Due to the increasing significance of TLU in the ICs industry, the standard practice, *ANSI/ESD SP5.4-2004* [26], to evaluate the robustness of CMOS ICs against TLU has been recently established by the *Electrostatic Discharge Association*. The test setup for TLU is shown in Figure 1.19. The DC voltage power supply is used for powering the DUT. The pulse generator is used as the transient signal source to generate the rectangular pulse. Both the DC supply voltage and the transient rectangular pulse are

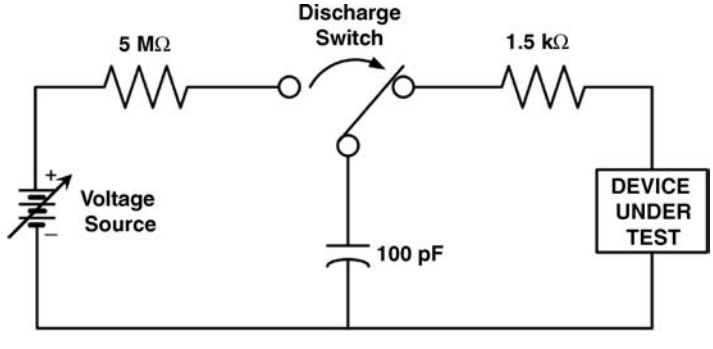


Figure 1.17 Equivalent circuit of the human body model (HBM) in the component-level ESD test. The charging capacitor (discharge resistor) is a smaller (larger) value of 100 pF (1.5 kΩ).

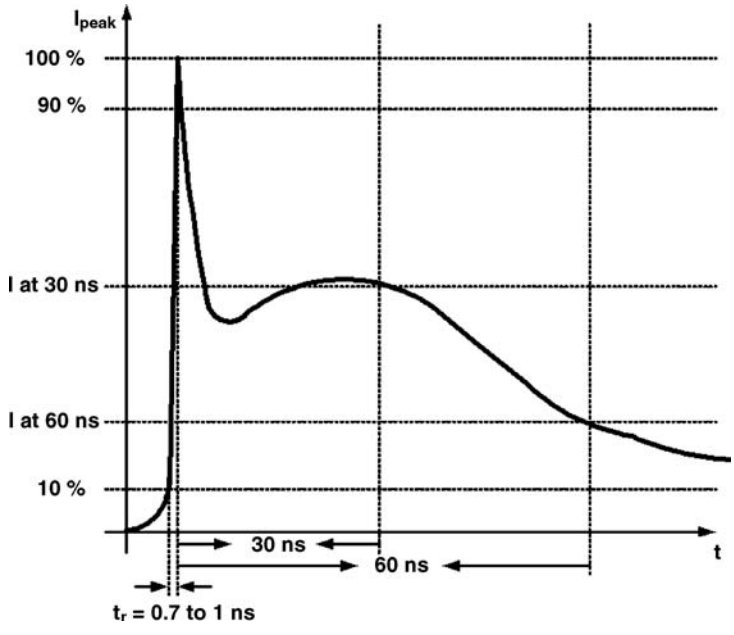


Figure 1.18 Typical waveform of the output current of an ESD gun.

Table 1.1 Preferential range of test levels specified in the test standard.

Contact discharge		Air discharge	
Level	Test voltage (kV)	Level	Test voltage (kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X[a]	Special	X[a]	Special

[a] "X" is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be needed.

Table 1.2 Failure criteria of the test results specified in the test standard.

Criterion	Performance	Result
Level A	EUT is unaffected by ESD stress	Pass
Level B	EUT works abnormally during ESD stress, but it can reset automatically	Pass
Level C	EUT works abnormally after ESD stress, but it needs to be reset manually	Fail
Level D	Hardware failure	Fail

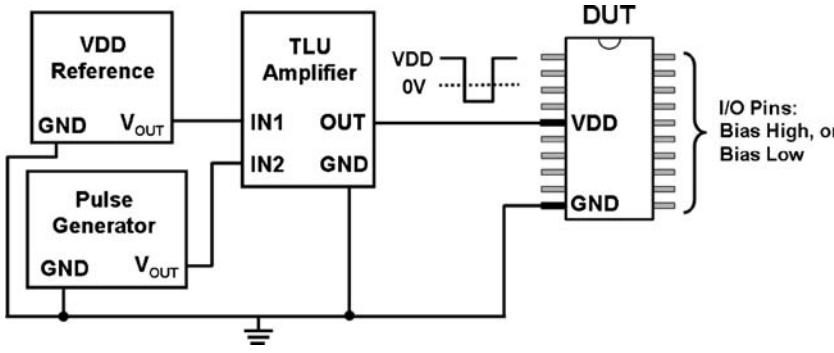


Figure 1.19 Test setup for TLU according to the standard practice, *ANSI/ESD SP5.4-2004* [26].

applied directly to the TLU amplifier inputs. The TLU amplifier acts as the main power supply for the DUT and has the integral adjustable current limit. It can be described as a signal amplifier with low output impedance, which is capable of superimposing the DC supply voltage and the rectangular pulse from the pulse generator. The TLU amplifier will generate a negative-going rectangular voltage pulse with a DC VDD offset and a negative peak voltage. Such a negative-going rectangular voltage pulse is applied on the power (VDD) pins of CMOS ICs as a TLU-triggering source, as shown in Figure 1.20. During the test, the voltage waveform shows that the VDD voltage initially goes down from its normal operating voltage to the negative peak voltage, lasting a pulse-width-long time period, and subsequently returns to its initial

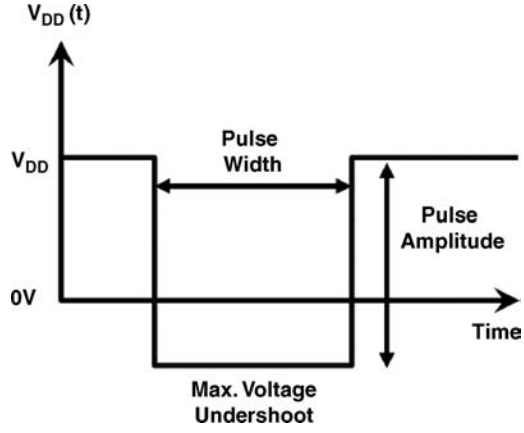


Figure 1.20 The TLU-triggering source used in standard practice to evaluate the TLU immunity of CMOS ICs: negative-going rectangular voltage pulse with a DC VDD offset and a negative peak voltage applied on the power pins of CMOS ICs.

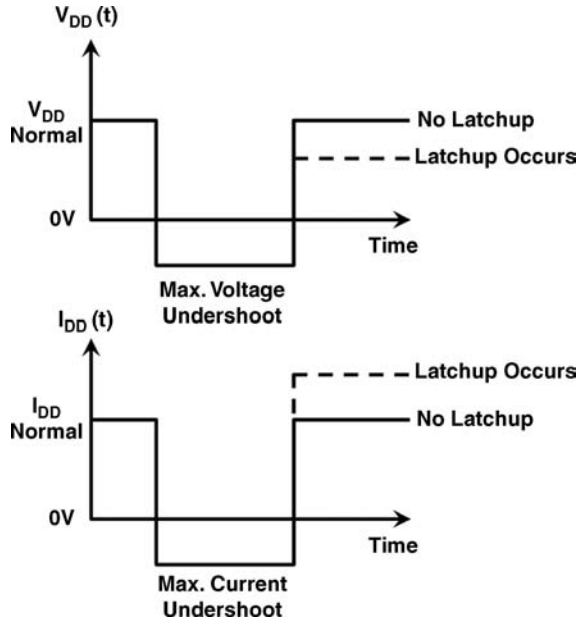


Figure 1.21 The typical waveforms which indicate if TLU occurs when using the standard practice TLU test.

voltage level. The typical waveforms to indicate if TLU occurs are shown in Figure 1.21. After applying the negative-going rectangular voltage pulse on the pin under test, if the VDD voltage is reduced and the IDD current increases, TLU occurs and the DUT fails. Otherwise, if both the VDD voltage and IDD current return to their initial levels, TLU does not occur and the DUT passes. Obviously, such a TLU-triggering source is used to simulate the transient undershoots on the power pins of CMOS ICs, which is different from all of the above TLU-triggering modes. Thus, it implies that TLU would be more susceptible to transient power-pin undershoots.

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2

Physical Mechanism of TLU under the System-Level ESD Test[1]

This chapter focuses on the clarification of the TLU physical mechanism in CMOS ICs in the system-level ESD test. An underdamped sinusoidal voltage stimulus is clarified as the realistic TLU-triggering stimulus in the system-level ESD test. With TLU characterization by device simulation and experimental verification in the time domain, the specific "sweep-back" current caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs is qualitatively proved to be the major cause of TLU. A simple 1-D analytical model of such a "sweep-back" current is also introduced. This model can qualitatively describe the sweep-back current dependency on the TLU-triggering stimulus.

2.1 Background

To ensure that electronic products offer a reliable performance in any environment and at any time, electronic products are always requested to meet the specifications of EMC regulations. Among the related EMC regulations, the system-level ESD test [1] is an essential test that is needed to evaluate the reliability of electronic equipment when subjected to system-level ESD events. However, because of the aggressive scaling of device feature sizes, as well as the clearance (spacing) between PMOS and NMOS devices, more and more ICs located within the equipment under test (EUT), unfortunately, are rather susceptible to TLU under a strictly demanded system-level ESD test [1]. Although latchup was once predicted to never have a reliability issue again in future nanoscale CMOS technologies, it has been proven that latchup issues still certainly exist, even though the power supply voltage is reduced with the scaling rules of CMOS ICs [2, 3].

[1] © 2005 IEEE. Reprinted, with permission, from Ming-Dou Ker and Sheng-Fu Hsu, Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test (sections II–VIII and all figures except figure 20), in *IEEE Transactions on Electron Devices*, Vol. 52, no. 8, pp. 1821–1831, Aug. 2005. IEEE, Piscataway, NJ.

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To investigate the physical mechanism of TLU in the system-level ESD test, the most significant part is to clarify the TLU-triggering stimulus at first. To clarify this issue, unlike all the TLU-triggering stimuli introduced in Chapter 1, an underdamped sinusoidal voltage stimulus, which can reflect the real situations of CMOS ICs within the EUT in the system-level ESD test [4–6], is adopted as the TLU-triggering stimulus for both TLU measurement and device simulation [7, 8]. With the clearly defined TLU-triggering stimulus, the physical mechanism of TLU in the system-level ESD test can be well explained in the time domain by device simulation and experimental verifications.

2.2 TLU in the System-Level ESD Test

To evaluate the performance of electrical/electronic equipment when subjected to ESD events, performing the system-level ESD test for electrical/electronic equipment is necessary. For example, a "notebook" under the system-level ESD test with a direct contact-discharge test mode is shown in Figure 2.1. An electrical/electronic product with CMOS ICs must sustain an ESD level of $\pm 8\,\text{kV}$ ($\pm 15\,\text{kV}$) under the contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4" in the system-level ESD test [1]. During such a system-level ESD test, electromagnetic interference (EMI) coming from the ESD will be coupled into the driver ICs of the liquid crystal display (LCD) panel. The inset figure in Figure 2.1 depicts the typically measured ESD-generated voltage waveforms on the power pins of CMOS ICs, which

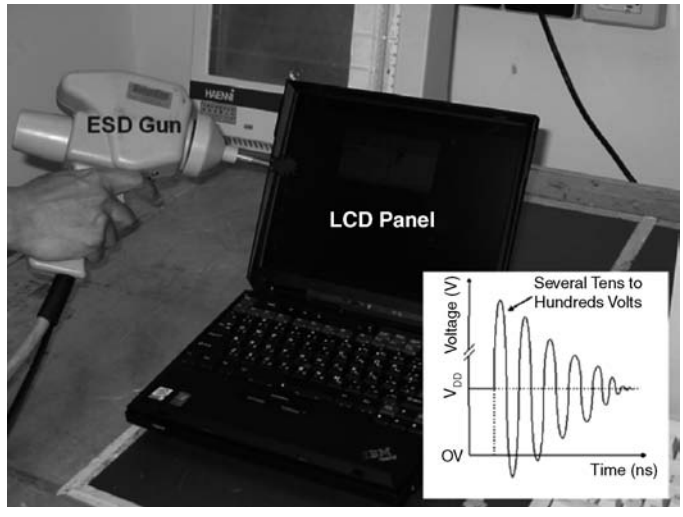


Figure 2.1 System-level ESD test on a notebook with the direct contact-discharge mode according to the IEC 61000-4-2 international standard [1]. The inset figure depicts the typically measured waveforms of transient noise voltage on the power pins of CMOS ICs, which locate within the EUT, in the system-level ESD test [4–6]. (Reprinted with permission from IEEE).

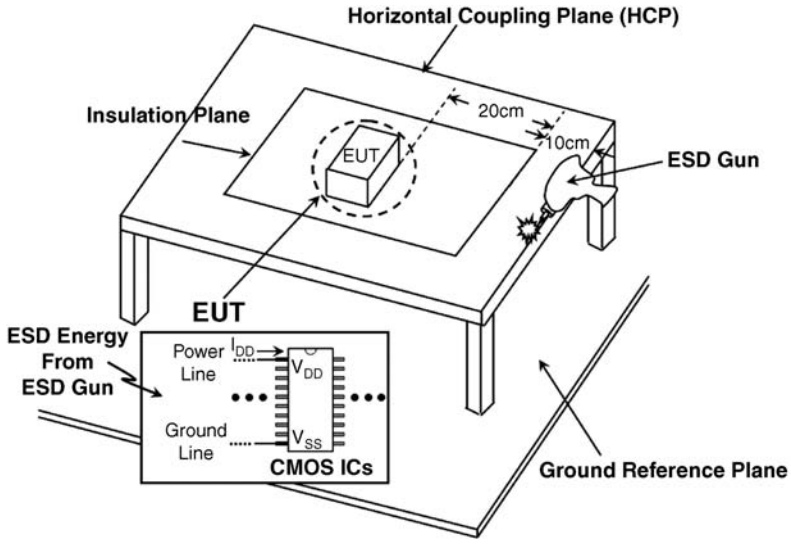


Figure 2.2 Measurement setup of the system-level ESD test with the indirect contact-discharge test mode [1]. The ESD gun discharging on the horizontal coupling plane (HCP) could cause TLU events on all the CMOS ICs inside the EUT. (Reprinted with permission from IEEE).

locate within the EUT, in the system-level ESD test [4–6]. This ESD-generated transient voltage is quite large (with amplitudes of several tens to hundreds volts) and fast (with period of several tens of nanoseconds), which can randomly exist on the power, ground, or I/O pins of the driver ICs to cause TLU failures.

To clarify this issue, the system-level ESD test for an indirect contact-discharge test mode is shown in Figure 2.2 [1]. When the ESD gun discharges to the horizontal coupling plane (HCP), the EMI coming from the ESD will be coupled into all CMOS ICs inside the EUT. With ESD voltages of $+1000$ V, the measured V_{DD} transient waveforms on one of the CMOS ICs (CMOS IC#A) inside the EUT are shown in Figure 2.3. The transient peak voltage on V_{DD} is as large as ± 50 V. Clearly, the V_{DD} with an initial DC voltage of $+2.5$ V will become an underdamped sine-wave-like voltage due to the disturbance of the ESD energy. Once the ESD voltage keeps increasing, TLU can be initiated and results in malfunction or damage of the CMOS IC inside the EUT. For example, with an ESD voltage of $+2000$ V, the measured V_{DD}, I_{DD}, and V_{OUT} transient waveforms on CMOS IC#A are shown in Figure 2.4. The transient peak voltage on V_{DD} is greater than ± 100 V, during such a system-level ESD test. TLU occurs with instantaneously increasing I_{DD}, so that V_{OUT} (100 MHz voltage clock) will fail to function correctly (pulled down to 0 V). Thus, it can be clarified that the underdamped sinusoidal voltage existing on the power (ground) lines of the CMOS ICs is the major cause for initiating TLU during the system-level ESD test.

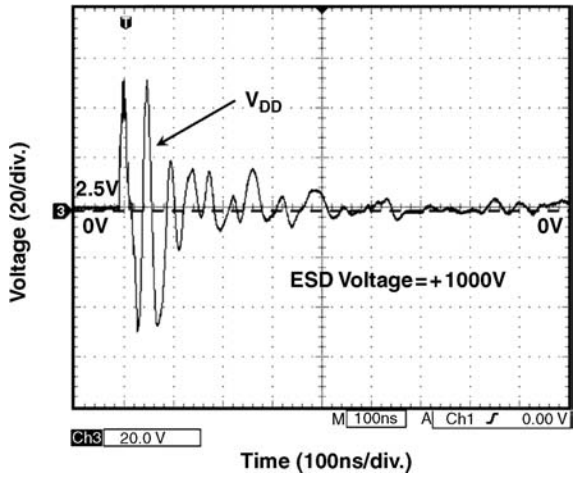


Figure 2.3 For an ESD gun with an ESD voltage of + 1000 V discharging on the HCP, the measured V_{DD} transient waveform on one of the CMOS ICs (CMOS IC#A) inside the EUT. (Reprinted with permission from IEEE).

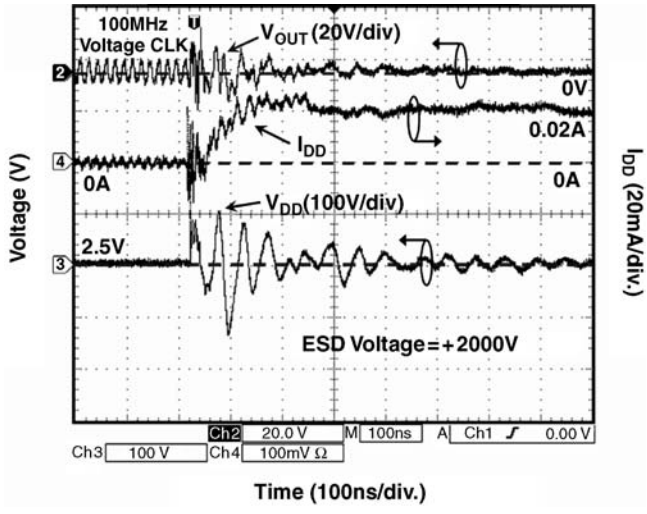


Figure 2.4 For an ESD gun with an ESD voltage of + 2000 V discharging on the HCP, the measured V_{DD}, I_{DD}, and V_{OUT} transient waveforms on CMOS IC#A inside the EUT. TLU occurs during the system-level ESD test. (Reprinted with permission from IEEE).

2.3 Test Structure

The silicon controlled rectifier (SCR) structure is used as the test structure for TLU measurements because the occurrence of latchup is due to the inherent SCR of two cross-coupled bipolar junction tansistors (BJT), parasitic vertical PNPs and lateral

NPN BJTs, in bulk CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are illustrated in Figure 2.5a and b, respectively. Geometrical parameters such as D, S, and W represent the distances between the well-edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively. In CMOS ICs, the P^+ anode (source of PMOS) and the N^+ well contact are connected to V_{DD}, whereas the N^+ cathode (source of NMOS) and the P^+ substrate contact are connected to ground. Once latchup occurs inside the SCR structure, a huge current will be generated through the mechanism of positive-feedback regeneration [9, 10]. As a result, a huge current will conduct through the low-impedance path from V_{DD} to ground, and further probably burn out the chip due to excess heat.

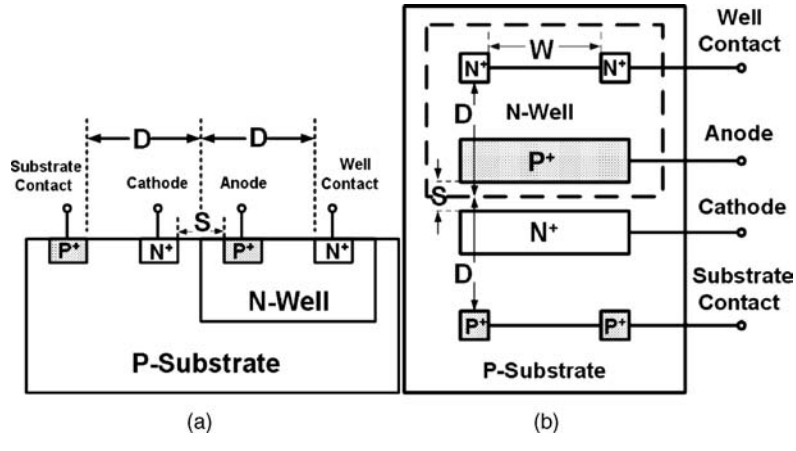


Figure 2.5 (a) Device cross-sectional view, and (b) layout top view, of the SCR structure for TLU measurements. Geometrical parameters such as D, S, and W represent the distances between the well-edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively. (Reprinted with permission from IEEE).

Different values of geometrical parameters such as D, S, and W in Figure 2.5a and b will certainly result in different TLU immunities of the SCR structures due to different latchup triggering (holding) voltages or currents. However, the TLU physical mechanism should be the same and not related to the variations of geometrical parameters. As a result, to qualitatively analyze the physical mechanism of TLU through TLU measurements, a specified SCR structure with layout parameters of $D = 6.7\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$ fabricated in 0.25-μm CMOS technology is used for all TLU measurements in this chapter. Because the parasitic SCR existing in the core circuitry of CMOS ICs is most sensitive to TLU due to compact integration, the minimum anode-to-cathode spacing ($S = 1.2\,\mu m$) according to foundries'design rules is used to consider the worst-case situation (most sensitive to TLU) encountered in the core circuitry of CMOS ICs.

To verify the relationship between the TLU measurement and device simulation, the specified SCR structure with the same geometrical parameters of $D = 6.7\,\mu m$ and $S = 1.2\,\mu m$ is used for all TLU device simulations in this chapter by the two-dimensional device simulation tool (MEDICI), as shown in Figure 2.6. With the specified two-dimensional SCR structure, the boundary condition can be well defined to perform the numerical analysis of electrical characteristics such as electric potential, electric field, carrier concentration, 2-D current flow line, and so on.

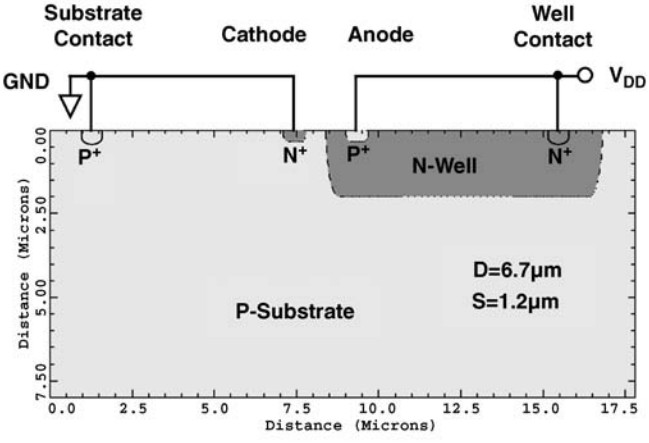


Figure 2.6 The SCR structure used in a two-dimensional device simulation tool (MEDICI). The specified SCR structure with geometrical parameters of $D = 6.7\,\mu m$ and $S = 1.2\,\mu m$ is used for all the TLU device simulations in this chapter. (Reprinted with permission from IEEE).

2.4 Measurement Setup

In the system-level ESD test, this can only judge whether the EUT passes the required criterion through its abnormal function (for example,the EUT shuts down). Nevertheless, it is hard to directly evaluate the TLU immunity of a single IC inside the EUT. To solve this problem, a component-level TLU measurement setup with the following two advantages is used. First, it can easily evaluate the TLU immunity of a single IC by the related measured voltage/current waveforms via an oscilloscope. Second, with the ability of generating an underdamped sinusoidal voltage, it can accurately simulate how an IC inside the EUT will be disturbed by the ESD-generated noise in the system-level ESD test. Figure 2.7 depicts such a component-level TLU measurement setup [11, 12]. The SCR structure shown in Figure 2.5 is used as the device under test (DUT) where the P^+ anode and the N^+ well contact are connected together to the V_{DD}, but the

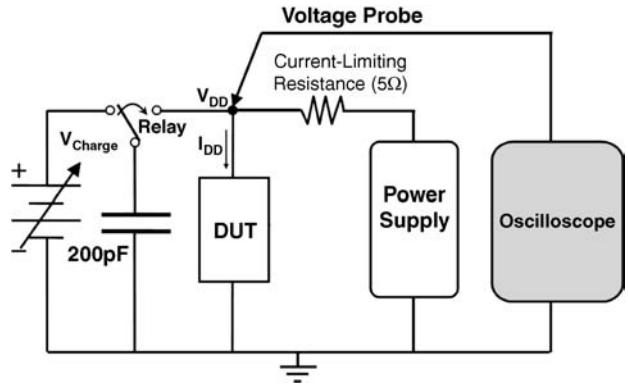
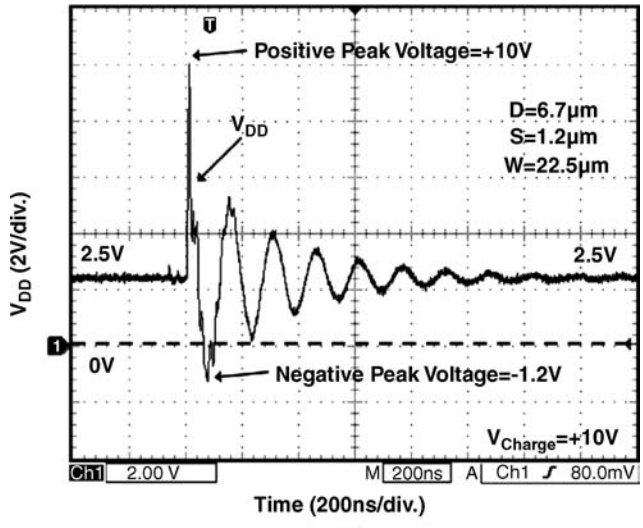
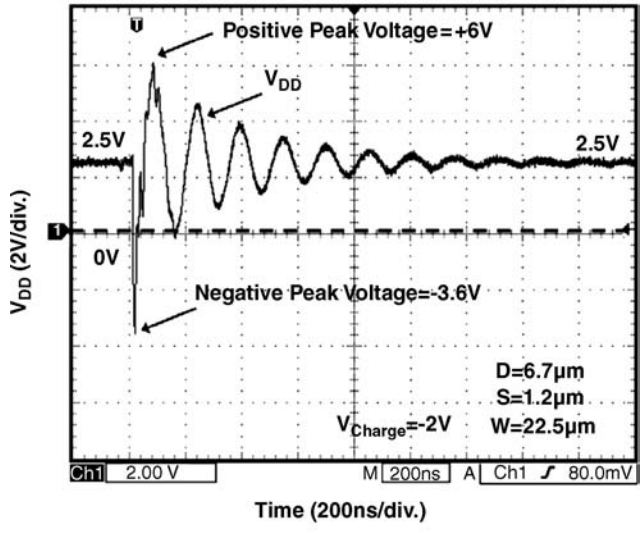


Figure 2.7 A component-level TLU measurement setup [11, 12]. This can accurately simulate how an IC inside the EUT will be disturbed by the ESD-generated noise in the system-level ESD test. (Reprinted with permission from IEEE).

N^+ cathode and the P^+ substrate contacts are connected to ground. An electrostatic-discharge simulator is used as the TLU-triggering source, V_{Charge}, to produce an underdamped sinusoidal voltage stimulus. Through applying a positive (negative) V_{Charge}, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated just as that in the system-level ESD test for an ESD gun with positive (negative) voltage [4]. For example, with a V_{Charge} of $+10$ V (-2 V), Figure 2.8a and b show the measured V_{DD} waveform across the SCR structure. Clearly, the intended underdamped sinusoidal voltage can be produced to simulate the transient voltage on the power pins of CMOS ICs in the system-level ESD test, no matter which polarity (positive or negative) the ESD voltage is. Because a large discharge resistance will result in a large damping factor of the intended underdamped sinusoidal voltage [11], there is no discharge resistance (0 Ω) between the relay and the V_{DD} node, as shown in Figure 2.7. As a result, the intended underdamped sinusoidal voltage can be produced, but not the unwanted overdamped voltage waveform due to a large discharge resistance [11]. In addition, a charged capacitance of 200 pF is used to store charges offered by the TLU-triggering source, V_{Charge}, and then these stored charges are discharged to the DUT through the relay. Because the charged capacitance will affect the damping frequency of the underdamped sinusoidal voltage, it should be properly selected to achieve a reasonable damping frequency as that in the system-level ESD test. For example, the damping frequency ($\sim$10 MHz) observed in Figures 2.8a and b is slightly smaller than that in the system-level ESD test ($\sim$20 MHz) [4], therefore indicating that this measurement setup is reasonable for TLU characterization. Moreover, a small current-limiting resistance (5 Ω) is recommended to protect the DUT from electrical-over-stress (EOS) damage during a high-current (low-impedance) latchup state.



(a)



(b)

Figure 2.8 Measured V_{DD} waveform for the SCR structure with a V_{Charge} of (a) $+10$ V, and (b) -2 V. Clearly, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated just as that in the system-level ESD test for an ESD gun with a positive (negative) voltage [4]. (Reprinted with permission from IEEE).

2.5 Device Simulation

A two-dimensional device simulation tool (MEDICI) is used to investigate the physical mechanism of TLU in the time domain under the system-level ESD test.

In this two-dimensional device simulation tool, a specific time-dependent voltage source given by:

$$V_{DD}(t) = V_0 + V_P \exp(-(t - t_d)D_{Factor})\sin(2\pi D_{Freq}(t - t_d)) \quad (2.1)$$

is used to apply an underdamped sinusoidal voltage on V_{DD} of the already defined SCR structure in Figure 2.6. With the proper parameters such as the initial voltage V_0, applied voltage amplitude V_P, damping factor D_{Factor}, damping frequency D_{Freq}, and time delay t_d, the intended underdamped sinusoidal voltage can be constructed. The relations between all these parameters and the underdamped sinusoidal voltage are shown in Figure 2.9. In this figure, V_0 represents the normal circuit operating voltage of CMOS ICs; the D_{Factor} determines how fast the voltage amplitude will be attenuated with time, where a voltage with a larger D_{Factor} can decay faster with time; D_{Freq} is the inverse of voltage duration and V_P is the peak voltage amplitude for a $D_{Factor} = 0$. For $V_P > 0$ ($V_P < 0$), V_{DD} is a positive-going (negative-going) underdamped sinusoidal voltage while t_d is only the time delay after which the voltage begins to go up or go down from $V = V_0$, and is not correlated with the TLU characterizations. In the following TLU simulation with a positive or negative V_{Charge}, the same parameters such as $V_0 = 2.5\,V$, $D_{Factor} = 2 \times 10^7\,s^{-1}$, $D_{Freq} = 20MHz$, and $t_d = 50\,ns$ are used in both positive and negative V_{Charge}, whereas the only difference is $V_P = +14.6\,V$ for a positive V_{Charge}, but $-14.6\,V$ for a negative V_{Charge}. In addition, the specified SCR structure with geometrical parameters of $D = 6.7\,\mu m$ and $S = 1.2\,\mu m$ is used for all TLU device simulations in this chapter.

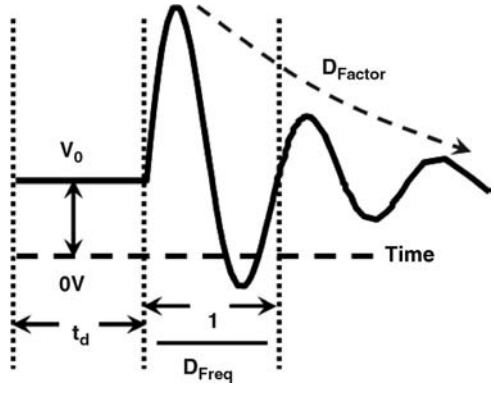


Figure 2.9 In device simulation, the underdamped sinusoidal voltage dependency on its constituting parameters: initial voltage V_0, applied voltage amplitude V_P, damping factor D_{Factor}, damping frequency D_{Freq}, and time delay t_d.

2.5.1 Latchup DC I–V Characteristics

The simulated latchup DC *I–V* characteristic of the specified SCR structure is shown in Figure 2.10. Once latchup occurs in the SCR structure, a low-impedance path will exist from V_{DD} to ground, resulting in a huge current conducting through this low-impedance path. The inset figure in Figure 2.10 shows that the DC latchup triggering voltage (current), V_{Trig} (I_{Trig}), is about 15.5 V (0.24 mA), while the DC latchup holding voltage (current), V_{Hold} (I_{Hold}), is about 1.25 V (0.5 mA). Clearly, under a latchup state, when the power supply voltage, V_{DD}, keeps at its normal circuit operating voltage ($+2.5$ V), the total power supply current, I_{DD}, flowing into both the anode and well contact is about 150 mA. This will offer vital evidence to verify whether TLU certainly occurs in the time domain through device simulation.

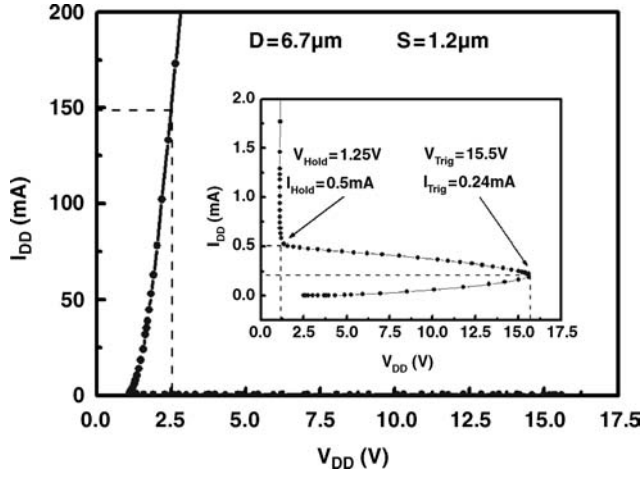


Figure 2.10 Simulated latchup DC *I–V* characteristic for the SCR structure. Under a latchup state, the fact that I_{DD} is about 150 mA when V_{DD} retains its normal operating voltage ($+2.5$ V) will offer vital evidence to prove whether TLU certainly occurs in the time domain through device simulation. (Reprinted with permission from IEEE).

2.5.2 Negative V_{Charge}

With a negative V_{Charge}, the simulated V_{DD} and I_{DD} transient responses on the SCR structure are shown in Figure 2.11. This can be divided into several parts for detailed discussions in the time domain. First, during the period of $0\,\text{ns} \leq t < 50\,\text{ns}$, the SCR operates in the blocking condition and V_{DD} is fixed at its normal operating voltage, $+2.5$ V. Within this duration, the N-well/P-substrate junction is at a normal reverse-biased state, and I_{DD} only comes from the negligible leakage current in the reverse junction. Second, during the period of $50\,\text{ns} \leq t \leq 62.5\,\text{ns}$, V_{DD} begins to

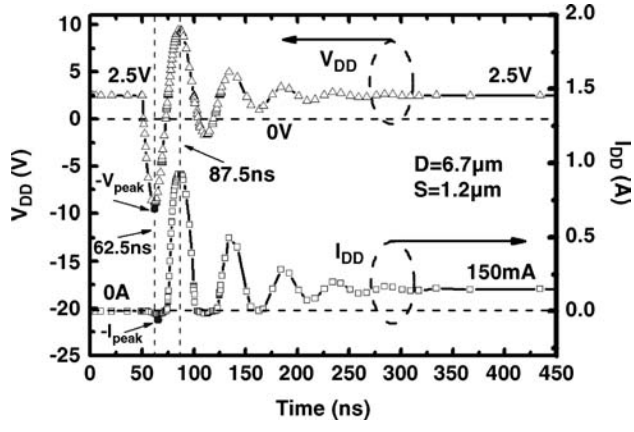


Figure 2.11 Simulated V_{DD} and I_{DD} transient responses for TLU with a negative V_{Charge}. During the period of 62.5 ns $\leq t \leq$ 87.5 ns, the "sweep-back" current, I_{Sb}, will be produced to initiate TLU (I_{DD} significantly increases) when V_{DD} increase from its negative peak voltage to the normal operating voltage of + 2.5 V. (Reprinted with permission from IEEE).

decrease rapidly from + 2.5 V at $t = 50$ ns, and will eventually reach the negative peak voltage, $-V_{peak}$ (−8 V), at $t = 62.5$ ns. Within this duration, the N-well/P-substrate junction gradually becomes slightly reverse biased when V_{DD} decreases from + 2.5 V to 0 V, and even becomes forward biased when V_{DD} drops below 0 V. Thus, at $t = 62.5$ ns, the largest forward-biased N-well/P-substrate junction can generate the forward peak current, $-I_{peak}$ (∼20 mA). Third, during the period of 62.5 ns $< t \leq$ 75 ns, when V_{DD} increases from $-V_{peak}$ to its normal operating voltage, + 2.5 V, the N-well/P-substrate junction will rapidly change from the forward-biased state to its original reverse-biased state. Meanwhile, inside the N-well (P-substrate) region, a large number of stored minority holes (electrons) offered by the forward peak current at $t = 62.5$ ns, will be instantaneously "swept-back" to the P-substrate (N-well) region where they originally come from. Thus, such a "sweep-back" current, I_{Sb}, will produce a localized voltage drop while flowing through the parasitic P-substrate or N-well resistance. Once this localized voltage drop approaches some critical value, the emitter-base junction of either a vertical PNP or lateral NPN BJT in the SCR structure will be forward biased to further trigger on latchup. This can be further illustrated by the simulated transient responses of both anode and well contact currents, as shown in Figure 2.12. This clearly proves where these stored minority carriers, Q_{Stored}, come from and when they will be "swept-back" to cause TLU. For example, the gradually enhanced forward-biased N-well/P-substrate junction will lead to gradually increasing well contact current during the period of 50 ns $\leq t \leq$ 62.5 ns. Meanwhile, the anode current is the negligible junction-leakage current due to an almost zero bias across the P^+-anode/N-well junction. Afterwards, during the period of 62.5 ns $< t \leq$ 75 ns,

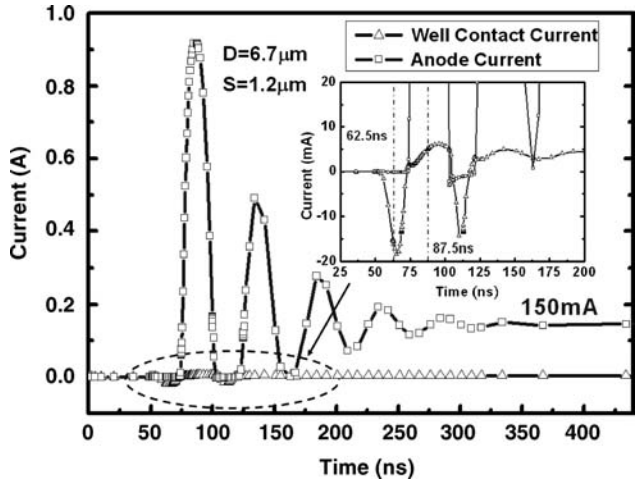


Figure 2.12 Simulated transient responses of both anode current and well contact current for TLU with a negative V_{Charge}. During the period of $62.5\,\text{ns} \leq t \leq 87.5\,\text{ns}$, latchup will be triggered on by I_{Sb}. Meanwhile, a huge anode current will conduct through the PNPN latchup path of the SCR structure. (Reprinted with permission from IEEE).

the forward well contact current will gradually decrease when V_{DD} increases from $-V_{\text{peak}}$ to $+2.5\,\text{V}$, indicating that the stored minority electrons (holes) are swept-back to the N-well (P-substrate) region where they originally come from. As a result, once the V_{DD} returns to, and even above, $+2.5\,\text{V}$ ($75\,\text{ns} < t \leq 87.5\,\text{ns}$), latchup will be triggered on and a huge anode current will conduct through the PNPN latchup path of the SCR structure. Meanwhile, the well contact current, however, is much smaller than the anode current because the well contact current is only the small base current of the parasitic vertical PNP BJT in the SCR structure.

In real CMOS ICs, when a low-impedance latchup state appears, V_{DD} may be pulled down to about the DC latchup holding voltage. This phenomenon is caused by two reasons. One is the finite current-supply ability of the system power supply, and the other is the inevitable parasitic series resistance existing between the V_{DD} node and the system power supply. In device simulation, however, when TLU occurs during the period of $75\,\text{ns} < t \leq 100\,\text{ns}$ shown in Figures 2.11 and 2.12, V_{DD} was not immediately pulled down to the DC latchup holding voltage. Instead, V_{DD} keeps at the given underdamped sinusoidal voltage. This fact results from the native limitation of the device simulation tool for transient analysis in the time domain. However, TLU is sure to occur because a huge I_{DD} (150 mA, refer to Figures 2.11 and 2.12) can be found when V_{DD} finally returns to its normal operating voltage, $+2.5\,\text{V}$. More importantly, it is consistent with the simulated latchup DC I–V characteristics that I_{DD} is 150 mA when V_{DD} keeps at its normal operating voltage, $+2.5\,\text{V}$, under a latchup state in Figure 2.10.

To further judge whether TLU indeed occurs, Figure 2.13 shows the corresponding simulated two-dimensional current flow lines with respect to various transient timing points with a negative V_{Charge}. Clearly, a large forward well (substrate) contact current appears when the N-well/P-substrate junction is forward-biased (timing points A, B, and F). Once the N-well/P-substrate junction quickly changes from the forward-biased state to its original reverse-biased state, TLU will be triggered due to a large enough I_{Sb} (timing points C–E, G, and H).

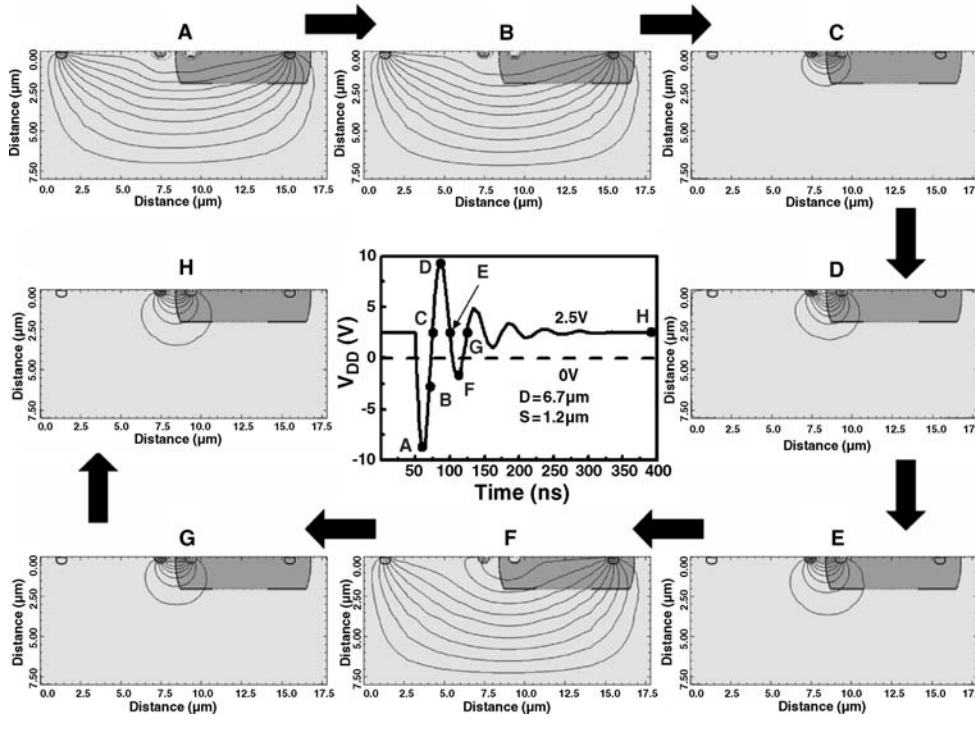


Figure 2.13 Simulated 2-D current flow lines with respect to various transient timing points for TLU with a negative V_{Charge}. A forward well (substrate) contact current appears when the N-well/P-substrate junction is forward-biased (timing points A, B, and F), and TLU will be triggered on due to a large enough I_{Sb} (timing points C–E, G, and H). (Reprinted with permission from IEEE).

2.5.3 Positive V_{Charge}

With a positive V_{Charge}, Figure 2.14 shows the simulated V_{DD} and I_{DD} transient responses on the SCR structure. During the period of $50\,ns \leq t \leq 62.5\,ns$, unlike the V_{DD} waveform with a negative V_{Charge} shown in Figure 2.11 where V_{DD} begins

decreasing rapidly at $t = 50$ ns, V_{DD} starts to increase at $t = 50$ ns and eventually reaches a positive peak voltage at $t = 62.5$ ns. Within this duration, the N-well/P-substrate junction is always reverse biased, and thus only a transient displacement current caused by the N-well/P-substrate junction can be found within the SCR. Such a displacement current will not cause TLU unless the frequency (amplitude) of the V_{DD} is large enough to induce a large enough displacement current [13, 14]. Afterwards, V_{DD} decreases from its positive peak voltage, at $t = 62.5$ ns, to its negative peak voltage, at $t = 87.5$ ns. Within this duration, the N-well/P-substrate junction gradually changes from the reverse-biased state to the forward-biased state, while more and more minority electrons (holes) are injected into the P-substrate (N-well) region. Once these Q_{Stored} are subsequently (87.5 ns $\leq t \leq$ 100 ns) swept back to the N-well (P-substrate) regions where they originally come from, TLU will be triggered on. As a result, I_{DD} will considerably increase during the period of 100 ns $\leq t \leq$ 112.5 ns. Obviously, TLU is sure to occur because the huge I_{DD} (150 mA, refer to Figures 2.10 and 2.14) can be found when V_{DD} eventually returns to its normal operating voltage of $+2.5$ V.

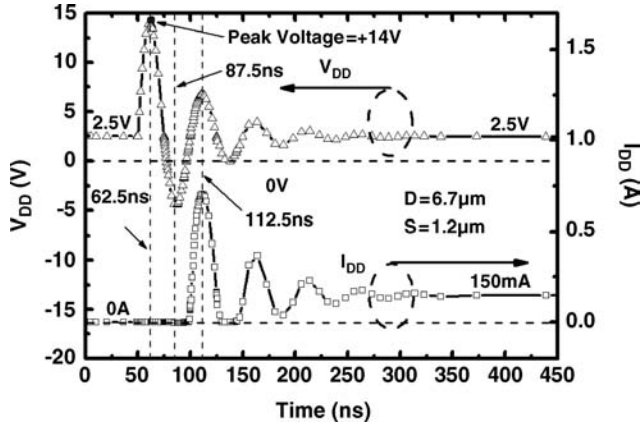


Figure 2.14 Simulated V_{DD} and I_{DD} transient responses for TLU with a positive V_{Charge}. During the period of 50 ns $\leq t \leq$ 75 ns, TLU will not be triggered on by the N-well/P-substrate junction displacement current. Afterwards, during the period of 87.5 ns $\leq t \leq$ 112.5 ns, I_{Sb} will be produced to initiate TLU (I_{DD} significantly increases) when V_{DD} increase from its negative peak voltage to the normal operating voltage, $+2.5$ V. (Reprinted with permission from IEEE).

Figure 2.15 shows the simulated two-dimensional current flow lines with respect to various transient timing points with a positive V_{Charge}. The N-well/P-substrate junction displacement current will not cause TLU (timing points A and B). However, a large forward well (substrate) contact current will appear when the N-well/P-substrate junction is forward-biased (timing points C and D), and then TLU will certainly be triggered on if I_{Sb} is large enough (timing points E–H).

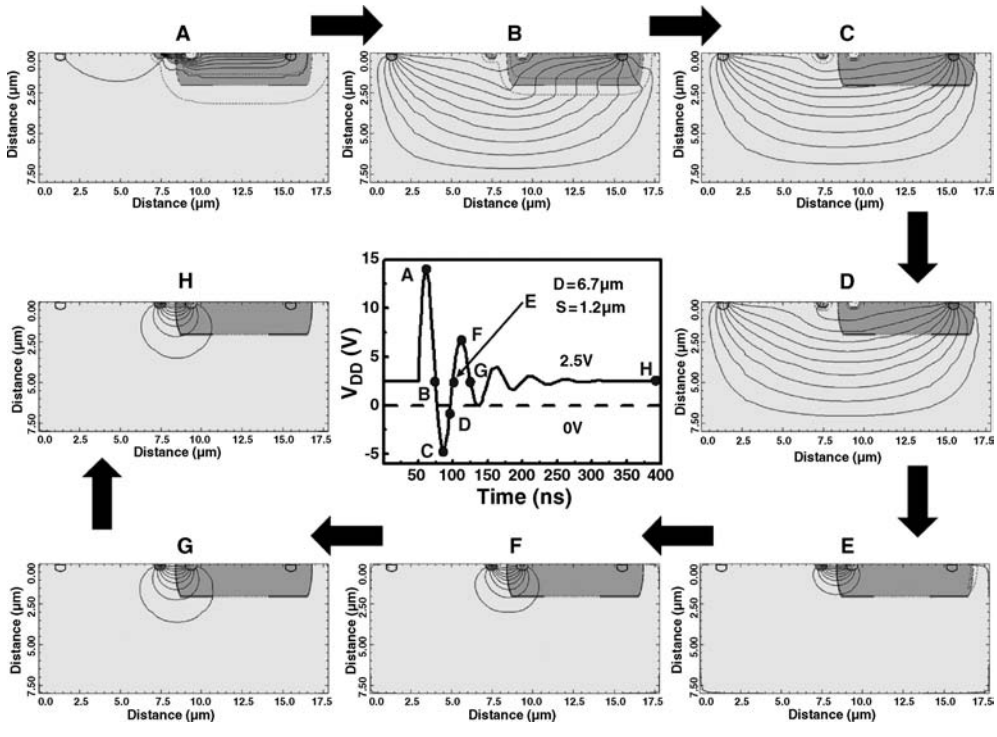


Figure 2.15 Simulated 2-D current flow lines with respect to various transient timing points for TLU with a positive V_{Charge}. The N-well/P-substrate junction displacement current will not cause TLU (timing points A and B) until a large enough I_{Sb} is produced (timing points E–H). (Reprinted with permission from IEEE).

2.5.4 A More Realistic Case

In real situations under the system-level ESD test, the oscillatory resonance voltage can randomly occur at both the V_{DD} and *GND* nodes [4–6], but not only at the V_{DD} node. With consideration of such a realistic situation, Figure 2.16 shows the simulated V_{DD}, *GND*, and I_{DD} transient responses on the SCR structure. Obviously, once the V_{DD}-to-*GND* voltage is negative enough (87.5 ns $\leq t \leq$ 100 ns) to produce a large enough I_{Sb} within the N-well/P-substrate junction, TLU can be easily triggered on afterwards when the V_{DD}-to-*GND* voltage returns to a positive voltage (100 ns $\leq t \leq$ 112.5 ns). Because the power and ground lines are widely distributed over the whole circuitry in a chip, such oscillatory resonance voltage can appear on some core circuitry. This fact implies that TLU can occur within the core circuitry, but not only in I/O circuitry. Thus, unlike the quasi-static latchup issue [15] which primarily concerns latchup immunity on I/O circuitry, latchup prevention skills such as layout optimization with additional guard rings [16], other specific advanced process technologies, or even latchup self-stop circuits [17] may be necessary for the core circuitry to prevent TLU in CMOS ICs.

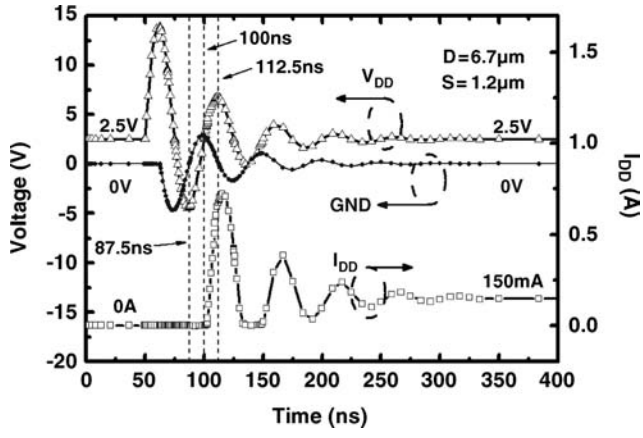


Figure 2.16 Simulated V_{DD}, *GND*, and I_{DD} transient responses for TLU under a more realistic situation. V_{DD} and *GND* can be disturbed simultaneously by EMI in a system-level ESD test [4–6]. Once the V_{DD}-to-*GND* voltage is negative enough (87.5 ns $\leq t \leq$ 100 ns) to produce a large enough I_{Sb}, afterwards TLU could be easily triggered on when the V_{DD}-to-*GND* voltage returns to a positive voltage (100 ns $\leq t \leq$ 112.5 ns). (Reprinted with permission from IEEE).

2.6 TLU Measurement

The component-level TLU measurement setup shown in Figure 2.7 is used to perform the TLU test. With both a positive and negative V_{Charge}, the measured V_{DD} (I_{DD}) transient response will be recorded through the voltage (current) probe to display on the oscilloscope. This will clearly indicate whether TLU occurs (I_{DD} significantly increases) when the absolute value of positive or negative V_{Charge} gradually increases from 0 V during the TLU test. More importantly, this will provide useful information for the comparison between the TLU measurement and the device simulation. In addition, the specified SCR structure with layout parameters of $D = 6.7\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$ fabricated in 0.25-μm CMOS technology is used for all the TLU measurements in this chapter.

2.6.1 Latchup DC I–V Characteristics

The measured latchup DC *I–V* characteristic for the fabricated SCR structure is shown in Figure 2.17. The inset figure in this figure indicates the DC latchup trigger voltage (current), V_{Trig} (I_{Trig}), is about 19.5 V (2 mA), while the DC latchup holding voltage (holding current), V_{Hold} (I_{Hold}), is about 1 V (9.5 mA). Through comparing these measured DC latchup parameters with the simulated ones in Figure 2.10, there is no large difference between the measured and the simulated DC latchup parameters. Thus, this non-calibrated device simulation tool is capable of performing reasonable qualitative analysis for TLU.

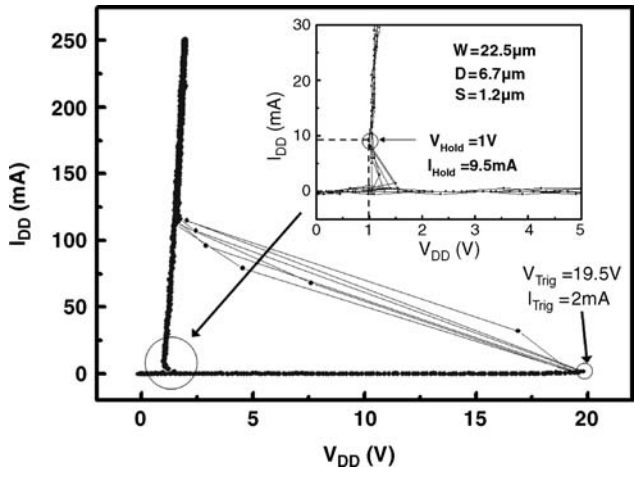


Figure 2.17 Measured latchup DC *I–V* characteristic for an SCR structure. (Reprinted with permission from IEEE).

2.6.2 Negative V_{Charge}

With a negative V_{Charge} of -5 V, the measured V_{DD} and I_{DD} transient waveforms on the SCR structure are shown in Figure 2.18. Obviously, the forward I_{DD} current appears due to the forward-biased N-well/P-substrate junction when V_{DD} initially decreases below 0 V. Afterwards, I_{DD} will greatly increase while V_{DD} returns to above 0 V, and therefore TLU does occur. As a result, both the V_{DD} and I_{DD} waveforms are slightly oscillatory under a low-impedance (high-current) latchup state. Finally, V_{DD} will eventually be pulled down to about the DC latchup holding voltage ($\sim$1 V) with a huge I_{DD} ($\sim$80 mA) after this transition.

Through comparisons between the experimental and the device simulation results in Figures 2.11 and 2.18, the experimental results are consistent with the device simulation results in the time domain. For example, TLU will be triggered due to a large enough I_{Sb} while V_{DD} increases from $-V_{\text{Peak}}$ to its normal operating voltage of $+2.5$ V. This can once again verify that the large number of the total stored minority carriers contributing to Q_{Stored} can trigger on TLU while they are quickly swept back to the regions where they originally come from.

2.6.3 Positive V_{Charge}

With a positive V_{Charge} of $+20$ V, the measured V_{DD} and I_{DD} transient waveforms on the SCR structure are shown in Figure 2.19. V_{DD} begins to increase rapidly from the normal operating voltage ($+2.5$ V) to a positive peak voltage of $+17$ V. Meanwhile, the N-well/P-substrate junction is reversed biased, and thus only the transient displacement current caused by the N-well/P-substrate junction can be found within the SCR. Such a junction displacement current is too small to initiate TLU because I_{DD}

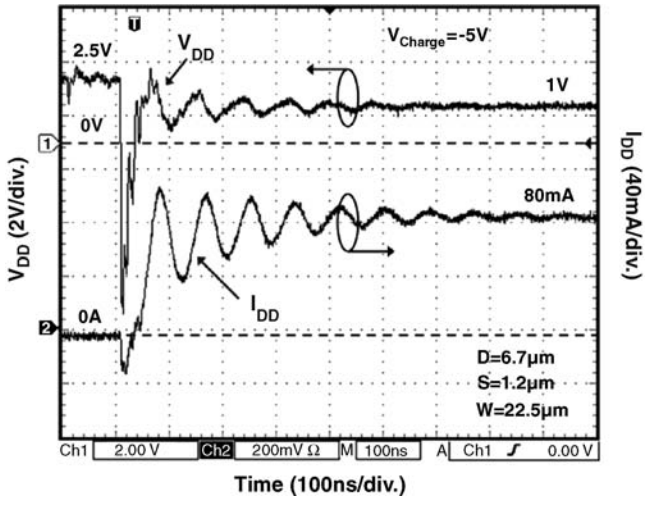


Figure 2.18 Measured V_{DD} and I_{DD} transient waveforms from the TLU test with a negative V_{Charge} of -5 V. This is consistent with the device simulation results in Figure 2.11 that TLU will be triggered on (I_{DD} significantly increases) when V_{DD} increase from its negative peak voltage to the normal operating voltage, $+2.5$ V. (Reprinted with permission from IEEE).

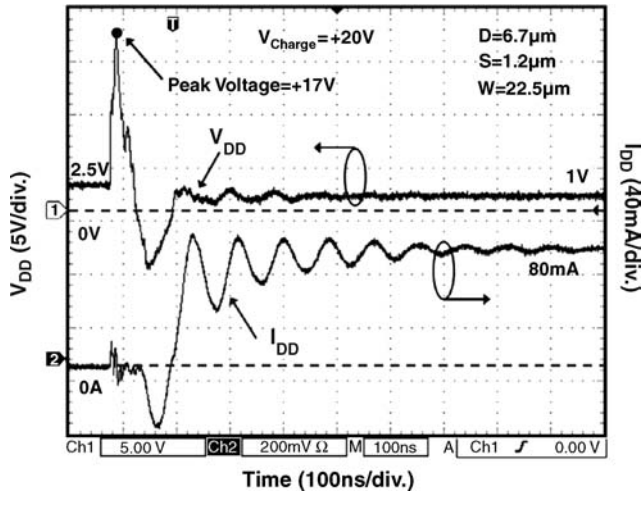


Figure 2.19 Measured V_{DD} and I_{DD} transient waveforms from the TLU test with a positive V_{Charge} of $+20$ V. This is consistent with the device simulation results in Figure 2.14 that TLU will not be initially ($V_{DD} > 0$ V) triggered on by the N-well/P-substrate junction displacement current until a large enough I_{Sb} is produced when V_{DD} increases from its negative peak voltage to the normal operating voltage, $+2.5$ V. (Reprinted with permission from IEEE).

doesn't significantly increase when V_{DD} increases from the normal operating voltage (+ 2.5 V) to the positive peak voltage of + 17 V. Afterwards, once a large enough I_{Sb} is produced when V_{DD} increases from its negative peak voltage back to the normal operating voltage (+ 2.5 V), TLU will be initiated with the large increase in I_{DD}. Moreover, both V_{DD} and I_{DD} waveforms are slightly oscillatory under a low-impedance (high-current) latchup state. Finally, V_{DD} will eventually be pulled down to about the DC latchup holding voltage (~1 V) with a huge I_{DD} (~80 mA) after this transition.

The physical mechanism of TLU in the system-level ESD test can be well proved once again by comparing the experimental results with the device simulation. As shown in Figures 2.14 and 2.19, a large enough I_{Sb} caused by the instantaneously forward-biased N-well/P-substrate junction can trigger on the TLU more easily than the reverse junction displacement current does.

2.7 Discussion

It has been clarified that the sweep-back current, I_{Sb}, caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs is the major cause of TLU in the system-level ESD test. Based on a simple 1-D analytical model of I_{Sb} [7, 8], the dominant parameter to initiate TLU can be identified. In addition, the minimum magnitude of the applied voltage to initiate TLU under different damping frequencies can be determined by the device simulations. By combining these 2-D device simulation results and the 1-D model of I_{Sb}, the minimum I_{Sb} or the minimum number of the total stored minority carriers contributing to Q_{Stored} to initiate TLU can be also estimated. To further provide the evidence that I_{Sb} is the major cause of TLU, the transient responses on the minority carriers stored within SCR can be calculated.

2.7.1 Dominant Parameter to Induce TLU

As shown in the inset figure of Figure 2.20, with the assumption that the N-well/P-substrate junction is treated as an ideal 1-D diode with a step junction profile, a simple 1-D analytical model of the averaged I_{Sb} ($\equiv I_{Ave}$) [7, 8] can be expressed as follows:

$$I_{Ave} \equiv \frac{Q_{Stored}}{t_B - t_A} \tag{2.2}$$

where t_A (t_B) is the initial (final) timing point of a specific duration when I_{Sb} exists, as shown in Figure 2.20. Q_{Stored} represents the total charge of the stored minority carriers (holes) causing I_{Sb} ($t_A \le t \le t_B$) inside the N-well region, which is given by:

$$Q_{Stored} = q\frac{{n_i}^2}{N_D}L_P\left(1 - e^{-\frac{X_{n'} - X_n}{L_P}}\right)\left(e^{\frac{qV(t_A)}{kT}} - e^{\frac{qV(t_B)}{kT}}\right) \tag{2.3}$$

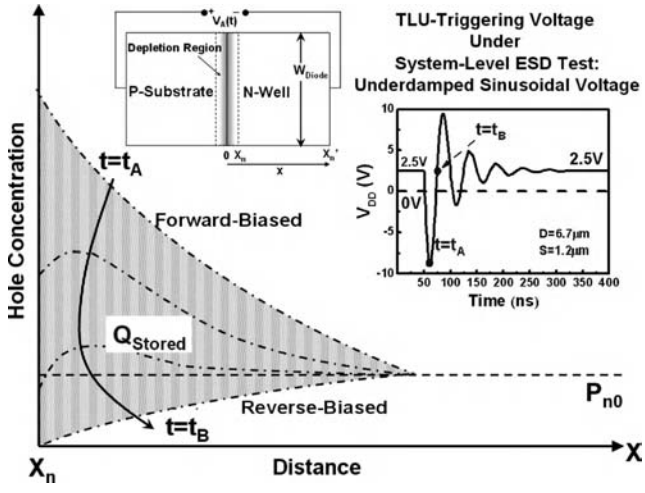


Figure 2.20 Total stored minority carriers, Q_{Stored}, causing I_{Sb} ($t_{\text{A}} \le t \le t_{\text{B}}$) inside the N-well region. The inset figure is an ideal 1-D diode used for deriving the 1-D analytical model of the averaged I_{Sb} ($\equiv I_{\text{Ave}}$) [7, 8]. (Reprinted with permission from IEEE).

From Equations (2.2) and (2.3), I_{Ave} can be further simplified as follows:

$$\begin{aligned} I_{\text{Ave}} \equiv \frac{Q_{\text{Stored}}}{t_{\text{B}} - t_{\text{A}}} &= \frac{Q_{\text{Stored}}}{(1/D_{\text{Freq}})/4} \\ &= 4D_{\text{Freq}} q \frac{{n_i}^2}{N_{\text{D}}} L_{\text{P}} \left(1 - \text{e}^{-\frac{X_{\text{n}}' - X_{\text{n}}}{L_{\text{P}}}}\right)\left(\text{e}^{\frac{qV(t_{\text{A}})}{kT}} - \text{e}^{\frac{qV(t_{\text{B}})}{kT}}\right) \\ &= Z\, D_{\text{Freq}}\, \text{e}^{\frac{qV(t_{\text{A}})}{kT}} \left(\because\ \text{e}^{\frac{qV(t_{\text{B}})}{kT}} = \text{e}^{\frac{V(t_{\text{B}})}{kT/q}} = \text{e}^{\frac{-2.5}{0.0259}} \cong 0\right) \end{aligned} \tag{2.4}$$

where:

$$Z = 4q \frac{{n_i}^2}{N_{\text{D}}} L_{\text{P}} \left(1 - \text{e}^{-\frac{X_{\text{n}}' - X_{\text{n}}}{L_{\text{P}}}}\right) \tag{2.5}$$

is a constant and independent on the damping frequency (D_{Freq}), applied voltage amplitude (V_{P}), and damping factor (D_{Factor}). By substituting $t_{\text{A}} = t_{\text{d}} + (1/D_{\text{Freq}})/4$ into Eqaution (2.1), $V(t_{\text{A}})$ can be expressed as follows:

$$\begin{aligned} V(t_{\text{A}}) &= V_0 + V_{\text{P}} \exp(-(t_{\text{A}} - t_{\text{d}}) D_{\text{Factor}}) \sin(2\pi D_{\text{Freq}}(t_{\text{A}} - t_{\text{d}})) \\ &= V_0 + V_{\text{P}} \exp\left(-\frac{D_{\text{Factor}}}{4D_{\text{Freq}}}\right) \end{aligned} \tag{2.6}$$

From Equations (2.4) and (2.6), it can be obviously identified that D_{Freq} is dominant on I_{Ave} (that is, dominant to induce TLU), because there is not only a proportional exponential relationship between D_{Freq} and $V(t_{\mathrm{A}})$ in Equation (2.6), but also a multiplication factor "D_{Freq}" on I_{Ave} in Equation (2.4).

2.7.2 Transient Responses on the Minority Carriers Stored within the SCR

To further provide the evidence that I_{Sb} is the major cause of TLU, the transient responses on the minority carriers stored within the SCR, $Q_{\mathrm{Stored}}(t)$, can be estimated from Equation (2.3) by using t to substitute for t_{A}. For the underdamped sinusoidal voltage with the same parameters (D_{Factor}, D_{Freq}, and V_{P} of $2 \times 10^7\,\mathrm{s}^{-1}$, 20 MHz, -14.6 V, respectively) as those in the case with the negative V_{Charge} of Figures 2.11 and 2.12, the calculated transient responses of Q_{Stored} (hole) in the N-well region are shown in Figure 2.21. Compared with the simulated TLU transient responses in Figures 2.11 and 2.12, the minority carriers (holes) stored in the N-well region significantly increase with a forward well contact current ($50\,\mathrm{ns} \le t \le 62.5\,\mathrm{ns}$) when V_{DD} decreases from 2.5 V to $-V_{\mathrm{peak}}$. Afterwards, Q_{Stored} decreases because these minority holes are swept back to their original P-substrate region ($62.5\,\mathrm{ns} \le t \le 75\,\mathrm{ns}$). As a result, TLU will be triggered on by these swept-back Q_{Stored}, and so the anode current will significantly increase ($75\,\mathrm{ns} \le t \le 87.5\,\mathrm{ns}$). From Figures 2.11, 2.12, and 2.21, the swept-back current I_{Sb} can be confirmed as the major cause of TLU during the system-level ESD stress.

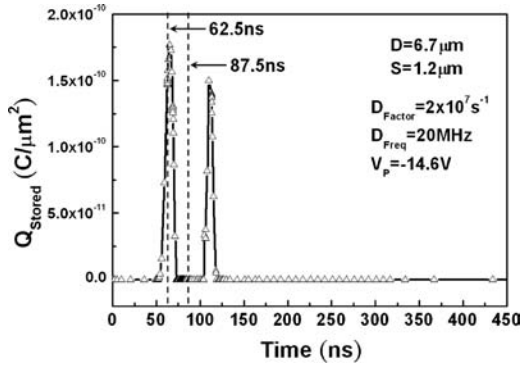


Figure 2.21 Calculated transient responses of Q_{Stored} (hole) in the N-well region. The underdamped sinusoidal voltage has the same parameters as those used in the negative V_{Charge} case of Figures 2.11 and 2.12 (D_{Factor}, D_{Freq}, and V_{P} of $2 \times 10^7\,\mathrm{s}^{-1}$, 20 MHz, and -14.6 V, respectively). (Reprinted with permission from IEEE).

2.8 Conclusion

The underdamped sinusoidal voltage stimulus has been clarified as the realistic TLU-triggering stimulus in the system-level ESD test. With the aid of device simulation, the specific "sweep-back" current caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs has been qualitatively proved to be the major cause of TLU. The behavior of the sweep-back current can be derived by a simple 1-D analytical model, which can qualitatively describe the sweep-back current dependency on the TLU-triggering stimulus. Through comparisons between device simulations and experimental measurements, the TLU reliability issue may still exist in a qualified CMOS IC product through a quasi-static latchup test. Thus, an efficient TLU measurement setup is needed to evaluate the TLU reliability of CMOS IC products. Because a TLU reliability issue potentially exists within the whole circuitry of CMOS ICs, latchup prevention skills such as layout optimization, specific advanced process technologies, or circuit techniques may be necessary to improve TLU immunity for core circuitry. Through both an understanding of the physical mechanism and the proposed simulation/verification methodology on TLU, the safe design/layout rules or circuit techniques in CMOS ICs can be developed against TLU events.

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3

Component-Level Measurement for TLU under System-Level ESD Considerations[1]

3.1 Background

During the system-level ESD test, the high-energy ESD-induced noises often cause TLU on CMOS ICs inside the electrical/electronic products, leading to shutdown or malfunction of the equipment under test (EUT). However, during the realistic system-level ESD test, it could be rather complicated or difficult to directly evaluate the TLU immunity of a "single" CMOS IC inside the EUT. To solve such a problem, a component-level TLU measurement setup with a bipolar trigger waveform [1–3] is utilized and introduced in this chapter. This measurement setup has the advantage of easily evaluating the TLU immunity of a single IC by monitoring the voltage/current waveforms through an oscilloscope. More importantly, with the ability of generating a bipolar trigger voltage, it can accurately simulate how a CMOS IC will be disturbed by the ESD-generated noises under the system-level ESD test.

Current-blocking diode and current-limiting resistance, which are generally suggested to be used in a TLU measurement setup with a bipolar trigger, are investigated for their impact on both the bipolar trigger waveforms and TLU immunity of the device under test (DUT). With the experimental results and verifications of device simulation, the TLU measurement setup without a current-blocking diode but with a small current-limiting resistance is suggested, which can accurately evaluate the TLU immunity of CMOS ICs with neither overestimation nor electrical-over-stress (EOS) damage to a

[1] © 2006 IEEE. 3.1–3.7 reprinted, with permission, from Ming-Dou Ker and Sheng-Fu Hsu, Component-level measurement for transient-induced latchup in CMOS ICs under system-level ESD considerations (sections II–VII, figures 5–19, and Table I), in *IEEE Transactions on Device and Materials Reliability*, Vol. 6, no. 3, pp. 461–472, Sep. 2006. IEEE, Piscataway, NJ.

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DUT during the TLU test. With the suggested TLU measurement setup, different types of board-level noise filter networks are evaluated to find their effectiveness for improving the TLU immunity of CMOS ICs.

3.2 Component-Level TLU Measurement Setup

The SCR structure is used as the test structure for TLU measurements because the occurrence of latchup results from the parasitic SCR in CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are illustrated in Figure 2.5a and b, respectively. The geometrical parameters such as D, S, and W represent the distances between the well-edge and well (substrate) contact, anode and cathode, and the adjacent contacts, respectively. In order to consider the layout dependences, the SCR structures with two sets of layout parameters ($D = 16.6\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$, as well as, $D = 16.6\,\mu m$, $S = 20\,\mu m$, and $W = 22.5\,\mu m$) are used in this chapter. All the SCR structures have been fabricated in a 0.25-μm salicided CMOS technology.

Several component-level measurement setups to evaluate TLU immunity of CMOS ICs have been developed [1–5]. In order to accurately simulate the ESD-induced noises on the power lines of CMOS ICs in the system-level ESD test, a component-level TLU measurement setup with a bipolar trigger voltage [1–3] is utilized in this chapter. The typical TLU measurement setup with a bipolar trigger is illustrated in Figure 3.1. The charging voltage, V_{Charge}, has two different polarities: positive ($V_{Charge} > 0$) and negative ($V_{Charge} < 0$). The positive (negative) V_{Charge} can generate the positive-going (negative-going) bipolar trigger noises on the power pins of the DUT. A capacitor with a capacitance of 200 pF used in the machine model (MM) [6] ESD test is employed as the charging capacitor. The SCR device shown in Figure 2.5 is used as the DUT where the P^+ anode (N^+ cathode) and the N^+ well (P^+ substrate)

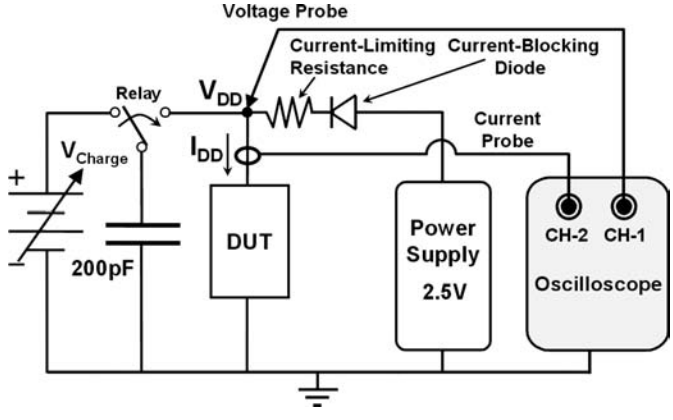


Figure 3.1 Component-level TLU measurement setup with a bipolar trigger [1–3]. This can accurately simulate how a CMOS IC will be disturbed by the ESD-generated noises in the system-level ESD test. (Reprinted with permission from IEEE).

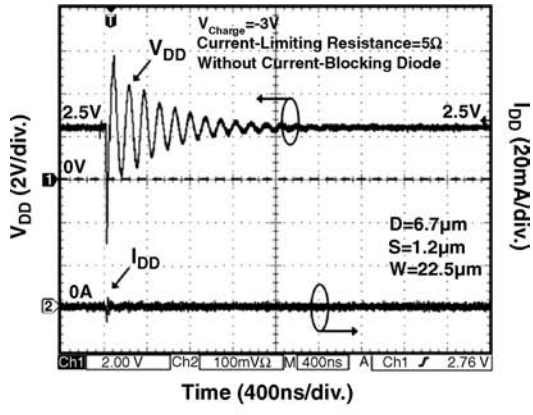
contacts are connected together to V_{DD} (ground). I_{DD} is the total current flowing into the P^+ anode and the N^+ well contact of the SCR. The I_{DD} current magnitude and waveform are measured by a separated current probe. The current-blocking diode, which is used to prevent the capacitor-discharged current from flowing into the power supply, is used to avoid the possible over-estimation for the TLU immunity of the DUT [1, 2]. The current-limiting resistance is used to avoid the EOS damage to the DUT under a high-current latchup state [3].

For a TLU measurement setup with a current-limiting resistance of 5 Ω but without the current-blocking diode, the measured V_{DD} and I_{DD} transient responses with a V_{Charge} of −3 V, −6 V, and + 13 V are shown in Figure 3.2a–c, respectively. The DUT under an initial V_{DD} bias of 2.5 V is the SCR with specified layout parameters of $D = 16.6\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$. With a smaller V_{Charge} of −3 V, V_{DD} acts as the intended bipolar trigger just similar to that measured in Figure 2.3 in the system-level ESD test. Meanwhile, TLU doesn't occur due to a rather small V_{Charge} (only −3 V), because I_{DD} doesn't increase after applying the bipolar trigger voltage on V_{DD}. However, with a larger negative (positive) V_{Charge} of −6 V (+ 13 V), TLU can be initiated, as shown in Figure 3.2b and c. Thus, I_{DD} significantly increases up to 120 mA, and V_{DD} is pulled down to the latchup holding voltage of 1.6 V. By using this TLU measurement setup with a bipolar trigger voltage, the measured V_{DD} and I_{DD} waveforms in Figure 3.2 can simulate the ESD-disturbed V_{DD} and I_{DD} waveforms in Figures 2.3 (no TLU) and 2.4 (TLU occurs) in the system-level ESD test.

3.3 Influence of the Current-Blocking Diode and Current-Limiting Resistance on the Bipolar Trigger Waveforms

Although a TLU measurement setup with a bipolar trigger can accurately simulate the practical system-level ESD event, both bipolar trigger waveforms and TLU immunity of CMOS ICs are strongly dependent on the current-blocking diode and current-limiting resistance. To clarify this issue, TLU measurement setups combining two kinds of current-blocking diodes, a fast recovery diode (PR1507) and a general purpose diode (1N4007), with various current-limiting resistances (0, 5, 10, 20, and 30 Ω) are investigated to find their impacts on both the bipolar trigger waveforms and TLU immunity of the DUT. Both the PR1507 and 1N4007 diodes have a very high reverse breakdown voltage of 1000 V. Thus, for a $V_{Charge} < 1000$ V, the PR1507 or 1N4007 diodes can certainly prevent the discharge current from flowing into the power supply without junction breakdown.

The SCR structure in Figure 2.5 drawn with layout parameters of $D = 16.6\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$ is used to investigate the influences of current-blocking diode and current-limiting resistance on the bipolar trigger waveform. Furthermore, the charging voltage source (V_{Charge}) is set as small as + 8 V for a positive V_{Charge} and −3 V for a negative V_{Charge} to prevent the occurrence of TLU, and so the bipolar trigger waveform on V_{DD} can be clearly observed.



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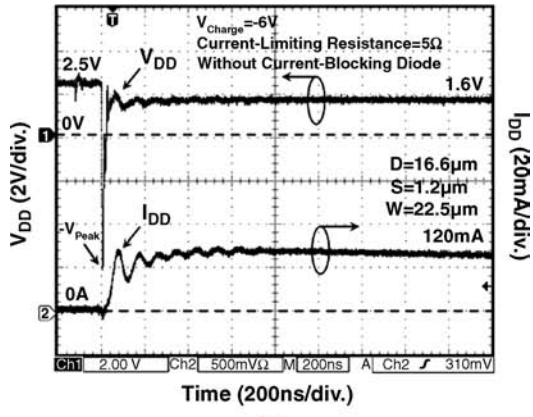

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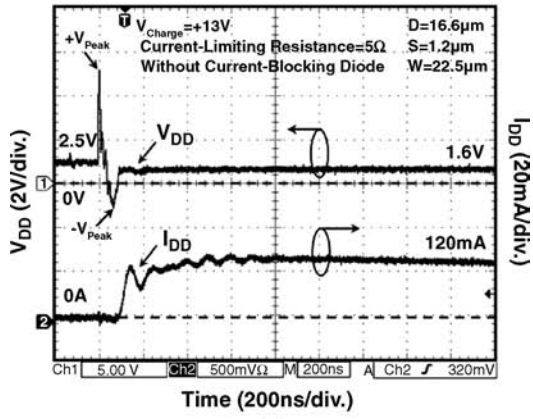


(c)

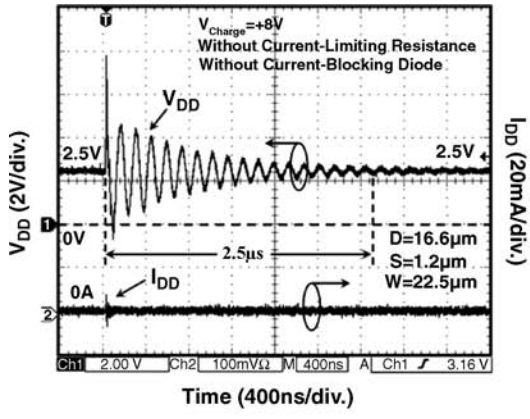
Figure 3.2 For a TLU measurement setup with a current-limiting resistance of 5 Ω but without the current-blocking diode, the measured V_{DD} and I_{DD} transient responses with V_{Charge} of (a) −3 V, (b) −6 V, and (c) + 13 V. (Reprinted with permission from IEEE).

3.3.1 Positive V_{Charge}

With a positive V_{Charge} of $+8$ V, when there is neither a current-blocking diode nor a current-limiting resistance in the TLU measurement setup, the measured V_{DD} and I_{DD} transient waveforms are shown in Figure 3.3a. The V_{DD} waveform reveals the intended positive-going bipolar trigger with a damping frequency of $\sim$10 MHz. Afterwards, when a current-limiting resistance of 20 Ω is added to the TLU measurement setup but still without the current-blocking diode, the damping factor of the V_{DD} waveform obviously increases, as shown in Figure 3.3b. In Figure 3.3a, the initial positive peak voltage of V_{DD} takes about 2.5 μs to be fully attenuated, but only 0.8 μs in Figure 3.3b. Furthermore, if a current-blocking diode (PR1507) is added to the measurement setup but without the current-limiting resistance, the V_{DD} waveform no longer reveals an underdamped bipolar waveform, but an overdamped unipolar waveform instead, as shown in Figure 3.3c. When the initially stored positive charges in the charging capacitor (200 pF) are discharged through the relay into the DUT and power supply, these positive charges are blocked by the current-blocking diode from flowing into the power supply, and so the current-blocking diode acts as a large equivalent resistance (open circuit) to these positive charges. As shown in Figure 3.3b, a current-limiting resistance of 20 Ω increases the damping factor of the V_{DD} waveform, and so the equivalent large resistance of the current-blocking diode tremendously increases the damping factor to result in the overdamped unipolar V_{DD} waveform in Figure 3.3c.

3.3.2 Negative V_{Charge}

With a negative V_{Charge} of -3 V, the measured V_{DD} transient waveforms are similar to the positive V_{Charge} case. For example, the measured V_{DD} waveform is a negative-going bipolar trigger when there is neither a current-blocking diode nor a current-limiting resistance in the measurement setup, as shown in Figure 3.4a. Additionally, the damping factor of this measured V_{DD} waveform will increase if an additional current-limiting resistance of 20 Ω is added to the measurement setup, as shown in Figure 3.4b. However, unlike the positive V_{Charge} case in Figure 3.3c where the V_{DD} waveform is an overdamped unipolar waveform, the V_{DD} waveform in Figure 3.4c is an underdamped bipolar waveform if there is a current-blocking diode (PR1507) but without the current-limiting resistance. When the initially stored negative charges in the charging capacitor (200 pF) are discharged into the power supply, the current-blocking diode is seen as a forward-biased diode by these negative charges, and so the current-blocking diode acts as a small equivalent resistance (short circuit) to these negative charges. Thus, similar to the current-limiting resistance of 20 Ω in Figure 3.4b, the small equivalent resistance of the current-blocking diode also leads to a larger damping factor of the V_{DD} waveform in Figure 3.4c.



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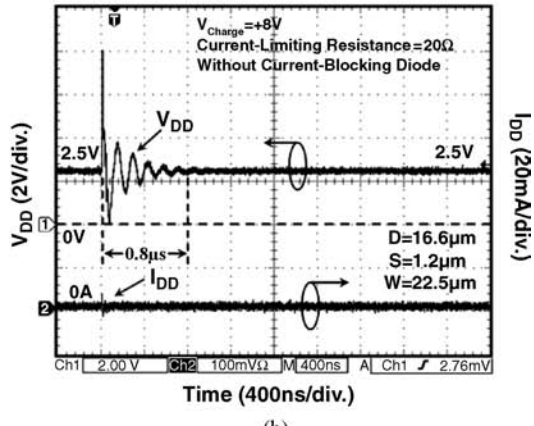

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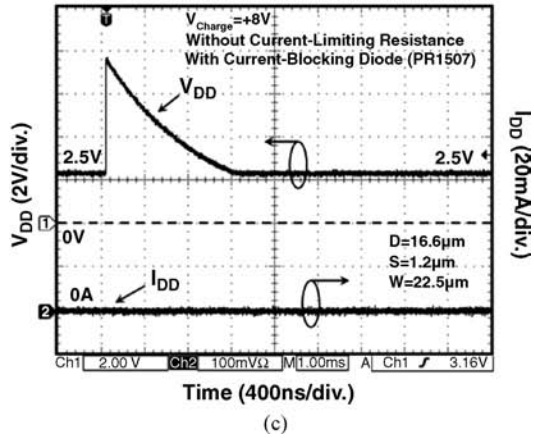
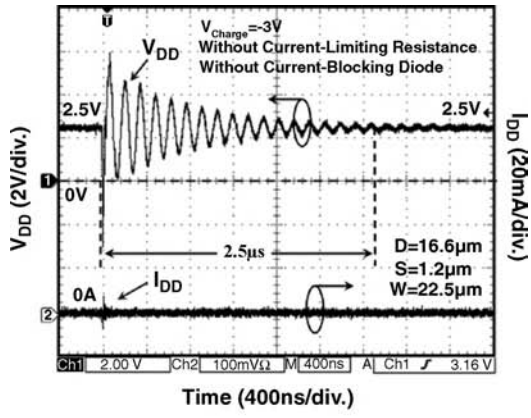


(c)

Figure 3.3 Measured V_{DD} and I_{DD} transient waveforms with a positive V_{Charge} of $+8$ V. (a) Neither a current-blocking diode nor a current-limiting resistance, (b) a current-limiting resistance of $20\,\Omega$ but without a current-blocking diode, and (c) a current-blocking diode (PR1507) but without a current-limiting resistance, are used in the TLU measurement setup. (Reprinted with permission from IEEE).



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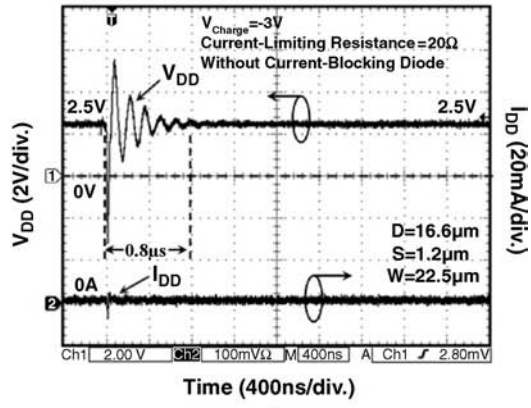

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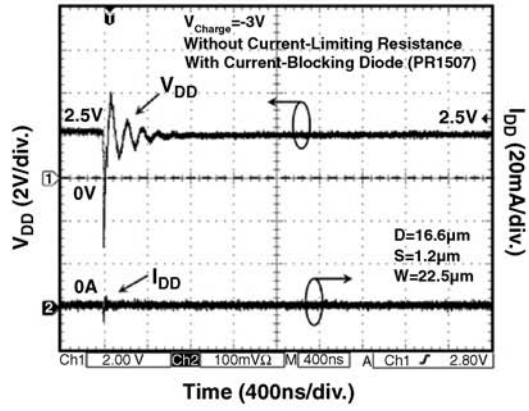


(c)

Figure 3.4 Measured V_{DD} and I_{DD} transient waveforms with a negative V_{Charge} of -3 V. (a) Neither a current-blocking diode nor a current-limiting resistance, (b) a current-limiting resistance of 20 Ω but without a current-blocking diode, and (c) a current-blocking diode (PR1507) but without a current-limiting resistance, are used in the TLU measurement setup. (Reprinted with permission from IEEE).

3.4 Influence of the Current-Blocking Diode and Current-Limiting Resistance on the TLU Level

The TLU level is defined as the minimum V_{Charge} which can trigger on TLU. Thus, a higher TLU level is desired for the DUT, because it means that the DUT is less sensitive to TLU. Furthermore, layout dependences on TLU level are also investigated by using two SCR structures with the same D (16.6 μm) and W (22.5 μm) but different S values of 1.2 μm and 20 μm in a 0.25-μm salicided CMOS process.

3.4.1 Latchup DC I–V Characteristics

The experimentally measured latchup DC I–V characteristics of two SCR structures with the same D (16.6 μm) and W (22.5 μm) but different S values of 1.2 μm and 20 μm are shown in Figure 3.5. These latchup DC I–V curves are measured by the continuous-type curve tracer. The SCR structure with $S = 1.2$ μm ($S = 20$ μm) has a trigger voltage (V_{Trig}) and a trigger current (I_{Trig}) of 19.5 V (21 V) and 2 mA (4 mA), respectively. Once latchup occurs, a low-impedance path will exist between V_{DD} and ground to conduct a huge current.

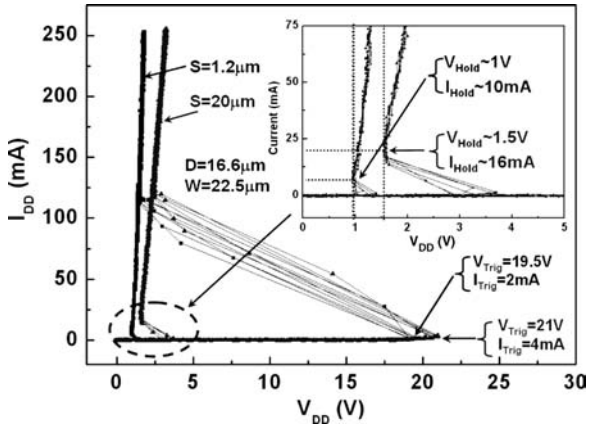


Figure 3.5 Measured latchup DC I–V characteristics of two SCR structures with the same D (16.6 μm) and W (22.5 μm) but different S values of 1.2 and 20 μm. (Reprinted with permission from IEEE).

For the same SCR, the latchup holding voltage should be the same for both quasi-static latchup and TLU, because the holding voltage only depends on the DUT layout styles and the process parameters. However, the pull-down V_{DD} (~1.6 V) of the measured TLU voltage waveforms in Figure 3.2b and c is somewhat higher than the holding voltage (~1 V) in the measured latchup DC I–V curves in Figure 3.5. For the measured TLU voltage waveforms, the pull-down V_{DD} is equal to the $V_{\text{Power-supply}}$-($\Delta V_{\text{Resistor}} + \Delta V_{\text{Diode}}$). Here, $V_{\text{Power-supply}}$ is the applied DC voltage of the power supply, and $\Delta V_{\text{Resistor}}$

(ΔV_{Diode}) is the voltage drop across the 5 Ω current-limiting resistance (current-blocking diode). This pull-down V_{DD} must be higher than the holding voltage of the DUT to sustain the latchup state. For the measured latchup DC *I–V* curves, however, there is neither an additional current-limiting resistance nor a current-blocking diode, and the latchup holding voltage is the minimum voltage that the DUT can pull down in the latchup state. Thus, the pull-down V_{DD} (~1.6 V) of the measured TLU voltage waveforms is slightly higher than the holding voltage (~1 V) in the measured latchup DC *I–V* curves.

3.4.2 Positive TLU Level

For the SCR structure with layout parameters of $D = 16.6\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$, the relations between the positive TLU level and current-limiting resistances under different current-blocking diodes are shown in Figure 3.6a. For a

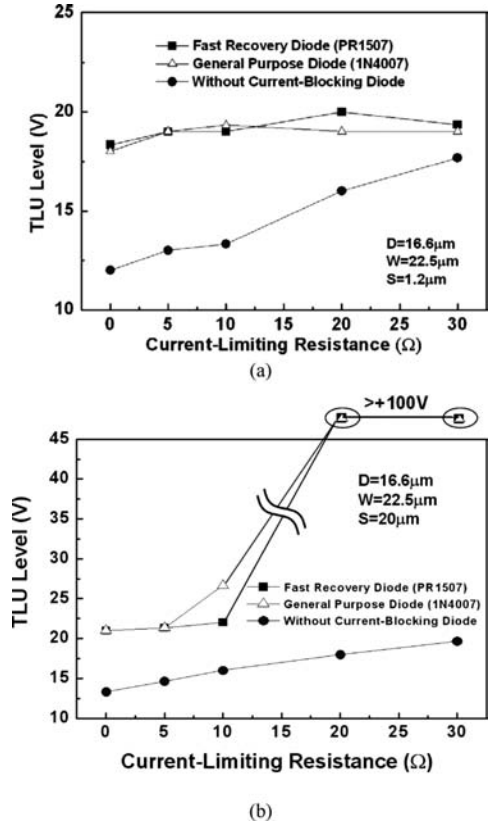


Figure 3.6 Relations between the positive TLU level and current-limiting resistances under different current-blocking diodes. The SCR structure has the layout parameters of (a) $D = 16.6\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$, and (b) $D = 16.6\,\mu m$, $S = 20\,\mu m$, and $W = 22.5\,\mu m$. (Reprinted with permission from IEEE).

measurement setup without a current-blocking diode, the TLU level is overall smaller than that equipped with a current-blocking diode, no matter whether with a general purpose (1N4007) or a fast recovery (PR1507) diode. For a measurement setup with a current-blocking diode, the TLU-triggering voltage is the unipolar trigger shown in Figure 3.3c. Such a unipolar trigger can generate I_{Ds} (the displacement current, as defined in Chapter 2) to initiate TLU while V_{DD} rapidly increases from $+2.5$ V to its positive peak voltage (that is, a large dV_{DD}/dt). However, for a measurement setup without a current-blocking diode, the TLU-triggering voltage is the bipolar trigger shown in Figure 3.3a. Such a bipolar trigger can generate I_{Sb} instead of I_{Ds} to initiate TLU while V_{DD} switches from the forward-biased state ($V_{DD} < 0$) to the normal reversed-biased blocking state ($V_{DD} > 0$). Because I_{Sb} can initiate TLU more easily than I_{Ds} [3, 7], the measurement setup without a current-blocking diode (induced I_{Sb}) can evaluate a much lower TLU level than that equipped with a current-blocking diode (induced I_{Ds}).

The influences of current-limiting resistance on the positive TLU level are also shown in Figure 3.6a. For the measurement setup without a current-blocking diode, the TLU level linearly increases with the current-limiting resistance, because a larger current-limiting resistance can cause a larger damping factor of bipolar voltage on V_{DD}, as shown in Figure 3.3b. A larger damping factor will lead to a smaller I_{Sb} due to a smaller voltage magnitude of $-V_{Peak}$ [7]. Therefore, although current-limiting resistance can avoid EOS damage to DUT, it overestimates the TLU level under a bipolar trigger voltage. However, for a measurement setup equipped with a current-blocking diode, the TLU level is almost independent of the current-limiting resistance, because the current-limiting resistance does not obviously affect the I_{Ds} (that is, dV_{DD}/dt in Figure 3.3c). The equivalent large resistance of the current-blocking diode in series with a small current-limiting resistance ($<30\,\Omega$) makes the effect of current-limiting resistance negligible.

In Figure 3.6a, the TLU levels are different from the latchup trigger voltage ($+19.5$ V) of the quasi-static latchup measurements shown in Figure 3.5. For the quasi-static latchup measurements, the main latchup-triggering current is the reverse junction breakdown current [8]. For the TLU measurements, if the unipolar trigger is the TLU-triggering voltage, it can generate the additional I_{Ds} (due to large dV_{DD}/dt values) to initiate TLU in addition to the junction breakdown current. Thus, if there is a current-blocking diode (inducing a unipolar trigger) but without the current-limiting resistance in the TLU measurement setup, the TLU level ($\sim +16$ V) is slightly lower than the latchup trigger voltage ($+19.5$ V) of the quasi-static latchup measurements. However, if the bipolar trigger voltage is the TLU-triggering voltage, the major TLU-triggering current is I_{Sb} (due to V_{DD} switching from a negative voltage level to a positive voltage level), but not I_{Ds}. It has been clarified that the bipolar trigger can initiate TLU more easily than the unipolar trigger [3, 7]. Thus, there will be a much lower TLU level ($\sim +12$ V) if there is neither a current-blocking diode (induced bipolar trigger) nor a current-limiting resistance in the TLU measurement setup.

For the SCR structure with layout parameters of $D = 16.6\,\mu m$, $S = 20\,\mu m$, and $W = 22.5\,\mu m$, the relations between the positive TLU level and current-limiting resistances under different current-blocking diodes are shown in Figure 3.6b. For a measurement setup equipped with a current-blocking diode, the TLU level greatly increases to exceed $+100$ V when the current-limiting resistance is larger than $20\,\Omega$. In fact, TLU does not occur in these cases due to one of the following two reasons. First, a larger current-limiting resistance leads to an I_{DD} lower than the latchup holding current. Second, a larger voltage drop across a larger current-limiting resistance makes V_{DD} lower than the latchup holding voltage. No matter which one happens, TLU does not occur. For example, with a positive V_{Charge} of $+35$ V, the measured V_{DD} and I_{DD} transient waveforms in a measurement setup with a current-blocking diode (PR1507) and a current-limiting resistance of $20\,\Omega$ are shown in Figure 3.7. TLU initially occurs but finally fails to be maintained, because V_{DD} is pulled down to about 1 V, which is lower than its latchup holding voltage ($\sim$1.5 V). Thus, an additional voltage drop across the current-blocking diode or a larger current-limiting resistance can prohibit the occurrence of TLU when the SCR has a larger latchup holding voltage or current ($D = 16.6\,\mu m$, $S = 20\,\mu m$, and $W = 22.5\,\mu m$).

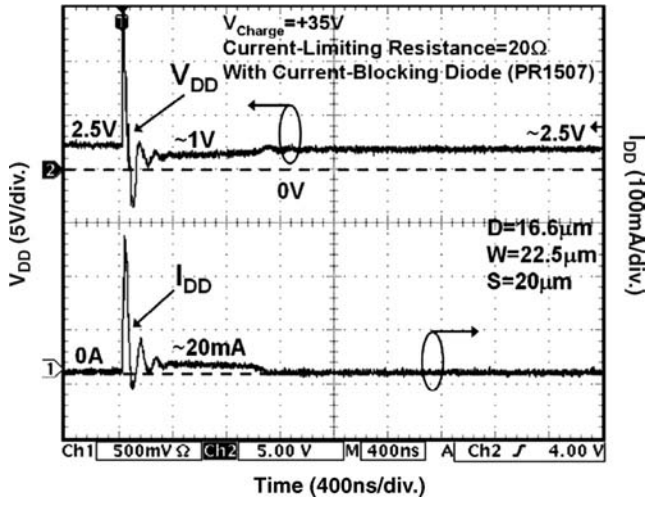


Figure 3.7 Measured V_{DD} and I_{DD} transient waveforms with a positive V_{Charge} of $+35$ V. A current-blocking diode (PR1507) and a current-limiting resistance of $20\,\Omega$ are used in the TLU measurement setup. (Reprinted with permission from IEEE).

3.4.3 Negative TLU Level

For an SCR structure with layout parameters of $D = 16.6\,\mu m$, $W = 22.5\,\mu m$, and $S = 1.2\,\mu m$ ($20\,\mu m$), the relations between the negative TLU level and current-limiting

resistances under different current-blocking diodes are shown in Figure 3.8a and b. Compared with the positive TLU level tests in Figure 3.6a and b, the magnitudes of the negative TLU level are overall lower than those of the positive TLU level. For example, the magnitudes of the negative TLU level are all lower than 6 V in Figure 3.8a, but those of the positive TLU level are all higher than 10 V in Figure 3.6a. Compared with the negative-going ($V_{\text{Charge}} < 0$) bipolar trigger, the positive-going ($V_{\text{Charge}} > 0$) bipolar trigger needs to take an additional half duration for decaying before V_{DD} reaches $-V_{\text{Peak}}$. Thus, under the same voltage magnitude of both positive and negative V_{Charge},

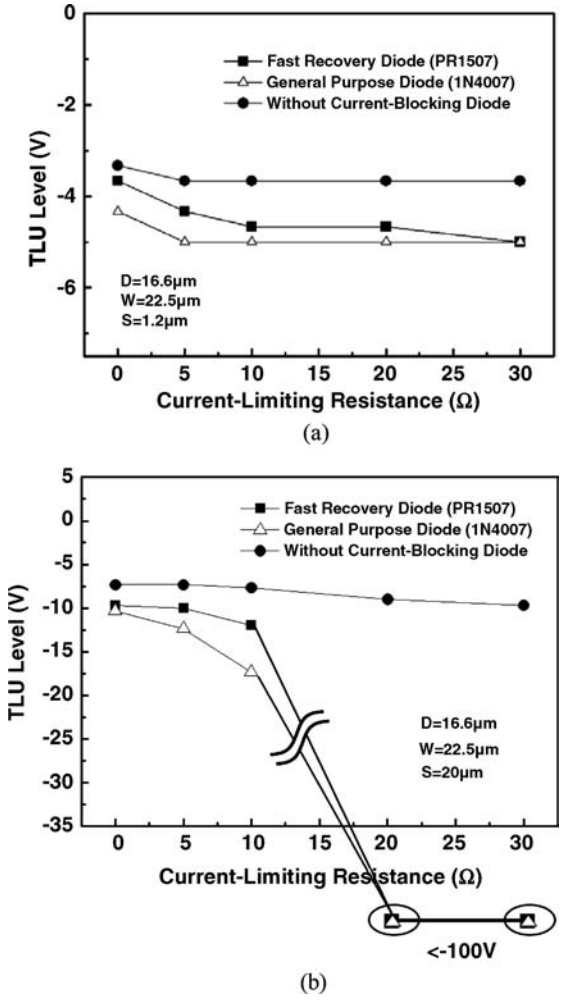


Figure 3.8 Relations between the negative TLU level and current-limiting resistances when using different current-blocking diodes. The SCR structure has the layout parameters of (a) $D = 16.6\,\mu\text{m}$, $S = 1.2\,\mu\text{m}$, and $W = 22.5\,\mu\text{m}$, and (b) $D = 16.6\,\mu\text{m}$, $S = 20\,\mu\text{m}$, and $W = 22.5\,\mu\text{m}$. (Reprinted with permission from IEEE).

a negative V_{Charge} can provide a larger voltage magnitude of $-V_{Peak}$ (that is, larger I_{Sb}) than the positive V_{Charge} [7]. As a result, SCR structures are more sensitive to TLU with a negative V_{Charge}, leading to a very low negative TLU level in comparison with the positive TLU level.

3.5 Verifications of Device Simulation

A two-dimensional device simulation tool (MEDICI) is used to verify the dependences of both the current-blocking diode and current-limiting resistance on the TLU level of the SCR structure. A specified SCR structure with the same geometrical parameters ($D = 16.6\,\mu m$ and $S = 1.2\,\mu m$) in the silicon is used for all TLU device simulations, as shown in Figure 3.9. With this device simulation, the 2-D boundary conditions of this specified SCR can be well defined to analyze TLU electrical characteristics such as transient *I–V* characteristics, 2-D current flow lines, electric field, carrier concentration, and so on.

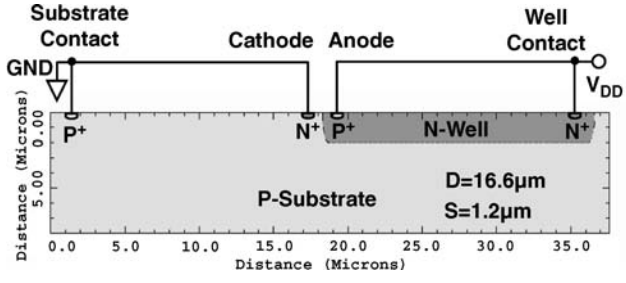


Figure 3.9 The SCR structure used in a two-dimensional device simulation tool (MEDICI). This specified SCR structure has the same geometrical parameters ($D = 16.6\,\mu m$ and $S = 1.2\,\mu m$) of SCR silicon test chips. (Reprinted with permission from IEEE).

3.5.1 Dependences of the Current-Blocking Diode on TLU Level

From the measured TLU level dependences in Figures 3.6 and 3.8, a TLU measurement setup equipped with the current-blocking diode (positive-going unipolar trigger) will lead to a higher TLU level (over estimation) of the DUT than without the current-blocking diode (bipolar trigger). To demonstrate this phenomenon by device simulation, the simulated V_{DD} and I_{DD} transient responses under a unipolar trigger and bipolar trigger are shown in Figures 3.10 and 3.11, respectively. The related parameters of the unipolar trigger (bipolar trigger) such as rise time and falling rate (damping frequency and damping factor) are extracted from the corresponding measured waveforms in Figure 3.3c and a.

With the unipolar trigger in Figure 3.10, TLU will not be initiated due to insufficient I_{Ds}, because the increasing rate ($\equiv (+V_{Peak} - 2.5\,V)$/rise time) of V_{DD} isn't large

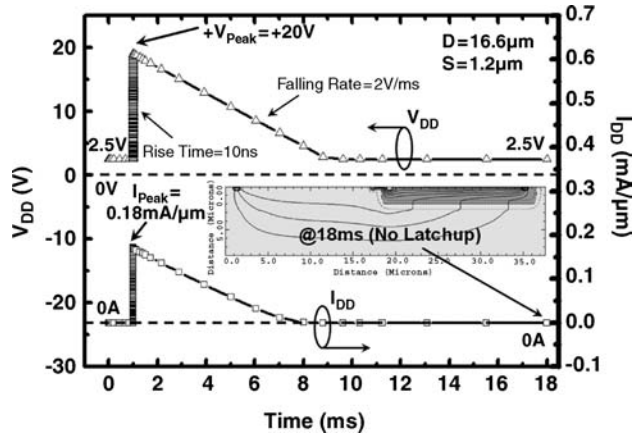


Figure 3.10 Simulated V_{DD} and I_{DD} transient responses for TLU with a unipolar trigger. This can simulate the V_{DD} voltage disturbance in Figure 3.3c for a TLU measurement setup equipped with the current-blocking diode. TLU cannot be initiated even though V_{Peak} is as high as $+20$ V. (Reprinted with permission from IEEE).

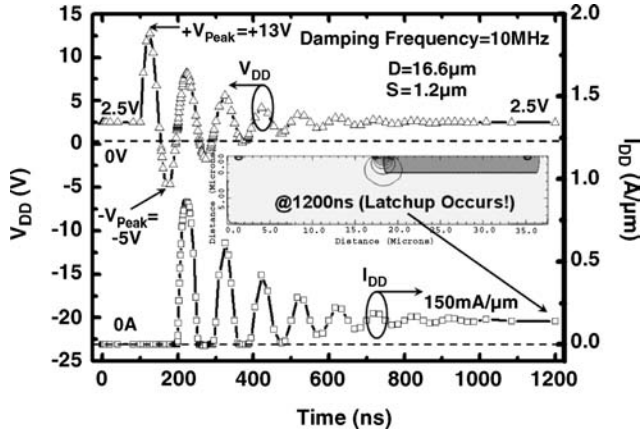


Figure 3.11 Simulated V_{DD} and I_{DD} transient responses for TLU with a bipolar trigger. This can simulate the V_{DD} voltage disturbance in Figure 3.3a for a TLU measurement setup without the current-blocking diode. TLU can be initiated even though V_{Peak} is as low as $+13$ V. (Reprinted with permission from IEEE).

enough, even though the $+V_{Peak}$ is as high as $+20$ V. Thus, I_{DD} only comes from the small I_{Ds} or leakage current whose positive peak current (I_{Peak}) is only 0.18 mA/μm, and then I_{DD} decreases to 0 A when V_{DD} finally returns to its normal operating voltage ($+2.5$ V). The simulated 2-D current flow line after applying the unipolar trigger voltage on V_{DD} (at 18 ms) is also shown in the inset figure of Figure 3.10. Clearly, TLU doesn't occur because no current flow lines conduct through the low-impedance latchup path.

Under the bipolar trigger in Figure 3.11, TLU can be initiated (I_{DD} significantly increases) by a large enough I_{Sb} while V_{DD} returns from $-V_{Peak}$ (-5 V) to the normal operating voltage of $+2.5$ V, even though its $+V_{Peak}$ is only $+13$ V, which is much smaller than $+20$ V in Figure 3.10 (unipolar trigger). Thus, I_{DD} will be kept at a high current latchup state (150 mA/μm) after V_{DD} finally returns to its normal operating voltage ($+2.5$ V). The simulated 2-D current flow line after applying the bipolar trigger voltage on V_{DD} (at 1200 ns) is also shown in the inset figure of Figure 3.11. Clearly, TLU occurs because all current flow lines conduct through the low-impedance latchup path. The simulation results in Figure 3.11 are consistent with the measured TLU waveforms in Figure 3.2c that I_{DD} simultaneously increases with V_{DD} while V_{DD} increases from $-V_{Peak}$ to $+2.5$ V (induced I_{Sb}), but not initially from $+2.5$ V to $+V_{Peak}$ (induced I_{Ds}). Thus, I_{Sb} is the major TLU-triggering current rather than I_{Ds}.

TLU can be also initiated by a unipolar trigger with a large enough I_{Ds}. For the unipolar trigger with a higher $+V_{Peak}$ of $+25$ V, the simulated V_{DD} and I_{DD} transient responses for TLU are shown in Figure 3.12. Due to a larger increasing rate of V_{DD}, TLU can be initiated by a large enough I_{Ds} while V_{DD} rapidly increases from the normal operating voltage ($+2.5$ V) to $+V_{Peak}$ ($+25$ V). Thus, I_{DD} will be kept at a high current latchup state (150 mA/μm) after V_{DD} finally returns to its normal operating voltage.

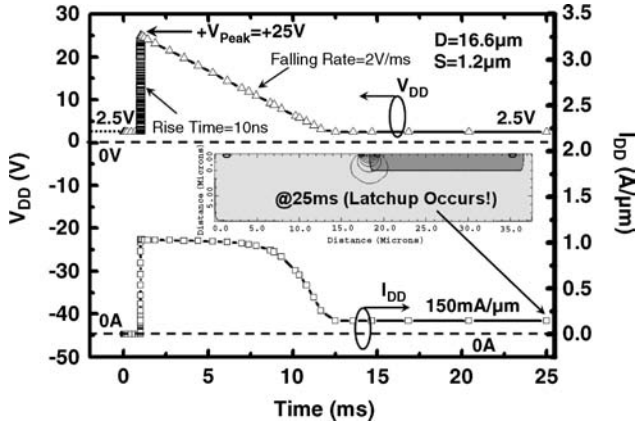


Figure 3.12 Simulated V_{DD} and I_{DD} transient responses for TLU with a unipolar trigger. V_{DD} has a V_{Peak} of $+25$ V, which is larger than $+20$ V in Figure 3.10, and so the increasing rate ($\equiv$ ($+$ V_{Peak} -2.5 V)/rise time) of V_{DD} is large enough to produce a large I_{Ds} to initiate TLU. (Reprinted with permission from IEEE).

The comprehensive simulation results in Figures 3.10–3.12 are all consistent with the experimental results to point out that TLU measurement setup equipped with the current-blocking diode will lead to a higher TLU level (over estimation) of the DUT than that without the current-blocking diode.

3.5.2 Dependences of Current-Limiting Resistance on TLU Level

From the measured TLU level dependences shown in Figures 3.6 and 3.8, the TLU level of a CMOS IC (SCR) increases with current-limiting resistance. To demonstrate this phenomenon by device simulation, two different bipolar triggers are used. As shown in Figures 3.11 and 3.13, these two different bipolar triggers have the same damping frequency of ~10 MHz but different damping factors. Compared to Figure 3.11, the bipolar trigger with a larger damping factor in Figure 3.13 is used to simulate the TLU measurement setup equipped with a current-limiting resistance, because the measured V_{DD} waveforms in Figure 3.3a and b show that the current-limiting resistance will lead to a larger damping factor. Clearly, because the magnitude of the $-V_{Peak}$ decreases from 5 V (Figure 3.11) to 2.5 V (Figure 3.13) due to a larger damping factor, I_{Sb} isn't large enough to initiate TLU while V_{DD} returns from $-V_{Peak}$ to its normal operating voltage. Thus, I_{DD} doesn't significantly increase (I_{Peak} is only 75 μA/μm) with V_{DD}, and then I_{DD} decreases to 0 A when V_{DD} finally returns to its normal operating voltage. Thus, the simulation results in Figures 3.11 and 3.13 are all consistent with the experimental results to verify that the TLU level is increased by the current-limiting resistance, as shown in Figures 3.6 and 3.8.

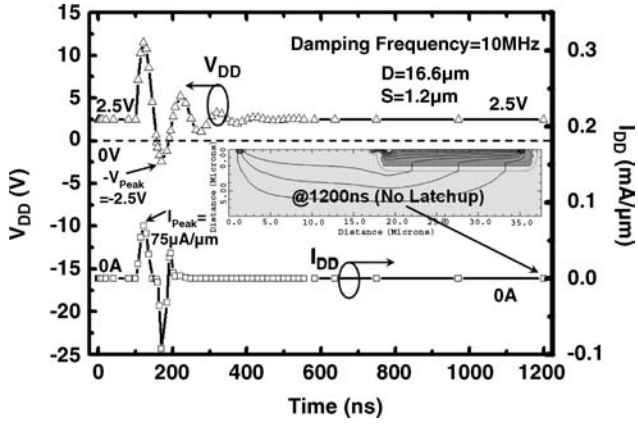


Figure 3.13 Simulated V_{DD} and I_{DD} transient responses for TLU with a bipolar trigger. Compared to Figure 3.11, this can simulate the bipolar trigger with a larger damping factor in Figure 3.3b for a TLU measurement setup equipped with a current-limiting resistance. TLU cannot be initiated due to an insufficient I_{Sb}. (Reprinted with permission from IEEE).

3.6 Suggested Component-Level TLU Measurement Setup

From the comprehensive measured and simulated TLU level dependency on current-limiting resistance and current-blocking diode in the component-level TLU measurement setup, the TLU measurement setup without a current-blocking diode but with a

small current-limiting resistance (5 Ω) is suggested. This suggested measurement setup not only can accurately evaluate the TLU immunity of CMOS ICs without over-estimation, but also can avoid the EOS damage to the DUT during the TLU test.

The current-blocking diode should be eliminated from the TLU measurement setup to accurately evaluate the TLU immunity of CMOS ICs without over-estimation. The bipolar transient noises on the power pins of the DUT are indeed representative of the practical system-level ESD events, as shown in Figures 2.3 and 2.4. However, because the current-blocking diode inherently alters the power supply network impedance, the use of a current-blocking diode certainly prohibits such a bipolar trigger voltage on the power pins of the DUT. Instead, an unipolar overdamped trigger voltage will be formed if the diode was added to the TLU measurement setup. Thus, to accurately simulate the practical system-level ESD event, the current-blocking diode should be eliminated from the TLU measurement setup. Additionally, unipolar and bipolar transient V_{DD} noises can generate two different TLU-triggering currents – I_{Ds} for a unipolar trigger, and I_{Sb} for a bipolar trigger. It has been clarified that the bipolar trigger (I_{Sb}) can initiate TLU more easily than the unipolar trigger (I_{Ds}). Thus, to accurately represent the actual TLU immunity of the DUT in the system-level ESD test, the component-level TLU test should be performed without the current-blocking diode.

Similar to the current-blocking diode, current-limiting resistance is also unsuitable for being equipped in the component-level TLU measurement setup. Although using a current-limiting resistance will not lead to a unipolar trigger, it certainly attenuates the voltage magnitude of the bipolar trigger (that is, larger damping factor), as shown in Figures 3.3b and 3.4b. A larger damping factor will lead to a smaller TLU-triggering current (I_{Sb}) due to the smaller voltage magnitude of the $-V_{Peak}$ [7]. Thus, the TLU level of the DUT will increase with the current-limiting resistance, leading to an over-estimation of the TLU immunity. Even worse, a too large current-limiting resistance ($>20\,\Omega$) has been proved to lead TLU not occurring in the SCR structure with a higher holding voltage (1.5 V), that is, an SCR with a larger S of 20 μm shown in Figures 3.6b and 3.8b. As a result, to accurately represent the actual TLU immunity of the DUT in the system-level ESD test, a small current-limiting resistance (5 Ω) is suggested to be used. This small current-limiting resistance has the advantage of not leading to a serious over-estimation of the TLU level, as shown in Figures 3.6 and 3.8. In addition, it can prevent the DUT from EOS damage during the high-current latchup state.

3.7 TLU Verification on Real Circuits

A 100 MHz ring oscillator consisting of a 101-stage inverter chain and a 7-stage taper buffer, fabricated in a 0.25-μm CMOS technology, is used as a real circuit for TLU verification. The schematic diagram and layout top view of the ring oscillator are shown in Figure 3.14a and b, respectively. The geometrical parameters such as X, Y, and Z represent the distances between the well-edge and well (substrate) contact,

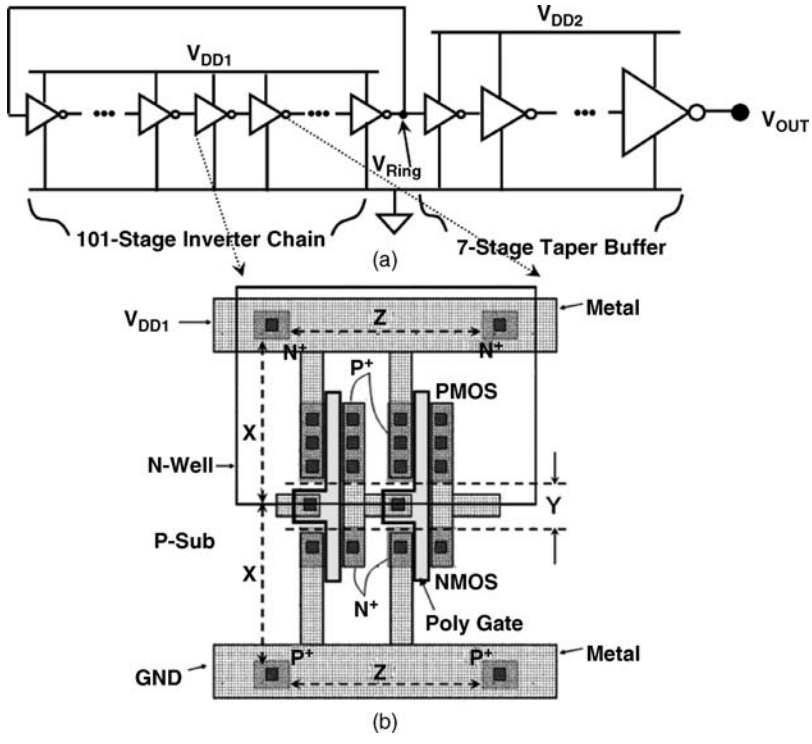


Figure 3.14 (a) Schematic diagram, and (b) layout top view, of the ring oscillator. The geometrical parameters such as *X*, *Y*, and *Z* represent the distances between the well-edge and well (substrate) contact, source (drain) regions of the PMOS and NMOS, and the adjacent well (substrate) contacts, respectively. (Reprinted with permission from IEEE).

source (drain) regions of the PMOS and NMOS, and the adjacent well (substrate) contacts, respectively. The ring oscillator is treated as the DUT, where the N^+ well contact and the P^+ source of the PMOS are connected together to V_{DD1}, whereas the P^+ substrate contact and the N^+ source of the NMOS are connected to ground. To evaluate the TLU level of the inverter chain but not the taper buffer, the power line of the taper buffer (V_{DD2}) is separated from the power line of the inverter chain (V_{DD1}). Once TLU is triggered on by a positive or negative V_{Charge} within the ring oscillator, a rapidly increasing current will conduct through a low-impedance path between V_{DD1} and ground to probably burn out the chip. To verify the TLU issue on the ring oscillator, a TLU measurement setup equipped with a current-limiting resistance of 5 Ω but without the current-blocking diode is used. For the ring oscillator with layout parameters of $X = 16.6\,\mu m$, $Y = 1.2\,\mu m$, and $Z = 22.5\,\mu m$, the measured V_{DD1}, I_{DD1}, and V_{OUT} transient responses for TLU with a V_{Charge} of $+7$ V and -5 V are shown in Figure 3.15a and b, respectively. In both cases, TLU is triggered on due to a large enough I_{Sb} while V_{DD1} increases from its negative peak voltage to the normal operating voltage ($+2.5$ V). Meanwhile, a rapidly increasing I_{DD1} accompanies the pull-down

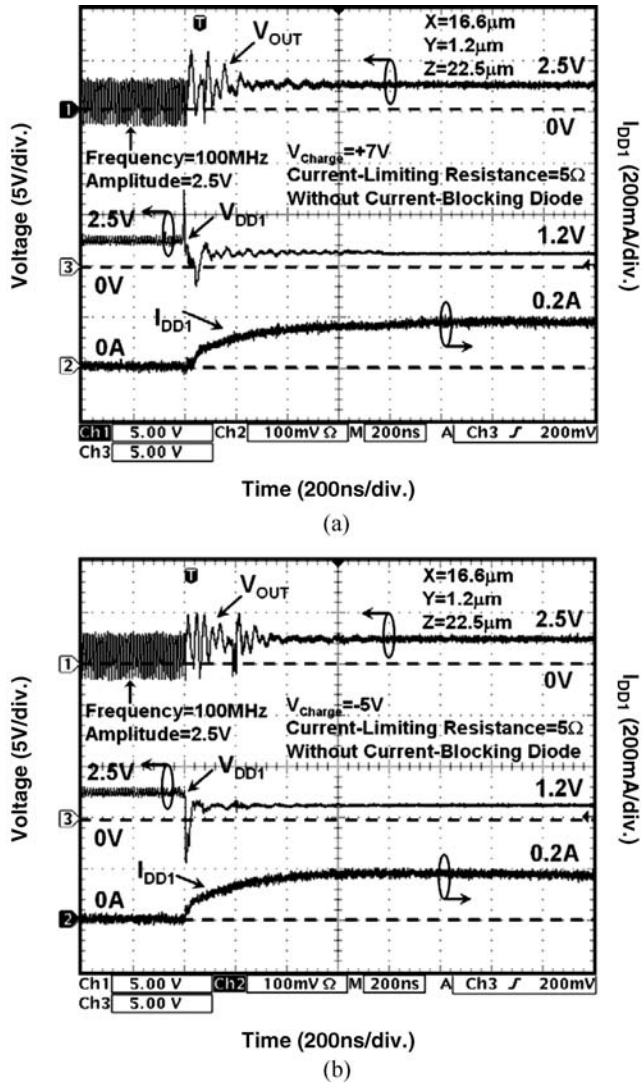


Figure 3.15 Measured V_{DD1}, I_{DD1}, and V_{OUT} transient waveforms of the ring oscillator with a V_{Charge} of (a) $+7$ V, and (b) -5 V. A current-limiting resistance of 5 Ω but without a current-blocking diode is used in the TLU measurement setup. (Reprinted with permission from IEEE).

V_{DD1} due to the low-impedance path between V_{DD1} and ground. Thus, the ring oscillator fails to function correctly, causing the output voltage of the ring oscillator, V_{Ring}, to be pulled down to ground. Thus, V_{OUT} is kept at $+2.5$ V after the 7-stage taper buffer.

Four measurement setups with two different types of current-blocking diodes (PR1507 and 1N4007) and current-limiting resistances (5 and 20 Ω) are used to verify whether the suggested measurement setup has the lowest TLU level (without over-estimation). Moreover, ring oscillators with two sets of layout parameters

($X = 16.6\,\mu m$, $Y = 1.2\,\mu m$, and $Z = 22.5\,\mu m$, as well as, $X = 16.6\,\mu m$, $Y = 10\,\mu m$, and $Z = 0.3\,\mu m$) are also used to investigate the layout dependences on the TLU level. Table 3.1 lists the TLU levels of the ring oscillators with two sets of layout parameters under four different TLU measurement setups.

Table 3.1 TLU levels of the ring oscillators with two sets of layout parameters under four different TLU measurement setups. (Reprinted with permission from IEEE).

Measurement setup		Type A (suggested)	Type B	Type C	Type D
Current-Blocking Diode		None	PR1507	None	1N4007
Current-Limiting Resistance		5Ω	5Ω	20Ω	20Ω
X = 16.6 μm Y = 1.2 μm Z = 22.5 μm	Positive TLU Level Negative TLU Level	+7 V −5 V	+15 V −9 V	+10 V −7 V	+15 V −10 V
X = 16.6 μm Y = 10 μm Z = 0.3 μm	Positive TLU Level Negative TLU Level	+26 V −11 V	TLU Does Not Occur		

For the ring oscillator with layout parameters of $X = 16.6\,\mu m$, $Y = 1.2\,\mu m$, and $Z = 22.5\,\mu m$, both positive and negative TLU levels measured by the suggested TLU measurement setup (Type A) are lower than those measured by the other three measurement setups (types B, C, and D) where a current-blocking diode or a large current-limiting resistance of $20\,\Omega$ is used. For the ring oscillator with layout parameters of $X = 16.6\,\mu m$, $Y = 10\,\mu m$, and $Z = 0.3\,\mu m$, TLU occurs only for the suggested measurement setup (type A). In types B, C, and D measurement setups, the additional voltage drop across the current-blocking diode or large current-limiting resistance leads the V_{DD} (I_{DD}) to be lower than the holding voltage (holding current) of the parasitic SCR in the ring oscillator. Thus, it has been proved once again that the suggested measurement setup (no current-blocking diode but a small current-limiting resistance) can efficiently evaluate the TLU level of CMOS ICs without over-estimation.

3.8 Evaluation on Board-Level Noise Filters to Suppress TLU[2]

To improve the TLU immunity of CMOS ICs, an intuitional solution is to utilize the board-level noise filters, because the board-level noise filter networks between the noise sources and CMOS ICs can decouple, bypass, or absorb noise voltage (energy) [9, 10] which may initiate TLU.

[2] © 2006 IEEE. 3.8 reprinted, with permission, from Ming-Dou Ker and Sheng-Fu Hsu, Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test (sections II–V and figures 6, 7, 9–13, 15, and 18), in *IEEE Transactions on Electromagnetic Compatibility*, Vol. 48, no. 1, pp. 161–171, Feb. 2006. IEEE, Piscataway, NJ.

To clarify such a TLU issue in the system-level ESD test, with an ESD voltage of −3000 V discharging on the horizontal coupling plane (HCP), the measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 are shown in Figure 3.16. With a large transient peak voltage of ±60 V, TLU is triggered on with a large transient current of I_{DD}. Thus, I_{DD} is kept at a high current of 80 mA, and V_{DD} is pulled down to the latchup holding voltage of 1.8 V, after the ESD-induced disturbance on V_{DD}. If an additional decoupling capacitance of 0.1 μF is added between V_{DD} and V_{SS} (ground) of such a TLU-sensitive CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with the same (−3000 V) ESD voltage discharging on the HCP are shown in Figure 3.17. Compared with the measured waveforms in Figure 3.16 where there is no decoupling capacitance for suppressing ESD-induced noise, the transient peak voltage (damping factor) of the bipolar trigger waveform is greatly reduced (increased) in Figure 3.17. As a result, TLU does not occur, and I_{DD} doesn't increase after the ESD-induced disturbance on V_{DD}. Thus, the occurrence of TLU strongly depends on the board-level noise filters, and they should be further investigated to find their improvements on the TLU immunity of CMOS ICs.

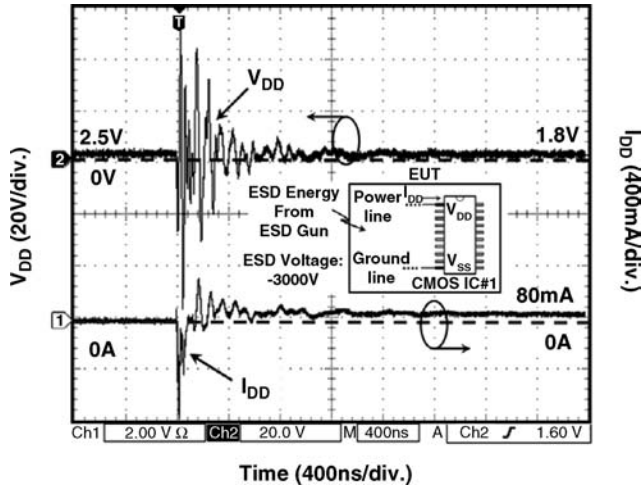


Figure 3.16 Measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 with an ESD voltage of −3000 V discharging on the HCP. With a large transient peak voltage of ±60 V, TLU is triggered on (I_{DD} is kept at a high current of 80 mA) after the ESD-induced disturbance on V_{DD}. (Reprinted with permission from IEEE).

The suggested component-level TLU measurement setup can used to evaluate the effectiveness of board-level noise filter networks to improve the TLU immunity of CMOS ICs in the system-level ESD test, as shown in Figure 3.18. The noise filter network located between the TLU-triggering source and the DUT is used to decouple, bypass, or absorb noise voltage (energy) produced by the TLU-triggering source. The

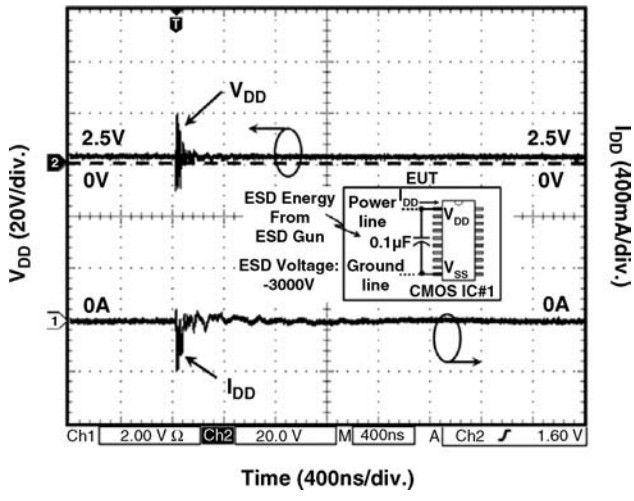


Figure 3.17 With the decoupling capacitance of 0.1 μF between V_{DD} and V_{SS} of the CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with the same (−3000 V) ESD voltage discharging on the HCP. Compared with the measured waveforms in Figure 3.16, TLU does not occur, because the ESD-induced disturbance on V_{DD} is greatly reduced. (Reprinted with permission from IEEE).

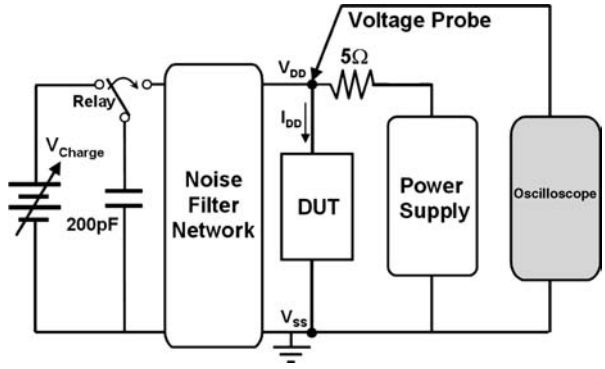
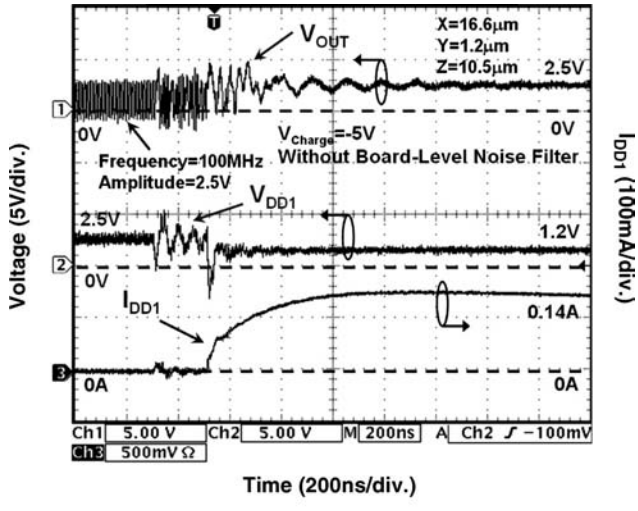


Figure 3.18 Using the suggested component-level TLU measurement setup to evaluate the effectiveness of board-level noise filters to improve the TLU immunity of CMOS ICs in the system-level ESD test. The DUT is the ring oscillator with $X = 16.6\,\mu m$, $Y = 1.2\,\mu m$, and $Z = 10.5\,\mu m$. (Reprinted with permission from IEEE).

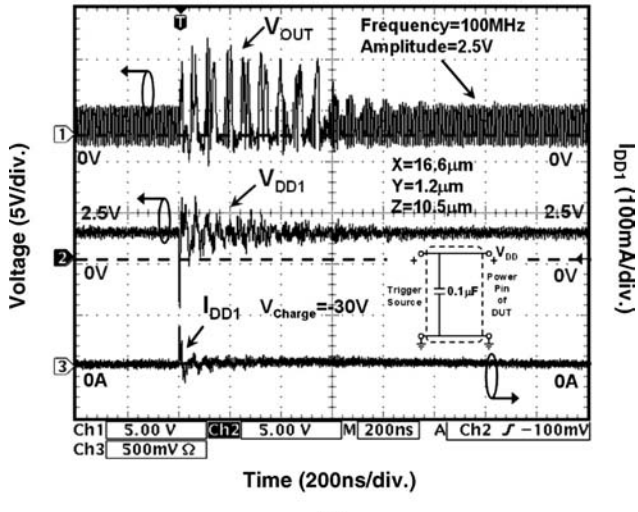
DUT is the ring oscillator fabricated in a 0.25-μm CMOS process, as shown in Figure 3.14. To consider the worst case of evaluating the TLU level, it has a minimum allowable anode-to-cathode spacing (Y) of 1.2 μm, and a large X (Z) of 16.6 μm (10.5 μm), and so it is very sensitive to latchup. Three common noise-decoupling components are evaluated to find their improvements on TLU immunity, including the decoupling capacitor, ferrite bead, and transient voltage suppressor (TVS).

3.8.1 TLU Transient Waveforms of the Ring Oscillator

Figure 3.19a and b show the measured V_{DD1}, I_{DD1}, and V_{OUT} transient responses for the ring oscillator without and with the board-level noise filter network, respectively. For the ring oscillator without the board-level noise filter network, TLU can be triggered on even if the V_{Charge} is as low as −5 V, as shown in Figure 3.19a. Once TLU is initiated,



(a)



(b)

Figure 3.19 Measured V_{DD1}, I_{DD1}, and V_{OUT} transient responses for the ring oscillator (a) without, and (b) with, the board-level noise filter network. With the help of a decoupling capacitance of 0.1 µF, TLU doesn't occur even though the V_{Charge} is as high as −30 V. (Reprinted with permission from IEEE).

I_{DD1} will significantly increase (0.14 A) with the pull-down V_{DD1} (1.2 V) due to a low-impedance latching path between V_{DD1} and ground. Thus, the ring oscillator fails to function correctly, causing the output voltage of the ring oscillator, V_{Ring}, to be pulled down to ground. So, V_{OUT} is kept at $+2.5$ V after the 7-stage taper buffer.

For the ring oscillator with the board-level noise filter network (capacitor filter with a decoupling capacitance of 0.1 μF), TLU doesn't occur even though the V_{Charge} is as high as -30 V, as shown in Figure 3.19b. Clearly, with the aid of the decoupling capacitor to decouple TLU-triggering noises on V_{DD1}, the ring oscillator still maintains its normal function (V_{OUT} with a100 MHz voltage clock) after the TLU-triggering disturbance on V_{DD1}. Thus, the measurement setup can be used to evaluate the effectiveness of different types of board-level noise filter networks to improve the TLU immunity of CMOS ICs in the system-level ESD test.

3.8.2 TLU Level of the Ring Oscillator with Noise Filters

Three common noise-decoupling components, i.e. decoupling capacitor, ferrite bead, and TVS, are depicted in Figure 3.20a–c, respectively. Figures 3.21 and 3.22 show their improvements on both the positive and negative TLU levels of the ring oscillator.

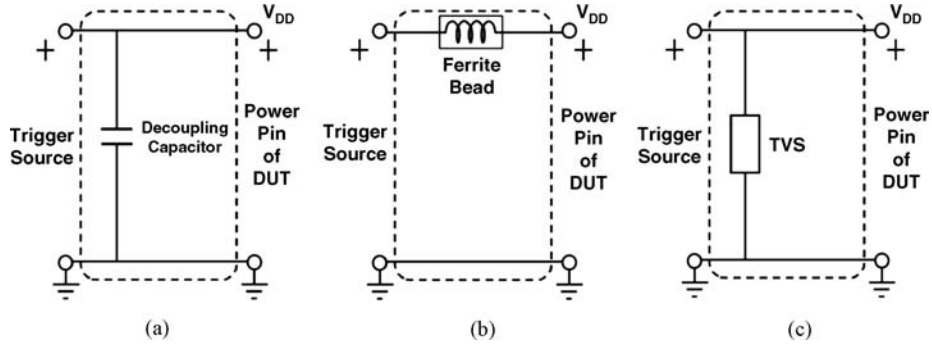


Figure 3.20 Three types of noise filters investigated for their improvements on the TLU level of the ring oscillator: (a) capacitor filter, (b) ferrite bead, and (c) TVS. (Reprinted with permission from IEEE).

The ceramic disc capacitor with advantages such as a high rated working voltage (1 kV), good thermal stability, and low loss over a wide range of frequencies is employed as the decoupling capacitor in the noise filter of Figure 3.20a. Decoupling capacitances widely ranging from 100 pF to 0.1 μF are used to investigate their improvements on the TLU level. With the aid of the capacitor filter to reduce the noise voltage on V_{DD}, the positive TLU level can be significantly enhanced from $+8$ V (without a decoupling capacitor) to $+70$ V (with a decoupling capacitance of 0.1 μF), as shown in Figure 3.21. Similarly, the negative TLU level can be also greatly enhanced

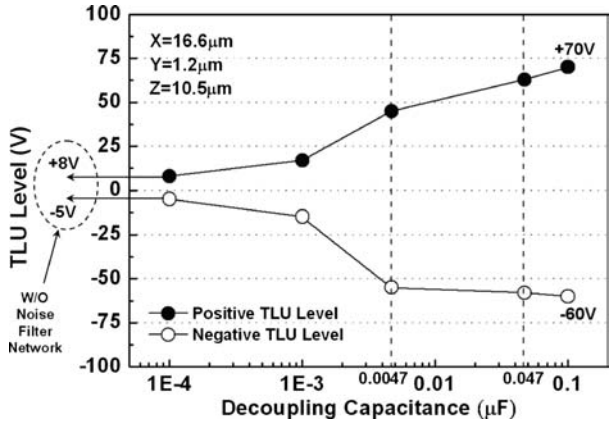


Figure 3.21 Relations between the decoupling capacitance and the TLU level of the ring oscillator.

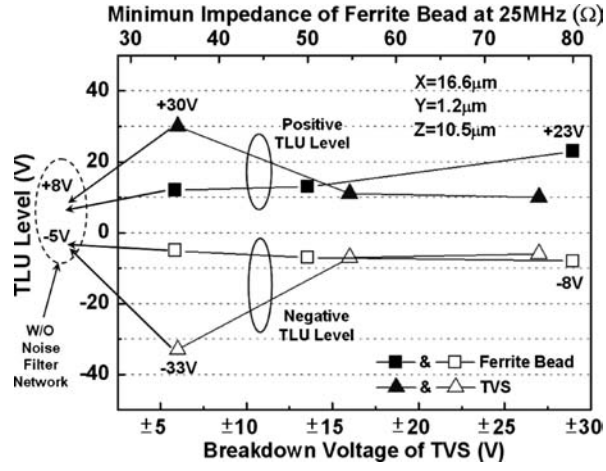


Figure 3.22 Relations among the TLU level of the ring oscillator, minimum impedance of the ferrite bead at 25 MHz, and the breakdown voltage of the TVS under two types of noise filters: ferrite bead and TVS.

from −5 V (without a decoupling capacitor) to −60 V (with a decoupling capacitance of 0.1 μF). Thus, by choosing a decoupling capacitor with the proper capacitance value, a simple first-order decoupling capacitor placed between V_{DD} and V_{SS} (ground) of CMOS ICs can be used to appropriately improve the TLU immunity of the DUT in the system-level ESD test, no matter whatever the positive or the negative TLU level.

The ferrite bead commonly used for absorbing radiofrequency (RF) energy is shown in Figure 3.20b. Here, a resistor-type ferrite bead (part number: RH 3.5 × 9 × 0.8 with a minimum impedance of 80 Ω (120 Ω) at 25 MHz (100 MHz)) is employed. Due to the

lesser energy-absorbing ability of the ferrite bead at a frequency lower than 10 MHz [10], the TLU level will not be efficiently improved by the ferrite bead alone (the magnitudes of both positive and negative TLU levels are all lower than 25 V), even though the minimum impedance of the ferrite bead at 25 MHz is as high as 80 Ω.

The TVS, which is commonly used to bypass/decouple the high-frequency transient noises, is also considered for its enhancement on the TLU immunity of the ring oscillator. The bidirectional-type TVS (part number: P6KE series) with three different breakdown voltages, V_{BR}, ($\pm$6.8, $\pm$16, and $\pm$27 V) are employed. As shown in Figure 3.22, the TVS with breakdown voltages of $\pm$16 V or $\pm$27 V fail to efficiently improve the TLU level (the magnitudes of both positive and negative TLU levels are all lower than 12 V), because TLU occurs prior to the breakdown of such a high-V_{BR} TVS. That is, the intrinsic TLU level of the ring oscillator (positive and negative TLU level of $+8$ and -5 V) is smaller than the V_{BR} of such a high-V_{BR} TVS ($\pm$16 and $\pm$27 V). Only the TVS with a V_{BR} lower than (or at least comparable to) the intrinsic TLU level of the DUT can effectively enhance the TLU level. For example, the positive (negative) TLU level can be enhanced up to $+30$ V (-33 V) for a low-V_{BR} ($\pm$6.8 V) TVS. Thus, to optimize the efficiency of the TVS for TLU prevention, it should be clarified in advance for the correlations between the V_{BR} of the TVS and the intrinsic TLU level of the DUT.

From Figures 3.21 and 3.22, it can be found that the TVS doesn't improve the TLU level as greatly as the decoupling capacitor. For example, the positive (negative) TLU level can be greatly enhanced up to 70 V (-60 V) for a decoupling capacitor with a capacitance of 0.1 μF, but only up to 30 V (-33 V) for a TVS with a low V_{BR} of $\pm$6.8 V. Thus, the decoupling capacitor is better than the TVS in acting as a noise-bypassing component. To further improve the TLU immunity, higher-order noise filters have proved to be good solutions, such as LC (second-order) or π-section (third-order) filters [9–12]. They have the advantage of avoiding an excessively or unreasonably large decoupling capacitance in a simple first-order capacitor filter. Therefore, the decoupling capacitance can be optimized according to the intended TLU level, as well as the category of the board-level noise filter.

3.9 Conclusion

An efficient component-level TLU measurement setup with a bipolar trigger is introduced. With a bipolar trigger voltage source, this measurement setup can accurately simulate how a CMOS IC will be disturbed by the ESD-generated noises in the system-level ESD test. Thus, it can be used to evaluate the TLU immunity of CMOS ICs for system-level ESD considerations. Through investigating the influences of both the current-blocking diode and the current-limiting resistance on the TLU-triggering voltage waveform and TLU level, it has been demonstrated that a TLU measurement setup equipped with either a current-blocking diode or a current-limiting resistance will over-estimate the TLU level of CMOS ICs. However, a small current-limiting

resistance has no significant impact on the TLU level, and therefore the TLU measurement setup without a current-blocking diode but with a small current-limiting resistance (5 Ω) is suggested. This suggested TLU measurement setup has the advantages of accurately evaluating the TLU immunity of CMOS ICs without overestimation, as well as avoiding the EOS damage to the DUT during the TLU test. Such a TLU measurement setup can be widely utilized to evaluate the TLU immunity of CMOS ICs in practical field applications. Also, different types of board-level noise filter networks can be evaluated to find their effectiveness for improving the TLU immunity.

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4

TLU Dependency on Power-Pin Damping Frequency and Damping Factor in CMOS Integrated Circuits[1]

The sweep-back current, I_{Sb} [1, 2], has been proven to be the major cause of TLU in the system-level ESD test. Three dominant parameters to determine I_{Sb} are D_{Freq}, D_{Factor}, and $+V_{Peak}$ $(-V_{Peak})$. Thus, it's important to investigate the TLU dependency on D_{Freq}, D_{Factor}, and $+V_{Peak}$ $(-V_{Peak})$. In real situations, these three parameters depend on the charged voltage of the ESD gun, the adopted TLU test mode, and the board-level noise-decoupling filters, and so on. Furthermore, the board-level transient voltage coupled into chips also strongly depends on the parasitic capacitance, inductance, and resistance of metal traces in board-/chip-level layout. Thus, the occurrence of TLU strongly depends on these three parameters. It is straightforward that a larger voltage amplitude of $+V_{Peak}$ $(-V_{Peak})$ (that is, larger transient noises) can initiate TLU more easily. However, it is not so clear how D_{Freq} and D_{Factor} affect the TLU immunity of the CMOS ICs in the system-level ESD test. In this chapter, the TLU dependency on both D_{Freq} and D_{Factor} can be well explained in the time domain by device simulation. Based on the comprehensive simulation results, board-level noise filters can be properly developed to efficiently eliminate the ESD-coupled noises for TLU prevention.

Nomenclature

D_{Freq} Damping frequency of bipolar trigger voltage on the power pins of CMOS ICs.

[1] © 2007 IEEE. 4.1–4.3 and part of 4.4 reprinted, with permission, from Sheng-Fu Hsu and Ming-Dou Ker, Transient-induced latchup dependence on power-pin damping frequency and damping factor in CMOS integrated circuits (abstract-section IV and figures 2, 3, 7–11, and 14–16), in *IEEE Transactions on Electron Devices*, Vol. 54, no. 8, pp. 2002–2010, Aug. 2007. IEEE, Piscataway, NJ.

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D_{Factor} Damping factor of bipolar trigger voltage on the power pins of CMOS ICs.
$+V_{\text{Peak}}$ Transient positive peak voltage of bipolar trigger voltage on the power pins of CMOS ICs.
$+I_{\text{Peak}}$ Transient positive peak current of bipolar trigger voltage on the power pins of CMOS ICs.
$-V_{\text{Peak}}$ Transient negative peak voltage of bipolar trigger voltage on the power pins of CMOS ICs.
$-I_{\text{Peak}}$ Transient negative peak current of bipolar trigger voltage on the power pins of CMOS ICs.
I_{Sb} Sweep-back current caused by the bipolar trigger voltage on the power pins of CMOS ICs.
D Distance between well-edge and well (substrate) contact in the PNPN latchup path.
S Distance between anode and cathode in the PNPN latchup path.
W Distance between the two adjacent well (substrate) contacts in the PNPN latchup path.
$V_{\text{DD}}(t)$ Time-dependent voltage function used in device simulation to simulate the bipolar trigger voltage on the power pins of CMOS ICs.

$$V_{DD}(t) = V_0 + V_P \cdot \exp\left(-(t - t_{\text{d}})D_{\text{Factor}}\right) \cdot \sin(2\pi D_{\text{Freq}}(t - t_{\text{d}})) \qquad (4.1)$$

where V_0 is the initial voltage, t_{d} is the time delay, and V_{P} is the applied voltage amplitude.

I_{Ds} Transient displacement current of P/N junction.
$V_{\text{P}+}$ Magnitude of minimum positive V_{P} to initiate TLU.
$V_{\text{P}-}$ Magnitude of minimum negative V_{P} to initiate TLU.
t_{P} Time period needed for V_{DD} increasing from $-V_{\text{Peak}}$ to the normal circuit operating voltage.
$D_{\text{Freq(min)}}$ Minimum D_{Freq} to initiate TLU.
$D_{\text{Freq(max)}}$ Maximum D_{Freq} to initiate TLU.
V_{Charge} Applied voltage on charged capacitor (200 pF) in the component-level TLU measurement setup.
f_{SR} Self-resonant frequency.

4.1 Examples of Different D_{Freq} and D_{Factor} in the System-Level ESD Test

The measurement setup of the system-level ESD test with an indirect contact-discharge test mode [3] is shown in Figure 2.2. Without board-level noise filters to help suppress ESD-induced transient noises, the measured V_{DD} transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT with an ESD voltage of $+1000$ V discharging on the HCP is shown in Figure 4.1. During the system-level ESD test, D_{Freq}, D_{Factor}, and $+V_{\text{Peak}}$ ($-V_{\text{Peak}}$) depend on many factors. Specifically, the board-level noise-decoupling filter is a dominant factor to determine these parameters. To clarify this issue, a decoupling capacitance of 1 nF is added between V_{DD}

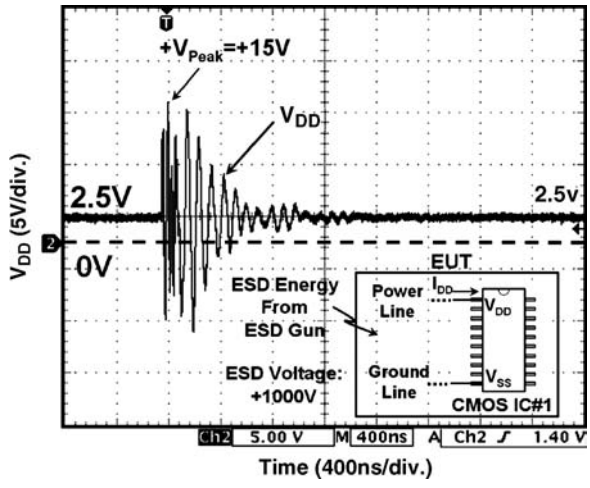


Figure 4.1 With an ESD voltage of $+1000$ V discharging on the HCP, the measured V_{DD} transient waveform on one (CMOS IC#1) of the CMOS ICs inside the EUT. The V_{DD} waveform is a bipolar voltage due to the disturbance of high ESD-coupled energy. (Reprinted with permission from IEEE).

and V_{SS} (ground) of the CMOS IC#1. With an ESD voltage of $+1000$ V discharging on the HCP, the measured V_{DD} transient waveform is shown in Figure 4.2. Compared with the original V_{DD} transient waveform in Figure 4.1, D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) are all different in Figure 4.2. Furthermore, with a resistor-type ferrite bead (minimum impedance of 80 Ω at 25 MHz) in series with the V_{DD} pin of the CMOS IC#1, the measured V_{DD} transient waveform with an ESD voltage of $+1000$ V dicharging on the HCP is shown in Figure 4.3. Clearly, D_{Factor} is larger than that of the original V_{DD} waveform in Figure 4.1, because the ferrite bead can absorb RF energy while the ESD-induced transient current flows through it. Without any board-level noise-decoupling filter on CMOS IC#1, the measured V_{DD} transient waveform with a higher ESD voltage of $+2000$ V discharging on the HCP is shown in Figure 4.4. The $+V_{Peak}$ of $+30$ V doubles that ($+15$ V) in Figure 4.1 (ESD discharging voltage of $+1000$ V), and so the V_{DD} peak voltage is proportional to the ESD discharging voltage. As a result, D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) could be different in each case, thus strongly dominating the occurrence of TLU in the system-level ESD test.

To clarify this issue, with an ESD voltage of $+3000$ V discharging on the HCP, the measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 are shown in Figure 4.5. With a large transient peak voltage of ± 50 V, TLU is triggered on with instantaneously increasing I_{DD}. After the ESD-induced disturbance on V_{DD}, I_{DD} is kept at a high current of 80 mA, while V_{DD} is pulled down to the latchup holding voltage of 1.8 V. If an additional decoupling capacitance of 0.1 μF is added between V_{DD} and V_{SS} (ground) of this TLU-sensitive CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with an ESD voltage of $+3000$ V discharging on the HCP are shown in Figure 4.6.

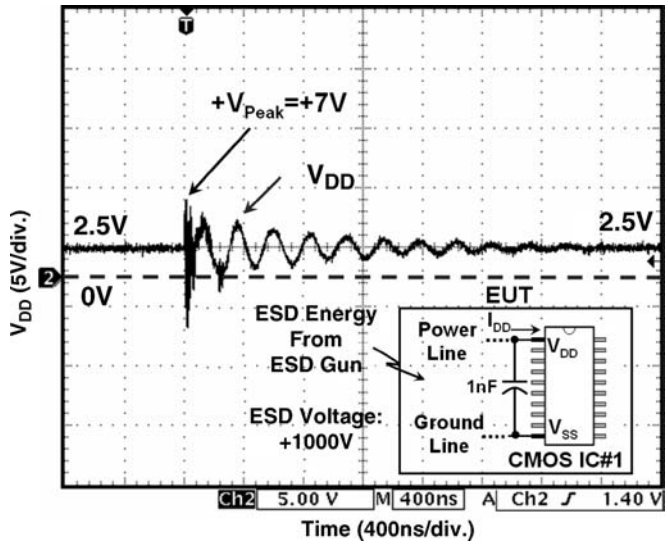


Figure 4.2 With an additional decoupling capacitance of 1 nF between V_{DD} and V_{SS} (ground) of the CMOS IC#1, the measured V_{DD} transient waveform with an ESD voltage of $+1000$ V discharging on the HCP. Compared with the original V_{DD} transient waveform in Figure 4.1, D_{Freq}, D_{Factor}, and $+V_{Peak}$ are all different.

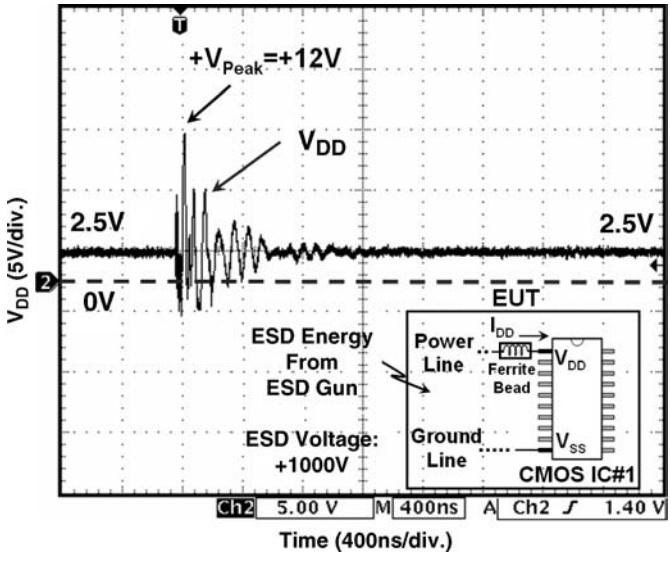


Figure 4.3 With a resistor-type ferrite bead (minimum impedance of 80 Ω at 25 MHz) in series with the V_{DD} pin of the CMOS IC#1, the measured V_{DD} transient waveform with an ESD voltage of $+1000$ V discharging on the HCP. The D_{Factor} is larger than that of the original V_{DD} waveform in Figure 4.1.

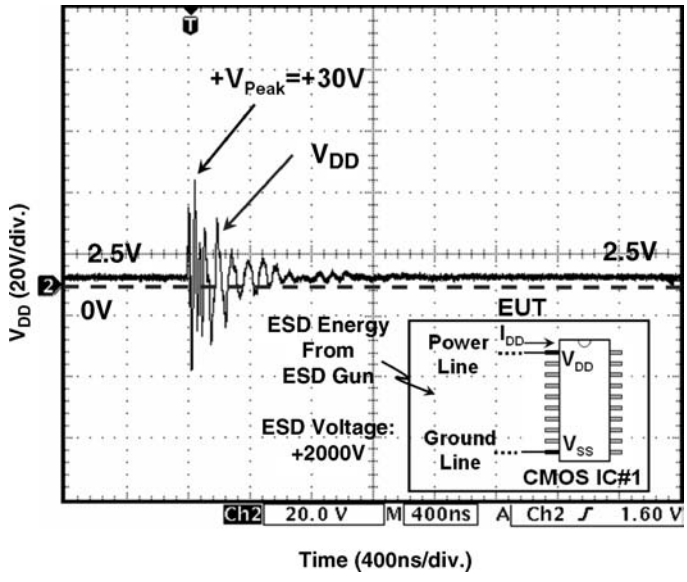


Figure 4.4 Without any board-level noise-decoupling filter on CMOS IC#1, the measured V_{DD} transient waveform with a higher ESD voltage of $+2000$ V discharging on the HCP. The $+V_{Peak}$ of $+30$ V doubles that ($+15$ V) in Figure 4.1 with a smaller ESD voltage of $+1000$ V.

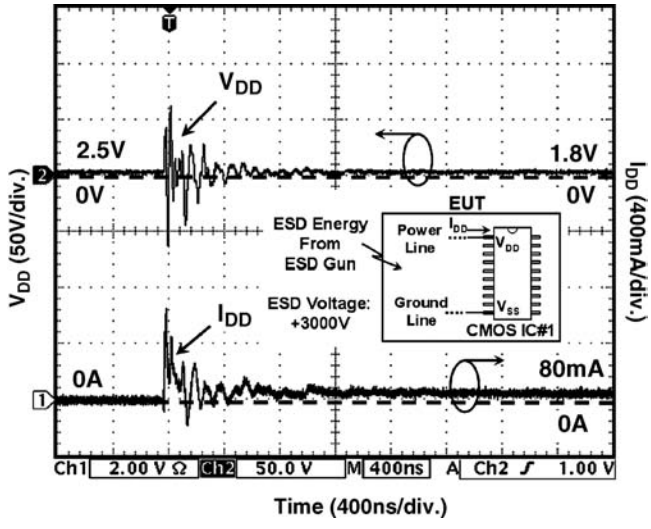


Figure 4.5 Measured V_{DD} and I_{DD} transient waveforms on CMOS IC#1 with an ESD voltage of $+3000$ V discharging on the HCP. With a large transient peak voltage of ± 50 V, TLU is triggered on (I_{DD} is kept at a high current of 80 mA) after the ESD-induced disturbance on V_{DD}. (Reprinted with permission from IEEE).

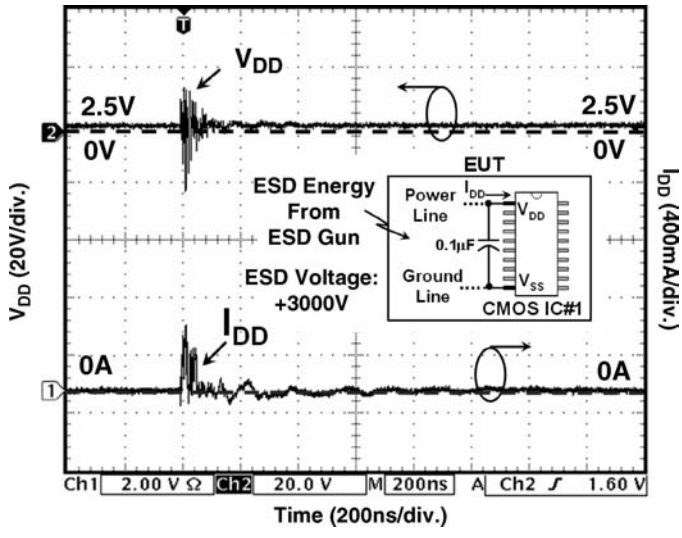


Figure 4.6 With the decoupling capacitance of 0.1 μF between V_{DD} and V_{SS} of the CMOS IC#1, the measured V_{DD} and I_{DD} transient waveforms with an ESD voltage of $+3000$ V discharging on the HCP. TLU does not occur due to different D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$). (Reprinted with permission from IEEE).

Compared with the V_{DD} waveforms in Figure 4.5 where no decoupling capacitance is used for suppressing the ESD-induced noise, D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) are all different in Figure 4.6. As a result, TLU does not occur, and I_{DD} doesn't increase after the ESD-induced disturbance on V_{DD}. Thus, the occurrence of TLU strongly depends on D_{Freq}, D_{Factor}, and $+V_{Peak}$ ($-V_{Peak}$) of the bipolar trigger waveforms on the power pins of CMOS ICs. The board-level noise filters dominate these parameters, which have strong impacts on TLU immunity.

4.2 TLU Dependency on D_{Freq} and D_{Factor}

A two-dimensional device simulation tool (MEDICI) is used to characterize the TLU dependency on both D_{Freq} and D_{Factor}. The SCR structure with the specified layout parameters of $D = 6.7$ μm and $S = 1.2$ μm is used for all the TLU device simulations in this chapter, as shown in Figure 2.5.

4.2.1 Relations between D_{Factor} *and Minimum Positive (Negative)* V_P *to Initiate TLU*

With a fixed D_{Freq} of 8 MHz, the relations between D_{Factor} and V_{P+} (V_{P-}) are shown in Figure 4.7a. V_{P+} (V_{P-}) is defined as the magnitude of minimum positive (negative) V_P to initiate TLU. The latter cannot be initiated if the magnitude of the applied positive

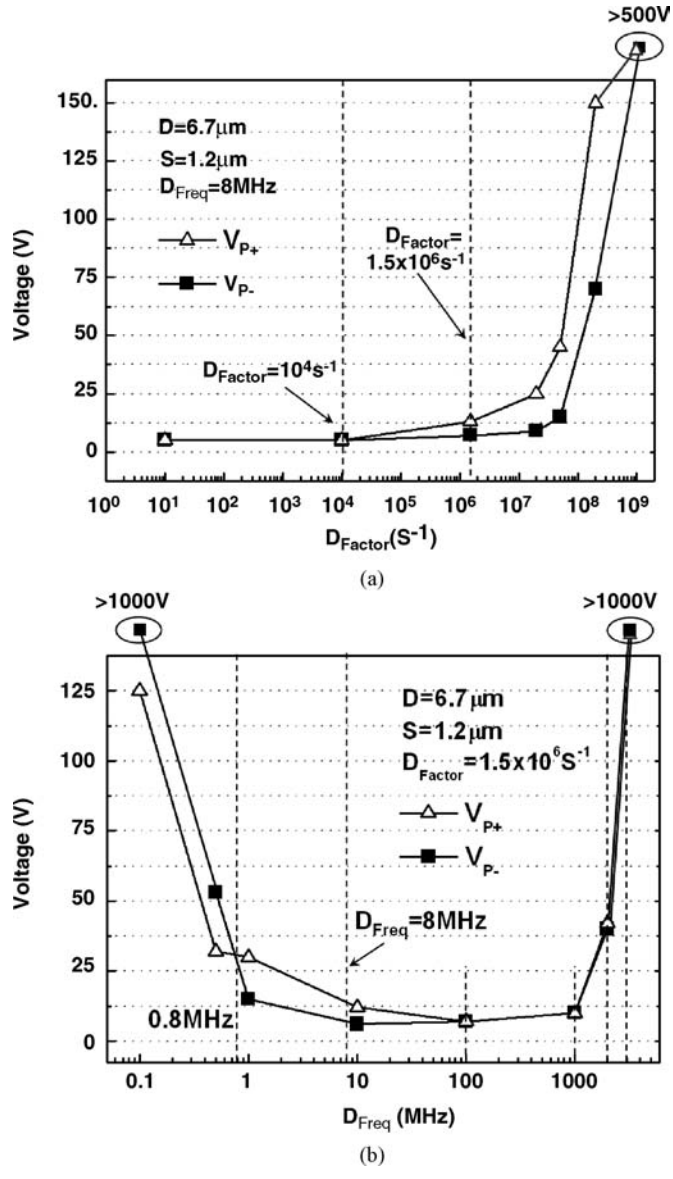


Figure 4.7 Relations between (a) D_{Factor} and $V_{\text{P}+}$ ($V_{\text{P}-}$), and (b) D_{Freq} and $V_{\text{P}+}$ ($V_{\text{P}-}$). $V_{\text{P}+}$ ($V_{\text{P}-}$) is defined as the magnitude of minimum positive (negative) V_{P} to initiate TLU. (Reprinted with permission from IEEE).

(negative) V_{P} is smaller than $V_{\text{P}+}$ ($V_{\text{P}-}$), because a too small V_{P} cannot provide a large enough $-V_{\text{Peak}}$ (that is, large enough I_{Sb}) to initiate TLU. In addition, because the D_{Factor} determines how fast the bipolar trigger voltage will be attenuated in the time domain, so the magnitude of $-V_{\text{Peak}}$ strongly depends on D_{Factor}. For example,

a larger D_{Factor} causes larger voltage attenuation within the first cycle of the bipolar trigger waveform (that is, smaller $-V_{\text{Peak}}$ or I_{Sb}). Thus, the relations between D_{Factor} and $V_{\text{P}+}$ ($V_{\text{P}-}$) are very important for TLU characterization.

For a $D_{\text{Factor}} < 10^4\ \text{s}^{-1}$, both $V_{\text{P}+}$ and $V_{\text{P}-}$ are independent of the D_{Factor} and equal to 6 V. From Equation (4.1), for the given D_{Freq} of 8 MHz, such a small D_{Factor} will not result in an obvious voltage attenuation within the first cycle of the bipolar trigger waveform (that is, $-V_{\text{Peak}}$ isn't obviously attenuated). Thus, for such a small D_{Factor}, if a known minimum $-V_{\text{Peak}}$ to initiate TLU is fixed, both $V_{\text{P}+}$ and $V_{\text{P}-}$ are the same and independent of the D_{Factor}.

For a $D_{\text{Factor}} > 10^4\ \text{s}^{-1}$, both $V_{\text{P}+}$ and $V_{\text{P}-}$ increase with the D_{Factor}. A larger D_{Factor} will result in a larger voltage attenuation (that is, smaller $-V_{\text{Peak}}$) within the first cycle of the bipolar trigger waveform, and so a larger $V_{\text{P}+}$ ($V_{\text{P}-}$) is necessary for a larger D_{Factor} to provide a known fixed $-V_{\text{Peak}}$ (that is, fixed I_{Sb}) which can initiate TLU. Compared with the negative-going ($V_{\text{P}} < 0$) bipolar voltage, the positive-going ($V_{\text{P}} > 0$) bipolar voltage needs to take an additional half duration for decaying before reaching $-V_{\text{Peak}}$. As a result, a $V_{\text{P}+}$ larger than $V_{\text{P}-}$ is necessary to compensate this additional voltage attenuation within the half duration.

4.2.2 Relations between D_{Freq} *and Minimum Positive (Negative)* V_{P} *to Initiate TLU*

With a fixed D_{Factor} of $1.5 \times 10^6\ \text{s}^{-1}$, the relations between D_{Freq} and $V_{\text{P}+}$ ($V_{\text{P}-}$) are shown in Figure 4.7b. D_{Freq} is inversely proportional to the duration of the bipolar trigger waveform. Thus, D_{Freq} determines how fast the bipolar trigger waveform will be attenuated within its first duration (cycle). For example, for a fixed V_{P} and D_{Factor}, a higher D_{Freq} (shorter duration) means that the bipolar trigger voltage takes less time for decaying before reaching $-V_{\text{Peak}}$ (that is, larger $-V_{\text{Peak}}$). Thus, $-V_{\text{Peak}}$ (I_{Sb}) strongly depends on D_{Freq}, and the relations between D_{Freq} and $V_{\text{P}+}$ ($V_{\text{P}-}$) are significant for TLU characterization.

For $0.8\ \text{MHz} < \mathrm{D}_{\text{Freq}} < 100\ \text{MHz}$, $V_{\text{P}+}$ is larger than $V_{\text{P}-}$ because the positive-going bipolar voltage must take an additional half duration for decaying before reaching $-V_{\text{Peak}}$. Thus, if the minimum $-V_{\text{Peak}}$ to initiate TLU is fixed, a $V_{\text{P}+}$ larger than $V_{\text{P}-}$ is needed to compensate the additional voltage attenuation within the half duration.

For a $D_{\text{Freq}} < 0.8$ MHz, however, $V_{\text{P}+}$ is smaller than $V_{\text{P}-}$. For the $V_{\text{P}-}$ case, Figure 4.8 shows the simulated V_{DD} and I_{DD} transient responses for a bipolar trigger with D_{Factor}, D_{Freq}, and V_{P} of $1.5 \times 10^6\ \text{s}^{-1}$, 0.1 MHz, and -200 V, respectively. Clearly, the given D_{Factor} of $1.5 \times 10^6\ \text{s}^{-1}$ is too large for such a low-frequency bipolar trigger to perform a negative-going bipolar voltage, but a negative-going unipolar overdamped voltage instead. TLU doesn't occur because t_{P} is too long ($\sim 3\ \mu\text{s}$) to generate sufficient I_{Sb} [1, 2], even though the magnitude of $-V_{\text{Peak}}$ is as high as 28 V. For the $V_{\text{P}+}$ case, Figure 4.9 shows the simulated V_{DD} and I_{DD} transient responses for a bipolar trigger with the same parameters as those in Figure 4.8 but with a V_{P} of

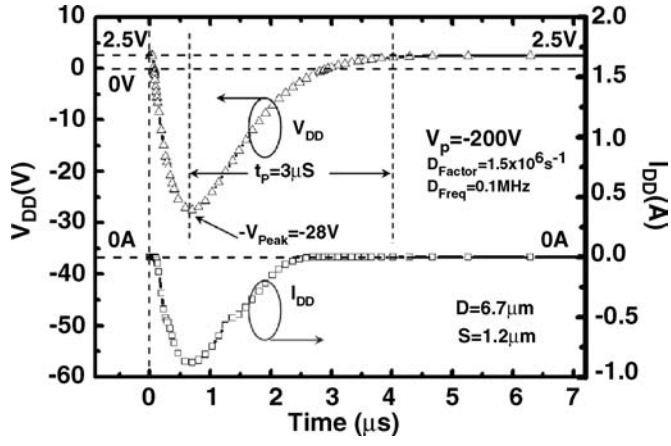


Figure 4.8 Simulated V_{DD} and I_{DD} transient responses for a bipolar trigger voltage with D_{Factor}, D_{Freq}, and V_P of $1.5 \times 10^6\,s^{-1}$, 0.1 MHz, and -200 V, respectively. TLU doesn't occur because t_P is too long ($\sim$3 μs) to generate sufficient I_{Sb}. (Reprinted with permission from IEEE).

$+150$ V. Similarly, a positive-going unipolar overdamped voltage is formed due to the given large D_{Factor}. However, TLU could be initiated by the I_{Ds} while V_{DD} initially increases from the normal operating voltage ($+2.5$ V) to $+V_{Peak}$, even though the magnitudes of both V_P and $+V_{Peak}$ (150 V and 25 V) are smaller than those (200 V and 28 V) in Figure 4.8. Two different TLU-triggering currents have been mentioned: I_{Ds} [4] and I_{Sb} [1, 2]. I_{Ds} results from a rapid increase of V_{DD} with time (for example, power-on transition or V_{DD} overshooting), and it's proportional to the junction

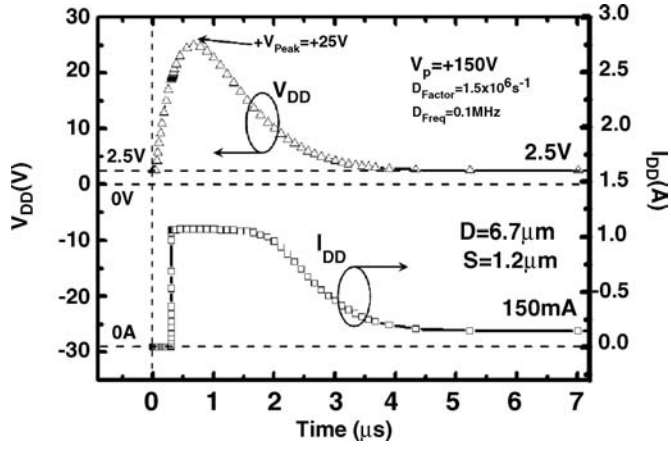


Figure 4.9 Simulated V_{DD} and I_{DD} transient responses for a bipolar trigger voltage with the same parameters as those in Figure 4.8 but with a V_P of $+150$ V. TLU can be triggered on by I_{Ds} while V_{DD} initially increases from the normal operating voltage ($+2.5$ V) to $+V_{Peak}$. (Reprinted with permission from IEEE).

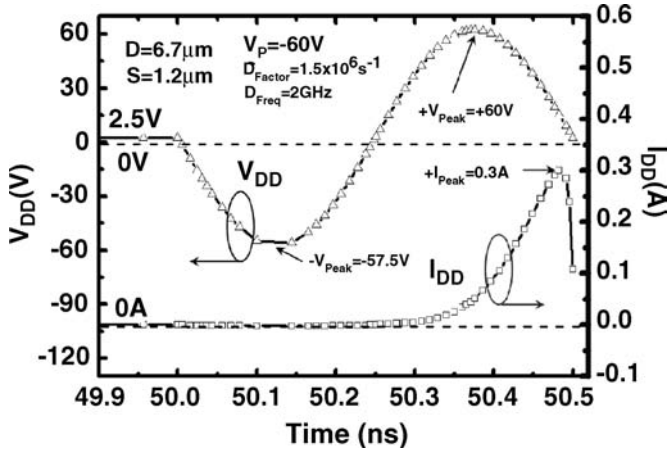


Figure 4.10 Simulated V_{DD} and I_{DD} transient responses for a bipolar trigger voltage with D_{Factor}, D_{Freq}, and V_P of $1.5 \times 10^6\,s^{-1}$, 2 GHz, and -60 V, respectively. I_{DD} cannot follow the V_{DD} variation in time for such a high D_{Freq} (>1 GHz) bipolar trigger, because the $+I_{Peak}$ doesn't simultaneously appear with the $+V_{Peak}$ but at the end of the first duration ($\sim$50.5 ns). (Reprinted with permission from IEEE).

capacitance. I_{Sb} results from V_{DD} switching from a negative voltage level to a positive voltage level (for example, bipolar transient noises on V_{DD}), and it correlates closely with D_{Freq}, D_{Factor}, and $-V_{Peak}$. It has been clarified that I_{Sb} can initiate TLU more easily than I_{Ds} [5]. From the simulation results in Figures 4.8 and 4.9, however, I_{Ds} (Figure 4.9) can initiate TLU more easily than I_{Sb} (Figure 4.8) due to a very low D_{Freq}. A too low D_{Freq} will significantly reduce I_{Sb} because of a too long a t_P (for example, 3 μs in Figure 4.8).

For a $D_{Freq} > 1000$ MHz, both V_{P+} and V_{P-} significantly increase, as shown in Figure 4.7(b). Figure 4.10 shows the simulated V_{DD} and I_{DD} transient responses for a bipolar trigger with D_{Factor}, D_{Freq}, and V_P of $1.5 \times 10^6\,s^{-1}$, 2 GHz, and -60 V, respectively. Clearly, the $+I_{Peak}$ doesn't simultaneously appear with the $+V_{Peak}$ but at the end of the first duration ($\sim$50.5 ns), because I_{DD} cannot follow the V_{DD} variation in time for such a high-D_{Freq} (>1GHz) bipolar trigger. Thus, the $+I_{Peak}$ of 0.3A is smaller than that (0.75 A) under the low-D_{Freq} (20 MHz) case in Figure 2.14, even though the $+V_{Peak}$ of $+60$ V is much larger than that ($+7.5$ V) in Figure 2.14. This means that a larger V_{P+} or V_{P-} is necessary for such a high-D_{Freq} (>1GHz) bipolar trigger to provide a fixed I_{Sb} which can initiate TLU. If D_{Freq} further increases to above 3GHz, TLU doesn't occur (both V_{P+} and V_{P-} larger than 1000 V), because the duration of the bipolar trigger isn't long enough to sustain a positive-feedback latchup event [6].

4.2.3 Relations between D_{Factor} and Minimum (Maximum) D_{Freq} to Initiate TLU

With a fixed V_P of both $+15$ V and -15 V, the relations between D_{Factor} and $D_{Freq(min)}$ ($D_{Freq(max)}$) are shown in Figure 4.11a and b. $D_{Freq(min)}$ ($D_{Freq(max)}$) is defined as the

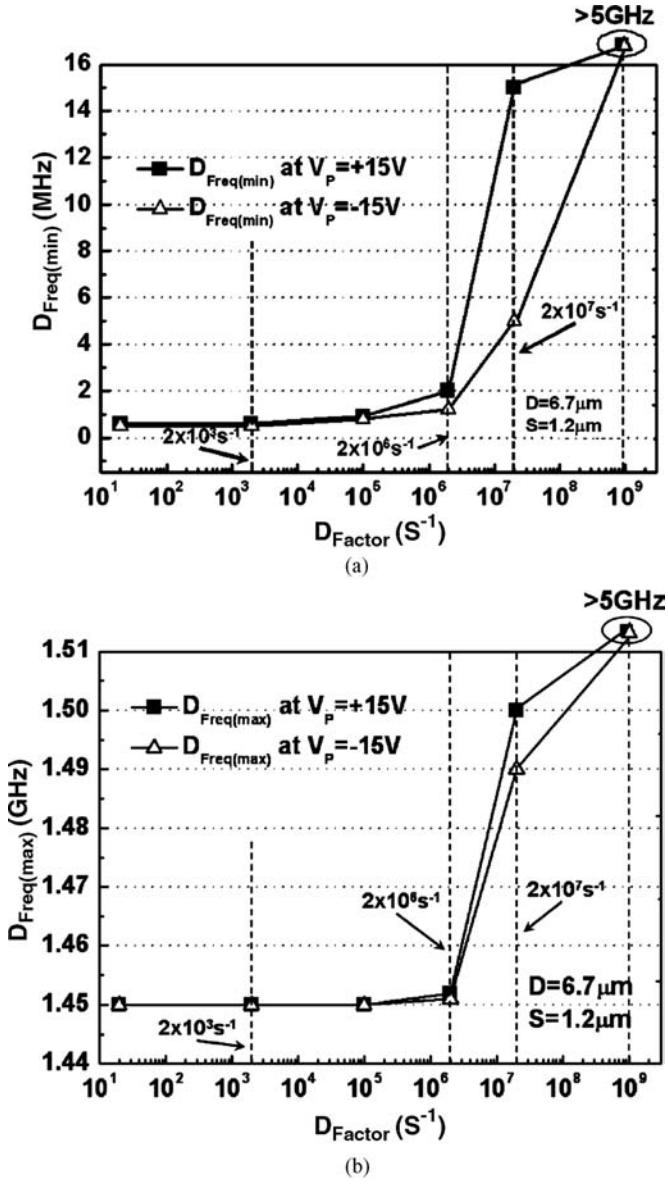


Figure 4.11 Relations between (a) D_{Factor} and $D_{\text{Freq(min)}}$, and (b) D_{Factor} and $D_{\text{Freq(max)}}$. $D_{\text{Freq(min)}}$ ($D_{\text{Freq(max)}}$) is defined as the minimum (maximum) D_{Freq} to initiate TLU under a fixed V_{P} of $+15$ V or -15 V. (Reprinted with permission from IEEE).

minimum (maximum) D_{Freq} to initiate TLU under a fixed V_{P} of $+15$ V or -15 V. A bipolar trigger with $D_{\text{Freq}} < D_{\text{Freq(min)}}$ ($D_{\text{Freq}} > D_{\text{Freq(max)}}$) cannot trigger TLU due to insufficient I_{Sb}. For D_{Freq} lower than $D_{\text{Freq(min)}}$, there is a too serious voltage attenuation on $-V_{\text{Peak}}$ (or a too long t_{P}) to produce sufficient I_{Sb} for initiating TLU.

For D_{Freq} higher than $D_{Freq(max)}$, I_{DD} cannot follow the V_{DD} variation in time to generate enough I_{Sb} for initiating TLU.

For a $D_{Factor} < 2 \times 10^3\ s^{-1}$ ($1 \times 10^5\ s^{-1}$), $D_{Freq(min)}$ ($D_{Freq(max)}$) is independent to D_{Factor} and equal to 500 kHz (1.45GHz). For such a small D_{Factor}, there is only little voltage attenuation within the first cycle of the bipolar trigger (that is, almost no voltage attenuation on $-V_{Peak}$). Thus, if a known minimum $-V_{Peak}$ to initiate TLU under a low- or high-D_{Freq} situation is fixed, both V_{P+} and V_{P-} are the same and independent of the D_{Factor}.

For a $D_{Factor} > 2 \times 10^3\ s^{-1}$ ($1 \times 10^5\ s^{-1}$), however, $D_{Freq(min)}$ ($D_{Freq(max)}$) increases with the D_{Factor}. A larger D_{Factor} will result in a larger voltage attenuation (that is, a smaller $-V_{Peak}$) within the first cycle of the bipolar trigger. Thus, to provide a known fixed $-V_{Peak}$ to initiate TLU, a higher $D_{Freq(min)}$ or $D_{Freq(max)}$ (that is, shorter duration) is necessary for a larger D_{Factor} bipolar trigger to compensate a larger voltage attenuation. In addition, there are higher $D_{Freq(min)}$ and $D_{Freq(max)}$ values under a V_P of $+15$ V. Compared with the negative-going bipolar trigger (V_P of -15 V), the positive-going bipolar trigger (V_P of $+15$ V) has a smaller $-V_{Peak}$ (smaller I_{Sb}) because it must take an additional half duration for decaying before reaching $-V_{Peak}$. Thus, a higher $D_{Freq(min)}$ or $D_{Freq(max)}$ is necessary for a positive-going bipolar voltage to initiate TLU.

From the above comprehensive simulation results, a bipolar trigger with a D_{Freq} of several tens of megahertz can initiate TLU most easily due to the smallest V_{P+} (V_{P-}) under 10 MHz $< D_{Freq} <$ 100 MHz, as shown in Figure 4.7b. Otherwise, TLU is less sensitive to a bipolar trigger with an excessively large D_{Factor} (Figure 4.7a), an excessively high D_{Freq} (Figure 4.7b), or an excessively low D_{Freq} (Figure 4.7b).

4.3 Experimental Verification on TLU

The component-level TLU measurement setup shown in Figure 2.7 is used for TLU measurements. As shown by the measurement results in Chapter 3, this proposed TLU measurement setup has a small current-limiting resistance (5 Ω) but no current-blocking diode between the V_{DD} node and the power supply. The device cross-sectional view and layout top view of the SCR test structure are illustrated in Figure 2.5a and b, respectively. The measured V_{DD} and I_{DD} transient responses with a V_{Charge} of $+10$ V and $+14$ V are shown in Figure 4.12a and b, respectively. With a smaller V_{Charge} of $+10$ V, V_{DD} is the intended bipolar trigger just similar to that in the system-level ESD test. In addition, TLU doesn't occur because I_{DD} doesn't increase after applying the bipolar trigger on V_{DD}, as shown in Figure 4.12a. TLU still doesn't occur until the V_{Charge} increases up to $+14$ V. Once TLU is initiated, I_{DD} significantly increases up to 120 mA, and V_{DD} is pulled down to the latchup holding voltage of 1.5 V, as shown in Figure 4.12b. The measured waveforms in Figure 4.12 can simulate the occurrence of TLU (the voltage disturbance on V_{DD}) in Figure 4.5 (Figure 4.1) in

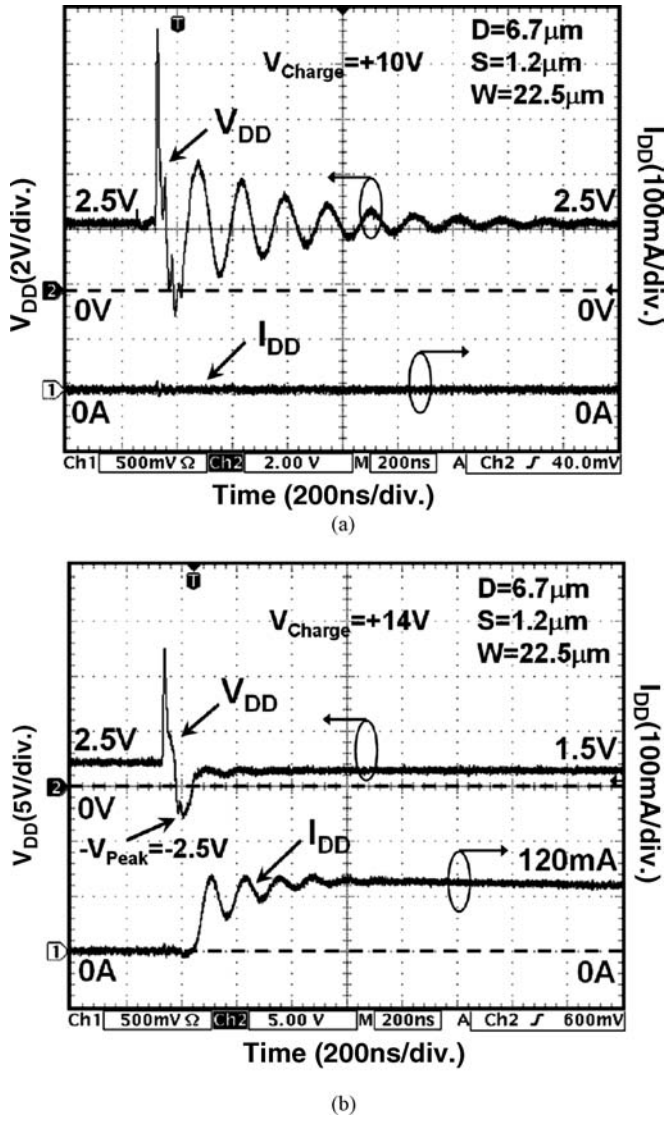
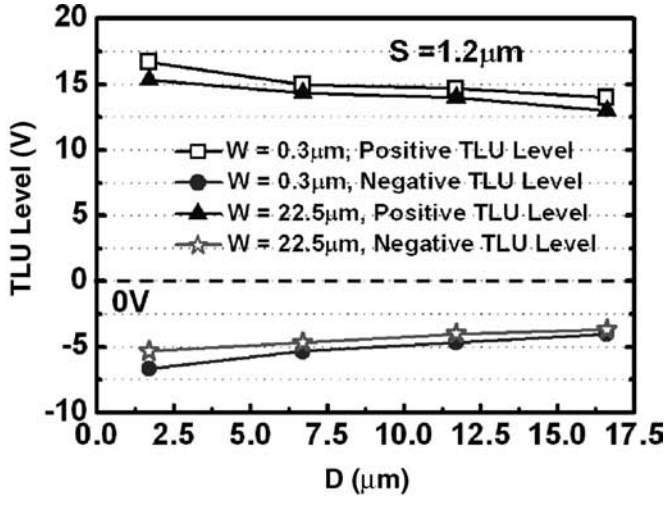


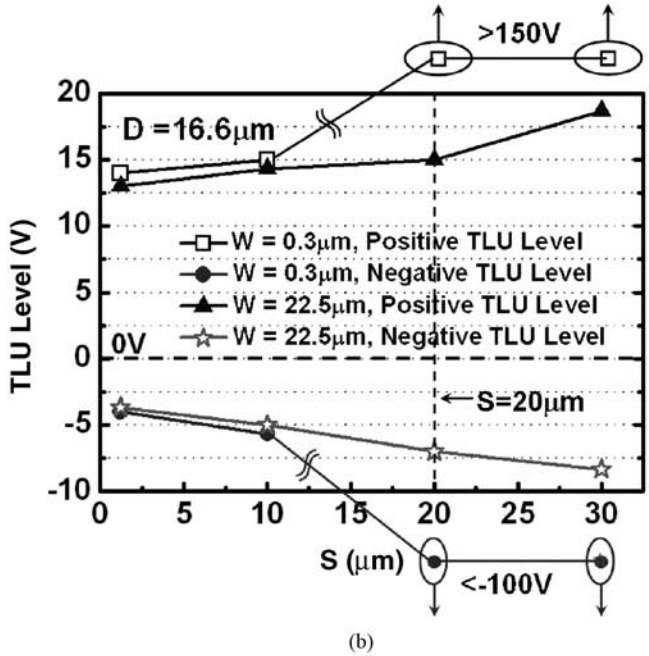
Figure 4.12 Measured V_{DD} and I_{DD} transient responses of the SCR with a V_{Charge} of (a) $+10$ V, and (b) $+14$ V. (Reprinted with permission from IEEE).

the system-level ESD test. Thus, this measurement setup can be used to evaluate the TLU dependency on D_{Factor} and D_{Freq} in the system-level ESD test.

The TLU levels of the fabricated SCR test devices with various geometrical parameters are shown in Figure 4.13. The TLU level is defined as the minimum positive (negative) V_{Charge} which can initiate TLU. The magnitudes of the negative TLU level (<9 V) of all the SCR structures are smaller than those of the positive TLU



(a)



(b)

Figure 4.13 Measured TLU level of the SCR structures with (a) various *D* and *W* values but a fixed *S* value of 1.2 μm, and (b) various *S* and *W* values but a fixed *D* value of 16.6 μm. The SCR structures are rather susceptible to TLU for all different geometrical parameters (the magnitudes of both positive and negative TLU levels are all smaller than 18 V) unless the SCR is latchup-free. (Reprinted with permission from IEEE).

level (>13 V), unless the SCR is initially latchup-free (that is, latchup holding voltage > +2.5 V). With the measured bipolar trigger waveform in Figure 4.12a, it can be extracted from Equation (4.1) that D_{Freq} is about 8 MHz (duration is about 125 ns), and D_{Factor} is about $1.5 \times 10^6\,\text{s}^{-1}$. From the simulation results in Figure 4.7a and b, V_{P-} is smaller than V_{P+} for a bipolar trigger with a D_{Freq} of 8 MHz and D_{Factor} of $1.5 \times 10^6\,\text{s}^{-1}$. Thus, the experimental verifications in Figure 4.13 are consistent with the device simulation results in Figure 4.7.

The simulated TLU characteristics in Figures 4.7 and 4.11 are explained with the assumption that the minimum $-V_{\text{Peak}}$ to initiate TLU is fixed for the same SCR structure. To experimentally verify this, a discharge resistor with resistance of 1.5 kΩ is placed between the relay and the V_{DD} node in the TLU measurement setup. Thus, another bipolar trigger with a higher D_{Freq} and a larger D_{Factor} can be generated. Figure 4.14a shows the measured V_{DD} and I_{DD} transient responses with a V_{Charge} of +120 V. Compared with the measured V_{DD} waveform in Figure 4.12a, a higher D_{Freq} of 12.5M Hz (larger D_{Factor} of $1.5 \times 10^7\,\text{s}^{-1}$) can be extracted from Equation (4.1). In addition, TLU doesn't occur due to a larger D_{Factor}, even though the V_{Charge} is as high as +120 V. If the V_{Charge} further increases, TLU still doesn't occur until the V_{Charge} increases up to +200 V. Figure 4.14b shows the measured V_{DD} and I_{DD} transient responses with a V_{Charge} of +200 V. In Figures 4.12b and 4.14b, the minimum $-V_{\text{Peak}}$ to initiate TLU is fixed (−2.5 V) for the same SCR structure ($D = 6.7\,\mu\text{m}$, $S = 1.2\,\mu\text{m}$, and $W = 22.5\,\mu\text{m}$), even though there are different D_{Freq} and D_{Factor} parameters. Based on this result, the simulated TLU characteristics in this chapter are indeed explained well with a reasonable assumption.

The simulated TLU characteristics in Figure 4.7a that V_{P+} increases with D_{Factor}, can be also experimentally verified by Figures 4.12b and 4.14b. For the bipolar trigger with a larger D_{Factor} in Figure 4.14b, in order to compensate larger voltage attenuation within the first cycle, a larger V_{Charge} (+200 V) is necessary to produce the same minimum $-V_{\text{Peak}}$ (−2.5 V) to initiate TLU. As a result, the positive TLU level of +200 V in Figure 4.14b is much larger than that of +14 V in Figure 4.12b, which is consistent with the simulation result in Figure 4.7a.

4.4 Suggested Guidelines for TLU Prevention[2]

To prevent the occurrence of TLU in CMOS ICs in the system-level ESD test, the most intuitional solution is to eliminate the ESD-coupled noises on the power lines of CMOS ICs. Usually, board-level noise filter is a common and efficient solution to decouple or bypass ESD-induced noises. Based on the comprehensive simulation results in this chapter, board-level noise filters can be properly developed to efficiently eliminate the ESD-coupled noises for TLU prevention.

[2] © 2006 IEEE. Part of 4.4 reprinted, with permission, from Ming-Dou Ker and Sheng-Fu Hsu, Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test, in *IEEE Transactions on Electromagnetic Compatibility*, Vol. 48, no. 1, pp. 161–171, Feb. 2006. IEEE, Piscataway, NJ.

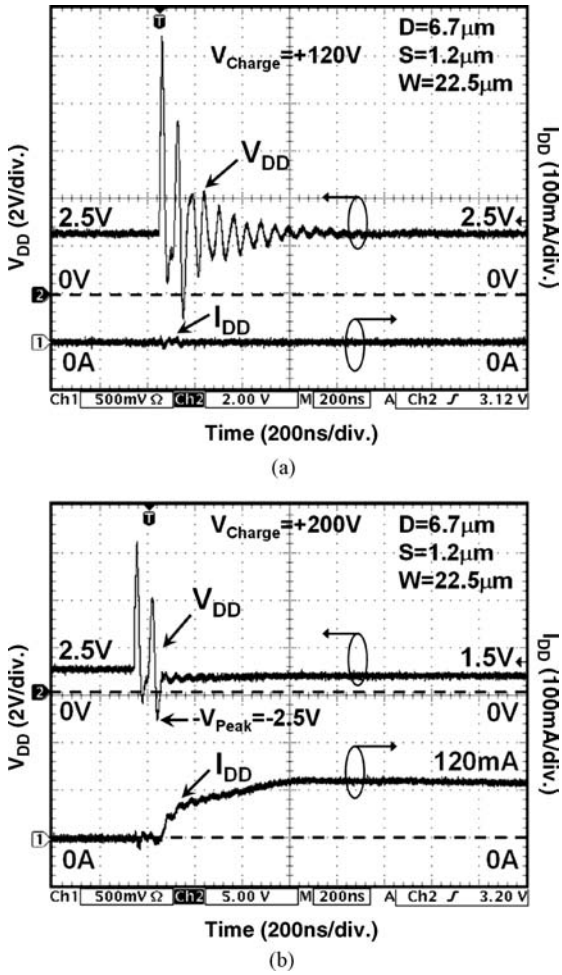


Figure 4.14 With a discharge resistor with a resistance of 1.5 kΩ between the relay and the V_{DD} node in the TLU measurement setup (Figure 2.7), the measured V_{DD} and I_{DD} transient responses with V_{Charge} of (a) + 120 V, and (b) + 200 V. In Figures 4.12b and 4.14b, the minimum $-V_{Peak}$ to initiate TLU is fixed (−2.5 V) for the same SCR structure ($D = 6.7\,\mu m$, $S = 1.2\,\mu m$, and $W = 22.5\,\mu m$). (Reprinted with permission from IEEE).

Figure 4.7a shows that increasing the D_{Factor} can enhance the TLU immunity of CMOS ICs. To achieve a larger D_{Factor}, a board-level noise filter with a higher insertion loss is necessary. Without any board-level noise filter (with a decoupling capacitance of 0.1 μF between V_{DD} and the ground lines) on the SCR, the measured V_{DD} and I_{DD} transient responses with a V_{Charge} of −7 V (−15 V) are shown in Figure 4.15a and b. Without any board-level noise filter, TLU occurs even if the V_{Charge} is as small as −7 V. With a decoupling capacitance, TLU doesn't occur due to a larger D_{Factor}, even though the V_{Charge} is as high as −15 V. However, an actual decoupling capacitor remains capacitive only up to its self-resonant frequency (f_{SR}) [7]. Above f_{SR}, the impedance of

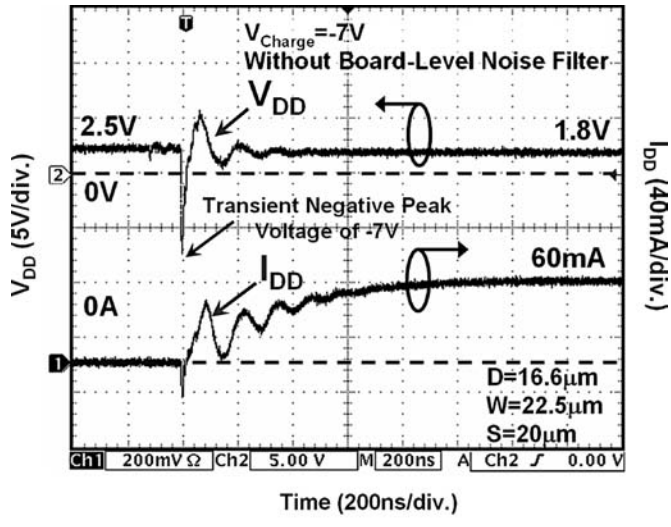


Figure 4.15 Measured V_{DD} and I_{DD} transient responses. (a) Without any board-level noise filters and a V_{Charge} of -7 V. (b) With an additional decoupling capacitance of 0.1 μF between V_{DD} and V_{SS} (ground) of the SCR, and a V_{Charge} of -15 V. (Reprinted with permission from IEEE).

the decoupling capacitance will increase with frequency (that is, inductive impedance characteristic). Thus, continually increasing the decoupling capacitance cannot efficiently enhance the TLU level of CMOS ICs, because f_{SR} is inversely proportional to the decoupling capacitance [7]. From Figure 4.7b, CMOS ICs are most sensitive to TLU over the frequency range of $10\,\text{MHz} < D_{Freq} < 100\,\text{MHz}$. Thus, a trade-off between a high insertion loss and a self-resonant frequency > 100 MHz is necessary to achieve the optimal decoupling capacitance for TLU prevention. For example,

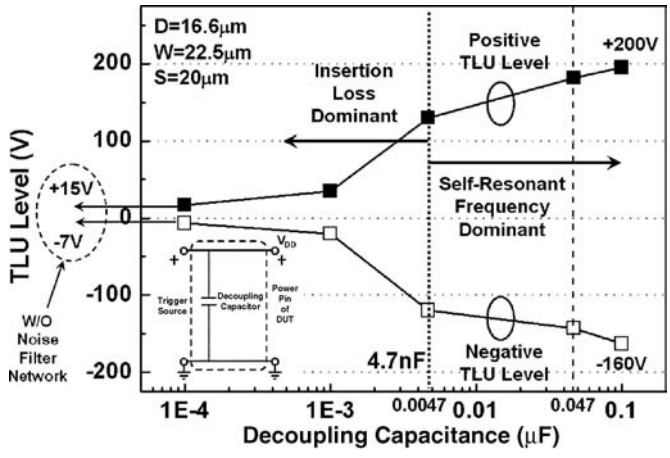


Figure 4.16 Relations between the decoupling capacitance and the TLU level of the SCR.

the relations between the decoupling capacitance and the TLU level of the SCR are shown in Figure 4.16 [8]. When the decoupling capacitance increases from 100 pF (f_{SR} of ~150 MHz) to 4.7 nF (f_{SR} of ~32 MHz), the TLU level will significantly increase with decoupling capacitance (insertion loss dominant). However, if the decoupling capacitance further increases from 4.7 nF (f_{SR} of ~32 MHz) to 0.1 μF (f_{SR} of ~5 MHz), the TLU level doesn't increase as significantly as that equipped with a decoupling capacitance < 4.7 nF (f_{SR} dominant). A too large decoupling capacitance cannot efficiently eliminate the TLU-sensitive harmonics (10 MHz < D_{Freq} < 100 MHz) due to a very low f_{SR}. Although the largest decoupling capacitance (0.1 μF) provides the highest TLU level (+ 200 V, −160 V), the optimal decoupling capacitance to enhance the TLU level is a smaller value of ~4.7 nF. Thus, instead of continuously increasing the decoupling capacitance of the first-order capacitor filter, it's suggested to use higher-order noise filters (for example, a third-order π-section filter [8]) based on the optimal decoupling capacitance (~4.7 nF) to further enhance the TLU level (> + 200 V).

4.5 Conclusion

To clarify the correlations between TLU and the bipolar trigger noises, two dominant parameters of the bipolar trigger – D_{Freq} and D_{Factor} – have been characterized to find their impacts on TLU. With the simulated TLU dependency on D_{Freq} and D_{Factor}, the bipolar trigger waveform with a D_{Freq} of several tens of megahertz can initiate TLU most easily. However, TLU is less sensitive to bipolar trigger waveforms with an excessively large D_{Factor}, an excessively high D_{Freq}, or an excessively low D_{Freq}. The simulated TLU characteristics are useful for optimizing a bipolar trigger to evaluate the TLU immunity of CMOS ICs without over-estimation. Furthermore,

the board-/chip-level noise filters can be properly designed to efficiently eliminate the ESD-coupled noises for TLU prevention.

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5

TLU in CMOS ICs in the Electrical Fast Transient Test

In the same way as the system-level ESD test, the electrical fast transient (EFT) test is also an important test standard to ensure that electrical products meet EMC regulations. TLU, however, is found to be easily initiated in CMOS ICs in the EFT test [1], even though the DUT has already passed component-level ESD specifications such as the human-body-model (HBM) of ± 2 kV, machine-model (MM) of ± 200 V, and charged-device-model (CDM) of ± 1 kV. This chapter focuses on TLU in the EFT test, including the introduction of the EFT test standard, the physical mechanism of TLU in the EFT test, and the effectiveness of the board-level noise filter for TLU prevention in the EFT tests.

5.1 Electrical Fast Transient Test

The IEC 61000-4-4 standard [2] defines immunity requirements and test methods for electronic equipment against repetitive fast transients. The repetitive EFT test is a test with bursts consisting of a number of fast pulses, coupled into the power supply, control, signal, and ground ports of electronic equipment. The characteristics of EFT tests are a high amplitude, short rise time, high repetition rate, and low energy of the transients. The EFT test is intended to demonstrate the immunity of electronic equipment to transient disturbances such as those originating from switching transients (interruption of inductive loads, relay contact bounce, etc.).

According to the IEC 61000-4-4 standard, the simplified circuit diagram of the EFT generator is shown in Figure 5.1. In particular, only the impedance matching resistor R_m (50 Ω) and the dc blocking capacitor C_d (10 nF) are fixed. The charging capacitor C_c is used to store the charging energy and R_c is the charging resistor. The resistor R_s is used to shape the pulse duration. The effective output impedance of the EFT generator is 50 Ω.

Transient-Induced Latchup in CMOS Integrated Circuits Ming-Dou Ker and Sheng-Fu Hsu
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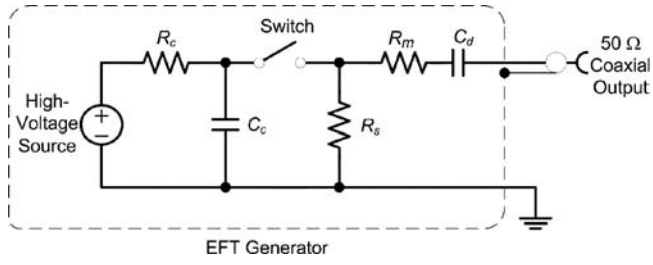


Figure 5.1 Simplified circuit diagram of an EFT generator [2].

The IEC 61000-4-4 standard defines the test voltage waveforms of these fast transients with repetition frequencies of 5 kHz and 100 kHz. A 5k Hz repetition rate is used in the traditional EFT test although 100 kHz is closer to reality. For an EFT pulse with a repetition frequency of 5 kHz, there are 75 pulses in each burst and the burst duration time is 15 ms. For an EFT pulse with a repetition frequency of 100 kHz, there are 75 pulses in each burst and the burst duration time is 0.75 ms. For both repetition rates, the burst repeats every 300 ms.

For EFT pulses with a repetition frequency of 5 kHz, the measured -200 V and $+200$ V voltage waveforms on the 50 Ω load are shown in Figure 5.2a and b. Due to the impedance matching, the measured pulse peak is half of the input EFT pulse voltage. As shown in Figure 5.2a and b, the measured output pulse peaks on the 50 Ω load are -100 V and $+100$ V, respectively. For an EFT repetition frequency of 5 kHz, the time interval between each pulse is 0.2 ms. Under the EFT tests, the application time should not be less than 1 min and both polarities have to be tested. The minimum start values of the pulse peak are ± 200 V from the EFT tester. With a 50 Ω load, the voltage waveforms of a single pulse with an EFT voltage of -200 V and $+200$ V are shown in Figure 5.3a and b, respectively. In Figure 5.3a and b, the waveform of a single pulse has a rise time of about 5 ns and the pulse duration (time interval at half of the peak EFT voltage) of 50 ns.

The EFT test levels for the power supply ports and for I/O, data, and control ports of the equipment are listed in Table 5.1. The voltage peak for testing I/O, data, and the control ports is half of the voltage peak for testing the power supply ports. The repetition rate is determined by specific products or product types. Level "X" is an open level which can be defined by the user. Level "X" is specified in the dedicated equipment specification. The output EFT voltage peak values are listed in Table 5.2. With an output load of 1000 Ω, the measured output voltage peak is equal to the open-circuit voltage peak multiplied by times 1000/1050 (the ratio of the 1000 Ω test load to the total circuit impedance of 1000 Ω plus 50 Ω). With an output load of 50 Ω, the measured output voltage is half of the value with an open-circuit load due to impedance matching.

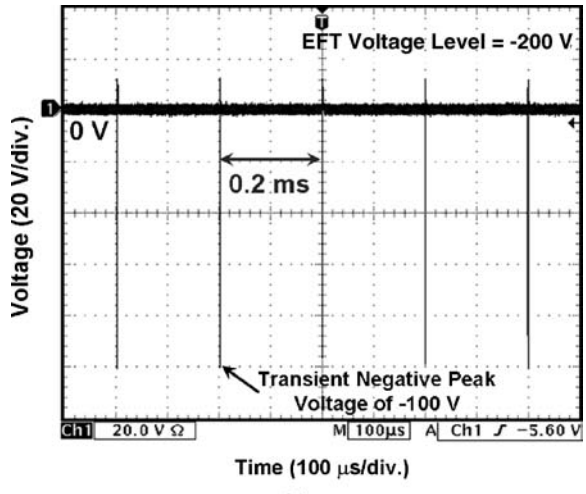
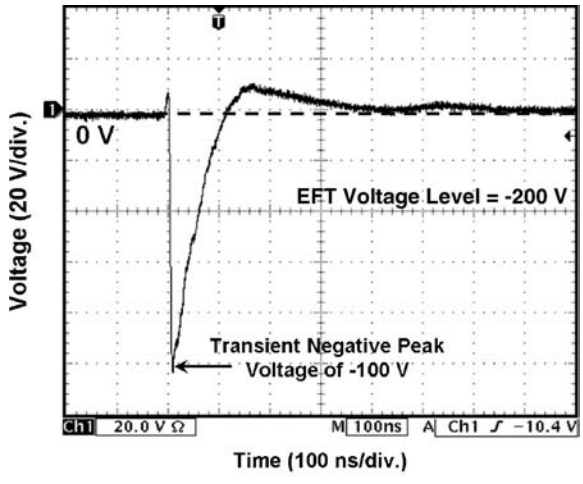
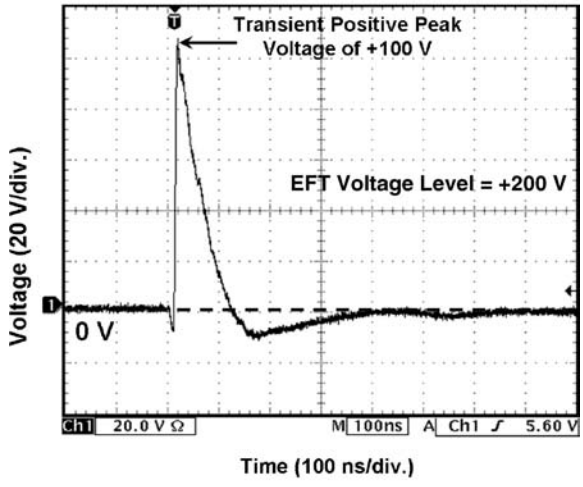


Figure 5.2 Measured voltage waveforms under a 50 Ω load in EFT tests with a repetition rate of 5 kHz and an EFT voltage of (a) −200 V and (b) + 200 V.

Because of the high-amplitude and fast-rise-time EFT pulses, TLU could be easily initiated in CMOS ICs. Emission microscope (EMMI) photographs of EFT-induced TLU in 0.5-µm CMOS ICs (VDD = 5 V) are shown in Figure 5.4. The photographs show the hot spot induced by a large leakage current is located between the PMOS and NMOS across the N-well/P-substrate boundary. This clearly indicates the occurrence of EFT-induced TLU, and the resulting latchup current flows through the parasitic SCR



(a)



(b)

Figure 5.3 Measured voltage waveforms of a single pulse under a 50 Ω load in EFT tests with an EFT voltage of (a) −200 V and (b) +200 V.

path from the P+ source tied to VDD in the PMOS, to the N+ source tied to the GND in the NMOS.

5.2 Test Structure

The SCR structure is used as the test structure for TLU measurements in EFT tests because the occurrence of latchup results from the inherent SCR in CMOS ICs. The device cross-sectional view and layout top view of the SCR structure are illustrated in

Table 5.1 EFT test levels.

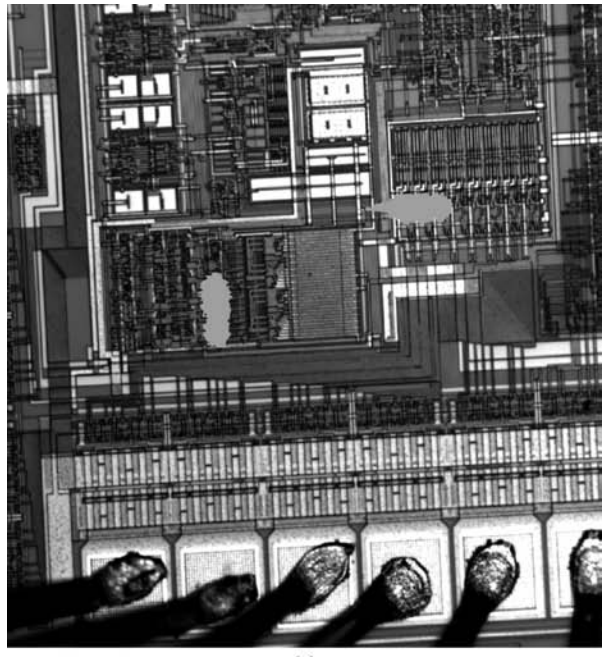
Level	On power and PE (protective earth) ports		On I/O (input/output) signal, data and control ports	
	Voltage peak (kV)	Repetition rate (kHz)	Voltage peak (kV)	Repetition rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X	Special	Special	Special	Special

Table 5.2 Output voltage peak (V_P) values and repetition rates.

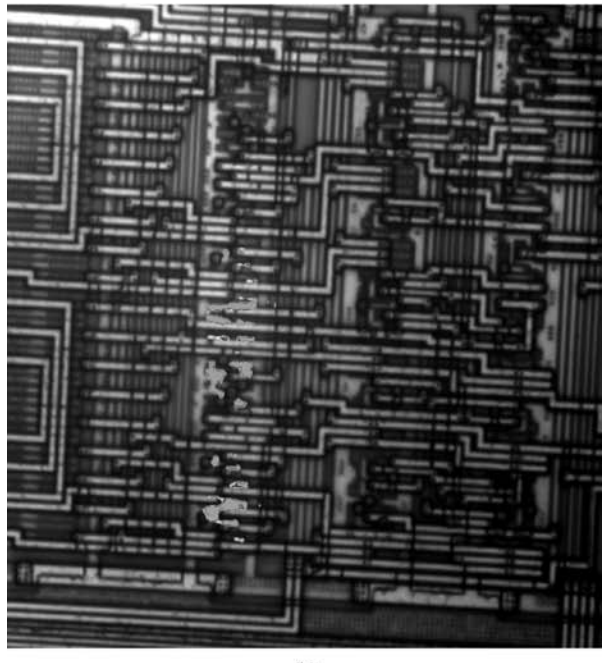
Set voltage (kV)	V_P (open circuit) (kV)	V_P (1000 Ω) (kV)	V_P (50 Ω) (kV)	Repetition rate (kHz)
0.25	0.25	0.24	0.125	5 or 100
0.5	0.5	0.48	0.25	5 or 100
1	1	0.95	0.5	5 or 100
2	2	1.9	1	5 or 100
4	4	3.8	2	5 or 100

Figure 5.5a and b, respectively. The anode of the SCR is connected to the N+ and P+ diffusions in the N-well, whereas the cathode of the SCR is connected to the N+ and P+ diffusions in the P-well. The geometrical parameters such as S_A, S_C, and S_{AC} represent the distances between the P+ diffusions in the N-well, the P+ and N+ diffusions in the P-well, and the P+ diffusion in the N-well and the N+ diffusion in the P-well, respectively. The SCR structure with $S_A = 29.12\,\mu m$, $S_C = 14.25\,\mu m$, and $S_{AC} = 4\,\mu m$ in a 0.18-μm 3.3 V CMOS process is used for the TLU measurements. Once latchup occurs through the SCR structure, a huge current will be generated by the mechanism of positive-feedback regeneration. As a result, a huge current will conduct through the low-impedance path from V_{DD} to ground, and further probably burn out the chip due to excess heat.

The equivalent circuit schematic of the SCR structure is shown in Figure 5.6a. The SCR structure consists of a lateral NPN BJT (Q_{NPN}) and a vertical PNP BJT (Q_{PNP}) to form a 2-terminal/4-layer PNPN (P+/N-well/P-well/N+) structure. The switching voltage of the SCR device is dominated by the avalanche breakdown voltage of the N-well/P-well junction, which could be as high as ~19 V in a 0.18-μm CMOS process. When the positive voltage applied to the anode of the SCR is greater than the breakdown voltage of the N-well/P-well junction with its cathode relatively grounded, the hole and electron currents will be generated through the avalanche breakdown mechanism. The hole current will flow through the P-well to the grounded P+ diffusion, whereas the electron current will flow through the N-well to N+ diffusion connected to the anode of SCR. As long as the voltage drop across the P-well resistor



(a)



(b)

Figure 5.4 Emission microscope (EMMI) photographs of EFT-induced TLU in 0.5-μm CMOS ICs (VDD = 5 V). (a) Hot spot (magnification, 100×), and (b) the corresponding zoom-in picture (magnification, 200×).

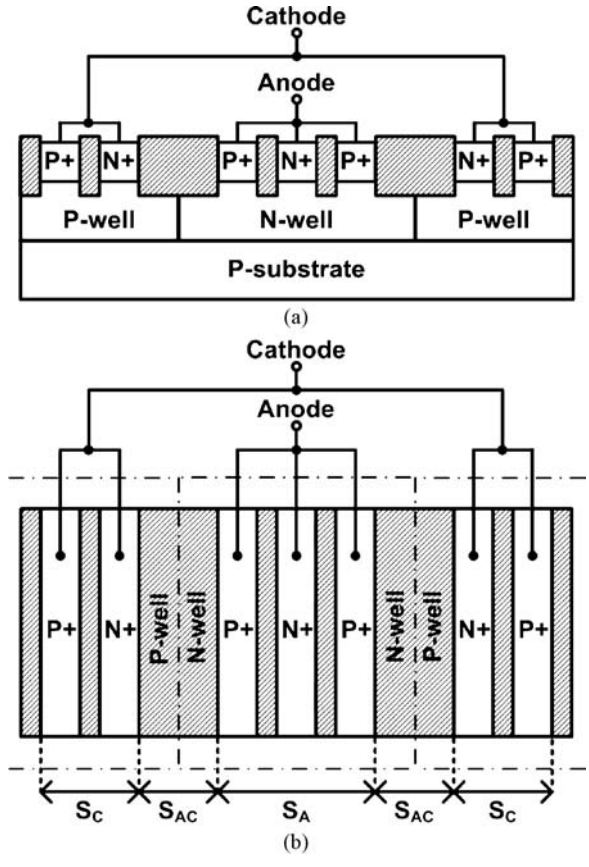


Figure 5.5 (a) Device cross-sectional view, and (b) layout top view, of the SCR test structure for TLU measurements.

(R_{Pwell}) (N-well resistor (R_{Nwell})) is greater than the cut-in voltage of the PN junction, the Q_{NPN} (Q_{PNP}) transistor will be turned on to inject the electron (hole) current to further bias the Q_{PNP} (Q_{NPN}) transistor, which initiates the SCR latching action. Finally, the SCR will be fully triggered into its latching state with the positive-feedback regenerative mechanism.

The DC *I–V* characteristic of the SCR test structure is shown in Figure 5.6b. Once the SCR is triggered on, the required holding current to keep turning on the NPN and PNP transistors can be generated through the positive-feedback latchup mechanism without involving the avalanche breakdown again. Therefore, the SCR has a lower holding voltage (V_{hold}) of typically $\sim$1.5 V in this 0.18-μm CMOS process. If a negative voltage is applied to the anode terminal of the SCR, the parasitic diode (N-well/P-well junction) inherent in the SCR structure will be forward-biased to clamp the negative voltage at the cut-in voltage of the diode.

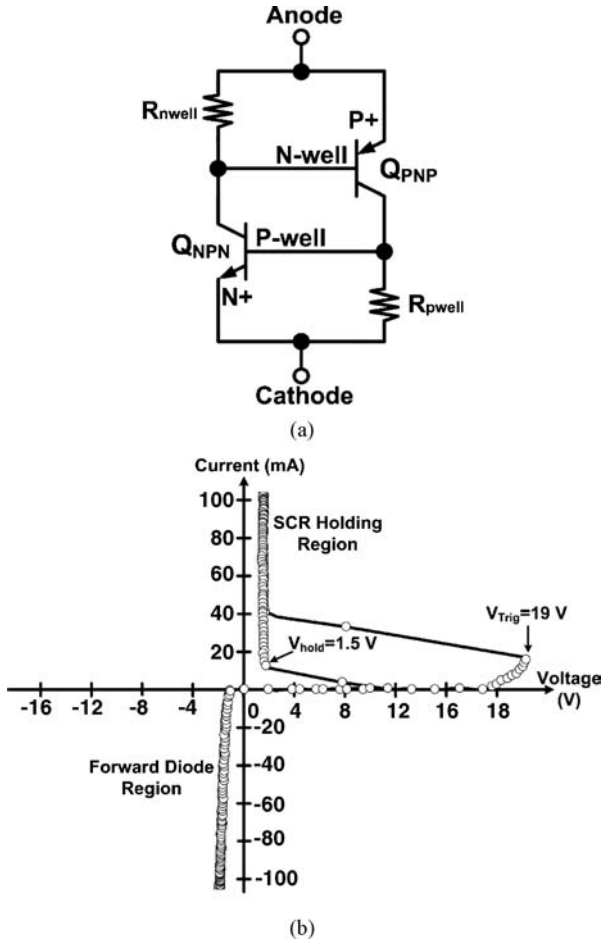


Figure 5.6 (a) Equivalent circuit schematic of an SCR device. (b) *I–V* characteristics of this SCR device under positive and negative biases.

5.3 Experimental Measurements

The TLU measurement setup in EFT tests is illustrated in Figure 5.7. The EFT generator can generate positive and negative transient EFT pulses on the power pins of the DUT. The SCR device shown in Figure 5.5a and b is used as the DUT where the anode (cathode) of the SCR is connected to V_{DD} (ground). I_{DD} is the total current flowing into the anode of the SCR and can be monitored by a separated current probe. The current-limiting resistor (5 Ω) is used to protect the DUT from electrical-overstress (EOS) damage during a high-current (low-impedance) latchup state. With both positive and negative EFT voltages, the measured V_{DD} (I_{DD}) transient response is recorded through the voltage (current) probe on the oscilloscope. This clearly indicates

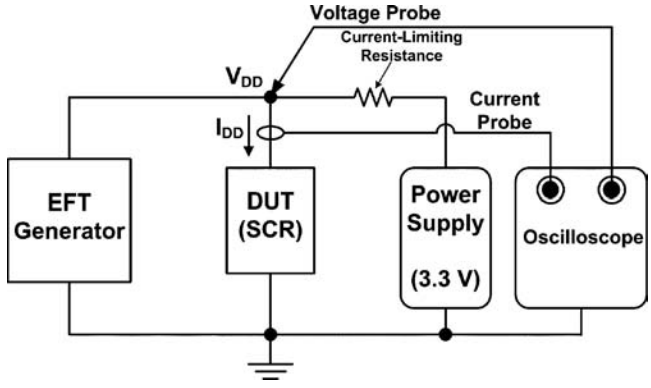


Figure 5.7 Measurement setup for TLU in EFT tests [3].

whether TLU occurs (I_{DD} significantly increases) during the TLU tests with applying EFT pulses.

5.3.1 Negative EFT Voltage

With a negative EFT voltage of −200 V, the measured V_{DD} and I_{DD} transient responses on the SCR structure are shown in Figure 5.8a. Before the EFT test ($V_{DD} = 3.3$ V), the SCR operates in the off-state and V_{DD} is kept at the normal operating voltage of 3.3 V. Within this duration, the N-well/P-well junction is in a normal reverse-biased state, and I_{DD} only comes from the negligible leakage current in the reverse-biased junction. When the EFT pulse is applied with a negative EFT voltage, V_{DD} begins to decrease rapidly from + 3.3 V and will eventually reach the negative peak voltage. Within this duration, the N-well/P-well junction becomes forward-biased when V_{DD} drops below 0 V. Thus, the forward-biased N-well/P-well junction can generate the forward current. When V_{DD} afterwards increases from the negative peak voltage back to its normal operating voltage of 3.3 V, the N-well/P-well junction will rapidly change from the forward-biased state to the reverse-biased state. Meanwhile, inside the N-well (P-well) region, a large number of stored minority holes (electrons) offered by the forward peak current will be instantaneously "swept-back" to the P-well (N-well) region where they originally come from. Therefore, such a "sweep-back" current, I_{Sb}, will produce a localized voltage drop and flow through the parasitic P-well or N-well resistance. Once this localized voltage drop approaches the cut-in voltage of the PN junction, the emitter-base junction of either the vertical PNP or the lateral NPN BJT in the SCR structure will be forward biased to further trigger on latchup. Thus, I_{DD} will greatly increase while V_{DD} returns to above 0 V, which indicates the occurrence of latchup. After EFT tests, V_{DD} will eventually be pulled down to the latchup holding voltage (+ 1.5 V), as shown in Figure 5.8a. Finally, the V_{DD} (I_{DD}) waveform is locked at a low voltage (high current) latchup state after this transition induced by the EFT pulse.

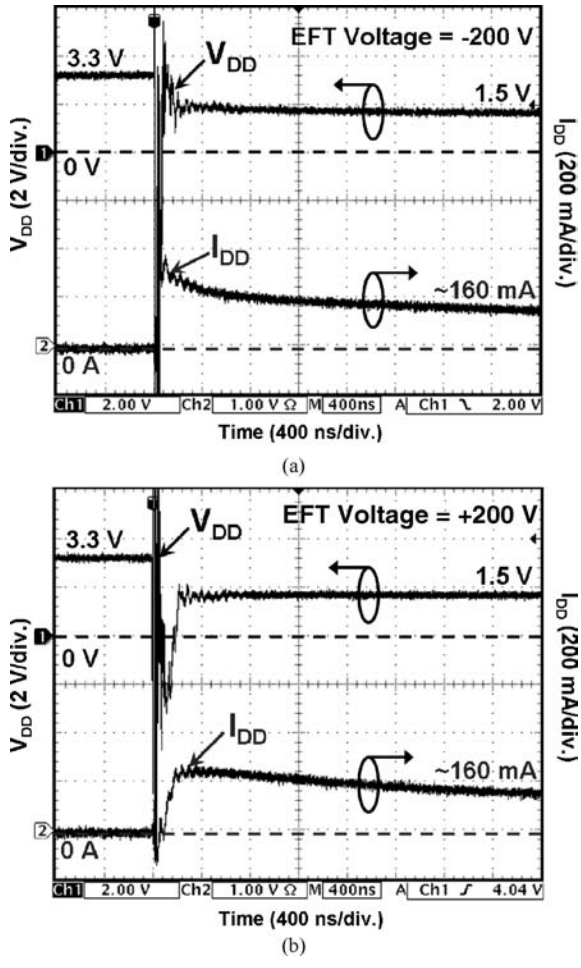


Figure 5.8 Measured V_{DD} and I_{DD} transient waveforms on the SCR test structure in EFT tests with EFT voltages of (a) -200 V and (b) $+200$ V.

5.3.2 Positive EFT Voltage

With a positive EFT voltage of $+200$ V, the measured V_{DD} and I_{DD} transient responses on the SCR structure are shown in Figure 5.8b. Unlike the V_{DD} waveform with a negative EFT voltage shown in Figure 5.8a, where V_{DD} begins decreasing rapidly, V_{DD} starts to increase and reaches a positive peak voltage. Within this duration, the N-well/P-well junction is always reverse biased within the SCR. Afterwards, V_{DD} decreases from the positive peak voltage to the negative peak voltage. Within this duration, the N-well/P-well junction gradually changes from the reverse-biased state to the forward-biased state, while more minority electrons (holes) are injected into the P-well

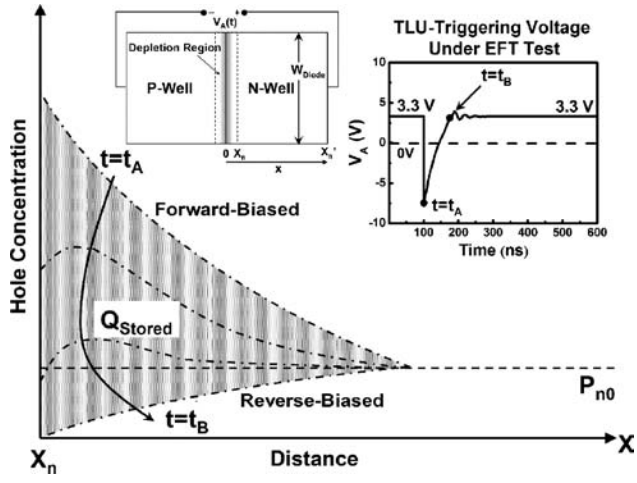


Figure 5.9 The total stored minority carriers, Q_{Stored}, causing I_{Sb} ($t_{\text{A}} \leq t \leq t_{\text{B}}$) inside the N-well region, where Q_{Stored} indicates the total charges due to the stored minority carriers in the ″shadowed area″. The inset figure is an ideal 1-D diode used for deriving the 1-D analytical model of the averaged I_{Sb} ($\equiv I_{\text{Ave}}$) [8].

(N-well) region. When V_{DD} returns from the negative peak voltage to the positive voltage, these minority electrons (holes) are subsequently swept back to the N-well (P-well) regions where they originally come from and finally TLU is triggered on. As a result, I_{DD} will considerably increase when V_{DD} returns from the negative peak voltage to the positive voltage. After the EFT test, TLU occurs because a huge I_{DD} of $\sim$160 mA can be found and V_{DD} eventually pulls down to its latchup holding voltage of $+1.5$ V, as shown in Figure 5.8b.

5.3.3 Physical Mechanism of TLU in the EFT Test

In the EFT test with a negative voltage pulse, it has been proved that the swept-back current, I_{Sb}, caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs is the major cause of the TLU. For simplicity, two reasonable assumptions are made. First, the N-well/P-well junction is treated as an ideal 1-D diode with a step junction profile, as shown in the inset figure in Figure 5.9. Second, the storage time of minority carriers is assumed to be negligible because I_{DD} can rapidly follow the polarity variation of V_{DD}. Therefore, from these assumptions, the charge due to the stored minority holes (Q_{Stored}) inside the N-well region can be expressed as follows:

$$Q_{\text{Stored}} = \int_{X_{\text{n}}}^{X_{\text{n}'}} [P_{\text{n}}(x,t)|_{t=t_{\text{B}}} - P_{\text{n}}(x,t)|_{t=t_{\text{A}}}]\text{d}x, \tag{5.1}$$

where $P_N(x, t)$ is the hole concentration in the N-well region and t_A (t_B) is the initial (final) timing point of a specific duration when I_{Sb} exists. Q_{Stored} represents the charge due to the total stored minority carriers (holes) causing I_{Sb} ($t_A \leq t \leq t_B$) inside the N-well region. Compared with the quasi-static latchup test [4], the specific duration ($t_A \leq t \leq t_B$) in the EFT test is much shorter than that in the quasi-static latchup test because the EFT pulse duration is only several tens of nanoseconds [2]. The rise time (fall) time for the quasi-static latchup test is much longer ($\sim\mu$s) than that for the EFT test. Thus, once these Q_{Stored} carriers (holes) are swept back to the regions where they come from, the averaged I_{Sb} can be expressed as follows:

$$I_{Ave} \equiv \frac{Q_{Stored}}{t_B - t_A}. \tag{5.2}$$

In both the TLU and quasi-static latchup conditions, if the initial ($t = t_A$) and the final ($t = t_B$) voltages during $t_A \leq t \leq t_B$ are equal (that is, with the same amount of Q_{Stored}), the averaged I_{Sb} in the TLU case will be about $10^3 \sim 10^6$ times larger than that in the quasi-static latchup case. The averaged I_{Sb} is rather small and hard to trigger on latchup in the quasi-static latchup test. Therefore, the averaged I_{Sb} is large enough to easily trigger on latchup in the SCR structure under the EFT test.

5.4 Evaluation on Board-Level Noise Filters to Suppress TLU in the EFT Test

It has been verified that CMOS ICs could be susceptible to TLU in the EFT test, because TLU can be easily initiated in the SCR test structure, even though the EFT pulse is as low as ± 200 V. Due to such weak immunity against TLU in EFT tests, different types of noise filter networks are investigated to find their effectiveness for improving the TLU immunity against EFT tests, including: (1) capacitor filters, (2) LC-like filters, (3) π-section filters, (4) ferrite bead, (5) transient voltage suppressors (TVS), and (6) hybrid type filters based on the combinations with TVSs and ferrite beads.

The modified TLU measurement setup in EFT tests with a noise filter network is illustrated in Figure 5.10. Noise filter networks between the EFT generator and the DUT are used to decouple, bypass, or absorb electrical transient voltage (energy) produced by the EFT generator. The DUT is the SCR structure shown in Figure 5.5a and b. The anodes of the SCR are connected together to V_{DD}, whereas the cathodes of the SCR are connected together to ground. I_{DD} is the total current flowing into the anode of the SCR.

5.4.1 Capacitor Filter, LC-Like Filter, and π-Section Filter

Three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter are depicted in Figure 5.11a–c, respectively. Figure 5.12 shows their improvements on both the positive and negative TLU levels of the SCR structure.

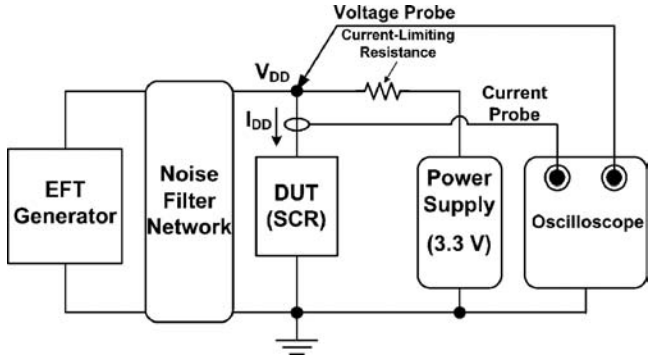


Figure 5.10 Measurement setup for TLU combined with a noise filter network in EFT tests.

The ceramic disc capacitor with advantages such as a high rated working voltage (1 kV), good thermal stability, and low loss over a wide range of frequencies is employed as the decoupling capacitor in the noise filter of Figure 5.11a. Decoupling capacitances ranging from 1 nF to 0.1 μF are used to investigate their improvements on the TLU level of the SCR structure. With the aid of the capacitor filter to reduce the electrical transient voltage on V_{DD}, the positive TLU level can be significantly enhanced from $+200$ V (without a decoupling capacitor) to over $+1000$ V (with a decoupling capacitance of 0.1 μF), as shown in Figure 5.12. Similarly, the negative TLU level can be also greatly enhanced from -200 V (without a decoupling capacitor) to -800 V (with a decoupling capacitance of 0.1 μF). Thus, by choosing a decoupling capacitor with the proper capacitance value, a simple first-order decoupling capacitor placed between V_{DD} and V_{SS} (ground) of CMOS ICs can be used to appropriately improve the TLU immunity of the DUT in the EFT tests.

The ferrite bead, which is commonly used for absorbing RF energy, substitutes for an inductor as a second-order LC-like filter component, as shown in Figure 5.11b. A resistor-type ferrite bead (part number: RH $3.5 \times 9 \times 0.8$ with a minimum impedance of 80 Ω (120 Ω) at 25 MHz (100 MHz)) is employed. Due to a higher insertion loss (second-order filter), such an LC-like filter has more TLU level enhancements than the capacitor filter (first-order filter) in Figure 5.11a. For example, the negative TLU level can also be greatly enhanced from -200 V (without a decoupling capacitor) to over -1000 V (with a decoupling capacitance of 0.1 μF). Thus, the LC-like filter can be used to achieve a higher negative TLU level.

A third-order π-section filter is used to further enhance the TLU level of the SCR, as shown in Figure 5.11c. This π-section filter consists of a ferrite bead (the same one in Figure 5.11b) and two decoupling capacitors with equal decoupling capacitance. The π-section filter has the highest insertion loss among the noise filter networks in Figure 5.11a–c, and gives the greatest improvement in the TLU level of the SCR. For

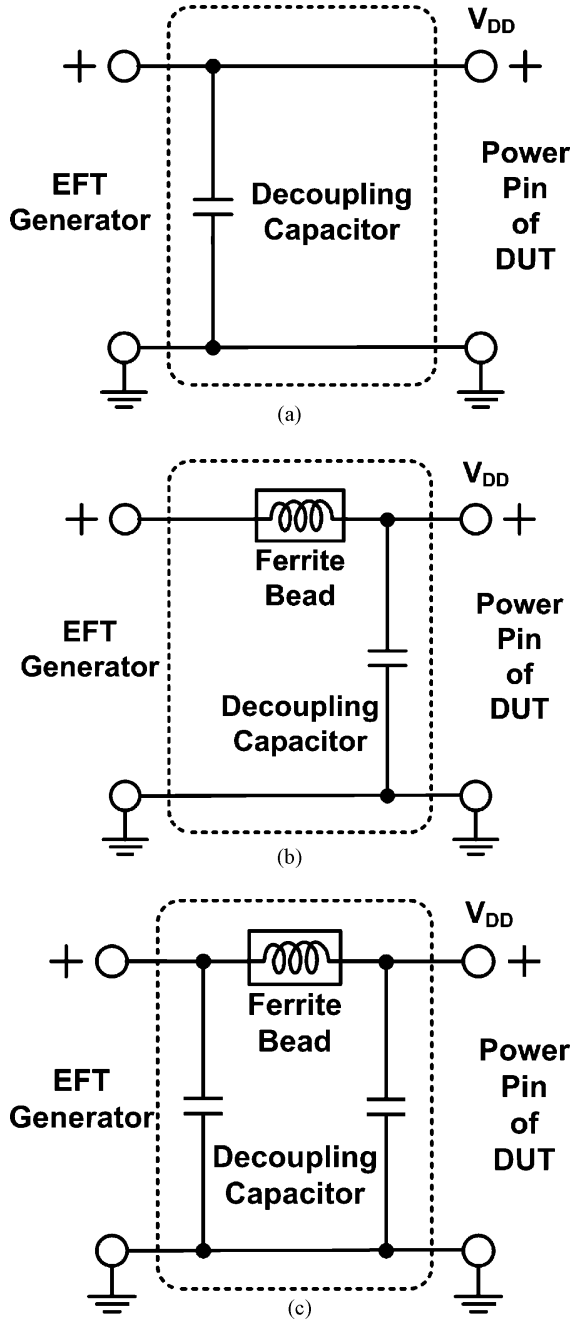


Figure 5.11 Three types of noise filter networks investigated for their improvements on the TLU level of the SCR. (a) Capacitor filter, (b) LC-like filter, and (c) π-section filter.

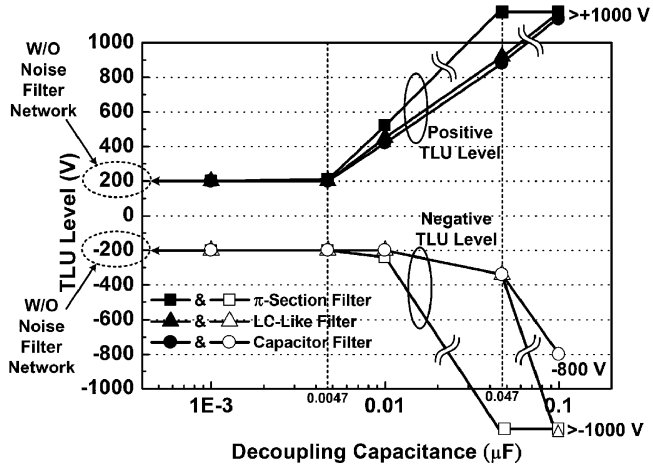


Figure 5.12 Relations between the decoupling capacitance and the TLU level of the SCR with three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter.

example, the positive TLU level can be significantly enhanced to over + 1000 V (with a decoupling capacitance of 47 nF), as shown in Figure 5.12. Similarly, the negative TLU level can also be significantly enhanced to over −1000 V (with a decoupling capacitance of 47 nF). From the comprehensive measured results in Figure 5.12, the decoupling capacitance can be optimized according to the desired TLU level and the type of board-level noise filter chosen.

5.4.2 Ferrite Bead, TVS, and Hybrid Type Filters

Four other types of noise filter networks, ferrite bead, TVS, hybrid type I, and hybrid type II are depicted in Figure 5.13a–d, respectively. Figure 5.14 shows their improvements on both the positive and negative TLU levels of the SCR test structure.

The ferrite bead can absorb RF energy while the noise-induced transient current flows through it. The resistor-type ferrite beads with three different minimum impedances at 25 MHz are employed in this work: 35 Ω, 50 Ω, and 80 Ω. However, a noise filter network with only a ferrite bead does not have an improvement on the TLU level due to a lesser energy-absorbing ability at frequencies lower than 10 MHz. As shown in Figure 5.14, the TLU level of the SCR structure will not be efficiently improved (the magnitudes of both positive and negative TLU levels are all equal to 200 V), even though the minimum impedance of the ferrite bead at 25 MHz is as high as 80 Ω.

A TVS, which is commonly used to bypass/decouple high-frequency transient noises, is also considered for its improvement on the TLU immunity of the SCR. The bidirectional-type TVS components (part number: P6KE series) with three different

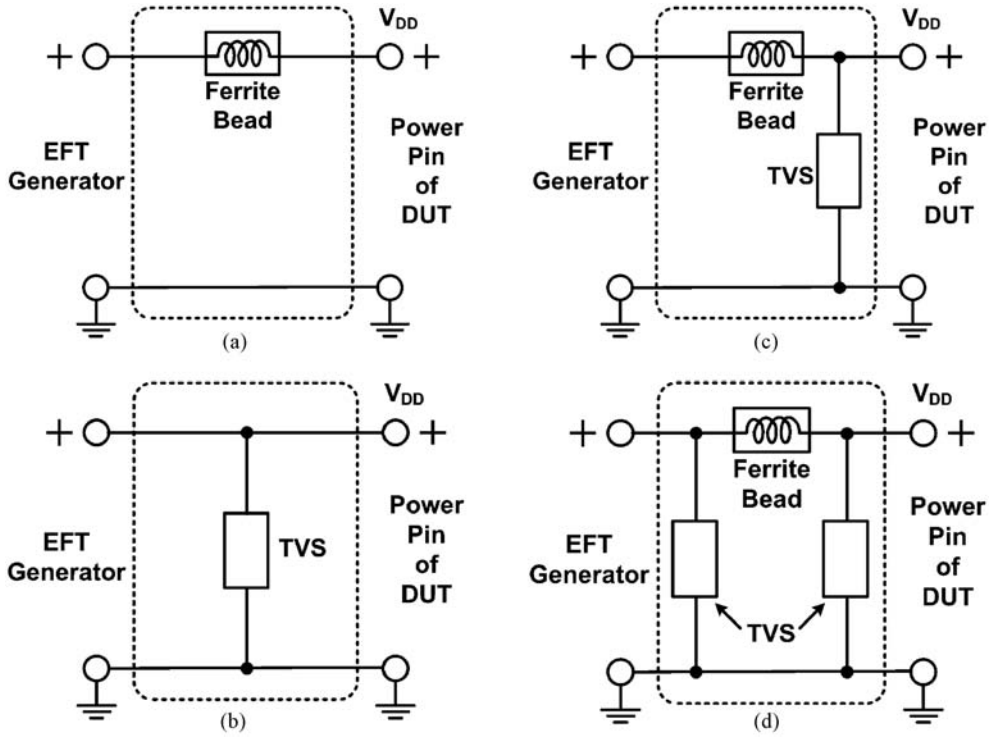


Figure 5.13 Four types of noise filter networks investigated for their improvement on the TLU level of the SCR. (a) Ferrite bead, (b) TVS, (c) hybrid type I, and (d) hybrid type II.

breakdown voltages, V_{BR}, (± 13 V, ± 82 V, and ± 200 V) are employed. As shown in Figure 5.14, the TVS components with a breakdown voltage of ± 82 V and ± 200 V fail to efficiently improve the TLU level of the SCR (the magnitudes of both positive and negative TLU levels are all equal to 200 V), because TLU occurs prior to the breakdown of the high-V_{BR} TVS. Only the TVS with a low V_{BR} can effectively enhance the TLU level. For example, the positive TLU level can be enhanced to $+520$ V for a TVS with a breakdown voltage of ± 13 V. Thus, to optimize the efficiency of the TVS for TLU prevention, the correlations between V_{BR} of the TVS and the intrinsic TLU level of the DUT should be clarified in advance.

Hybrid type filters consisting of both a ferrite bead (minimum impedance of 80 Ω at 25 MHz) and a TVS (with different V_{BR}) are also evaluated for their improvements on the TLU level of the SCR, as shown in Figure 5.13c and d. Hybrid types I and II are the counterparts of the LC-like and π-section filters where the TVS substitutes for the decoupling capacitor as a low-pass component. Because such higher-order hybrid type filters provide higher insertion loss, they enhance the TLU level of the SCR more

significantly than the ferrite bead or TVS alone, as shown in Figure 5.14. For example, hybrid type I with a low-V_{BR} ($\pm$13 V) TVS can enhance the positive TLU level up to $+$550 V. For hybrid type II with a low-V_{BR} ($\pm$13 V) TVS, the positive (negative) TLU level can be enhanced to over $+$1000 V ($-$780 V).

5.4.3 Discussion

Through investigating different types of noise filter networks to find their improvements on TLU levels in Figures 5.12 and 5.14, it is found that the TVS (hybrid type II) does not improve the negative TLU level as greatly as the first-order capacitor filter (LC-like filter) does. For example, the negative TLU level can be significantly enhanced to over $-$1000 V when using an LC-like filter with a decoupling capacitance of 0.1 μF, while the TLU level is $-$780 V when using the hybrid type II filter with a low V_{BR} ($\pm$13 V) TVS. To further improve the TLU immunity of electronic products, chip-level solutions should be adopted to meet the applications with high EFT specification and reduce the cost of electronic products. For example, an on-chip power-rail ESD clamp circuit between the V_{DD} and V_{SS} power lines can provide a low impedance path to efficiently discharge the ESD current during ESD stress conditions [5]. For CMOS ICs in EFT tests, it may be a solution to apply an on-chip power-rail ESD clamp circuit to suppress electrical transients and avoid unexpected current into the internal circuits. In the on-chip circuit design techniques, some circuits have been also proposed to avoid latchup or to detect electrical fast transients under

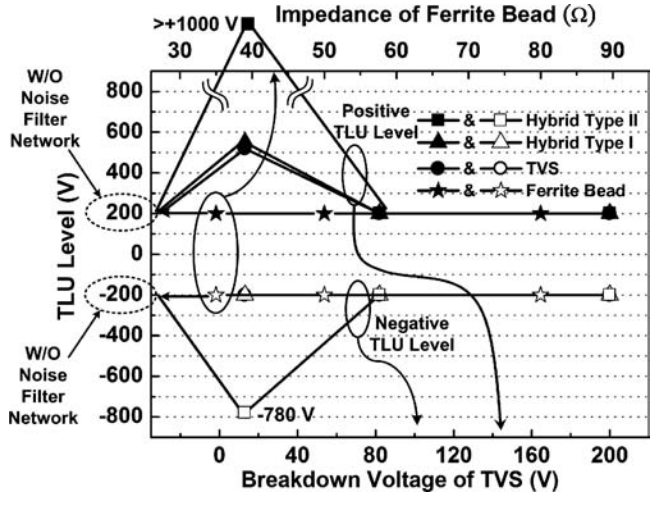


Figure 5.14 Relations between the TLU level of the SCR, the minimum impedance of the ferrite bead at 25 MHz, and the breakdown voltage of the TVS with four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II.

ESD stress conditions [6, 7]. The chip-level solutions have the advantages of single chip integration in nanoscale CMOS technology and substantially reduce the total cost of microelectronic products. Therefore, the chip-level solutions to meet high EFT specification for microelectronic products are highly requested in the IC industry.

5.5 Conclusion

The positive and negative EFT voltage pulses have been identified as the realistic TLU-triggering source in EFT tests. From experimental measurements, the specific "swept-back" current caused by the minority carriers stored within the parasitic PNPN structure of CMOS ICs has been proven to be the cause of TLU. Thus, TLU reliability issue may still exist in qualified CMOS IC products through the quasi-static latchup test. With an understanding of the physical mechanism and experimental verification of TLU, circuit design and layout techniques in CMOS ICs can be developed against TLU events in EFT tests.

By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs in EFT tests can be greatly improved. From the experimental results, the decoupling capacitor is better than the TVS as a noise-bypassing component in noise filter networks. The optimal design for enhancement of TLU immunity can be achieved through a clear characterization of TLU prevention from different kinds of board-level noise filters. In addition, chip-level solutions should be further developed to meet high EFT immunity requirements for microelectronic products.

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6

Methodology on Extracting Compact Layout Rules for Latchup Prevention[1]

To efficiently avoid the latchup issue in CMOS ICs, proper layout guidelines for latchup prevention are necessary for circuit design considerations. This chapter introduces experimental methodologies to extract area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, for internal circuits, and for between I/O and internal circuits. Through detailed investigations of latchup immunity dependencies on variations of geometrical layout parameters and temperatures, compact and safe layout rules can be established for latchup prevention in a given CMOS process.

6.1 Introduction

In CMOS ICs, the latchup PNPN path exists from the source (P+ diffusion connected to the V_{DD}) of a PMOS, through the N-well and P-substrate/P-well, to the source (N+ diffusion connected to the V_{SS}) of an NMOS. Many parasitic PNPN paths inevitably exist in CMOS ICs, because CMOS ICs have many PMOS devices connected to the V_{DD} and NMOS devices connected to the V_{SS}. If one of such parasitic PNPN paths between the V_{DD} and V_{SS} is firing, latchup can occur to burn out CMOS ICs [1–5]. Because of the parasitic latchup PNPN paths existing in both the I/O cells and internal circuits of a CMOS IC, latchup can occur at I/O cells or at internal circuits. Several advanced CMOS processes have been proposed to improve the latchup immunity,

[1] © 2003 IEEE. Reprinted, with permission, from Ming-Dou Ker and W.-Y. Lo, Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology (sections II–IV and figures 2–5, 7–10, 12-14, 20–25, and 27–32), in *IEEE Transactions on Semiconductor Manufacturing*, Vol. 16, no. 2, pp. 319–334, May 2003. IEEE, Piscataway, NJ.

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such as the epitaxial wafer [6], retrograde well [7], trench isolation [8], and silicon on insulator (SOI) devices [9]. However, with considerations of the unavoidable additional fabrication cost of these process solutions, latchup prevention in most commercial IC products is mainly achieved by adding the guard rings in the I/O cells and placing the substrate/well pickups as many as possible in the internal circuits. Thus, to certainly avoid the latchup failure in a given CMOS process, layout design guidelines must be specified for the I/O cells, for internal circuits, and for between the I/O cells and internal circuits.

Nowadays, due to the necessary integration of more complex functions and more circuit blocks into a single chip, a high-integration CMOS IC often has a pin count up to several hundreds. Especially, in communication ICs or chip set ICs, more I/O pins are designed to satisfy the desired system connections for function applications. In such high-pin-count CMOS ICs, the whole chip size is often dominated by the pad-limited effect but no longer the core-limited effect [10]. Therefore, the pad pitch of I/O cells is critically limited to reduce the total chip size of a high-pin-count CMOS IC. To further reduce the pad pitch for high-pin-count CMOS ICs, the staggered bond pad has been widely used in CMOS ICs to reduce the whole chip size [10]. With the staggered bond pad design, the layout pitch for a corresponding I/O cell has been scaled down to only $\sim$50 μm. With such a narrow layout pitch, the cell height of an I/O cell (including output buffer circuits and ESD protection circuits) and the widths of the latchup guard rings become much wider. The much longer cell height of the I/O cells causes a significant increase on the whole chip size. Therefore, compact and safe layout rules for latchup prevention are specifically demanded in high-pin-count CMOS ICs.

6.2 Latchup Test

The detailed test procedures and specifications to verify the latchup immunity in CMOS ICs have been clearly specified in the EIA/JEDEC Standard No. 78A [11]. The latchup testing classifications, as well as two different latchup test modes – trigger current and over-voltage tests, are briefly introduced in the following sections.

6.2.1 Latchup Testing Classification

The latchup testing classification is defined with respect to different test temperatures. Latchup testing classification is defined as below:

Class I – Latchup testing is performed at room temperature.
Class II – Latchup testing is performed at the maximum ambient rated temperature.

The elevated temperature will reduce the latchup hardness of the device under test (DUT), and the class II testing is recommended by the EIA/JEDEC standard for devices that are required to operate at an elevated temperature.

6.2.2 Trigger Current Test

The trigger current test should be performed on each input, output, and I/O pins as indicated below:

1. Bias the DUT as indicated in Figure 6.1 (Figure 6.2) for a positive (negative) trigger current test. All untested input and I/O pins should be tied to the maximum logic-

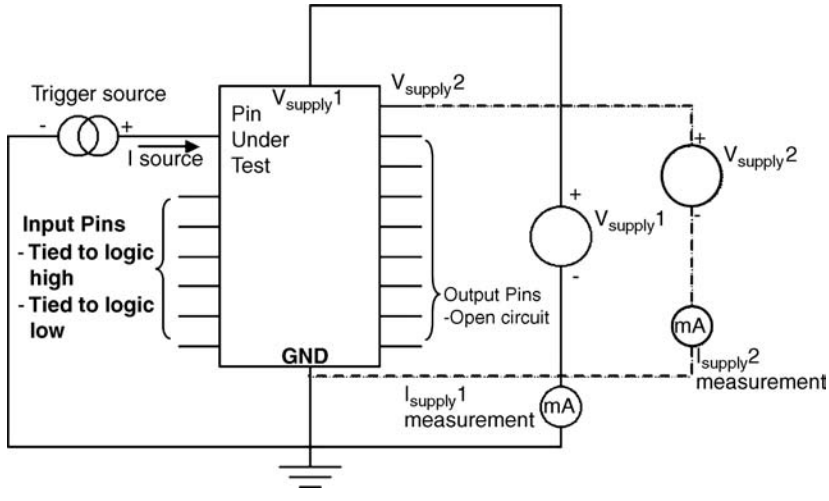


Figure 6.1 Equivalent circuit for the latchup test – positive trigger current test.

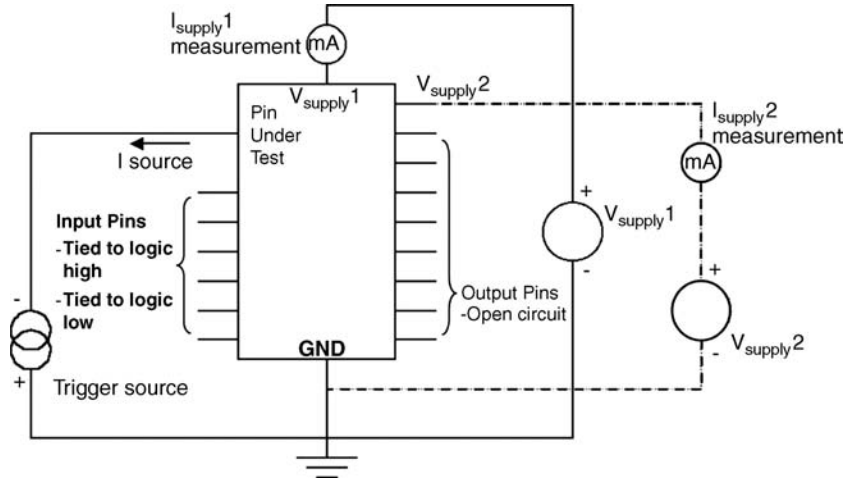


Figure 6.2 Equivalent circuit for the latchup test – negative trigger current test.

high level as specified in the device specification. Output pins should be open-circuit except when latchup tested. When the DUT stabilizes at the test temperature, the normal I_{supply} (I_{nom}, where this represents the I_{supply} at the IC normal operating condition) for each V_{supply} pin is measured.

2. Apply the positive (or negative) current pulse to the pin under test. The waveforms of the positive (negative) trigger currents are defined in Table 6.1 and Figure 6.3 (Figure 6.4).

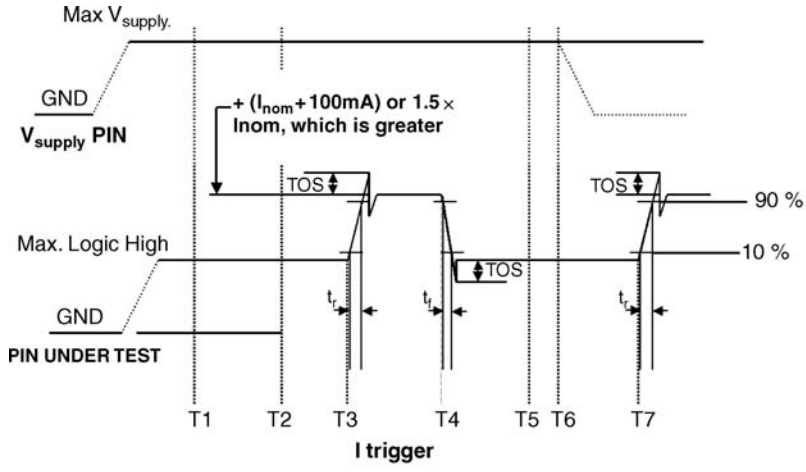
Table 6.1 Timing specifications for the trigger current test and V_{supply} over-voltage test.

Symbol	Time interval	Parameter	Limit	
			Minimum	Maximum
t_r	—	Trigger rise time	5 µs	5 ms
t_f	—	Trigger fall time	5 µs	5 ms
T_{width}	$T3 \rightarrow T4$	Trigger duration (width)	$2 \times t_r$	1 s
TOS	—	Trigger over-shoot	5% of pulse voltage	
T_{cool}	$T4 \rightarrow T7$	Cool down time	$>= T_{width}$	
T_{wait}	$T4 \rightarrow T5$	Waiting time before measuring I_{supply}	3 ms	5 s

3. After the trigger source has been removed, return the pin under test to the state it was in before the application of the trigger pulse, and measure the I_{supply} for each V_{supply} pin. If any I_{supply} is greater than or equal to the failure criteria specified as $1.4 \times I_{nom}$ or $I_{nom} + 10$ mA, latchup has occurred and power must be removed from the DUT. If latchup has occurred, stop the test.
4. If latchup has not occurred, after the necessary cool-down time (see Table 6.1), repeat steps 2 and 3 for all pins to be tested.
5. Repeat steps 1 through 4, except in step 1 that all untested input and I/O pins should be tied to a minimum logic-low level as specified in the device specification.

For CMOS ICs to meet the requirements of the JEDEC latchup specification, the DUT should not be triggered into latchup by a trigger current of ±100 mA.

The device cross-sectional view of CMOS ICs under a latchup trigger current test is illustrated in Figure 6.5. The positive/negative trigger current applied on the pad is conducted into the drain regions of the output devices. When the positive (negative) current is applied into the I/O pin, the P+ drain/N-well (N+ drain/P-substrate) junction in the output PMOS (NMOS) is forward biased to form the trigger current injecting into the substrate. This substrate current, indicated by the gray dashed line in Figure 6.5, can initiate latchup in the I/O cell or in the internal circuits. If the DUT is fired into latchup by applying the trigger current on the I/O pin, the current flowing from the V_{DD} power supply will obviously increase. Such a significant



Time	Operation
T1 → T2	Measure the normal operating current I_{supply} (I_{nom})
T2 → T3	Wait time prior to applying the trigger current on the I/O pin
T3 → T4	Apply the trigger current on the I/O pin
T4 → T5	Wait time prior to I_{supply} measurement
T4 → T7	Cool down time (T_{cool})
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria, Latchup has occurred and power must be removed from DUT
T7	Start the next test

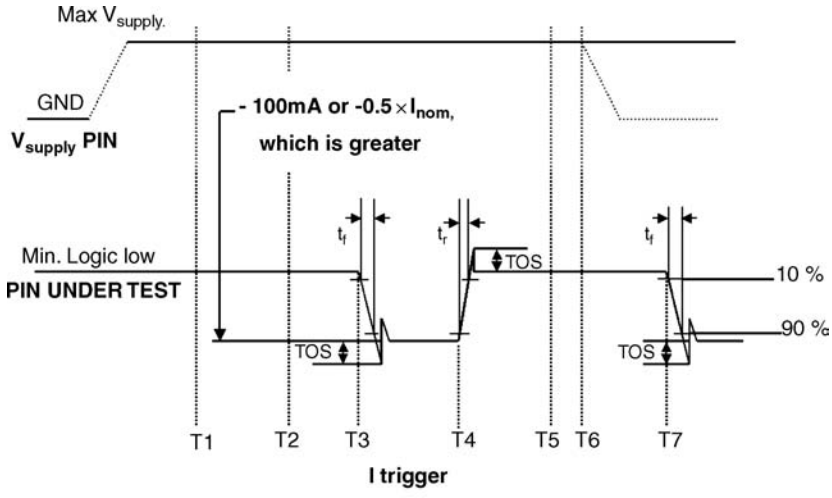
Figure 6.3 Test waveform for the positive trigger current.

increase on the V_{DD} current can be detected by a latchup tester to judge the occurrence of latchup.

6.2.3 V_{supply} *Over-Voltage Test*

The V_{supply} over-voltage test should be performed on each V_{supply} pin as indicated below:

1. Bias the DUT as indicated in Figure 6.6. All untested input and I/O pins should be tied to the maximum logic-high level as specified in the device specification.



Time	Operation
T1 → T2	Measure the normal operating current I_{supply} (I_{nom})
T2 → T3	Wait time prior to applying the trigger current on the I/O pin
T3 → T4	Apply the trigger current on the I/O pin
T4 → T5	Wait time prior to I_{supply} measurement
T4 → T7	Cool down time (T_{cool})
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria, Latchup has occurred and power must be removed from DUT
T7	Start the next test

Figure 6.4 Test waveform for the negative trigger current.

Output pins should be open-circuit. When the DUT stabilizes at the test temperature, measure the normal operating current I_{supply} (I_{nom}) for each V_{supply} pin at this time.

2. Apply the voltage trigger pulse to the V_{supply} pin under test. The waveform of the voltage trigger pulse is defined in Figure 6.7 and Table 6.1.
3. After the trigger source has been removed, return the V_{supply} pin under test to the state it was in before the application of the trigger pulse and measure the I_{supply} for each V_{supply} pin. If any I_{supply} is greater than or equal to the failure criteria specified

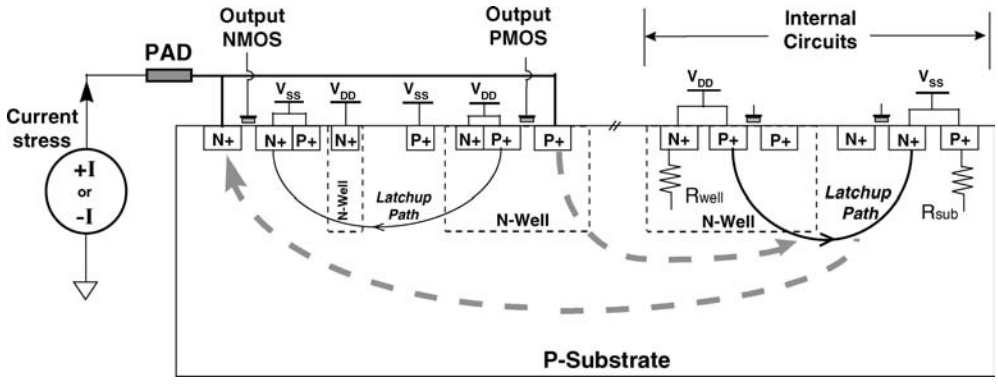


Figure 6.5 Device cross-sectional view of CMOS ICs under the latchup trigger current test. (Reprinted with permission from IEEE).

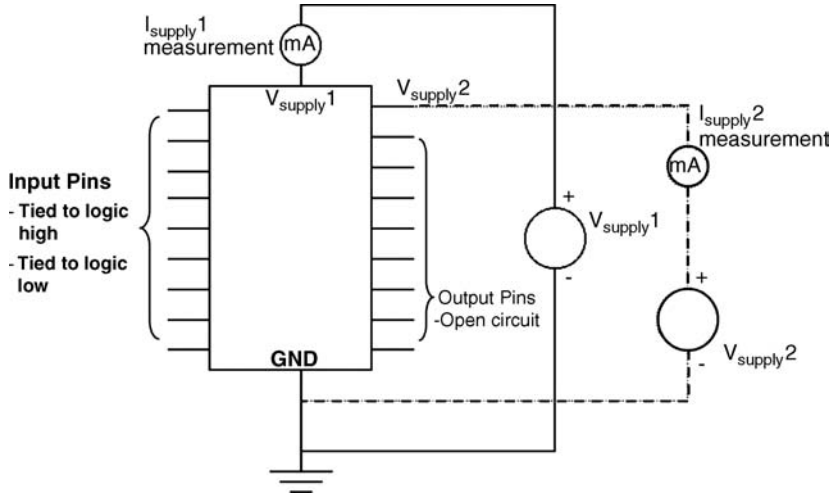
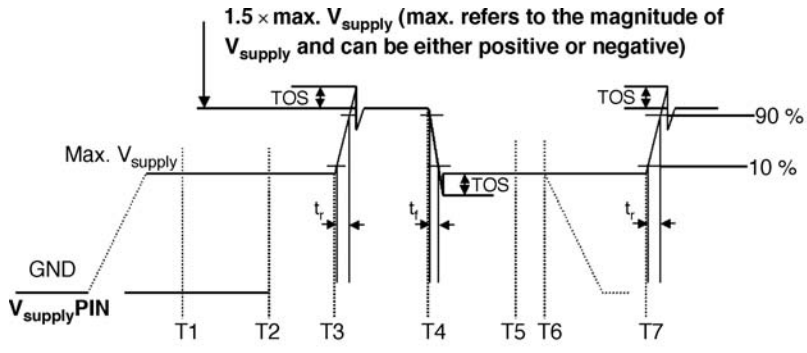


Figure 6.6 Equivalent circuit for the latchup test – V_{supply} over-voltage test.

as $1.4 \times I_{\text{nom}}$ or $I_{\text{nom}} + 10\,\text{mA}$, latchup has occurred and power must be removed from the DUT. If latchup has occurred, stop the test.

4. If latchup has not occurred, after the necessary cool-down time (see Table 6.1), repeat steps 2 and 3 for all V_{supply} pins to be tested.
5. Repeat steps 1 through 4, except in step 1 that all untested input and I/O pins should be tied to a minimum logic-low level as specified in the device specification.

For CMOS ICs to meet the requirements of the JEDEC latchup specification, the DUT should not be triggered into latchup by a trigger voltage level of $1.5 \times V_{\text{DD}}$ on the V_{DD} pins.



Time	Operation
T1 → T2	Measure the normal operating current I_{supply} (I_{nom})
T2 → T3	Wait time prior to applying the over-voltage pulse to the VDD pin
T3 → T4	Apply the over-voltage pulse to the VDD pin
T4 → T5	Wait time prior to I_{supply} measurement
T4 → T7	Cool down time (T_{cool})
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria, Latchup has occurred and power must be removed from DUT
T7	Start the next test

Figure 6.7 Test waveform for the V_{supply} over-voltage.

CMOS ICs could be very sensitive to latchup under the over-voltage transition on the V_{DD} pin (V_{supply} pin) [12, 13]. The device cross-sectional view of CMOS ICs in the latchup V_{supply} over-voltage test is illustrated in Figure 6.8, where the trigger voltage is applied on the V_{DD} pin (V_{supply} pin) of the DUT. The power-transition trigger voltage often generates the displacement current or junction breakdown current into the N-well or P-substrate to fire latchup paths in the I/O cells or the internal circuits of the CMOS ICs. If the DUT is fired into latchup by the trigger voltage on the V_{DD} pin, the current flowing into the V_{DD} pin has an obvious increase. Such an obvious increase on the V_{DD} current can be detected by the latchup tester to judge the occurrence of latchup.

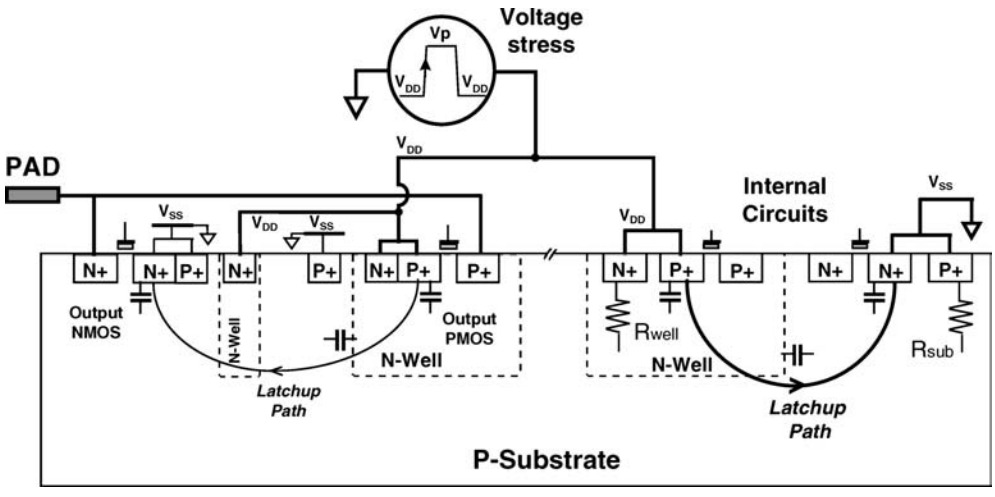


Figure 6.8 Device cross-sectional view of CMOS ICs under the latchup V_{supply} over-voltage test. (Reprinted with permission from IEEE).

6.3 Extraction of Layout Rules for I/O Cells

6.3.1 Latchup in I/O Cells

Because of the direct connection with the bond pads in CMOS ICs, the I/O cells can be easily initiated to a latchup state by the external overshooting or undershooting voltage/current glitches. In general, the layout design rules for latchup prevention often mainly focus on the I/O cells. A typical layout example of an inverter output buffer in an I/O cell is shown in Figure 6.9. To certainly prevent the occurrence of latchup in the I/O cells, guard rings are always used to surround both the PMOS and NMOS. In addition, the NMOS must be separated by a proper anode-to-cathode spacing away from the PMOS. As a result, several layout guidelines need to be identified, such as the guard ring designs (double guard rings, single guard ring, or no guard ring), the minimum guard ring width, the maximum distance between the first and second guard rings, and the minimum anode-to-cathode spacing. These design guidelines, without doubt, are also always specified in the foundry's design rules.

The device cross-sectional view and layout top view of the I/O cell are shown in Figures 6.10a and b, respectively. The latchup path is also indicated. Both the NMOS and PMOS in the I/O cell are surrounded by double guard rings to efficiently avoid latchup in the I/O cells. For NMOS devices, the first guard ring (also called the base guard ring) is the P+ diffusion region that surrounds the source of the NMOS (N+ diffusion connected to the V_{SS}), and the second guard ring (also called the collector guard ring) is the N+ diffusion that often surrounds the first guard ring. For an NMOS,

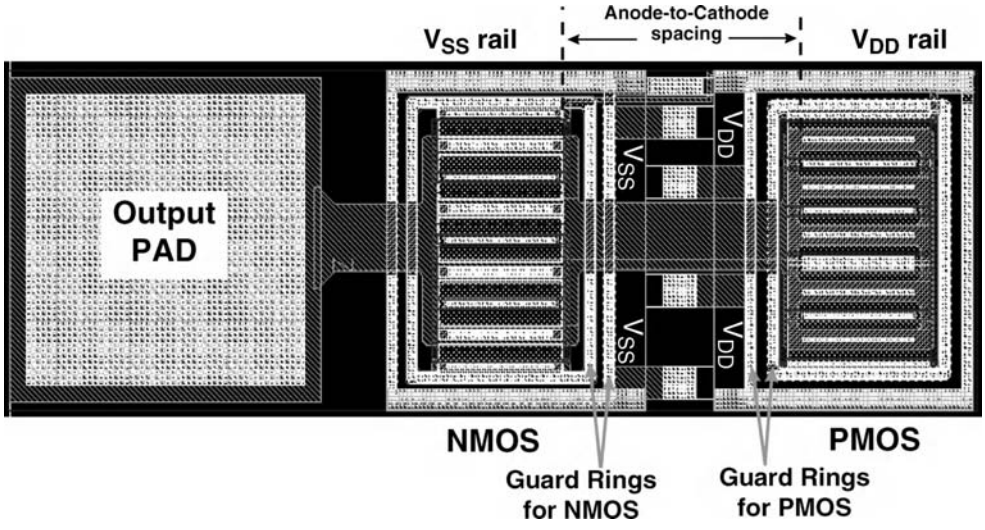
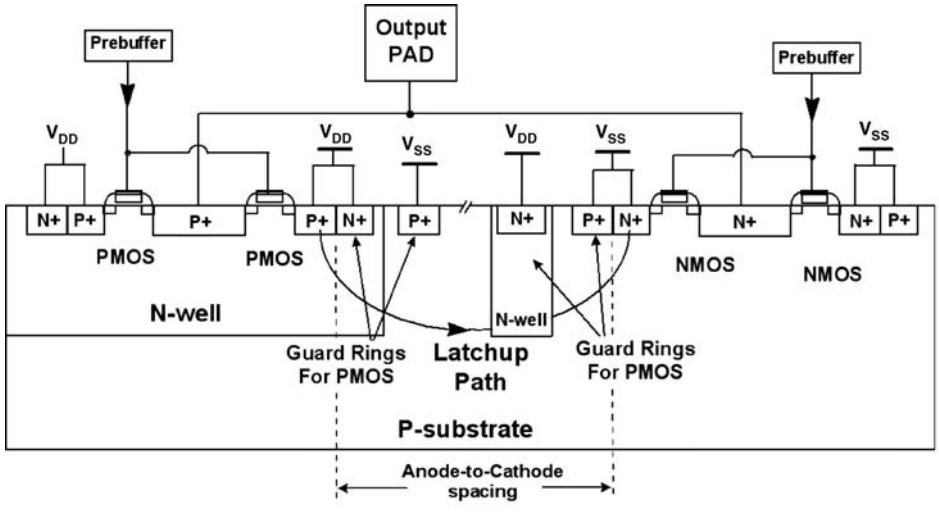


Figure 6.9 Layout example of an inverter output buffer in the I/O cell. (Reprinted with permission from IEEE).

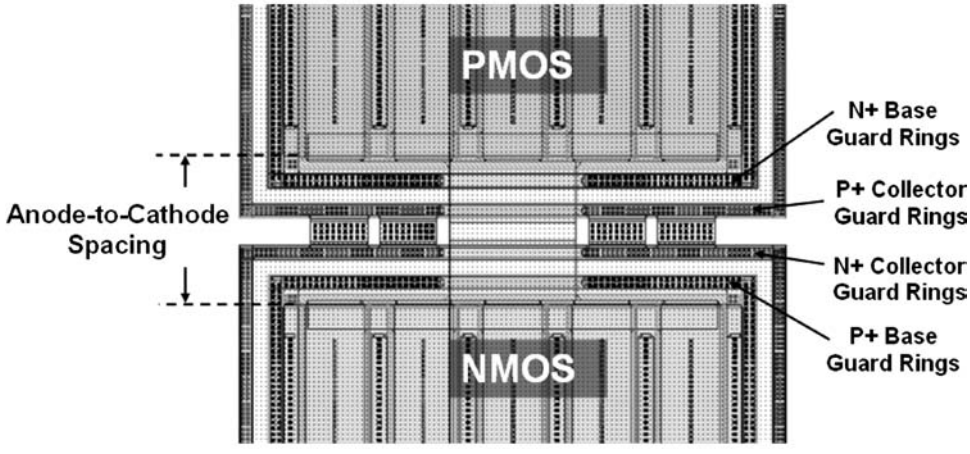
the first P+ guard ring is biased at the V_{SS} and the second N+ guard ring is biased at the V_{DD} to prevent latchup. To improve guard ring efficiency, the N-well region is often added under the second N+ guard ring of the NMOS. The N-well has a deeper junction depth ($\sim$2 μm) than that ($\sim$0.2 μm) of an N+ diffusion, and so the N+ guard ring efficiency can be enhanced. For PMOS devices, the first guard ring is the N+ diffusion located in the N-well region, surrounding the source of the PMOS (P+ diffusion connected to the V_{DD}). The second guard ring is the P+ diffusion located in the P-substrate region, surrounding the first guard ring. For a PMOS, the first N+ guard ring is biased at the V_{DD} and the second P+ guard ring is biased at the V_{SS} to prevent latchup.

With double guard rings surrounding the NMOS and PMOS in the I/O cell layout, the current gain of the parasitic BJTs in I/O cells can be greatly reduced. Thus, the latchup robustness of an I/O cell can be significantly improved, leading to an obvious increase of the latchup holding voltage of the parasitic PNPN in an I/O cell. If the latchup holding voltage can be increased up to greater than the normal V_{DD} operating voltage level of the CMOS IC, the parasitic PNPN path in the I/O cell can be free to latchup. Thus, it is critical to specify the layout guidelines of the guard rings in the I/O cell for latchup prevention, such as the guard ring designs (double guard rings, single guard ring, or no guard ring), the minimum width of the first and second guard rings to surround the NMOS or PMOS, and the maximum distance between the first and second guard rings.

In addition to the guard ring, one critical layout parameter to dominate the latchup immunity of the I/O cell is the "anode-to-cathode spacing" between the sources of the PMOS and NMOS, as shown in Figures 6.9 and 6.10. Enlarging the anode-to-cathode



(a)



(b)

Figure 6.10 (a) Device cross-sectional view, and (b) layout top view, of the I/O cell. The latchup path, as well as the double guard rings to prevent latchup are also indicated. (6.10(a) reprinted with permission from IEEE).

spacing reduces the current gain of the parasitic BJTs, improving the latchup immunity in I/O cells. However, a very large anode-to-cathode spacing also leads to the burden of increasing layout area. Thus, it is necessary to specify a minimum anode-to-cathode spacing to save the layout area of the I/O cell for high-pin-count CMOS ICs, but still able to maintain good latchup immunity in CMOS ICs.

6.3.2 Design of Test Structure for I/O Cells

To extract the layout rules for latchup prevention in I/O cells, the I/O cells with different geometrical parameters are used as the test structures. A layout example of the I/O cell is shown in Figure 6.9. The PMOS and NMOS devices in I/O cells are drawn in the multiple-finger style with a fixed finger length, and the total channel widths are the same for both the NMOS and PMOS. To simplify the measurements of latchup DC *I–V* characteristics and the JEDEC latchup test, the gate of the PMOS is connected to V_{DD} and the gate of the NMOS is connected to V_{SS}, turning off both the PMOS and NMOS.

To verify the efficiency of different guard ring designs for latchup prevention, the layouts of I/O cells can be prepared with double guard rings, a single guard ring, or no guard ring, as shown in Figure 6.11a–c, respectively. Using a guard ring can greatly

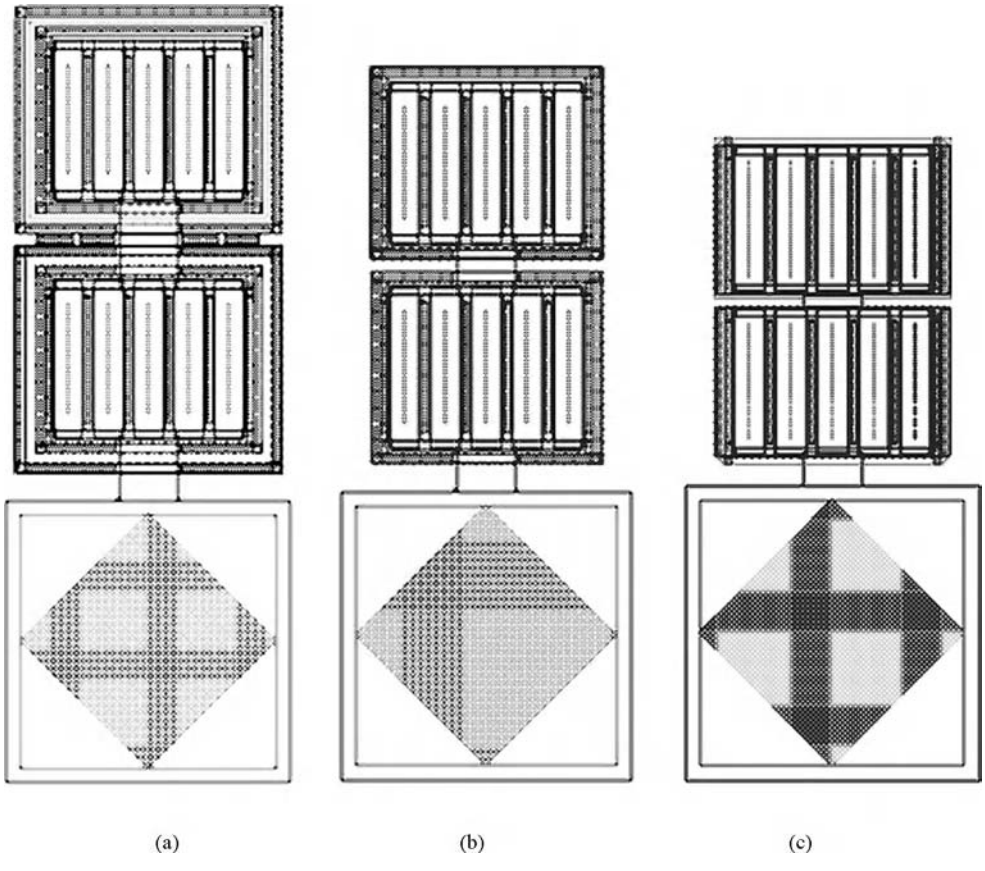


Figure 6.11 The I/O cell layouts with (a) double guard rings, (b) a single guard ring, and (c) no guard ring, to verify the efficiency of different guard ring designs. (Reprinted with permission from IEEE).

enhance the latchup robustness of the I/O cells, but also inevitably result in additional layout areas, that is, production cost, especially for high-pin-count CMOS ICs. Thus, it is critical to determine whether the guard rings are necessary for I/O cells to be latchup-free (holding voltage higher than the V_{DD} normal operating voltage of the I/O cells). Instead of using double guard rings, if simply the single guard ring, or even no guard ring, is enough to help the I/O cells be latchup-free, the layout areas of the I/O cells can be greatly reduced for cost-down purposes.

Anode-to-cathode spacing and guard ring width are also two dominant factors to affect the latchup robustness and the layout areas of the I/O cells, and therefore the test structures with different anode-to-cathode spacings and guard ring widths also need to be carefully considered for their influences on latchup immunity. For a given anode-to-cathode spacing, it is noteworthy that the guard rings located between the PMOS and NMOS should be drawn as compact as possible to achieve the best latchup robustness. As a result, through the optimizations between the anode-to-cathode spacing and guard ring width, compact and safe design rules in I/O cells for latchup prevention can be accurately extracted.

6.3.3 Latchup Immunity Dependency of I/O Cells

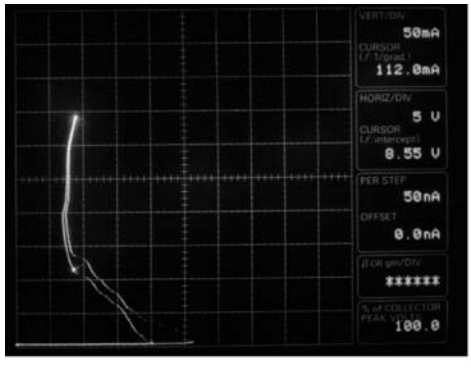
The latchup robusness dependency of I/O cells on two dominant factors, i.e. anode-to-cathode spacing and the guard ring designs (double guard rings, single guard ring, or no guard ring), are presented in this section. With the help of the related measured results, safe and compact layout rules can be determined for latchup prevention in the I/O cells. The impacts of some other layout parameters on latchup immunity of the I/O cells, such as the guard ring width and the distance between the first and second guard rings, are referred to in detail in Appendix A. Additionally, the degradations of the latchup robustness due to the high test temperature are also considered for different anode-to-cathode spacings and the guard ring designs, and so it is helpful to determine the proper layout rules under their corresponding demanded operating temperatures in a given CMOS process.

To evaluate the latchup robustness of the DUT, it is important to characterize the latchup holding voltage from the latchup DC *I–V* characteristics of the DUT. If the holding voltage of I/O cells is greater than V_{DD}, the I/O cell is latchup-free. As a result, latchup never occurs under the JEDEC latchup test, regardless of the trigger current test or the over-voltage test. Choosing any specified layout rule as a suggested rule needs to make sure that the holding voltage is higher than the V_{DD} normal operating voltage (that is, latchup-free) under this specified layout rule.

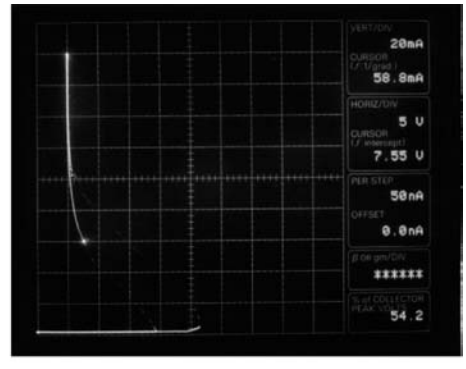
The latchup DC *I–V* characteristics can be measured by the continuous-type curve tracer (e.g. *Tek*370A). Both the NMOS and PMOS in the I/O cell are in their turn-off states by connecting the gate of the PMOS to V_{DD}, while connecting the gate of the NMOS to V_{SS}. The finger width and total channel width have fixed values of 50 and 500 μm, respectively, for both the NMOS and PMOS. Each latchup guard ring

(including base or collector guard rings) has a diffusion width of 3 µm. Moreover, a *ThermoChuck* system with a temperature range up to 200 °C and a temperature accuracy of ±0.5 °C, is used to investigate latchup behavior under different test temperatures. All the latchup test structures are fabricated in a 0.5-µm silicided bulk CMOS process.

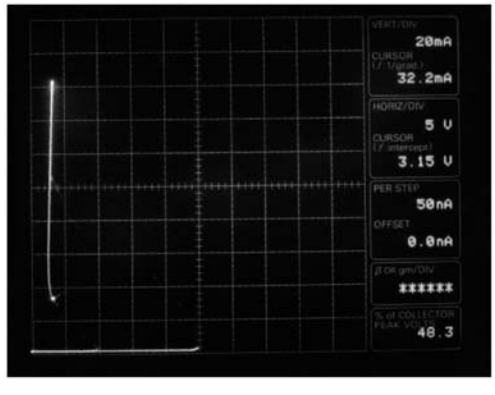
The typical latchup DC *I–V* characteristics of I/O cells with different guard ring designs, anode-to-cathode spacings, and test temperatures are shown in Figure 6.12. Figure 6.12a shows the latchup *I–V* characteristics of an I/O cell with double guard rings and an anode-to-cathode spacing of 22 µm at a temperature of 75 °C. Figure 6.12b shows the latchup *I–V* characteristics of an I/O cell with a single guard ring and an anode-to-cathode spacing of 15 µm at a temperature of 100 °C. Figure 6.12c shows the latchup *I–V* characteristics of an I/O cell without a guard



(a) (*x* axis: 5V/div.; *y* axis: 50mA/div.)



(b) (*x* axis: 5V/div.; *y* axis: 20mA/div.)



(c) (*x* axis: 5V/div.; *y* axis: 20mA/div.)

Figure 6.12 Measured latchup DC *I–V* characteristics of I/O cells with (a) double guard rings at a temperature of 75 °C, (b) a single guard ring at a temperature of 100 °C, and (c) no guard ring at a temperature of 25 °C. (Reprinted with permission from IEEE).

ring and with an anode-to-cathode spacing of 20 μm at a temperature of 25 °C. The latchup holding voltage can be extracted from the latchup *I–V* curves to evaluate the latchup immunity. The holding voltage is defined as the minimum voltage in the *I–V* curve of the latchup holding region [14]. As shown in Figure 6.12, the holding voltages are 7, 5.5, and 2.5 V, in Figure 6.12a–c, respectively. Thus, only the specified layout parameters in Figure 6.12a and b can make sure that the I/O cells are latchup-free, because their holding voltages of 7 or 5.5 V are higher than the V_{DD} normal operating voltage of 5 V. Such holding-voltage-based criteria can be used to determine the safe and compact latchup-preventing layout rules in I/O cells, such as the minimum anode-to-cathode spacing, the minimum guard ring width, and the maximum distance between the first and second guard rings, and the required guard ring designs (double guard rings, single guard ring, or no guard ring).

The relations between the holding voltage and the anode-to-cathode spacing in different guard ring designs are shown in Figure 6.13. The test temperature is 25 °C. Obviously, the holding voltage increases with the anode-to-cathode spacing. Because of the much higher holding voltages, the I/O cells with double guard rings or a single guard ring can perform much better in latchup immunity than that without the guard ring, even if there is a much longer anode-to-cathode spacing for an I/O cell without the guard ring. For example, the holding voltage of an I/O cell without the guard ring is only a small value of 3.6 V, even though the anode-to-cathode spacing is as large as 40 μm. However, the I/O cell with a single guard ring

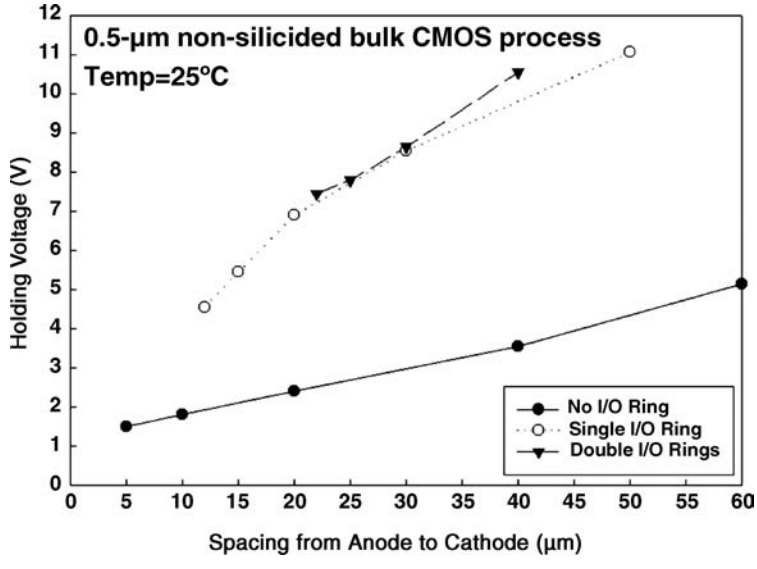


Figure 6.13 Relations between the holding voltage and the anode-to-cathode spacing with different guard ring designs. (Reprinted with permission from IEEE).

can achieve a very high holding voltage of 5.5 V (latchup-free), even if there is a much smaller anode-to-cathode spacing of 15 μm. From Figure 6.13, single guard rings are necessarily suggested (double guard rings could be optional) in layout design guidelines for latchup prevention, because the I/O cells can be latchup-free even though the anode-to-cathode spacing is as small as 15 μm. Otherwise, at least a large anode-to-cathode spacing of 60 μm is necessary for the I/O cells without guard rings to be latchup-free.

The degradations of latchup robustness due to a high test temperature are also considered for different guard ring designs, as shown in Figure 6.14. The holding voltage decreases with the temperature, whether we are considering I/O cells with double guard rings, a single guard ring, or no guard ring. Thus, the suggested layout rules must be tighter for high-temperature applications. For example, Figure 6.14 shows that the I/O cell with a single guard ring can be latchup-free (holding voltage of 5.5 V) under an anode-to-cathode spacing of 15 μm at room temperature, but it may suffer the latchup reliability issue at a high temperature of 100 °C because of its declined holding voltage (4.5 V). Thus, enlarging the anode-to-cathode spacing or using double guard rings is necessary to further improve the latchup immunity. For example, with double guard rings and an anode-to-cathode spacing of 25 μm, the I/O cell still performs very good latchup robustness at a high temperature of 125 °C because of its high holding voltages of 6.5 V (latchup-free).

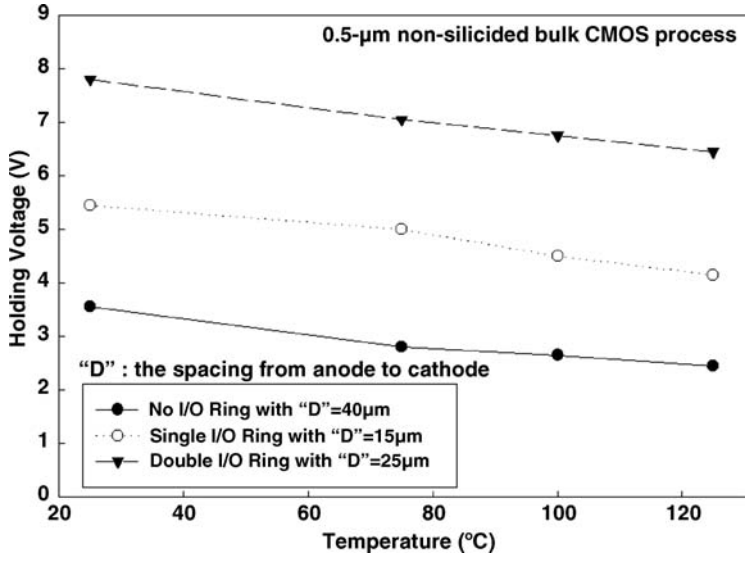


Figure 6.14 Relations between the holding voltage and the temperature with different guard ring designs. (Reprinted with permission from IEEE).

From Figures 6.13 and 6.14, the suggested layout rules for latchup prevention should include a single guard ring in the I/O cells. Compared with the I/O cells without a guard ring, although the I/O cells with a single guard ring need the additional layout area of the guard ring, it can significantly reduce the anode-to-cathode spacing. More importantly, it can perform much better in latchup robustness under a much smaller anode-to-cathode spacing, that is, a much smaller total chip layout area, no matter whether at room temperature or an elevated temperature.

6.4 Extraction of Layout Rules for Internal Circuits

6.4.1 Latchup in Internal Circuits

As I/O cells, the internal circuits could be also very sensitive to latchup. Compared with I/O cells, the internal circuits do not directly suffer, but only a portion of, the noise current injection into the bond pads. However, due to the lack of protection of the guard rings as well as the demand for high integration of circuitry, the internal circuits are often driven to be very susceptible to latchup. To efficiently suppress the latchup-susceptibility of the internal circuits, several layout guidelines need to be identified, such as the maximum distance from substrate/well pickup to the well edge (or the maximum distance from any point inside the source/drain region to the nearest well or substrate pickup), and the maximum distance between two adjacent substrate/well pickups.

Latchup can be easily initiated though any parasitic PNPN path in internal circuits. For example, a typical layout example of an inverter circuit is shown in Figure 6.15, where the latchup path goes through from the source (P + diffusion) of the PMOS to

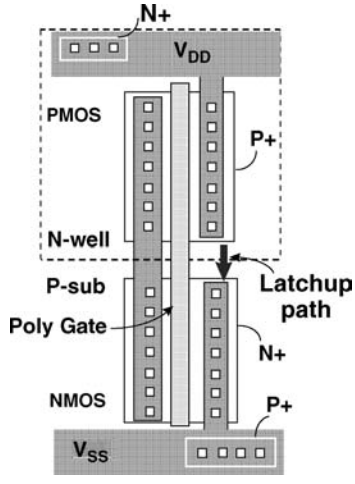


Figure 6.15 Layout example of an inverter circuit. (Reprinted with permission from IEEE).

the source (N+ diffusion) of the NMOS, as indicated by an arrow. The N-well pickups are formed by the N+ diffusions drawn in the N-well and directly connected to V_{DD}. The P-substrate pickups are formed by the P+ diffusions drawn in the P-substrate and directly connected to V_{SS}. Such an inverter circuit is the basic logic component in CMOS ICs. Once latchup is triggered on by a large enough substrate or well current, a positive feedback mechanism will lead to a large current conducting through this low-impedance PNPN path from V_{DD} (source of the PMOS) to V_{SS} (source of the NMOS). As a result, CMOS ICs will malfunction or even be burned out due to the latchup-generated high power.

N-well (P-substrate) pickups are often placed under the V_{DD} (V_{SS}) power rail of a core cell to save the layout area. However, if such well/substrate pickups under the power rail are located too far away from the well edge, the parasitic well (substrate) resistance of the parasitic vertical PNP (lateral NPN) BJTs will greatly increase, leading the parasitic SCR to be much more susceptible to latchup. Thus, it is critical to specify the maximum distance from the substrate/well pickup to the well edge (or the maximum distance from any point inside the source/drain region to the nearest well or substrate pickup).

In addition to the distance from the substrate/well pickup to the well edge, the distance between two adjacent well (substrate) pickups can also dominate the parasitic well (substrate) resistance of the parasitic vertical PNP (lateral NPN) BJTs, and of course, the latchup robustness of the internal circuits. The distance between two adjacent well (substrate) pickups represents the pickup density. More well (substrate) pickups, that is, a higher pickup density, can more efficiently shunt the well current (substrate current), thus further reducing the parasitic well (substrate) resistance of the parasitic SCR to improve the latchup immunity of the internal circuits. As a result, the maximum distance between two adjacent well (substrate) pickups should be specified in internal circuits for latchup prevention. Under this specified rule, the well/substrate pickups should be placed as compact as possible. However, it should be noted that too high a pickup density may raise the difficulties of metal routing among the devices.

6.4.2 Design of Test Structure for Internal Circuits

SCR structures are used as test structures to extract the latchup-prevention rules for internal circuits. The layout top view of the SCR test structure is shown in Figure 6.16 [15–20]. Such a test structure is used to simulate the parasitic SCR in the internal circuits. The P+ anode is used to simulate the P+ source of the PMOS, whereas the N+ cathode is used to simulate the N+ source of the NMOS. To simulate the real bias condition in CMOS ICs, the N+ well pickup connected together with the P+ anode is biased at V_{DD}, while the P+ substrate pickup connected together with the N+ cathode is biased at V_{SS}.

In order to extract the maximum distance from the substrate/well pickup to the well edge, the test structures are drawn with different distances (h_P, h_N) from the pickups to

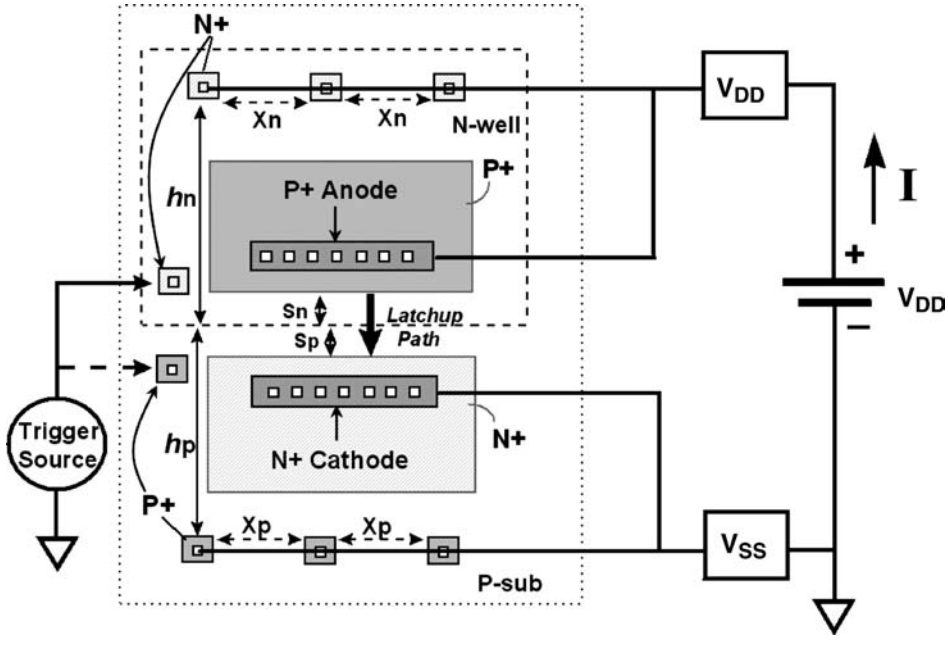


Figure 6.16 Layout top view of the SCR test structure. (Reprinted with permission from IEEE).

the N-well edge, as shown in Figure 6.16. In addition, test structures with different distances (X_P, X_N) between two adjacent pickups are also used to extract the maximum distance between two adjacent well (substrate) pickups. The P+ (N+) trigger node located in the P-substrate (N-well) region is used to investigate the latchup robustness dependency on the positive (negative) trigger current injecting into the P-substrate (N-well). By applying different trigger currents into the trigger nodes of the test structures, the threshold trigger current to initiate latchup in the test structure can be identified. The related information is useful to characterize the order of trigger current magnitude under which the test structures are most susceptible to latchup. Typically in a bulk CMOS process, a trigger current of only hundreds of microamperes can easily initiate latchup in such SCR test structures. Once latchup is triggered by the injection of the trigger current, the V_{DD} voltage level will be pulled down to around the holding voltage of the PNPN path. To avoid possible electrical-over-stress (EOS) damage of the test structure due to the huge latchup current, a current-limiting resistor of $\sim 100\,\Omega$ is suggested to be added between V_{DD} and the P+ anode of the PNPN path.

6.4.3 Latchup Immunity Dependency of the Internal Circuits

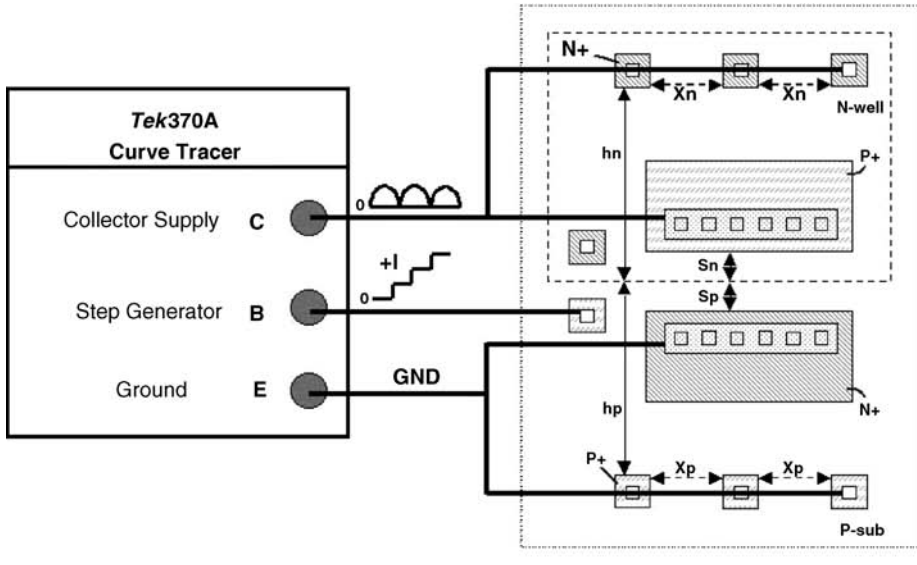
The latchup immunity dependency of internal circuits (SCR test structures) on two dominant layout parameters, i.e. distance from the substrate/well pickup to the well

edge (h_P, h_N), as well as the distance between two adjacent well or substrate pickups (X_P, X_N), are presented in this section. To identify the degradation of the latchup immunity due to the high temperature, the latchup robustness dependency on test temperature is also evaluated for different X_P and X_N. The safe and compact layout rules for latchup prevention in internal circuits can be determined upon the related experimental results, regardless of room or a high temperature. Additionally, in order to see how the trigger current waveforms influence the latchup susceptibility of the internal circuits, the relations between the threshold magnitude and the pulse width of the trigger current to initiate latchup are also investigated.

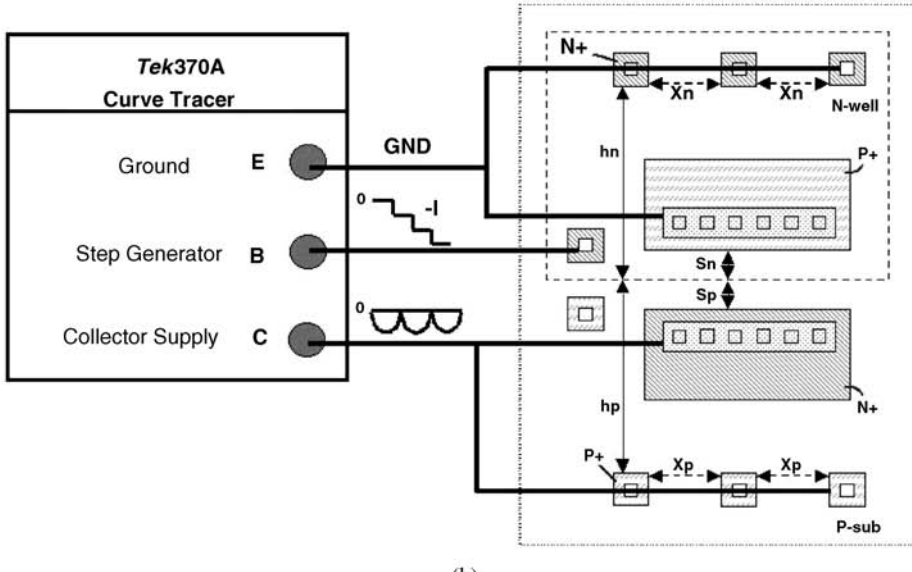
As the characterization methodologies of latchup robustness in I/O cells, the holding voltage is also extracted from the latchup DC *I–V* characteristics in internal circuits to judge if the DUT could be latchup-free. The *Tek*370A curve tracer is used to measure the latchup DC *I–V* characteristics, and the corresponding measurement setups with positive and negative trigger currents are shown in Figure 6.17a and b, respectively. The positive trigger current is applied into the P+ trigger node in the P-substrate, whereas the negative trigger current is applied into the N+ trigger node in the N-well. By applying different trigger currents into the trigger nodes, the latchup trigger voltage dependency on trigger current can be characterized. Furthermore, for the DUT biased at its DC V_{DD} operating voltage, the threshold trigger current to initiate latchup can be also identified.

The typical latchup DC *I–V* characteristics with different positive (negative) trigger currents (100 μA per step) injecting into the P-substrate (N-well) are shown in Figure 6.18a and b. The DUT is fabricated in a 0.5-μm CMOS process and has h_N/h_P of 40 μm and X_N/X_P of 20 μm. Compared with no trigger current injecting into the P-substrate/N-well, the injection of the trigger current leads to a decrease of the latchup trigger voltage, and the reduction in its magnitude is also proportional to the trigger current. In Figure 6.18, the DUT cannot be latchup-free, because the holding voltage is as small as 0.85 V, which is much smaller than the normal circuit operating voltage of 5 V, even though there is no trigger current injecting into the P-substrate/N-well.

The relations between the holding voltage and h_N/h_P (X_N/X_P) under different test temperatures are shown in Figure 6.19 (Figure 6.20). The latchup holding voltage will decrease with both h_N/h_P and X_N/X_P, because an increase of h_N/h_P or X_N/X_P can raise the parasitic well (substrate) resistance of the parasitic vertical PNP (lateral NPN) BJTs in the DUT, and of course, can degrade the latchup robustness. In addition, the experimental results also reveal that the holding voltage will decrease with the temperature, meaning that the latchup immunity will be degraded under a high test temperature. With wide ranges of h_N/h_P and X_N/X_P in Figures 6.19 and 6.20, all the holding voltages are smaller than 1 V and failed to be latchup-free, and so the internal circuits with such X_N/X_P and h_N/h_P pickup rules are still sensitive to latchup. The same tendency can be also observed in a 0.35-μm CMOS technology node, as shown in Figure 6.21. Compared with a much better latchup robustness in the I/O cells, such a weak latchup immunity in the internal circuits is mainly due to the lack of protection of

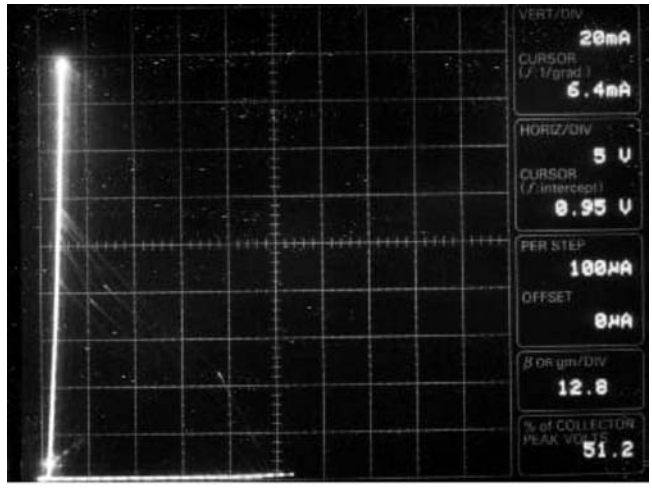


(a)

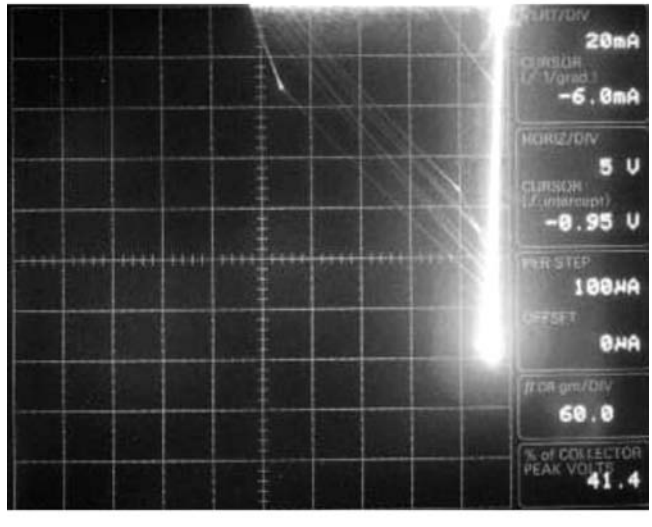


(b)

Figure 6.17 Measurement setups to measure the latchup DC *I–V* characteristics of SCR test structures with (a) a positive bias current in the P-substrate, and (b) a negative bias current in the N-well.



(a)



(b)

Figure 6.18 Typical latchup DC *I–V* characteristics with different (a) positive trigger currents (100 μA per step) injecting into the P-substrate, and (b) negative trigger currents (100 μA per step) injecting into the N-well. (Reprinted with permission from IEEE).

the guard rings, as well as the aggressive scaling of the minimum allowable distance between the PMOS and NMOS. Thus, it can be predicted that the internal circuits would be always very sensitive to latchup, unless the technology node is evolved down to 90 nm, 65 nm, or even below, where the circuit operating voltages are all lower than 1 V.

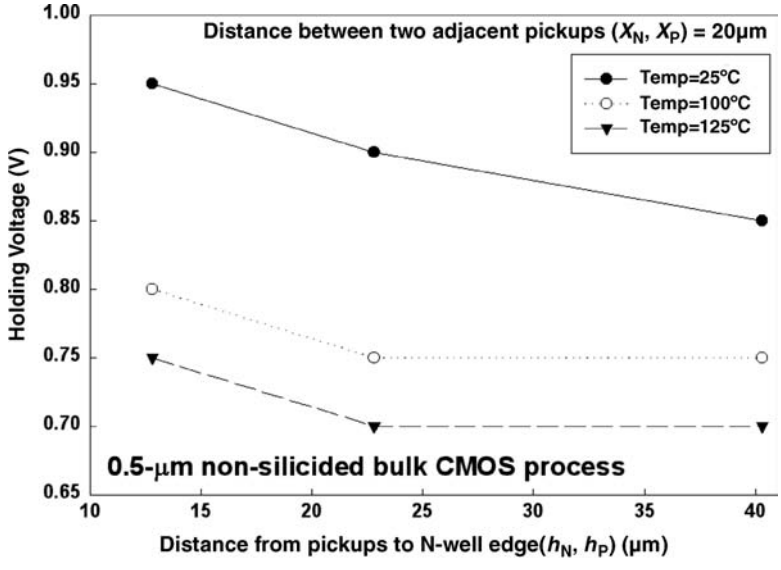


Figure 6.19 Relations between the holding voltage and h_N/h_P at different temperatures. (Reprinted with permission from IEEE).

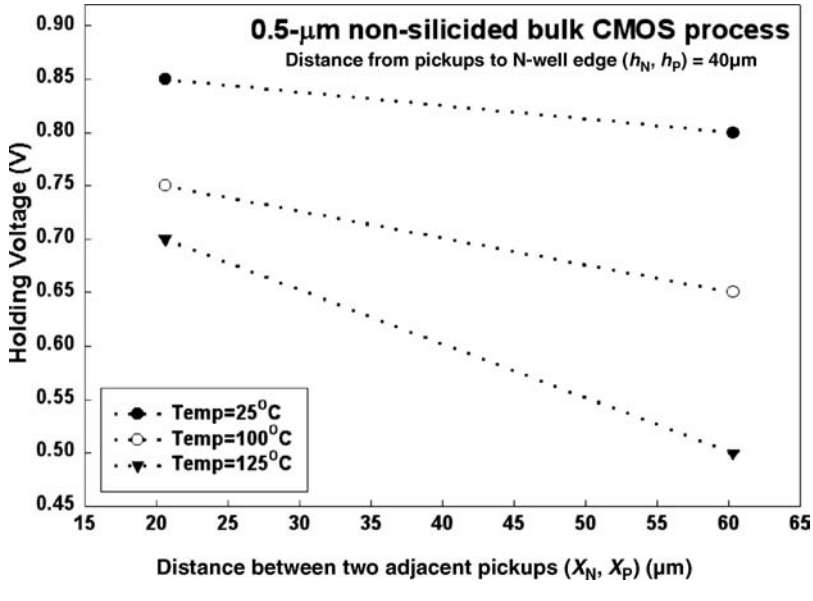


Figure 6.20 Relations between the holding voltage and X_N/X_P at different temperatures. (Reprinted with permission from IEEE).

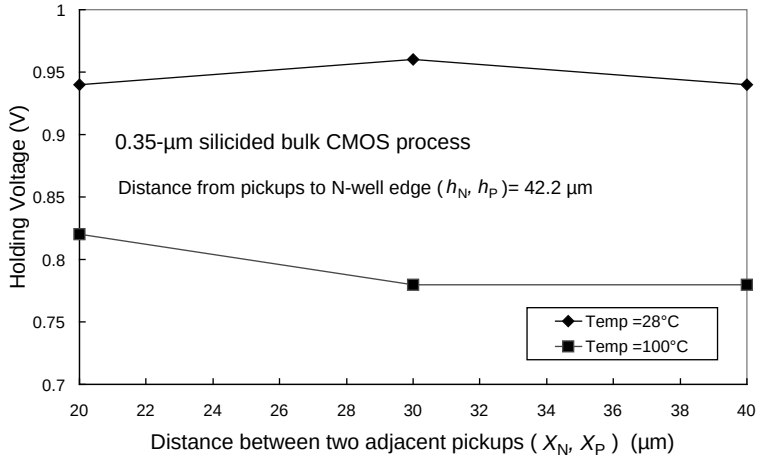


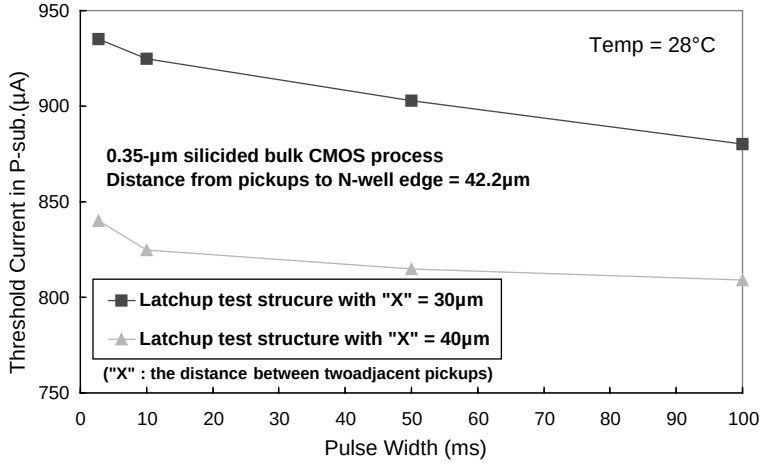
Figure 6.21 Relations between the holding voltage and X_N/X_P at different temperatures. The test structures are fabricated in a 0.35-μm CMOS technology. (Reprinted with permission from IEEE).

The relations between the threshold magnitude and the pulse width of the positive (negative) trigger current to initiate latchup are shown in Figure 6.22a and b. The threshold magnitude of the latchup trigger current will decrease with the pulse width, regardless of the positive or the negative trigger current. It is noteworthy that the threshold magnitude of the trigger current obviously increases under a very short pulse width of <10 ms, which is in agreement with the experimental results in transient-induced latchup (TLU) [21]. Thus, the pulse width could be a dominant factor to evaluate how the trigger current waveforms influence the latchup susceptibility of the internal circuits.

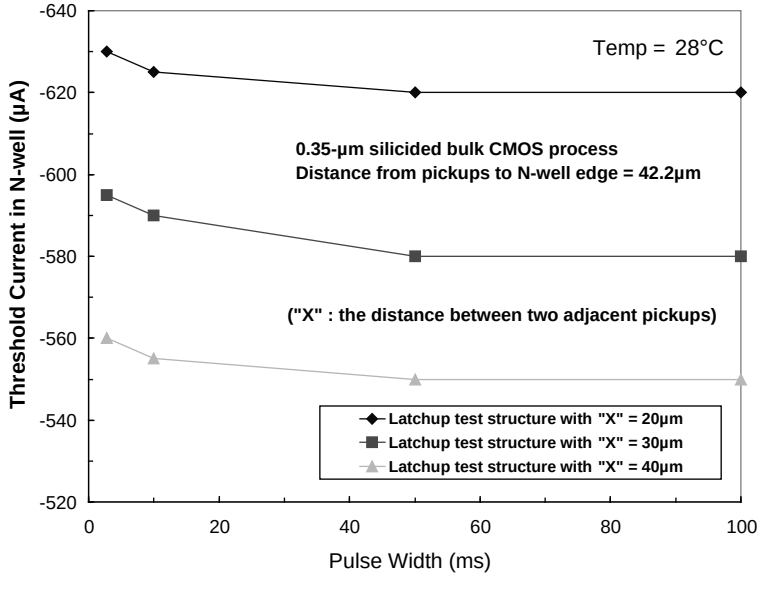
6.5 Extraction of Layout Rules between I/O Cells and Internal Circuits

6.5.1 Layout Considerations between I/O Cells and Internal Circuits

The internal circuits can be triggered onto a latchup state under the noise current injecting into the I/O pins (Figure 6.5), or under the transient overshoots occurring on the V_{DD} pin (Figure 6.6). Because of the demand of high circuitry integration in CMOS ICs, the guard rings, which are usually placed in the I/O cells for latchup immunity enhancement, are unallowable in the internal circuits. However, due to the lack of protection of guard rings, the internal circuits could be very susceptible to latchup even though there is a high pickup density (that is, small h_N/h_P or X_N/X_P). For example, the EMMI photographs of I/O-triggering latchup in the internal circuits of a CMOS ICs are shown in Figure 6.23 [22]. When the positive trigger current is applied to some I/O pin,



(a)



(b)

Figure 6.22 Relations between the threshold magnitude and the pulse width of the (a) positive, and (b) negative, trigger currents to initiate latchup. (Reprinted with permission from IEEE).

the hot spot emerges due to the latchup-induced leakage current. The zoom-in picture of the hot spot clearly indicates that the internal circuits could be very susceptible to noise current injecting into the I/O pins. As a result, it is important to find some other layout rules for greatly improving the latchup immunity in the internal circuits.

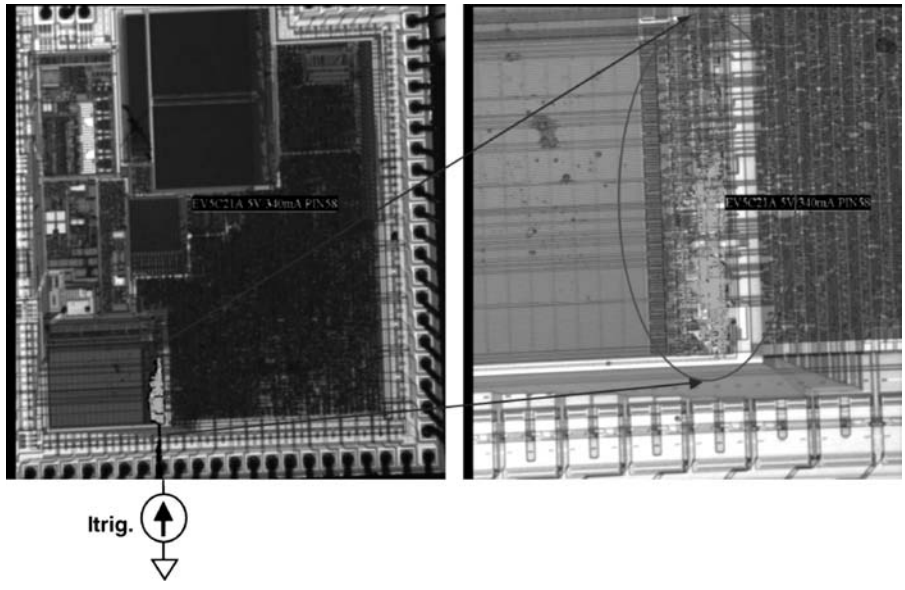


Figure 6.23 EMMI photographs of I/O-triggering latchup in the internal circuits of CMOS ICs. The hot spot indicates the location of the latchup-induced leakage current [22].

To certainly avoid the substrate current (generated from the I/O cells) firing latchup in the internal circuits, the internal circuits, in general, are kept at a large enough distance away from the I/O cells. In addition, placing additional guard rings between the I/O cells and the internal circuits can also enhance the latchup immunity in the internal circuits against the trigger currents at the I/O pins. Thus, some important layout design guidelines are often specified for between the I/O cells and internal circuits, such as the minimum spacing between the I/O and internal circuits, the guard ring designs (with or without the inserted guard rings) between the I/O and internal circuits, and the minimum width of the inserted guard rings between the I/O and internal circuits. The device cross-sectional view to show such layout requirements is shown in Figure 6.24. Before the injecting noise current can disturb the internal circuits, it needs to go through a distance along the P-substrate from the I/O cells to the internal circuits. Due to the recombination mechanism between electrons and holes in the P-substrate, the noise current, which could probably disturb the internal circuits, will decay with the spacing between the I/O cells and the internal circuits. As a result, the latchup robustness in internal circuits can be improved by enlarging the spacing between the I/O cells and the internal circuits, and thus the minimum spacing between the I/O and internal circuits needs to be determined.

Although enlarging the spacing between the I/O and internal circuits can enhance the latchup immunity of the internal circuits, a too large spacing, however, will suffer

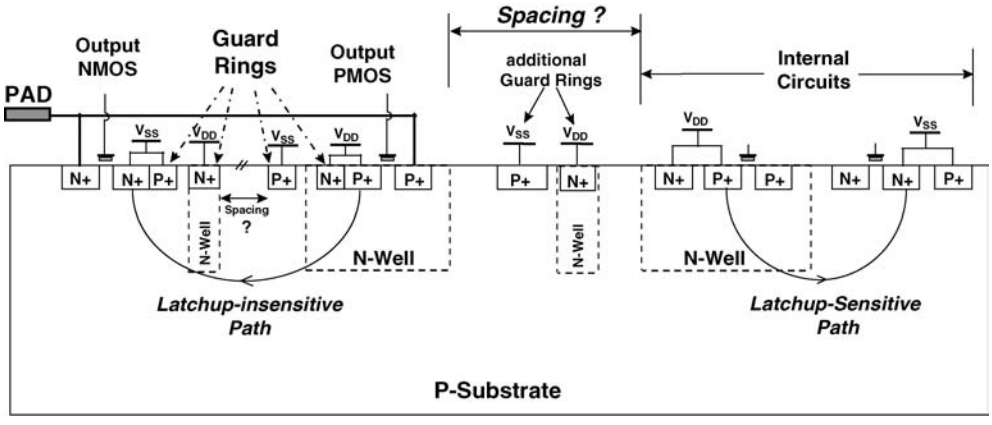


Figure 6.24 Device cross-sectional view to show the additional guard rings placed between the I/O cells and the internal circuits. (Reprinted with permission from IEEE).

the drawback of a large layout area. To solve this issue, double guard rings can be inserted between the I/O and internal circuits, as shown in Figure 6.24. The P+ guard ring is biased at V_{SS}, whereas the N+ ring located in the N-well region is biased at V_{DD}. The inserted guard rings can help collect electrons or holes (coming from the injecting noise current at the I/O pins) in the substrate before they can reach the internal circuits to fire latchup. The wider the inserted guard ring is, the better the collection efficiency the inserted guard ring has. Thus, the latchup robustness can be enhanced by placing the inserted double guard rings as compact as possible between the I/O and internal circuits. These additional guard rings also allow the possible reduction of the distance between the I/O cells and internal circuits to save layout area. To make sure of a safe and compact design rule for latchup prevention in the internal circuits, it is necessary to specify the inserted guard ring designs (with or without the inserted guard rings) and the minimum inserted guard ring width.

6.5.2 Design of Test Structure between I/O Cells and Internal Circuits

The latchup test structure shown in Figure 6.25 can be used to investigate the proper distance from the I/O cells to the internal circuits [23–25]. The latchup sensor cells (zoomed in the box) are the same SCR test structures as those shown in Figure 6.16, and they are used to simulate the parasitic SCR in internal circuits. In addition, the latchup sensors are intended to be placed in parallel to the I/O cells. Both P+ anode and N+ well pickups (N+ cathode and P+ substrate pickups) of all the latchup sensors are connected together to the same V_{DD} (V_{SS}) power rail. When the trigger current is applied at the I/O pins, the V_{DD} power rail connected to the latchup sensor cells is monitored to judge whether latchup is triggered on, or not. If the trigger current

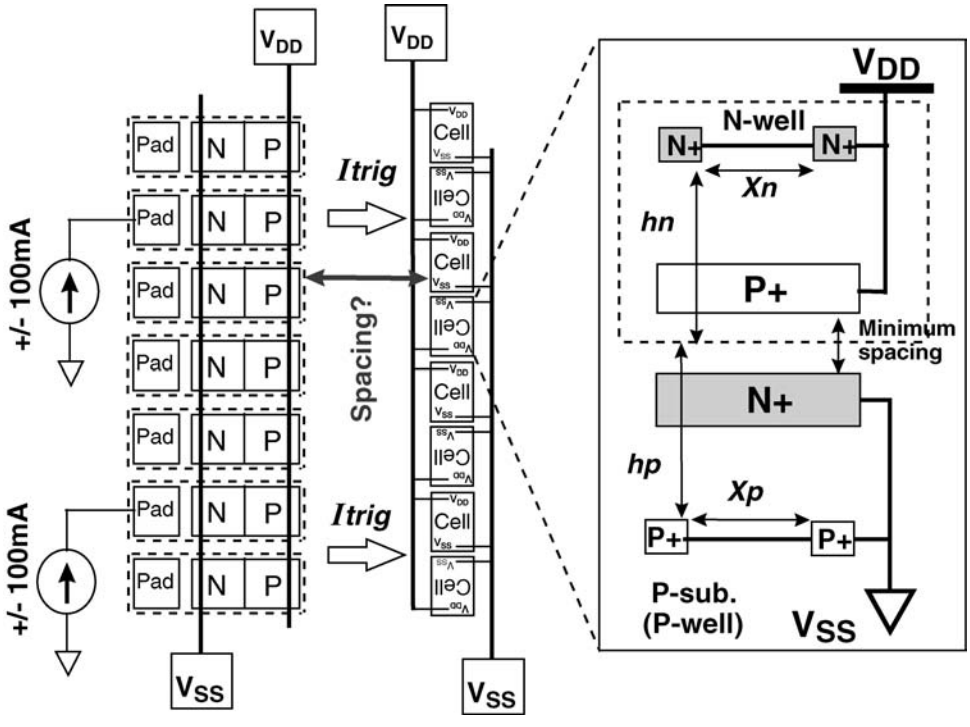


Figure 6.25 Latchup test structure to evaluate the proper layout spacing from the I/O cell to the internal circuits. (Reprinted with permission from IEEE).

injecting into the I/O pins is large enough to initiate latchup in any one of the latchup sensors, the V_{DD} will be pulled down to about the holding voltage of the latchup sensor. Therefore, the threshold trigger current to fire latchup in internal circuits (simulated by the latchup sensor cells) can be determined by this test structure.

To extract the minimum spacing between the I/O and internal circuits, test structures need to be prepared with different spacing. Additionally, the latchup sensor cells can be drawn with different pickup distances (X_N, h_N, X_P, h_P) to investigate how a large trigger current at the I/O pin can fire latchup in the internal circuits under a specified distance from the I/O cells to the internal circuits. In general, the latchup sensor cells, drawn with a smaller X_N, h_N, X_P, and h_P, need a higher trigger current at the I/O cells to cause latchup in the internal circuits. By using this method, the design rules about the pickup distances (X_N, h_N, X_P, h_P) of the internal circuits can be extracted more meaningfully to meet the real circuit operating condition in CMOS ICs.

To extract the minimum width of the inserted guard ring between the I/O and internal circuits, the same test structures as shown in Figure 6.25 but with different inserted guard ring widths also need to be prepared, as shown in Figure 6.26. The P+ guard

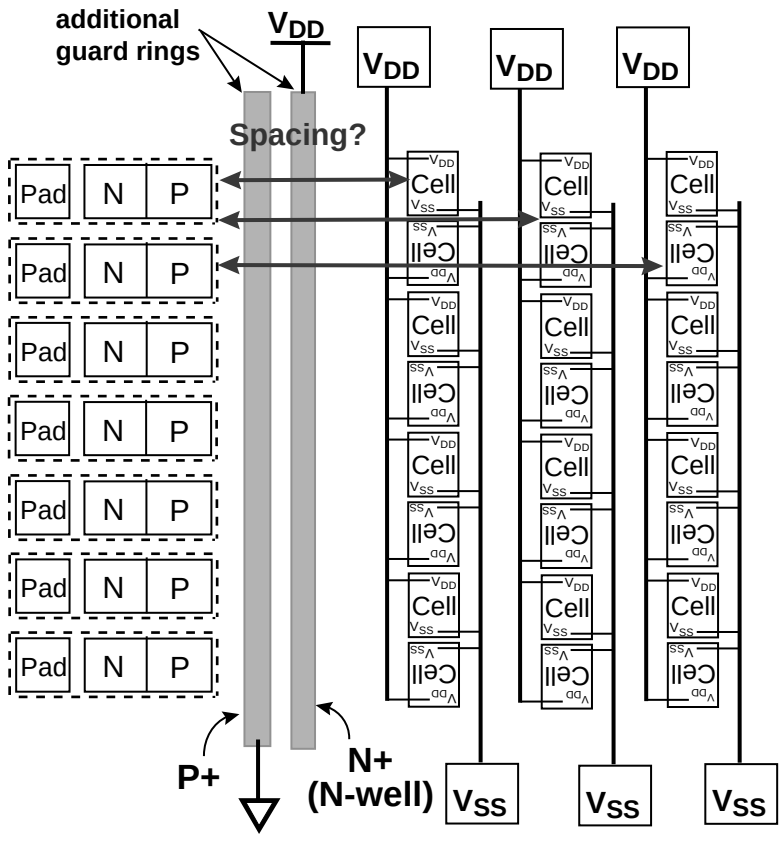


Figure 6.26 Latchup test structure to extract the minimum width of the inserted guard ring between the I/O and the internal circuits. (Reprinted with permission from IEEE).

ring is biased at V_{SS}, whereas the N+ guard ring located in the N-well region is biased at V_{DD}, as those shown in Figures 6.24 and 6.26. It is noteworthy that the inserted guard ring should be placed as compact as possible to gain the best latchup robustness under a specified spacing between the I/O and internal circuits. As a result, the most compact but still safe design rules for latchup prevention can be determined. In addition, the I/O cells in these test structures need to be confirmed latchup-free in advance, or otherwise the I/O cells could suffer the latchup issue during the measurements.

6.5.3 Threshold Latchup Trigger Current Dependency

The latchup immunity dependency of internal circuits on three major layout parameters for latchup robustness enhancement, i.e. the spacing between the I/O and internal circuits, the guard ring designs (with or without the inserted guard rings)

between the I/O and internal circuits, and the minimum width of the inserted guard rings between the I/O and internal circuits, are presented in this section. Additionally, the relations between the threshold magnitude and the pulse width of the trigger current to initiate latchup under different guard ring designs are also investigated. As a result, how the trigger current waveforms (injecting into the I/O pins) influence the latchup susceptibility of internal circuits can be well characterized.

From the above measured results in Section 6.3, the I/O cells with single or double guard rings can easily gain a holding voltage greater than V_{DD} (that is, latchup-free). Therefore, the I/O cells with guard rings never suffer the latchup problem. However, the internal circuits with high pickup density are still sensitive to latchup, because their holding voltages are all very small, about $\sim$1 V only, as described in Section 6.4. Therefore, an interesting question is how a large trigger current injecting at the I/O pins will initiate latchup in the internal circuits, and how well the latchup immunity will be improved by adding the guard rings or enlarging the spacing between the I/O and internal circuits. Thus, several testchips are drawn with different layout spacings from the I/O cells to the internal latchup sensors, ranging from 15 to 60 μm. The latchup sensors are specifically drawn with a large $h_N/h_P(X_N/X_P)$ of 42.2 μm (20 μm) to make sure of a high latchup susceptibility for the sensors. The I/O cells are only surrounded by a single guard ring with an anode-to-cathode spacing of 14.4 μm. The width of the additional P+ (N+) inserted guard ring is kept at 3 μm (3.4 μm). All the test chips are fabricated in a 0.35-μm CMOS process, and the test temperature is 30 °C. These I/O cells are already confirmed in advance that their holding voltages are higher than V_{DD} (3.5 V), that is, latchup-free. Thus, it is sure that the noise current injecting into the I/O pins never triggers on latchup in the I/O cells, but could only do so in the internal circuits.

The measurement setup to extract the latchup-prevention rules between the I/O and internal circuits is shown in Figure 6.27. The test procedures are in compliance with the JEDEC latchup trigger current test [11], as introduced in Section 6.2. The *Keithley* 2410 current source with a maximum power delivery of 21 W and a current source range from $\pm$50 pA to $\pm$1.05 A is used to provide the required trigger current pulses at the I/O cells. Three independent DC power supplies are used to separately bias the I/O cells, the inserted guard rings, and the latchup sensors. A current-limiting resistor of 100 Ω is connected between the V_{DD} power supply and the internal latchup sensors to limit a huge latchup current, avoiding possible EOS damage of the latchup sensors. The *HP*54602A oscilloscope with a bandwidth of 150 MHz is used to monitor the voltage waveform of the input current pulse at the I/O pin (CH1), and to monitor the voltage waveform of the V_{DD} power rail of the latchup sensors (CH2). When a positive (negative) trigger current injects into the I/O pins, the typical transient curves monitored by the oscilloscope are shown in Figure 6.28a and b. If latchup is fired in the internal latchup sensors by the trigger current applied at the I/O pins, the voltage level of CH2 will drop from V_{DD} to the voltage level around the holding voltage ($\sim$1 V) of the latchup sensors. Otherwise, if latchup is not triggered on in the internal latchup sensors, the voltage level of CH2 remains at the original V_{DD} voltage level (5 V for the

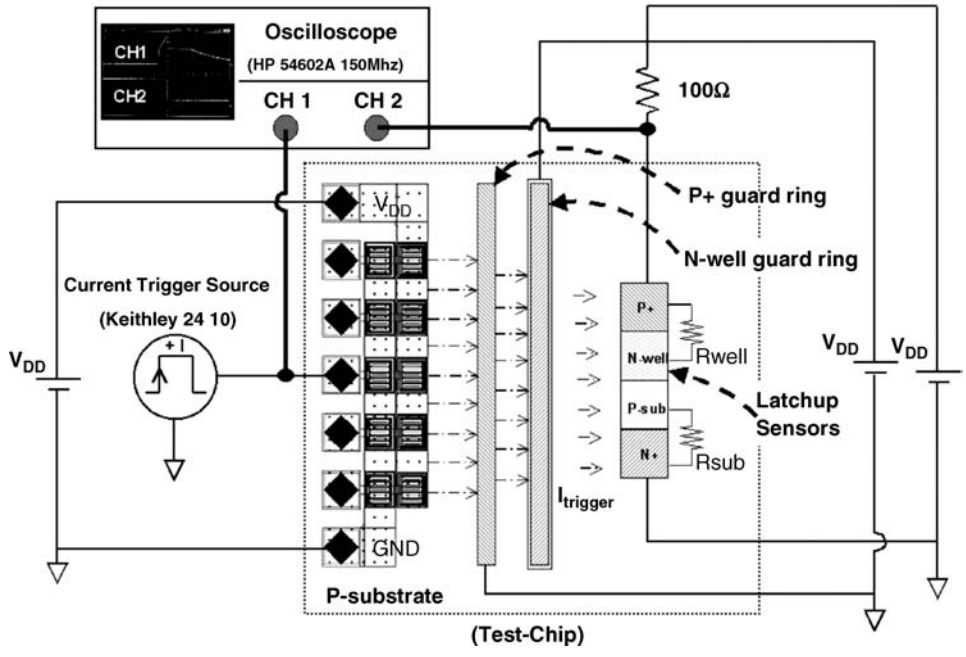
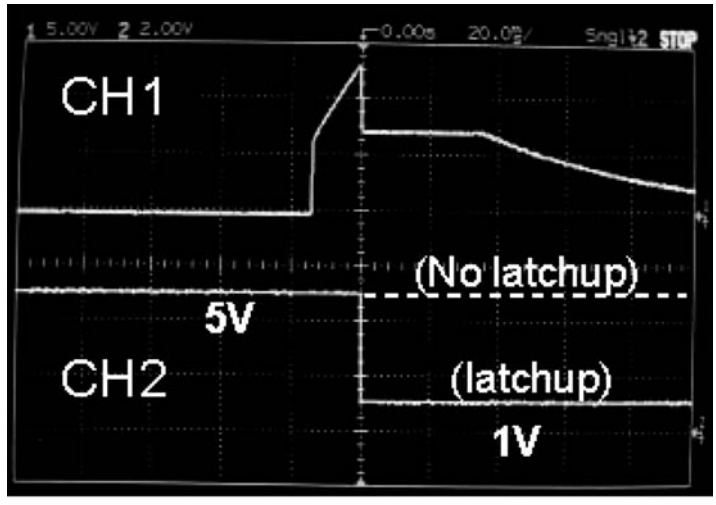


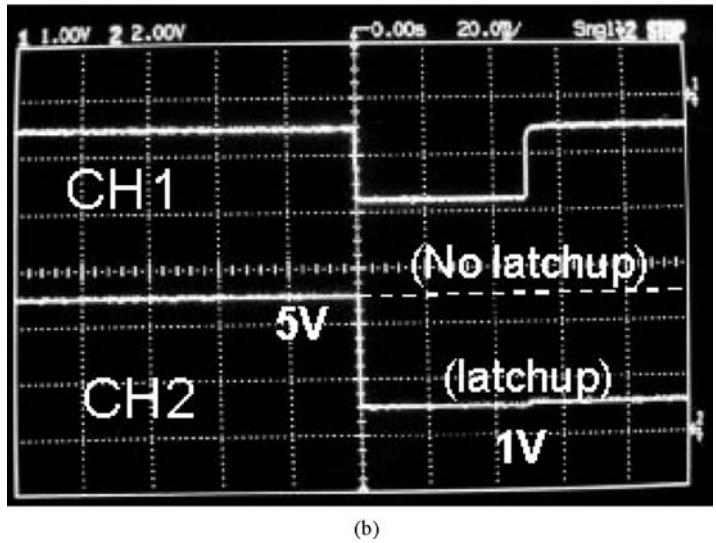
Figure 6.27 Measurement setup to extract the latchup-prevention rules for between the I/O and internal circuits. (Reprinted with permission from IEEE).

0.5-μm technology node). By adjusting the current magnitude of the trigger current applied at the I/O pins, the critical (threshold) trigger current at the I/O pins to fire latchup in internal latchup sensors can be found.

The relations between the threshold positive (negative) trigger current and the spacing from the I/O cells to the latchup sensors with different guard ring designs are shown in Figure 6.29a and b. The pulse width of the trigger current is 50 ms in compliance with the JEDEC standard [11]. Compared to the test structures without the inserted guard rings, the test structures with the additional inserted guard rings can gain a much higher threshold trigger current to fire latchup in the internal circuits (latchup sensors). Such an increase of threshold trigger current by adding additional inserted guard rings is much higher than that obtained by simply enlarging the distance between the I/O and internal circuits, regardless of a positive or negative trigger current test. For example, even with a small distance of 30 μm from the I/O cells to the internal circuits, the test structures with the additional inserted guard rings can still meet the requirements of the JEDEC specification (threshold trigger current $> \pm 100$ mA). Without such additional inserted guard rings, however, the test structures failed to pass the JEDEC positive trigger current test, even though the distance between the I/O and internal circuits is as high as 60 μm where the threshold trigger current is only 38 mA. Therefore, it is strongly recommended that the additional inserted double guard rings



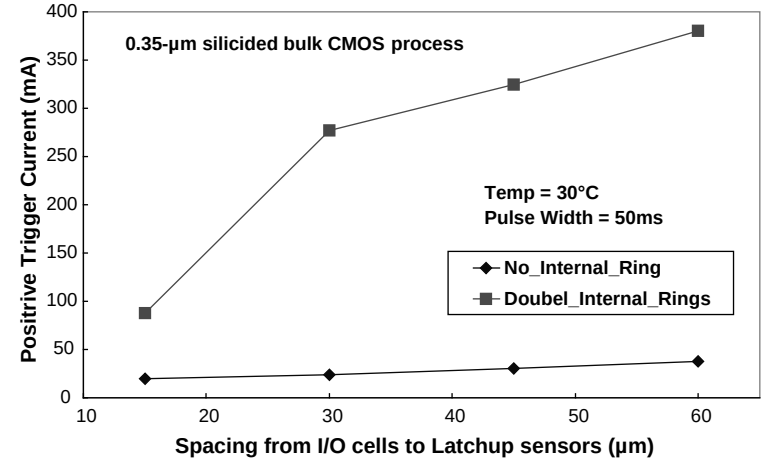
(a)



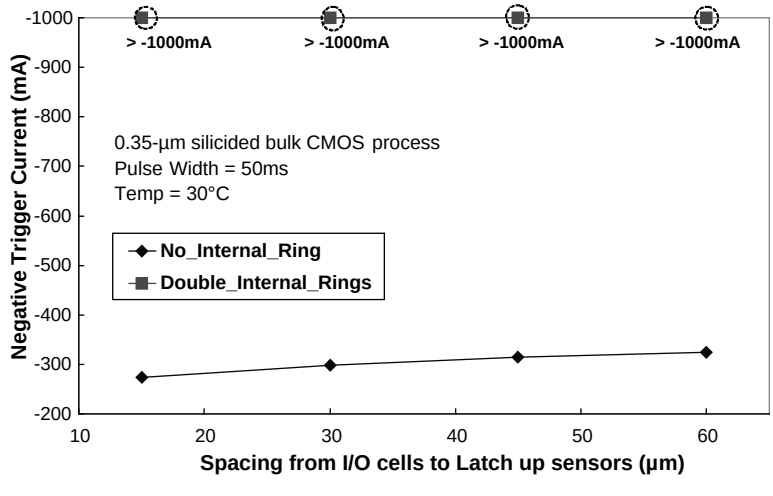
(b)

Figure 6.28 Typical transient curves monitored by the oscilloscope with a (a) positive, and (b) negative, trigger currents injecting into the I/O pins. CH1 is the voltage waveform of the input current pulse at the I/O pins, and CH2 is the voltage waveform of the V_{DD} power rail of the latchup sensors.

should be placed between the I/O cells and internal circuits to maintain high latchup immunity. Not only can they significantly improve the latchup immunity of the internal circuits, but also can save more layout area by reducing the spacing from the I/O cells to the internal circuits.



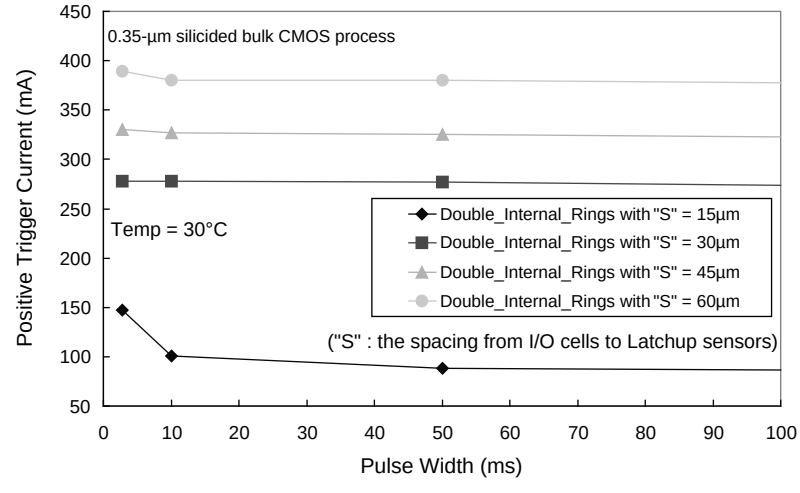
(a)



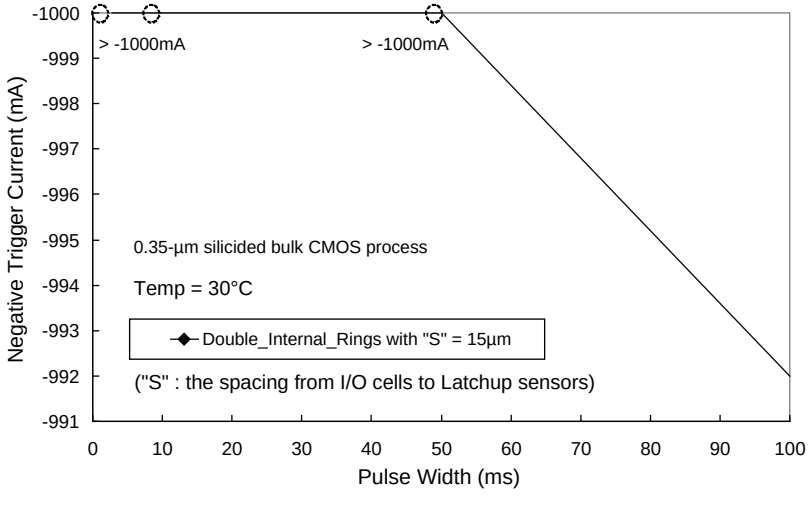
(b)

Figure 6.29 Relations between the (a) threshold positive trigger current and the spacing from the I/O cells to the latchup sensors, and (b) threshold negative trigger current and the spacing from the I/O cells to the latchup sensors, with different inserted guard ring designs. (Reprinted with permission from IEEE).

The relations between the threshold positive/negative trigger current and its pulse width under different spacings from the I/O cells to the internal circuits are shown in Figures 6.30 and 6.31. The test patterns in Figure 6.30 have the inserted double guard rings, but is opposite (no inserted guard rings) in Figure 6.31. In most cases there is a fairly obvious increase of threshold positive/negative trigger current for pulse widths shorter than 10 ms. This tendency is consistent with the characteristic in TLU [21] that



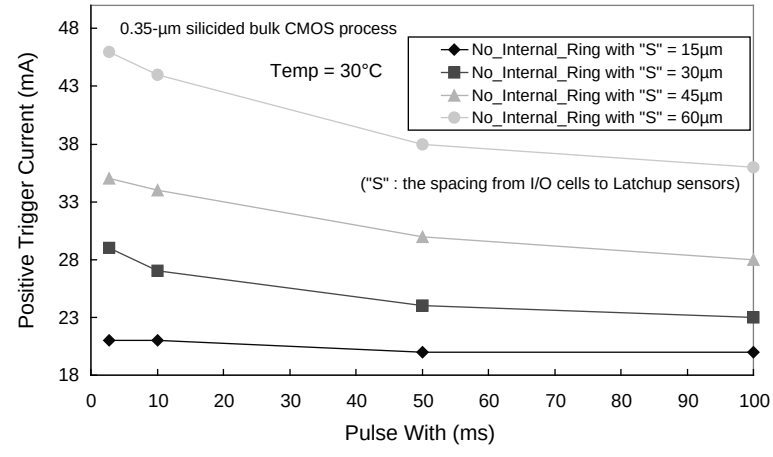
(a)



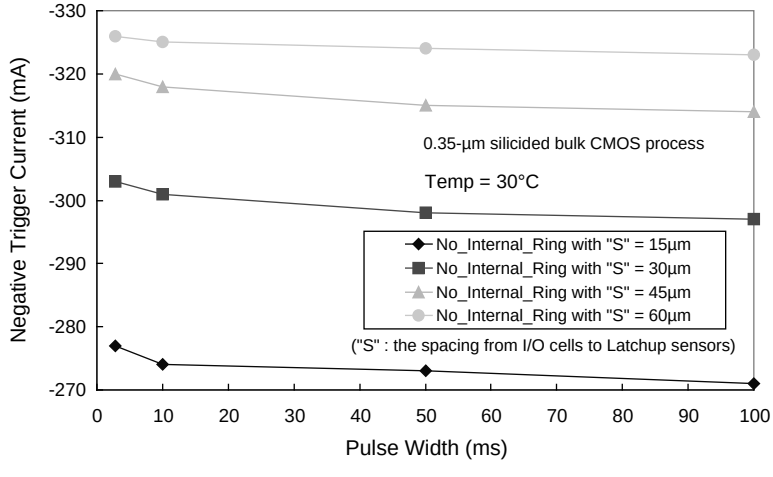
(b)

Figure 6.30 For the test patterns with additional inserted double guard rings, the relations between the (a) threshold positive trigger current and its pulse width, and (b) threshold negative trigger current and its pulse width, with different spacings from the I/O cells to the internal circuits. (Reprinted with permission from IEEE).

a "transient" (short pulse width) trigger voltage/current needs a large voltage/current magnitude to initiate TLU in comparison with the quasi-static latchup. In addition, as shown by the above measured results in Figure 6.29, it is proven once again that the use of additional inserted guard rings can gain high threshold positive/negative trigger currents, thus improving the latchup immunity of the internal circuits.



(a)



(b)

Figure 6.31 For the test patterns without inserted double guard rings, the relations between the (a) threshold positive trigger current and its pulse width, and (b) threshold negative trigger current and its pulse width, with different spacings from the I/O cells to the internal circuits. (Reprinted with permission from IEEE).

To investigate how an inserted guard ring width impacts the latchup robustness of the internal circuits, the relations between the threshold positive trigger current and the inserted P+ guard ring width are shown in Figure 6.32. The spacing from the I/O cells to the internal circuits is at a fixed distance of 30 μm. The width of the inserted P+ guard ring is drawn with 3, 6, and 9 μm to investigate the guard ring efficiency, whereas the width of the other inserted N+ (with an N-well) guard ring is kept at 3.4 μm. Due to

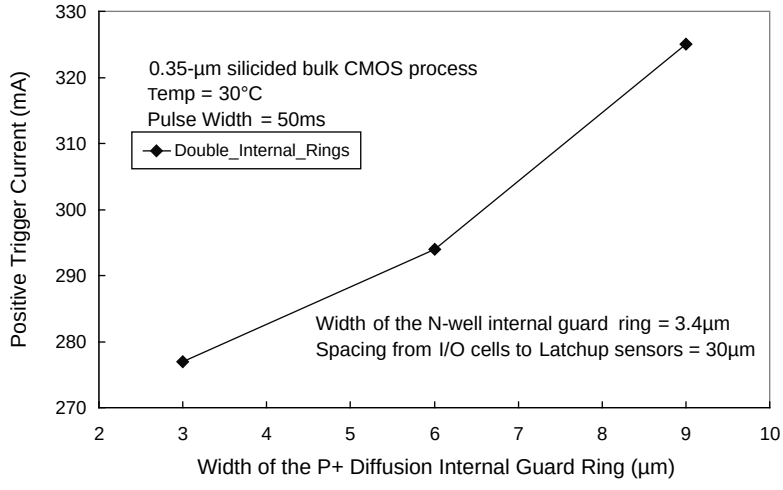


Figure 6.32 Relations between the threshold positive trigger current and the inserted P + guard ring width. (Reprinted with permission from IEEE).

the better guard ring efficiency for a wider guard ring width, the threshold trigger current increases with the inserted guard ring width. For example, when the P+ guard ring width increases from 3 to 9 µm, the threshold positive trigger current can be enhanced from 275 to 325 mA. Thus, the additional inserted double guard rings should be drawn as wide as possible in the real chip layout under a specified spacing from the I/O cells to the internal circuits. Based on this layout methodology, one set of compact (area-efficient) but still safe latchup-prevention layout rules can be established between the I/O and the internal circuits.

6.6 Conclusion

Methodologies to extract compact and safe layout guidelines for latchup prevention are introduced for I/O cells, for internal circuits, and for between I/O cells and internal circuits. For the I/O cells, the extraction methodologies can be performed to determine the required guard ring designs (double guard rings, single guard ring, or no guard ring), the minimum guard ring width, the maximum distance between the base and collector guard rings, and the minimum anode-to-cathode spacing. For the internal circuits cells, the methodologies can help extract the maximum distance from substrate/well pickup to the well edge (or the maximum distance from any point inside the source/drain region to the nearest well or substrate pickup), and the maximum distance between two adjacent substrate/well pickups. For between the I/O cells and internal circuits, the methodologies can also help determine the minimum spacing between the I/O and internal circuits, the guard ring designs (with or without

the inserted guard rings) between the I/O and internal circuits, and the minimum width of the inserted guard rings between the I/O and internal circuits.

From all the experimental results presented in this chapter (0.35 or 0.5-μm CMOS processes), the I/O cells possess a good latchup robustness by simply using a single guard ring to surround the NMOS and PMOS in I/O cells, even though there is only a small anode-to-cathode spacing under a very high temperature of 125 °C. Therefore, the I/O cells can be drawn with only a single guard ring to save layout area but still have prominent latchup robustness. The internal circuits, however, are always sensitive to latchup even with a high pickup density. As a result, the additional inserted guard rings should be added between the I/O cells and internal circuits to further improve the latchup immunity of the internal circuits. The introduced methodologies can be easily implemented in all different CMOS technology nodes, and the safe/compact design rules for latchup prevention can be specified upon the requirements of miscellaneous specifications.

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7

Special Layout Issues for Latchup Prevention

As mentioned in Chapter 6, the design guidelines for latchup prevention usually focus on I/O cells, internal circuits, and between I/O and internal circuits. However, unexpected latchup issues still potentially exist, even though the ICs layout designs are fully in compliance with the aforementioned latchup design guidelines. This chapter specifically introduces such special layout issues which need to be noted. Neglecting these layout issues could draw an unanticipated latchup problem. In addition, the corresponding solutions to these unexpected latchups are also given. By using these, IC designers could prevent possible design mistakes, eliminate the waste of masks and wafers, and decrease the time to market for products.

7.1 Latchup between Two Different Power Domains

Conventional latchup is usually referred to the so-called "V_{DD}-to-GND" latchup, meaning that the PNPN latchup path goes through from the V_{DD} (P+ source of the PMOS) to the GND (the N+ source of the NMOS). Although usually unexpected, however, latchup could also happen between two different power domains, leading to the so-called "$V_{DD,H}$-to-$V_{DD,L}$" latchup, as shown in Figure 7.1. $V_{DD,H}$ ($V_{DD,L}$) represents the higher (lower) power supply voltage in multiple-power CMOS ICs. Two different power supply voltages are commonly seen in the mixed-signal design requirements [1], where the I/O buffer is usually designed with thick-oxide devices powered by $V_{DD,H}$, whereas the internal circuitry is designed with thin-oxide devices powered by $V_{DD,L}$. Unlike the conventional latchup path going through from V_{DD} to GND, such a specific latchup path goes through from $V_{DD,H}$ (P+ source of the PMOS) to $V_{DD,L}$ (N+ well contact). Once $V_{DD,H}$-to-$V_{DD,L}$ latchup occurs, a huge latchup

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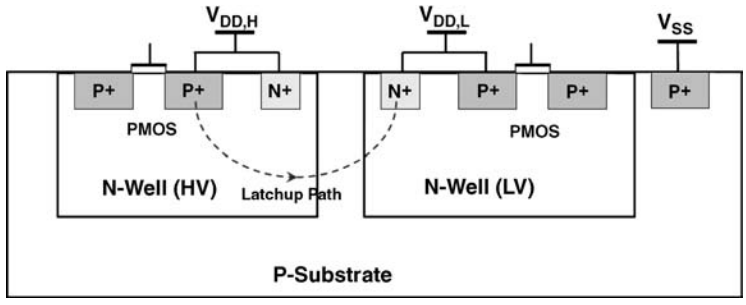

Figure 7.1 Device cross-sectional view to show the latchup path between two different power domains, $V_{DD,H}$ and $V_{DD,L}$.

current will conduct through from $V_{DD,H}$ to $V_{DD,L}$, leading to temporary malfunction or permanent damage in the CMOS ICs.

7.1.1 Practical Examples

Practical failure returns have proven such $V_{DD,H}$-to-$V_{DD,L}$ latchup issues [2–3] in mixed-voltage I/O circuitry. For example, the schematic diagram of an I/O buffer with a 3.3 V driving capability and 5 V tolerance is shown in Figure 7.2 [2]. This I/O buffer

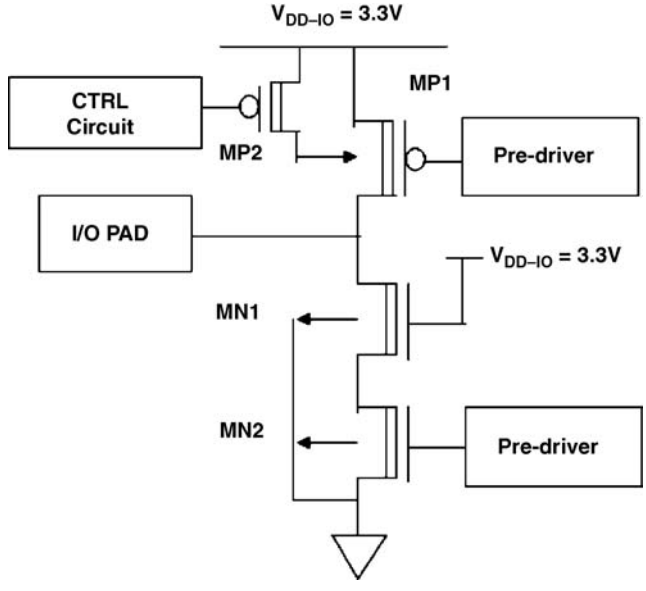

Figure 7.2 Schematic diagram of an I/O buffer with a 3.3 V driving capability and 5 V tolerance. (Reprinted with permission from C.-N. Wu, H.-M. Chou, and M.-C. Chang, "Latch-up failure path between power pins in the mixed-voltage process," *Proceedings of the IEEE International Reliability Workshops*, IEEE, Piscataway, NJ. © 2003 IEEE).

consists of two cascade NMOS transistors (MN1 and MN2) and a PMOS transistor (MP1) with a floating N-well [4]. By connecting the gate of MN1 to V_{DD}_IO (that is, $V_{DD,H}$) of 3.3 V, and the gate of MN2 to the pre-driver output, the gate oxide and hot carrier overstress can be avoided on MN1 or MN2 under a 5 V application for the input mode. The floating N-well of MP1 is connected to V_{DD}_IO through a control circuit (MP2). MP2 can bias the floating N-well to 3.3 V when the voltage on the I/O pad is smaller than 3.3 V. However, if the voltage on the I/O pad is higher than 3.3 V, MP2 will bias the floating N-well as the input voltage. As a result, there is no gate oxide overstress on MP1 when this I/O buffer receives a 5 V signal.

With the JEDEC latchup trigger current test [5], latchup failure is found between this I/O buffer and the internal circuits. The corresponding hot spot picture and device cross-sectional view are shown in Figure 7.3. The hot spot picture is monitored by the emission microscope (EMMI), indicating that the latchup current path goes through from V_{DD}_IO (3.3 V) in the I/O buffer, to V_{DD}_core (that is, $V_{DD,L}$) in the internal circuitry. In the parasitic SCR between V_{DD}_IO and V_{DD}_core, the parasitic vertical PNP BJT (VPNP) is formed with the source of MP1 connected to V_{DD}_IO (emitter), the N-well (NW2) connected to V_{DD}_IO via MP2 (base), and the P-substrate connected to V_{SS} (collector). The parasitic horizontal NPN BJT (LNPN) is formed with the NW1 connected to the V_{DD}_core (emitter), the P-substrate connected to the V_{SS} (base), and the NW2 connected to V_{DD}_IO via MP2 (collector). The resistor, R1, represents the local substrate contact rings with a higher resistance due to the narrow silicided diffusions. The diode, DW, represents the parasitic diode formed with NW1 and the

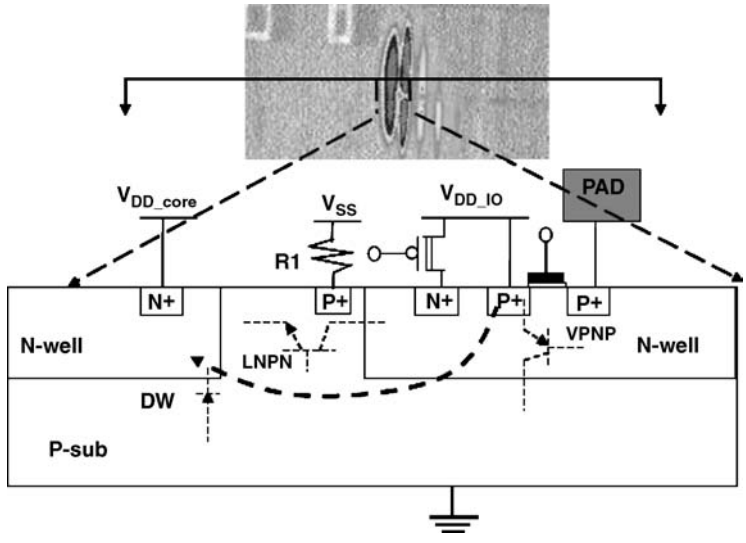

Figure 7.3 Hot spot picture and device cross-sectional view to show the latchup failure between the I/O buffer and the internal circuits. (Reprinted with permission from C.-N. Wu, H.-M. Chou, and M.-C. Chang, "Latch-up failure path between power pins in the mixed-voltage process," *Proceedings of the IEEE International Reliability Workshops*, IEEE, Piscataway, NJ. © 2003 IEEE).

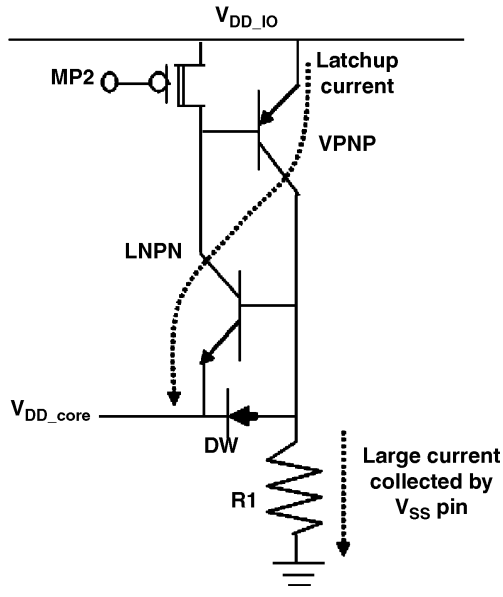

Figure 7.4 Equivalent schematic diagram to show the latchup failure between the I/O buffer and the internal circuits. (Reprinted with permission from C.-N. Wu, H.-M. Chou, and M.-C. Chang, "Latch-up failure path between power pins in the mixed-voltage process," *Proceedings of the IEEE International Reliability Workshops*, IEEE, Piscataway, NJ. © 2003 IEEE).

P-substrate. The corresponding equivalent schematic diagram is illustrated in Figure 7.4.

For the positive trigger current test, the injecting holes will inject to NW2 from the P+ drain of MP1, and subsequently be collected by V_{SS} through R1. As a result, the resulting hole current flow can induce voltage across R1. If the hole current is large enough to cause a voltage drop higher than the V_{DD}_core + V_f (the forward-biased voltage of DW), the emitter/base junction (DW) of LNPN will be forward-biased to turn on the LNPN. Afterwards, the turn-on LNPN also injects large number of electrons into NW2, turning on the VPNP. Thus, a positive-feedback regeneration mechanism leads the latchup to be triggered on between V_{DD}_IO (3.3 V) in the I/O buffer, and V_{DD}_core in internal circuitry. For the negative trigger current test, a similar triggering mechanism can be found. For instance, the electrons will first inject into the P-substrate, and subsequently be collected by V_{DD}_IO through NW2. Thus, the resulting electron current will first lead the emitter/base junction of VPNP to be forward-biased, turning on the VPNP. The turn-on VPNP subsequently provides a large numbers of holes injecting into the NW to trigger on LNPN, further driving the parasitic SCR into the latchup state between V_{DD}_IO and V_{DD}_core.

The "$V_{DD,H}$-to-$V_{DD,L}$" latchup issues have been verified in this 5 V-tolerance I/O library with three technology nodes: 0.13, 0.18, and 0.25 μm CMOS technologies. The latchup test results are summarized in Table 7.1. V_{Dmax} is defined as the voltage difference of V_{DD_IO} and V_{DD}_core plus 10% tolerance. Furthermore, the measured

Table 7.1 Summary of latchup test results in a 5 V-tolerance I/O library with three technology nodes: 0.13, 0.18, and 0.25 μm CMOS technologies. (Reprinted with permission from C.-N. Wu, H.-M. Chou, and M.-C. Chang, "Latch-up failure path between power pins in the mixed-voltage process," *Proceedings of the IEEE International Reliability Workshops*, IEEE, Piscataway, NJ. © 2003 IEEE).

Process	0.25 μm	0.18 μm	0.13 μm
Latchup test result	Pass	Fail	Fail
System voltage (V_{DD_IO}, V_{DD_core})	3.3 V, 2.5 V	3.3 V, 1.8 V	3.3 V, 1.2 V
$V_{Dmax} = (V_{DD\_IO}–V_{DD\_core}) + 10\%$	0.9 V	1.7 V	2.3 V
Holding voltage	1.06 V	0.71 V	0.92 V

DC latchup *I–V* characteristics between V_{DD_IO} and V_{DD}_core with these three technology nodes are also shown in Figure 7.5, from which the holding voltage can be extracted, as listed in Table 7.1. The test results show that only the DUT implemented with the 0.25 μm process can pass the test, but fails to pass for 0.13 and 0.18 μm processes. To make sure the occurrence of latchup between V_{DD_IO} and V_{DD_core}, the V_{Dmax} ($V_{DD\_IO}–V_{DD\_core} + 10\%$) should be higher than the holding voltage, which is the required minimum voltage to sustain latchup occurrence [6–8]. For the 0.25 μm process, because the V_{Dmax} (0.9 V) is smaller than its corresponding holding voltage (1.06 V), the DUT can pass the latchup test due to no potential risk of latchup (that is, latchup-free) between V_{DD_IO} and V_{DD_core}. For 0.13 and 0.18 μm processes, on the contrary, because V_{Dmax} isgreater than its corresponding holding voltage, the DUT fails to pass the latchup test due to the existence of potential latchup risks between V_{DD_IO} and V_{DD_core}. It was found that V_{DD_IO}-to-V_{DD_core} latchup occurs in the 0.25 μm process if V_{Dmax} is increased up to greater than the holding voltage, whereas there is no latchup in the 0.13 and 0.18 μm processes if V_{Dmax} is

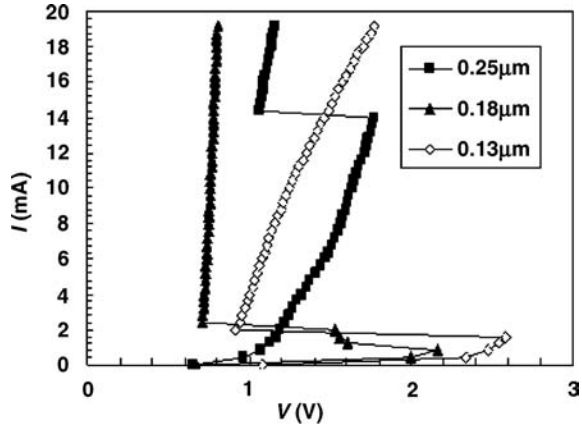

Figure 7.5 Measured DC latchup *I–V* characteristics between V_{DD_IO} and V_{DD_core} with three technology nodes: 0.13, 0.18, and 0.25 μm CMOS technologies. (Reprinted with permission from C.-N. Wu, H.-M. Chou, and M.-C. Chang, "Latch-up failure path between power pins in the mixed-voltage process," *Proceedings of the IEEE International Reliability Workshops*, IEEE, Piscataway, NJ. © 2003 IEEE).

decreased down to lower than the corresponding holding voltages. This evidence proves once again that latchup indeed occurs between V_{DD_IO} and V_{DD_core}.

7.1.2 Suggested Solutions

To suppress the latchup susceptibility between two different power domains, additional double guard rings can be inserted between two different N-wells (NW1 and NW2). The device cross-sectional view when inserting double guard rings to achieve the latchup-free layout plan is shown in Figure 7.6. The P + guard ring is connected to GND, and the N + /N-well guard ring is connected to V_{DD_IO}. The inserted guard ring can help decouple the VPNP from LNPN, raising the holding voltage up to greater than V_{Dmax} for latchup prevention. With the inserted guard rings, the latchup test results show that the aforementioned latchup-sensitive 0.13 and 0.18 μm processes can pass the requirements of the standard specification. Most foundry design rules only focus on the latchup design guidelines for I/O cells, internal circuits, and between the I/O and internal circuits. The latchup design guidelines between two different power domains ($V_{DD,H}$-to-$V_{DD,L}$ latchup), however, are rarely specified in foundry design rules. Thus, both foundry and IC designers should be aware of the design solution by inserting guard rings between the two different power domains.

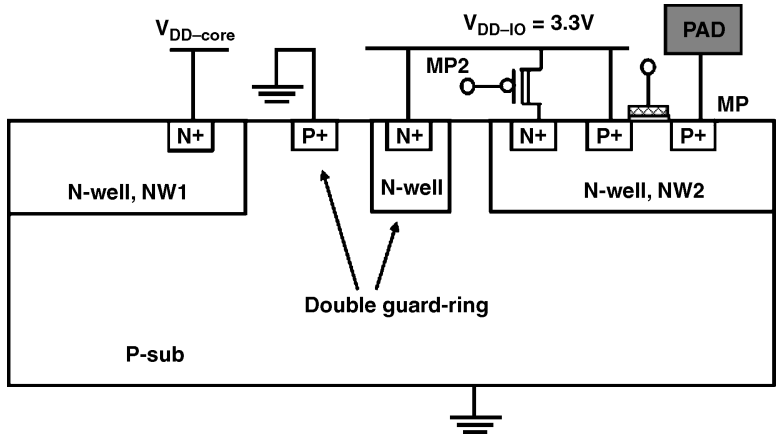

Figure 7.6 Device cross-sectional view of inserting double guard rings to prevent the occurrence of latchup between V_{DD_IO} and V_{DD_core}. (Reprinted with permission from C.-N. Wu, H.-M. Chou, and M.-C. Chang, "Latch-up failure path between power pins in the mixed-voltage process," *Proceedings of the IEEE International Reliability Workshops*, IEEE, Piscataway, NJ. © 2003 IEEE).

7.2 Latchup in Internal Circuits Adjacent to Power-Rail ESD Clamp Circuits

With the highly strong ESD robustness against pin-to-pin and V_{DD}-to-V_{SS} ESD stress, the power-rail ESD clamp circuit is a popular on-chip solution for component-level

ESD protection [9–14]. A generic power-rail ESD clamp circuit is shown in Figure 7.7. With proper design of the RC time constant to be ∼μs, the ESD-clamping NMOS (Mn2) can be turned on to discharge ESD current for ESD protection, and turned off under normal circuit operations without any adverse impact. In general, the power-rail ESD clamp circuit is not a latchup-triggering source because there is no N+/P+ diffusions directly connected to the I/O pads (only V_{DD}/V_{SS} pads). However, if the power-rail ESD clamp circuit is very close to both the I/O pads and internal circuits, it could be a latchup-triggering source to unexpectedly initiate latchup in the nearby internal circuits.

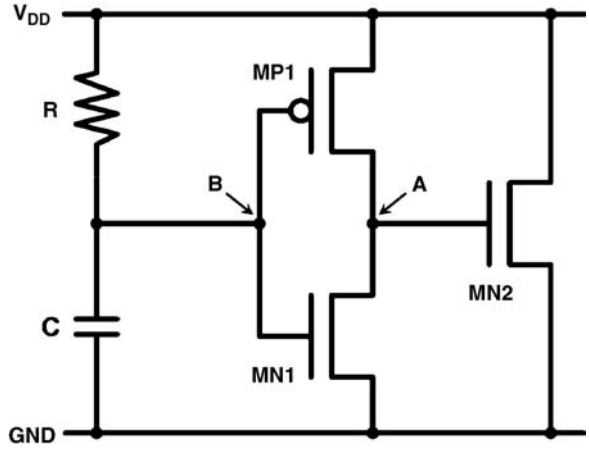

Figure 7.7 Circuit schematic of the generic power-rail ESD clamp circuit. The ESD-clamping NMOS (MN2) can be turned on to discharge the ESD current for ESD protection, and turned off under normal circuit operation without any adverse impact.

7.2.1 Practical Examples

Practical failure returns show the latchup issue in internal circuits adjacent to the power-rail ESD clamp circuit [14]. In this case, the die photograph is shown in Figure 7.8. Under the latchup trigger current test, specifically latchup immunity is degraded when negative current injects into pad numbers 14 and 23, which are located close to the power-rail ESD clamp circuit. The device cross-section of the power-rail ESD clamp circuit is shown in Figure 7.9, and its circuit schematic is shown in Figure 7.7.

During negative current injection, some of the electrons can be collected by V_{DD} through the N-well resistor, thus generating a voltage drop along this N-well resistor. Once the voltage drop is higher than the threshold voltage of MP1, the latter will be turned on and raise the potential at node A. Consequently, the ESD-clamping NMOS (MN2) will be turned on and induce a large substrate current to initiate latchup in the nearby internal circuits. This latchup mechanism is confirmed by directly connecting

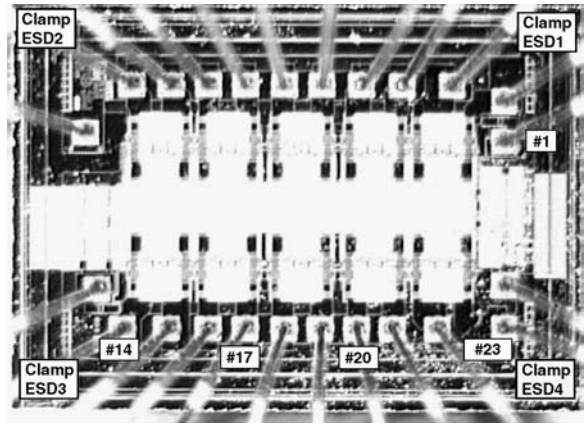

Figure 7.8 Die photograph of the CMOS chip [14]. Latchup issue exists in the internal circuits adjacent to the power-rail ESD clamp circuit. (Reprinted with permission from P. Tong, W. Chen, R. Jiang et al., "Active ESD shunt with transistor feedback to reduce latchup susceptibility or false triggering," *Proceedings of the IEEE International Symposium. on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, IEEE, Piscataway, NJ. © 2004 IEEE).

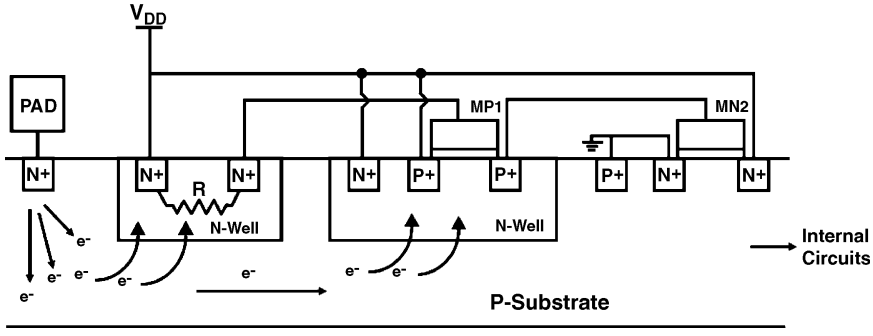

Figure 7.9 Device cross-section of the power-rail ESD clamp circuit. (Reprinted with permission from P. Tong, W. Chen, R. Jiang et al., "Active ESD shunt with transistor feedback to reduce latchup susceptibility or false triggering," *Proceedings of the IEEE International Symposium. on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, IEEE, Piscataway, NJ. © 2004 IEEE).

the node B to V_{DD}. With a V_{DD} potential for node B, node A will be pulled down to the GND and MN2 will be turned off. As a result, latchup disappears under the same negative trigger current levels.

During the positive current injection, however, the injecting carriers are the holes. They could only be collected by the GND, and have no chance to turn on MN2. Even though some injected holes can directly reach the nearby internal circuits through the P-substrate, the amount should be negligible because of recombination and are unable to induce latchup. Thus, latchup immunity remains normal under the positive trigger current test.

7.2.2 Suggested Solutions

To avoid potential latchup risks in internal circuits which are close to the power-rail ESD clamp circuit, a straightforward solution is to take the internal circuits away from the ESD clamp circuit as far as possible. However, it is not an economical solution because of a larger layout area. To achieve good latchup immunity and a compact layout in CMOS ICs, a new power-rail ESD clamp circuit with transistor feedback was proposed [14]. The circuit schematic is shown in Figure 7.10. With a feedback PMOS, MP2, node B remains at a high voltage level of V_{DD} because node A is at the low-state (GND) during normal circuit operation. During the latchup negative trigger current test, node B will not be lowered even though the injected electrons are collected by V_{DD} through the N-well resistor. Thus, MN2 always stays turn-off, and potential latchup danger can be avoided in internal circuits which are very close to this new power-rail ESD clamp circuit with a transistor feedback. For the design of this new ESD clamp circuit, the only concern is the premature turn-off of MN2 during the ESD events, because MP2 always helps MN2 to be turned off via feedback. This design criterion can be well clarified with device simulation by choosing proper R and C values [14].

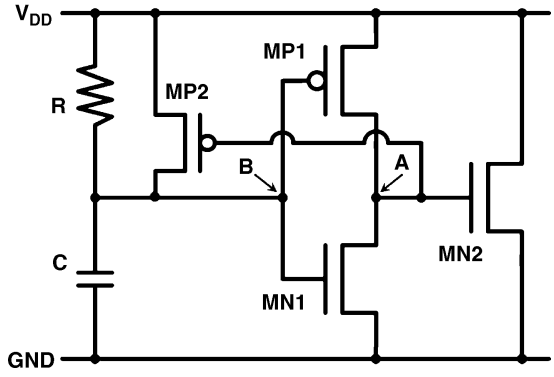

Figure 7.10 Circuit schematic of the power-rail ESD clamp circuit with a transistor feedback [14].

7.3 Unexpected Trigger Point to Initiate Latchup in Internal Circuits

In internal circuits, latchup can be easily triggered on by the trigger current injecting into the I/O pads. To prevent the occurrence of latchup in internal circuits, adding substrate/well pickups, inserting guard rings between the I/O and the internal circuits, and enlarging the spacing between the I/O and the internal circuits are the common solutions. However, even though these latchup design guidelines are certainly implemented, unexpected latchup in internal circuits could still happen when there are diffusion regions, which are directly connected to the I/O pads, in the internal circuits. The device cross-sectional view and layout top view to show such specific

latchup issue in the internal circuits are illustrated in Figure 7.11a and b, respectively. With the directly connected metal line between the I/O pad and the diffusion region in the internal circuits, the diffusion region can be treated as a latchup trigger point. The trigger current injecting into the I/O pads can reach this trigger point, generating the substrate current to initiate latchup in the neighboring internal circuits. As a result,

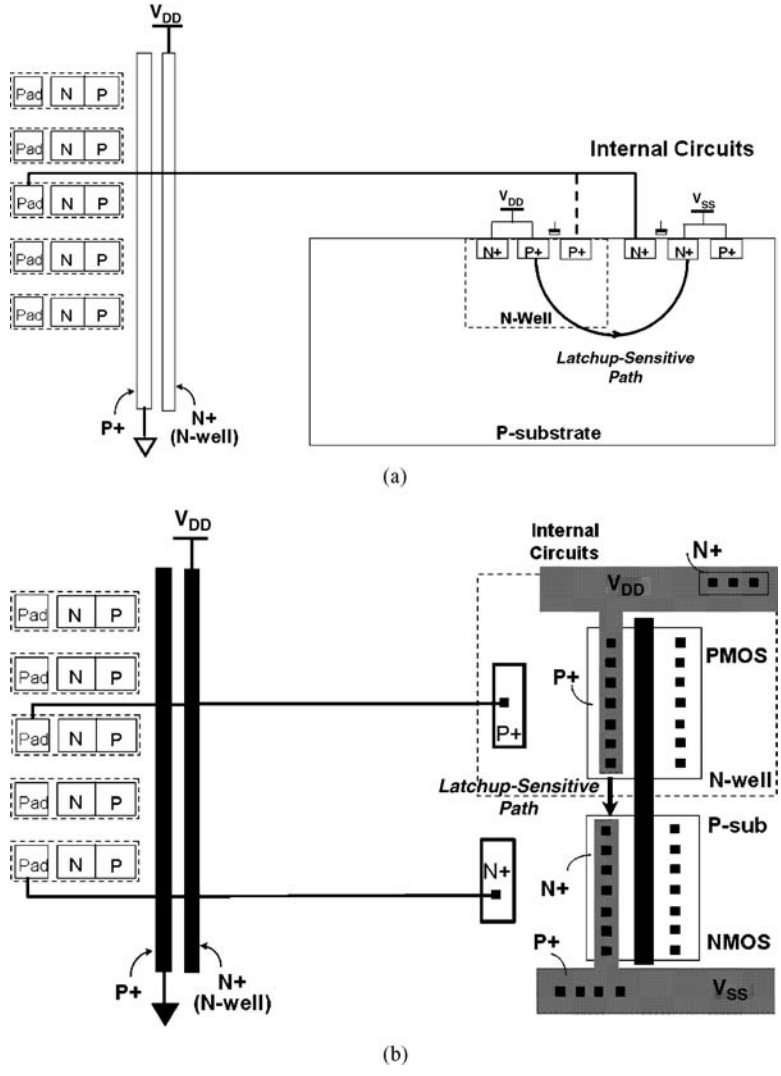

Figure 7.11 (a) Device cross-sectional view, and (b) layout top view, to show latchup occurrence in the internal circuits. With the directly connected metal line between the I/O pad and the diffusion region in the internal circuits, the trigger current injecting into the I/O pads can reach the internal circuits, generating the substrate current to initiate latchup in the internal circuits.

inserting additional guard rings or enlarging the spacing between the I/O and the internal circuits has no effectiveness in improving the latchup immunity in the internal circuits, because the trigger current no longer travels along the substrate, but along the metal instead to the internal circuits. In general, due to the lack of protection of the guard rings as well as the demand for high integration of the circuitry, the internal circuits are always very susceptible to such latchup issues. To ensure reliable CMOS ICs, designers should particularly beware of such latchup issues and their related solutions.

7.3.1 Practical Examples

Practical failure returns [15–16] have proven that the diffusion regions directly connected to the I/O pads can induce latchup in the internal circuits. A CDM [17–18] ESD clamp device is one practical example. A typical schematic diagram of the ESD protection designs for CDM ESD events is shown in Figure 7.12. During the CDM events, the CDM ESD clamp device (gate-grounded NMOS, GGNMOS), which is placed between V_{SS} and the gate of MN/MP, can shunt most CDM ESD current (I_{ESD}) to protect MN from CDM ESD damage. However, the drain diffusion region of the CDM ESD clamp device, which is directly connected to the I/O pad via the metal connection, could be a latchup trigger point to induce latchup occurrence in the internal circuits. Once there is a negative trigger current injecting into the I/O pad, the electron current can reach the N+ drain diffusion of the CDM ESD clamp device via the metal connection. Subsequently, the injecting electron current can flow into the P-substrate (or P-well), inducing latchup in the neighboring internal circuits.

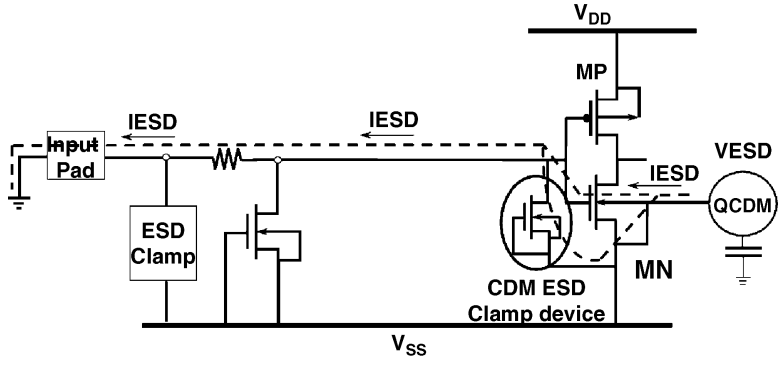

Figure 7.12 Typical schematic diagram of the ESD protection designs for CDM ESD events.

Another failure return [16] also shows that the diffusion regions directly connected to the I/O pads can induce latchup in the internal circuits of a power controller IC. In this IC, all I/O pins have the same I/O cell including an ESD protection devices.

However, the latchup test results reveal that a specific "pin A" is very susceptible to the negative trigger current test in comparison with the other pins. The schematic diagram and the EMMI photograph of the latchup path under the latchup negative trigger current test are shown in Figure 7.13a and b, respectively. The EMMI photograph shows that latchup does not occur in the I/O cell of pin A, but in its adjacent internal circuits. The equivalent circuit and the device cross-sectional view of the internal circuit (PMOS) which is directly connected to such a specific pin A are shown in Figure 7.14a and b, respectively. With the design considerations of reducing the threshold voltage in the PMOS, pin A is directly connected to the N+ well contact and P+ source of the PMOS. However, because of the direct metal

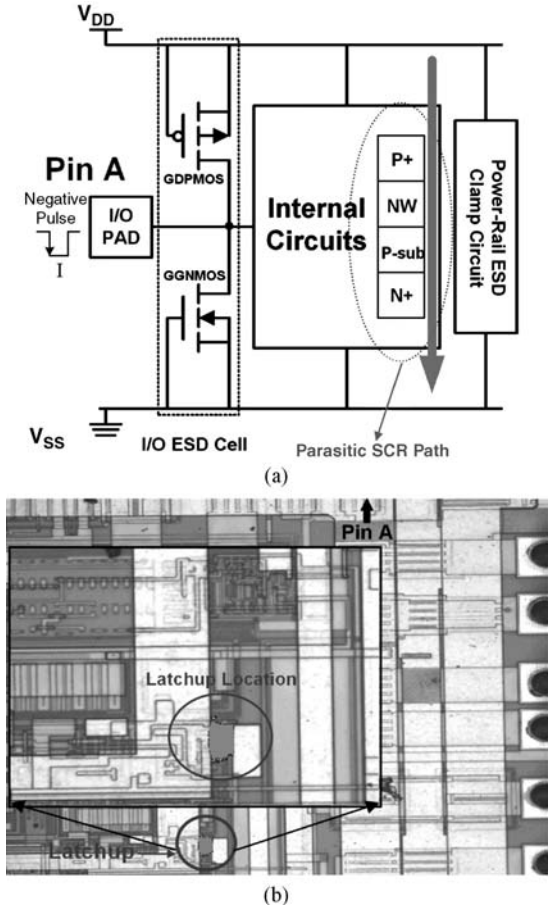

Figure 7.13 (a) Schematic diagram, and (b) EMMI photograph, of the latchup path in the latchup negative trigger current test. (Reprinted with permission from S.-H. Chen and Ming-Dou Ker, "Failure analysis and solutions to overcome latchup failure event of a power controller IC in bulk CMOS technology." *Microelectronics Reliability*, Elsevier, Oxford, UK. © 2006 Elsevier).

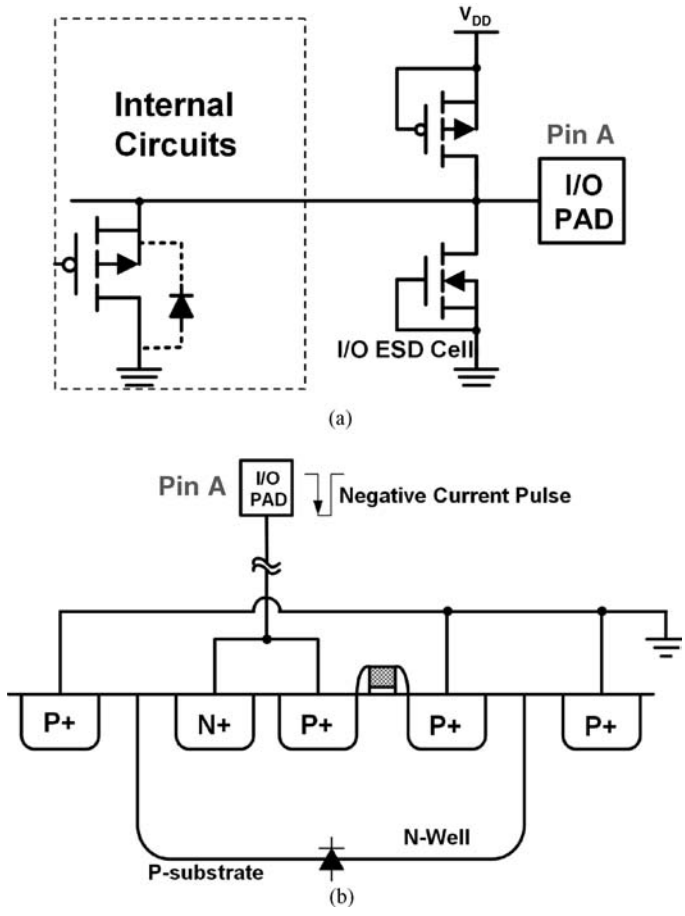

Figure 7.14 (a) Equivalent circuit, and (b) device cross-sectional view, of the internal circuit (PMOS) which is directly connected to pin A. (Reprinted with permission from S.-H. Chen and Ming-Dou Ker, "Failure analysis and solutions to overcome latchup failure event of a power controller IC in bulk CMOS technology." *Microelectronics Reliability*, Elsevier, Oxford, UK. © 2006 Elsevier).

connection between pin A and the N+ well contact, the injecting negative trigger current (from pin A) can flow into the P-substrate via the parasitic N-well/P-substrate diode, initiating latchup in the neighboring internal circuits. The device cross-sectional view to illustrate such a latchup-firing mechanism is shown in Figure 7.15, and the corresponding layout patterns are also shown in Figure 7.16. As a result, the neighboring internal circuits are very sensitive to the negative trigger current (with a latchup immunity level of only −50 mA), even though there are good latchup-preventing layout designs in the I/O cells (with double guard rings) and in between the I/O and internal circuits (with inserted guard rings between them).

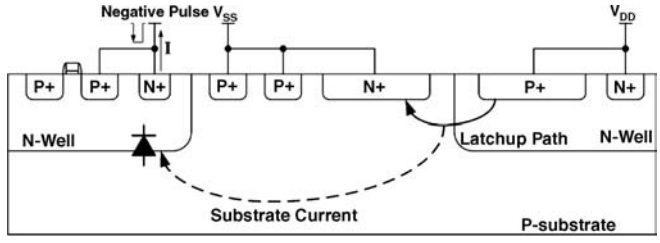

Figure 7.15 Device cross-sectional view to illustrate the latchup path triggered by the substrate current that is induced from the forward N-well/P-substrate diode. (Reprinted with permission from S.-H. Chen and Ming-Dou Ker, "Failure analysis and solutions to overcome latchup failure event of a power controller IC in bulk CMOS technology." *Microelectronics Reliability*, Elsevier, Oxford, UK. © 2006 Elsevier).

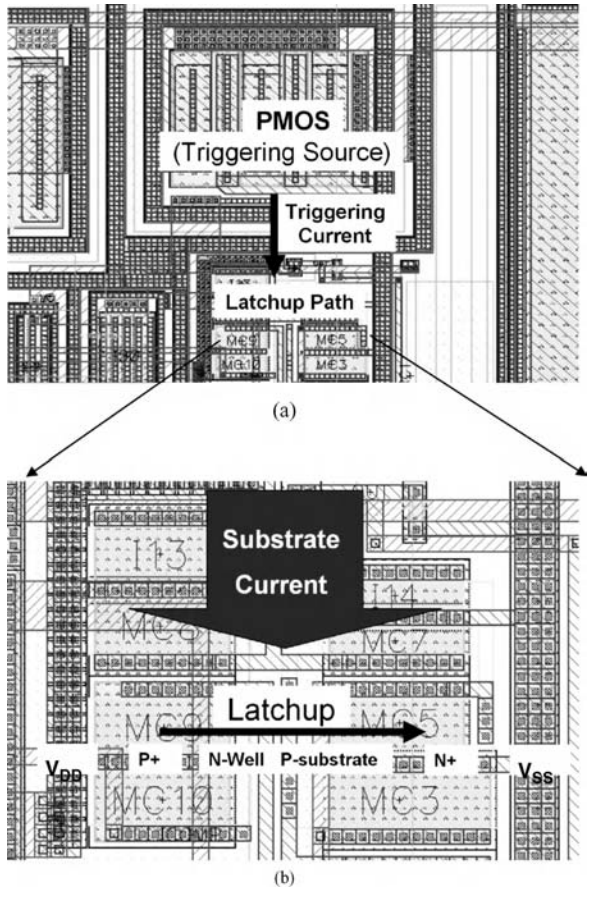

Figure 7.16 (a) Relationship between the PMOS and latchup path in the layout pattern. (b) Zoomed-in layout pattern to show the latchup location at the neighboring circuits. (Reprinted with permission from S.-H. Chen and Ming-Dou Ker, "Failure analysis and solutions to overcome latchup failure event of a power controller IC in bulk CMOS technology." *Microelectronics Reliability*, Elsevier, Oxford, UK. © 2006 Elsevier).

7.3.2 Suggested Solutions

The aforementioned practical failure returns show that any diffusion region, which is directly connected to the I/O pad, in the internal circuits could be the unexpected latchup trigger point to induce latchup in the internal circuits. To certainly prevent such a latchup issue, it is an efficient solution by using the guard rings to surround the diffusion trigger point, or by inserting the guard rings between the diffusion trigger point and its adjacent latchup-sensitive internal circuits. The guard ring can collect the injecting carriers coming from the I/O pad, further preventing these carriers from escaping to induce latchup in the neighboring internal circuits. In addition, a small current-limiting resistor can be also added between the diffusion trigger point and its directly-connected I/O pad [16]. Such a current-limiting resistor can improve the latchup immunity of the internal circuits by reducing the trigger current which flows into the diffusion trigger point. However, it will induce the additional voltage drop across itself, consequently degrading the circuit performance. Therefore, the resistance of the current-limiting resistor should be optimized for efficiently improving the latchup immunity level but without serious degradation on circuit performance.

7.4 Other Unexpected Latchup Paths in CMOS ICs

Another unexpected latchup path can go through from the power pins to the adjacent grounded N+ diffusions or N-well. The typical schematic diagram to show such a latchup issue is illustrated in Figure 7.17. Due to the ESD protection diode (diode_1)

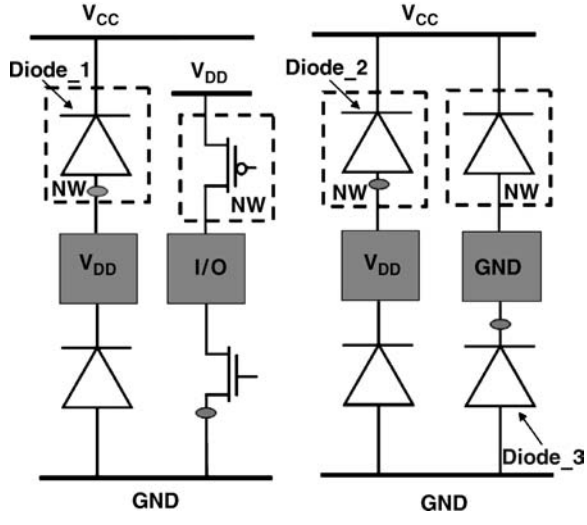

Figure 7.17 Schematic diagram to show the unexpected latchup issue between the power pins and the adjacent grounded N+ diffusions or N-well.

between the terminal rails VDD and VCC ($V_{CC} > V_{DD}$, where V_{CC} and V_{DD} are actual voltage values), the latchup path can go through from the P+ diffusion (anode of diode_1) connected to the V_{DD} pin, the N-well (cathode of diode_1) connected to V_{CC}, and the P-substrate connected to GND, to the grounded N+ source of the NMOS output driver (MN) in the neighboring I/O buffer, as shown in the left-hand figure. Also, the latchup path can go through from the P+ diffusion (anode of diode_2) connected to the V_{DD} pin, the N-well (cathode of diode_2) connected to V_{CC}, and the P-substrate connected to GND, to the N+ diffusion (cathode of diode_3) of the neighboring ESD protection diode connected to the GND pin, as shown in the right-hand figure.

Additionally, unexpected latchup can occur due to the existence of the ESD-connection diodes between the separated power lines. The typical configuration of such ESD-connection diodes between the separated power lines is shown in Figure 7.18. Because of the existence of the ESD-connection diodes, the latchup path can go through from the P+ diffusion (anode of diode_A) connected to V_{DD_1}, the floating N-well (cathode of diode_A), and the P-substrate connected to GND, to the N-well (cathode of diode_B or diode_C) connected to GND_1/GND_2. Also, the latchup path can go through from the P+ diffusion (anode of diode_D) connected to V_{DD_2}, the floating N-well (cathode of diode_D), and the P-substrate connected to GND, to the N-well (cathode of diode_B or diode_C) connected to GND_1/GND_2.

Another unexpected case is the I/O-to-I/O cell interaction-induced latchup [3]. The schematic diagram of such a latchup issue is shown in Figure 7.19. The latchup

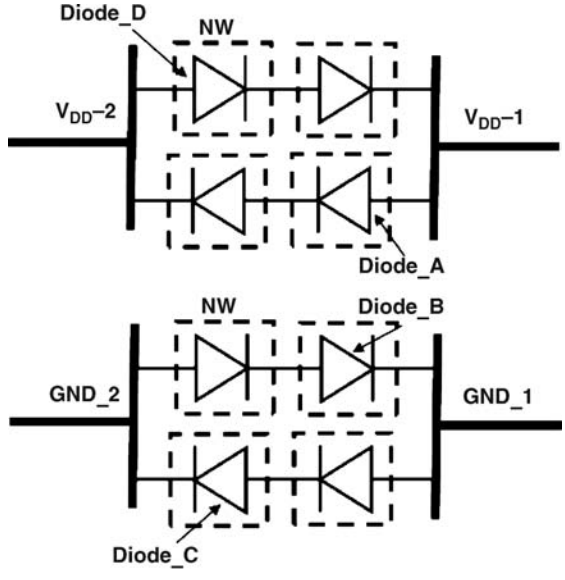

Figure 7.18 Schematic diagram of ESD-connection diodes between the separated power lines.

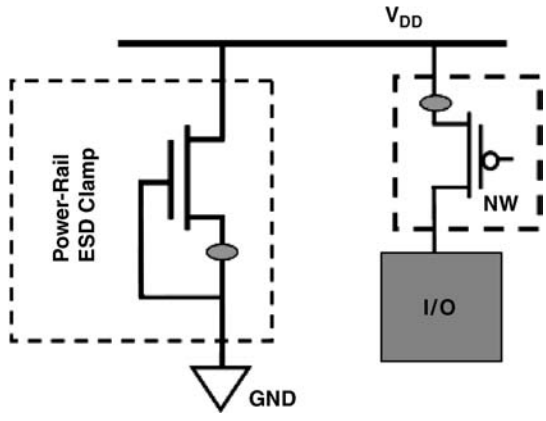

Figure 7.19 Schematic diagram to show the unexpected I/O-to-I/O cell interaction-induced latchup.

path can go through from the P+ source of the PMOS output driver connected to V_{DD}, the N-well connected to V_{DD}, and the P-substrate connected to GND, to the N+ source of the neighboring power-rail ESD clamped cell (GGNMOS). Such an I/O-to-I/O cell interaction-induced latchup is difficult to detect, because the latchup rules in I/O cells are usually checked in unit I/O cells, but not checked in between two adjacent I/O cells.

To prevent the aforementioned unexpected latchup issues, one common solution is to enlarge the anode-to-cathode spacing of these unexpected latchup paths. Together with the insertions of additional guard rings to decouple these latchup paths, safe and compact layout schemes for latchup prevention can be achieved.

7.5 Conclusion

In general, foundry latchup design guidelines do not cover the unexpected latchup paths introduced in this chapter. These latchup paths can exist between two different power domains ($V_{DD,H}$-to-$V_{DD,L}$ latchup), between the power-pins and grounded N+/N-well, and between two adjacent I/O cells. The ESD-coupled diodes between separated power lines can also lead to the unexpected V_{DD}-to-V_{SS} latchup. In addition, unexpected latchup can occur in internal circuits due to the direct connection between the I/O pads and the N+/P+ diffusions in the internal circuits. If the power-rail ESD clamp circuit is very close to the I/O pads, ESD-clamping NMOS could be unexpectedly turned on during the negative trigger current test, probably initiating latchup in the nearby internal circuits.

IC designers usually neglect these unexpected latchup issues, leading to potential latchup risks in most CMOS ICs. Many practical failure returns have proven to show such unexpected latchup paths in CMOS ICs, and related latchup-preventing solutions should be implemented. Enlarging the anode-to-cathode spacing together with the

insertions of additional guard rings in these unexpected latchup-sensitive paths are common solutions to prevent these potential latchup risks. A power-rail ESD clamp circuit with a transistor feedback can be used to efficiently eliminate the potential latchup danger in its nearby internal circuits. By combining these solutions with the general foundry's latchup design guidelines, IC designers can design latchup-robust IC products and decrease the time to market for IC products.

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8

TLU Prevention in Power-Rail ESD Clamp Circuits

Effective power-rail ESD clamp circuits have been playing an important role for whole-chip ESD protection in the state-of-the-art CMOS ICs. These power-rail ESD clamp circuits, however, have been found to be particularly sensitive to TLU in the system-level ESD test. This chapter introduces several TLU issues in power-rail ESD clamp circuits fabricated in both low-voltage (LV) and high-voltage (HV) 40-V CMOS processes. In LV CMOS processes, although the TLU-free ESD-clamp circuit can be easily designed by placing double guard rings to surround each MOS devices, a specific "TLU-like" failure would still occur due to the latch-on state of the ESD-clamping NMOS in the system-level ESD test. In HV CMOS processes, the bottleneck is that the latchup holding voltage is generally much smaller than the HV nominal operating voltage, thus inevitably leading to TLU risks in HV power-rail ESD clamp circuits. In addition to the clarification of TLU-related issues in the power-rail ESD clamp circuits, the investigation and design of TLU-free power-rail ESD clamp circuits are also introduced. These TLU-free power-rail ESD clamp circuits can guarantee robust ESD immunity without suffering TLU or any TLU-like danger in both LV and HV CMOS ICs.

8.1 In LV CMOS ICs[1]

ESD protection has been one of the most important reliability issues in CMOS ICs. ESD failures caused by thermal breakdown due to high current transient, or dielectric breakdown in a gate oxide due to high voltage overstress, often result in immediate malfunction of the IC chips. In order to obtain high ESD robustness, CMOS ICs must

[1] © 2008 IEEE. Reprinted, with permission, from Ming-Dou Ker and C.-C. Yen, Investigation and design of on-chip power-rail ESD clamp circuits without suffering latchup-like failure during system-level ESD test (sections I–V, figures 1, 2, 6–15, 17–19, and tables V, VI. VII, and VIII), in *IEEE Journal of Solid-State Circuits*, Vol. 43, no. 11, pp. 2533–2545, Nov. 2008. IEEE, Piscataway, NJ.

Transient-Induced Latchup in CMOS Integrated Circuits Ming-Dou Ker and Sheng-Fu Hsu
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be designed with on-chip ESD protection circuits at the I/O pins and across the power lines [1]. With the reduced breakdown voltage of the thinner gate oxide in advanced deep-submicron CMOS processes, turn-on-efficient ESD protection circuit is required to clamp the overstress across the gate oxide of the internal circuits. Since the stored electrostatic charges could be either positive or negative, there are four different ESD-testing modes at the input–output I/O pins with respect to the grounded V_{DD} or V_{SS} pins [2]. Moreover, for comprehensive ESD verification, two additional pin combinations in the ESD test, which are the pin-to-pin ESD stress and the V_{DD}-to-V_{SS} ESD stress, are performed to verify the ESD reliability of IC chips [2]. These two additional ESD testing modes often lead to some unexpected ESD current through the I/O pins and power lines into the internal circuits and result in ESD damage in the internal circuits [3]. Therefore, an effective power-rail ESD clamp circuit between the V_{DD} and V_{SS} power lines is necessary for whole-chip ESD protection. The typical on-chip ESD protection design with an active power-rail ESD clamp circuit in CMOS ICs is shown in Figure 8.1 [4]. When the input (or output) pin is discharged under the positive-to-V_{SS} (PS-mode) or negative-to-V_{DD} (ND-mode) ESD stresses, the power-rail ESD clamp circuit can provide a low impedance path between the V_{DD} and V_{SS} power lines to efficiently discharge the ESD current. Thus, to avoid unexpected ESD damage in the internal circuits under pin-to-pin and V_{DD}-to-V_{SS} ESD stresses, the power-rail ESD clamp circuit must be designed with a high turn-on efficiency and a fast turn-on speed.

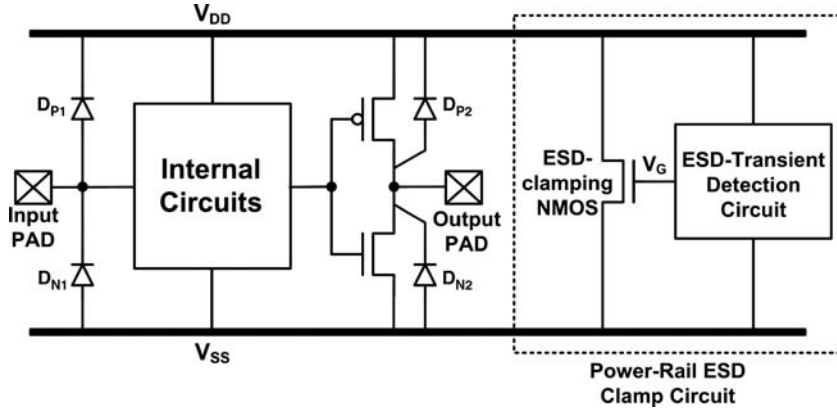


Figure 8.1 Typical on-chip ESD protection design with an active power-rail ESD clamp circuit. (Reprinted with permission from IEEE).

In the active power-rail ESD clamp circuit, the ESD-transient detection circuit is designed to detect the ESD event and sends a control voltage to the gate of the ESD-clamping NMOS. Since the ESD-clamping NMOS is turned on by a positive gate voltage rather than by snapback breakdown, the ESD-clamping NMOS can be turned on quickly to discharge the ESD current before the internal circuits

are damaged. Thus, the effective power-rail ESD clamp circuit is necessary for protecting the internal circuits against ESD damage, and several modified designs of the ESD-transient detection circuits have been reported to enhance the performance of power-rail ESD clamp circuits [5–9].

8.1.1 Power-Rail ESD Clamp Circuits

Four different power-rail ESD clamp circuits are depicted in Figure 8.2a–d [5–9]: (a) a power-rail ESD clamp circuit with typical RC-based detection, (b) a power-rail ESD clamp circuit with PMOS feedback, (c) a power-rail ESD clamp circuit with NMOS + PMOS feedback, and (d) a power-rail ESD clamp circuit with cascaded PMOS feedback.

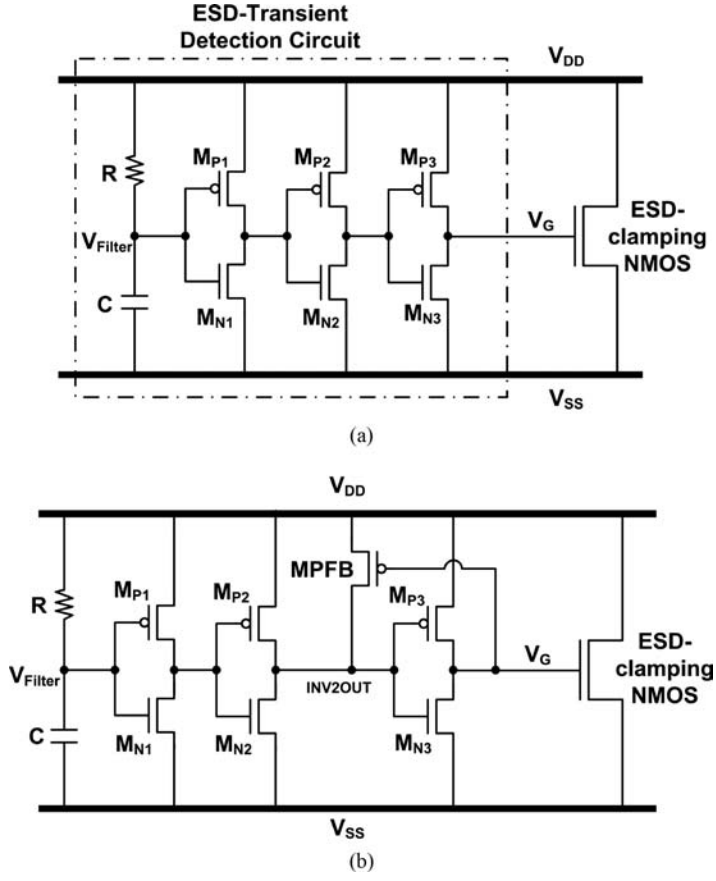
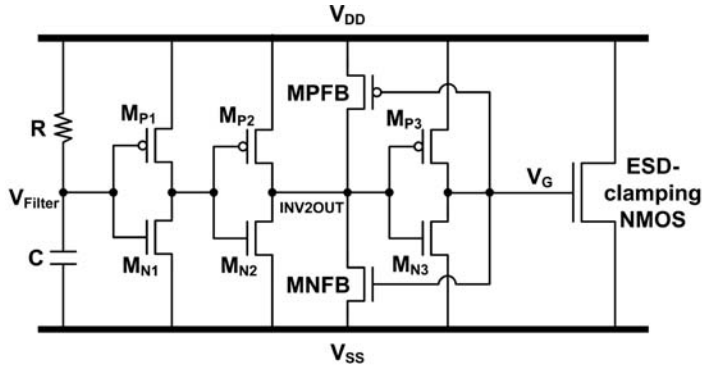
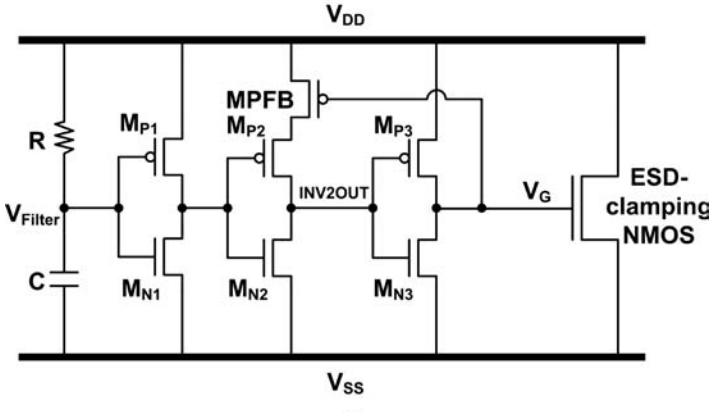


Figure 8.2 Four different power-rail ESD clamp circuits designed with (a) typical RC-based detection, (b) PMOS feedback, (c) NMOS + PMOS feedback, and (d) cascaded PMOS feedback. (Reprinted with permission from IEEE).



(c)



(d)

Figure 8.2 (*Continued*).

8.1.1.1 Power-Rail ESD Clamp Circuit with Typical RC-Based Detection

A typical RC-based power-rail ESD clamp circuit is illustrated in Figure 8.2a with a three-stage buffer between the RC circuit and the ESD-clamping NMOS [5]. The ESD-clamping NMOS provides a low impedance path between V_{DD} and V_{SS} to discharge the ESD current. The ESD-transient detection circuit can detect ESD pulses with a rise time of ~10 ns and send a control voltage to the gate of the ESD-clamping NMOS. Under the ESD stress condition, the voltage level at the V_{Filter} node is increased much slower than that on the V_{DD} power line, because the RC circuit has a time constant of the order of microseconds (μs). Due to the delay of the voltage increase at the V_{Filter} node, the three-stage buffer is powered by the ESD energy and conducts a voltage to the V_G node to turn on the ESD-clamping NMOS. The turned-on ESD-clamping NMOS, which provides a low-impedance path between the V_{DD} and V_{SS} power lines, clamps

the overstress ESD voltage to effectively protect the internal circuits against ESD damage.

The turn-on time of the ESD-clamping NMOS during ESD transition can be adjusted by designing the RC time constant in the ESD transient detection circuit. The turn-on time is usually designed to be around ~100 ns to meet the half-energy discharging time of the HBM ESD current. Under normal circuit operating conditions, the power-rail ESD clamp circuit must be kept off to avoid power loss from V_{DD} to V_{SS}. The rise time of V_{DD} powered up is around ~1 ms or even longer in most microelectronics systems. To meet such a timing requirement, the RC time constant in the RC-based ESD-transient detection circuit is typically designed with $0.1 \sim 1\,\mu s$ to achieve the design constrains.

8.1.1.2 Power-Rail ESD Clamp Circuit with PMOS Feedback

Another design consideration for the power-rail ESD clamp circuit is the circuit immunity to false triggering during the power-up condition. The power-rail ESD clamp circuit should be turned on when the ESD voltage appears across the V_{DD} and V_{SS} power lines, but is kept off when the IC operates under the normal power-on condition. To meet these requirements, the RC time constant has been usually designed with $0.1 \sim 1\,\mu s$ to achieve the design constraints. However, the large RC time constant used in the power-rail ESD clamp circuit may cause false triggering during a fast power-up condition with a rise time of less than 10 µs. The modified power-rail ESD clamp circuit incorporated with a PMOS feedback, as shown in Figure 8.2b, was used to mitigate such a mis-trigger problem [6]. The transistor MPFB can help to keep the gate voltage of the ESD-clamping NMOS below its threshold voltage and further reduce the current drawn during the power-up condition.

8.1.1.3 Power-Rail ESD Clamp Circuit with NMOS + PMOS Feedback

In advanced CMOS technology with a thinner gate oxide, the power-rail ESD clamp circuit with a large MOS capacitance in the RC timer was reported to cause significant stand-by power consumption due to gate oxide leakage current [7]. Thus, modified power-rail ESD clamp circuits with a small MOS capacitance are desired for combating the gate leakage. It was reported that a power-rail ESD clamp circuit incorporated with a regenerative feedback network can be used to significantly reduce the RC time constant, as illustrated in Figure 8.2c [8].

The transistors MPFB and MNFB provide a feedback loop, which can latch the ESD-clamping NMOS in the conductive state during the ESD-stress condition. When a fast positive-going ESD transient appears across the power rails, the MNFB can further pull the potential of the INV2OUT node towards ground to latch the ESD-clamping NMOS in the conductive state until the voltage on V_{DD} drops below the threshold voltage of the ESD-clamping NMOS. With this feedback loop in the

power-rail ESD clamp circuit, the dynamic currents of M_{P2}, M_{N2}, MPFB, and MNFB determine the critical voltage to trigger on the ESD-clamping NMOS. After the timing out of the RC time constant in the ESD transient detection circuit, the transistor M_{P2} begins to conduct and increase the potential of the INVOUT2 node. The settling potential of the INVOUT2 node is set by the current balance between M_{P2} and MNFB. Thus, the device ratios of M_{P2} and MNFB in the power-rail ESD clamp circuit with a NMOS + PMOS feedback should be appropriately selected.

8.1.1.4 Power-Rail ESD Clamp Circuit with Cascaded PMOS Feedback

Another RC-based power-rail ESD clamp circuit with cascaded PMOS feedback has been proposed to reduce the RC time constant and to solve the false trigger issue during fast power-up constrains, as shown in Figure 8.2d [9]. The PMOS transistor MPFB is connected to form the cascaded feedback loop, which is a dynamic feedback design.

During the ESD-stress condition, the transistor MPFB was turned off and the voltage on the INV2OUT node can remain in a low state. Thus, the turn-on time of the ESD-clamping NMOS can be longer than that of the typical RC-based power-rail ESD clamp circuit. If the ESD-clamping NMOS is mis-triggered during the fast power-up condition or by an overvoltage under normal operating conditions, the voltage on the INV2OUT node can be charged up toward V_{DD} by the subthreshold current of MPFB. Therefore, the ESD-clamping NMOS will not stay in the latch-on state and turn itself off after the fast power-up condition. Compared with the feedback designs with a direct PMOS feedback in Figure 8.2b, the power-rail ESD clamp circuit with a cascaded PMOS feedback has the advantage of capacitance reduction.

8.1.2 TLU-Like Issues in LV Power-Rail ESD Clamp Circuits

IC malfunction or wrong triggering behavior due to a TLU-like issue can be investigated among the aforementioned four different power-rail ESD clamp circuits [10]. The so-called "TLU-like" issue means that the ESD-transient detection circuits would continually keep the ESD-clamping NMOS in a latch-on state when suffering ESD stresses. Thus, the latch-on ESD-clamping NMOS between the V_{DD} and V_{SS} power lines in the powered-up microelectronic system causes a serious latchup-like failure in CMOS ICs. Both the component-level TLU measurement [11] and the system-level ESD test [12] are used to evaluate the IC susceptibility to TLU-like issues. All of the DUTs are realized in a 0.18-μm CMOS process.

8.1.2.1 Component-Level TLU Test

With the TLU measurement setup shown in Figure 2.7, the V_{DD} and I_{DD} transient responses can be recorded by the oscilloscope, which can clearly indicate whether TLU occurs (I_{DD} significantly increases) or not. The power-rail ESD clamp circuits shown in

Figure 8.2a–d are the DUTs. The V_{DD} supply voltage is 1.8 V and the noise trigger source is directly connected to the DUTs through the relay in the measurement setup.

Figure 8.3a and b show the measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with NMOS + PMOS feedback under stresses with V_{Charge} of −4 V and + 12 V, respectively. After the TLU test with an initial V_{Charge} of −4 V, the latchup-like failure occurs in this power-rail ESD clamp circuit, because I_{DD} significantly increases and V_{DD} is pulled down, as shown in Figure 8.3a. Similarly, after the TLU test with an initial V_{Charge} of + 12 V, latchup-like failure is also observed

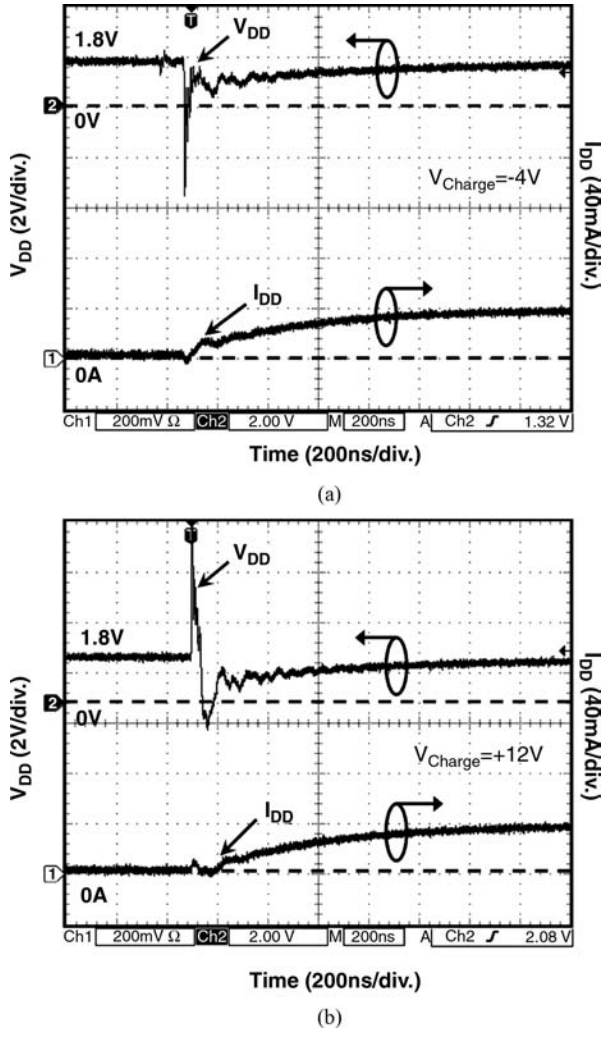


Figure 8.3 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS + PMOS feedback in the TLU test with V_{Charge} of (a) −4 V and (b) + 12 V. (Reprinted with permission from IEEE).

and shown in Figure 8.3b. All the PMOS and NMOS devices in the ESD-transient detection circuits are surrounded with double guard rings to guarantee no latchup issue in this part [13]. This implies that the feedback loop in the ESD-transient detection circuit is locked after the TLU test and continually keeps the ESD-clamping NMOS in a latch-on state. From the observed voltage and current waveforms, a large I_{DD} current is caused by the latch-on state of the ESD-clamping NMOS after the TLU test.

For the power-rail ESD clamp circuit with a cascaded PMOS feedback, the measured V_{DD} and I_{DD} transient responses are shown in Figure 8.4a and b in

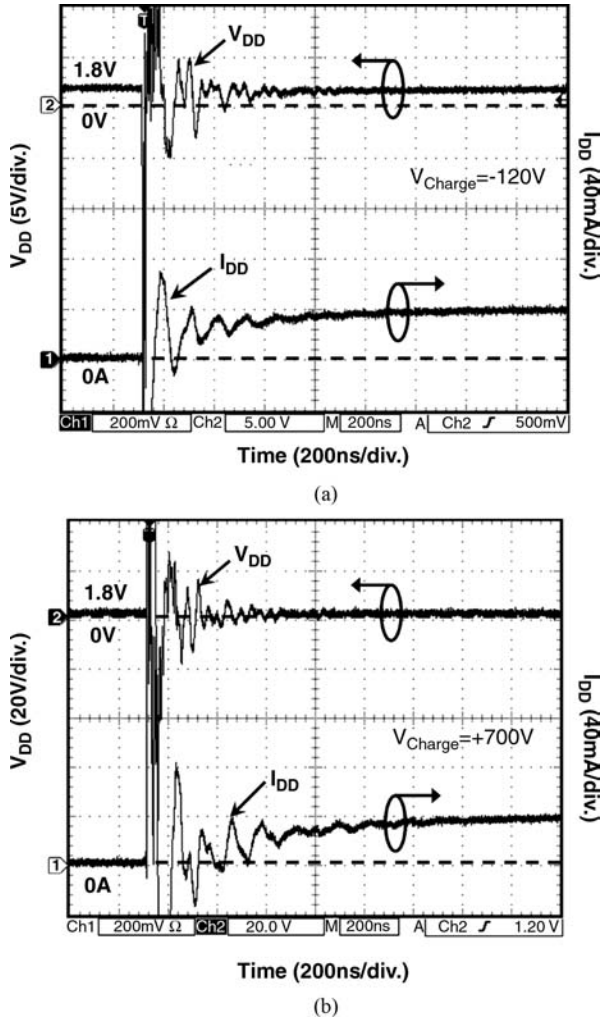


Figure 8.4 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback in the TLU test with V_{Charge} of (a) -120 V and (b) $+700$ V. (Reprinted with permission from IEEE).

the TLU test with an initial V_{Charge} of -120 V and $+700$ V, respectively. The similar latchup-like failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of the ESD-clamping NMOS after the TLU test. The TLU levels (the minimum voltage of V_{Charge} to induce the TLU-like failure on V_{DD}) among the aforementioned four different power-rail ESD clamp circuits are listed in Table 8.1.

Table 8.1 Comparison of theTLU levels among four different power-rail ESD clamp circuits in the TLU test. (Reprinted with permission from IEEE).

Power-rail ESD clamp circuits	Positive TLU level	Negative TLU level
Typical RC-based detection	$> +1$ kV	> -1 kV
With PMOS feedback	$> +1$ kV	> -1 kV
With NMOS + PMOS feedback	$+12$ V	-4 V
With a cascaded PMOS feedback	$+700$ V	-120 V

8.1.2.2 System-Level ESD Test

With the system-level ESD measurement setup shown in Figure 8.5, the susceptibility of different power-rail ESD clamp circuits to the system-level ESD stresses can be evaluated. The stand alone power-rail ESD clamp circuit in the IC package is the DUT and is powered up with a DC power supply of 1.8 V. Before any ESD discharging, the initial V_{DD} voltage level on the IC is measured to make sure of the correct bias of 1.8 V. After every ESD discharging, the voltage level on the V_{DD} node of the IC is measured

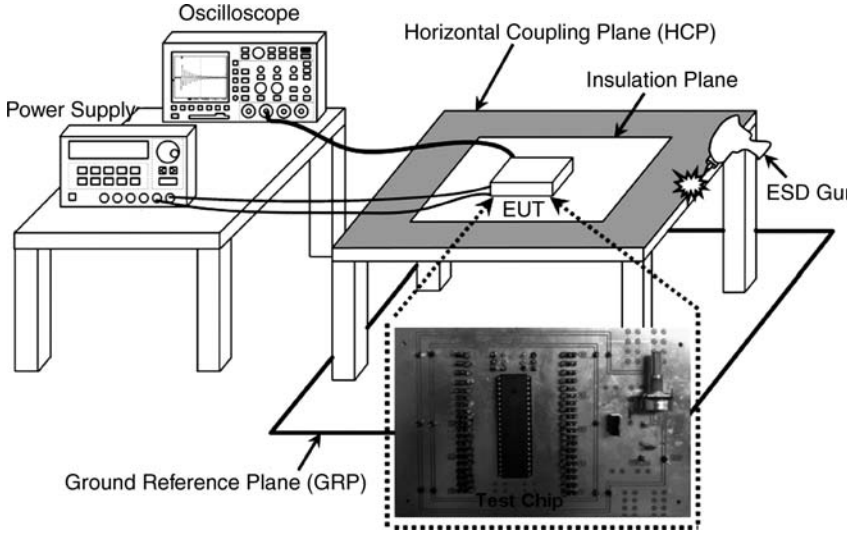


Figure 8.5 Measurement setup for the system-level ESD test in the indirect contact-discharge test mode to evaluate the susceptibility of power-rail ESD clamp circuits. (Reprinted with permission from IEEE).

again to observe whether TLU-like failure occurs after the system-level ESD test, or not. If TLU-like failure occurs, the potential on the V_{DD} node will be pulled down to a much lower level due to the latch-on state of the ESD-clamping NMOS in the power-rail ESD clamp circuits, and I_{DD} will be significantly increased.

Figure 8.6a and b show the measured V_{DD} and I_{DD} transient responses on the power-rail ESD clamp circuit with typical RC-based detection when the ESD gun with an ESD voltage of $-10\,\text{kV}$ and $+10\,\text{kV}$ discharges on the HCP, respectively. After the

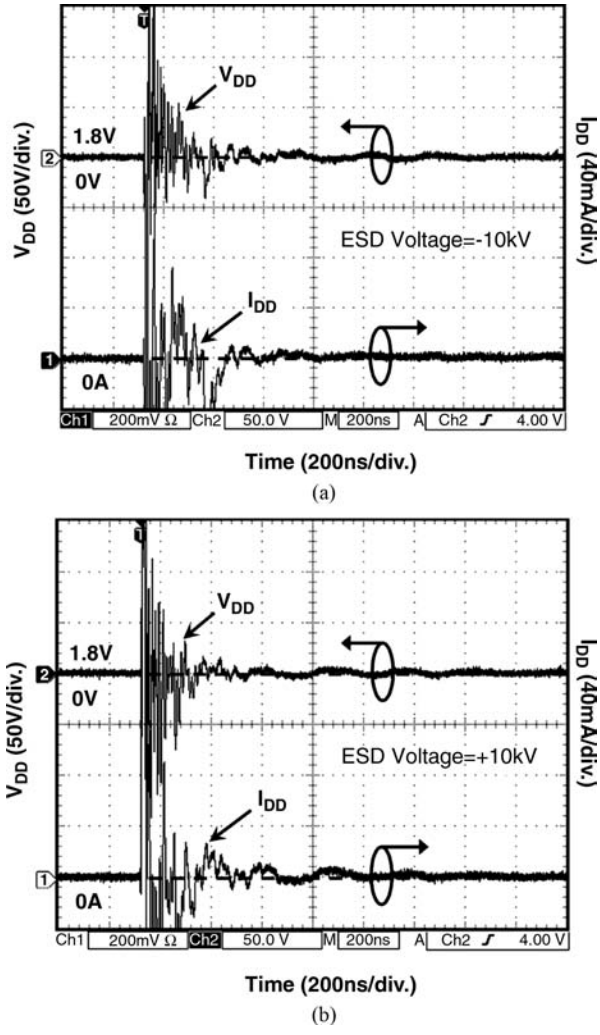


Figure 8.6 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with a typical RC-based detection in the system-level ESD test with an ESD voltage of (a) $-10\,\text{kV}$ and (b) $+10\,\text{kV}$. (Reprinted with permission from IEEE).

system-level ESD test with an ESD voltage of −10 kV, TLU-like failure is not initiated in this power-rail ESD clamp circuit, because I_{DD} is still kept at zero, as shown in Figure 8.6a. Similarly, with an ESD voltage of +10 kV, TLU-like failure is not observed in Figure 8.6b. In the system-level ESD test with an ESD voltage of −10 kV and +10 kV, the measured V_{DD} and I_{DD} transient waveforms on the power-rail ESD clamp circuit with PMOS feedback are shown in Figure 8.7a and b, respectively. In the system-level ESD test with an ESD voltage of −10 kV (+10 kV), TLU-like failure

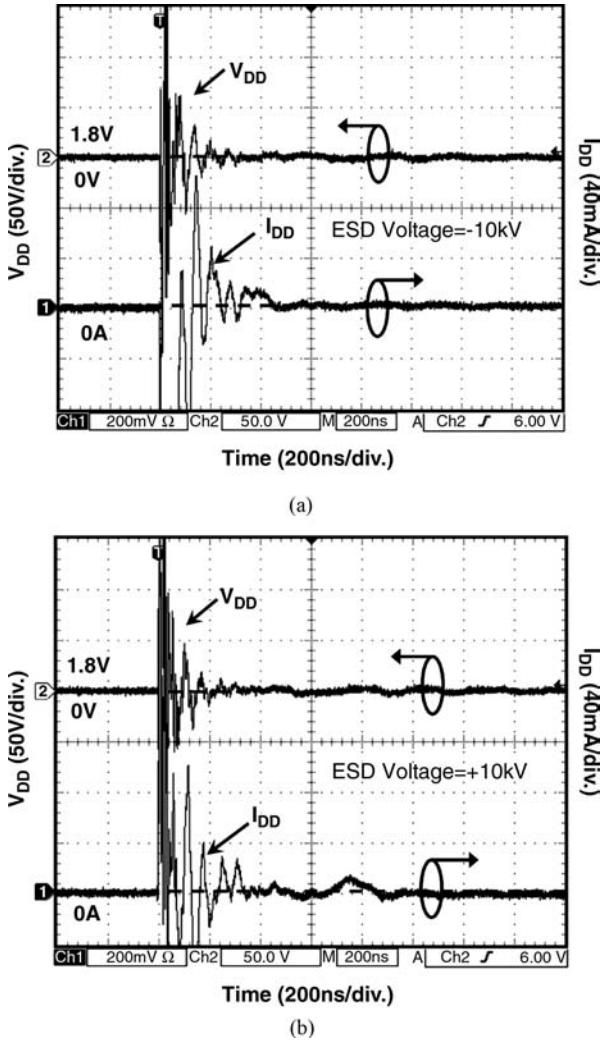
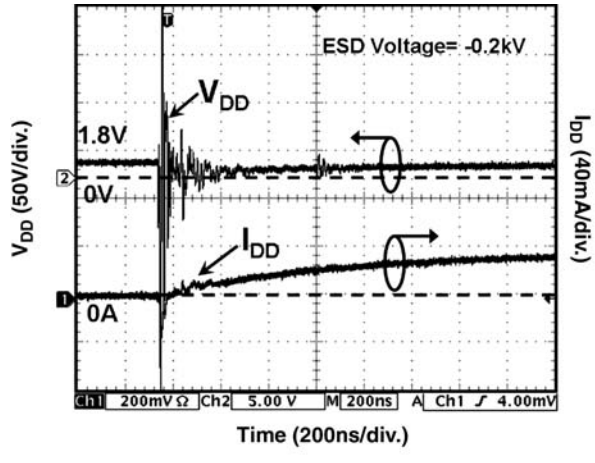


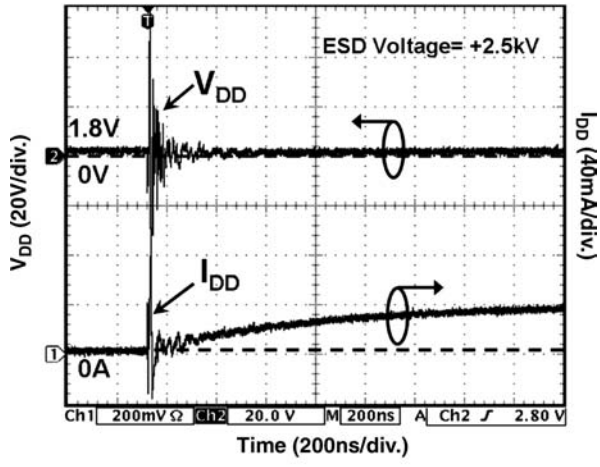
Figure 8.7 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with PMOS feedback in the system-level ESD test with an ESD voltage of (a) −10 kV and (b) +10 kV. (Reprinted with permission from IEEE).

does not occur because I_{DD} is not increased, as shown in Figure 8.7a and b. For the power-rail ESD clamp circuits with typical RC-based detection or PMOS feedback, TLU-like failure does not occur even though the ESD voltage is as high as -10 kV or $+10$ kV in the system-level ESD test.

Figure 8.8a and b show the measured V_{DD} and I_{DD} transient responses on the power-rail ESD clamp circuit with NMOS + PMOS feedback in the system-level ESD test with ESD voltages of -0.2 kV and $+2.5$ kV, respectively. After the system-level ESD test with an ESD voltage of -0.2 kV, TLU-like failure can be initiated in this power-



(a)



(b)

Figure 8.8 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS + PMOS feedback in the system-level ESD test with an ESD voltage of (a) -0.2 kV and (b) $+2.5$ kV. (Reprinted with permission from IEEE).

rail ESD clamp circuit, because I_{DD} is significantly increased and V_{DD} is pulled down as shown in Figure 8.8a. After the system-level ESD test with an ESD voltage of $+2.5$ kV, TLU-like failure can be also found in Figure 8.8b. For the power-rail ESD clamp circuit with cascaded PMOS feedback, the measured V_{DD} and I_{DD} transient responses are shown in Figure 8.9a and b in the system-level ESD test with ESD voltages of -1 kV and $+10$ kV, respectively. A similar TLU-like failure also occurs in this power-rail ESD clamp circuit due to the latch-on state of the ESD-clamping

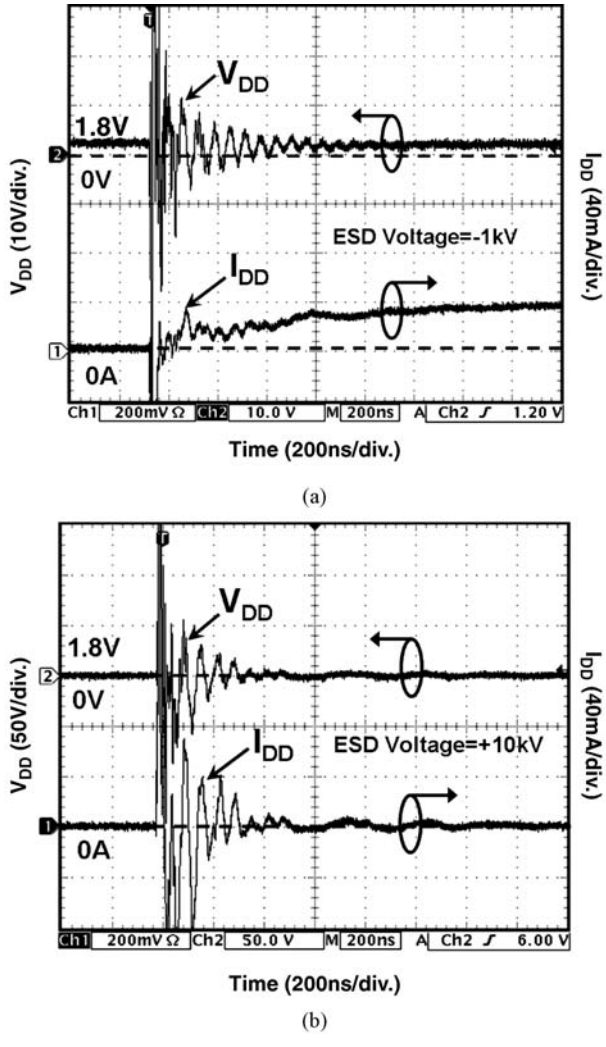


Figure 8.9 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with cascaded PMOS feedback in the system-level ESD test with an ESD voltage of (a) -1 kV and (b) $+10$ kV. (Reprinted with permission from IEEE).

NMOS in the system-level ESD test with an ESD voltage of -1 kV, as shown in Figure 8.9a.

The susceptibility among the aforementioned four different power-rail ESD clamp circuits to the system-level ESD tests are listed in Table 8.2. The power-rail ESD clamp circuits with NMOS + PMOS feedback or with cascaded PMOS feedback have a lower ESD voltage level to cause TLU-like failure in the system-level ESD test. Such measured results are consistent with those of the TLU measurements shown in Table 8.1. Thus, the power-rail ESD clamp circuit designed with NMOS + PMOS feedback is highly sensitive to TLU-like failure. However, the typical power-rail ESD clamp circuits with RC-based detection and with PMOS feedback are free to such a TLU-like failure.

Table 8.2 Comparison of the susceptibility among four different power-rail ESD clamp circuits in the system-level ESD test. (Reprinted with permission from IEEE).

Power-rail ESD clamp circuits	Positive ESD stress	Negative ESD stress
Typical RC-based detection	$> +10$ kV	> -10 kV
With PMOS feedback	$> +10$ kV	> -10 kV
With NMOS + PMOS feedback	$+2.5$ kV	-0.2 kV
With a cascaded PMOS feedback	$> +10$ kV	-1 kV

The failure location after the system-level ESD test has been inspected, as shown in Figure 8.10. Obviously, the failure location is located at the V_{DD} metal line from the V_{DD} pad to the power-rail ESD clamp circuit, which was drawn with a metal width of

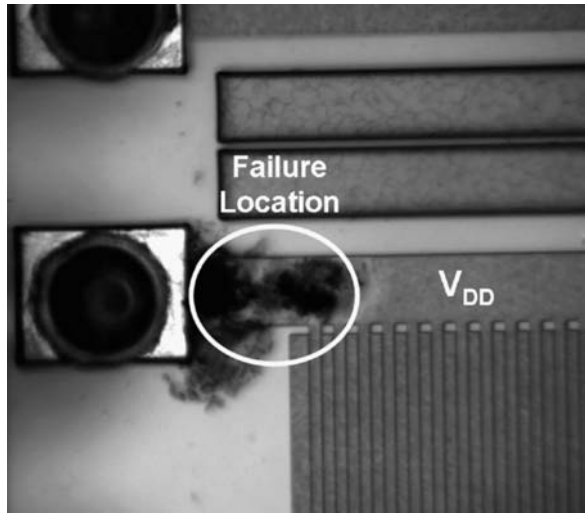


Figure 8.10 Failure location of the power-rail ESD clamp circuit after system-level ESD stress. (Reprinted with permission from IEEE).

30 μm. It can be proved again that TLU-like failure is caused by the latch-on state of the ESD-clamping NMOS in the system-level ESD test.

8.1.3 Design of TLU-Free Power-Rail ESD Clamp Circuits

From the above examples, some ESD-transient detection circuits designed with a feedback loop in the power-rail ESD clamp circuits would malfunction due to a latch-on ESD-clamping NMOS after the system-level ESD test. The latch-on ESD-clamping NMOS between the V_{DD} and V_{SS} power lines in the powered-up microelectronic system causes a serious latchup-like failure in CMOS ICs. In order to meet the electromagnetic compatibility regulation in the system-level ESD test, modified power-rail ESD clamp circuits without suffering TLU-like failure are highly desirable. In order to avoid such a TLU-like failure, it could be useful to reduce the latch strength of the feedback loop in the ESD-transient detection circuit by suitable device dimension sizing. Additionally, another power-rail ESD clamp circuit is introduced to provide a high enough chip-level ESD robustness without suffering TLU-like failure during the system-level ESD test.

Figure 8.11 shows the power-rail ESD clamp circuit with a NMOS reset function to overcome TLU-like failure, which is realized with NMOS + PMOS feedback and an additional NMOS device (M_{NR1}) to provide the reset function after system-level ESD stresses. After the system-level ESD tests, the potential on the V_{Filter} node is charged toward the voltage potential on V_{DD}. When the potential at the V_{Filter} node is greater than the threshold voltage of M_{NR1}, M_{NR1} can be turned on to pull down V_G. If TLU-like failure occurs, that is, the ESD-clamping NMOS is latched-on, the NMOS device (M_{NR1}) will be turned on after the time out of the RC time constant. Thus, the gate

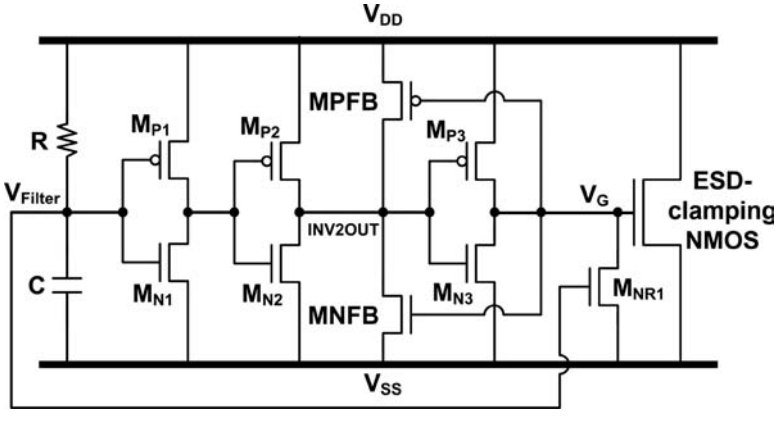


Figure 8.11 The power-rail ESD clamp circuit with an NMOS reset function to overcome TLU-like failure. (Reprinted with permission from IEEE).

potential of the ESD-clamping NMOS will be pulled down toward 0 V to turn off the ESD-clamping NMOS and release the "latch-on" state.

Figure 8.12 shows the simulated transient responses on V_G voltages of the power-rail ESD clamp circuit with NMOS + PMOS feedback. The voltage on V_{DD} is 1.8 V and the initial voltage on V_G is set to 1.8 V to simulate the "latch-on" state of the ESD-clamping NMOS after system-level ESD tests. With an initial voltage of 1.8 V, the V_G voltage of the power-rail ESD clamp circuit without the NMOS reset function continues to keep at 1.8 V. However, with the help of the NMOS reset function, the V_G voltage of the power-rail ESD clamp circuit can be pulled down to 0 V to release the "latch-on" state of the ESD-clamping NMOS.

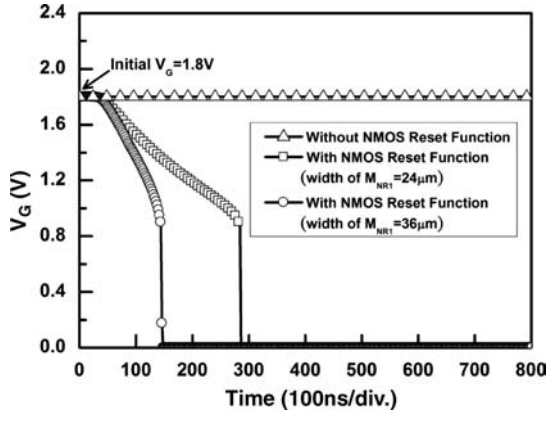


Figure 8.12 Simulated V_G voltage waveforms of the power-rail ESD clamp circuit with an NMOS reset function. V_G can be pulled down to 0 V to release the TLU-like latch-on state of the ESD-clamping NMOS. (Reprinted with permission from IEEE).

In addition to the circuit simulation, experimental verification can also prove the existence of the desired circuit functions of the power-rail ESD clamp circuit with the NMOS reset function. Through the turn-on verification, the component-level TLU test, and the system-level ESD test, the power-rail ESD clamp circuit with the NMOS reset function can be verified as an efficient solution to prevent possible TLU-like danger in the system-level ESD test.

8.1.3.1 Turn-On Verification

To verify the ESD-transient detection function of the power-rail ESD clamp circuit with the NMOS reset function, a voltage pulse generated from a pulse generator is used to simulate the rising edge of the HBM ESD pulse, which has a square-type voltage waveform with a rise time of about 10 ns. When the voltage pulse is applied to the V_{DD}

power line with V_{SS} grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD-clamping NMOS to provide a low-impedance path between the V_{DD} and V_{SS} power lines. Due to the limited driving current of the pulse generator, the voltage on the V_{DD} power line will be degraded by the turned-on ESD-clamping NMOS. The voltage waveform on the V_{DD} power line of the power-rail ESD clamp circuit with the NMOS reset function is shown in Figure 8.13a, where a voltage pulse

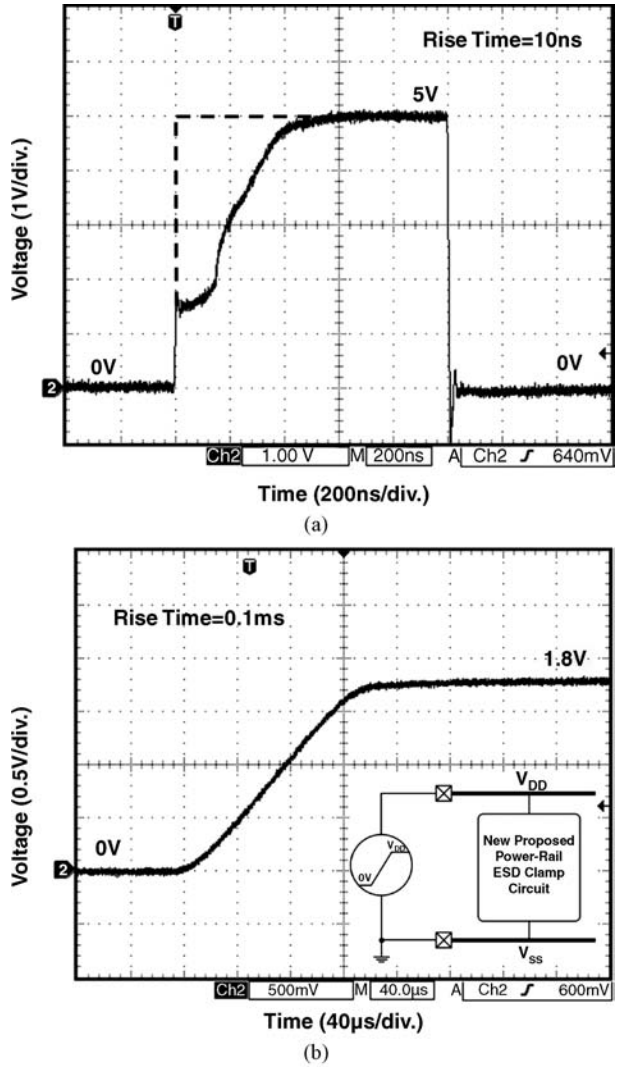


Figure 8.13 Measured voltage waveforms on the power-rail ESD clamp circuit with an NMOS reset function in (a) the ESD-stress condition and (b) the power-on condition. (Reprinted with permission from IEEE).

with a pulse height of 5 V and a pulse width of 1000 ns is applied to the V_{DD} power line. The voltage waveform is degraded at the rising edge because the ESD-clamping NMOS is simultaneously turned-on when the ESD-like voltage pulse is applied to the V_{DD} power line. The voltage degradation is dependent on the turned-on resistance of the ESD-clamping NMOS and the output resistance (typically, 50 ohm) of the pulse generator. A larger device dimension of the ESD-clamping NMOS leads to a more serious degradation on the voltage waveform. When the V_{Filter} node is charged up to the threshold voltage of inverter1 (formed by M_{P1} and M_{N1} in Figure 8.11), the ESD-clamping NMOS will be turned off and the voltage waveform will be restored to the original voltage level. In Figure 8.13a, the applied 5-V voltage pulse has a recovery time of about 400 ns, which corresponds to the turn-on time of the ESD-clamping NMOS.

To verify the action of the power-rail ESD clamp circuit with the NMOS reset function under normal power-on conditions, an experimental setup is shown in the inset figure of Figure 8.13b. A ramp voltage with a rise time of 0.1 ms and a magnitude of 1.8 V is applied to the V_{DD} power line with the V_{SS} power line grounded to simulate the power-on condition. The measured voltage waveform on the V_{DD} power line is shown in Figure 8.13b, where the voltage waveform still remains as a ramp voltage without degradation. Thus, the ESD-clamping NMOS in the power-rail ESD clamp circuit with the NMOS reset function is verified to remain off while the IC is in the power-on condition.

8.1.3.2 TLU Immunity

With the TLU measurement setup shown in Figure 2.7, the measured V_{DD} and I_{DD} responses on the power-rail ESD clamp circuit with V_{Charge} of -1 kV and $+1$ kV are shown in Figure 8.14a and b, respectively. With a negative (positive) V_{Charge} of -1 kV ($+1$ kV), TLU-like failure does not occur in Figure 8.14a and b because I_{DD} is not significantly increased and V_{DD} is not pulled down. The TLU levels of the power-rail ESD clamp circuit with the NMOS reset function and the original power-rail ESD clamp circuit with NMOS + PMOS feedback are listed in Table 8.3. TLU-like failure does not occur in the power-rail ESD clamp circuit with a NMOS reset function after TLU tests with an ESD voltage of up to -1 kV and $+1$ kV.

8.1.3.3 System-Level ESD Susceptibility

The measured V_{DD} and I_{DD} responses on the power-rail ESD clamp circuit with a NMOS reset function in the system-level ESD tests with ESD voltages of -10 kV and $+10$ kV are shown in Figures 8.15a and b, respectively. With a negative (positive) ESD voltage of -10 kV ($+10$ kV), TLU-like failure does not occur in Figure 8.15a and b because the I_{DD} is not significantly increased and V_{DD} is not pulled down.

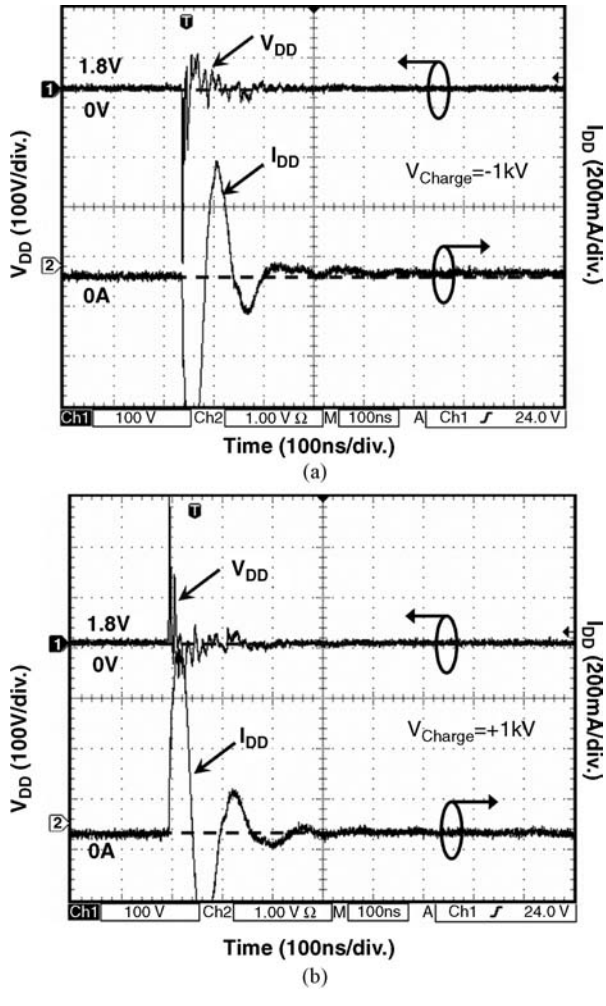


Figure 8.14 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with an NMOS reset function in the TLU test with V_{Charge} of (a) -1 kV and (b) $+1$ kV. No TLU-like failure occurs in the TLU test. (Reprinted with permission from IEEE).

Table 8.3 Comparison of the TLU levels between the power-rail ESD clamp circuit with a NMOS reset function and the original power-rail ESD clamp circuit with NMOS + PMOS feedback. (Reprinted with permission from IEEE).

Power-rail ESD clamp circuits	Positive TLU level	Negative TLU level
With NMOS + PMOS feedback and NMOS reset function	$> +1$ kV	> -1 kV
With NMOS + PMOS feedback (original)	$+12$ V	-4 V

The susceptibility of the power-rail ESD clamp circuit with a NMOS reset function and the original power-rail ESD clamp circuit with NMOS + PMOS feedback against the system-level ESD test are compared in Table 8.4. In the same way as the TLU test, the power-rail ESD clamp circuit with a NMOS reset function is found to be immune to TLU-like danger in the system-level ESD test, even though the ESD stress is as high as −10 kV and +10 kV.

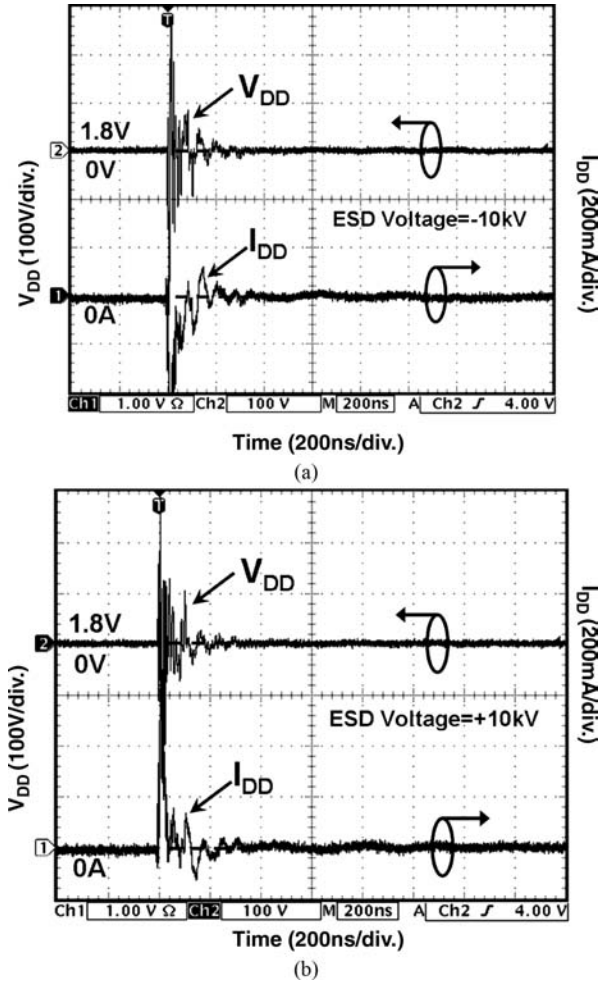


Figure 8.15 Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with an NMOS reset function in the system-level ESD test with an ESD voltage of (a) −10 kV and (b) +10 kV. No TLU-like failure occurs in the system-level ESD test. (Reprinted with permission from IEEE).

Table 8.4 Comparison of the susceptibility between the power-rail ESD clamp circuit with a NMOS reset function and the original power-rail ESD clamp circuit with NMOS + PMOS feedback in the system-level ESD test. (Reprinted with permission from IEEE).

Power-rail ESD clamp circuits	Positive ESD stress	Negative ESD stress
With NMOS + PMOS feedback and NMOS reset function	> + 10 kV	> −10 kV
With NMOS + PMOS feedback (original)	+ 2.5 kV	− 0.2 kV

8.2 In HV CMOS ICs[2]

High-voltage transistors in smart power technologies have been extensively used for display driver ICs, power supplies, power management, and automotive electronics. ESD reliability is an important issue for high-voltage transistors with applications in these products. In smart power technology, high-voltage MOSFET, SCR, and bipolar junction transistors had been used as on-chip ESD protection devices [14–19]. Those works mainly focused on analyzing and improving ESD robustness of the ESD protection devices in high-voltage CMOS processes. In addition to ESD robustness in HV ICs, latchup issues are also significant and need to be carefully considered, especially when the devices are used in power-rail ESD clamp circuits.

HV CMOS technology has been widely used in driver ICs to control the display of liquid crystal display (LCD) panels. Figure 8.16 shows the typical ESD protection scheme for LCD driver ICs (typically, a gate driver with 40 V, and source driver with 12 V, for a 14.1-inch notebook LCD panel). The output buffers (M_P and M_N) are

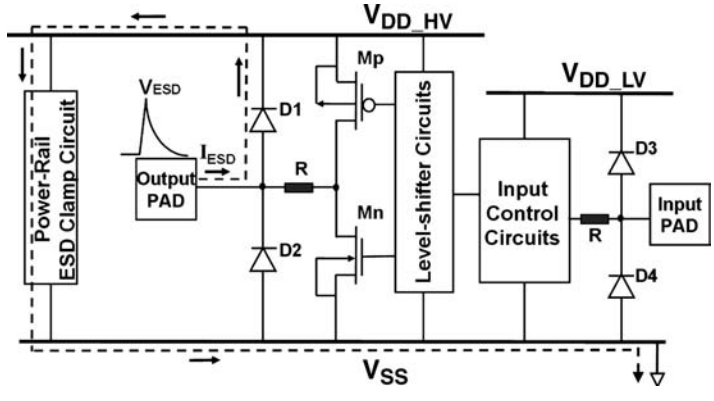


Figure 8.16 The typical ESD protection scheme for LCD driver ICs. (Reprinted with permission from IEEE).

[2]© 2005 IEEE. Reprinted, with permission, from Ming-Dou Ker and K.-H. Lin, The impact of low-holding-voltage issue in high-voltage CMOS technology and the design of latchup-free power-rail ESD clamp circuit for LCD driver ICs (sections I–III and figures 1, 3–6, and 8–17), in *IEEE Journal of Solid-State Circuits*, Vol. 40, no. 8, pp. 1751–1759, Aug. 2005. IEEE, Piscataway, NJ.

controlled by the input control circuits through the level-shifter circuits. The diodes D1 – D4 are used as on-chip ESD protection devices for the input and output pads. For the purpose of avoiding the unexpected ESD damage in the internal circuits of CMOS ICs, the turn-on-efficient power-rail ESD clamp circuit was placed between the V_{DD} and VSS power rails [4]. The ESD current at the output pad under positive-to-V_{SS} ESD stress can be discharged through the diode D1 to the V_{DD}_HV power line, and then discharged through the power-rail ESD clamp circuit from the V_{DD}_HV power line to the grounded V_{SS} power line, as shown by the dashed line in Figure 8.16. Consequently, the traditional I/O circuits cooperating with the power-rail ESD clamp circuit can achieve a much higher ESD level. When the ESD protection device is used in the power-rail ESD clamp circuit, the device is expected to be kept off in the normal circuit operating condition. During the ESD stress conditions, the ESD protection device should be triggered on to discharge the ESD current. If the holding voltage of the ESD protection device in the power-rail ESD clamp circuit is smaller than the power supply voltage, the ESD device may be triggered on by the system-level EMC/ESD transient pulses to cause "TLU" or "TLU-like" failure in CMOS ICs. This phenomenon often leads to IC function failure or even destruction by burning out [20, 21].

8.2.1 High-Voltage ESD Protection Devices

8.2.1.1 TLP I-V Characteristics

The lateral diffused MOS (LDMOS) device, SCR device, and field-oxide (FOD) device are three general ESD protection devices in an HV CMOS process. To investigate the turn-on behaviors of such ESD protection devices during high ESD current stress, a transmission line pulse (TLP) generator [22] with a pulse width of 100 ns and a rise time of ~10 ns is used to measure the "snapback" *I–V* curves of the devices. The cross-sectional views and the TLP-measured *I–V* characteristics of a high-voltage gate-grounded NMOS (GGNMOS) device, an SCR device, an FOD device, and a gate-V_{DD} PMOS (GDPMOS) are shown in Figures 8.17–8.20, respectively. These DUTs are fabricated in a 0.25-μm 40-V CMOS process, and the layout parameters of such ESD protection devices are drawn according to the foundry's ESD rules with a silicide-blocking mask.

For the high-voltage GGNMOS device shown in Figure 8.17a, a "double-snapback" characteristic can be found. As shown in Figure 8.17b, after the first TLP-trigger voltage at 27.2 V (52 V in DC), the device "snaps back" to 23 V, from where the voltage strongly increases again. Then, the device goes into the second "snapback", and the voltage drops to only ~7 V. The turn-on resistance of the first "snapback" state is much larger than that of the second "snapback" state. The "double-snapback" characteristic of the GGNMOS device is related to the turn-on behavior of the parasitic bipolar transistor and the occurrence of the "Kirk effect" (base push-out effect) [23, 24]. The second breakdown current (It2) of a GGNMOS device with a 200-μm channel width is 2.7 A. For the high-voltage SCR device in Figure 8.18a, characteristics of a very low holding voltage and a high ESD robustness can be found. As shown in Figure 8.18b, the holding voltage of the SCR device is only ~4 V and the It2 current of the SCR device with a 200-μm width is

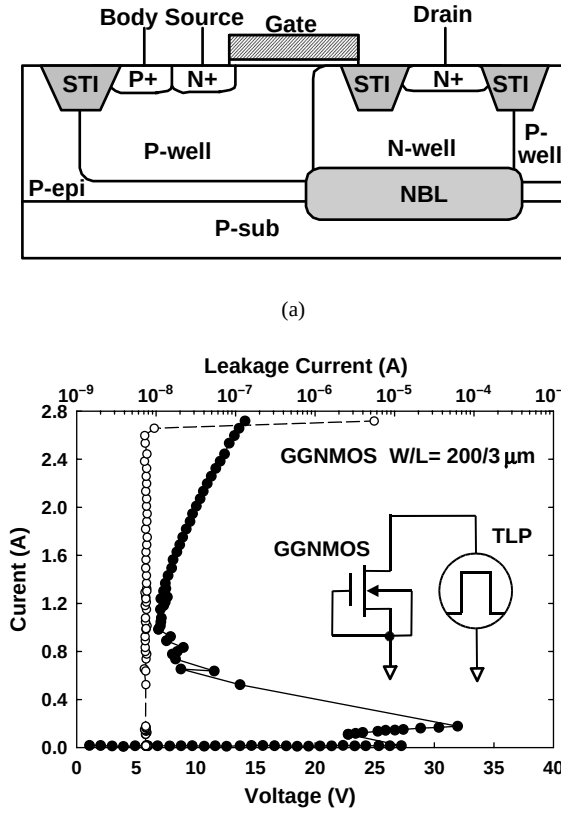
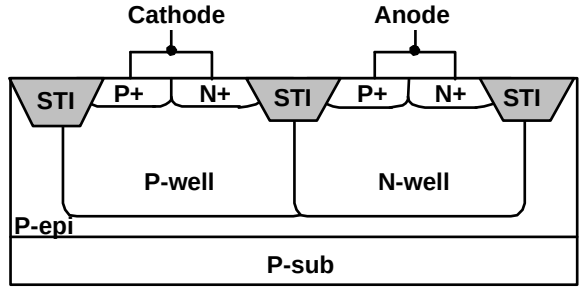
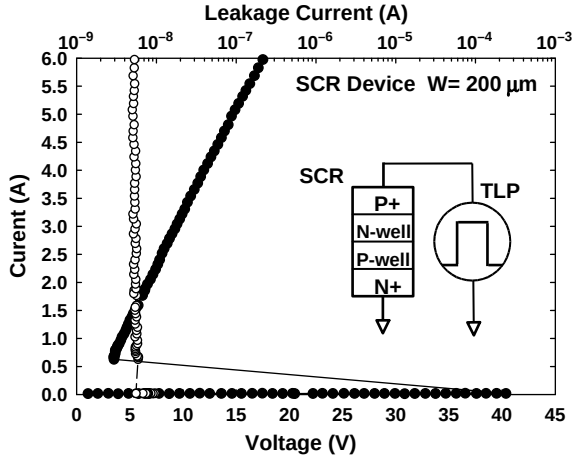


Figure 8.17 (a) Cross-sectional view, and (b) TLP-measured *I–V* characteristics, of a high-voltage gate-grounded NMOS (GGNMOS) device fabricated in a 0.25-µm 40-V CMOS process. (Reprinted with permission from IEEE).

over 6 A. For the high-voltage FOD device structure shown in Figure 8.19a, the device is isolated by the N + buried layer (NBL) from the common P-type substrate. The emitter diffusion is enclosed by the collector diffusion, while the base diffusion is inserted between the emitter diffusion and collector diffusion in the layout structure. The spacing from the collector diffusion to the emitter diffusion of the FOD device is 6 µm in the DUT. As shown in Figure 8.19b, the TLP-trigger voltage is 19.7 V (50 V in DC), and the holding voltage is ~16 V. The It2 current of the FOD device with a 200-µm width is 0.5 A. The difference on the trigger voltages of the device measured by DC (HP4155) and TLP is caused by the transient-coupling effect (d*V*/d*t* transient) through the parasitic capacitance in the drain/bulk junction of the device. The TLP is designed with a rise time of 10 ns to simulate the human-body-model (HBM) ESD event [2]. The d*V*/d*t* transient voltage at the discharging node can generate the displacement current to turn on the parasitic bipolar transistor of the device without involving avalanche breakdown. Therefore, the trigger voltage of the device is lower in the TLP measurement.



(a)



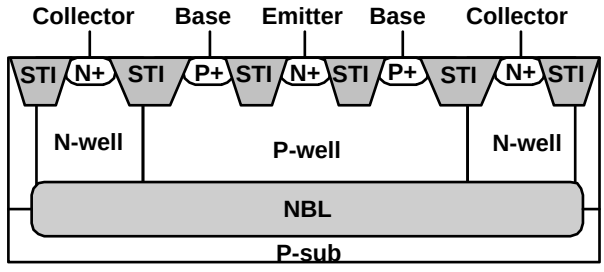
(b)

Figure 8.18 (a) Cross-sectional view, and (b) TLP-measured *I–V* characteristics, of a high-voltage silicon controlled rectifier (SCR) device fabricated in a 0.25-µm 40-V CMOS process. (Reprinted with permission from IEEE).

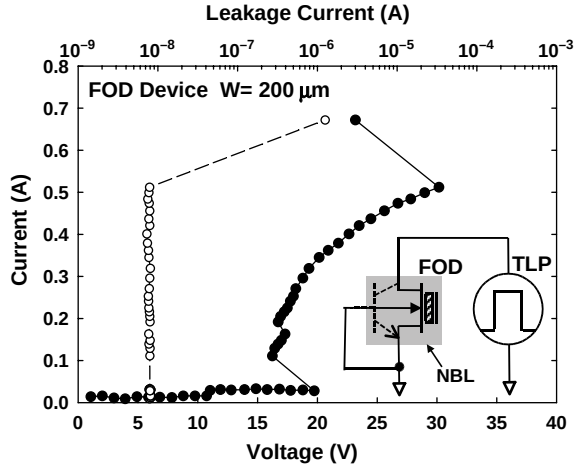
For the high-voltage GDPMOS device shown in Figure 8.20a, no "snapback" characteristic is found. The holding voltage of the device is larger than the supply voltage of 40 V. Due to the inefficient parasitic PNP bipolar action, the It2 current of the GDPMOS device with a 200-µm channel width is only 0.06 A, as shown in Figure 8.20b. Therefore, GDPMOS is not suitable for on-chip ESD protection devices in high-voltage CMOS ICs due to poor ESD robustness.

8.2.1.2 TLU Test

The TLU test is used to investigate the susceptibility of the ESD protection devices to the noise transient or glitch on the power lines during the normal circuit operating condition. The measurement setup for the TLU test is shown in Figure 2.7. A supply



(a)

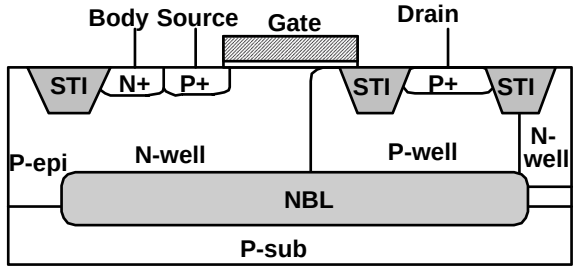


(b)

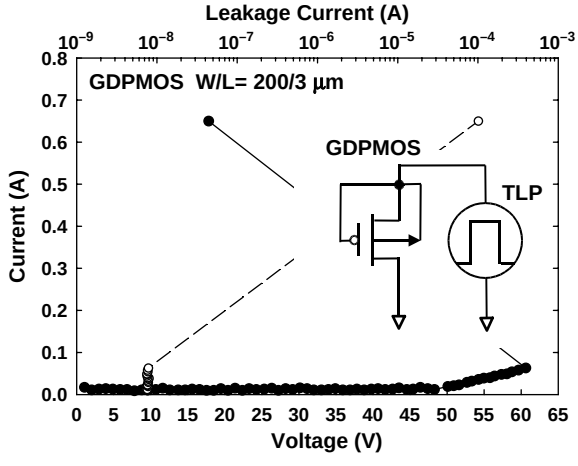
Figure 8.19 (a) Cross-sectional view, and (b) TLP-measured *I–V* characteristics, of a high-voltage field-oxide device (FOD) fabricated in a 0.25-µm 40-V CMOS process. (Reprinted with permission from IEEE).

voltage of 40 V was used to bias the device as the normal circuit operating condition. The measured voltage waveforms on high-voltage GGNMOS devices, SCR devices, and FOD devices in the TLU test are shown in Figures 8.21–8.23, respectively.

The devices are initially kept off before the transient trigger, and therefore the voltage waveforms are initially kept at 40 V. After the transient trigger, the "snapback" characteristic in the device can be triggered on to generate a low-holding-voltage state. The clamped voltage level of the devices in the "snapback" breakdown condition is consistent with the holding voltage measured by TLP stress. In Figure 8.21, the clamped voltage level of a high-voltage GGNMOS device is ~7 V due to the transient triggering with the capacitor charging voltage of 55 V. The GGNMOS device is triggered into the second snapback state directly by the transient pulse. If such a high-voltage NMOSFET is used in the power-rail ESD clamp circuit, the TLU-like issue between the power rails will occur, when the high-voltage NMOSFET is triggered on



(a)



(b)

Figure 8.20 (a) Cross-sectional view, and (b) TLP-measured *I–V* characteristics, of a high-voltage gate-V_{DD} PMOS (GDPMOS) device fabricated in a 0.25-μm 40-V CMOS process. (Reprinted with permission from IEEE).

by the noise transient on the power lines. In Figure 8.22, the clamped voltage level of a high-voltage SCR device is only ∼4 V due to the transient triggering with the capacitor charging voltage of only 44 V. Although a SCR device has the advantage of high ESD robustness, the latchup issue in high-voltage CMOS ICs becomes worse. Figure 8.23a and b show the measured voltage waveforms of a high-voltage FOD device in the TLU test with positive and negative charging voltages, respectively. Both the positive and negative charging voltages can trigger the FOD device into the latch state. The clamped voltage level of the FOD device is ∼16 V due to the transient triggering with a capacitor charging voltage of 47 V or −10 V. For a negative charging voltage, the parasitic N-well/P-substrate junction between the power rails may be turned on initially, but it is turned off quickly due to the transient ringing voltage waveform. Finally, the FOD device is triggered into the holding state. The TLU-like issue is a

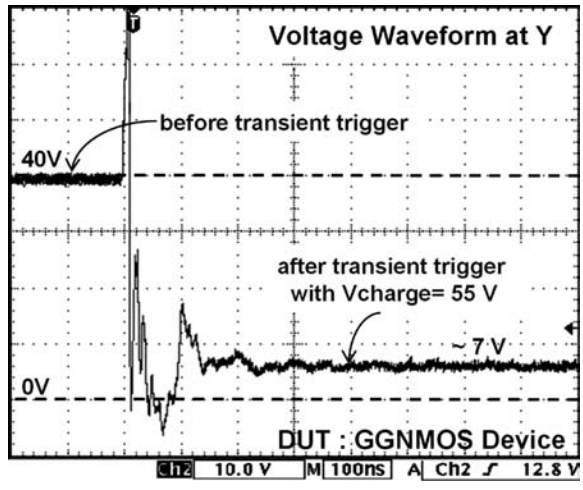


Figure 8.21 The measured voltage waveform on the high-voltage GGNMOS device in the TLU test (Y-axis = 10 V/div., X-axis = 100 ns/div.). (Reprinted with permission from IEEE).

concern with the use of a single FOD device as the power-rail ESD clamp in high-voltage CMOS ICs.

From the power dissipation view, a device with a lower holding voltage is helpful for sustaining a much higher ESD current. However, TLU may be triggered on by the noise transient or glitch on the power lines during normal circuit operating conditions, especially in the system-level EMC/ESD discharging test. If the holding voltages of

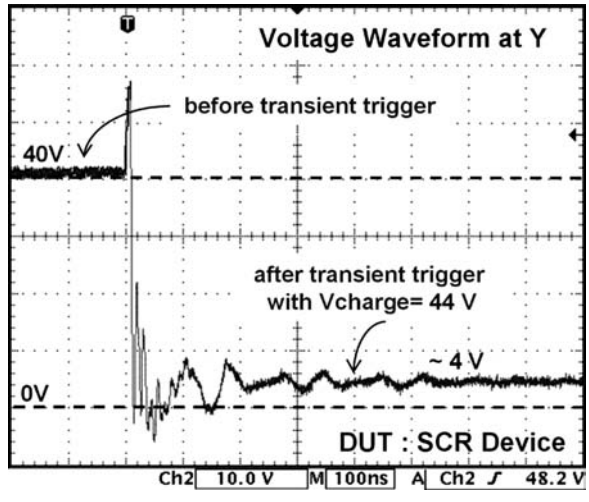
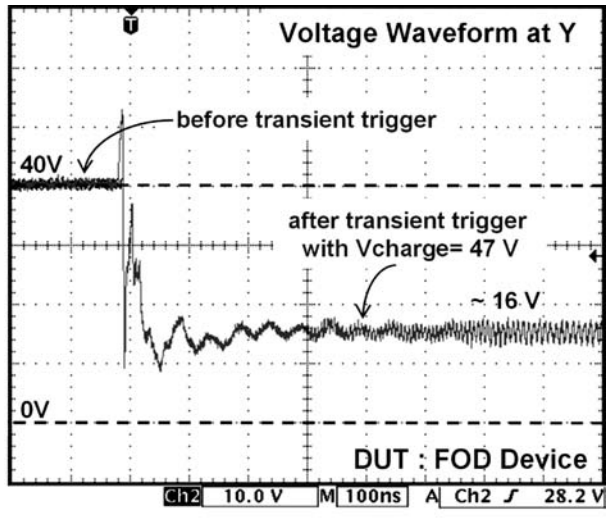
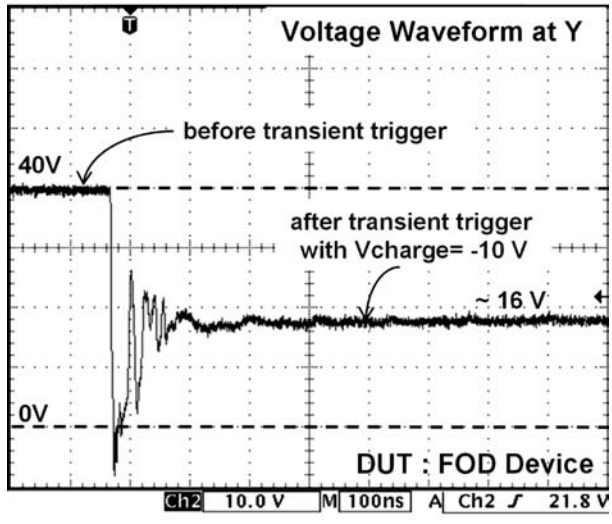


Figure 8.22 The measured voltage waveform on the high-voltage SCR device in the TLU test (Y-axis = 10 V/div., X-axis = 100 ns/div.). (Reprinted with permission from IEEE).



(a)



(b)

Figure 8.23 The measured voltage waveforms on the high-voltage FOD device in the TLU test with (a) a positive charging voltage, and (b) a negative charging voltage (Y-axis = 10 V/div., X-axis = 100 ns/div.). (Reprinted with permission from IEEE).

high-voltage ESD protection devices are smaller than the power supply voltages in normal circuit operating conditions, high-voltage CMOS ICs will be susceptible to TLU or TLU-like danger in system applications, which often encounter such issues as noise or transient glitches.

8.2.2 Design of TLU-Free Power-Rail ESD Clamp Circuits

NMOS and SCR devices have a higher It2 than that of the FOD device, but their holding voltages (∼7 V in an NMOS, ∼4 V in a SCR) are far away from the 40-V operating voltage level. Such ESD protection devices with a low holding voltage in power-rail ESD clamp circuits will cause serious TLU failure to high-voltage CMOS ICs. To overcome the TLU or TLU-like issue between the power rails in high-voltage CMOS ICs during the normal circuit operating condition, a new stacked-field-oxide structure can be designed to increase the total holding voltage. The layout top view with the corresponding schematic diagram and the cross-sectional view of the stacked-field-oxide structure with two cascaded FOD devices fabricated in a 0.25-μm 40-V CMOS process are shown in Figure 8.24a and b, respectively. The layout area of the stacked-field-oxide structure with a device width of 200 μm for each FOD device is $150 \times 60\,\mu m$.

8.2.2.1 ESD Robustness

The measurement setup of a single high-voltage FOD device and a stacked-field-oxide structure under TLP stress is shown in Figure 8.25a. The TLP-measured *I–V* characteristics of these devices with different device widths are compared in Figure 8.25b. The holding voltage of the stacked-field-oxide structure in the "snapback" region is double that of a single FOD device. It's important to note that each FOD device in a stacked-field-oxide structure is isolated by the NBL from the common P-type substrate. The turn-on current can flow through the cascaded parasitic bipolar transistor of each FOD device and the accumulation property in holding voltage for the stacked-field-oxide structure can be achieved. Therefore, the holding voltage of a stacked-field-oxide structure can be linearly increased by increasing the number of cascaded FOD devices. The It2 currents of a single FOD device and the stacked-field-oxide structure as a function of device channel width are compared in Figure 8.26. The It2 current of the stacked-field-oxide structure is linearly increased while the device channel width increases. In addition, the It2 current of the stacked-field-oxide structure is only slightly degraded when compared with that of a single FOD device. The relation between It2 and the HBM ESD level, V_{ESD}, can be approximated as follows:

$$V_{ESD} \cong (1500 + R_{ON}) \times \text{It2} \tag{8.1}$$

where R_{ON} is the dynamic turn-on resistance of the DUT. From Figure 8.26, the stacked-field-oxide structure with a device width of ∼650 μm for each FOD device can sustain the typical 2-kV (It2 of ∼1.33 A) HBM ESD stress. To meet the specified ESD level of driver ICs, this can be achieved by adjusting the device width of the stacked-field-oxide devices.

To investigate the temperature-dependent behavior of the stacked-field-oxide structure, the TLP-measured *I–V* characteristics of the stacked-field-oxide structure

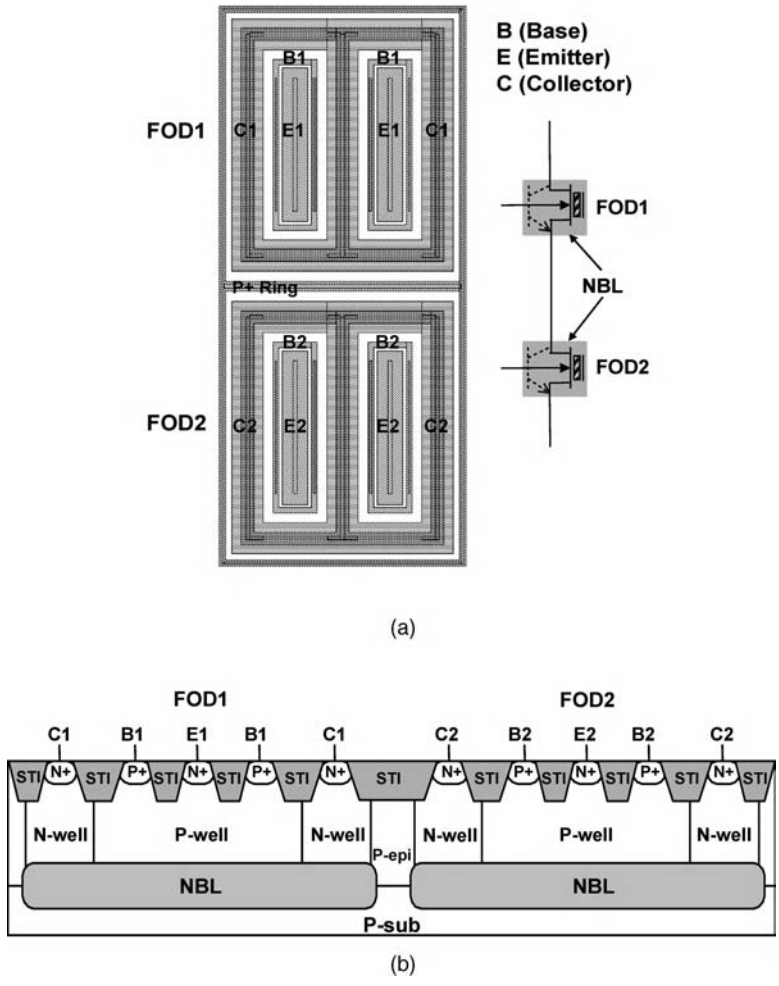
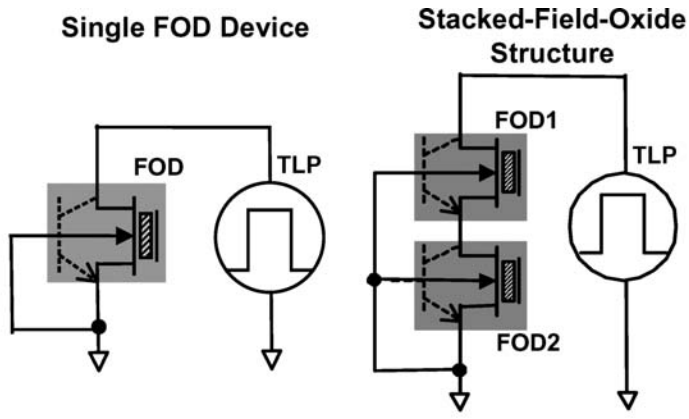


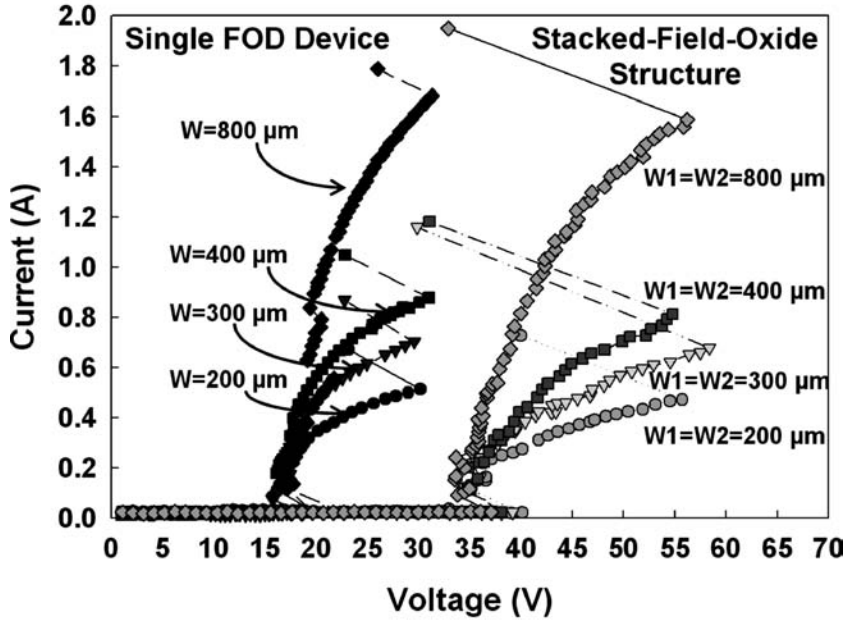
Figure 8.24 (a) The layout view with the corresponding schematic diagram, and (b) the cross-sectional view, of the stacked-field-oxide structure with two cascaded FOD devices. Each FOD device in the stacked-field-oxide structure is isolated by the N+ buried layer (NBL) from the common P-type substrate. The metal connections between the FOD devices are not shown. (Reprinted with permission from IEEE).

under different temperatures (25, 75, and 125 °C) are compared in Figure 8.27. No significant difference on the holding voltage of the stacked-field-oxide structure is observed when the temperature increases. Therefore, the holding voltage of the stacked-field-oxide structure can be successfully controlled by the cascaded FOD devices, even at high temperatures.

During the ESD stress condition, the ESD clamp device should turn on quickly to bypass the ESD current, before the internal circuits are damaged by the ESD



(a)



(b)

Figure 8.25 (a) The measurement setup of a single high-voltage FOD device and a stacked-field-oxide structure under TLP stress. (b) The TLP-measured *I–V* characteristics of these devices with different device widths. W1 is the channel width of FOD1, and W2 is the channel width of FOD2. (Reprinted with permission from IEEE).

energy. From Figure 8.25, the trigger voltage of the stacked-field-oxide structure is increased as compared with that of a single FOD device. The substrate-triggered technique [25–28] can be applied to lower the trigger voltage of the device to ensure effective ESD protection. The TLP-measured *I–V* curves of the stacked-field-oxide

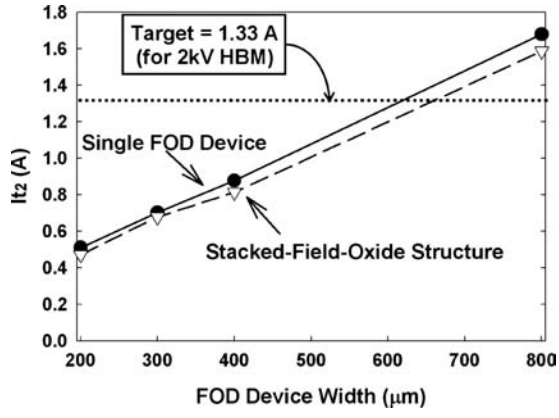


Figure 8.26 It2 currents of a single FOD device and a stacked-field-oxide structure as a function of device channel width. (Reprinted with permission from IEEE).

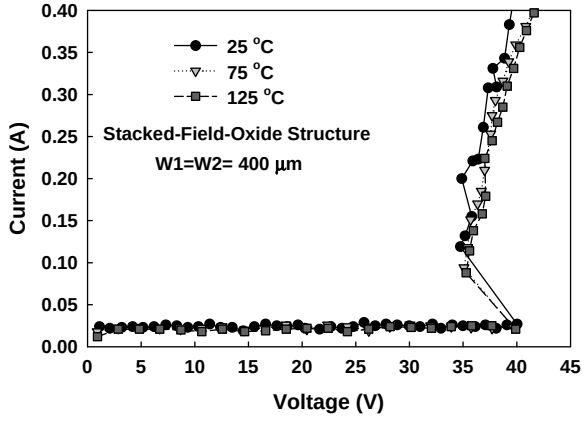


Figure 8.27 The holding voltage of the stacked-field-oxide structure (two cascaded FOD devices) under different temperatures measured by TLP. (Reprinted with permission from IEEE).

structure with different substrate-triggered currents (I_{trig}) are shown in Figure 8.28. The trigger voltage of the stacked-field-oxide structure is obviously decreased when the substrate-triggered current is applied. The trigger voltage can be reduced to only 17 V when the substrate-triggered current is 10 mA. Therefore, the trigger voltage of the stacked-field-oxide structure can be effectively reduced to be lower than the breakdown voltage of the internal circuits by the substrate-triggered technique. Moreover, the It2 level of the stacked-field-oxide structure with a substrate-triggered current can be improved.

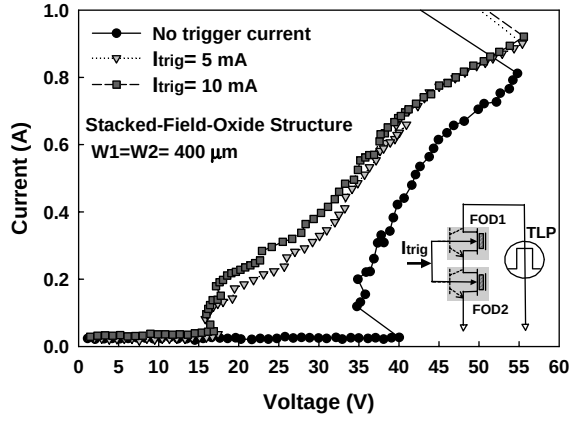


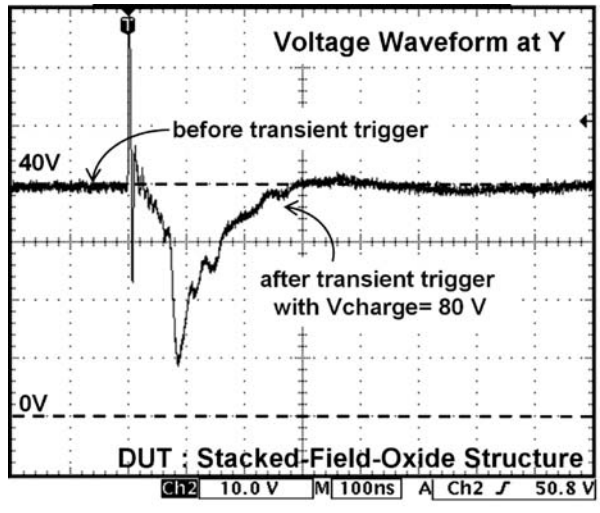
Figure 8.28 The TLP-measured *I–V* curves of the stacked-field-oxide structure with different substrate-triggered currents. (Reprinted with permission from IEEE).

8.2.2.2 TLU Immunity

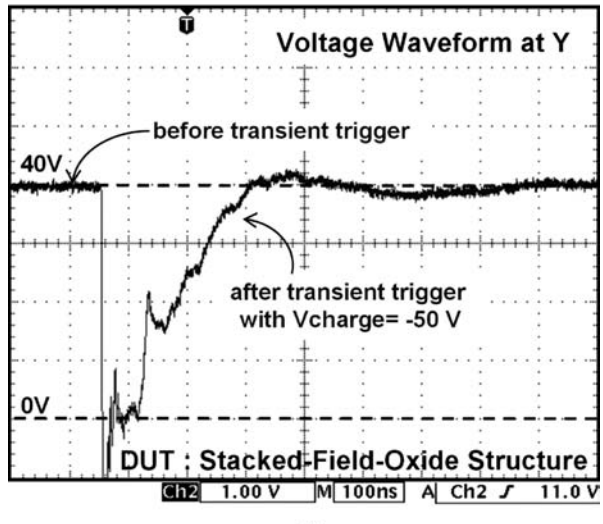
The measured voltage waveforms of the stacked-field-oxide structure in the TLU test with transient triggering of the positive and negative charging voltages are shown in Figure 8.29a and b, respectively. The stacked-field-oxide structure is triggered on due to transient triggering with capacitor charging voltages of 80 V or −50 V. But, the clamped voltage waveform quickly comes back to the original supply voltage level of 40 V, without keeping in the latch state after triggering. This is consistent with the TLP-measured *I–V* curves shown in Figure 8.25b. The total holding voltage of the stacked-field-oxide structure with two cascaded FOD devices is near the supply voltage of 40 V. After the stacked-field-oxide structure is triggered on during the TLU test, the clamped voltage level can quickly restore to the supply voltage. Therefore, no TLU or TLU-like issue occurs. In addition, a higher charging voltage is needed to trigger on the stacked-field-oxide structure during the TLU test. Therefore, the TLU immunity of stacked-field-oxide structure to the noise transient on the power lines in high-voltage CMOS ICs can be significantly improved.

8.2.2.3 Latchup-Free Power-Rail ESD Clamp Circuits

The power-rail ESD clamp circuits with two cascaded FOD devices and three cascaded FOD devices in high-voltage CMOS ICs are shown in Figure 8.30a and b, respectively. Each FOD device in the stacked-field-oxide structure is isolated by the NBL from the common P-type substrate. With two cascaded FOD devices as shown in Figure 8.30a, the total holding voltage of the stacked-field-oxide structure in the "snapback" region is double that of a single FOD device. The TLU immunity of the power-rail ESD clamp circuit to the noise transient during normal circuit operating conditions can be highly



(a)



(b)

Figure 8.29 The measured voltage waveforms on the stacked-field-oxide structure in the TLU test with (a) positive charging voltage, and (b) negative charging voltage (Y-axis = 10 V/div., X-axis = 100 ns/div.). (Reprinted with permission from IEEE).

improved. With the three cascaded FOD devices shown in Figure 8.30b, the total holding voltage of the stacked-field-oxide structure can be designed to be higher than the supply voltage. The blocking diodes (Db) are used to block the current flowing through the metals connected between the trigger nodes (base nodes) of the stacked FOD devices [29]. Therefore, the unexpected current path can be avoided and the

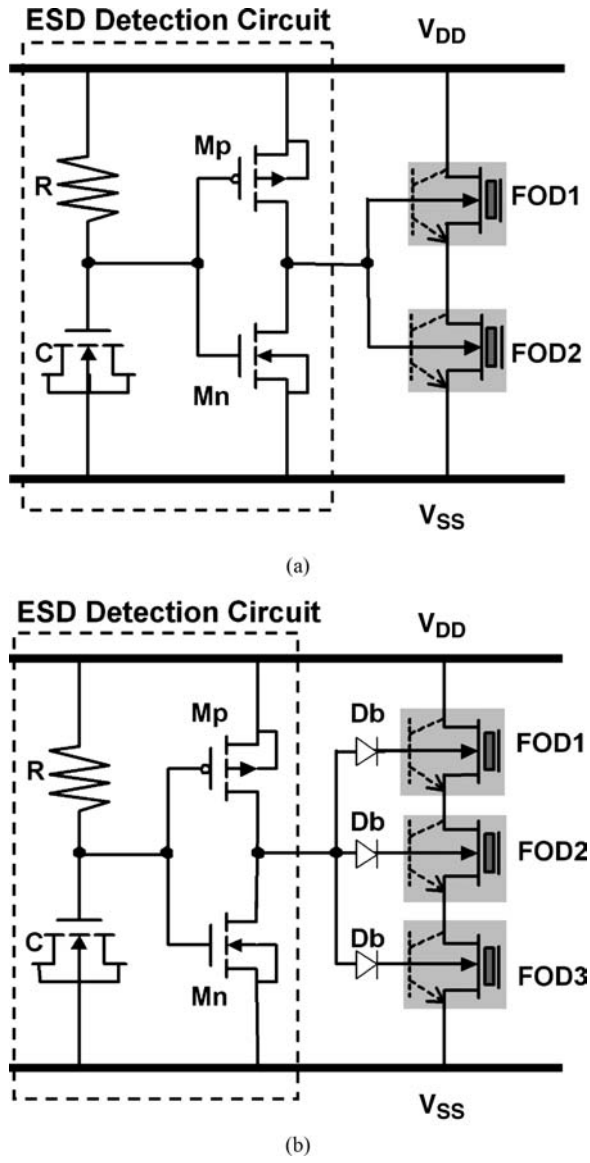


Figure 8.30 The power-rail ESD clamp circuits in high-voltage CMOS ICs with (a) two cascaded FOD devices, and (b) three cascaded FOD devices. The blocking diodes Db are used to block the current flowing through the metals connected among the trigger nodes (base nodes) of the stacked FOD devices [29]. (Reprinted with permission from IEEE).

accumulation property in the holding voltage for the three cascaded FOD devices can be achieved. In addition, if the total holding voltage of the stacked structure can be designed to be higher than the supply voltage, the FOD3 in Figure 8.30b can be even replaced by other types of ESD device. By adjusting different numbers or even

different types of the stacked ESD devices (NMOS, SCR, or FOD) in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed to be higher than the supply voltage. With a total holding voltage of the stacked structure higher than the supply voltage, the TLU or TLU-like issue will not occur even though the stacked structure is mis-triggered by the noise transient or glitch on the power lines during a normal circuit operating condition. Therefore, the TLU issue can be successfully overcome without modifying the high-voltage CMOS process. To provide effective ESD protection for the internal circuits during ESD stress, the substrate-triggered technique can be achieved by the RC-based ESD detection circuit [25]. The RC-based ESD detection circuit can detect the ESD pulse to provide trigger current into the stacked structure, and then the stacked structure can turn on quickly to discharge the ESD current.

8.3 Conclusion

With continually progressing CMOS technologies, ESD robustness is always the major concern when designing the power-rail ESD clamp circuits. However, TLU or TLU-like issues are usually overlooked and most probably lead to IC malfunction or damage in field applications. Moreover, the strictly demanded EMC regulations have made TLU or TLU-like issue a significant reliability concern in electronic products.

In LV CMOS ICs, it is generally believed that latchup is no longer a major reliability concern due to the continually shrinking nominal operating voltages of ICs. Once the layout schemes are carefully arranged with guard ring protection in the latchup-sensitive parts, the latchup holding voltage could always be enhanced higher than such small operating voltage, resulting in latchup not happening anymore. In the advanced LV power-rail ESD clamp circuits, however, a "TLU-like" risk could still lead to IC malfunction or damage if the regenerative feedback network is used to reduce the RC time constant and stand-by power consumption. With experimental verification and failure analysis, such a TLU-like issue results from the continually turn-on ESD-clamping NMOS after the system-level ESD stress. Therefore, a regenerative feedback network incorporated with a carefully-designed device size or NMOS reset function is necessary to solve the TLU-like issue.

In contrast to LV CMOS ICs, HV CMOS ICs are usually sensitive to latchup due to a much higher nominal operating voltage, even if the double guard rings are equipped in the HV latchup-sensitive parts. Thus, in the HV power-rail ESD clamp circuits, TLU could easily be initiated by a noise transient or glitch on the power lines during normal circuit operating conditions. The stacking structures of HV ESD protection devices can avoid the potential TLU risk by increasing the latchup holding voltage to be higher than the IC operating voltage. Although the ESD robustness would be somewhat degraded in stacking ESD protection devices, a properly enlarged device size or substrate-triggered technique can be used to enhance the ESD robustness without suffering TLU risk.

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9

Summary

9.1 TLU in CMOS ICs

In the system-level ESD test or EFT test, more and more failure returns indicated that TLU issues are the major reasons. As electronic products are subjected to increasingly tight requirements of the EMC specifications, TLU issues continue to play an important failure mechanism throughout the ICs industry. As the technology feature sizes continually scale down to the nanometer regime, the aggressively decreasing anode-to-cathode spacing of the parasitic SCR leads the CMOS ICs to be very susceptible to TLU. Specifically, state-of-the-art IC design trends or process technologies, such as mixed signals, SOC, RF, scaling of trench isolation, and usage of low-doped substrates, also drive TLU to be a major reliability issue in CMOS ICs. Consumer electronic products that are usually carried with humans, such as cell phones, personal digital assistants (PDAs), digital cameras, thumb disks, and so on, are specifically demanded to be robust in the system-level ESD test or EFT test. Much stricter requirements than those specified in the IEC standard are strongly requested for CMOS ICs used in such consumer electronic products. Therefore, experimental methodologies for TLU characterization, as well as efficient protection designs against TLU are necessary for the ICs industry.

The underdamped sinusoidal (bipolar) voltage stimulus on the power or ground pins of CMOS ICs has been clarified as the practical TLU-triggering stimuli in the system-level ESD test. Such a bipolar trigger can generate the sweep-back current, which is also found in the EFT test, to activate the parasitic SCR into the latchup state. Therefore, compared with the component-level TLU measurement setup with a negative-going rectangular voltage pulse as specified in TLU standard practice, the component-level TLU measurement setup with a bipolar trigger voltage source is preferable to evaluate the TLU robustness of CMOS ICs. In this measurement setup with a bipolar trigger, two common discrete components used in the measurement

Transient-Induced Latchup in CMOS Integrated Circuits Ming-Dou Ker and Sheng-Fu Hsu
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setup – the current-blocking diode and current-limiting resistor, have been found to have adverse impacts on TLU characterization. Measurement setups equipped with a current-blocking diode or a current-limiting resistor can fail to produce the intended bipolar trigger or can attenuate the amplitude of a bipolar trigger, leading to the over estimation of TLU immunity of a DUT. Thus, a TLU measurement setup without a current-blocking diode but with a small current-limiting resistance (e.g. 5 Ω) is suggested. This suggested TLU measurement setup not only can accurately evaluate the TLU immunity of CMOS ICs without over estimation, but also can avoid EOS damage to the DUT during a TLU test. It can be also used to evaluate the effectiveness of discrete board-level noise filters for enhancements of TLU immunity. In addition, it has been proven that a bipolar trigger with a proper D_{Factor} ($<10^7\ \text{s}^{-1}$) and a specified D_{Freq} of tens of megahertz is better for characterizations of TLU immunity, because bipolar triggers with such specified D_{Factor} and D_{Freq} parameters can initiate TLU most easily. Thus, each constituting component in the measurement setup, including the charged capacitor, discharge resistor, relay, sockets, current-limiting resistor, and so on, should be optimized to be capable of producing the bipolar trigger with intended D_{Factor} and D_{Freq} parameters. When this is done, the measurement setup can precisely evaluate the TLU immunity of CMOS ICs without over estimation.

The ESD-induced bipolar voltage on the power or ground pin of CMOS ICs is the major cause of TLU in the system-level ESD test. Thus, compared with the quasi-static latchup that usually occurs in I/O cells rather than the internal circuitry, TLU initiated by the system-level ESD test could easily happen in the internal circuitry, because the power and ground lines are widely distributed over the whole circuitry in a chip. For quasi-static latchup, the general solution to improve the latchup immunity of core circuitry is to enlarge the distance from the I/O to the internal circuitry, or to insert additional guard rings between the I/O and the internal circuitry. Such a solution, however, is not suitable for TLU prevention, because ESD-coupled noises can be generated via the induction of an electromagnetic field. This phenomenon reminds us that CMOS ICs will be much more susceptible to TLU than to quasi-staic latchup in advanced CMOS technologies. Thus, novel systems, circuits, and process techniques to efficiently suppress the TLU susceptibility of CMOS ICs are necessary. In addition to using board-level noise filters, some other techniques could be implemented simultaneously to further improve the TLU immunity of the CMOS ICs in the system-level ESD test. For example, circuit design techniques such as on-chip noise filters, ESD-induced noise detection circuits, and latchup auto-detection circuits with self-stop functions can be used to detect and suppress TLU. As for the system design techniques, hardware and firmware co-design with system-auto-reset functions can be also used to solve TLU issues by detecting system-level ESD events and subsequently resetting the system without disturbing normal functionality. In addition, proper enclosure, PCB layout, circuit layout, and package type designs are also help further improve the robustness of CMOS ICs against TLU.

9.2 Extraction of Compact and Safe Layout Rules for Latchup Prevention

It has been a long time since latchup was an important reliability issue in CMOS ICs. With the introduction of retrograde wells, trench isolation, epitaxial wafers, and so on, latchup was once thought to be never an issue again. However, with the increasing focus on device integration densities, mixed signals, RF, SOC, and P-(low-doped) substrates, robust CMOS ICs have once again become a tough challenge. Additionally, because of the continually increasing complexity of circuit functionality, future generations of CMOS ICs can easily possess pad counts in excess of 1000. In such high-pin-count CMOS ICs, the total layout area of the I/O circuitry is dominant with respect to the total chip layout area. For cost-down purposes, the layout design rules for latchup prevention in I/O cells is critical in saving the total chip area in future CMOS ICs. As a result, compact and safe design rules are highly demanded for CMOS ICs.

In general, layout design rules for latchup prevention must be specified for I/O cells, for internal circuits, and for between I/O cells and internal circuits. Latchup-preventing layout rules in I/O circuitry are critical for saving the total chip layout area. Especially, the layout rules such as guard ring designs (double guard rings, a single guard ring, or no guard ring) and minimum spacing between the source regions of the PMOS and the NMOS (anode-to-cathode spacing) are dominant factors. Practical experience have shown that a single guard ring is enough to help the I/O cells to be immune to latchup (that is, latchup-free) by raising the latchup holding voltage to be greater than the normal circuit operating voltage. With a single guard ring and a proper anode-to-cathode spacing, latchup-free and area-efficient I/O cells can be achieved. For internal circuits, however, latchup-free is hardly achieved due to the lack of protection of the guard rings as well as the demand for high integration of circuitry, even though there is a high pickup density. Enlarging the spacing between the I/O and the internal circuitry can greatly enhance the latchup robustness of the internal circuitry against the trigger current injecting into the I/O pins. Furthermore, inserting additional double guard rings between the I/O and the internal circuitry can also help to further improve the latchup immunity of the internal circuitry. As a result, latchup-preventing layout rules between the I/O and the internal circuitry need to be specified to ensure a latchup-robust internal circuitry.

In addition to the general latchup-preventing layout rules that specify detailed latchup rules for I/O cells, for internal circuits, and for between the I/O cells and the internal circuits, some other important latchup rules for circuits across two different power domains are also required. Specifically in mix-voltage CMOS ICs, power-supply voltages with different magnitudes can coexist in a single CMOS chip, leading to potential latchup issues between two different power domains. Similar to conventional latchup phenomena, the occurrence of this unique latchup is mainly due to the parasitic SCR in CMOS ICs. However, unlike the conventional latchup path going through from V_{DD} to the GND, such a specific latchup path exists between the two different power domains ($V_{DD,H}$ and $V_{DD,L}$), going through from $V_{DD,H}$ to $V_{DD,L}$. To

prevent the potential latchup between $V_{DD,H}$ and VDD,$_L$, critical parameters such as the minimum spacing between the P+ diffusions powered by $V_{DD,H}$ in the N-Well, and N+ diffusions powered by $V_{DD,L}$ in the N-well should be clearly defined. Besides, the inserted P+ guard ring located in the P-well between $V_{DD,H}$ and $V_{DD,L}$ also suppresses the latchup susceptibility between the two different power domains, and its minimum width also needs to be well defined in comprehensive latchup design rules.

As mentioned, the effect of latchup on circuit reliability has been a major hindrance to achieving reliable circuit performance. Only developing safe and compact design rules for latchup prevention can ensure latchup-robust and area-efficient IC designs.

Appendix A: Practical Application—Extractions of Latchup Design Rules in a 0.18-μm 1.8 V/3.3 V Silicided CMOS Process

This appendix gives a practical example of extracting layout rules/guidelines for latchup prevention in a 0.18-μm 1.8 V/3.3 V silicided CMOS process. The methodologies to extract all the latchup design rules/guidelines are in compliance with those presented in Chapter 6. The layout top view and device cross-sectional view to illustrate layout rules for latchup prevention are shown in Figure A.1a and b, respectively. The latchup layout rules/guidelines are extracted for I/O cells, for internal circuits, and for between I/O and internal circuits. In addition, the latchup layout rules for circuits across two different power domains are also extracted to avoid possible latchup danger between two N-wells powered by two different power-supply voltages (1.8 V and 3.3 V), as introduced in Chapter 7.

A.1 For I/O Cells

A.1.1 Nomenclature

The nomenclatures representing the latchup layout rules for I/O cells are listed below, and can be referred to in detail in Figure A.1.

3A3 (3B3): Minimum width of an N+ base guard ring for a 1.8 V (3.3 V) PMOS.
3A4 (3B4): Minimum width of a P+ base guard ring for a 1.8 V (3.3 V) NMOS.
3A7 (3B7): Minimum width of a P+ collector guard ring for a 1.8 V (3.3 V) PMOS.
3A8 (3B8): Minimum width of an N+ collector guard ring for a 1.8 V (3.3 V) NMOS.
3A9 (3B9): Minimum spacing between the source regions of a 1.8 V (3.3 V) NMOS and a 1.8 V (3.3 V) PMOS.

Transient-Induced Latchup in CMOS Integrated Circuits Ming-Dou Ker and Sheng-Fu Hsu
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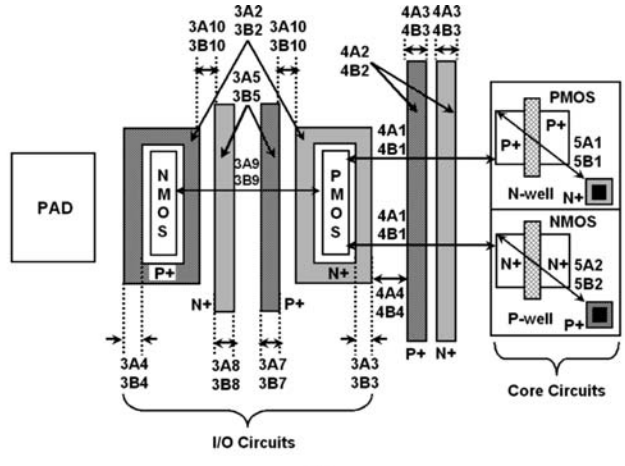
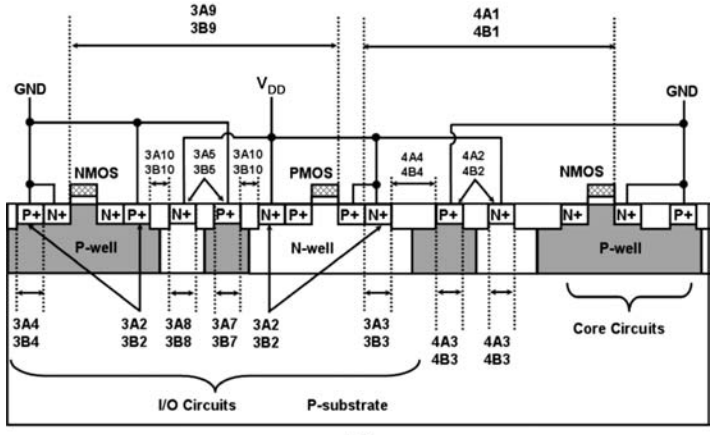


(a)



(b)

Figure A.1 (a) Layout top view, and (b) device cross-sectional view, to illustrate the layout rules for latchup prevention in a 0.18-μm 1.8 V/3.3 V silicided CMOS process.

3A10 (3B10): Maximum spacing between the base guard ring and the collector guard ring for 1.8 V (3.3 V) Devices.

A.1.2 I/O Cells with Double Guard Rings

A.1.2.1 Design of Test Structures

As presented in Chapter 6, the I/O cells with different geometrical parameters are used as the test structures. A layout example of the I/O test structure with double guard

rings is shown in Figure A.2. The PMOS and NMOS devices in the I/O cells are drawn in the multiple-finger style with a fixed length of 30 μm per finger. The channel lengths of PMOS and NMOS are the same, 0.25 μm (0.5 μm), for 1.8 V (3.3 V) devices, and the total channel width consisting of 14 fingers are the same, 420 μm, for both PMOS and NMOS. To simplify measurements of the latchup DC *I–V* characteristics and the JEDEC latchup test, the gate of the PMOS is connected to V_{DD} and the gate of the NMOS is connected to V_{SS}, turning off both the PMOS and NMOS. It is noteworthy that the collector guard rings do not surround the base guard rings, but instead, the collector guard rings are only inserted between the PMOS and NMOS. Such placement methodologies of the collector guard rings can save more layout area, and simultaneously do not degrade the latchup robustness of the I/O cells at all.

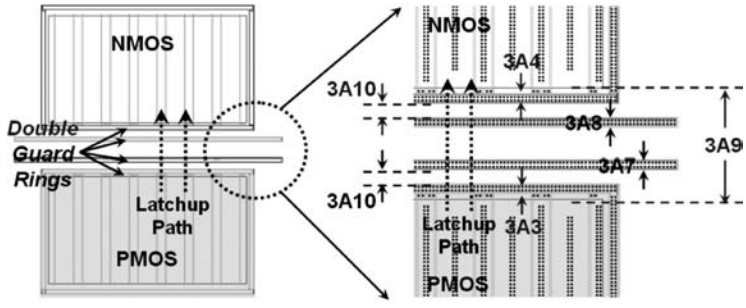


Figure A.2 Layout example of the I/O test structure with double guard rings.

The splits of the layout parameters to evaluate the minimum anode-to-cathode spacing (3A9 and 3B9) and base/collector guard ring width (3A3, 3A4, 3A7, 3A8, 3B3, 3B4, 3B7, and 3B8) are listed in Table A.1a, and the splits of the layout parameters to evaluate the maximum spacing between the base and collector guard ring (3A10 and 3B10) are listed in Table A.1b. For a given anode-to-cathode spacing, the base/collector guard ring width should be drawn as compact as possible to achieve the best latchup robustness. For example, for a given anode-to-cathode spacing of 15 μm, the maximum base/collector guard ring width that can be drawn within this specific spacing is 3 μm. Thus, safe and compact latchup layout rules can be extracted.

A.1.2.2 Latchup Immunity Dependency of I/O Cells with Double Guard Rings

The JEDEC latchup test is performed at first. The related experimental results are summarized in Table A.2. With a test temperature of 25 °C, all structures pass the JEDEC specifications that latchup is not triggered on with 1.5× maximum *V*supply for the over-voltage test, and with ±100 mA at the I/O pins for the trigger current test. Indeed, all the test structures are latchup-robust because they can sustain a large trigger

Table A.1a Splits of layout parameters to evaluate latchup immunity dependencies on 3A3, 3A4, 3A7, 3A8, and 3A9 (3B3, 3B4, 3B7, 3B8, and 3B9), in I/O cells with double guard rings.

3A10 (3B10) = 0.36 μm	
3A9 (3B9)	3A3 = 3A4 = 3A7 = 3A8 (3B3 = 3B4 = 3B7 = 3B8)
7 μm	1 μm
11 μm	1 μm
	2 μm
15 μm	1 μm
	2 μm
	3 μm
19 μm	1 μm
	2 μm
	3 μm
	4 μm

Table A.1b Splits of layout parameters to evaluate latchup immunity dependencies on 3A10 (3B10), in I/O cells with double guard rings.

3A9 (3B9) = 15 μm	3A3 = 3A4 = 3A7 = 3A8 (3B3 = 3B4 = 3B7 = 3B8) = 1 μm
3A10 (3B10)	0.36 μm
	1.2 μm
	2.2 μm
	3.2 μm
	4.2 μm

Table A.2 Experimental results of the JEDEC latchup test for I/O cells with double guard rings.

	V_{supply} over-voltage test	*I*-test
Specification requirement	1.5 × maximum V_{supply}	> +/−100 mA
1.8 V I/O (double guard rings)	Pass (> 2.7 V)	Pass (> +/−400 mA)
3.3 V I/O (double guard rings)	Pass (> 5 V)	Pass (> +/−400 mA)

current of ±400 mA without latchup being initiated, regardless of 1.8 V or 3.3 V devices.

Although all the test structures have good latchup immunity, they could still probably suffer latchup under an even higher trigger voltage or current. To further judge whether the test structures are immune to latchup, the latchup holding voltage dependency on layout parameters are also considered. An example of the measured latchup *I–V* curve of the I/O circuits with double guard rings is shown in Figure A.3. Both the 1.8 V and 3.3 V DUTs have an anode-to-cathode spacing (3A9 and 3B9) of

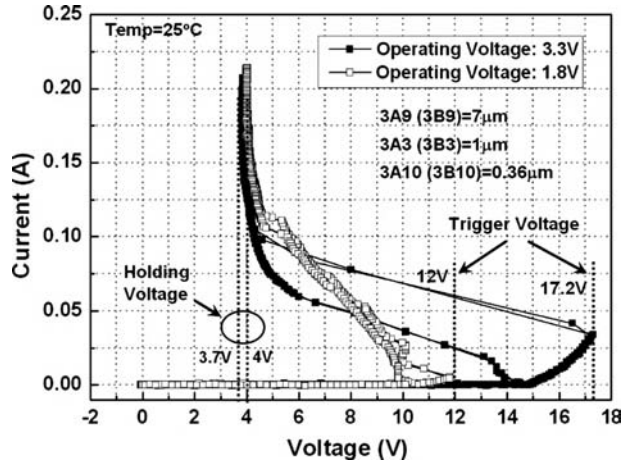


Figure A.3 Example of the measured latchup *I–V* curve of I/O circuits with double guard rings.

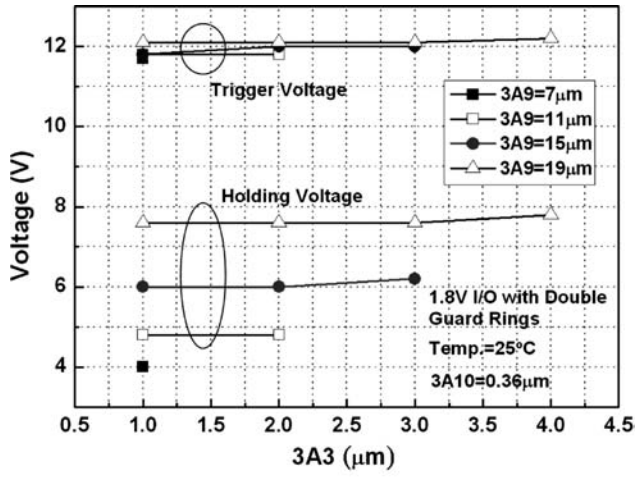
7 μm, a base/collector guard ring width (3A3 and 3B3) of 1 μm, and a spacing between the base and collector guard ring (3A10 and 3B10) of 0.36 μm. Obviously, the 1.8 V (3.3 V) DUT has a very large holding voltage of 4 V (3.7 V), which is larger than its normal circuit operating voltage of 1.8 V (3.3 V), that is, latchup-free, even though there are a small 3A9 and 3A3 (3B9 and 3B3). For the 1.8 V devices, the latchup trigger and holding voltage dependencies on all layout splits are shown in Figure A.4a and b. It was found that all the test structures have a latchup trigger voltage of ∼12 V, and a latchup holding voltage of >4 V. Similarly, the corresponding measurement results for 3.3 V devices are shown in Figure A.5a and b. Again, the I/O cells with double guard rings are very latchup-robust due to their large holding voltages of >3.7 V, even for a very small 3B3 of 1 μm and a small 3B9 of 7 μm.

Measurements to consider the degradation of latchup immunity due to a high test temperature are also performed. For 1.8 V (3.3 V) devices, the holding voltage dependencies on all layout splits under different test temperatures are shown in Figures A.6 and A.7. I/O cells with double guard rings still perform well in latchup robustness, even under a high test temperature of 125 °C. For example, the holding voltage is at least higher than 3.3 V under a test temperature of 125 °C, even for a very small 3B3 of 1 μm and a small 3B9 of 7 μm, regardless of 1.8 V or 3.3 V devices. Thus, I/O cells with double guard rings certainly have good latchup immunity.

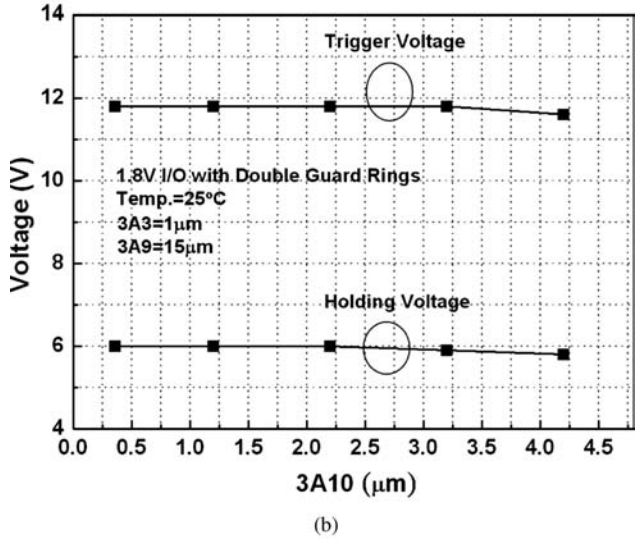
A.1.3 I/O Cells with a Single Guard Ring

A.1.3.1 Design of Test Structures

Although I/O cells with double guard rings perform very well in latchup robustness, double guard rings inevitably occupy a large layout area in comparison with a single



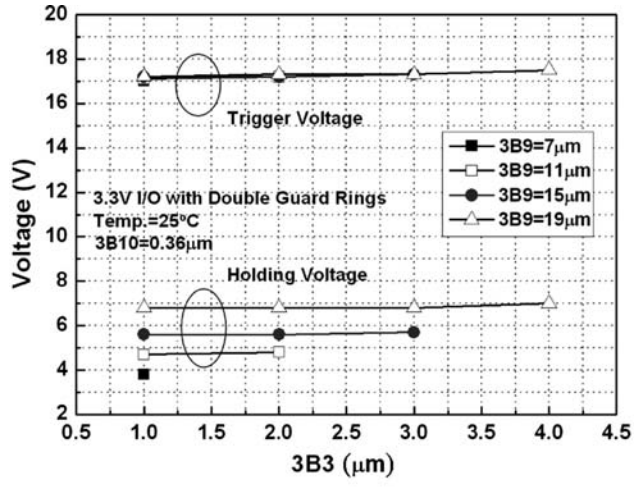
(a)



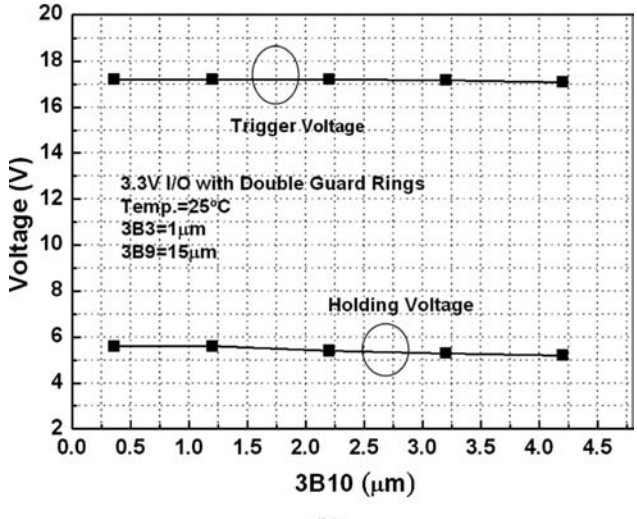
(b)

Figure A.4 Latchup trigger and holding voltage dependencies on (a) 3A3 and 3A9, and (b) 3A10, for 1.8 V devices.

guard ring. To save more layout area in the I/O cells, especially in high-pin-count CMOS ICs, I/O cells with a single guard ring are also evaluated for their enhancements on latchup robustness. If the single guard ring is enough to make the I/O cells latchup-free, safe and compact layout rules for the I/O cells can be easily specified. A layout example of an I/O cell with a single guard ring is shown in Figure A.8. The test



(a)

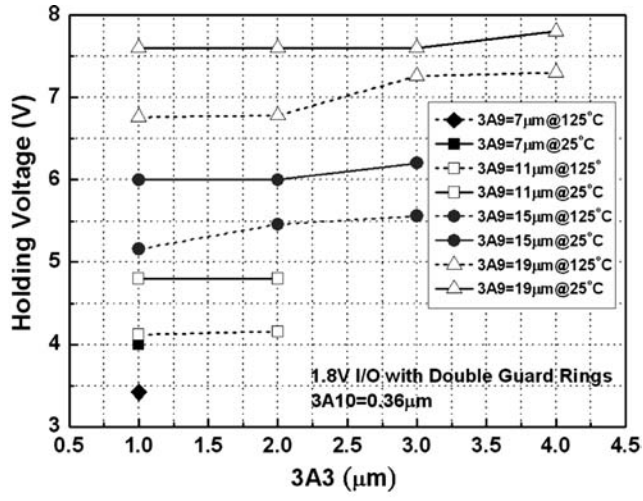


(b)

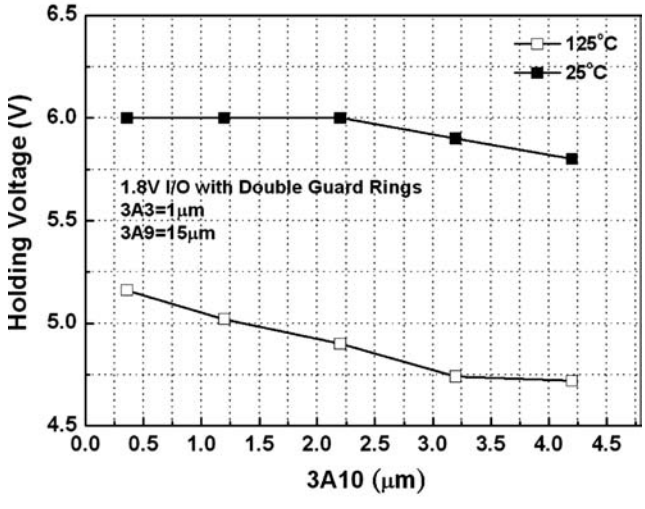
Figure A.5 Latchup trigger and holding voltage dependencies on (a) 3B3 and 3B9, and (b) 3B10, for 3.3 V devices.

structures are the same as those shown in Figure A.2, except that the collector guard rings are removed. For example, the finger width (30 μm), channel length (0.25 μm for 1.8 V devices, and 0.5 μm for 3.3 V devices), and channel width (420 μm) in PMOS/NMOS are all the same as those shown in Figure A.2.

The splits of the layout parameters to evaluate the latchup immunity dependencies on anode-to-cathode spacing (3A9 and 3B9) and base guard ring width (3A3, 3A4,



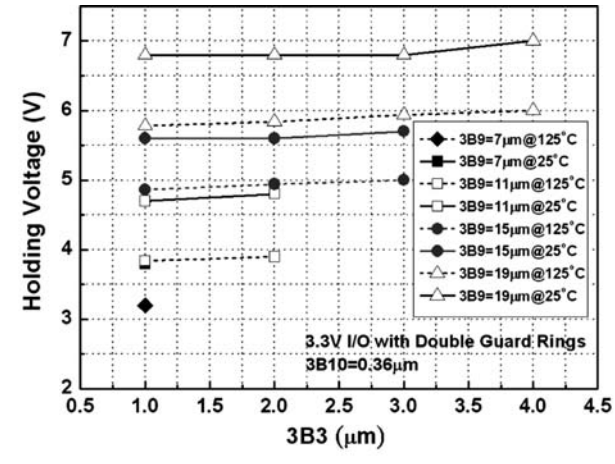
(a)



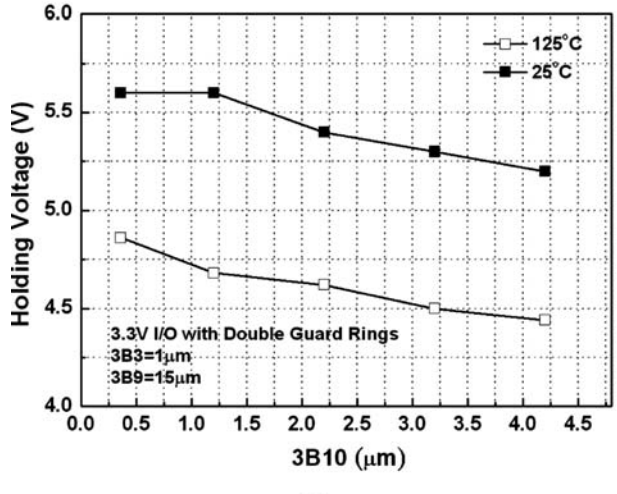
(b)

Figure A.6 Latchup holding voltage dependencies on (a) 3A3 and 3A9, and (b) 3A10, for 1.8 V devices under different test temperatures.

3B3, and 3B4) are listed in Table A.3. Compared with the layout splits listed in Table A.1, the anode-to-cathode spacing is drawn with the smaller values, ranging from 4.5 μm to 10.5 μm. As a result, the purpose of saving layout area in I/O cells could be fulfilled. Also, for a given anode-to-cathode spacing, the base guard ring width is also drawn as compact as possible to achieve the best latchup robustness.



(a)



(b)

Figure A.7 Latchup holding voltage dependencies on (a) 3B3 and 3B9, and (b) 3B10, for 3.3 V devices under different test temperatures.

A.1.3.2 Latchup Immunity Dependency of I/O Cells with a Single Guard Ring

The JEDEC latchup test is performed at first to evaluate the latchup robustness of I/O cells with a single guard ring. The related experimental results are summarized in Table A.4. It was found that a single guard ring is enough to help all structures pass the JEDEC specifications under a room temperature of 25 °C. In fact, these test structures can even sustain a large trigger current of up to ±400 mA without latchup being initiated, regardless of 1.8 V or 3.3 V devices. Due to the resulting latchup-robust

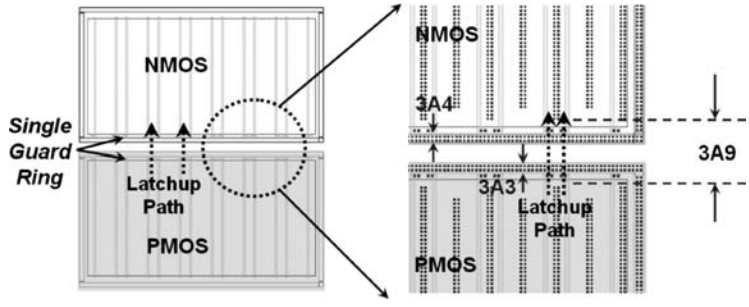


Figure A.8 Layout example of the I/O test structure with a single guard ring.

Table A.3 Splits of layout parameters to evaluate latchup immunity dependencies on anode-to-cathode spacing (3A9 and 3B9) and base guard ring width (3A3, 3A4, 3B3, 3B4) in I/O cells with a single guard ring.

3A9 (3B9)	3A3 = 3A4 (3B3 = 3B4)
4.5 µm	1 µm
6.5 µm	1 µm
	2 µm
8.5 µm	1 µm
	2 µm
	3 µm
10.5 µm	1 µm
	2 µm
	3 µm
	4 µm

Table A.4 Experimental results of the JEDEC latchup test for I/O cells with a single guard ring.

	V_{supply} over-voltage test	*I*-test
Specification requirement	1.5 × maximum V_{supply}	> +/−100 mA
1.8 V I/O (single guard ring)	Pass (> 2.7 V)	Pass (> +/−400 mA)
3.3 V I/O (single guard ring)	Pass (> 5 V)	Pass (> +/−400 mA)

performance in the JEDEC latchup test, it seems that a single guard ring can substitute for double guard rings in I/O cells.

To further ensure whether the I/O cells with a single guard ring could be latchup-free, the holding voltages are extracted and characterized from the latchup DC *I–V* curves. A typical measured latchup *I–V* curve of I/O circuits with a single guard ring is shown in Figure A.9. Both 1.8 V and 3.3 V DUTs have a very small anode-to-cathode spacing (3A9 and 3B9) of 4.5 µm, and a small base guard ring width (3A3

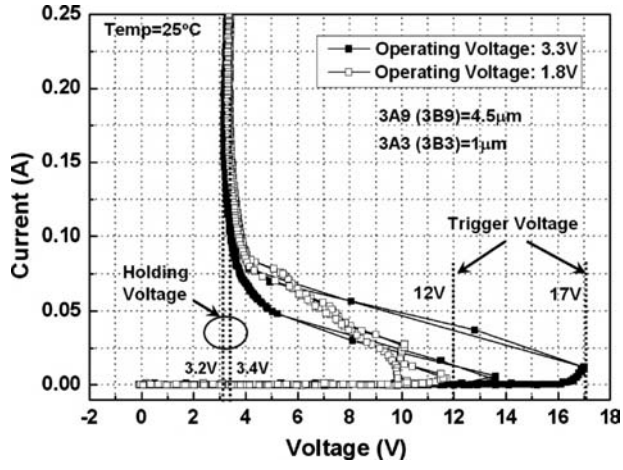


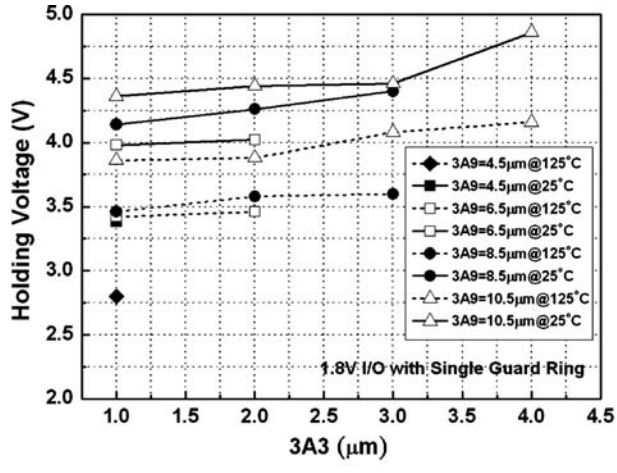
Figure A.9 Typical measured latchup *I–V* curve of I/O circuits with a single guard ring.

and 3B3) of 1 μm. Compared to that in I/O cells with double guard rings, the holding voltage in I/O cells with a single guard ring is smaller. However, it is still large enough (3.4 V) to make 1.8 V I/O cells latchup-free. For a 3.3 V DUT, the holding voltage is 3.2 V, which is very close to the target of 3.3 V. Enlarging the anode-to-cathode spacing (3A9 and 3B9) or the base guard ring width (3A3 and 3B3) can easily raise the holding voltage to be greater than 3.3 V. For the 1.8 V (3.3 V) DUT, the measured latchup holding voltage dependencies on the layout parameters under different test temperatures are shown in Figure A.10a and b. 1.8 V I/O cells are latchup-free (holding voltage > 1.8 V) for all the layout splits listed in Table A.3, even in the worst cases of 3A9 of 4.5 μm, 3A3 of 1 μm, and a test temperature of 125 °C. 3.3 V I/O cells, however, at least need 3A9 of 10.5 μm and 3A3 of 1 μm to achieve latchup-free.

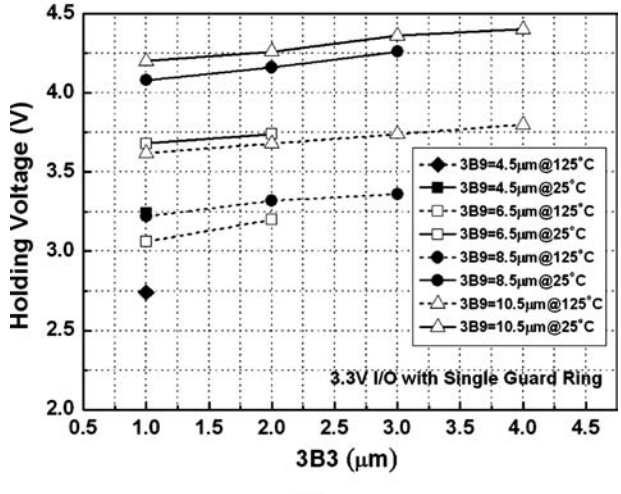
A.1.4 Suggested Layout Rules for I/O Cells

From the above measured results, the suggested latchup-preventing layout rules in I/O cells can be properly defined. The detailed layout guidelines are referred to in Section A.5, *Suggested Layout Guidelines.*

For 1.8 V I/O cells, a single guard ring is enough to provide good latchup robustness, even at high test temperatures. Thus, both the NMOS and PMOS in the I/O cells should be at least surrounded by base guard rings, but the use of collector guard rings could be optional. To make sure the I/O cells are certainly latchup-free, the minimum spacing between the source regions of the NMOS and PMOS (3A9) can be defined as 7 μm, and the minimum width of the base guard ring (3A3 and 3A4) can be defined as 1 μm. For 3.3 V I/O cells, due to its higher target holding voltage of 3.3 V to be latchup-free,



(a)



(b)

Figure A.10 For (a) 1.8 V, and (b) 3.3 V I/O cells, the measured latchup holding voltage dependencies on layout parameters under different test temperatures.

double guard rings would better be added in the I/O cells. Thus, 3B9 can be defined as 7 μm, 3B3 (=3B4 = 3B7 = 3B8) can be defined as 1 μm, and 3B10 can be defined as 4 μm to ensure a latchup-free I/O cell. In addition, for two adjacent PMOS (NMOS), the N+ (P+) base guard rings can be merged to have a compact layout. As the design rule of 3A11 (3A12) shown in Figure A.11, the minimum spacing between two adjacent P+ (N+) base guard rings of the I/O driver could be 0 μm to save the I/O layout area.

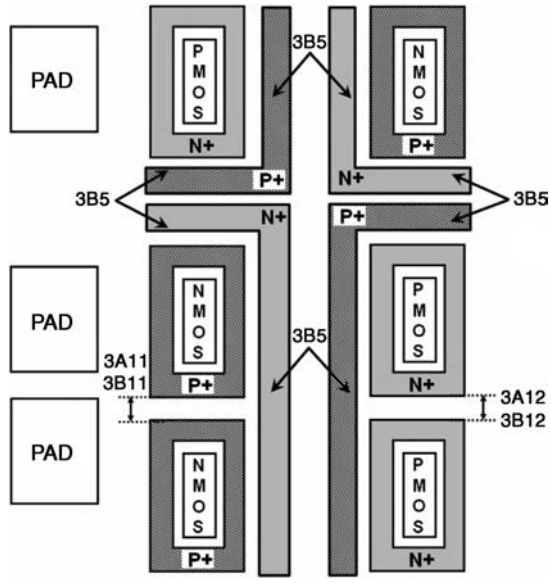


Figure A.11 For two adjacent I/O PMOSs (NMOSs), the N+ (P+) base guard rings can be merged to save I/O layout area.

A.2 For Internal Circuits

A.2.1 Nomenclature

The nomenclatures representing the latchup layout rules for the internal circuits are listed below, and can be referred to in detail in Figure A.1.

5A1 (5B1): For a 1.8 V (3.3 V) PMOS, the maximum distance from any point inside the source/drain region to the nearest N-well pickup in the same N-well.
5A2 (5B2): For a 1.8 V (3.3 V) NMOS, the maximum distance from any point inside the source/drain region to the nearest P-well pickup in the same P-well.

A.2.2 Design of Test Structures

The SCR is used as the test structure to extract the latchup-prevention rules for the internal circuits, as indicated in Chapter 6. The device cross-sectional view and layout top view of the SCR test structure are shown in Figure A.12, and the latchup paths are also indicated. The N+ well pickup connected together with the P+ anode is biased at V_{DD}, while the P+ substrate pickup connected together with the N+ cathode is biased at GND. The P+ (N+) trigger node located in the P-substrate (N-well) region is used to investigate the latchup robustness dependency on the positive (negative) trigger

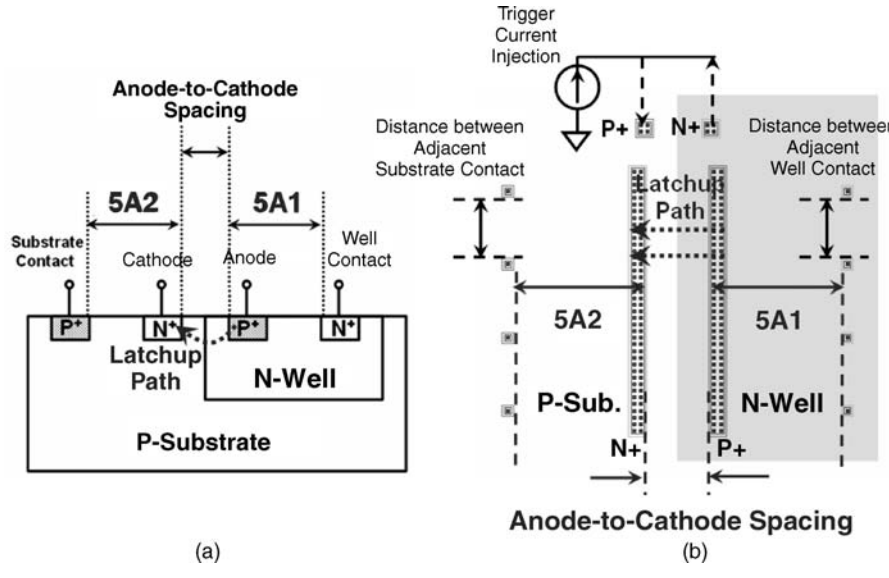


Figure A.12 (a) Device cross-sectional view, and (b) layout top view, of the SCR test structure. The SCR structure is used to extract the latchup-prevention rules for the internal circuits.

current injecting into the P-substrate (N-well). As a result, the threshold trigger current to initiate latchup in the SCR structure can be identified.

The splits of layout parameters to evaluate latchup immunity dependencies on 5A1, 5A2, 5B1, and 5B2, are listed in Table A.5. The distance between adjacent substrate (well) contacts is kept at 5 μm, and an anode-to-cathode spacing ranging from 0.86 μm to 5 μm is also used to consider its impact on latchup robustness. In order to simulate the compact density in the core circuitry of real CMOS chips, the anode-to-cathode spacing drawn in the SCR should avoid too large a distance. For example, the maximum anode-to-cathode spacing is limited as 5 μm in the SCR test structures. In addition, the minimum anode-to-cathode spacing is 0.86 μm, which is used to simulate the minimum allowable spacing between the source regions of the PMOS and NMOS in this given CMOS process. Thus, the most latchup-sensitive case in this given CMOS process can be simulated.

A.2.3 Latchup Immunity Dependency of Internal Circuits

The JEDEC V_{supply} over-voltage test is performed at a room temperature of 25 °C. It was found that SCR structures with all layout splits pass the JEDEC specifications that latchup is not triggered on with 1.5× maximum V_{supply}, regardless of a 1.8 V or 3.3 V SCR. The JEDEC trigger current test, however, is not needed, because the SCR has no I/O pins, but only V_{DD} and GND pins.

Table A.5 Splits of layout parameters to evaluate latchup immunity dependencies on 5A1, 5A2, 5B1, and 5B2, in SCR test structures.

Distance between adjacent substrate (well) contact: 5 μm	
5A1 = 5A2 (5B1 = 5B2)	Anode-to-cathode spacing
10 μm	0.86 μm
	1.5 μm
	3 μm
	5 μm
20 μm	0.86 μm
	1.5 μm
	3 μm
	5 μm
30 μm	0.86 μm
	1.5 μm
	3 μm
	5 μm
40 μm	0.86 μm
	1.5 μm
	3 μm
	5 μm

It seems that SCR structures with all layout splits are robust enough against latchup. However, they could still probably suffer latchup under an even higher trigger voltage on the V_{DD} pins, unless their holding voltages can be identified as latchup-free holding voltages, that is, the holding voltage is greater than V_{DD}. The measured latchup *I–V* curves of a 1.8 V SCR with two different layout splits are shown in Figure A.13. Obviously, even with the anode-to-cathode spacing increasing up to 5 μm, and the 5A1 (5A2) decreasing down to 10 μm, the holding voltage is still a very small value of 1.2 V. Such a small holding voltage is almost the same as that in the worst case of layout splits, where the anode-to-cathode spacing (5A1 and 5A2) is 0.86 μm (40 μm). Thus, it seems that the internal circuits are impossible to be latchup-free due to the lack of protection of the guard rings. To confirm this point, the latchup trigger and holding voltage dependencies on layout splits for a 1.8 V and 3.3 V SCR are shown in Figure A.14a and b, respectively. From the measured results, only the trigger voltages have more obvious variations under different layout splits. The holding voltages, however, are almost independent of layout variations and are kept at ∼1.2 V, which is much smaller than the target latchup-free holding voltages of 1.8 V or 3.3 V. This means that inevitably the internal circuits could still suffer latchup. As a result, the other worse cases of latchup immunity dependencies under high test temperatures and trigger currents injecting into the trigger nodes are not shown here.

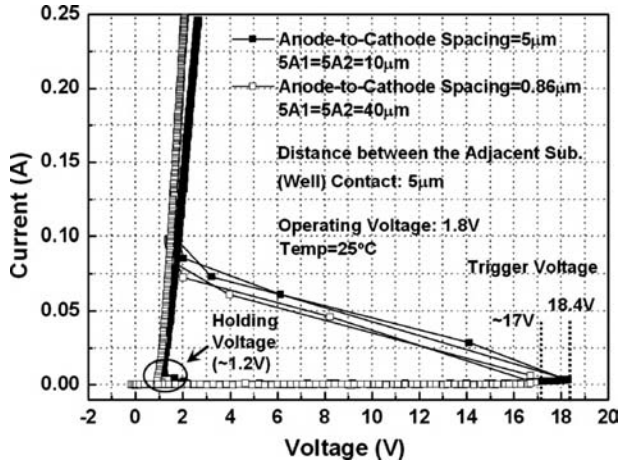


Figure A.13 Measured latchup *I–V* curves of a 1.8 V SCR with two different layout splits.

A.2.4 Suggested Layout Rules for Internal Circuits

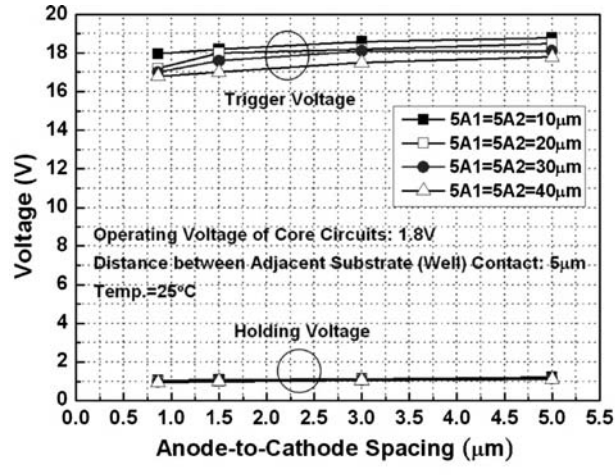
Without the protection of guard rings, it was clarified that the holding voltages of the SCR are kept at only ~1.2 V and almost independent on layout variations, even though all the SCR test structures passed the JEDEC specifications. Thus, the latchup-prevention rules in internal circuits cannot be determined according to the magnitude of the holding voltage. Instead, the 5A1, 5A2, 5B1, and 5B2 are empirically specified as a proper spacing of 30 μm. If we use 5A1 with 30 μm, in most field applications, latchup will not occur in the internal circuits of the ICs. This result has been empirically verified in many field applications. This empirical data has been proven in field applications that most latchup issues in the internal circuits can be prevented. In addition, it is suggested that as many N-well or P-well pickups as possible are placed in the layout. The detailed layout guidelines are referred to in Section A.5, *Suggested Layout Guidelines.*

A.3 For between I/O and Internal Circuits

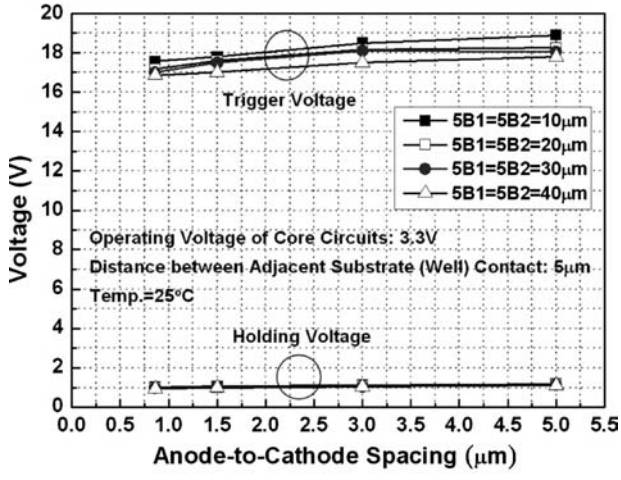
A.3.1 Nomenclature

The nomenclatures representing the latchup layout rules for between I/O and the internal circuits are listed below, and can be referred to in detail in Figure A.1.

4A1 (4B1): Minimum spacing between 3.3 V I/O Cells and 1.8 V (3.3 V) internal circuits.
4A3 (4B3): Minimum width of additional guard ring located between 3.3 V I/O Cells and 1.8 V (3.3 V) internal circuits
4A4 (4B4): Maximum spacing from the inserted additional guard ring to 3.3 V I/O Cells.



(a)



(b)

Figure A.14 For (a) 1.8 V, and (b) 3.3 V SCRs, the measured latchup trigger and holding voltage dependencies on anode-to-cathode spacing under different 5A1, 5B1, 5A2, and 5B2.

A.3.2 I/O and Internal Circuits (SCR)

A.3.2.1 Design of Test Structures

In CMOS ICs, internal circuits can be triggered on to a latchup state due to noise current injection at the I/O pins. To further enhance the latchup robustness of the internal circuits, latchup-prevention layout rules between I/O and the internal circuits should be specified, as presented in Chapter 6. A layout example of a test structure to

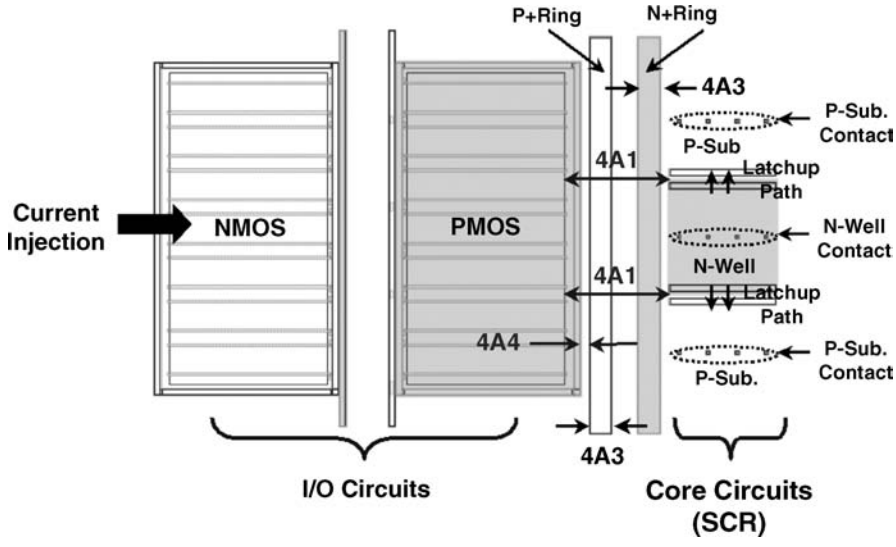


Figure A.15 Layout example of a test structure to evaluate the latchup layout rules between I/O and the internal circuits (SCR).

evaluate the latchup layout rules between I/O and the internal circuits (SCR) is shown in Figure A.15. Both the PMOS and NMOS in the I/O cells are drawn in the multiple-finger style with a fixed length of 30 μm per finger. The channel length of the PMOS and NMOS is the same, 0.5 μm, for the 3.3 V I/O, and the total channel width is the same, 420 μm, for both the PMOS and NMOS. To ensure a robust latchup immunity in I/O cells, double guard rings are added to the I/O cells where 3A9 = 15 μm, 3A10 0.36 μm, and 3A3 = 3A4 = 3A7 = 3A8 = 1 μm. These I/O cells are already confirmed in advance that their holding voltages are higher than V_{DD} (3.3 V), that is, latchup-free. Thus, it is sure that the noise current injecting into the I/O pins never triggers on latchup in the I/O cells, but could only do so in the internal circuits. The SCR, which is planned to parallel the I/O cells, is used to simulate the practical internal circuits. This has an anode-to-cathode spacing of 1.5 μm, a distance between the adjacent substrate (well) contacts of 5 μm, and a 5A1 of 10 μm for both 1.8 V and 3.3 V SCRs. Only two combinations – a 3.3 V I/O and a 1.8 V SCR, as well as a 3.3 V I/O and a 3.3 V SCR – are planned in the test structures, because the combination of a 1.8 V I/O and 1.8 V internal circuits is rare in real CMOS chips.

The splits of layout parameters to evaluate the latchup immunity dependencies on 4A1 and 4A3 (4B1 and 4B3) are listed in Table A.6a, and the splits of the layout parameters to evaluate the latchup immunity dependencies on 4A4 (4B4) are listed in Table A.6b. For a given spacing between I/O and the internal circuits (4A1 and 4B1), the inserted guard rings should be drawn as compact as possible to achieve the best latchup robustness of the internal circuits. For example, for a given spacing between

Table A.6a Splits of layout parameters to evaluate latchup immunity dependencies on 4A1 and 4A3 (4B1 and 4B3).

4A4 (4B4)=2 μm	
4A1 (4B1)	4A3 (4B3)
20 μm	2 μm
	4 μm
	6 μm
35 μm	6 μm
	10 μm
	13 μm
50 μm	10 μm
	15 μm
	20 μm

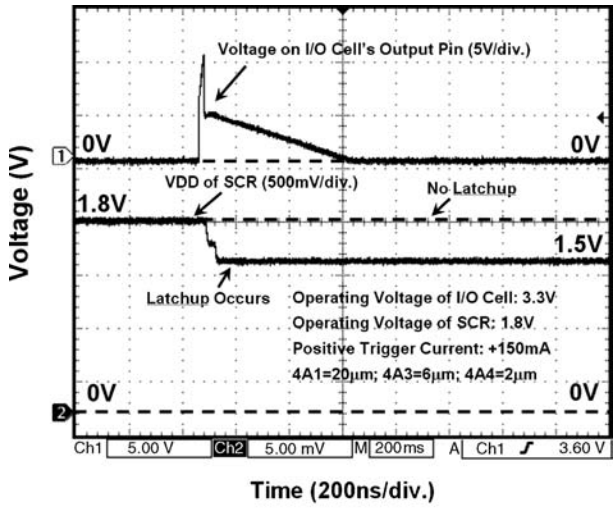
Table A.6b Splits of layout parameters to evaluate latchup immunity dependencies on 4A4 (4B4).

4A1 (4B1) = 20 μm	4A3 (4B3) = 2 μm
4A4 (4B4)	2 μm
	4 μm
	6 μm

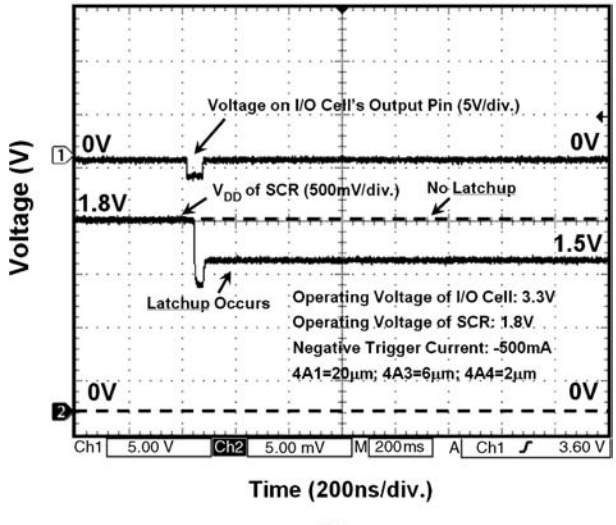
I/O and the internal circuits (4A1 and 4B1) of 20 μm, the maximum inserted guard ring width (4A3 and 4B3) that is allowed to be placed within this specific spacing is 6 μm. Based on such layout plans, safe and compact latchup-preventing layout rules can be extracted.

A.3.2.2 Threshold Trigger Current Dependencies

The JEDEC trigger current test is performed to evaluate the threshold trigger current dependencies on all layout splits. The typical measured transient responses of a test structure (3.3 V I/O and 1.8 V SCR) in the positive and negative trigger current tests are shown in Figure A.16a and b, respectively. When there is a positive (negative) trigger current injecting into the output pins of the I/O cells, the voltage on the pin under test will increase (decrease) simultaneously. Subsequently, if the V_{DD} of the SCR is pulled down (∼holding voltage) after the voltage on the pin under test returns to its initial DC level, latchup occurs. Otherwise, if the V_{DD} of SCR is not pulled down but always kept at its initial DC level, latchup does not occur. Based on such criteria to judge if latchup occurs in internal circuits (SCR) due to the trigger current injection at the I/O pins of the I/O cells, the threshold trigger current at the I/O pins to fire latchup in the internal



(a)



(b)

Figure A.16 Typical measured transient responses of a test structure (3.3 V I/O and 1.8 V SCR) under JEDEC (a) positive, and (b) negative, trigger current tests.

circuits can be found. Thus, proper latchup-prevention layout rules between I/O and the internal circuits can be determined.

For test structures with a 3.3 V I/O and a 1.8 V SCR, the positive and negative triggering current dependencies on all layout splits are shown in Figure A.17. Enlarging the spacing between I/O and the internal circuits (4A1) and the inserted

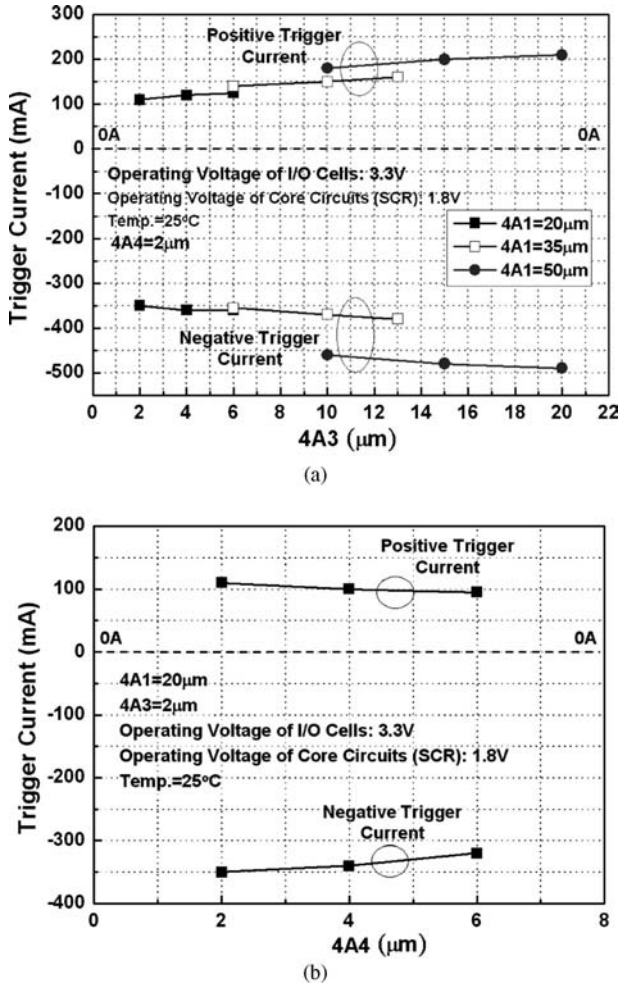


Figure A.17 Positive and negative triggering current dependencies on (a) 4A1 and 4A3, and (b) 4A4, for test structures with a 3.3 V I/O and a 1.8 V SCR.

guard ring width (4A3) can enhance the latchup robustness of the internal circuits. For example, if 4A1 (4A3) is only 20 μm (2 μm), the positive trigger current is only $+110$ mA, which only just meet the JEDEC specification ($> +100$ mA). If 4A1 (4A3) increases up to 50 μm (20 μm), almost a double positive trigger current of $+210$ mA and a very high negative trigger current of -490 mA can be achieved, as shown in Figure A.17a. Additionally, increasing the spacing from the inserted guard ring to I/O (4A4) will slightly degrade the latchup immunity in the internal circuits. As shown in Figure A.17b, increasing 4A4 from 2 μm to 6 μm will lead the positive (negative) trigger current to decrease from $+110$ mA (-350 mA)

down to $+90$ mA (-320 mA). From the comprehensive measured results shown in Figure A.17a and b, the dominant layout rules to develop latchup-robust internal circuits is to enlarge the spacing between I/O and the internal circuits, to insert additional double guard rings between I/O and the internal circuits, and to draw these double guard rings as wide as possible.

Similar positive and negative trigger current dependencies can be observed in test structures with a 3.3 V I/O and a 3.3 V SCR, as shown in Figure A.18. Compared with

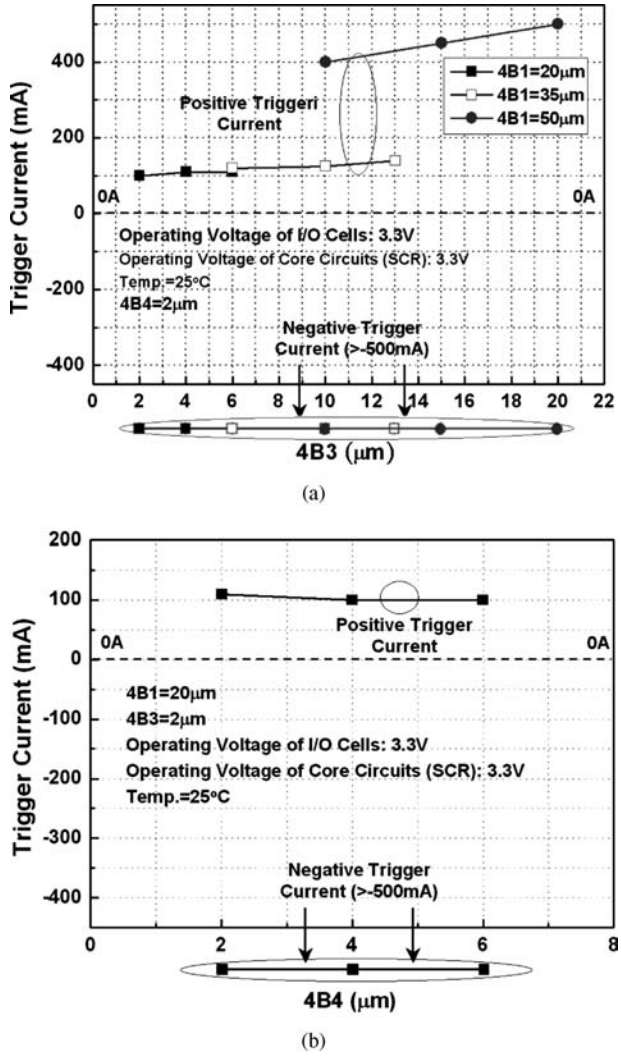


Figure A.18 Positive and negative triggering current dependencies on (a) 4B1 and 4B3, and (b) 4B4, for test structures with a 3.3 V I/O and a 3.3 V SCR.

the test structures with a 3.3 V I/O and a 1.8 V SCR, an obvious difference is that there is a much higher positive trigger current ($> +400$ mA) for 4B1 = 50 µm, and a much higher negative trigger current (> -500 mA) for all layout splits. As a result, the spacing between I/O and the internal circuits (4B1), as well as the inserted guard ring width (4B3), can be smaller to save layout area in CMOS chips with a 3.3 V I/O and 3.3 V internal circuits.

A.3.3 I/O and the Internal Circuits (Ring Oscillator)

A.3.3.1 Design of Test Structures

In order to make test structures approach real situations in CMOS chips, the ring oscillator can be used to substitute for the SCR as real circuit verifications. A layout example of a test structure to evaluate the latchup layout rules between I/O and the internal circuits (ring oscillator) is shown in Figure A.19. The I/O cells are the same as those shown in Figure A.15. The 1.8 V (3.3 V) ring oscillators are designed with an oscillating frequency of 80 MHz, consisting of 197-stage (101-stage) inverter chains. The PMOS (NMOS) in each inverter has dimension (*W*/*L*) of 0.44 µm/0.18 µm (0.22 µm/0.18 µm) for a 1.8 V ring oscillator, and 0.9 µm/0.4 µm (0.45 µm/0.4 µm) for a 3.3 V ring oscillator. The parasitic SCR path existing in the ring oscillator goes through from the P+ source of the PMOS, N-well, P-substrate, to the N+ source of the NMOS. The parasitic SCR has an anode-to-cathode spacing of 0.86 µm, a distance between the adjacent substrate (well) contacts of 5 µm, and a 5A1 (5A2) of 4.5 µm. Only two combinations – a 3.3 V I/O and a 1.8 V ring oscillator, as well as a 3.3 V I/O

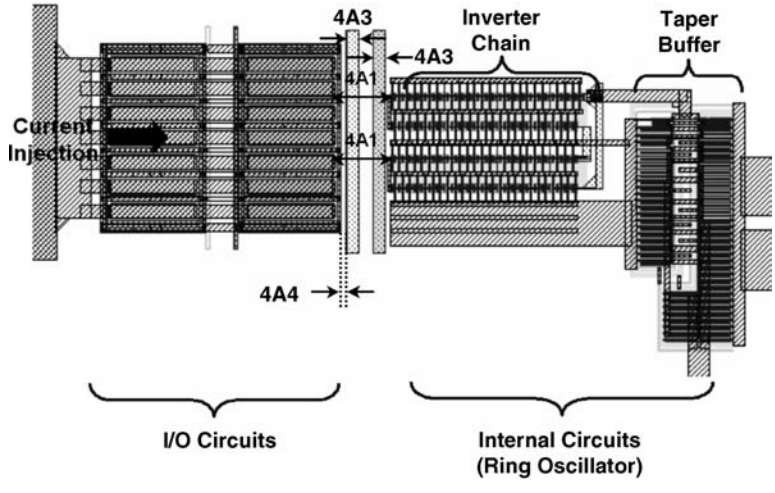


Figure A.19 Layout example of a test structure to evaluate the latchup layout rules between I/O and the internal circuits (ring oscillator).

and a 3.3 V ring oscillator – are planned in the test structures. In addition, all the layout splits are the same as those in the test structures with an SCR as their internal circuits, as shown in Table A.6.

A.3.3.2 Threshold Trigger Current Dependencies

The JEDEC trigger current test is performed to find the threshold trigger current at the I/O pins to fire latchup in the internal circuits (ring oscillator). The measured transient responses in the positive trigger current test are shown in Figure A.20. After a positive trigger current injecting into the output pins of the I/O cells, obviously latchup occurs because the V_{DD} of the ring oscillator is pulled down to the holding voltage of ~1.5 V. Furthermore, the output voltage of the ring oscillator fails to function correctly (80 MHz voltage clock), but is pulled down to 0 V instead.

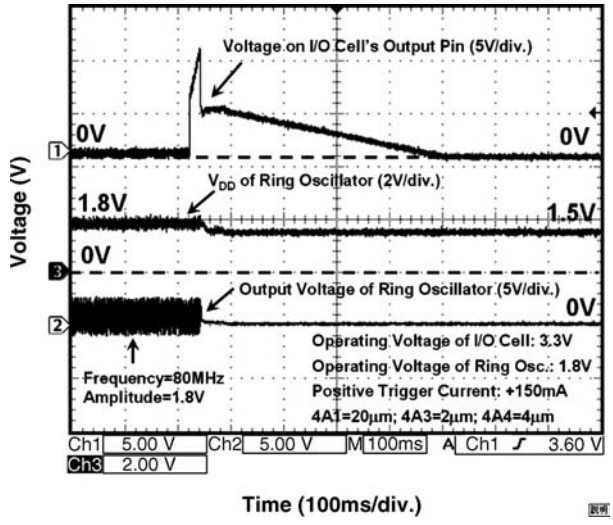


Figure A.20 For a ring oscillator as the internal circuits, the measured transient responses of the test structure in the JEDEC positive trigger current test.

For test structures with a 3.3 V I/O and a 1.8 V (3.3 V) ring oscillator, the positive and negative triggering current dependencies on all layout splits are shown in Figures A.21 and A.22. Similar triggering current dependencies can be observed to those shown in Figures A.17 and A.18. For example, enlarging the spacing between I/O and the internal circuits (4A1 and 4B1) and the inserted guard ring width (4A3 and 4B3) can efficiently enhance the latchup robustness of the ring oscillator, but increasing the spacing from the inserted guard ring to I/O (4A4 and 4B4) will slightly

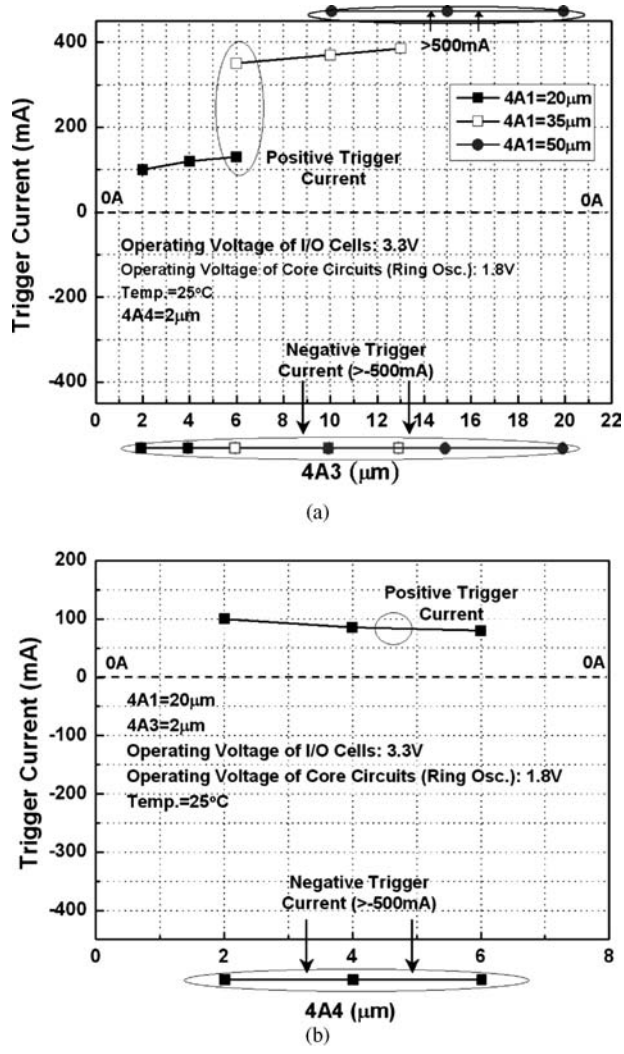


Figure A.21 Positive and negative triggering current dependencies on (a) 4A1 and 4A3, and (b) 4A4, for test structures with a 3.3 V I/O and a 1.8 V ring oscillator.

degrade the latchup immunity in the ring oscillator, regardless of whether it is a 1.8 Vor 3.3 V ring oscillator.

A.3.4 Suggested Layout Rules for between I/O and the Internal Circuits

From the above measured results shown in Figures A.17, A.18, A.21 and A.22, the suggested latchup-prevention layout rules for between I/O and the internal circuits

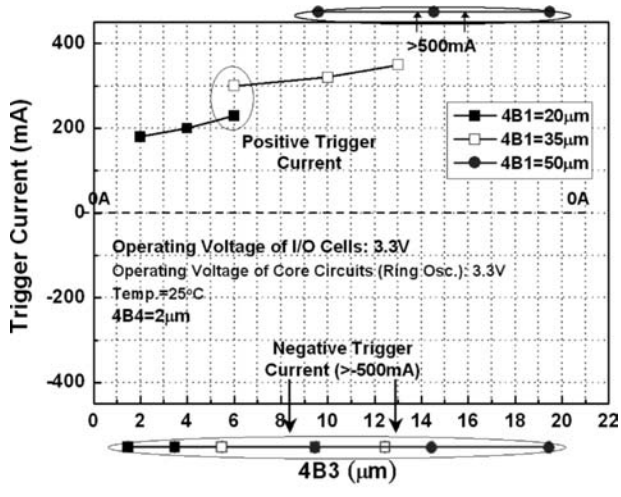


Figure A.22 Positive and negative triggering current dependencies on (a) 4B1 and 4B3, and (b) 4B4, for test structures with a 3.3 V I/O and a 3.3 V ring oscillator.

can be properly defined. The detailed layout guidelines can be referred to in Section A.5, *Suggested Layout Guidelines*.

The target value of the trigger current is set as ± 200 mA. This target value is double that in the JEDEC latchup specification (± 100 mA), and so any DUT that can sustain a ± 200 mA trigger current without latchup happening should be robust enough against latchup. The measured results show that a large 4A1 of 50 μm is necessary to make the positive trigger current higher than $+200$ mA, as shown in Figure A.17. With such

a large 4A1 of 50 μm, 4A3 is not so critical and can be chosen as a small value of 5 μm. Thus, two dominant parameters to enhance the latchup immunity of internal circuits – minimum spacing between I/O and the internal circuits (4A1 and 4B1), and a minimum inserted guard ring width (4A3 and 4B3) – can be defined as 50 μm and 5 μm, respectively. Generally, I/O cells are usually composed of a driver and a pre-driver. Because the pre-driver is not directly connected to the I/O pads and is thus not a dominant noise injecting source, the layout rules for 4A1 and 4B1 should be the minimum spacing from the I/O driver, but not the pre-driver, to the internal circuits, as shown in Figure A.23. In addition, because the spacing from the inserted guard rings to I/O (4A4 and 4B4) is not a critical parameter to affect latchup robustness, a proper 4A4 of 5 μm for 1.8 V internal circuits, and 4B4 of 10 μm for 3.3 V internal circuits are chosen. Compared with 4A4, a larger 4B4 is mainly due to the considerations of better latchup immunity in 3.3 V internal circuits, as shown in Figures A.18 and A.22.

A.4 For Circuits across Two Different Power Domains

A.4.1 Nomenclature

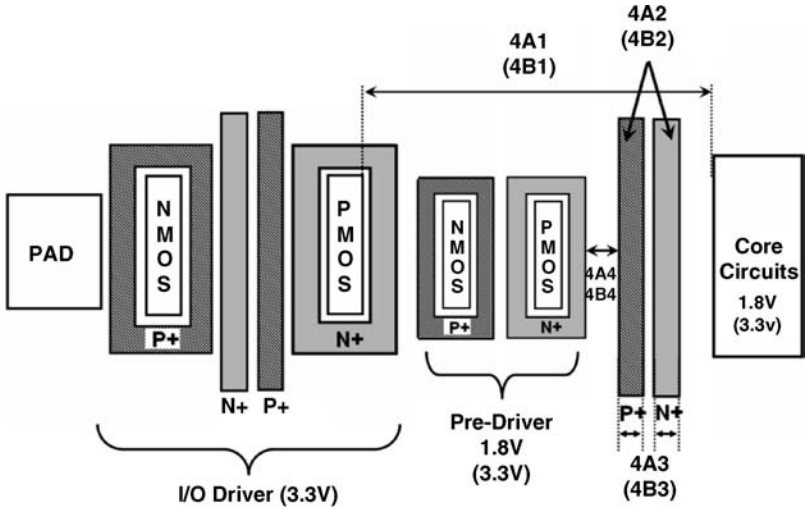
The nomenclatures representing the latchup layout rules for different power-domain applications are listed below, and can be referred to in detail in Figure A.24.

6A: Minimum spacing between P+ diffusions powered by 3.3 V in the N-well, and N+ diffusions powered by 1.8 V in the N-well.
6C: Minimum width of a P+ inserted guard ring located between the P+ diffusions powered by 3.3 V in the N-well, and the N+ diffusions powered by 1.8 V in the N-well.
6D: Minimum width of the N+ base guard ring for a 1.8 V device.
6E: Minimum width of the N+ base guard ring for a 3.3 V device.

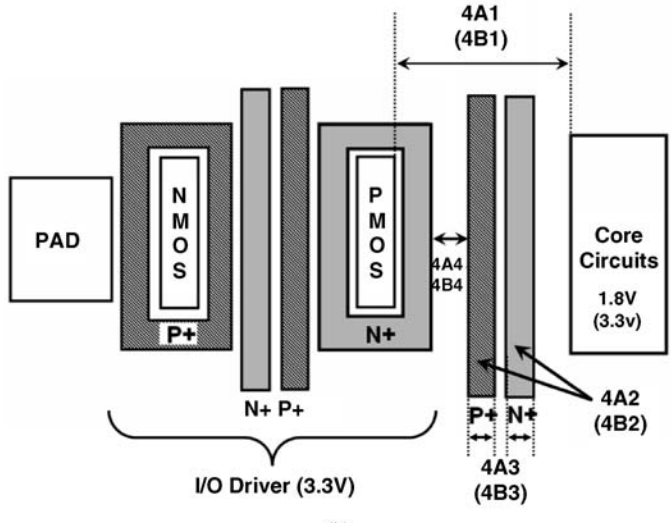
A.4.2 Design of Test Structures

For mixed-voltage CMOS ICs, power-supply voltages with different magnitudes can coexist in a single CMOS chip. Thus, latchup issues potentially exist between the two different power domains, as shown in Figure A.24. Unlike the conventional latchup path going through from V_{DD} (P+ source of the PMOS) to GND (the N+ source of the NMOS), such specific latchup path goes through from $V_{DD,H}$ of 3.3 V (P+ source of the PMOS) to $V_{DD,L}$ of 1.8 V (N+ well contact). When latchup is initiated between the two different power domains, a huge latchup current will conduct through from $V_{DD,H}$ to $V_{DD,L}$, leading to temporary malfunction or permanent damage in the CMOS ICs. Therefore, in order to avoid such a latchup issue, latchup design rules between two different power domains should be extracted.

The SCR with a butted (non-butted) 3.3 V N-well contact is used as the test structure to extract the latchup-prevention rules between the two different power domains,



(a)



(b)

Figure A.23 (a) Pre-driver is located between the I/O driver and the core circuits. (b) Pre-driver is not located between the I/O driver and the core circuits. The layout rules 4A1 and 4B1 should be the minimum spacing from the I/O driver, but not pre-driver, to the internal circuits.

as shown in Figure A.25a and b. To simulate this specific latchup path between the two different power domains in Figure A.24, the SCR has the P+ anode connected to 3.3 V, and the N+ cathode connected to 1.8 V. The P+ anode is used to simulate the P+ source of the PMOS, whereas the N+ cathode is used to simulate N+ well

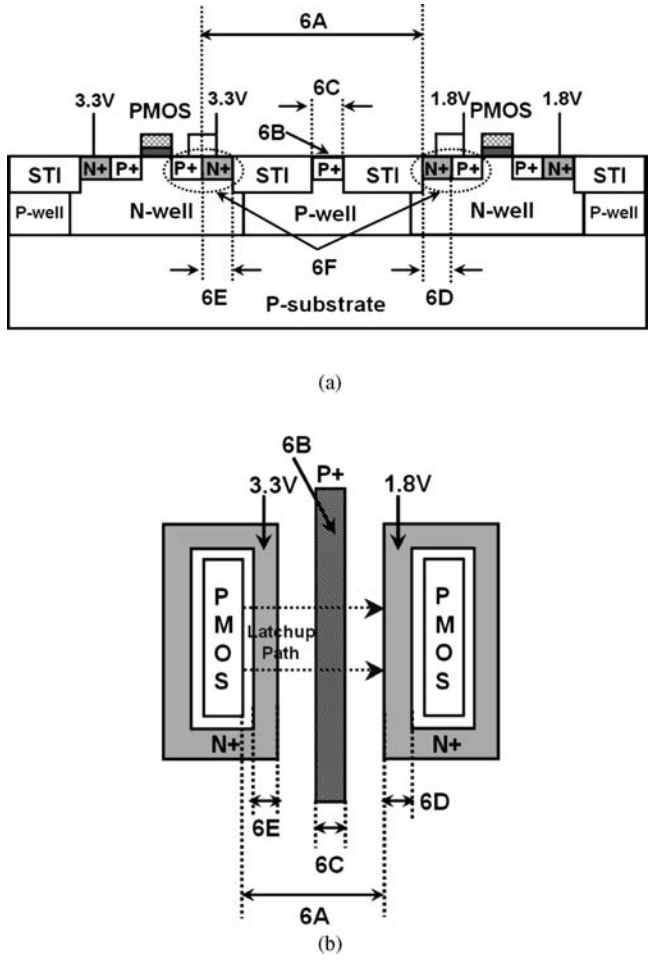
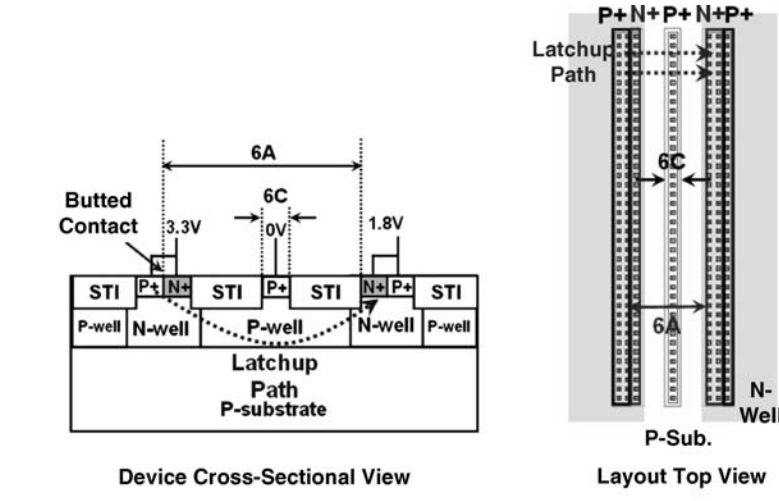
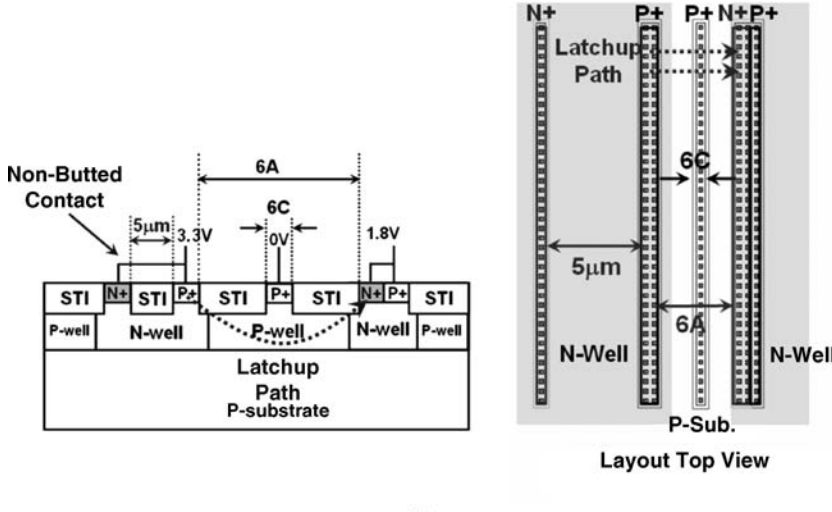


Figure A.24 (a) Device cross-sectional view, and (b) layout top view, to illustrate the layout rules for latchup prevention between the two different power domains.

contact. To further enhance the latchup immunity between the two different power domains, the inserted P+ guard ring connected to GND can be placed in the P-well, which is located between the 3.3 V N-well and the 1.8 V N-well. The SCR with a butted 3.3 V N-well contact is used to simulate the real situation that the PMOS has a butted contact, as shown in Figure A.25a. The SCR with non-butted 3.3 V N-well contact is used to simulate the real situation that the PMOS has a non-butted contact, as shown in Figure A.25b. Obviously, the SCR with a non-butted 3.3 V N-well contact is more susceptible to latchup, because the well resistance of the parasitic vertical BJT will be larger, leading latchup to be initiated more easily.



(a)



(b)

Figure A.25 An SCR with (a) butted, and (b) non-butted 3.3 V N-well contact, to extract the latchup-preventing rules between the two different power domains.

The anode-to-cathode spacing (6A) and the inserted P+ guard ring width (6C) are the two dominant layout parameters for determining the latchup immunity between the two different power domains. The splits of the layout parameters to evaluate the latchup immunity dependencies on 6A and 6C are listed in Table A.7. For the plan of

Table A.7 Splits of layout parameters to evaluate latchup immunity dependencies on 6A and 6C.

6D = 1 μm 6A	6E = 0.5 μm 6C
2.23 μm	0.5 μm
4 μm	0.5 μm
	1 μm
	2 μm
7 μm	1 μm
	2 μm
	3.5 μm
	5 μm
10 μm	2 μm
	4 μm
	6 μm
	8 μm

layout splits, the inserted P+ guard ring (6C) should be drawn as compact as possible within a given anode-to-cathode spacing (6A). As a result, the best latchup robustness under a given anode-to-cathode spacing can be evaluated to extract compact and safe latchup-preventing layout rules between the two different power domains. In addition, the width of the N+ base guard ring is fixed as 1 μm and 0.5 μm for 1.8 V (6D) and 3.3 V (6E) devices, respectively. Such a narrow guard ring width (0.5 μm) in the 3.3 V device is used to minimize the guard ring protection efficiency introduced in Section A.1. Thus, the latchup immunity dependencies on 6A and 6C can be highlighted.

A.4.3 Latchup Immunity Dependency between Two Different Power Domains

To evaluate the latchup robustness dependencies on layout splits, latchup holding voltages are extracted from the latchup DC *I–V* curves of the SCR test structures. The typical measured latchup *I–V* curves of the SCR with butted and non-butted 3.3 V N-well contacts are shown in Figure A.26. The DUT has 6A of 4 μm, and 6C of 0.5 μm. It should be noted that the *X*-axis represents the anode-to-cathode voltage, and the inserted P+ guard ring is biased at −1.8 V during the measurements. As a result, if the holding voltage in the *X*-axis is higher than the difference of the two power-supply voltages ($V_{DD,H}$-$V_{DD,L}$ = 3.3 V–1.8 V) of 1.5 V, it would be latchup-free between the two different power domains. In Figure A.26, both of the SCRs are latchup-free because the holding voltages are higher than 1.5 V, regardless of the SCR with either a butted or non-butted 3.3 V N-well contact. However, compared with the SCR with

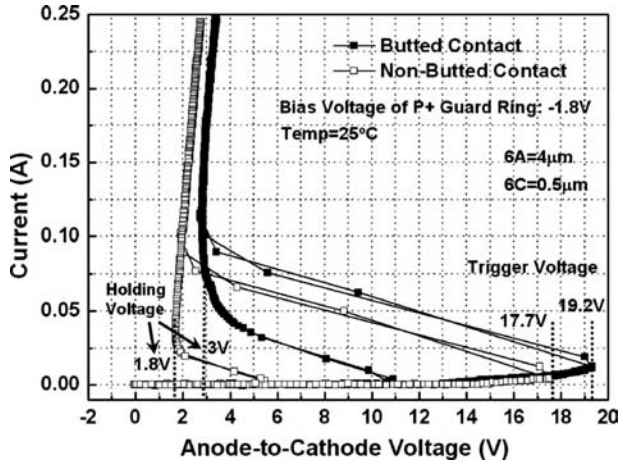


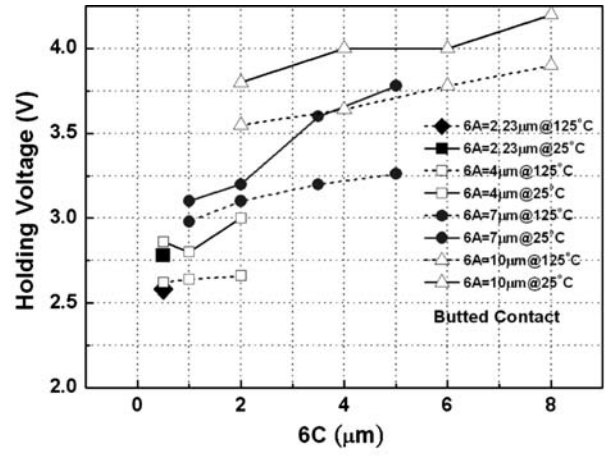
Figure A.26 Measured latchup *I–V* curves of an SCR with a butted and non-butted 3.3 V N-well contact.

a non-butted 3.3 V N-well contact where the holding (trigger) voltage is only 1.8 V (17.7 V), the SCR with a butted 3.3 V N-well contact has a higher holding (trigger) voltage of 3 V (19.2 V). Thus, the SCR with a butted contact should perform better in latchup immunity enhancement.

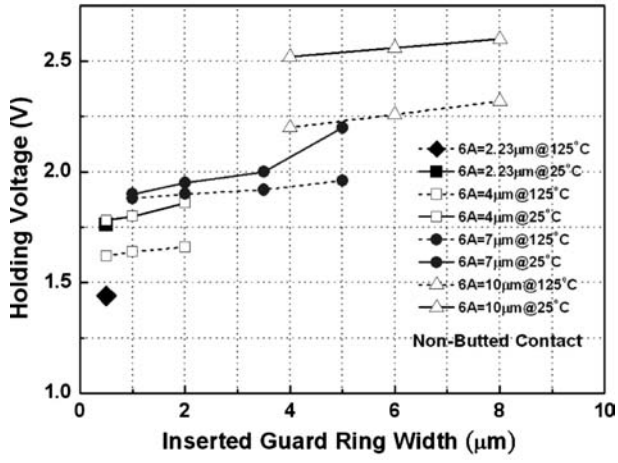
For the SCR with a butted (non-butted) 3.3 V N-well contact, the holding voltage dependencies on 6A and 6C under different test temperatures are shown in Figure A.27a and b. Due to the better latchup robustness in the SCR with the butted contact, the holding voltages for any layout splits are all higher than 2.6 V, even under the worst case that 6A is 2.23 μm, 6C is 0.5 μm, and the test temperature is 125 °C. This means that it would be latchup-free between the two different (3.3 V and 1.8 V) power domains during the normal circuit operating condition. For the SCR with a non-butted contact, however, the holding voltage will be degraded down to only 1.4 V in the worst case. Thus, enlarging 6A or 6C is necessary to enhance the holding voltage greater than the target holding voltage of 1.5 V, as shown in Figure A.27b.

A.4.4 Suggested Layout Rules between Two Different Power Domains

The proper layout rules can be determined upon the magnitudes of the holding voltages in the worse case that the SCR has a non-butted 3.3 V N-well contact and the test temperature is 125 °C, as shown in Figure A.27b. If the holding voltage is higher than 1.5 V (latchup-free), the given layout splits are acceptable. From Figure A.27b, 6A of 4 μm and 6C of 0.5 μm meet this criterion. However, due to the consideration of



(a)



(b)

Figure A.27 For an SCR with (a) butted, and (b) non-butted, 3.3 V N-well contact, the holding voltage dependencies on 6A and 6C under different test temperatures.

the worse case that the distance between two non-butted contacts may be larger than that (5 μm) in Figure A.25b, a larger 6A of 7 μm and 6C of 2 μm are chosen to increase the safe margin. As discussed in Section A.1, the minimum width of the N+ base guard ring for 1.8 V (6D) and 3.3 V (6E) devices should be 1 μm and 2 μm, respectively. Detailed layout guidelines can be referred to in Section A.5, *Suggested Layout Guidelines*.

A.5 Suggested Layout Guidelines

A.5.1 Latchup Design Guidelines for I/O Circuits

A.5.1.1 For 1.8 V I/O Cells

Rule No.	Layout Rule and Layout Suggestion (Figures A.1 and A.11)
3A1	Base guard ring of each NMOS (PMOS) must be directly tied to GND (VDD of 1.8 V) through metal line.
3A2	Both NMOS and PMOS should be surrounded by base guard rings.
3A3	Minimum width of N+ base guard ring for PMOS is 1 μm.
3A4	Minimum width of P+ base guard ring for NMOS is 1 μm.
3A9	Minimum spacing between the source regions of NMOS and PMOS is 9 μm.
3A11	Minimum spacing between two adjacent P+ base guard rings of I/O driver is 0 μm. For two adjacent NMOS, the P+ base guard rings can be merged to have compact layout.
3A12	Minimum spacing between two adjacent N+ base guard rings of I/O driver is 0 μm. For two adjacent PMOS, the N+ base guard rings can be merged to have compact layout.

*Base guard ring is enough to make 1.8-V devices latchup-free (holding voltage > VDD of 1.8 V). Collector guard ring is optional for better latchup robustness, but it will occupy more layout area.

A.5.1.2 For 3.3 V I/O Cells

Rule number	Layout rule and layout suggestion (Figures A.1 and A.11)
3B1	The base guard ring of each NMOS (PMOS) must be directly tied to GND (V_{DD} of 3.3 V) through a metal line
3B2	Both the NMOS and PMOS should be surrounded by base guard rings
3B3	Minimum width of the N+ base guard ring for the PMOS is 2 μm
3B4	Minimum width of the P+ base guard ring for the NMOS is 2 μm
3B5	For two adjacent NMOS and PMOS, collector guard rings should be inserted between the NMOS and PMOS
3B6	The collector guard ring of each NMOS (PMOS) must be directly tied to V_{DD} of 3.3 V (GND) through a metal line
3B7	The minimum width of the P+ collector guard ring for the PMOS is 2 μm
3B8	The minimum width of the N+ (with N-well) collector guard ring for the NMOS is 2 μm
3B9	The minimum spacing between the source regions of the NMOS and PMOS is 11 μm
3B10	The maximum spacing between the base guard ring and collector guard ring is 4 μm
3B11	The minimum spacing between the two adjacent P+ base guard rings of the I/O driver is 0 μm. For two adjacent NMOSs, the P+ base guard rings can be merged to have a compact layout
3B12	The minimum spacing between two adjacent N+ base guard rings of the I/O driver is 0 μm. For two adjacent PMOSs, the N+ base guard rings can be merged to have a compact layout

A.5.2 Latchup Design Guidelines for between I/O and the Internal Circuits

A.5.2.1 For between a 3.3 V I/O and 1.8 V Internal Circuits

Rule number	Layout rule and layout suggestion (Figure A.1)
4A1	The minimum spacing between the source regions of I/O and the internal circuits is 50 μm
4A2	Additional double guard rings must be inserted between I/O and the internal circuits
4A3	The minimum width of the additional guard ring located between I/O and the internal circuits is 5 μm
4A4	The maximum spacing from the inserted additional guard ring to the I/O cells is 5 μm
4A5	The V_{DD} (GND) metal line of the I/O cells should be separated from the V_{DD} (GND) metal line that is directly connected to the inserted additional guard rings
4A6	If the additional double guard rings are not inserted between the I/O driver and the core circuits, the minimum spacing between the source regions of the I/O driver and the core circuits (4A1) is 100 μm. In addition, as many substrate/well pickups or guard rings as possible should be placed in the core circuits

A.5.2.2 For between a 3.3 V I/O and 3.3 V Internal Circuits

Rule number	Layout rule and layout suggestion (Figure A.1)
4B1	The minimum spacing between the source regions of I/O and the internal circuits is 50 μm
4B2	Additional double guard rings must be inserted between I/O and the internal circuits
4B3	The minimum width of the additional guard ring located between I/O and the internal circuits is 5 μm
4B4	The maximum spacing from the inserted additional guard ring to the I/O cells is 10 μm
4B5	The V_{DD} (GND) metal line of the I/O cells should be separated from the V_{DD} (GND) metal line that is directly connected to the inserted additional guard rings
4B6	If the additional double guard rings are not inserted between the I/O driver and the core circuits, the minimum spacing between the source regions of the I/O driver and the core circuits (4B1) is 100 μm. In addition, as many substrate/well pickups or guard rings as possible should be placed in the core circuits

A.5.3 Latchup Design Guidelines for Internal Circuits

A.5.3.1 For 1.8 V Internal Circuits

Rule number	Layout rule and layout suggestion (Figure A.1)
5A1	The maximum distance from any point inside the P+ source/drain region to the nearest N-well pickup in the same N-well is 30 μm
5A2	The maximum distance from any point inside the N+ source/drain region to the nearest P-well pickup in the same P-well is 30 μm
5A3	It is suggested that the number of N-well or P-well pickups should be as many as possible in the layout

A.5.3.2 For 3.3 V Internal Circuits

Rule number	Layout rule and layout suggestion (Figure A.1)
5B1	The maximum distance from any point inside the P+ source/drain region to the nearest N-well pickup in the same N-well is 30 μm
5B2	The maximum distance from any point inside the N+ source/drain region to the nearest P-well pickup in the same P-well is 30 μm
5B3	It is suggested that the number of N-well or P-well pickups should be as many as possible in the layout

A.5.4 Latchup Design Guidelines for Circuits across Two Different Power Domains

Rule number	Layout rule and layout suggestion (Figure A.24)
6A	The minimum spacing between the P+ and N+ diffusions powered by two different (1.8 V and 3.3 V) power supply voltages is 7 μm
6B	A P + guard ring should be inserted between the P+ and N+ diffusions powered by two different power supply voltages
6C	The minimum width of the P+ inserted guard ring is 2 μm
6D	The minimum width of the N+ base guard ring for a 1.8-V device is 1 μm
6E	The minimum width of the N+ base guard ring for a 3.3-V device is 2 μm
6F	The 1.8-V N-well pickup and the P+ source of a 1.8-V PMOS should be abutted together if possible. The 3.3-V N-well pickup and the P+ source of a 3.3-V PMOS should be abutted together if possible

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Transient-Induced Latchup in CMOS Integrated Circuits Ming-Dou Ker and Sheng-Fu Hsu

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ISBN: 978-0-470-82407-8