Chapter 1 CMOS Processing Flow

- 0.25um 1P5M
- 0.18um 1P6M
- 0.15um 1P7M
- 0.13um 1P8M
- 0.09um
- Copper Interconnection
- Mixed-Signal / RF
- CMOS Processing
- Processing Integration

TSMC 0.25um 1P5M

Characteristics of 0.25μm CMOS Logic Product	
	CL025G
Core Voltage	2.5 V
I/O Voltage Option	3.3 V or 5 V tolerant
Physical Gate	0.24-μm
Contacted Metal Pitch	M1: 0.64-μm M2~M4: 0.80-μm M5: 0.90-μm
Ring Oscillator Delay	38 ps
I_{OFF} Spec. (worst case)	0.1 nA/μm
Well Formation	Retrograde Well
Isolation	Shallow Trench Isolation
Salicide	$TiSi_2$
Metal	Up to five layers AlCu
Via Fill	Tungsten with CMP
Lithography	Deep UV

TSMC 0.18um 1P6M

Characteristics of 0.18μm CMOS Logic Product Family			
	CL018G	**CL018LV**	**CL018LP**
Core Voltage	1.8 V	1.5 V	1.8 V
I/O Voltage Option	3.3 V		
Physical Gate	0.16-μm	0.13-μm	0.16-μm
Contacted Metal Pitch	M1: 0.46-μm M2~M5: 0.56-μm M6: 0.90-μm		
Ring Oscillator Delay	28 ps	25 ps	36 ps
I_{OFF} Spec. (worst case)	0.1 nA/μm	1 nA/μm	0.003 nA/μm
Well Formation	Super-Steep Retrograde		
Isolation	Shallow Trench Isolation		
Salicide	$CoSi_2$		
Metal	AlCu, up to six layers		
Via Fill	Tungsten with CMP		
Lithography	Deep UV, with Phase-Shift Mask		
Applications	Baseline e.g., ASIC	High Speed e.g., Graphics	Low Power e.g., Portables

TSMC 0.15um 1P7M

Characteristics of 0.15 μm CMOS Logic Product Family				
	CL015LV	**CL015G**	**CL015HS**	**CL015LP**
Core Voltage	1.2 V	1.5 V	1.5 V	1.5 V
I/O Voltage Option	3.3 V			
Contacted Metal Pitch	M1: 0.39-μm M2~M6: 0.48-μm M7: 0.90-μm			
Ring Oscillator Delay	20 ps	23 ps	14 ps	31 ps
I_{OFF} Spec. (worst case)	＜1 nA/μm	＜1 nA/μm	17 nA/μm	＜0.005 nA/μm
Well Formation	Super-Steep Retrograde			
Isolation	Shallow Trench Isolation			
Salicide	$CoSi_2$			
Metal	AlCu or Cu, up to seven layers			
Via Fill	Tungsten or copper, with CMP			
Lithography	Deep UV, with phase-shifting mask			
Applications	High - Performance e.g., Graphics	Core-Logic e.g., ASIC	Ultra-Fast e.g., CPU	Low-Power e.g., Portables

TSMC 0.13um 1P8M

Characteristics of 0.13 μm CMOS Logic Product Family				
	CL013LV	**CL013G**	**CL013HS+**	**CL013LP**
Core Voltage	1.0 V	1.2 V	1.2 V	1.5 V
I/O Voltage Option	3.3 V or 2.5 V	3.3 V or 2.5 V	3.3 V	3.3 V or 2.5 V
Contacted Metal Pitch	M1: 0.34-μm M2~M7: 0.41-μm M8: 0.90-μm			
Ring Oscillator Delay (ps/gate)	14 (std. Vt) 17 (high Vt)	19 (std. Vt) 27 (high Vt) 15 (low Vt)	10 ps	28 ps
I_{off_nom} Spec. (nA/μm)	10 (std. Vt) 1 (high Vt	0.3 (std. Vt) 0.03 (high Vt) 10 (low Vt)	15	0.0015
Well Formation	Super-Steep Retrograde			
Isolation	Shallow Trench Isolation			
Salicide	$CoSi_2$			
Metal	Copper interconnect up to eight layers			
Via Fill	Copper, with CMP			
Lithography	193/248 nm			
Applications	High - Performance e.g., Graphics	Core-Logic e.g., ASIC	Ultra-Fast e.g., CPU	Low-Power e.g., Portables

0.09um

TSMC unveiled its full 90-nanometer technology under the brand name Nexsys and, at the same time announced that 90-nanometer risk production would start in September of 2002. Volume production of the Nexsys 90-nm process will be manufactured on 300mm wafers.
Nexsys technology satisfies the power, performance and integration requirements of a broad spectrum of applications and includes high-performance, low-power, mixed-signal/RF, and embedded memory options. TSMC established the Nexsys brand for its next-generation SOC process technology platform. The company's 90-nm technology is the first TSMC process to adopt this brand. Nexsys offers a unique triple gate oxide option that facilitates three different oxide thicknesses on a single chip. The triple gate oxide feature removes design restrictions caused by various core/IO combination requirements and should lead to more innovative SOC designs. With 70-75% linear shrinkage and a two-times performance improvement, compared to TSMC's 0.13-micron technology, Nexsys is poised to become the de facto SoC process technology platform standard.

TSMC 0.09um

The 90-nm process technology features:
Core supply voltage ranging from 1.0V to 1.2V
I/O and analog blocks ranging from 1.8V to 3.3V
Multiple threshold voltage (Vt) option for optimized transistor speed and power consumption trade-offs
Extremely tight process control for 50-nanometer gate length - the high speed process
Ni-salicide for better sheet resistance (Rs) in narrow line widths
Nine-layer copper interconnect, with an extra redistribution layer optional for flip-chip package
Low-k dielectrics with k £ 2.9 for the lowest RC delay and power consumption
A fully logic process-compatible 90-nanometer version of the Nexsys mixed-signal/RF technology will be available in January 2003. Nexsys mixed signal/RF process will feature:
MiM capacitor
High resistance resistor
High Q inductor and varactor
DNW(deep N-well) bipolar junction transistor

TSMC 0.09um

TSMC has scheduled the release of embedded 1TRAMTM and 6T/8T SRAM by September 2002. A common 6T SRAM cell will be available in core, low-power and high-speed processes to enable SOC designs.
Ultra-high-density (UHD) cell and high-cell-current (HC) cell for different applications will also be available at a later date. Aggressive release schedules of embedded 1TRAMTM and Flash make SOC designs on Nexsys more realistic than ever.

Launching Nexsys Prototyping Service
TSMC's will launch 90-nm prototyping service beginning in the second quarter of 2002. This cost-sharing prototyping service has become essential considering the escalating costs of masks and wafers for the 90-nm generation. The launching frequency will increase to every other month or more in 2003 to meet anticipated demand.

Copper Interconnection

Copper Interconnection

The electrical resistance of copper interconnects is less than two-thirds that of tungsten-aluminum interconnects. The series resistance of copper via runs as low as 20% that of tungsten plugs. Starting from the 0.18-micron process, TSMC has offered customers the option of copper interconnects for the top two layers, which are commonly used for power, clock routing and bonding pads. With this option alone, customers can realize 15% RC delay reduction.TSMC provides both top two-layer and all-layer copper options at the 0.15-micron process. While copper offers the greatest performance advantage when implemented to the top two metal layers, TSMC also offers an all-layer copper option. In fact, TSMC's 0.13-micron process and beyond will be built on an all copper interconnect architecture.The lower electrical resistance due to copper leads to improved power distribution and device performance throughout the chip. Copper also improves the electromigration resistance, a major concern in IC's long term reliability, by as much as 50 times. Furthermore, copper's lower resistance helps to reduce cross-talk by providing a better control over the tight metal pitch.In summary, advanced technology demands extremely high routing density that necessitates copper interconnects. TSMC made its commitment early and has successfully developed the industry-leading copper process.

Mixed Signal / RF

Mixed Signal / RF

TSMC is the only dedicated foundry to offer all-CMOS mixed signal and RF 0.35-µm, 0.25-µm and 0.18-µm processes. The company's 0.35-µm process was recently used to manufacture the world's first fully integrated single-chip Bluetooth transceiver using all-CMOS 2.4GHz RF integrated circuit.

TSMC's CMOS Mixed Signal and RF processes provide designers with smaller device dimensions, increased performance and lower costs than expensive BiCMOS and gallium arsinide processes.

Mixed Signal / RF

Characteristics of TSMC MixedSignal/RF CMOS Family			
	CM035	**CM025**	**CM018**
Core Voltage	3.3 V	2.5 V	1.8 V
I/O Voltage Option	3.3 /or 5V	3.3 /or 5V	3.3 V
Physical Gate	0.35-μm	0.24-μm	0.16-μm
Metal	Up to 4M+	Up to 5M+	Up to 6M+
Contacted Metal Pitch	M1: 0.95-μm M2~M3: 1.10-μm M4: 1.20-μm	M1: 0.64-μm M2~M4: 0.80-μm M5: 0.90-μm	M1: 0.46-μm M2~M5: 0.56-μm M6: 0.90-μm
Ring Oscillator Delay	51 ps	38 ps	28 ps
I_{OFF} Spec. (worst case)	0.1 nA/μm	0.1 nA/μm	0.01 nA/μm
Well Formation	Twin well (drive_in)	Retrograde well	Super Steep retrograde)
Isolation	LOCOS	STI(shallow trench isolation)	STI
Salicide	$TiSi_2$	$TiSi_2$	
Capacitor	Metal(MiM) or Poly(PiP)	Metal(MiM) or Poly(PiP)	MiM
Inductor	Thick Metal(Top)	Thick Metal(Top)	Thick Metal(Top)
Via Fill	W plug	W plug	W plug
Lithography	I-line	Deep UV	Deep UV(phase shift mask)

CMOS PROCESSING

Silicon Wafer

Czochralski method – single-crystal method

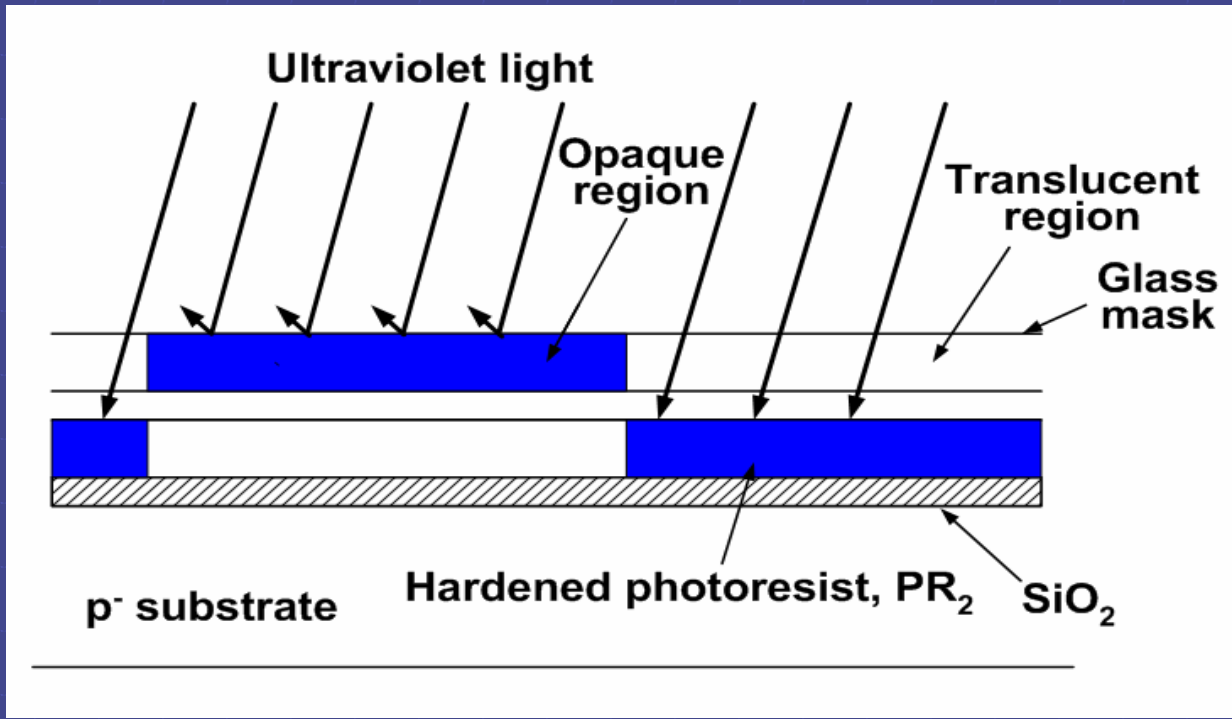
- starts with a seed of single crystal silicon, and the pull rate and speed of rotation determine the diameter of the crystal rod or ingot
- heavily doped silicon is added to the melt before the single-crystal ingot is pulled
- the ingot is cut into wafers using a large diamond saw
- p^- is doped around $N_A \cong 2 \times 10^{21}$ donor/m^3, *resistivity* $\cong$ 10-20 $\Omega \cdot$ cm.

Epitaxial

The surface of wafer might be doped more heavily, and a single-crystal epitaxial layer of the opposite type might be grown over its surface.

Photolithography

Selected portion of silicon wafer can masked out so that the some type of processing step can be applied to the remaining areas.

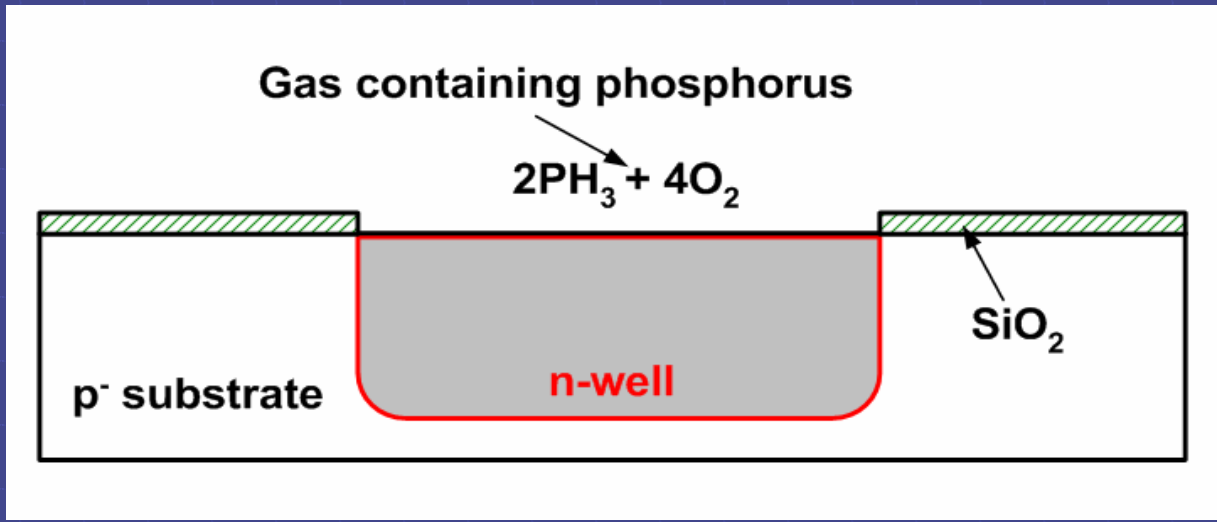


- grow a thin oxide (SiO_2) to protect the surface

Photoresist

- ***negative photoresist***, exposed photoresist remains after the masking
- ***positive photoresist***, exposed photoresist is dissolved by organic solvents, the photoresist still remains where the mask was opaque
- By using both positive and negative photoresist, a single mask can sometimes be used for two steps.

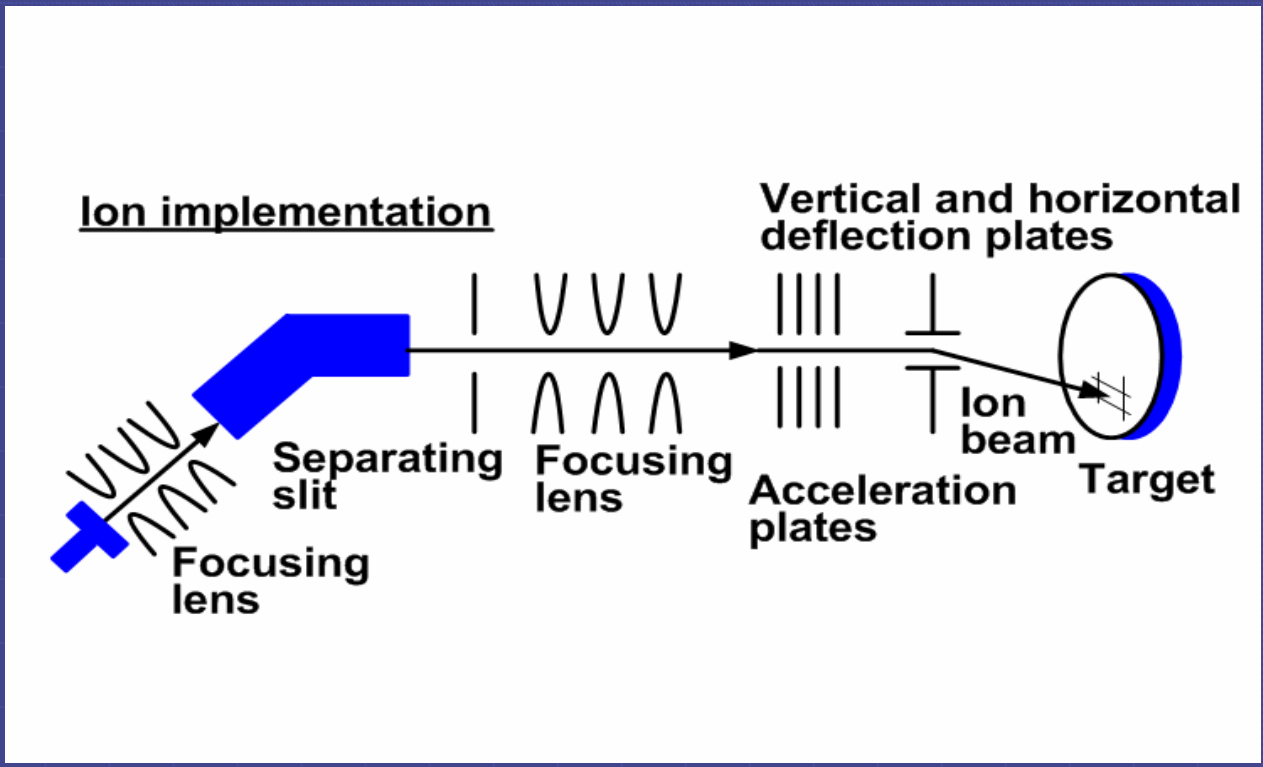
Diffusion



Forming an n well by diffusing phosphorus from a gas into the silicon, through the opening in the SiO_2

- **Dopant is Phosphorus for n-well, Arsenic takes much longer time to diffuse.**
- **900-1100 ºC, high temperature causes dopant to diffuse vertically and laterally. Dopant concentration is the greatest at surface.**
- ***Boron* for p-well.**

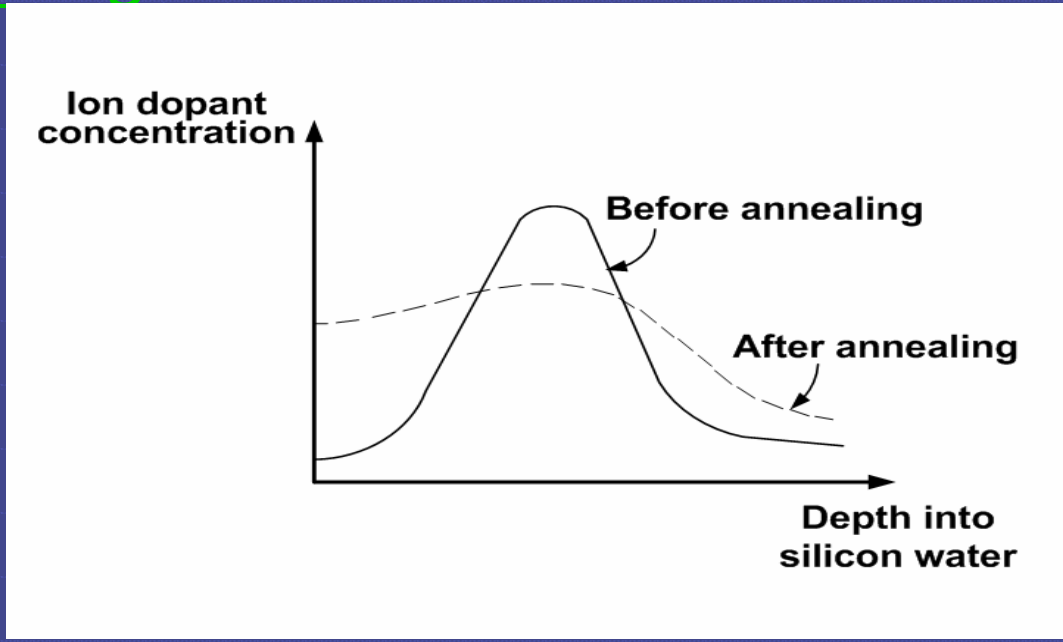
Ion implementation



An ion-implantation system

- Allows more independent control over concentration and the thickness of doped region.
- Ion beams are focused and accelerated at 10 keV and 1 MeV.
- Lattice damage due to nuclear collisions results in displacement of substrate atoms.
- Narrow profile results in heavy concentration (Arsenic with 100 keV, 0.06 um $\pm$ 0.02 um.)
- Greater control over doping level.
- Much smaller side wall diffusion, allows devices to be more closely spaced, minimize overlap between gate-source and gate-drain regions.

Annealing



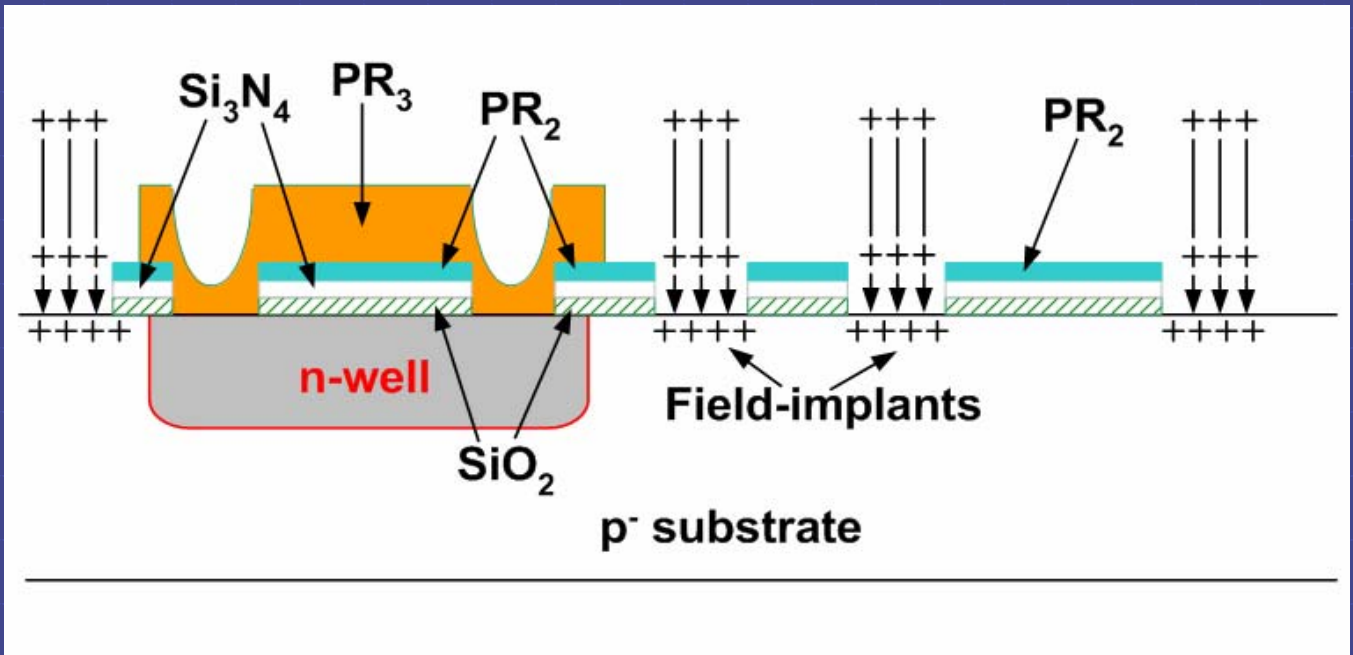
Dopant profiles after ion implantation both before and after annealing

- 1000 ºC for 15-30 minutes, then cooled down.
- Broaden concentration profile, make profile more uniform.
- Solve the above mentioned problems in ion implementation.

Chemical Vapor Deposition

- E.g. Si_3N_4 deposited during a gas-phase reaction at about 800 ºC.

Field-implementation



The cross section when field-implants are being formed

- Field implant where field-oxide grown.
- Guarantee silicon under field-oxide will never invert when the conductor over the field-oxide has a large voltage.
- Leakage between junctions of separate transistors in the substrate region is intended to be unconnected.

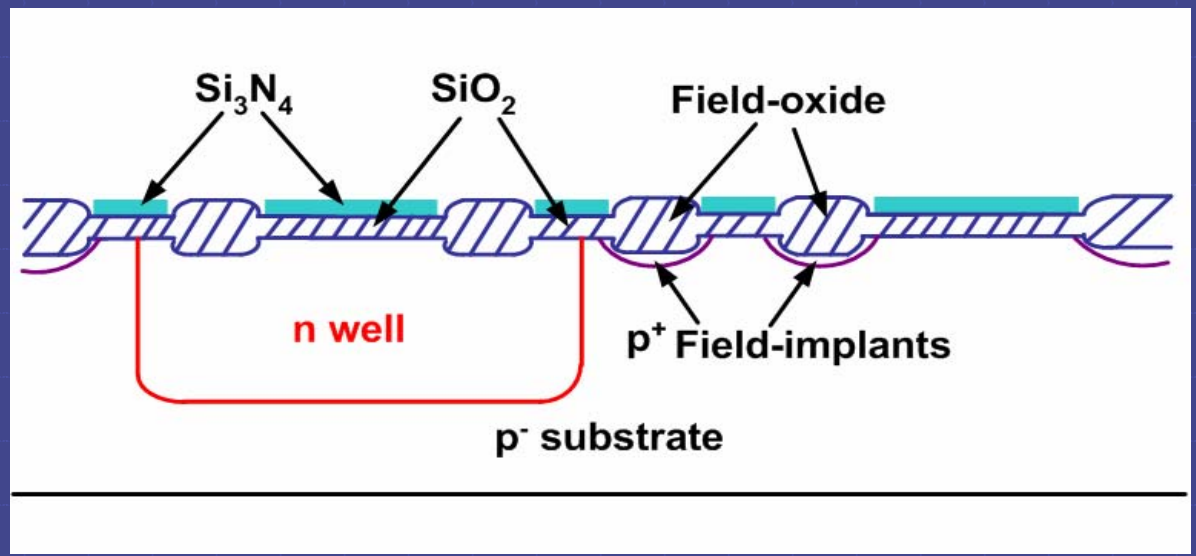
Growing Field-Oxide: *thermal oxide*

***Wet process*: water vapor diffuses into silicon**

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

Dry process: oxygen introduced over wafer, slightly higher temperature then wet process

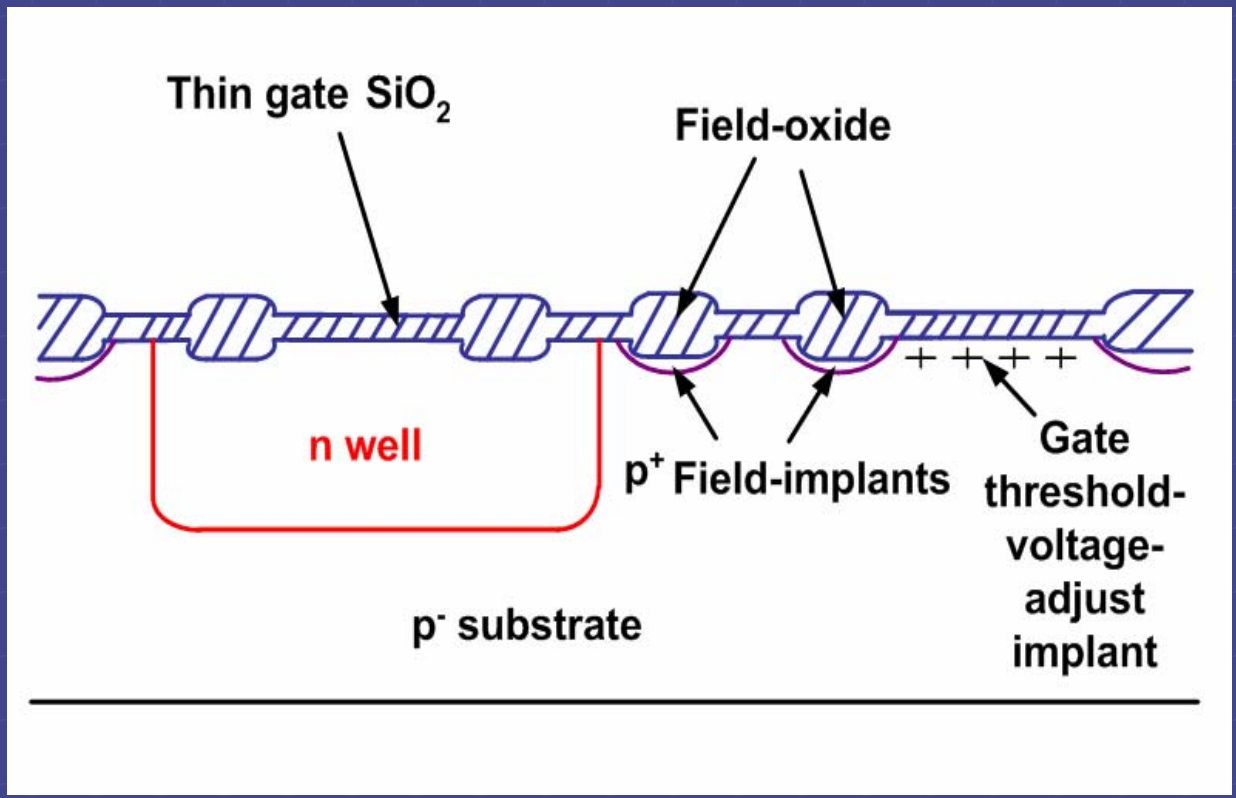
$$Si + O_2 \rightarrow SiO_2$$



The cross section after the field-oxide has been grown.

- SiO_2 takes up approximately 2.2 times the volume of the original silicon, causes SiO_2 to extend approximately 45 percent into, and 55 percent above the surface.
- Wet process is faster because H_2O diffuses faster in silicon than O_2 does.
- Dry process results in denser, higher-quality SiO_2 that is less porous.

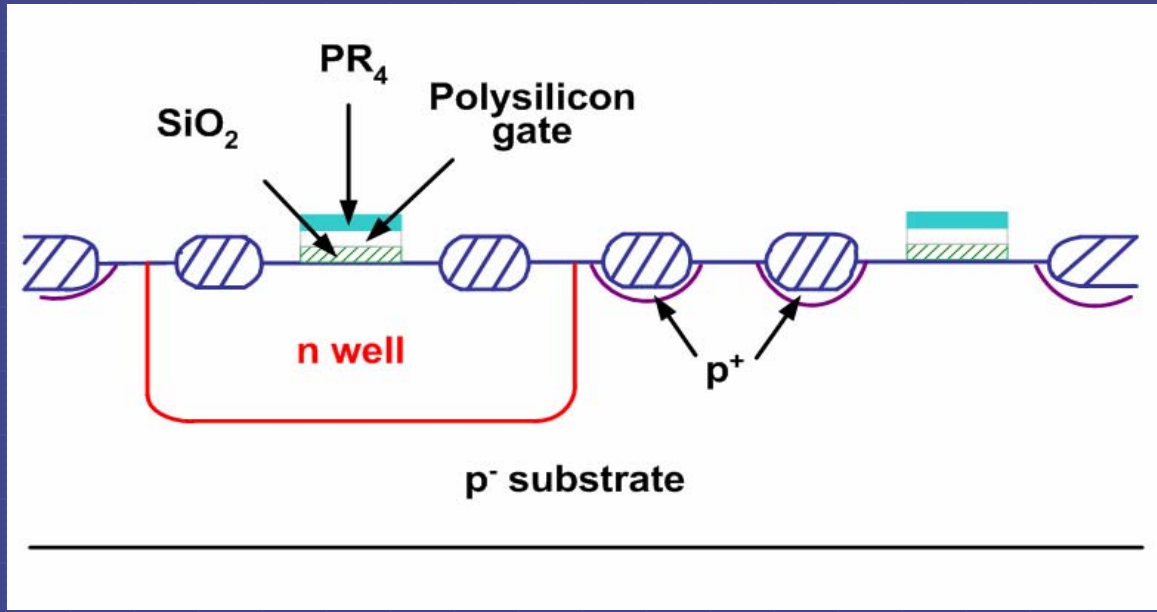
Gate-Oxide and Threshold-Voltage Adjust



Cross section after the thin gate-oxide growth and threshold-adjust implant.

- After gate-oxide (about < 0.01-0.03 um) is grown, donors (boron) are implemented through the oxide to adjust the threshold voltage.
- p-transistor and n-transistor are adjusted at the same time (n-transistor from - 0.1 to 0.7-0.8, p-transistor from - 1.6 to - 0.8-0.9.
- Higher doping level increases the junction capacitance and body effect of transistors in the well.
- Double threshold adjust allows optimum well doping.

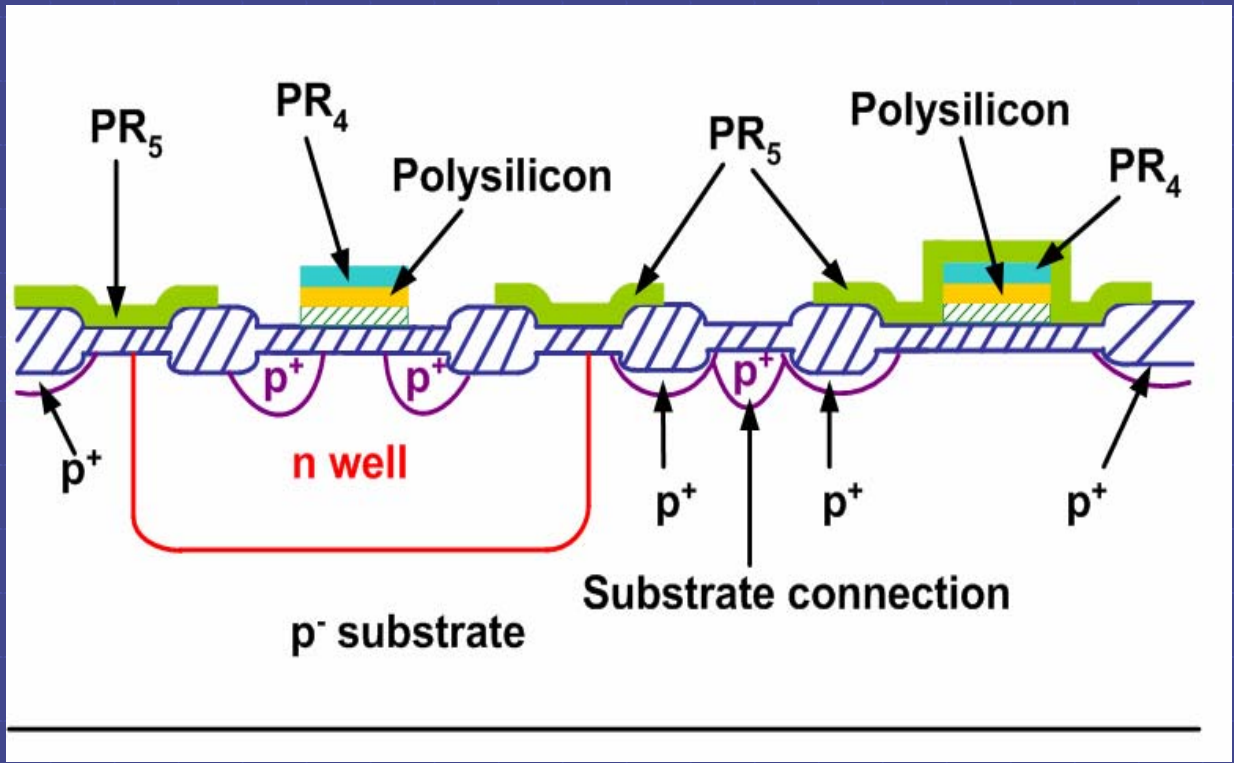
Polysilicon Gate Formation



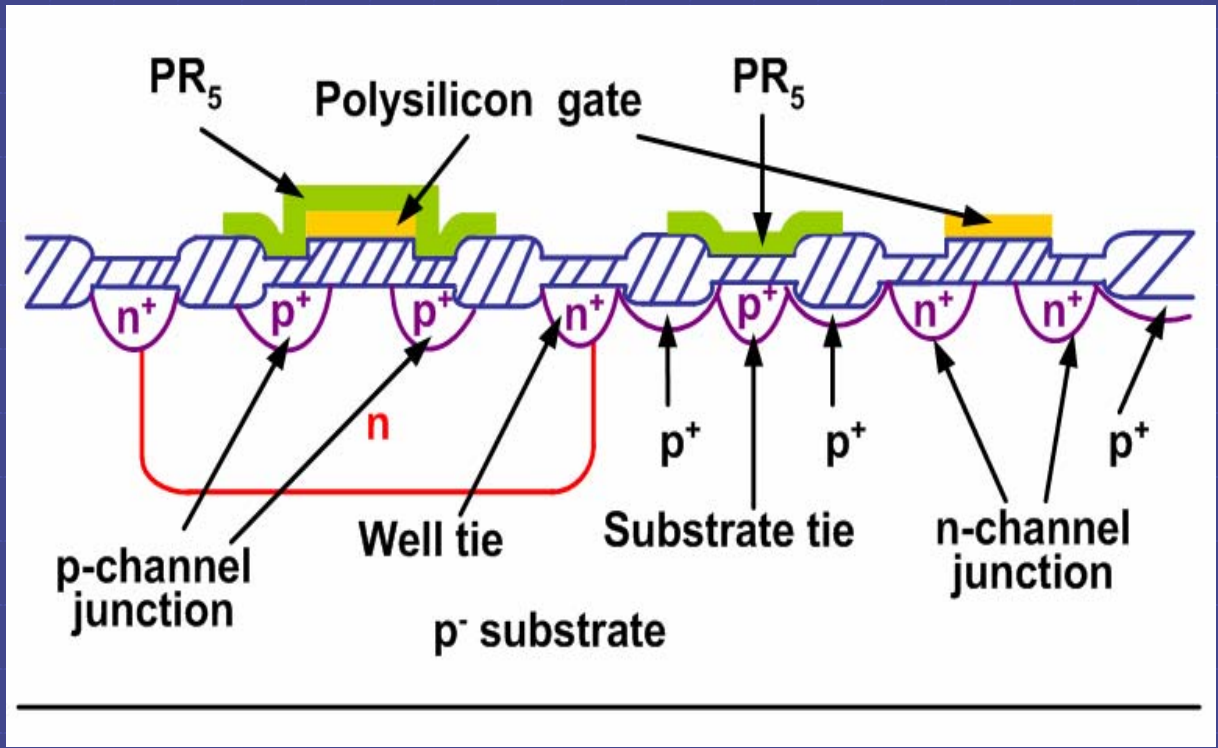
Cross section after depositing and patterning the polysilicon gates.

- Chemical deposition of polysilicon with silane (SiH_4) gas.
- 650 ºC, *noncrystaline or armophous*. (1000-1250 ºC on silicon to create single-crystal silicon)
- Ion implemented with Arsenic to increase its conductivity (10-30 Ω/ □)

Implanting Junction



Cross section after ion-implanting the p^+ junctions.



Cross section after ion-implanting the n^+ junctions.

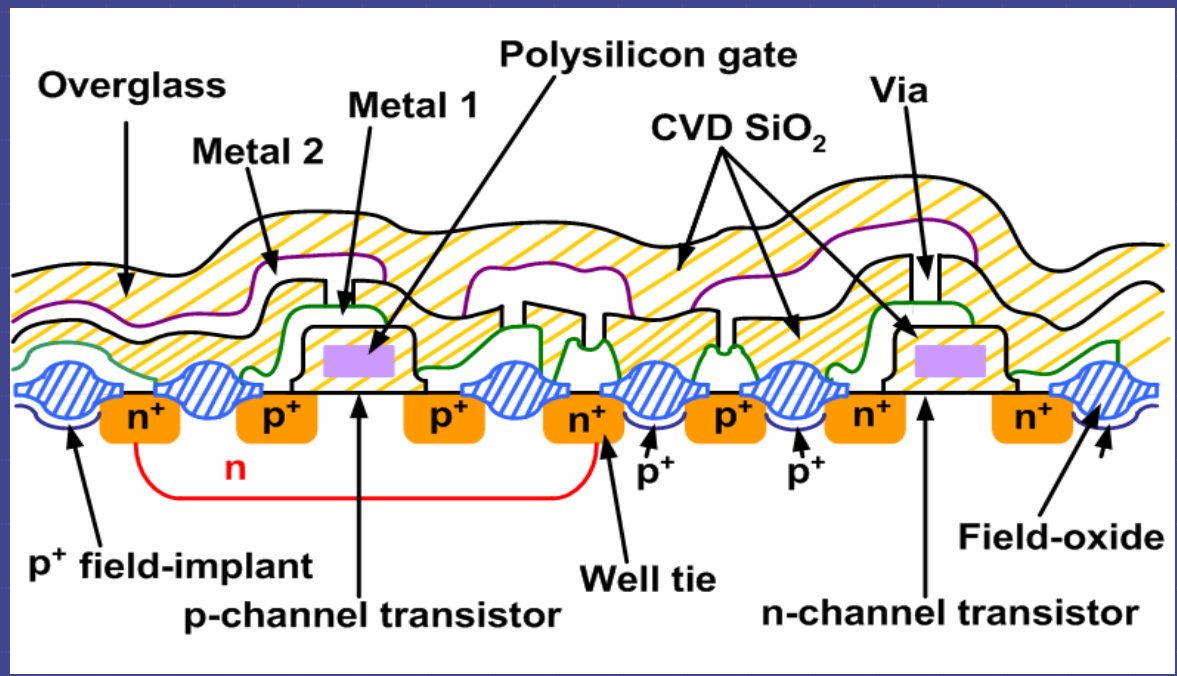
- Boron implemented to from p^+ region. self-aligned to poly edge, resulting in very little overlap.
- p^+ also for substrate Vss contact to prevent latch-up.
- Arsenic implemented to from n^+ region.
- N+ also for n-well V_{DD} contact to prevent latch-up.
- After all junctions have been implanted, the complete wafer is covered in CVD SiO_2. 500 ºC, 0.25-0.5 um.
- Next step, open *contact* hole.

Depositing and Patterning Metal

- Aluminum (Al) for interconnection
- *Evaporation* techniques in a vacuum, the heat for evaporation is produced by electron-beam bombarding in a sputtering system.
- Low-temperature annealing (550ºC), give better bonds between metal and silicon.

Overglass Deposition

Final *passivation* CVD SiO_2 is deposited, often an additional Si_3N_4 is deposited for better impervious to moisture.

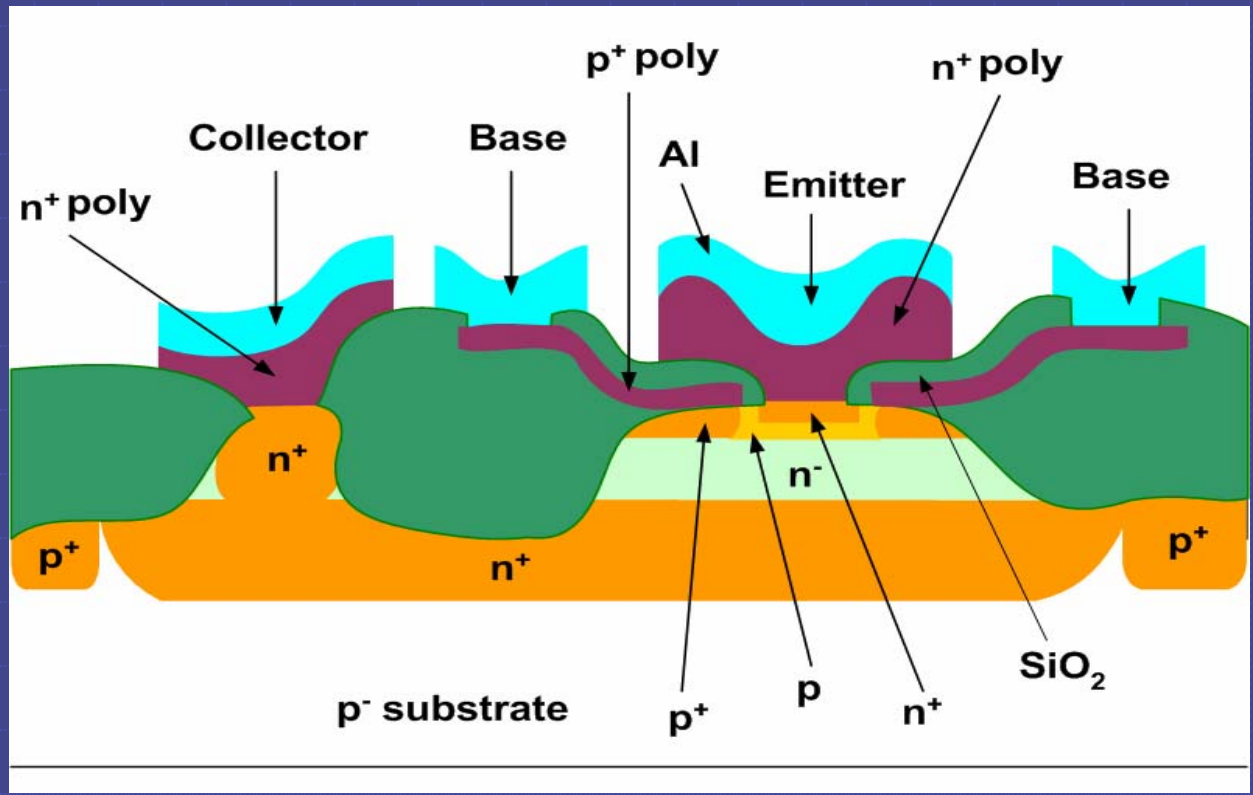


Final cross section of an example CMOS microcircuit.

Some possible process:

- *twin wells*
- *poly-poly* capacitor, thin thermal oxide
- high resistivity poly, 1G Ω/ □ , SRAM
- field-implant under field-oxide in well region
- n-channel and p-channel transistors with different threshold adjust
- 2, 3, 4, 5, or 6 layer of metal
- *planarized* after each metal-patterning step, reactive etching, cover with SiO_2 , the hills are etched faster than the valleys
- thin-film nichrome resistors under the top layer of metal
- transistors realized in epitaxial layer
- BiCMOS

Bipolar Processing



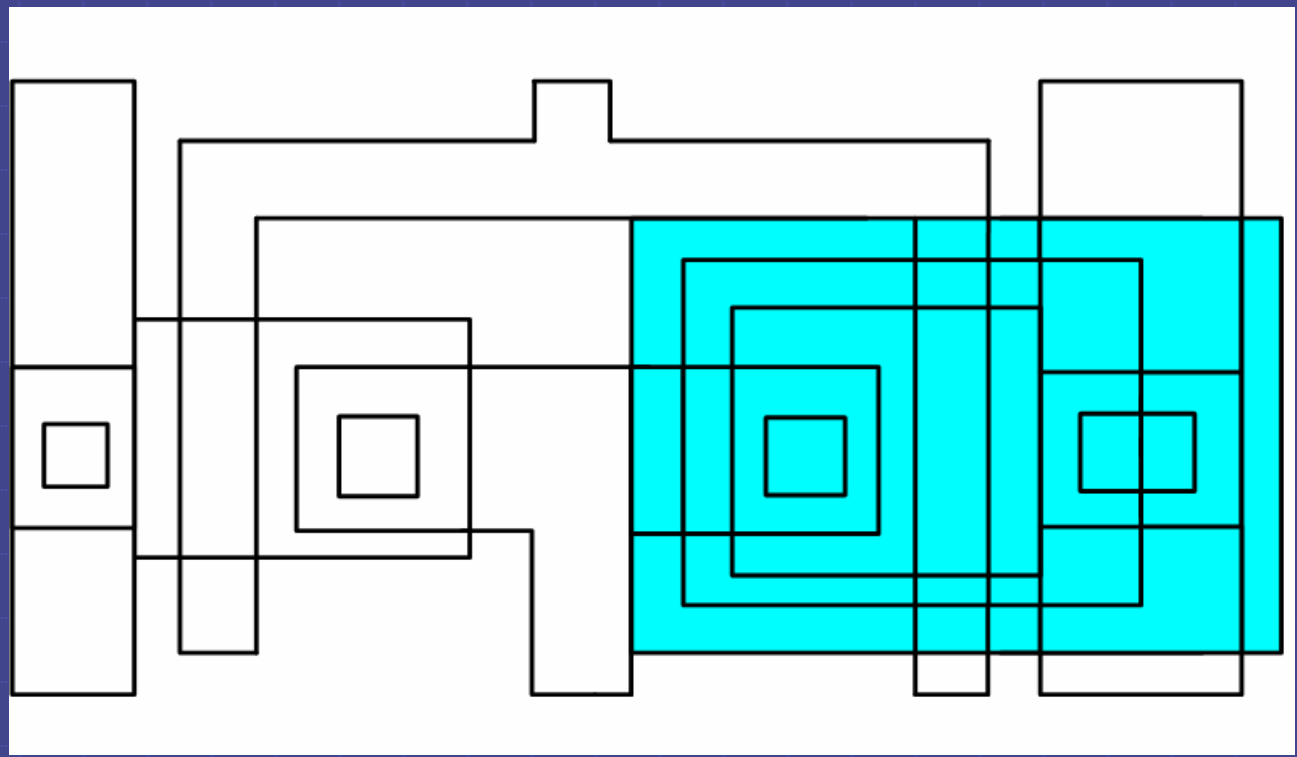
Cross section of a modern, self-aligned bipolar transistor with oxide isolation. The term "poly" refers to polysilicon

- p^- substrate
- n^+ region to lower series collector resistance
- n^- single-crystal epitaxial
- n^+ collector contact region is implemented, the region extends from surface down to n^+ buried region
- polysilicon is used to contact emitter, base, collector
- base p^+ polysilicon is deposited first, during a high temperature step, the boron dopant from polysilicon contact diffuses into silicon to make underlying region p^+ .
- base polysilicon is covered with a thin layer of SiO_2 (0.5um in thickness), the SiO_2 spacer allows the base contact, thereby minimizing base resistance.
- n^+ from emitter polysilicon diffuses into the base p silicon to from emitter region .

PROCESSING INTEGRATION

N-WELL CMOS TECHNOLOGY

(a)



(b)

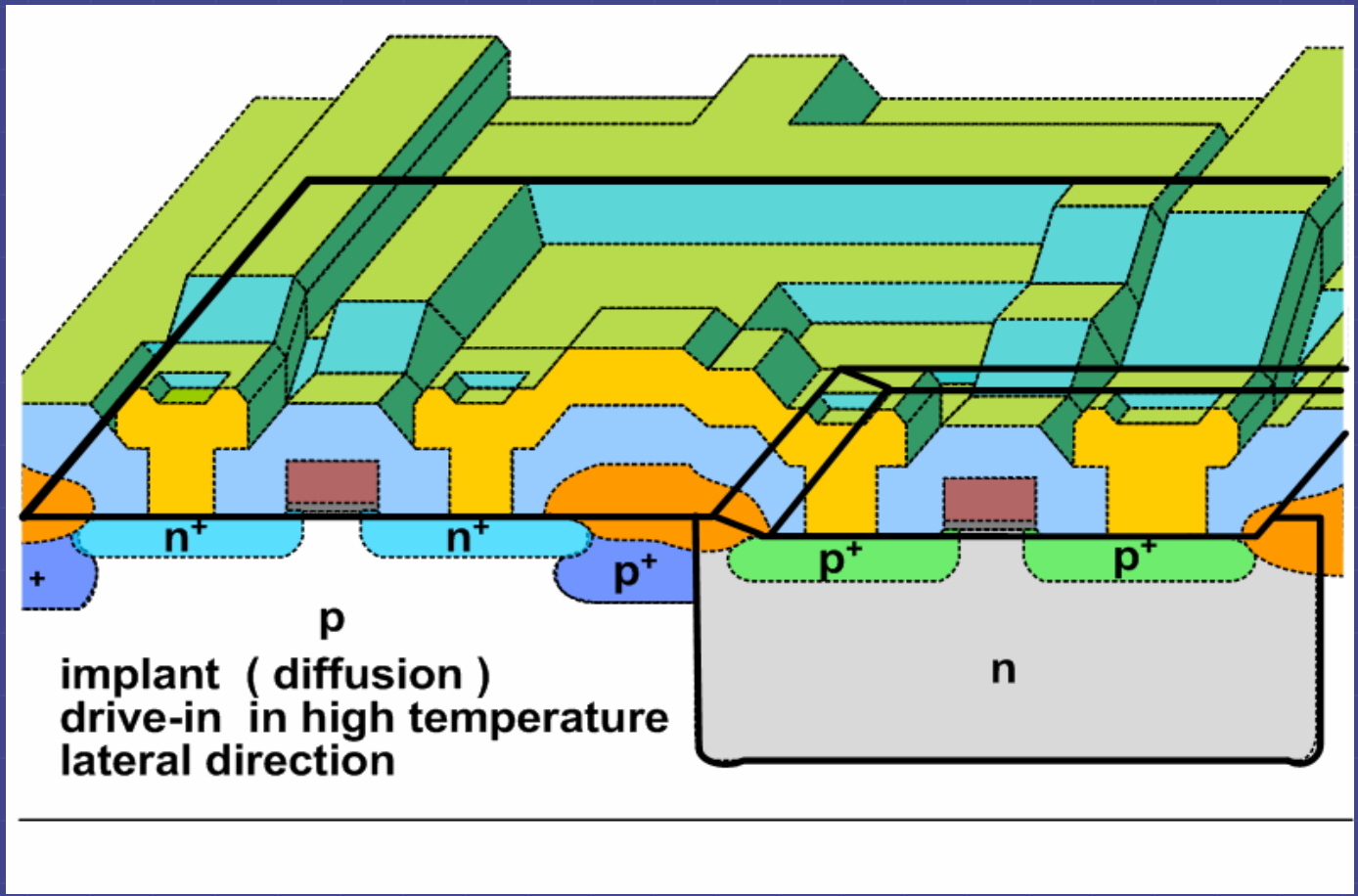
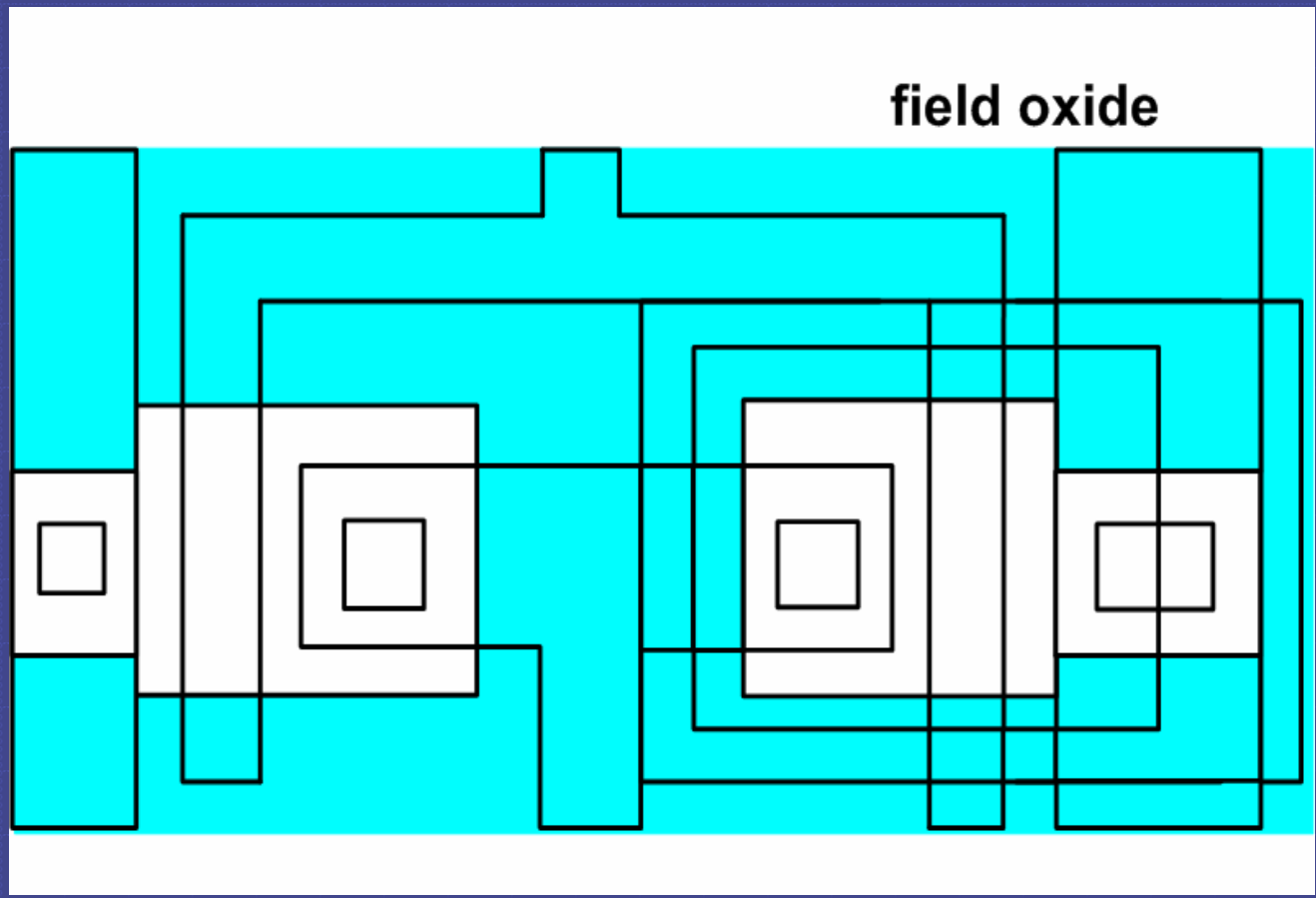


Figure 1: Well implant and drive-in in the n-well CMOS inverter. Window in the mask (a) and cross-section (b)

(a)



(b)

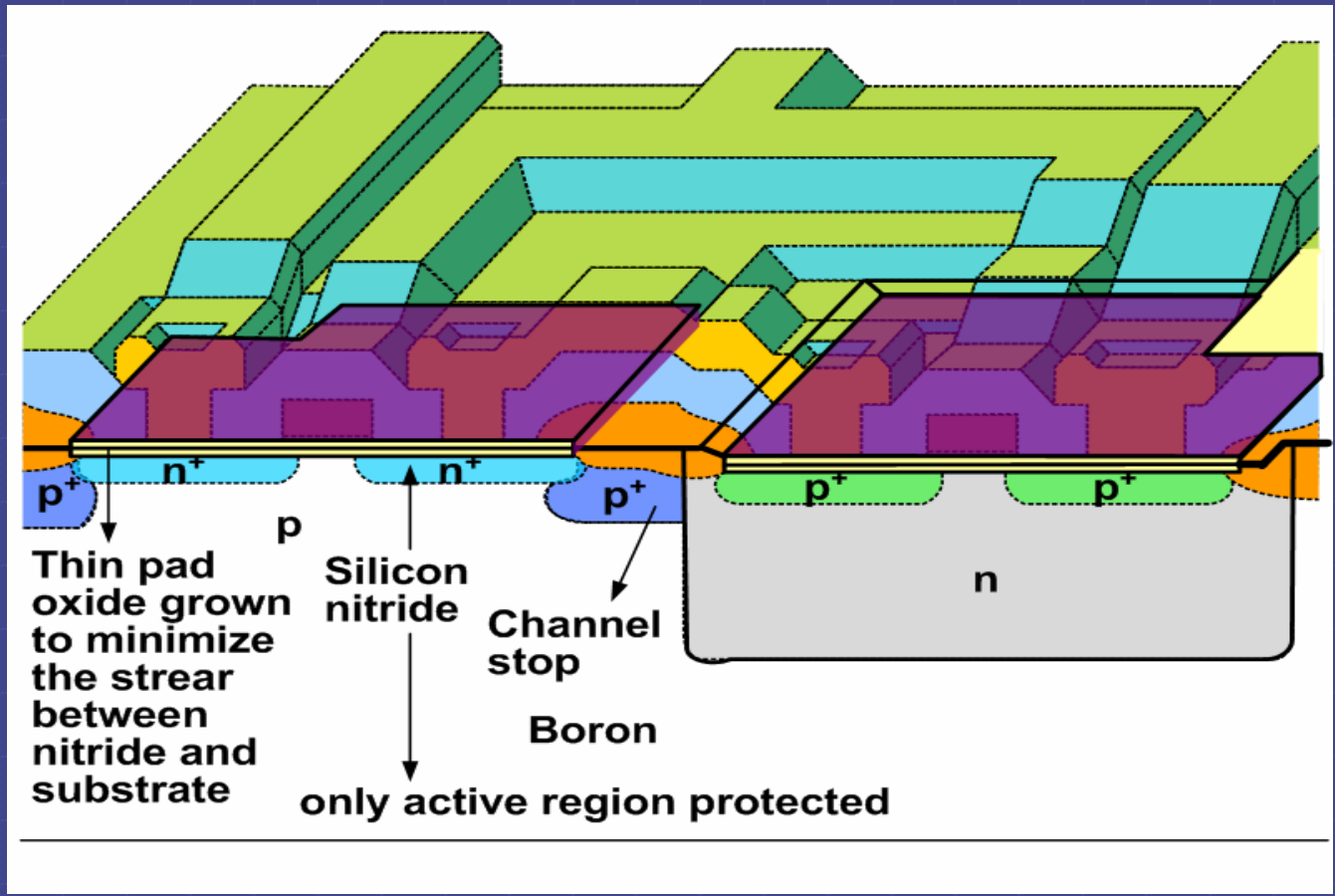
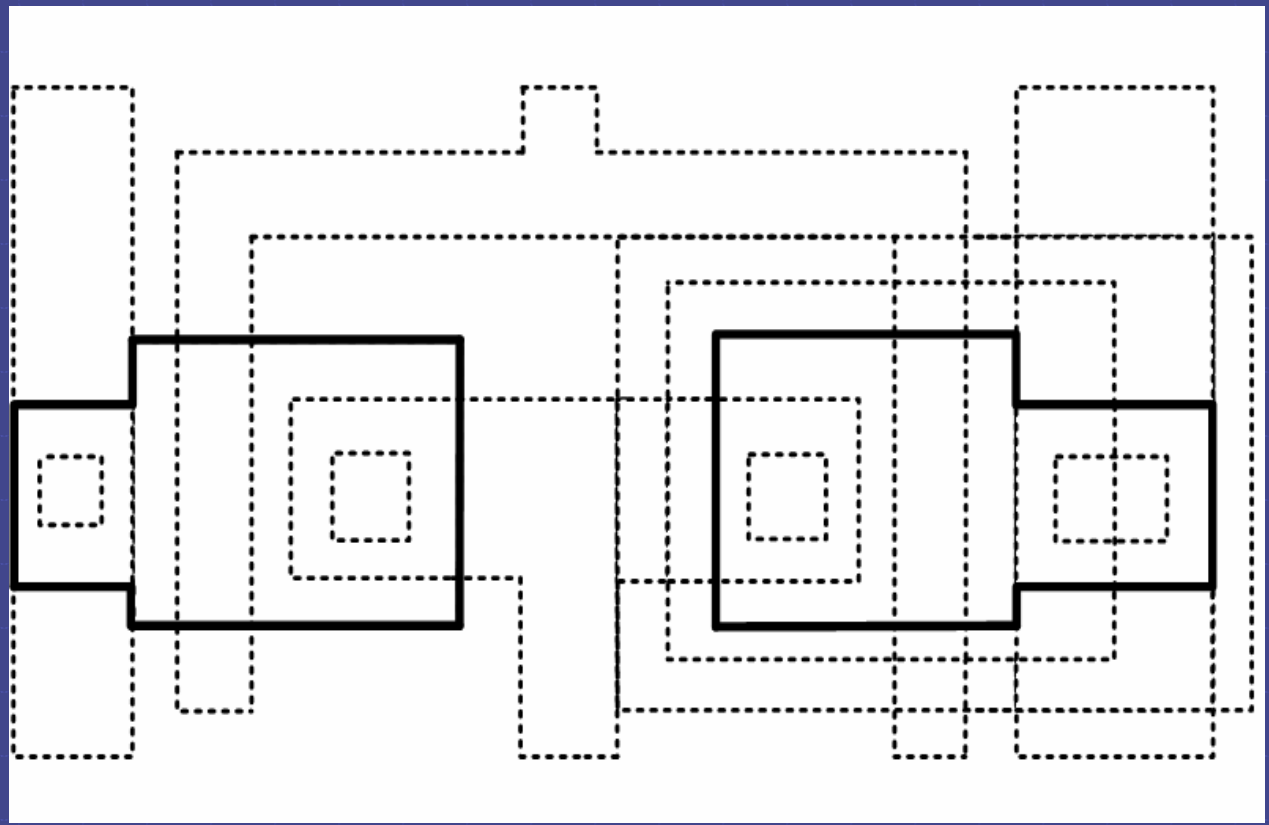


Figure 2: Formation of the active regions in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

(a)



(b)

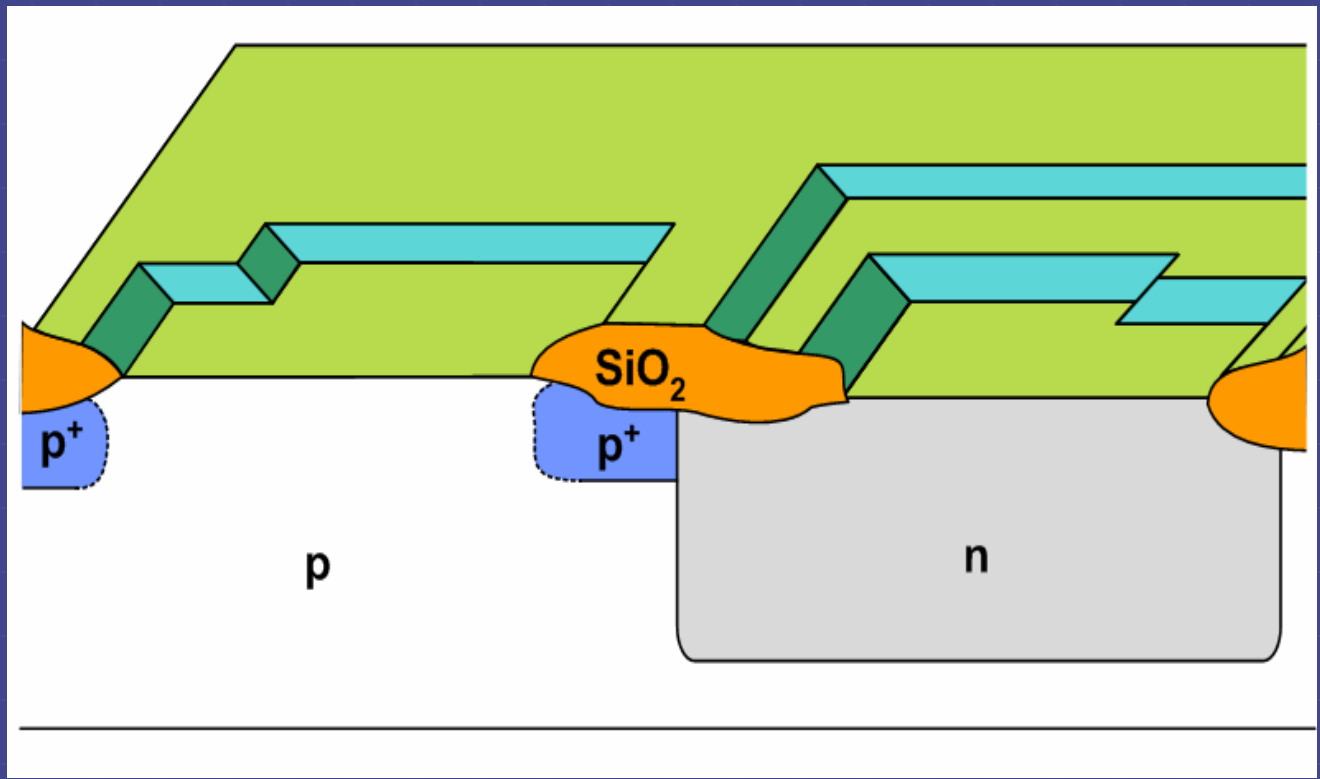
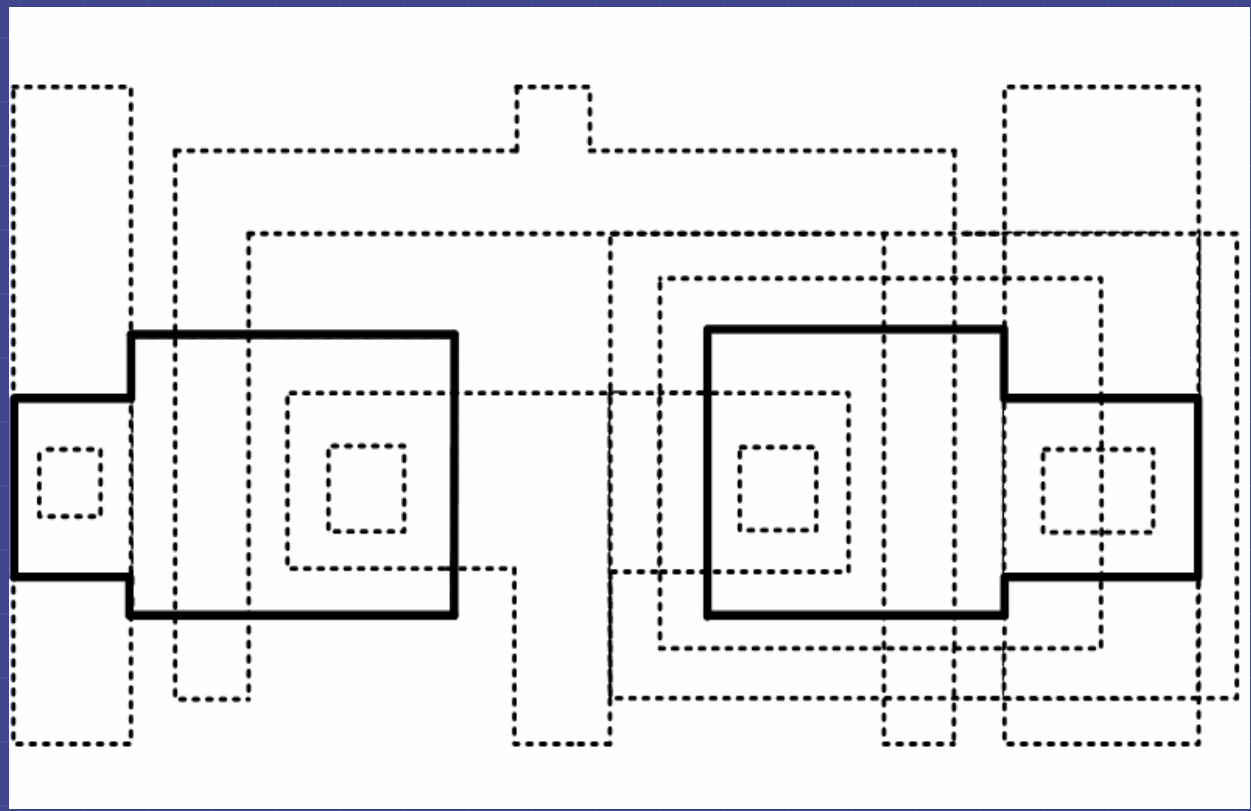


Figure 3: Active regions in the n-well CMOS inverter. Edges of active regions in the mask (a) and cross-section of the inverter.

(a)



(b)

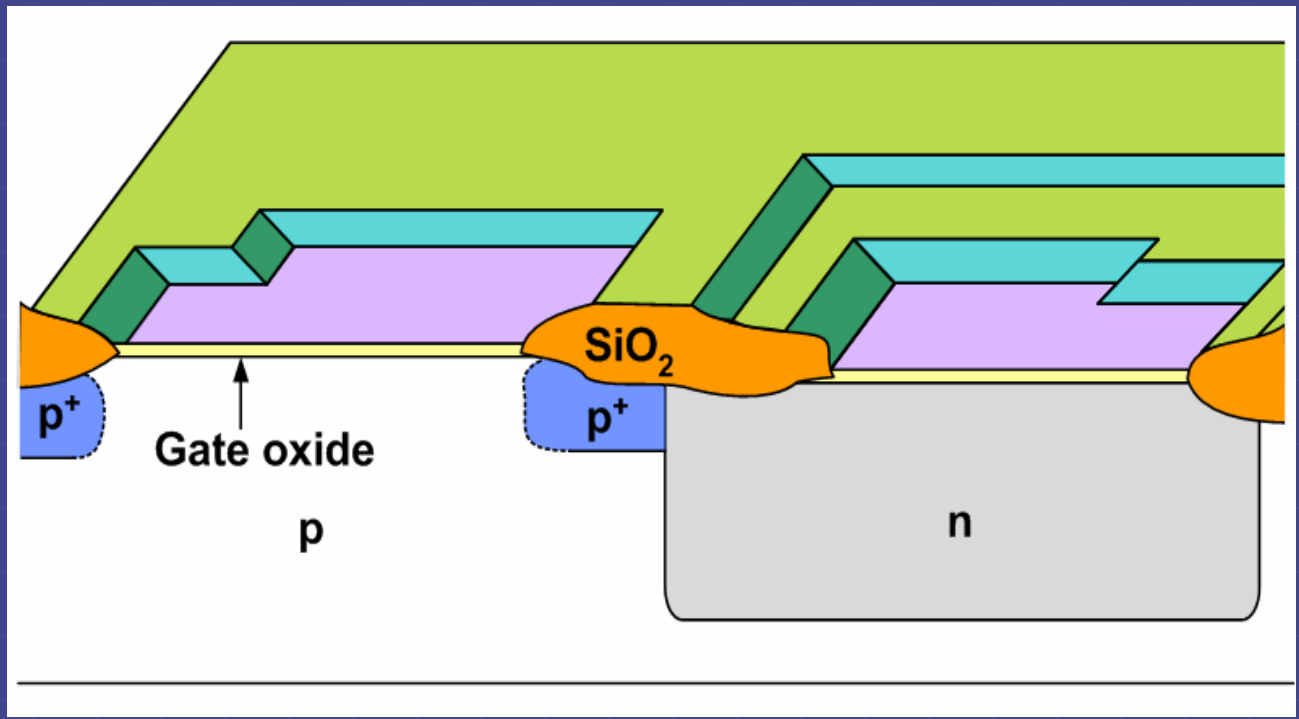
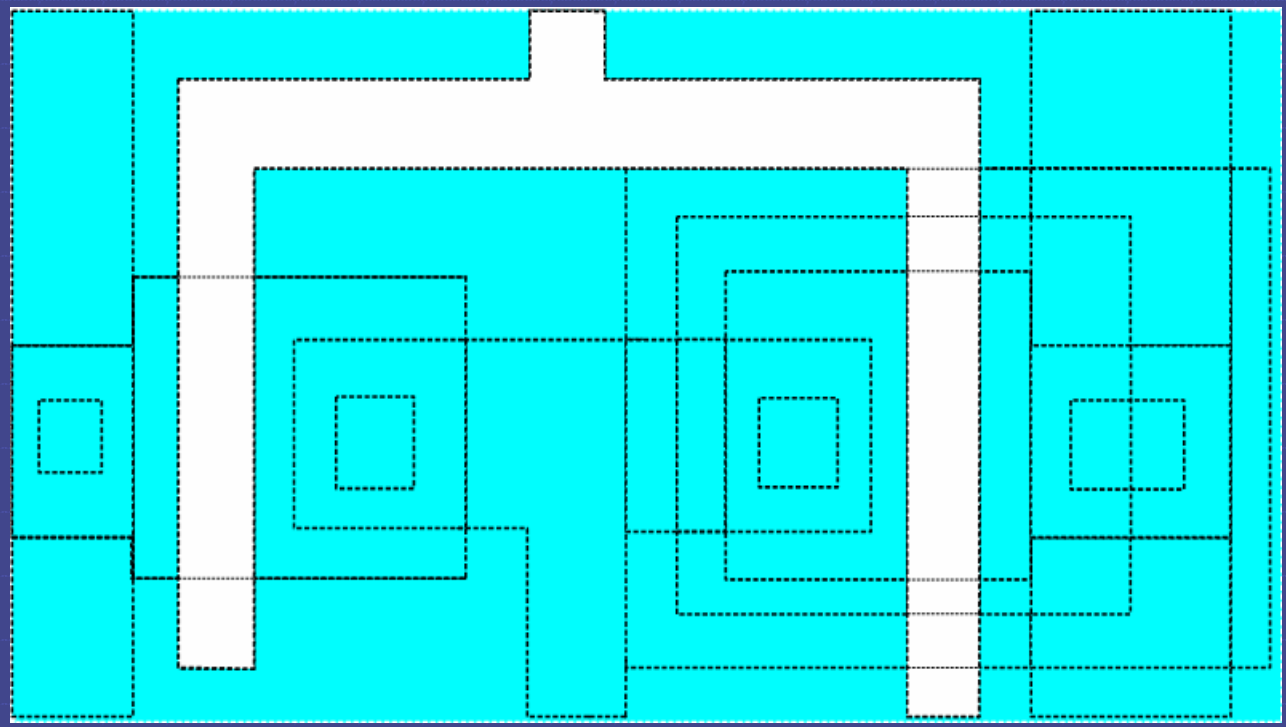


Figure 4: Gate oxide growth in the n-well CMOS inverter. Edges of the gate oxide regions (a) and cross-section of the inverter (b).

CVD: usually doped with n-type impurity with low resistivity

(a)



(b)

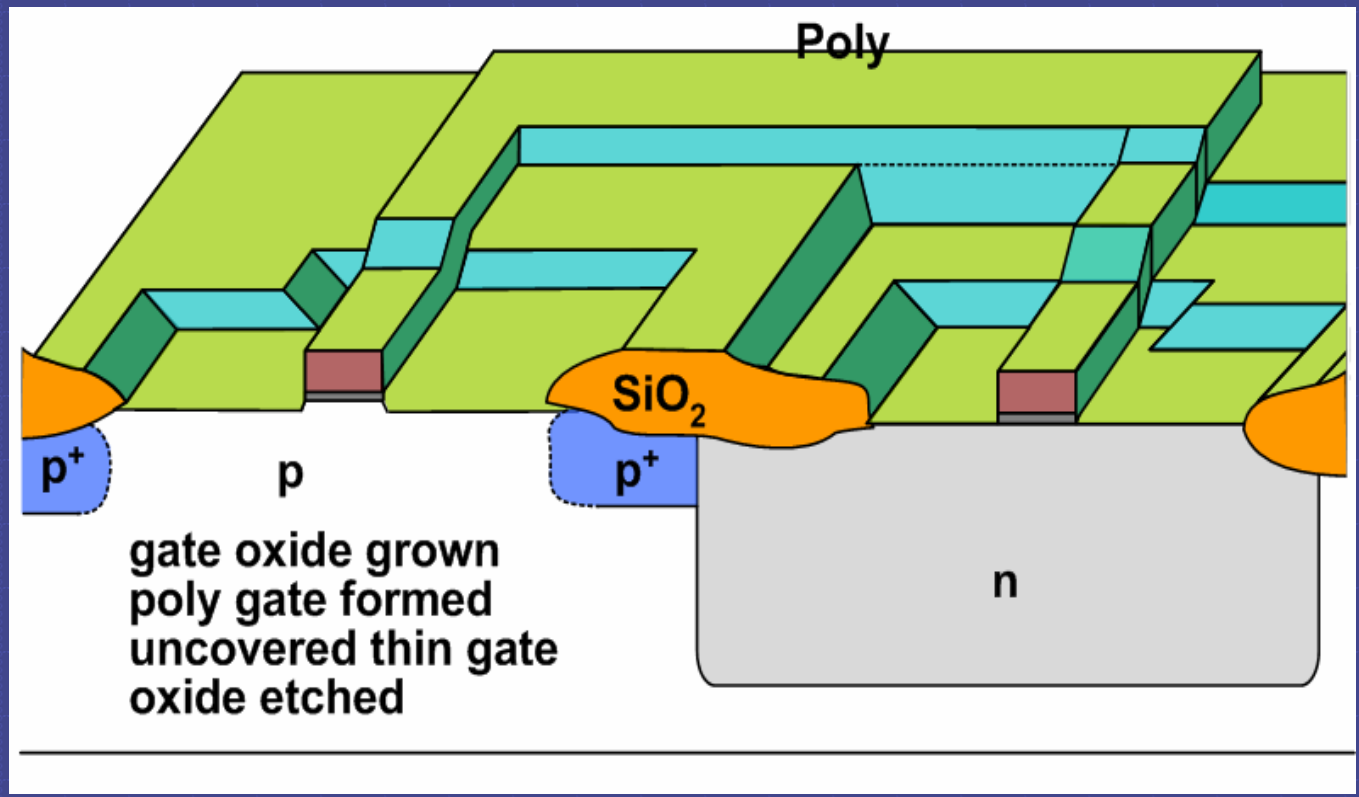
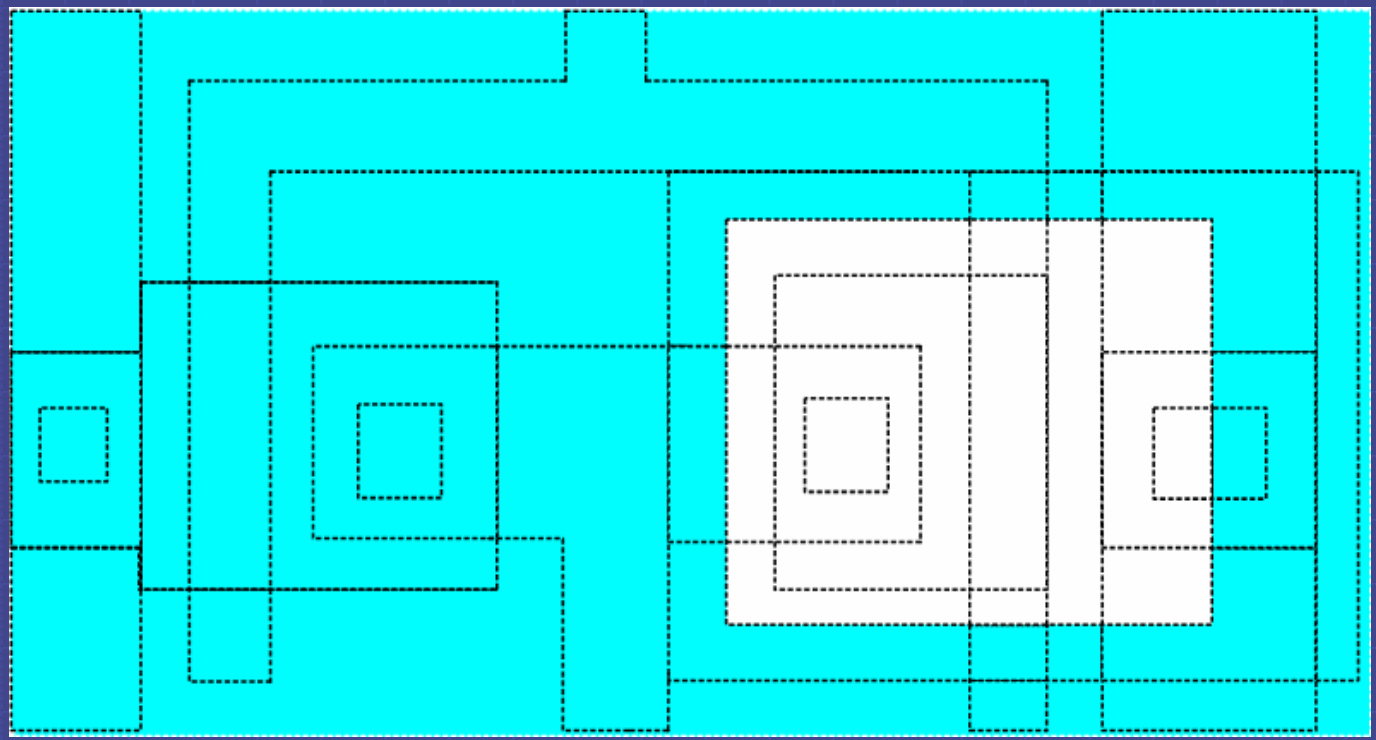


Figure 5: Polysilicon region in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

(a)



(b)

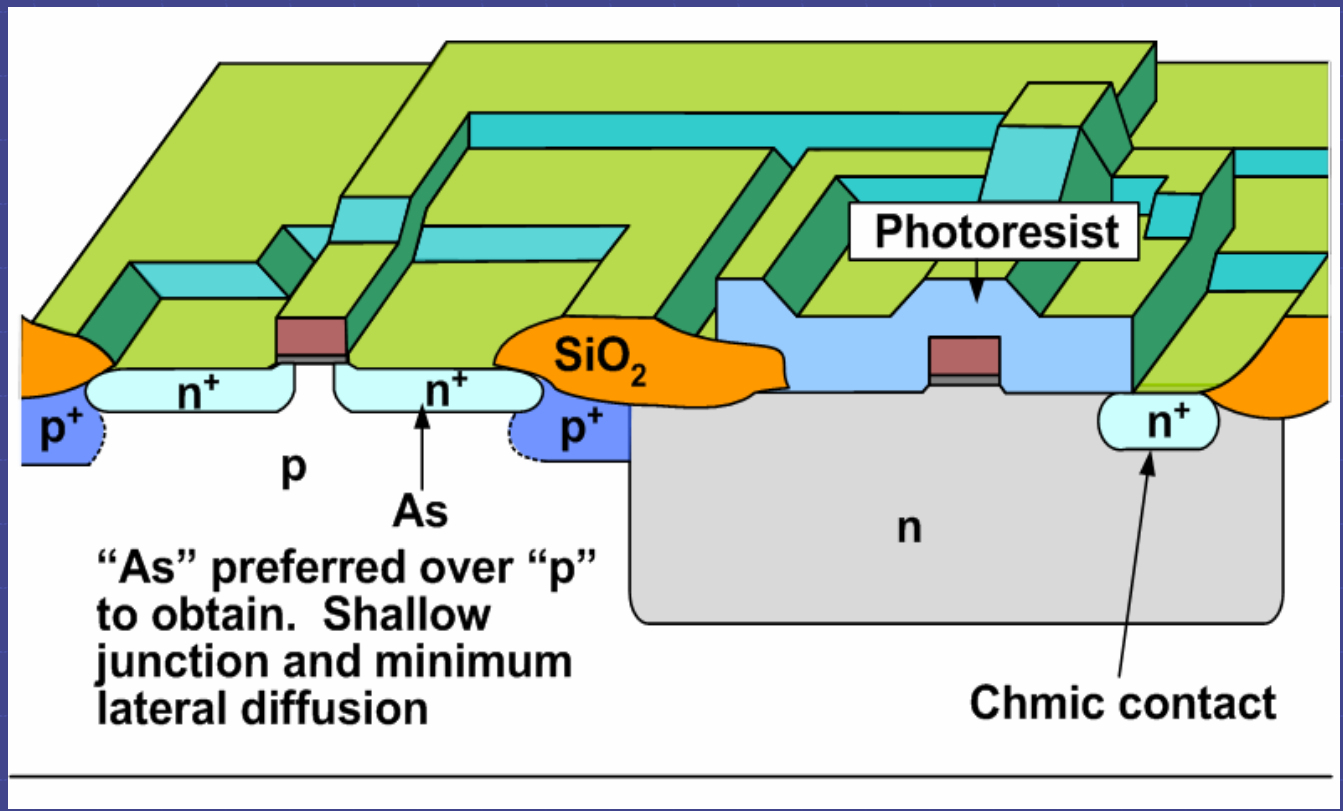
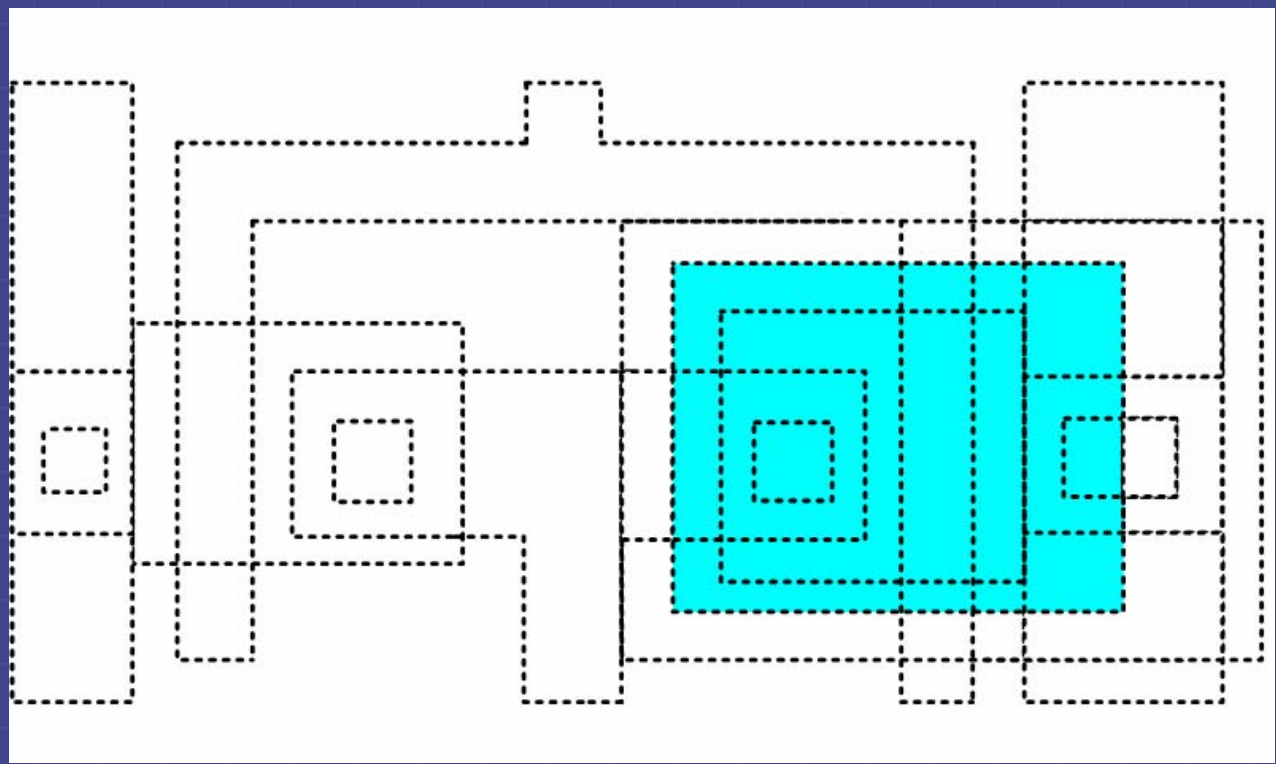


Figure 6: Implantation of n-channel transistor drain and source. Window in the n-select mask (a) and cross-section of the inverter (b).

(a)



(b)

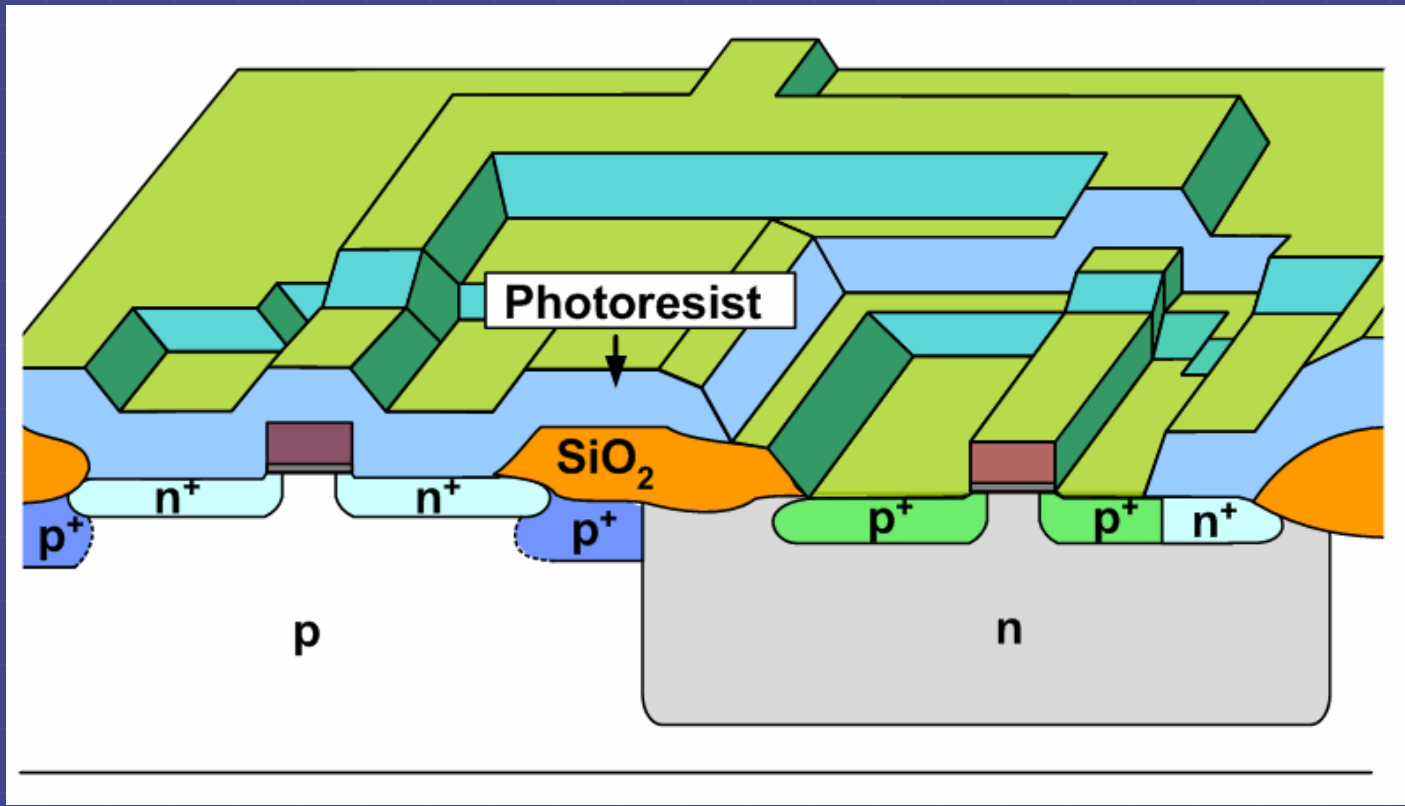
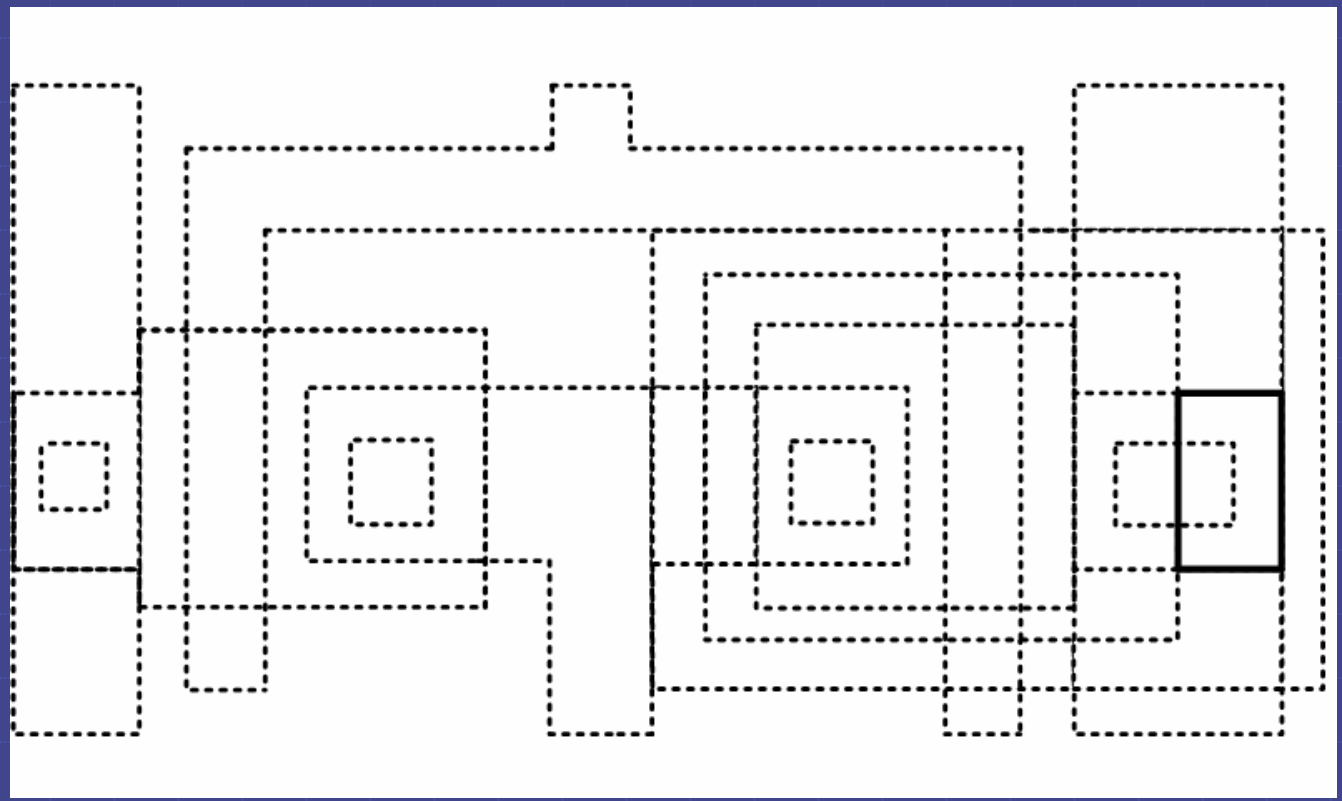


Figure 7: Implantation of p^+ regions. Window in the negative of the n-select mask (a) and cross-section of the inverter (b).

(a)



(b)

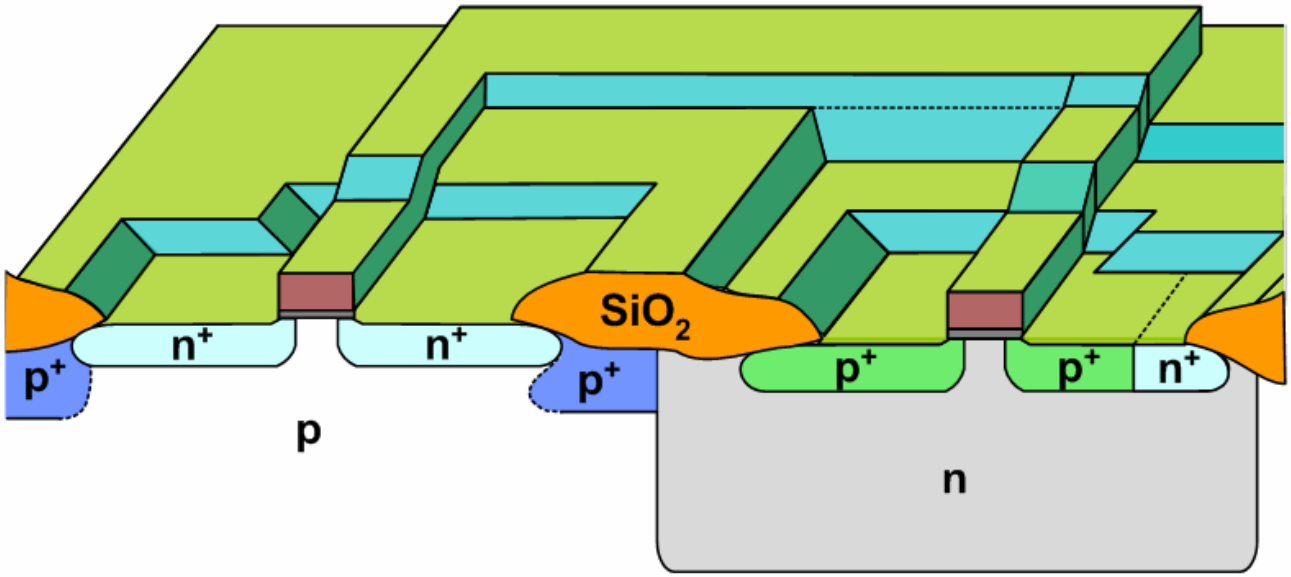
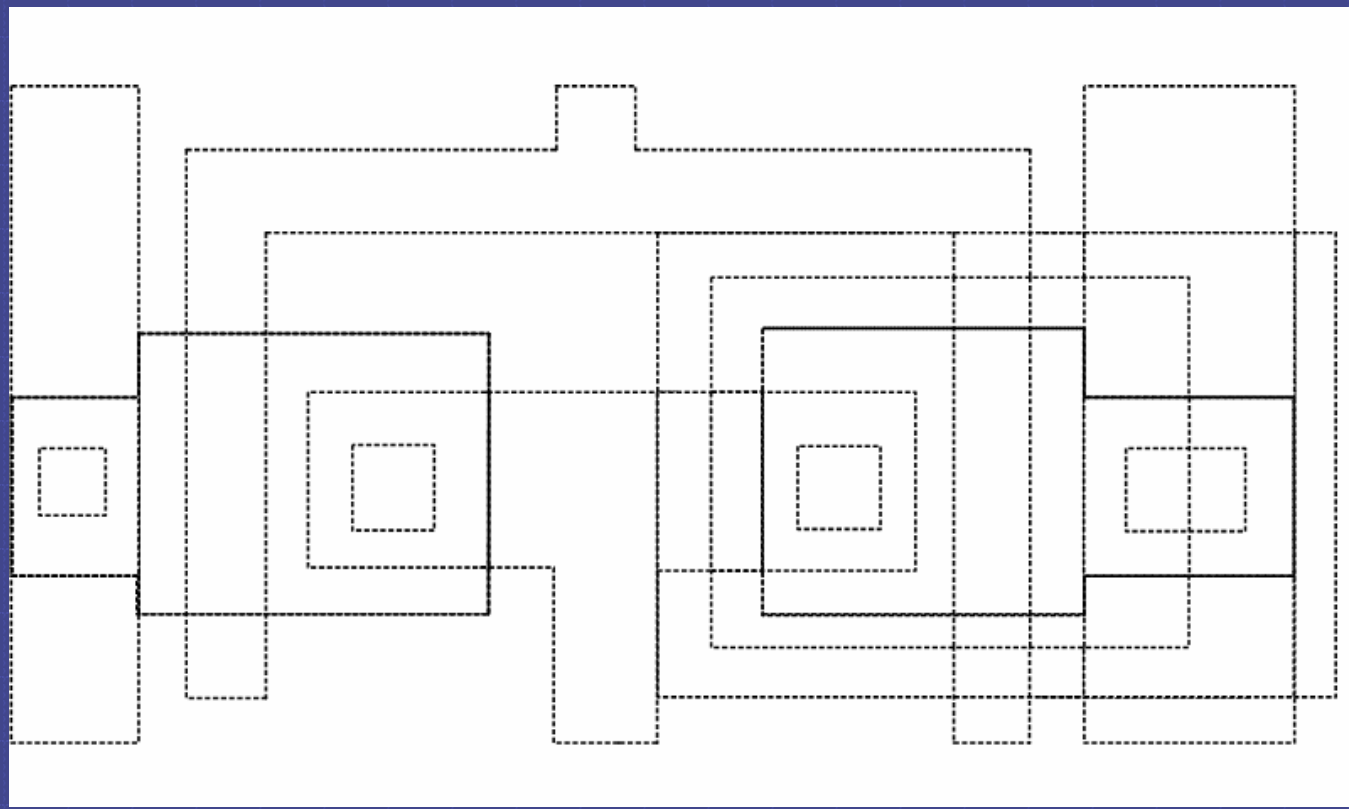


Figure 8: N^+ region in the n-well of the CMOS inverter. Edges of the drain region of the p-channel device and the n^+ region in the n-well (a) and cross-section of the inverter (b).

(a)



(b)

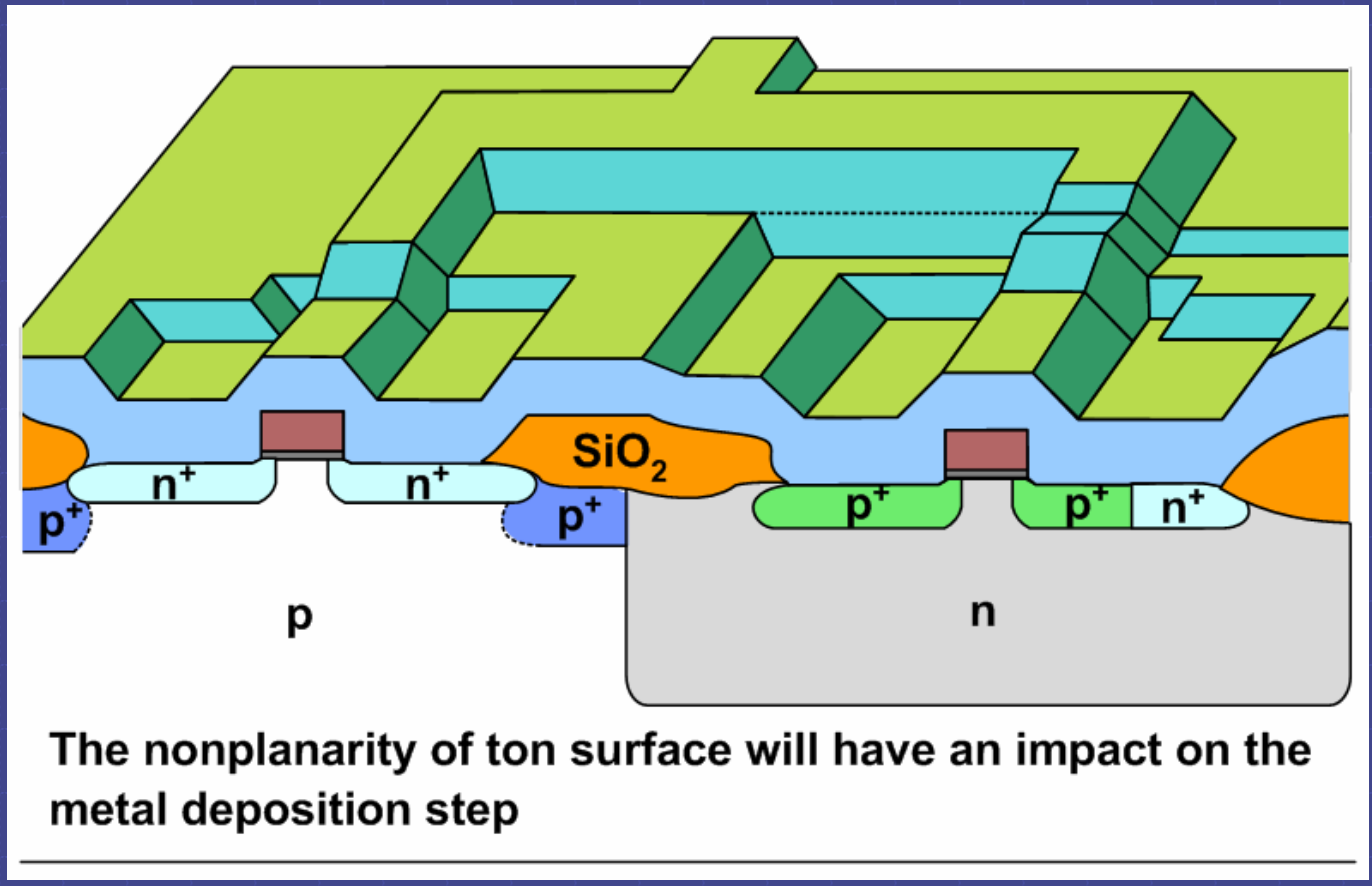
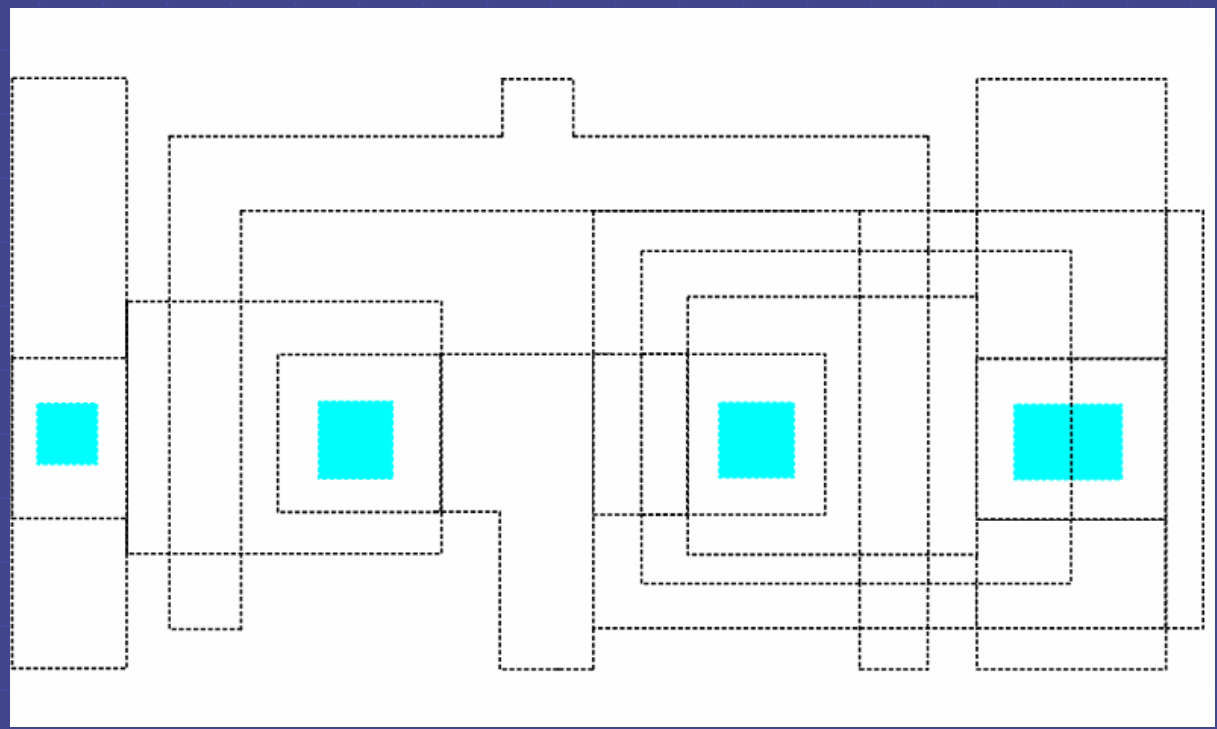


Figure 9: CVD deposition of SiO_2 in the n-well CMOS process. Layout (a) and cross-section of the inverter (b)

- in the source/drain areas or poly layers.
- contacts to poly must be made outside the gate region to avoid metal spikes through the poly and the thin gate oxide.

(a)



(b)

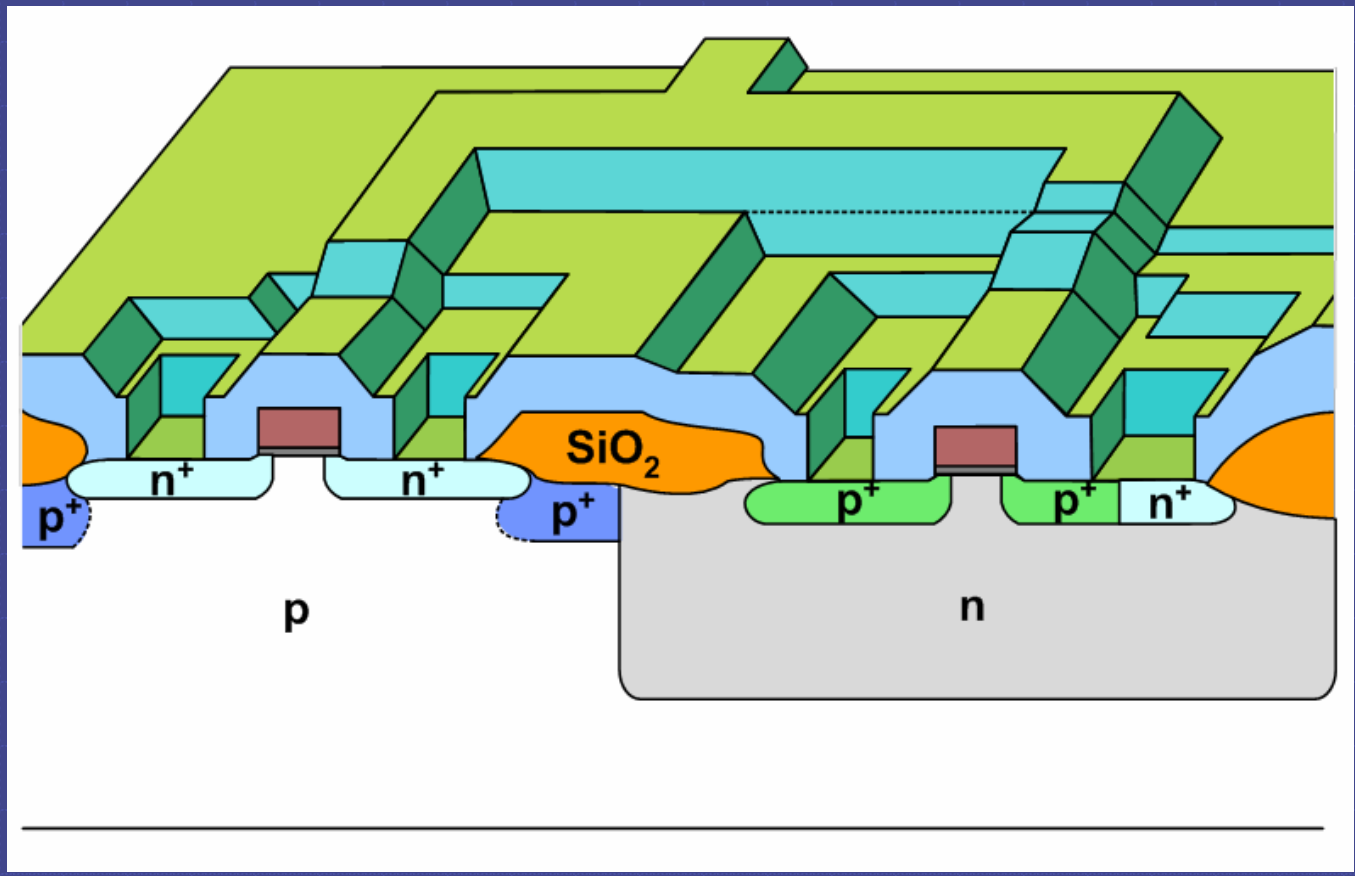
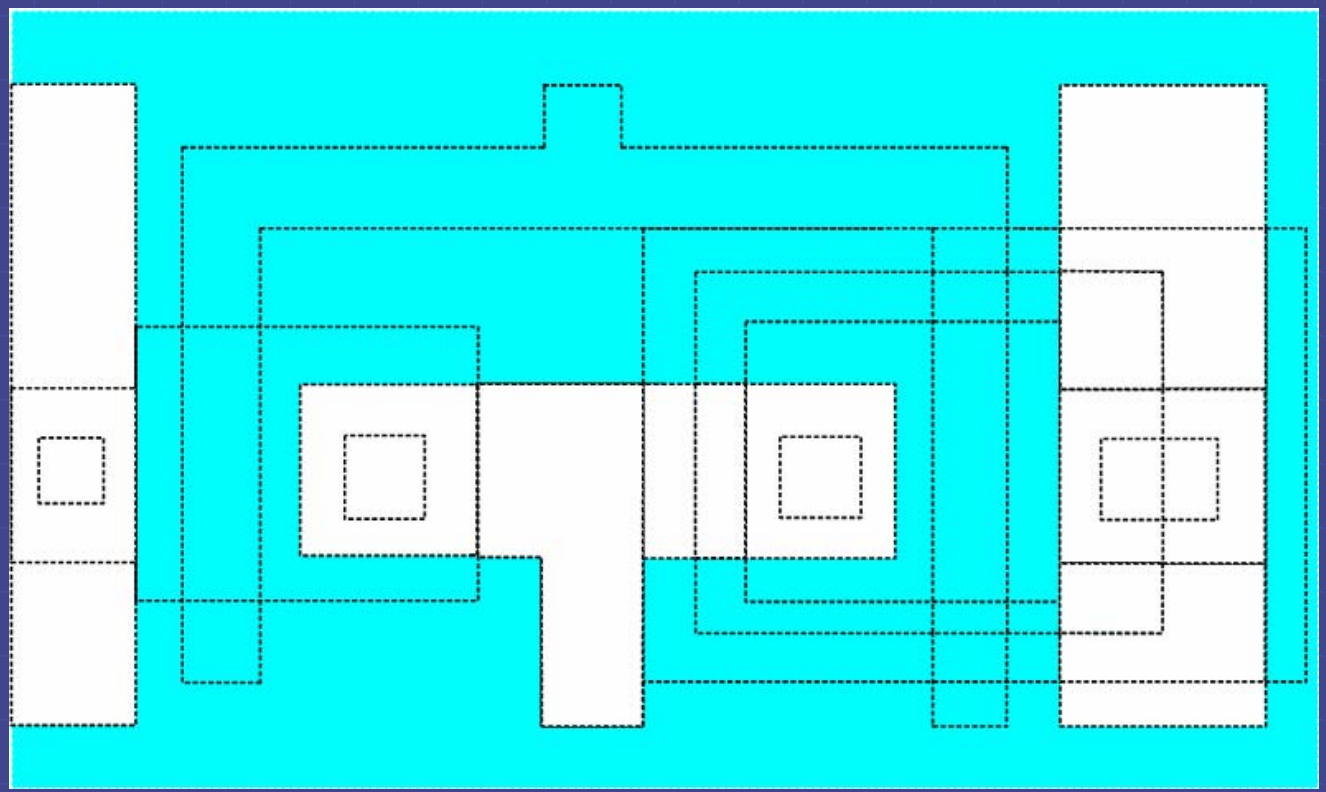


Figure 10: Contact cuts in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

- “Al” deposited over the entries wafer
- Step coverage is the most critical.
- undefined Al is removed.

(a)



(b)

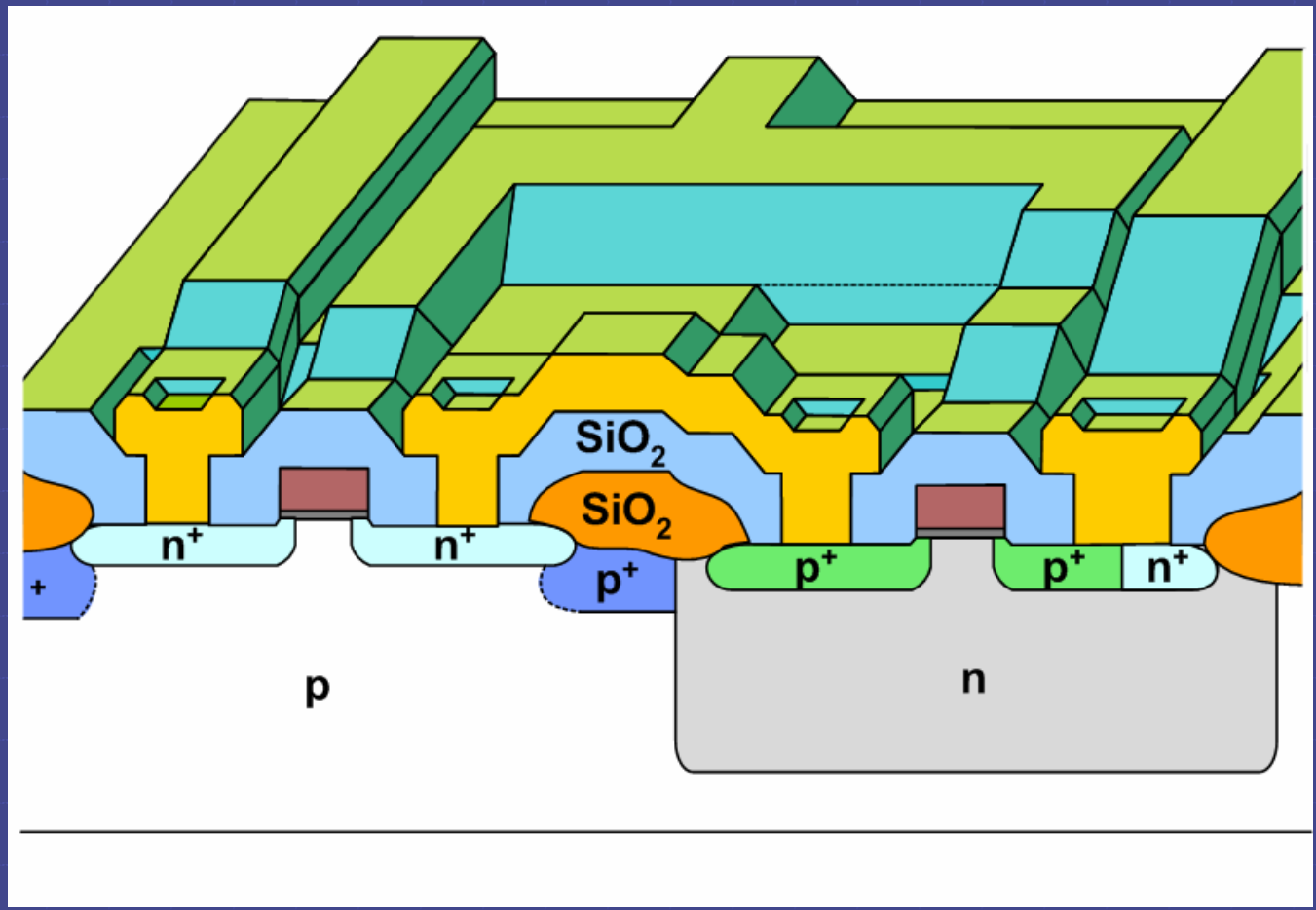
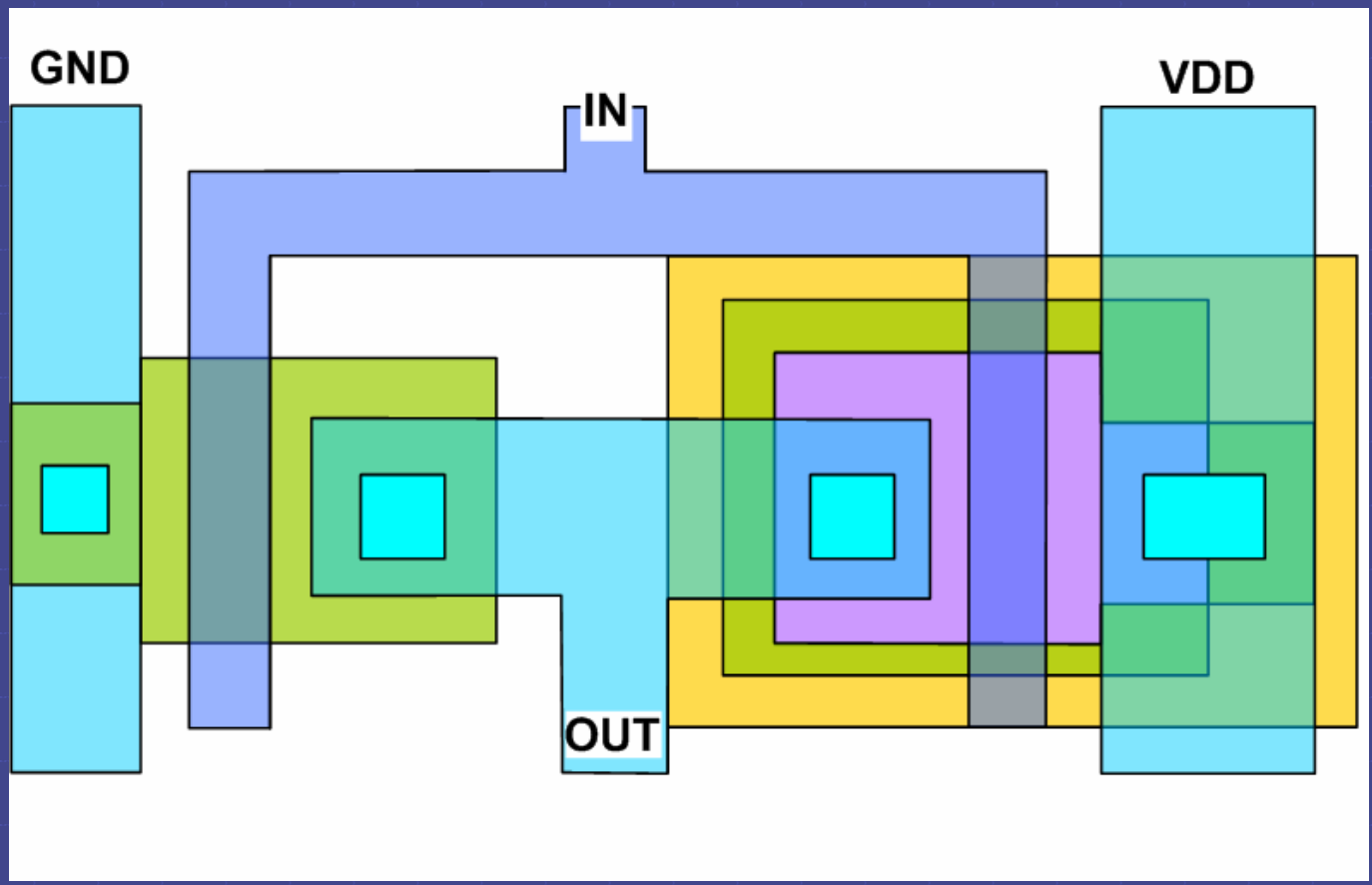


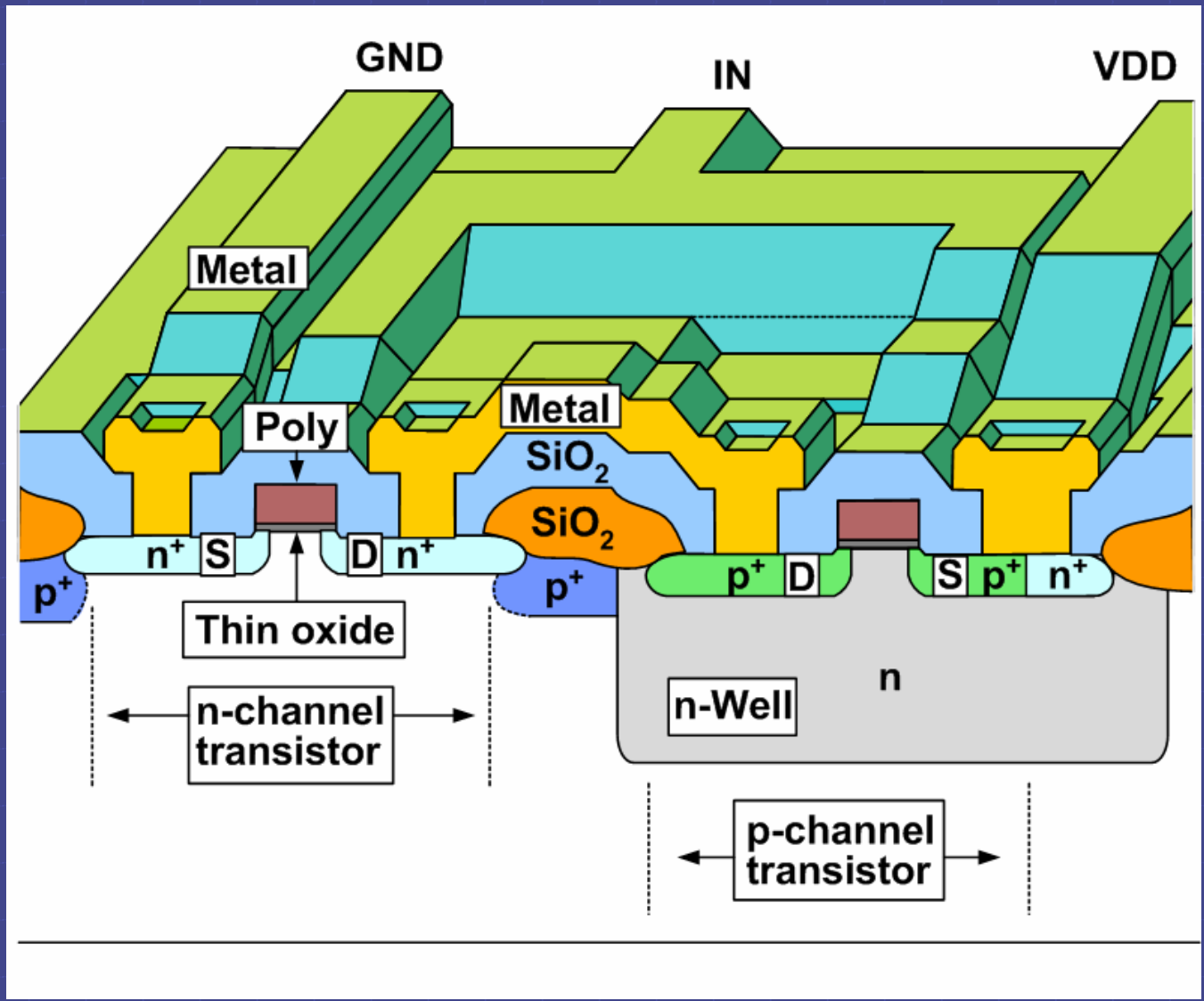
Figure 11: Metallization in the n –well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).

Final step: passivation glass to protect the surface from contaminants and scratches.

(a)



(b)


GND
IN
VDD
Metal
Poly
Metal
SiO_2
SiO_2
n^+
S
D
n^+
p^+
p^+
p^+
D
S
p^+
n^+
Thin oxide
n-channel transistor
n
n-Well
p-channel transistor

(c)

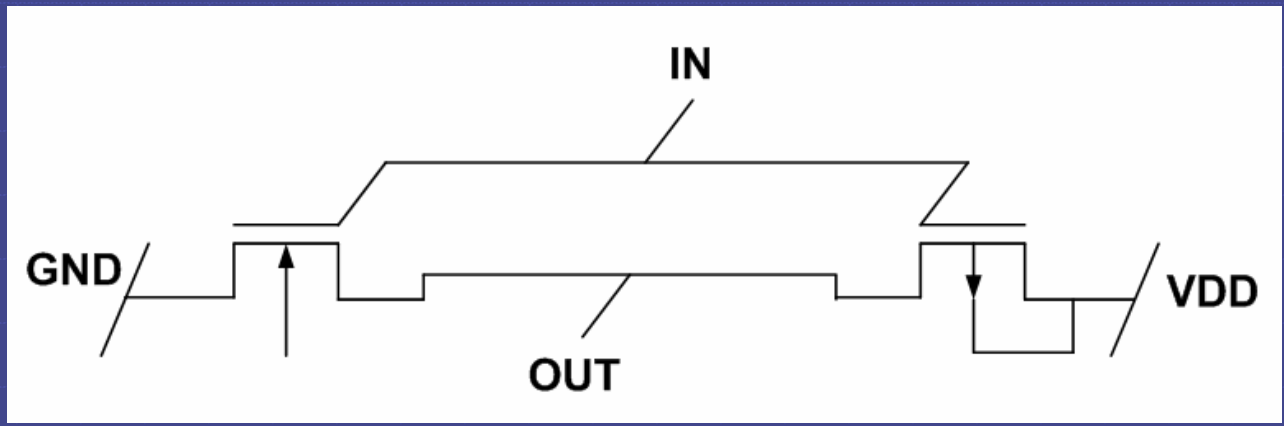
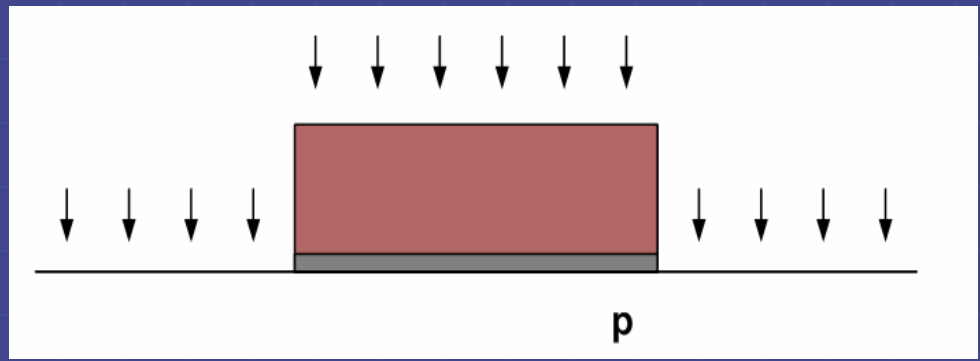


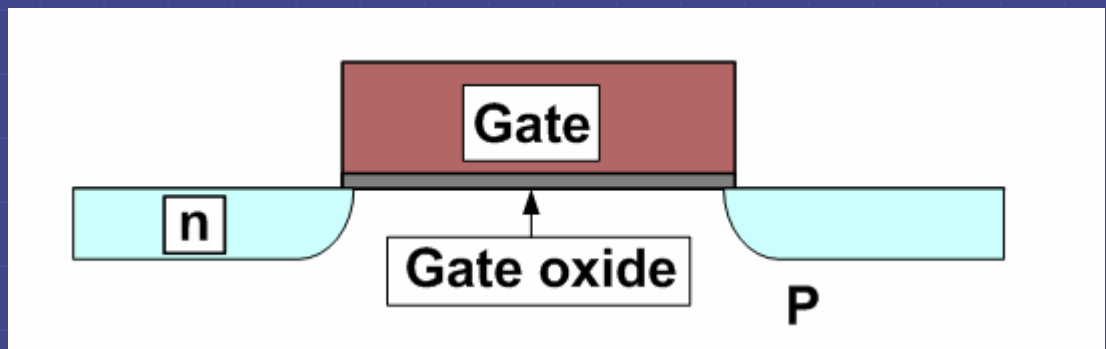
Figure 12: CMOS inverter. Composite layout (a), cross-section (b), and electrical diagram (c).

LDD allow very small transistor without suffering from “ hot electron “

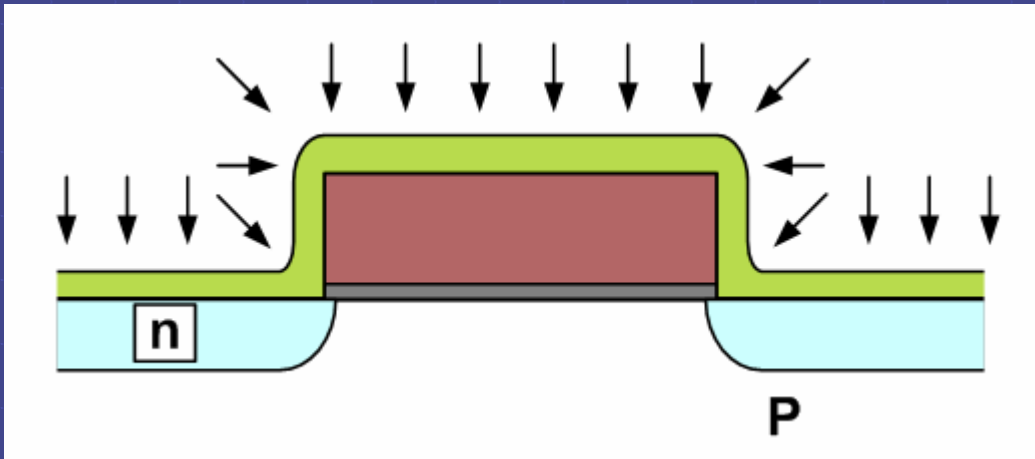
(a)



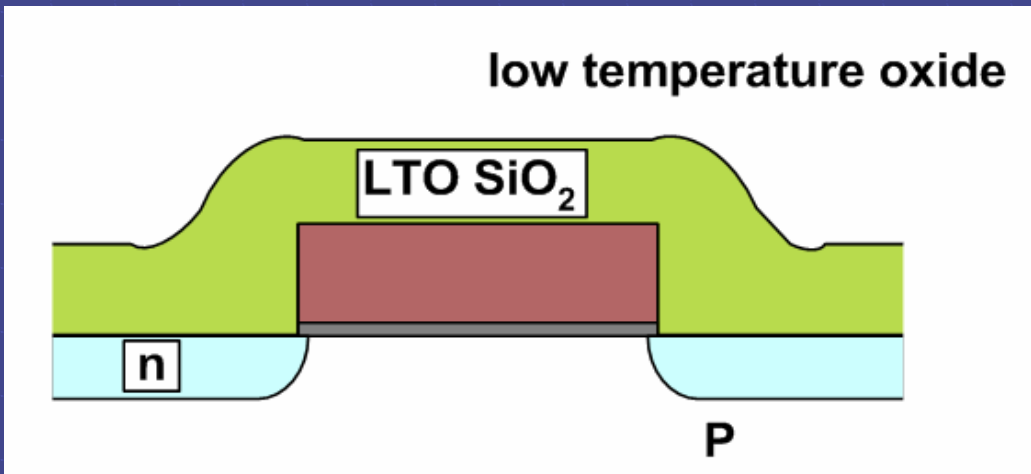
(b)

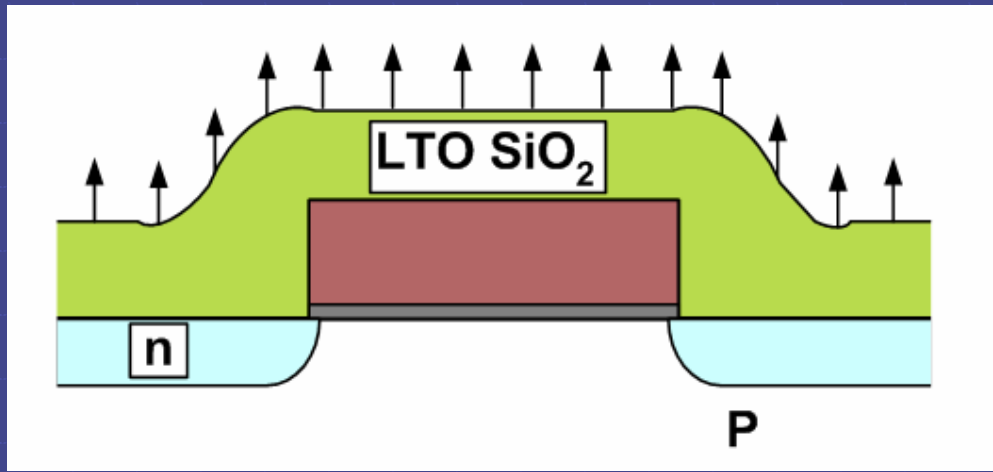


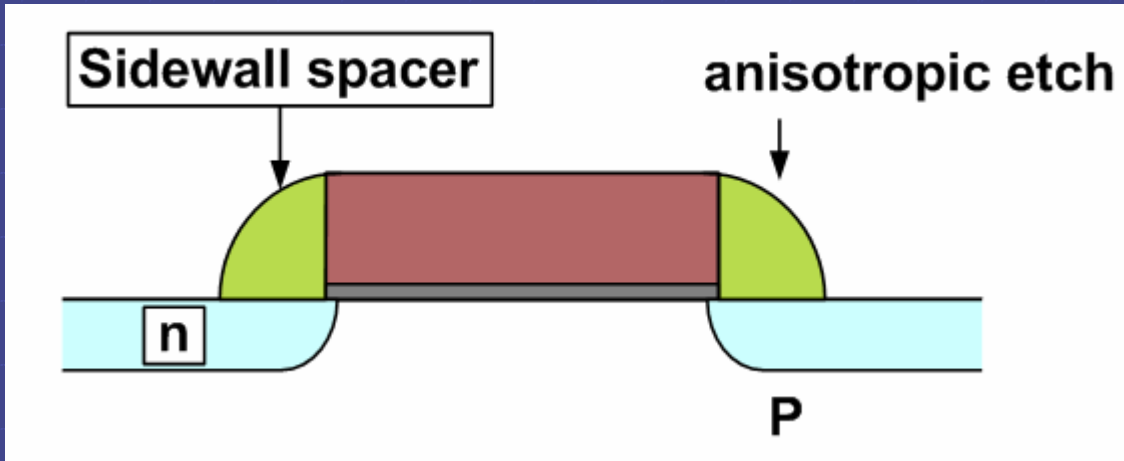
(c)

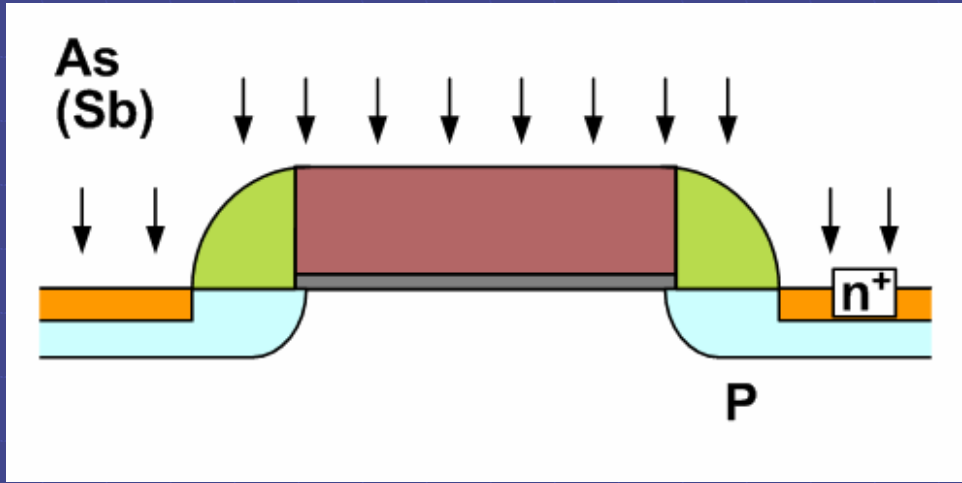


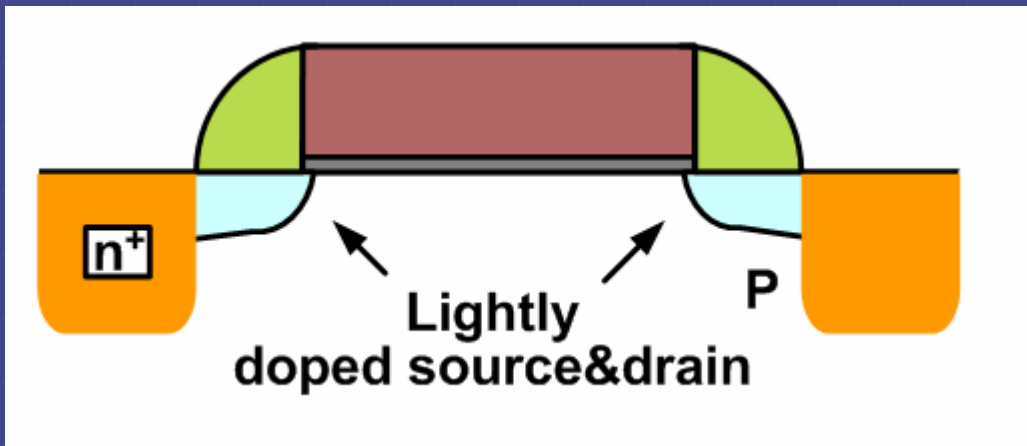
(d)



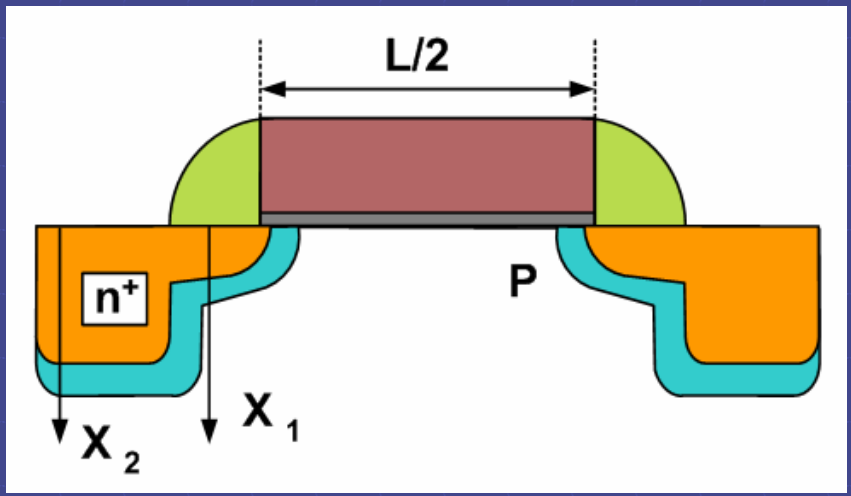

LTO SiO_2
n
P


Sidewall spacer
anisotropic etch
n
P


As
(Sb)
n+
P


n+
P
Lightly
doped source&drain

(i)



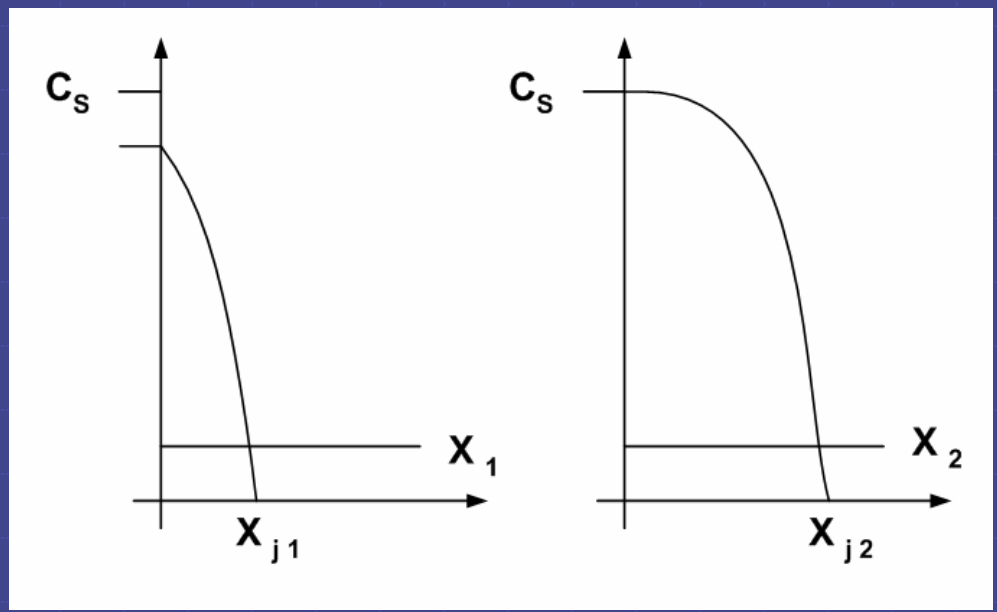


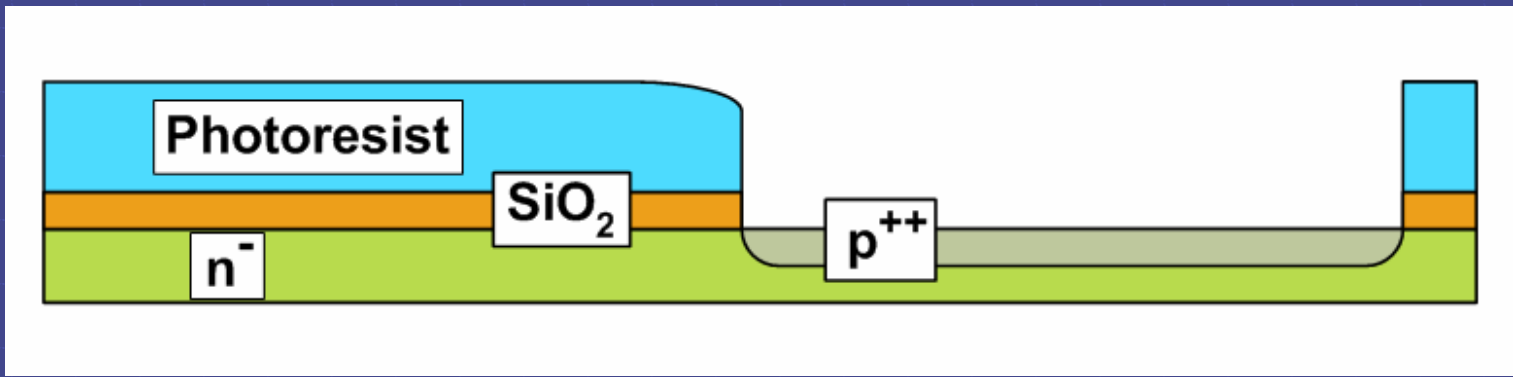
Figure 13: Formation of the LDD transistor structure

TWIN-Well CMOS PROCESS

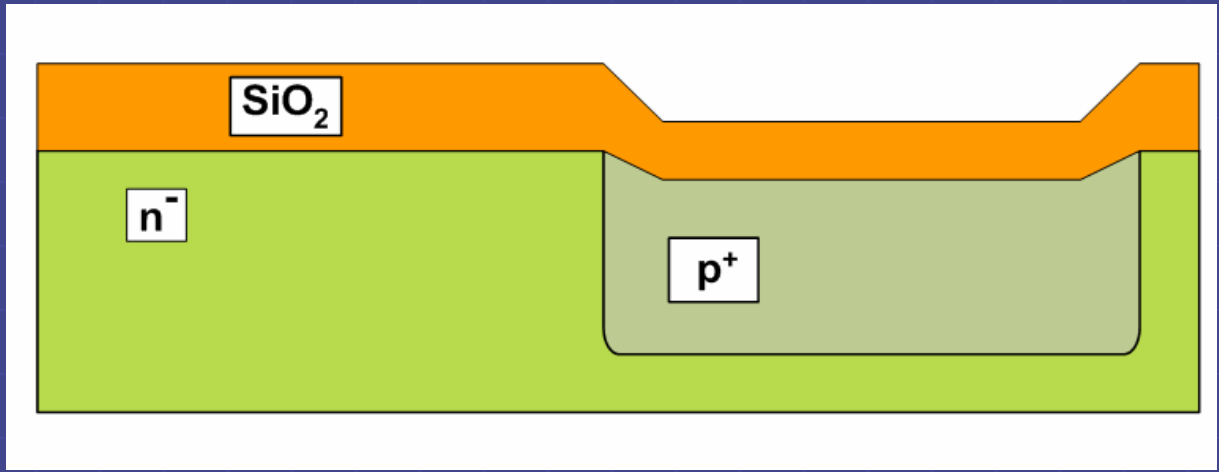
twin-well

- **allows independent control of the threshold voltage.**
- **keeps resistivity of the wells small.**

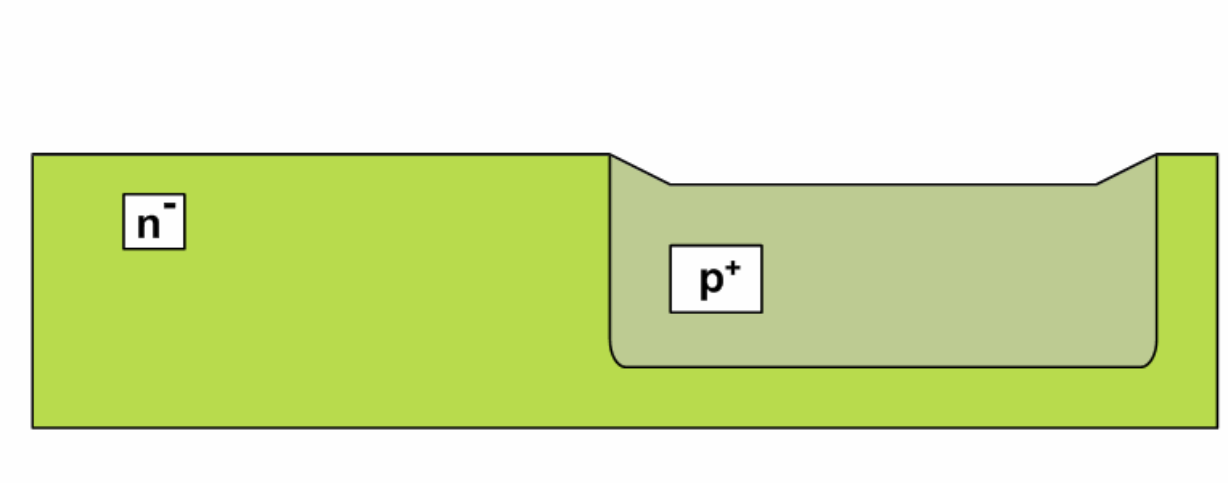
(a)



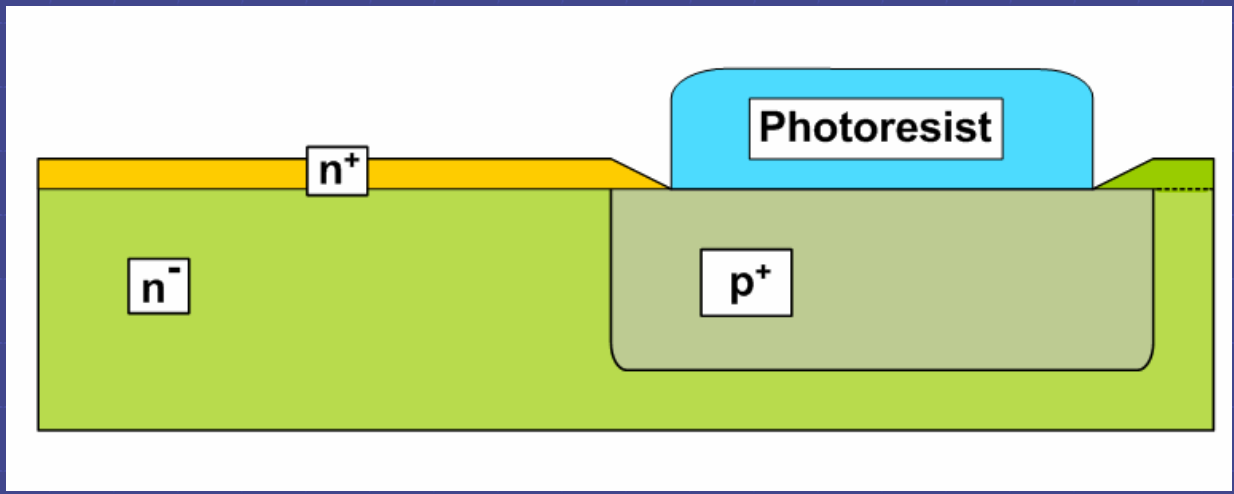
(b)



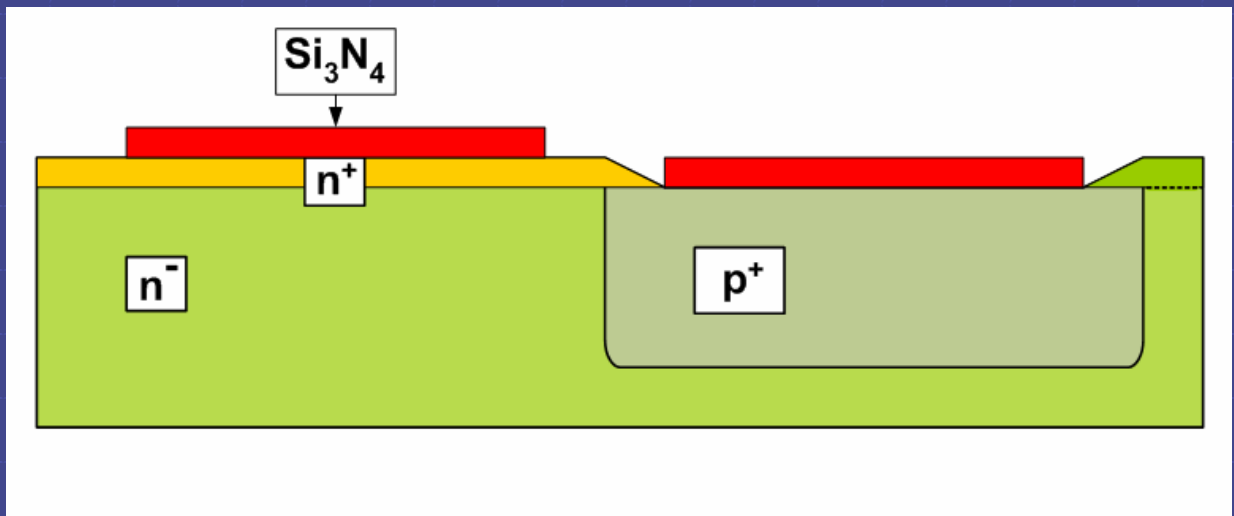
(c)



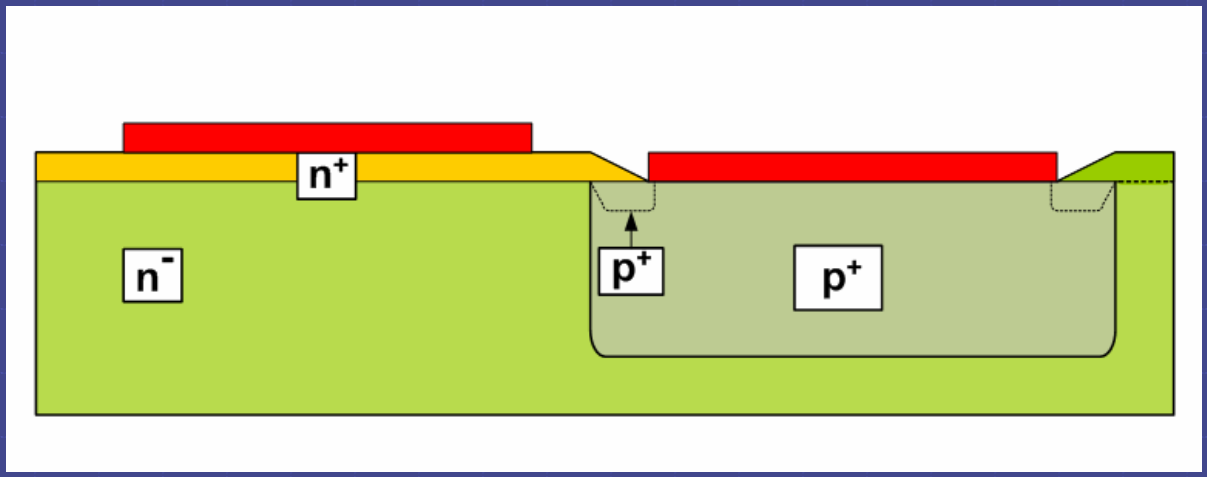
(d)



(e)



(f)



(g)

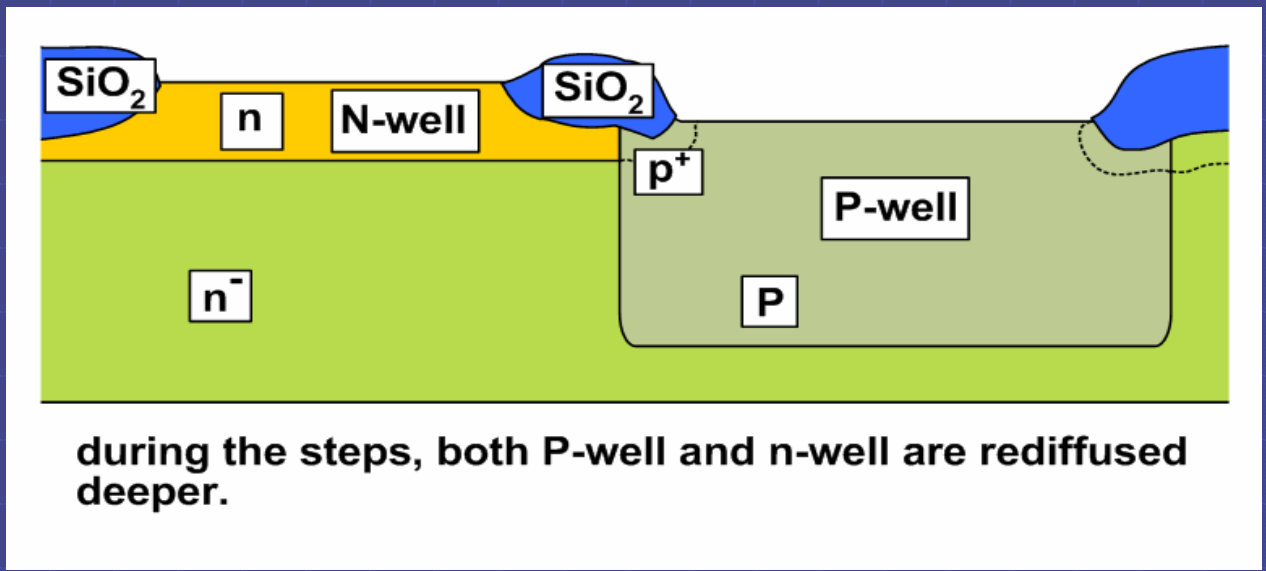
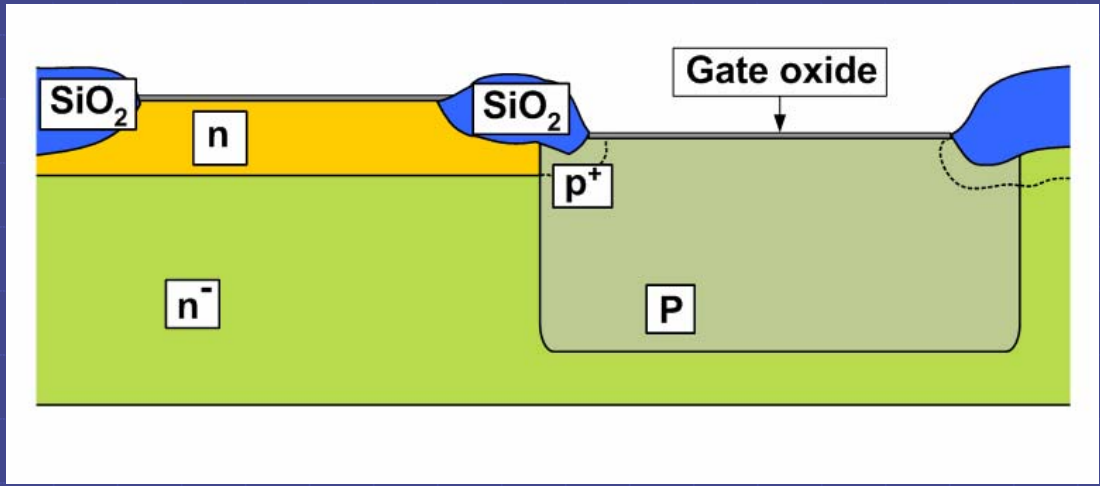
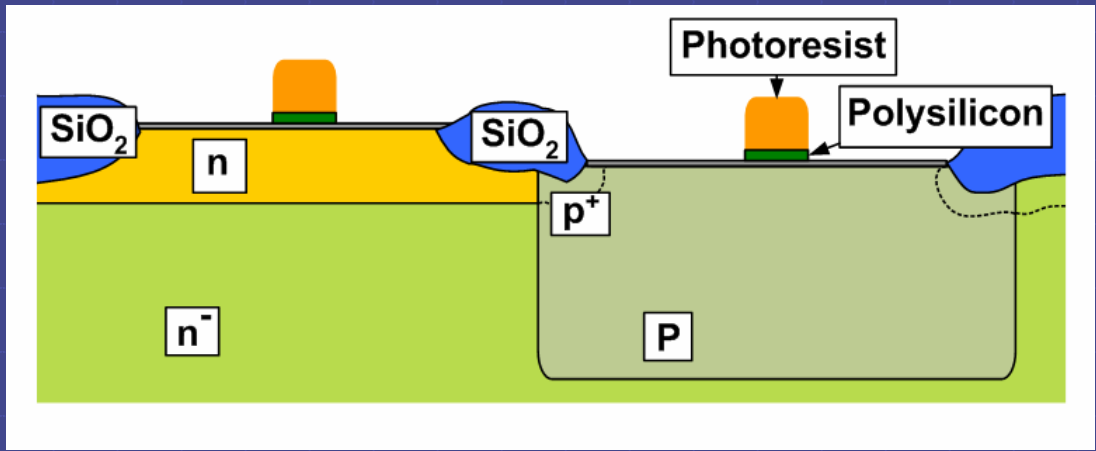
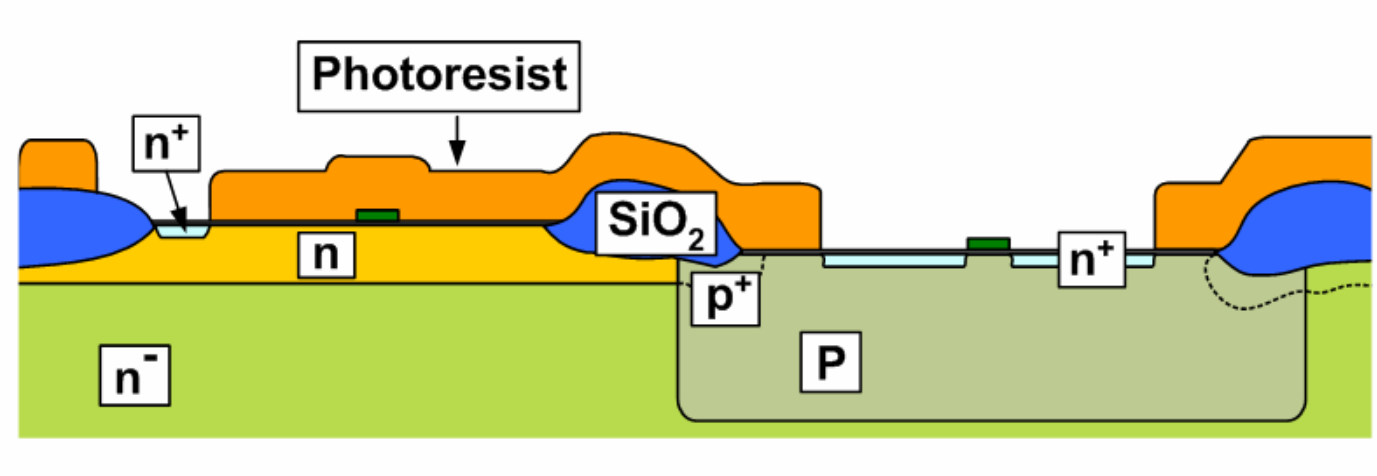


Figure 14: Advanced CMOS process. Part 1.

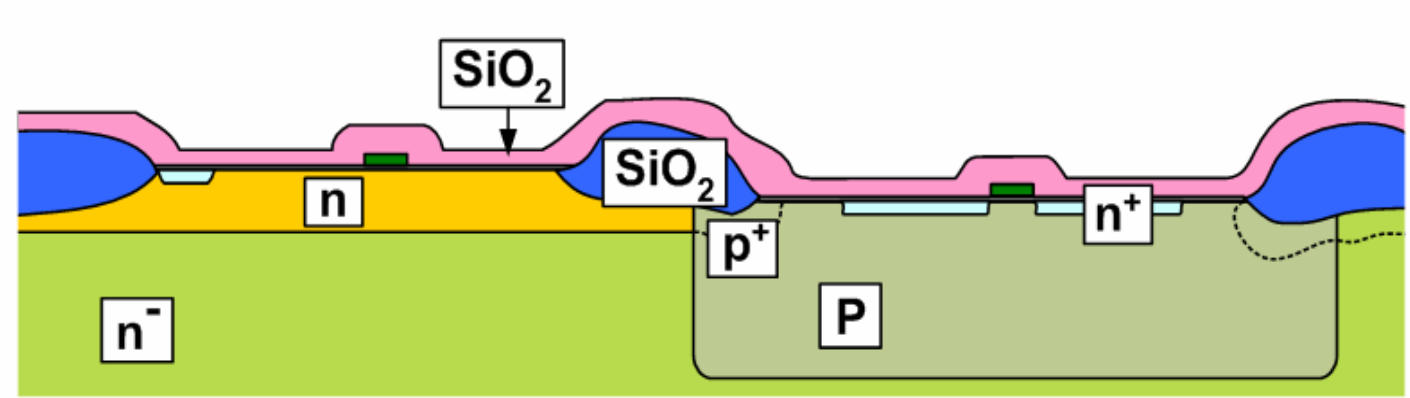

Gate oxide
SiO2
SiO2
n
p+
n-
P


Photoresist
Polysilicon
SiO2
SiO2
n
p+
n-
P

(c)



(d)



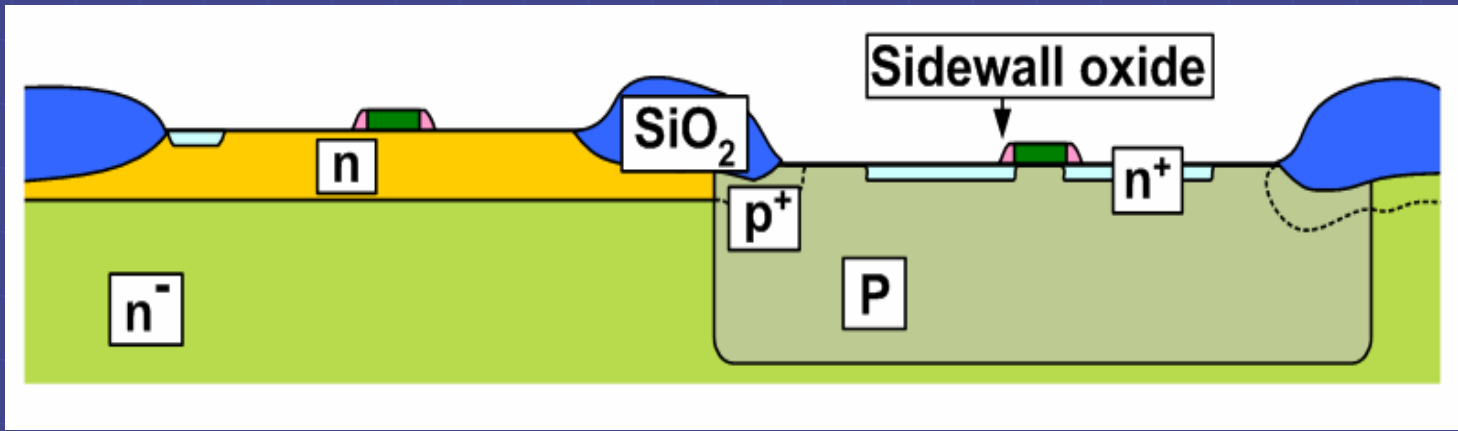
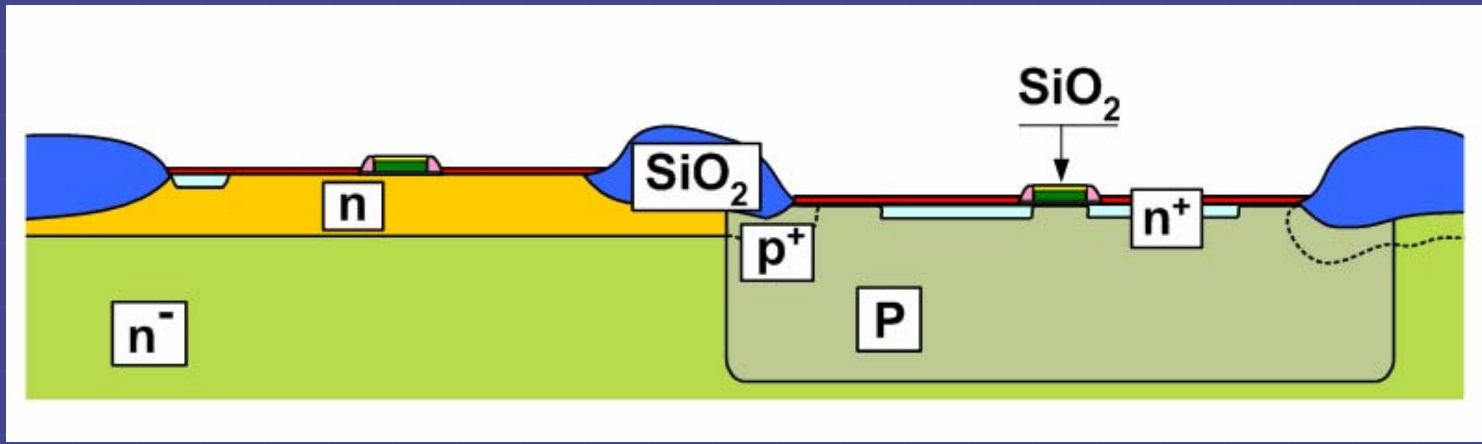
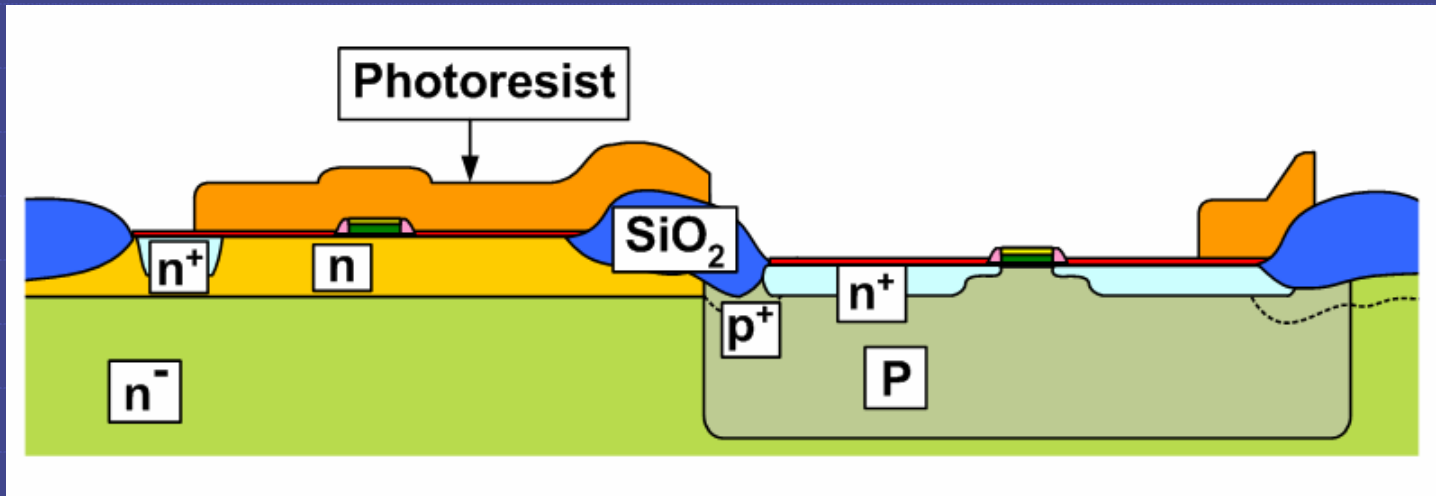
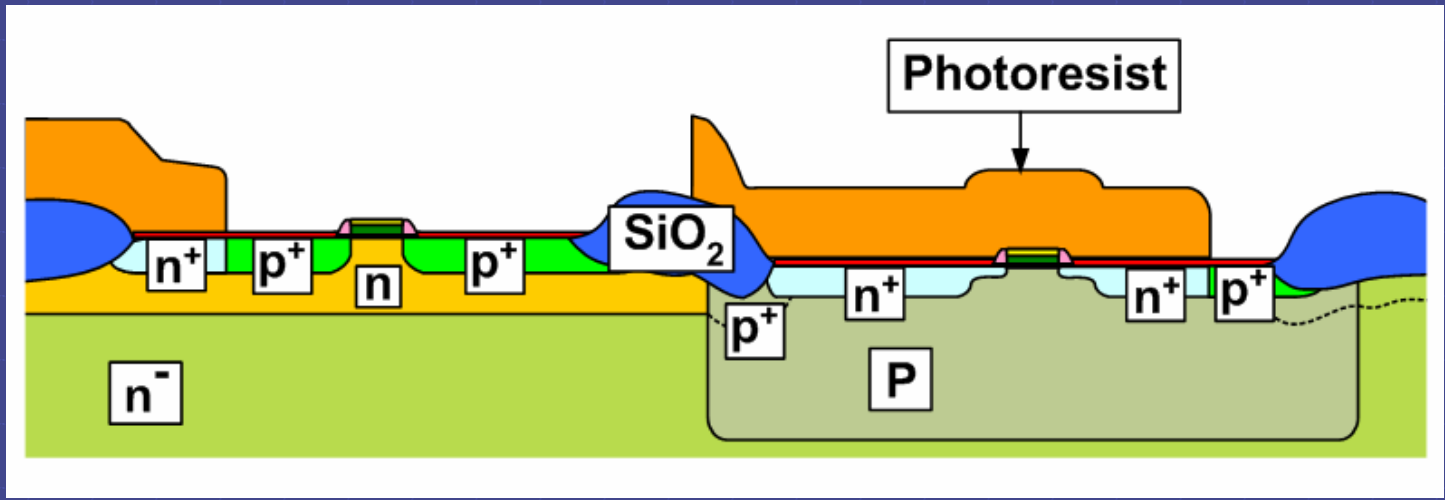


Figure 15: Advanced CMOS process. Part 2.


SiO2
SiO2
n
n+
p+
n-
P


Photoresist
SiO2
n+
n
n+
p+
n-
P

(c)



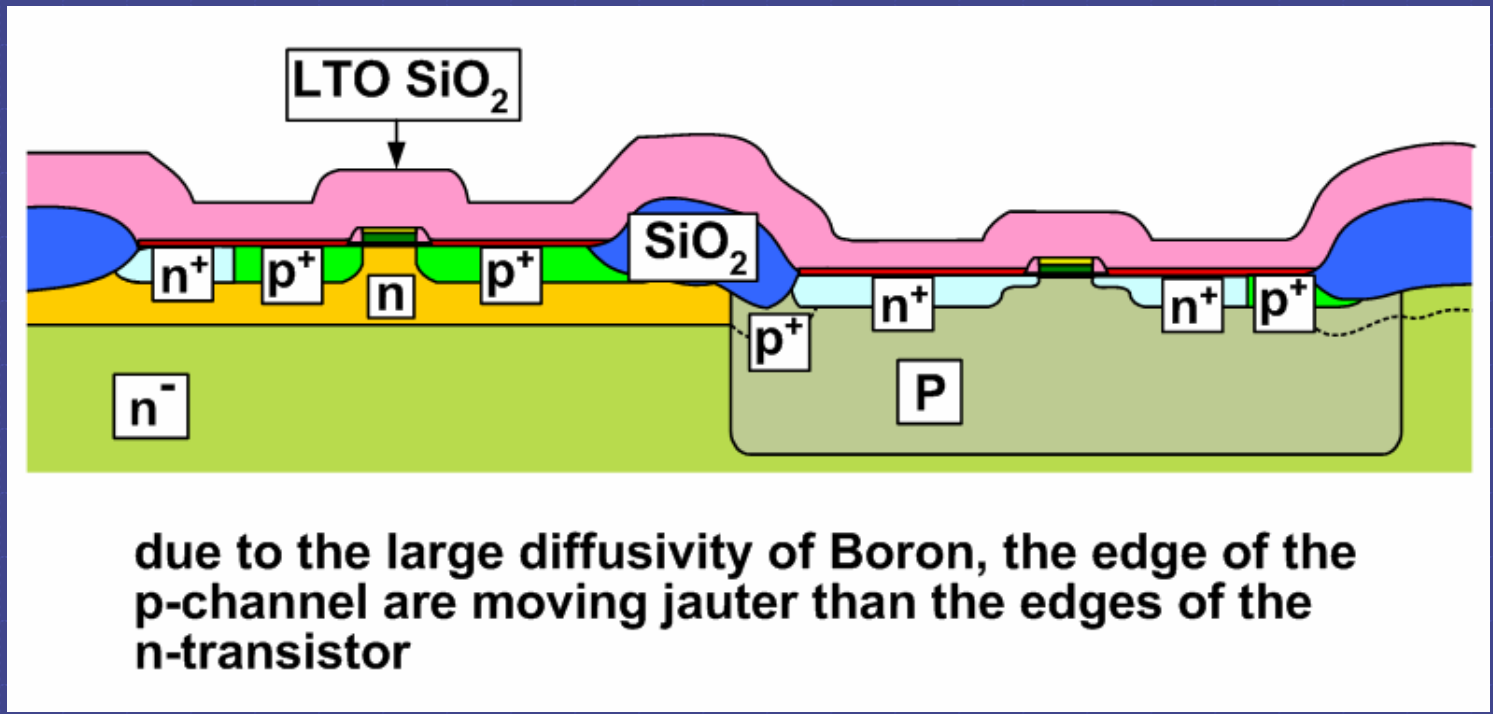
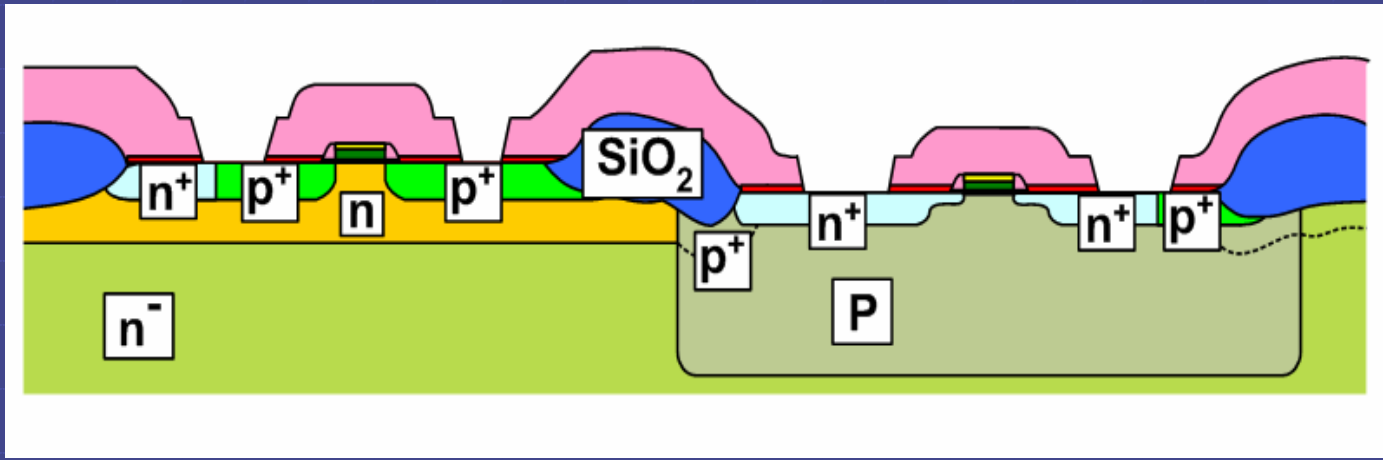
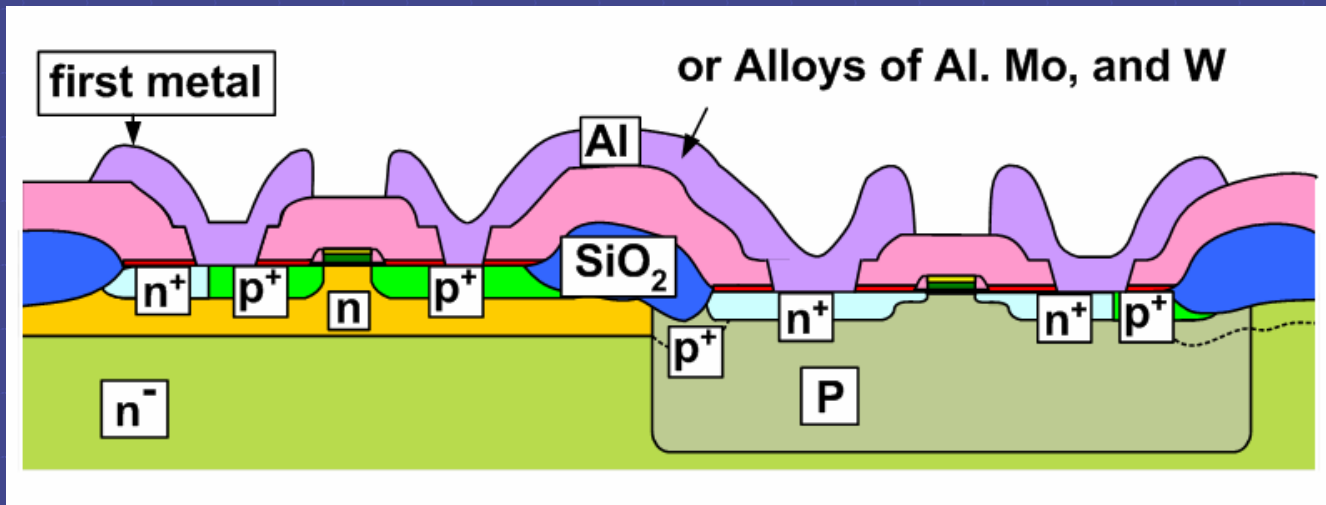


Figure 16: Advanced CMOS process. Part 3.


n+
p+
n
p+
SiO2
p+
n+
n+
p+
n-
P


first metal
or Alloys of Al. Mo, and W
Al
n+
p+
n
p+
SiO2
p+
n+
n+
p+
n-
P

(c)

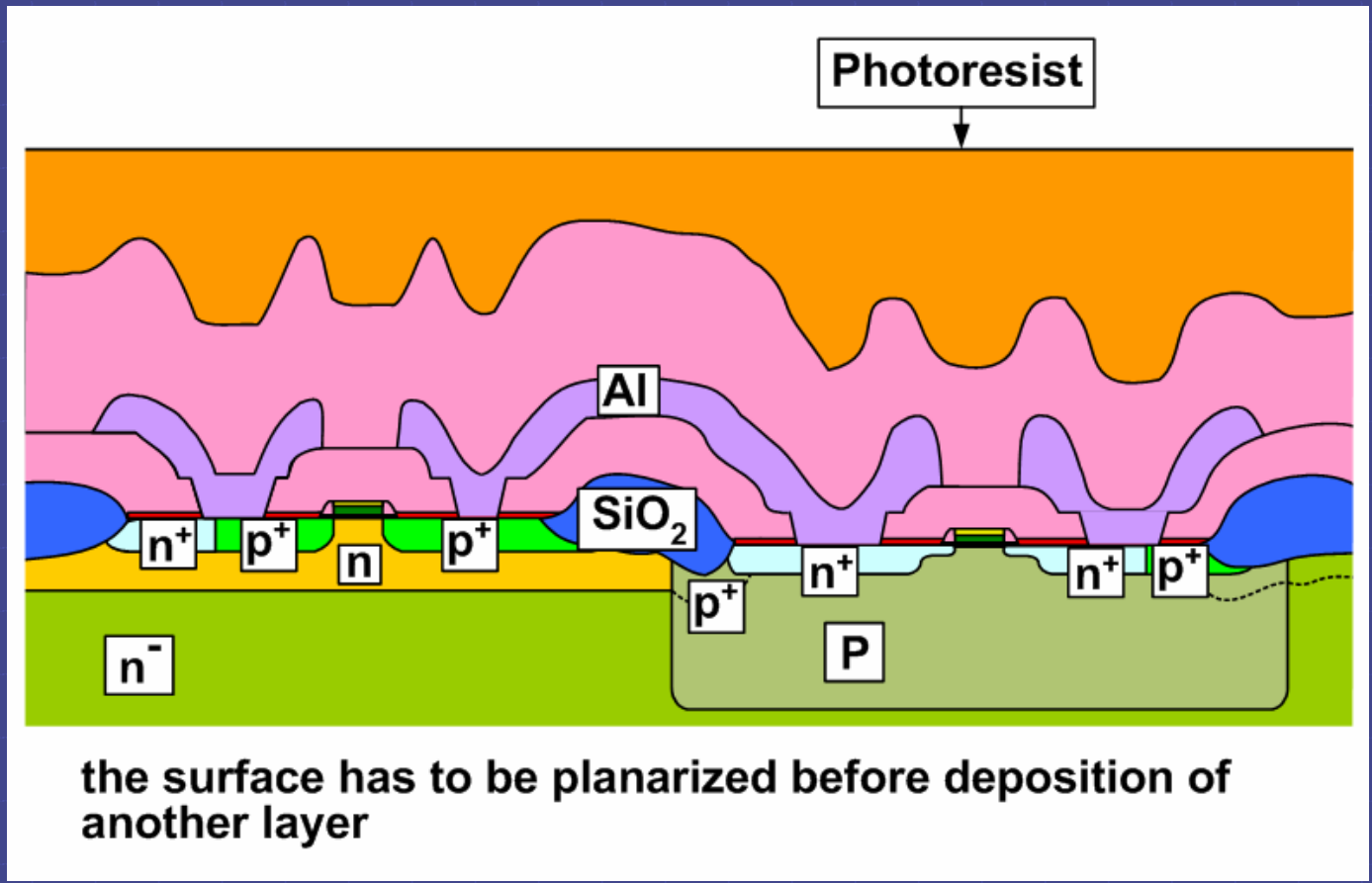
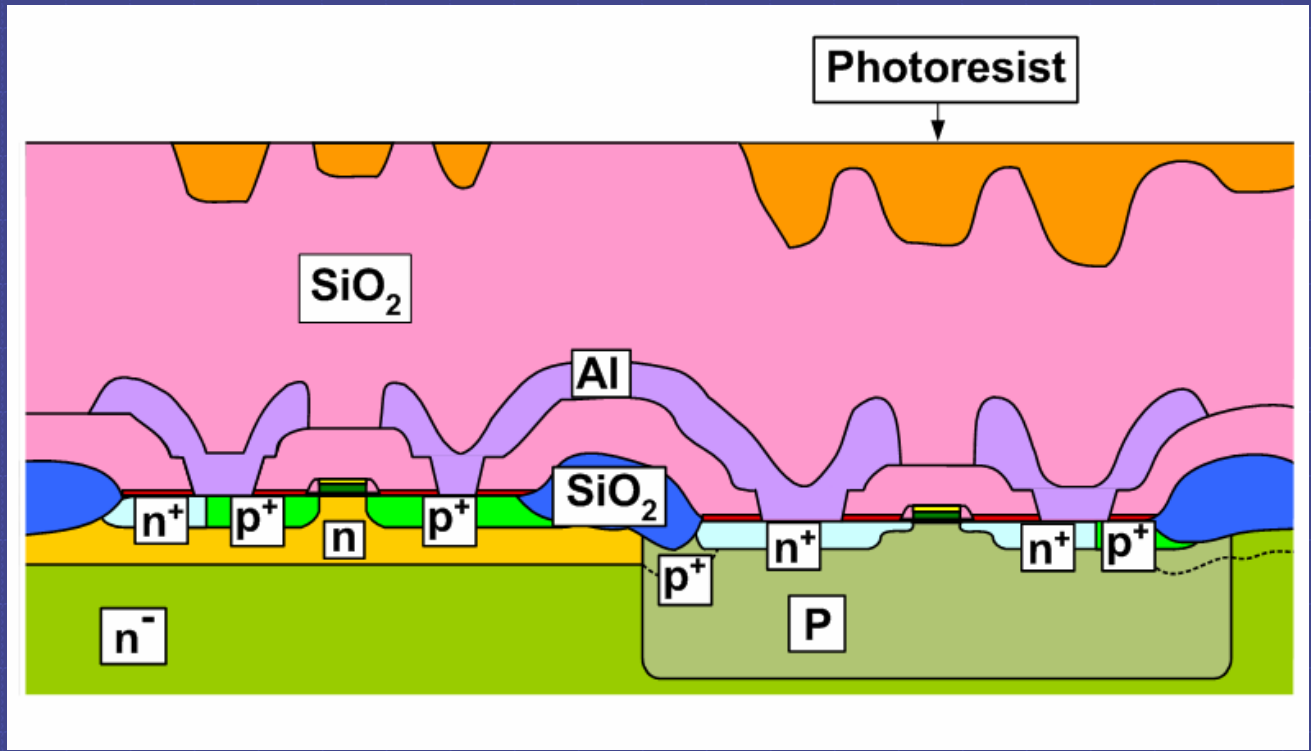
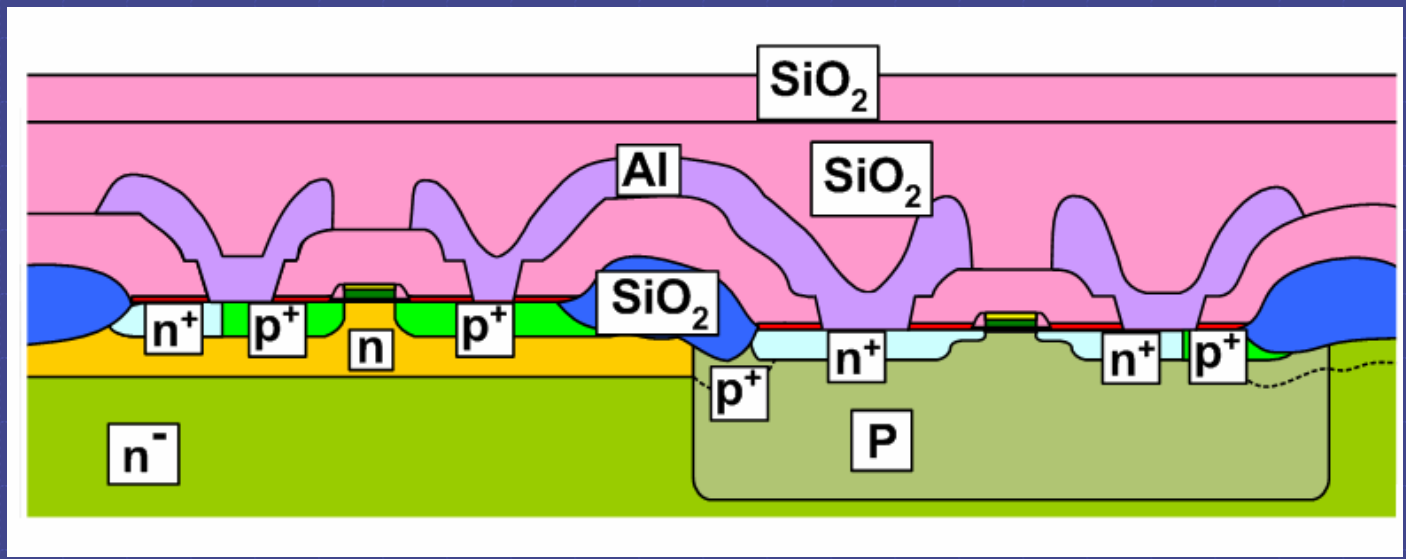


Figure 17: Advanced CMOS process. Part 4.

etched with a soltion that has the same etching rate for photoresistor & oxide

(a)




SiO2
Al
SiO2
SiO2
n+
p+
n
p+
p+
n+
n+
p+
n-
P

(c)

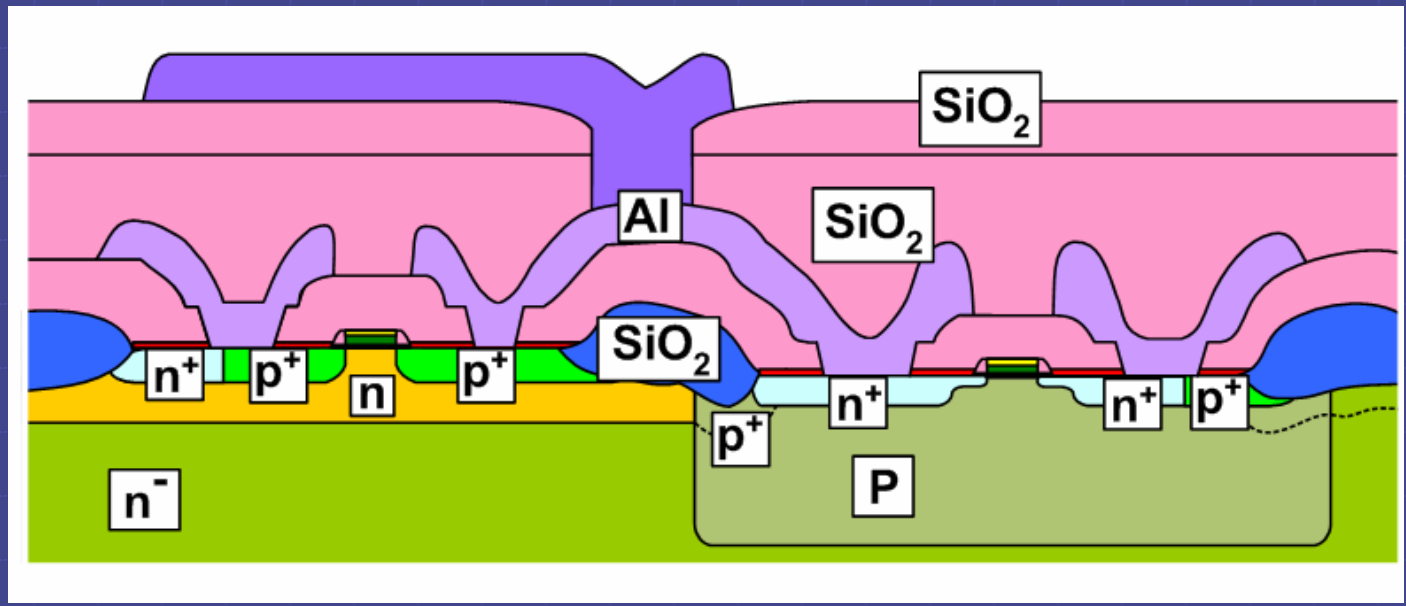


Figure 18: Advanced CMOS process. Part 5.

- two layer method, high quality due to planarization step
- LDD:NMOS preventing hot-electron phenomena
- optimal threshold voltage both PMOS & NMOS through twin-well
- good latch-up protection by minimizing, the lateral voltage drops inside the wells

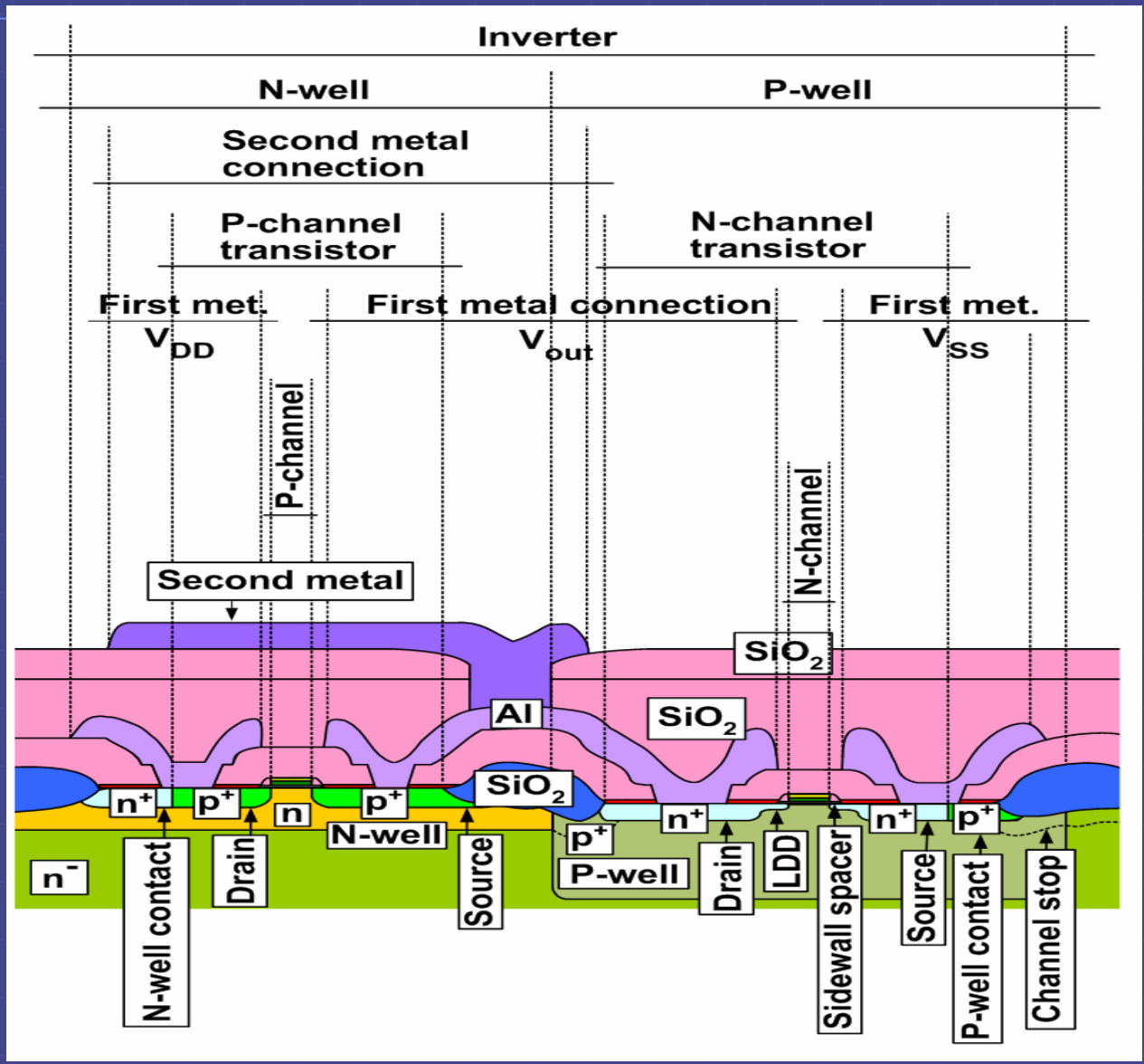


Figure 19: Summary of basic features.