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# CMOS single-ended-to-differential low-noise amplifier

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ABSTRACT

In this work, a low-power single-ended-to-differential low-noise amplifier (LNA) is reported. The circuit has been designed and optimized to be included in an IEEE 802.15.4 standard receiver. In order to minimize power consumption, active loads and currents mirrors have been replaced by optimized inductors and transformers. Moreover, an exhaustive study of the mixed-mode parameters has been carried out, enabling the definition of single-ended figures of merits in terms of mixed-mode *S*-parameters. The LNA has been implemented using a 0.35 μm RFCMOS technology. Performances are a noise figure of 4.3 dB, a power gain of 21 dB, and a phase balance of $180 \pm 1^{\circ}$. Regarding non-linear behaviour, the obtained 1 dB-compression point obtained is −9.5 dB m while intermodulation intercept point is −3 dB m, dissipating 6 mA from 1.5 V supply voltage.



## 1. Introduction

Low-noise amplifiers (LNA) are one of the key components in receivers because it tends to dominate the sensitivity and noise figure (NF) of the whole system [1]. This sensitivity is directly related to both active and passive devices available in a given technology. Thus the chosen technology will have a high impact on the final specs that could be achievable. However, the specifications of the communication standard and product cost as well as small size, level of integration, power consumption are additional constraints that will complicate the technology selection process. Actually, in high performance applications, LNA noise figures below 2 dB have been demonstrated [2–4] using integrated technologies such as SiGe, GaAs or improved CMOS (micromachining, SOI, etc.).

Nonetheless there are applications where the system specifications are relaxed, e.g. in wireless sensor networks, enabling the use of conventional CMOS processes. The LNA proposed in this work is a part of the RF front-end receiver of a reduced functional device (RFD) intended to work in compliance with the IEEE 802.15.4 low-frequency band (European 868–868.6 MHz) [5]. The key characteristic of the standard is its protocol simplicity and flexibility providing a reliable data transfer in a short-range operation (typically within a range of 10 m). A summary of the most important specifications of the standard is shown in Table 1.

Due to the final application, i.e. a wireless sensor network, the RFD units must be tiny, consume a small amount of power, and have a very low final cost. Taking into account such constraints, RFCMOS 0.35 μm is a good technology option for the implementation of a complete transceiver of the RFD unit.

Once the framework, has been established, the designer must face three challenges. First, the choice of communication system architecture will have a strong influence on the possible circuit topologies of the LNA for achieving the specifications of the standard. Second, the designer should identify and apply the best design methodologies and strategies for archiving a low-voltage low-power (LVLP) circuit. And third, once the technology has been fixed, the LNA performance depends strongly on the quality of the passives components; therefore, the designer has to be able to evaluate their behaviour using full-wave electromagnetic simulators.

In this work, the selected transceiver architecture uses one single-ended antenna for both transmission and reception paths that are split using an external switch, as shown in Fig. 1. To minimize the effects of the common-mode noise, e.g. digital switching noise, the received signal must be processed differentially. Therefore, this assumption points out the need of a single-ended-to-differential LNA design. Commonly, out of chip passive BalUn has been used to convert single-ended signals to differential signals. Unfortunately, it introduces losses increasing the system noise figure. To avoid these mentioned drawbacks, an active topology is preferred in this work. Moreover, to compensate the dynamic range of the complete system without increasing the total power consumption, a fully differential variable gain amplifier has been connected to LNA output. With this selected architecture, the system specifications are translated into the LNA block as a maximum NF of 7 dB, a minimum gain of 18 dB, and an input intercept point to the third harmonic (IIP3) of −10 dB m.

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**Table 1**
IEEE 802.15.4 standard specifications.

| Quantity | Value |
|---|---|
| Sensitivity | −92 dB m |
| BER | $6.25 \times 10^{-5}$ |
| Max. power input | −20 dB m |
| Channel bandwidth | 600 kHz |

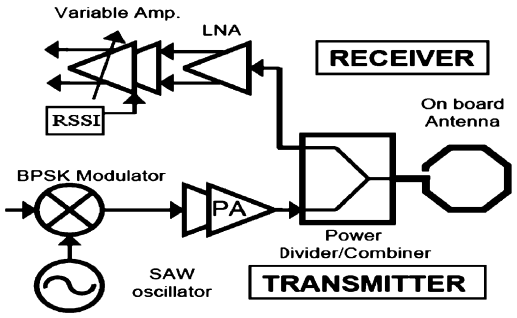


**Fig. 1.** Input and output stage of the transceiver.

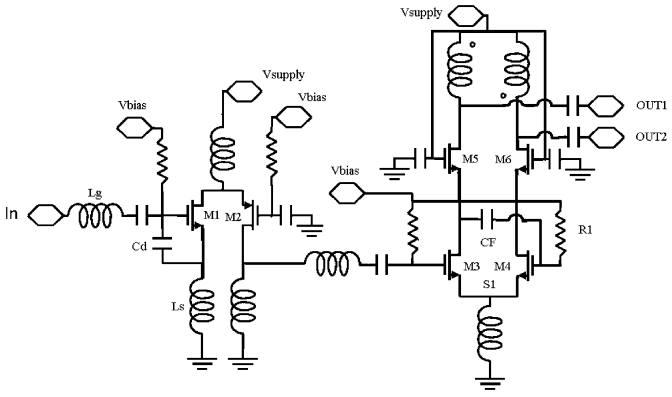


**Fig. 2.** Schematic of a single-ended-to-differential low-noise amplifier.

Of course, the LNA must dissipate a lower current consumption. In order to accomplish this last request, the supply voltage has been reduced to 1.5 V, considerably lower than typical value of 3.3 V for a 0.35 μm technology where nominal threshold voltages are around 0.5 V. This voltage reduction supposes a clear penalty for the designer who has to reduce the possible number of stacked transistor, with the corresponding reduction of some of the basics LNA performance, e.g., gain, NF, or reverse isolation, among others. To avoid this drawback, for the first time the substitution of resistive or active loads, as well as current mirrors by optimized on-chip inductors and transformers [6] is proposed. Considering this framework, RFCMOS accurate models for such inductors and transformers are not always available. Therefore, the designer has to be able to evaluate the performance of these integrated passive using full-wave electromagnetic simulators, particularly if layout optimization techniques are used. This disadvantage becomes a benefit, due to the fact that the designer can obtain the best component for each application. In the work presented hereafter, the benefits translate in achieving the best resonance tank for a specific frequency, the exact inductance value and the higher quality factor Q for a degeneration inductor beyond the inductor library supplied by the foundry manufacturer. Moreover, each inductance of the LNA has been designed to obtain the best performance depending on its specific application, i.e., as a load, RF chock, AC current source, input/output matching or source degeneration. It is the use of the optimizing components [7] that allows complete monolithic integration of a compliance solution.

The schematic of the proposed LNA is shown in Fig. 2. The first stage is based on a folded cascode topology [8] that allows a low-power dissipation using a low-voltage supply. It will be explained in Section 2 using power constraint simultaneous noise and input-matching impedance design technique (PCSNIM). The second stage is a differential cascode structure that supports the single-ended-to-differential conversion [9]. Therefore, Section 3 establishes the formalism to study three-port amplifiers, and will analyse the designed active BalUn. In Section 4, the LNA characterization is presented, where measurements are compared with simulations. Finally, Section 5 gives the conclusions of the work.

## 2. First stage: single-ended LNA

The key point in the design of a LNA consists in the determination of suitable tradeoffs between the different circuit specs such as NF, gain, linearity, impedance matching, and power dissipation. Over the years, there have appeared several design techniques for optimizing such tradeoffs. To name a few representatives, one can find the classical noise matching (CNM) technique, the simultaneous noise and input matching (SNIM) at any specified amount of power dissipation technique, the power-constrained noise optimization (PCNO) technique, and the PCSNIM technique [10].

For the design of the first stage, the PCSNIM has been selected. The PCSNIM basically consist in SNIM, but the topology includes a feedback capacitor $C_d$ in addition to the well-known source degeneration inductor $L_S$. This is shown in Fig. 3 where a folded cascode topology is presented in detail. The inclusion of the feedback capacitor adds a new degree of freedom that allows the inclusion of the power constraint in the design. As it has been reported in [10], the LNA performance parameters are given by

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}} + j\left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left(\frac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right)} - sL_S \tag{1}$$

$$F_{\min} = 1 + \frac{2\omega\sqrt{\gamma\delta(1-|c|^2)}}{\omega_T\sqrt{5}} \tag{2}$$

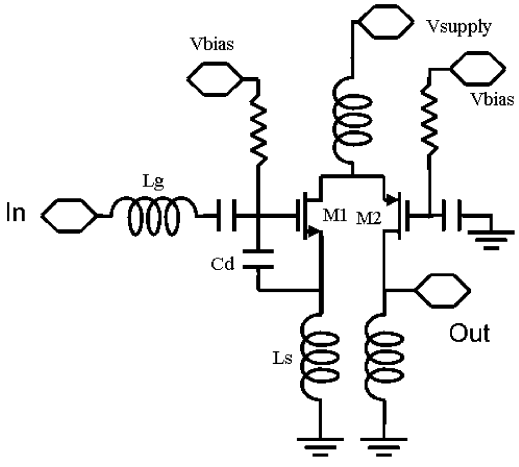


**Fig. 3.** Schematic of a folded cascode LNA adapted to apply PCSNIM technique.

**Table 2**
Parameter definitions.

| Parameter name | Definition |
|---|---|
| $Z_{opt}$ | Optimum noise impedance |
| $F_{min}$ | Noise factor minimum |
| $Z_{in}$ | Input impedance |
| $\omega_T$ | Cut-off frequency |
| $g_m$ | Transconductance |
| $C_{gs}$ | Gate–source capacitance |
| $C_t$ | $C_{gs}$+$C_d$ |
| $C$ | Noise correlation coefficient |
| $\alpha$ | $g_m/g_{d0}$ |
| $g_{d0}$ | Drain–source conductance |
| $\gamma$ | Experimental parameter related to the channel thermal noise current, for short-channel transistors it can be greater than 2 |
| $\delta$ | Experimental parameter related to the channel noise current. For short-channel transistors it can be greater than 2 |

$$Z_{in} = sL_S + \frac{1}{sC_t} + \frac{g_m L_S}{C_t} \tag{3}$$

And the condition that allows SNIM is

$$Z_{opt} = Z_{in}^* \tag{4}$$

From (1)–(3), the conditions that satisfy (4) and the matching with the source impedance are as follows:

$$\mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_S] \tag{5}$$

$$\mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_S] \tag{6}$$

$$\mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_S] \tag{7}$$

All the parameter definitions are summarized in Table 2.

The design parameters that can make (5)–(7) to be satisfied simultaneously are: $V_{GS1}$, $W_1$ the width of $M1$, $L_S$, and $C_d$. Since there are three equations and four unknowns, (5)–(7) can be solved for an arbitrary value by fixing the value of one of the design parameters. Therefore, in the PCSNIM LNA design technique, by the addition of an extra capacitor, the SNIM can be achieved at any level of power dissipation. The optimization is limited by the input impedance prescript. In order to adapt to the desired impedance, it is necessary to add and input inductance $L_g$.

The qualitative description of the PCSNIM design process would be as follows:

(1) Choose the transistor size $W_1$ and $V_{GS1}$ based on the power constraint $P_D$ and minimum NF $F_{\min}$.
(2) Choose the additional capacitance $C_d$, as well as the degeneration inductance $L_S$ to satisfy (5) and (6) simultaneously. The value of $C_d$ should be selected considering the compromise between the size of $L_S$ and the available power gain. Too much $L_S$ can lead to the increase in $NF_{\min}$, while large $C_d$ leads to the gain reduction due to the degradation of the effective cutoff frequency of the composite transistor (transistor including $C_d$).
(3) If there exists any mismatch between $Z_{in}$ and $Z_s^*$, $L_g$ is selected to provide impedance matching. The different components values that allow a PCSNIM are also limited by inductors sizes.

If the inductors area exceeds the expected values, it is necessary to relax the gain, noise, and power constraints. Furthermore, due to the folded cascode capacity to diminish the supply voltage, the folding of the common-gate transistor helps to extend the cutoff frequency of the common-source transistor. Moreover, the parasitic capacitances at the drain node of the common-source transistor can easily be eliminated by the resonance with the RF chock inductance. In Fig. 3, the size of $M1$ is 800 μm and $M2$ is 280 μm. Selecting a $V_{gs}$ of 0.65 V, the current for this LNA stage is of 2.96 mA, from a supply voltage of 1.5 V. The value of the degeneration inductance is 3 nH. In order to adapt the impedance input to the antenna impedance of 50 Ω, $L_g$ is designed with a value of 25 nH.

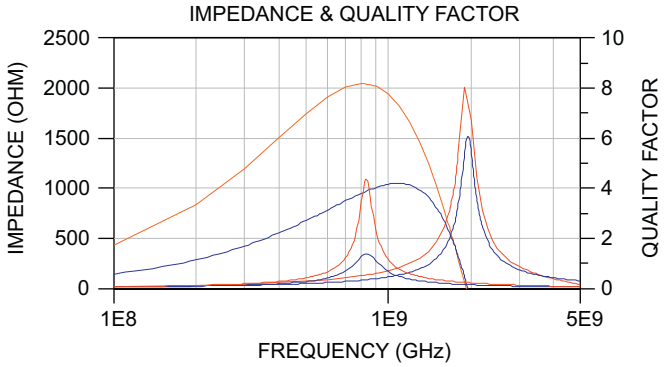


**Fig. 4.** In red, impedance and quality factor simulated by MoMentum for a 25 nH inductance. In blue, impedance and quality factor for the maximum inductor available in technology Hit Kit, 13 nH.

The inductor quality factor $Q$ represents an important characteristic that directly affects LNA power and noise performance. For instance, when it is used to match different stages or to degenerate a transistor, it adds actually a voltage noise source to the node where the inductor is connected with a value proportional to $1/Q$. In the case of a RF chock or load, the inductor is designed to resonate out; therefore, the $Q$ affects directly to the maximum allowable impedance. Fig. 4 shows, in red, the impedance and quality factor of an optimized layout inductor of 25 nH using a different strip width at each turn [11]. The optimization has been performed using MoMentum EM simulator from Agilent Technologies to obtain the highest $Q$ at 868.35 MHz. To compare, impedance and $Q$ of the biggest inductor supplied by the manufacturer, with an inductance of 13 nH, have been traced in blue on the same plot. Additionally, both inductors have been resonated at 868.35 MHz with an ideal capacitance. Improvement obtained using the inductor optimization procedure is easily observed: the impedance at resonance has been boosted by a factor of three. Therefore, for a fixed gain value of the LNA, the solution using the optimized inductor will have a power consumption three times lower than the one using the standard inductor library.

## 3. Active BalUn

In conventional CMOS receiver architectures, the conversion of the single-ended signal from the antenna to a differential signal at the input of LNA is performed by mean of an off chip passive BalUn. The disadvantage of this scheme is that the overall receiver NF is degraded by the insertion loss of the BalUn. In addition, the cost of the receiver grows due to the need of an extra off chip component. An alternative to this solution is to implement the conversion using an integrated active BalUn. This option provides an additional gain to LNA, desensitizing the overall NF of the system with respect to the NF of the next stages. Furthermore, by means of the active BalUn, the matching of the gain in the differential branches and the phase unbalance over a larger bandwidth are enhanced.

To evaluate the performance of the circuit, some of the typical characterization parameters defined for fully differential stages need to be redefined, e.g., the common-mode rejection ratio (CMRR). In fully differential schemes, this parameter is defined as

the differential and common-mode gain quotient. In single-ended topologies, this parameter involves a conversion of the single-ended input signal to a differential or common mode at the output. Therefore, although mixed-mode *S*-parameters are commonly well established for N-even number of ports, it is not the case for odd N-ports networks [12]. Thus, for completeness and with the aim of accurate study, the active BalUn features, will be discussed with the mixed-mode *S*-parameters formulation for the single-ended to differential conversion hereafter.

The well-known nine *S*-parameter matrix is related to its stimulus and response by $B_{std} = S_{std}A_{std}$, where $B_{std}$ and $A_{std}$ are response and stimulus waves vectors, respectively. The standard suffix has been used to discard any possible mistake. To resume the balance and unbalance information of the design, it is possible to express a new mixed-mode *S*-parameter matrix with respect to the standard matrix. In order to find this relation, it is possible to express the response and stimulus of standard mode and mixed-mode as follows:

$$a_{d_2} = \frac{1}{\sqrt{2}}(a_2 - a_3) \tag{8}$$

$$b_{d_2} = \frac{1}{\sqrt{2}}(b_2 - b_3) \tag{9}$$

$$a_{c_2} = \frac{1}{\sqrt{2}}(a_2 + a_3) \tag{10}$$

$$b_{c_2} = \frac{1}{\sqrt{2}}(b_2 + b_3) \tag{11}$$

The port 1 remains grounded with respect to the common-mode. Accordingly

$$a_{P_1} = a_1 \tag{12}$$

$$b_{P_1} = b_1 \tag{13}$$

where $a_{P_1}$ and $b_{P_1}$ represent the excitation in Port 1 referred to ground. $a_{d_2}$ and $b_{d_2}$ are, respectively, the differential stimulus and response in Port 2. And $a_{c_2}$ and $b_{c_2}$ are common-mode stimulus and response in Port 2, respectively. Following on with the matrix representation, it is easy to express the mixed-mode excitations from its standard definition

$$\begin{pmatrix} a_{P_1} \\ a_{d_2} \\ a_{c_2} \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \end{pmatrix} \tag{14}$$

The same transformation is found for the response $B_{mm} = MB_{std}$.

Once the matrix transformation *M* is known, the transformation between the *S* mixed-mode matrix and the standard matrix is given by [13]

$$S_{mm} = MS_{std}M^{-1} \tag{15}$$

The mixed-mode *S* parameters can be represented by

$$\begin{pmatrix} b_{P_1} \\ b_{d_2} \\ b_{c_2} \end{pmatrix} = \begin{pmatrix} S_{P_1P_1} & S_{P_1d_2} & S_{P_1c_2} \\ S_{d_2P_1} & S_{d_2d_2} & S_{d_2c_2} \\ S_{c_2P_1} & S_{c_2d_2} & S_{c_2c_2} \end{pmatrix} \begin{pmatrix} a_{P_1} \\ a_{d_2} \\ a_{c_2} \end{pmatrix} \tag{16}$$

where $S_{d_2P_1}$ and $S_{c_2P_1}$ represent, respectively, the gain in differential and common mode:

$$S_{d_2P_1} = \frac{1}{\sqrt{2}}(S_{21} - S_{31}) \tag{17}$$

$$S_{c_2P_1} = \frac{1}{\sqrt{2}}(S_{21} + S_{31}) \tag{18}$$

where $S_{P_1d_2}$ and $S_{P_1c_2}$ represent the inverse isolation to differential and common-mode:

$$S_{P_1d_2} = \frac{1}{\sqrt{2}}(S_{12} - S_{13}) \tag{19}$$

$$S_{P_1c_2} = \frac{1}{\sqrt{2}}(S_{12} + S_{13}) \tag{20}$$

The different reflection coefficients are given by the next expressions:

$$S_{P_1P_1} = S_{11} \tag{21}$$

$$S_{d_2d_2} = \tfrac{1}{2}(S_{22} - S_{23} - S_{32} + S_{33}) \tag{22}$$

$$S_{c_2c_2} = \tfrac{1}{2}(S_{22} + S_{23} + S_{32} + S_{33}) \tag{23}$$

In addition, it appears that mixed-mode conversions $S_{d_2c_2}$ represents the conversion of common-mode to differential when a common-mode stimulus loads Port 2. Similarly, $S_{c_2d_2}$ represents the differential mode to common-mode conversion:

$$S_{d_2c_2} = \tfrac{1}{2}(S_{22} + S_{23} - S_{32} + S_{33}) \tag{24}$$

$$S_{c_2d_2} = \tfrac{1}{2}(S_{22} - S_{23} + S_{32} - S_{33}) \tag{25}$$

Now we can revise is the CMRR and the balanced phase (BP):

$$CMRR = \frac{S_{P_1d_2}}{S_{P_1c_2}} \tag{26}$$

$$BP = phase(S_{21}) - phase(S_{31}) \tag{27}$$

Notice the difference with the actual *CMRR* definition in fully differential circuits where the relation does not include mode conversion.

Now, with these figures of merit, the performance of the second stage, shown in Fig. 5, can be correctly evaluated. The second stage of the LNA is formed by a differential cascode configuration, where the input signal is copied from one branch to the other through a bypass capacitor. The feedback circuit consists of *R*1 and $C_F$. The resistor *R*1 plays two roles: it keeps DC bias of *M*4, while it senses the signal feedback from *M*3 drain. $C_F$ provides a DC blocking function and RF signal copy [14].

Ideally, this circuit will provide equal amplitude (or gain) and 180° phase difference. However, due to the finite impedance at node *S*1 caused by parasitics at high frequency, the gain matching and the balanced phase are degraded. An active device is often used as the current source; however, the voltage drop across the

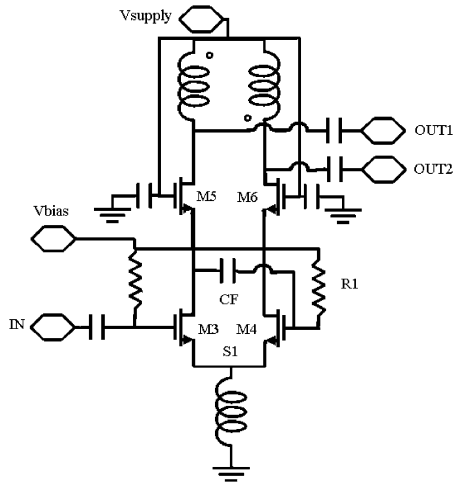


**Fig. 5.** Schematic of an active BalUn.

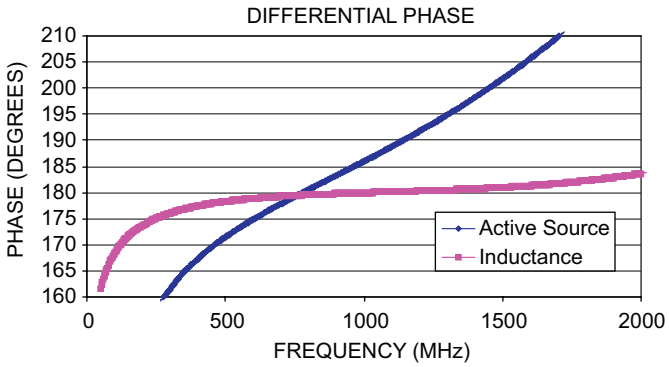


**Fig. 6.** Phase unbalance comparing between used of active source or inductive.

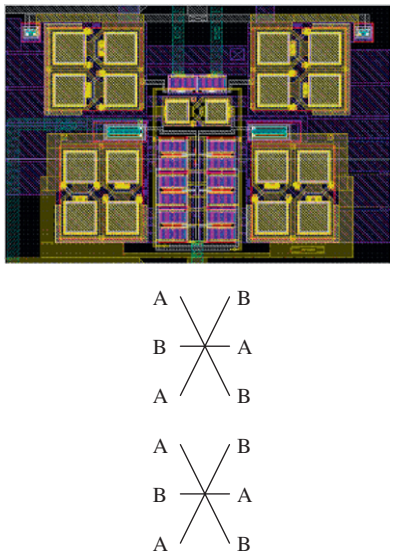


**Fig. 7.** Doubled centroid interdigitation topology for the differential pair in the active BalUn. layout and schematic.

drain and source makes implementing using a low-power supply difficult. For that reason, the active current source has been replaced by an inductor to increase the impedance of $S1$ at high frequencies. Fig. 6 shows the improvement in the phase balance when an inductor is used.

The differential transformer at the drain of the cascode pair transistors $M5$ and $M6$ is designed to resonate at 868.35 MHz. From the differential signal point of view, it generates a large impedance and, at the same time, it presents a notch for common-mode signal. The transformer has been optimized varying the width of each turn [15] using the former layout optimization procedure for inductors.

In Fig. 5, size of M3 and M4 is 1200 μm. Selecting a $V_{gs}$ of 0.65 V, the current consumption for this LNA stage is 2.71 mA drawn from a supply voltage of 1.5 V. The value for $C_F$ is 1 pF.

Gain and phase imbalance, as well as mixed-mode behaviour, are hardly dependent on device mismatches and layout symmetry and with intention of reducing any transistor mismatches, common-centroid topologies have been implemented. Hence, in the design of the folded cascode, a square ABBA configuration has been employed. Furthermore, in the case of the differential pair, the centroid interdigitation shown in Fig. 7 has been used [16]. Similarly, all capacitors, inductors and transformers have been designed keeping symmetry as much as possible. Fig. 8 shows the

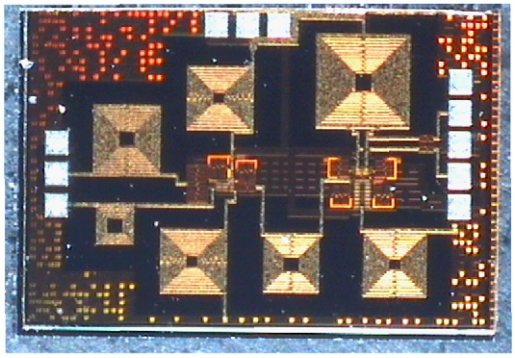

**Fig. 8.** Single-ended-to-differential LNA.

complete LNA single-ended-to-differential implementation with a total die area of 3 $mm^2$ including pads.

## 4. Experimental results

The LNA was implemented using a 0.35 μm RFCMOS process from Austrian Micro System. This technology contemplates the possibility of using four metal levels where the last one is a thick metal of 2.8 μm thickness and 10 mΩ/□.

The circuit has been measured on wafer using a CASCADE Microtech ACP40-GSG probe for the single-ended input and an ACP40-GSGSG probe for the differential output. A four-port ENA RF network analyzer [17] from Agilent Technologies has been used for the small signal characterization, whereas the probes have been deembedded using a three-port SOLT calibration technique with a LRMM differential substrate. In addition, test structures (open and short) have been fabricated in order to remove the effect of the pads. It must be kept in mind that the LNA design has been optimized to be matched with the previous and next transceiver stages, and does not matter instrumentation source and load impedances, i.e. 50 Ω.

The main measured figures of merit of the LNA gain are a single ended to differential gain of 21 dB, an output-to-input isolation better than 50 dB, and an input return loss of 10 dB while consuming 5.8 mA from a 1.5 V voltage supply. The differential output reflection coefficient is −4.8 dB referred to 100 Ω. Actually, the LNA has been designed to be matched to a differential VGA. Under that loading condition, the output reflection coefficient is −9.8 dB. Fig. 9 shows both the measured and simulated gains, and isolation. Fig. 10 shows input return loss and differential output return loss. Note that the simulated gain is less than the measured one. This is due to the fact that the actual quality factor of the fabricated inductors and transformers are better than the simulated ones.

One of the main features of the proposed circuit is the rejection of the common mode thanks to the inverter transformer placed at the output of the active BalUn. It is important to keep in mind that such device forces a differential broadband boundary condition. Therefore, the effectiveness for rejecting the common mode depends mainly on transformer mismatches. In Fig. 11, the measured difference of the phase between the two output branches has been plotted from 650 to 950 MHz showing an excellent performance of $180.0 \pm 1.0^{\circ}$ in the whole frequency range.

Another interesting figure of merit is the CMRR calculated as the differential gain $S_{d_2P_1}$ divided by common-mode gain $S_{c_2P}$. Notice that the CMRR is only important if the next stage connected to the LNA is single ended; otherwise, the rejection to the common-node noise is measured from the phase imbalance of

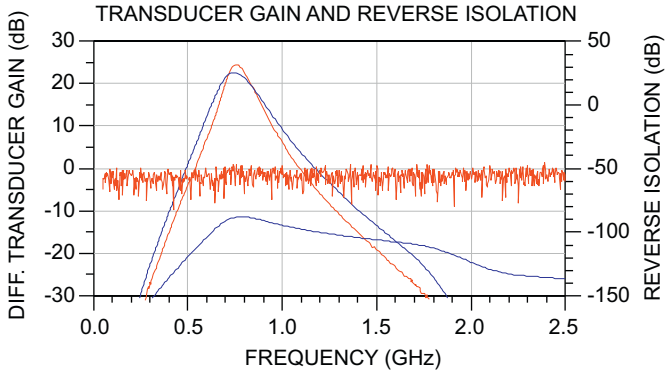


**Fig. 9.** Differential transducer power gain and reverse isolation. Measure is in red and simulation is in blue.

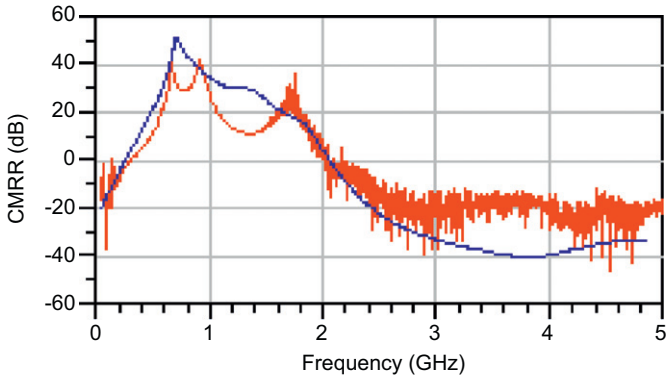


**Fig. 12.** Common-mode rejection ratio (CMRR). Measured data is in red and simulation data is in blue.

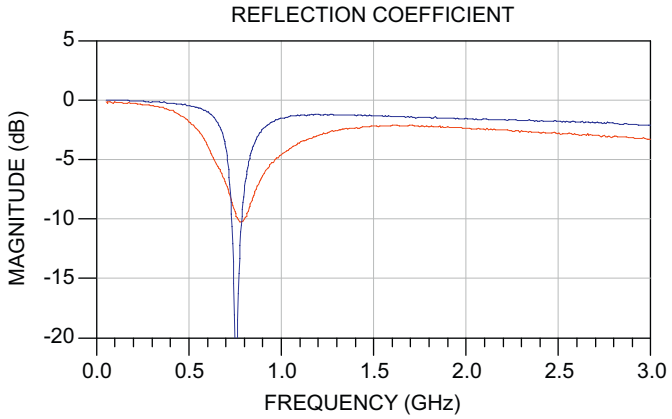


**Fig. 10.** Measured input reflection coefficients for 50 Ω reference in red. Measured differential reflection coefficient for 100 Ω reference in blue.

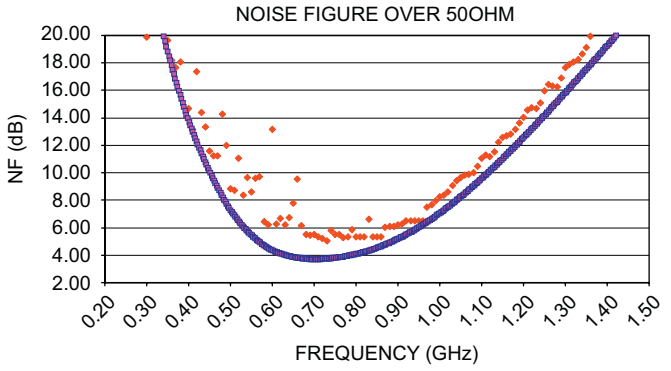


**Fig. 13.** Noise figure measured and simulated over 50 Ω. Measured data is in red and simulation data is in blue.

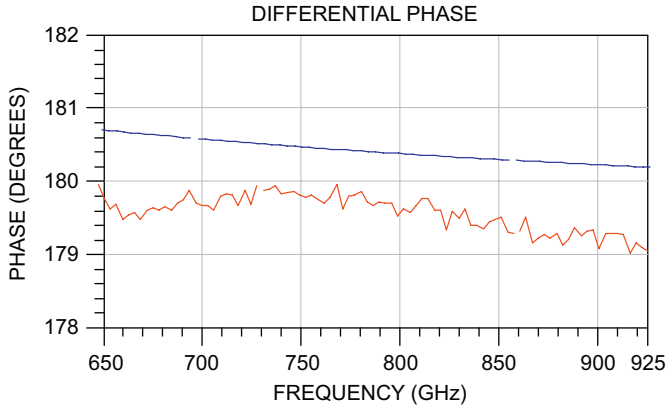


**Fig. 11.** Differential phase in more detail. Measure is in red and simulation is in blue.

**Table 3**
Performance comparison for 900 MHz LNAs in CMOS technology.

| Quantity | [18] | [19] | [10] | This work |
|---|---|---|---|---|
| Gain (dB) | 20 | 17.5 | 12 | 21 |
| NF (dB) | 3.2 | 2 | 1.35 | 4.3 |
| S11 (dB) | −12 | −10 | −18 | −9.5 |
| S22 | n.a. | −15 dB | n.a. | −9.8 dB |
| 1 dB CP (dB m) | −4 | −15 | −15 | −9.5 |
| IIP3 (dB m) | 8 | −6 | −4 | −3.0 |
| DC power (mW) | 27 | 22 | 2 | 9 |

both output branches. As shown in Fig. 12, a CMRR of −33 dB has been measured. Notice that the difference with the simulated value is quite large. The reason is an amplitude imbalance between both outputs. For the circuit described in this work, the output of the LNA is connected to a differential input VGA. In that case, the CMRR lowers to a value better than −50 dB.

In order to measure the noise figure, a HP 8970B NF meter has been used. Fig. 13 shows the simulated and measured NF over 50 Ω. At the frequency of interest, the NF measured value is 5.0 dB, whereas the simulated one is 4.7 dB. Although there are lower NF reported values, as shown in Table 3, such designs do not include the input gate matching inductor integrated on chip.

The non-linear behaviour of the LNA has been characterized through the measurements of the 1 dB-compression point (P1 dB) and the third order input referred interception point (IIP3). Keeping in mind that the IEEE 802.15.4 establishes only one channel in the European 868 MHz band, the 1 dB-compression point value is a better figure of merit about the maximum power at the input that can hold the LNA. Both outputs of the LNA have been combined out of chip by means of a hybrid coupler. Fig. 14 shows the obtained result. At a value of −9.5 dB m of the input power, the differential gain falls by 1 dB.

For measuring the IIP3 value, two signals have been combined using one hybrid coupler at the input of the LNA. The signals have been separated 1 MHz in frequency. At the same time, both outputs of the LNA have been combined in a single-ended signal.

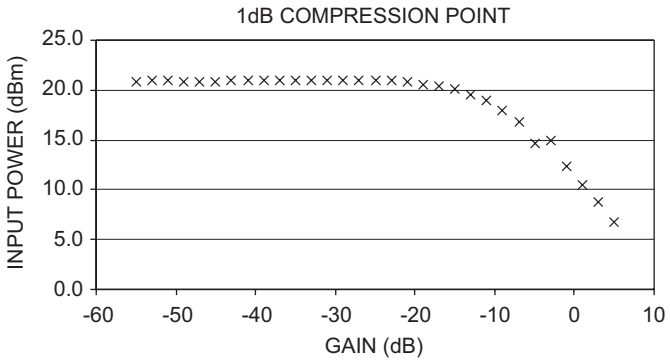


**Fig. 14.** Compression point −1 dB.

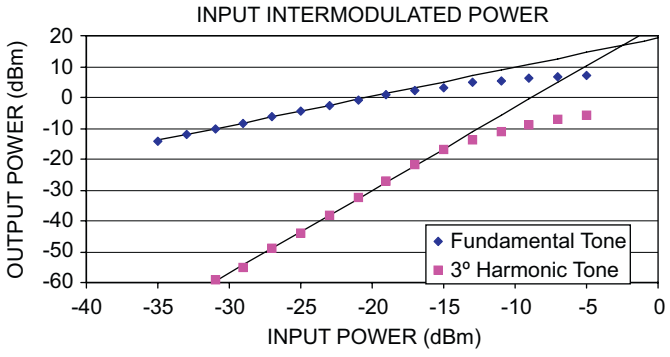


**Fig. 15.** Intermodulation input power measured. Fundamental tone at 868.35 MHz is in blue. In cyan, the third harmonic at 869.35 MHz.

Fig. 15 shows a measured IIP3 value of −3 dB m. Theoretically, an IIP3 value 9 dB greater than P1 dB value should be expected.

In order to summarize the resulting performance of the proposed LNA, Table 3 shows a comparison with other state-of-the-art 900 MHz LNAs in CMOS technologies. Notice that this work is the only one which provides a complete monolithic solution, integrating all inductors in the same die. For equivalent gain and IIP3 conditions in [18,19], the power consumption has been reduced by half due to the use of optimized inductors, while still keeping a good noise performance. Although [10] shows a lower NF and power consumption, it must be kept in mind that only the source degeneration inductor has been integrated; consequently the LNA performance depends mainly on the external components.

## 5. Conclusion

In this work, a low-power single-ended-to-differential LNA for IEEE 802.15.4 application has been implemented in a conventional 0.35 μm RFCMOS process. In order to enhance LNA performance for the first time, the substitution of current mirrors as well as resistive and active loads, by optimized on-chip inductors and transformers has been proposed. It has been proved that the replacement of the current mirrors by optimized inductance allows a supply voltage reduction of ($V_{th,nmos}$+|$V_{th,pmos}$|) value. In addition, the use of optimized load transformers and RF chocks has enabled the decrease of the polarization current by a factor of three for a fixed LNA gain value. Moreover, the behaviour of the symmetric inverter transformer as a load in the active BalUn presents a notch for the common-mode signal resulting. Thus, the phase balance is better than 1° in a large frequency range. All these improvements translate to the figures of merit of the designed LNA as follows: a NF of 4.3 dB, power gain of 21 dB, and a balance of 180±1°, while dissipating 6 mA from supply voltage of 1.5 V.

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