A 2.3-mW, 5-Gb/s Decision-Feedback Equalizing Receiver Front-End with Static-Power-Free Signal Summation and CDR-based Precursor ISI Reduction

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***Abstract*— This paper demonstrates a low-power decision feedback equalization (DFE) receiver with 0.46-mW/Gbps efficiency that can compensate up to -15-dB of channel loss while operating at 5-Gb/s. The key is the use of a clocked comparator design that can also perform the signal summations required for 1-tap direct-feedback DFE, additional DFE with an infinite impulse response (IIR) filter, and offset compensation, all without dissipating any static current. As a result, the power-hungry, high-bandwidth stages used in the prior backplane DFE receivers such as the continuous-time linear equalizer (CTLE), current-mode summing circuits, and fast selection logic for loop-unrolling DFE are all removed in this design. The pre-cursor ISIs are mitigated with passive inductive peaking at the termination loads and CDR timing adjustment, instead of a CTLE. A prototype DFE receiver fabricated in a 65nm LP CMOS demonstrates the measured eye opening of 112-mV_{pp} and 0.66-UI_{pp} while operating at 5-Gb/s with a -15-dB-loss channel.**

I. Introduction

Despite the steady demand for the higher bitrates in backplane serial I/O transceivers, the resulting increase in the power dissipation has been one of the hindering factors. Especially, the power dissipated by various channel equalization circuits such as the linear equalizer and decision feedback equalizer (DFE) grows sharply as the bitrate or channel loss increases. In fact, the degrading power efficiency with the higher channel loss serves as a strong motivation for adopting optical channels for board-to-board, chip-to-chip, and even on-chip I/Os, since their low channel loss can obviate the need for such power-demanding equalization circuits.

This paper demonstrates that yet a very power-efficient equalizing receiver can be realized by judiciously combining the existing circuit techniques in literature [4]-[8]. Our primary design objective in this work is to adopt a set of circuit techniques that can effectively compensate the pre-cursor or post-cursor inter-symbol interferences (ISIs) without requiring high-bandwidth amplifying or filtering stages, which tend to dissipate large amount of static currents while supporting the required high gain-bandwidth products.

Fig. 1 identifies the circuit blocks that tend to consume large currents in many of the existing backplane equalizing receiver designs [1]-[3]. First, the high-bandwidth CML differential stages placed on the input signal path are one of the power hogs, such as the limiting amplifiers (not shown) and continuous-time linear equalizers. Their power efficiencies are particularly poor when these circuits are composed of multiple stages in order to provide both high gain and high bandwidth. Second, a DFE requires a summing node where the expected post-cursor ISIs due to the previously-arrived bits can be subtracted, and this summing circuit may dissipate considerable power depending on the implementation. For instance, the widely-used current-mode summing circuit shown in Fig. 1 can consume large static current when trying to satisfy the required linearity and bandwidth or to increase the number of DFE finite impulse response (FIR) filter taps. Third, many backplane receivers adopted loop-unrolling DFE architecture for high-speed operation and its high-speed digital logic gates to select the proper comparator output based on the previously detected bits are typically oversized to meet the stringent timing requirements and hence can consume significant power.

The receiver design proposed in this paper aims to remove all of these power-hungry circuits (Fig. 2). First, the received signals are fed directly to the comparator inputs, without going through any limiting amplifiers or CTLE stages. The precursor ISIs are mitigated instead by the passive inductors added in series with the termination resistors [4] and by shifting the data sampling phase from its nominal position [5]. Second, the DFE signal summation is performed within the comparator circuit without consuming static power. Understanding of the comparator's operation during the sampling phase, i.e. integration of the input signals onto its internal capacitors, led to a design that achieved both good linearity and high bandwidth. Third, the timing-critical first

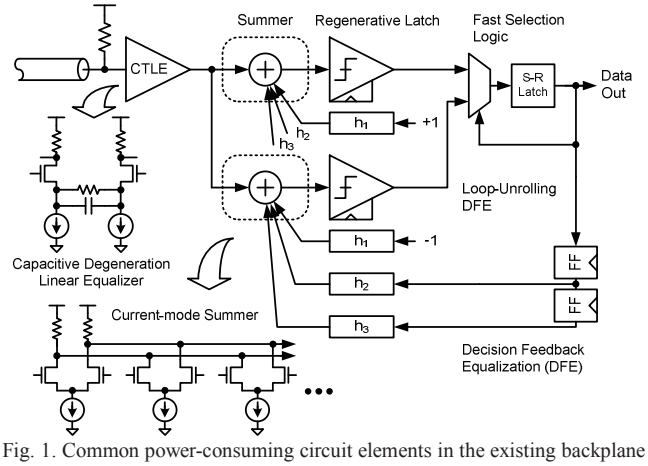


Fig. 1. Common power-consuming circuit elements in the existing backplane high-speed receivers: linear equalizers (CTLE), DFE summing circuits, and fast digital logic for loop-unrolling DFE.

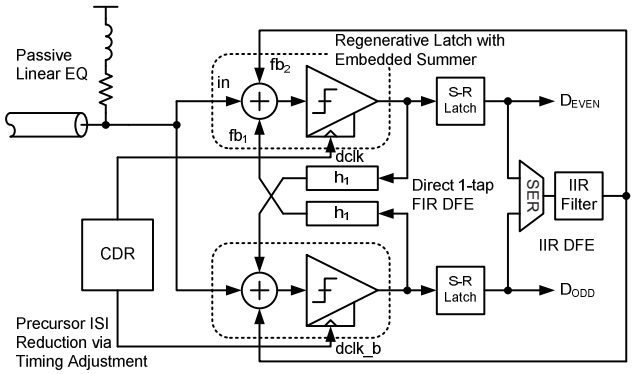


Fig. 2. The proposed DFE receiver front-end with three ISI-reduction schemes: 1-tap FIR DFE, IIR DFE, and CDR timing adjustment.

post-cursor ISI is cancelled by a direct FIR DFE feedback exploiting the overlaps between the two half-rate comparators' evaluation periods [6], which eliminates the fast digital logic required for the loop-unrolling DFEs. And lastly, to reduce the number of DFE feedback signals at the summing circuit, an infinite-impulse-response (IIR) filter is adopted to subtract the residual post-cursor ISIs after the first one [7].

Such a careful selection of the circuit techniques made a highly energy-efficient equalizing receiver possible with only 2.3mW of power consumption while compensating -15dB channel loss at 5Gb/s. The following sections will present the overall architecture of the proposed receiver, its circuit implementations, and the measurement results from a prototype chip implemented in a 65nm LP CMOS process.

II. Receiver Architecture

As outlined in the introduction and illustrated in Fig. 3, the proposed receiver compensates the channel-induced ISIs largely by three means. First, a 1-tap FIR DFE cancels the first post-cursor ISI. Second, an IIR DFE with a first-order continuous-time low-pass filter cancels the trailing post-cursor ISIs after the first one. Third, the pre-cursor ISIs are reduced by shifting the data sampling points to the earlier positions instead of using a CTLE. The ISI due to the input capacitance of the receiver is also mitigated by the shunt-peaking inductors to some extent.

Interestingly, each of these three ISI compensation means corresponds to one of the input signals to our summer-

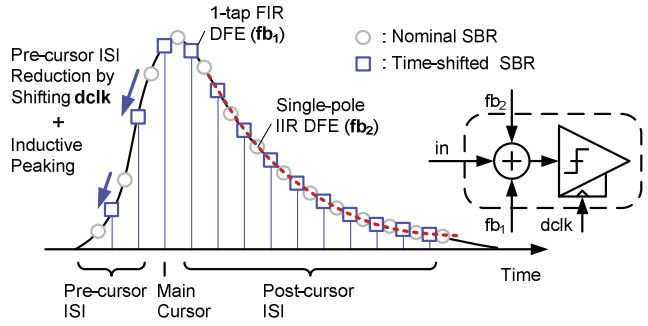


Fig. 3. Channel loss compensation schemes of the proposed equalizing receiver.

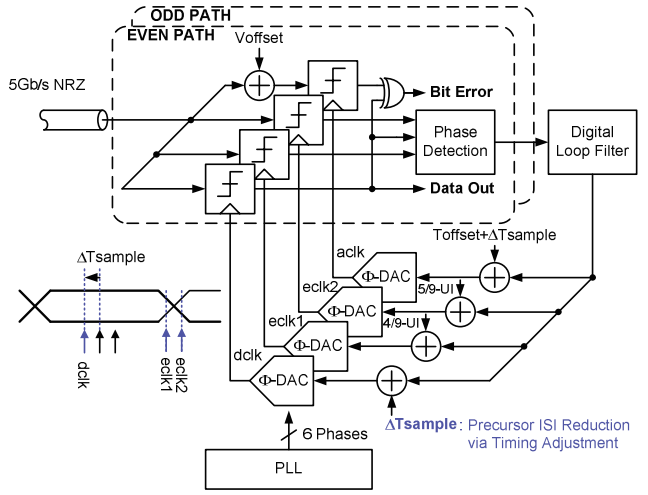


Fig. 4. The overall architecture of the receiver front-end including the clock-and-data recovery (CDR) unit.

embedding clocked comparator in Fig. 3. For instance, the 1-tap FIR DFE feedback is fed to the fb_1 input, the IIR DFE feedback is fed to fb_2, and the pre-cursor ISI is reduced by adjusting the clock timing (dclk). Hence, the design of the clock comparator is central to our proposed receiver and its circuit details will be described in the next section.

The overall receiver front-end is a half-rate architecture with two parallel data paths (even and odd) as illustrated in Fig. 4. Each data path consists of total of 4 comparators: one for sampling the data, two for detecting the timing errors, and one for monitoring the *in-situ* eye opening [8]. Each comparator is driven by a dedicated clock (dclk, eclk1, eclk2, and aclk), whose timing is digitally controlled via a phase-domain digital-to-analog converter (DAC), selecting two out of 6 clock phases and interpolating them in 3 steps. Thus, the nominal resolution of the phase DAC is only 1/9-UI, yet the employed CDR is still able to achieve the target BER < 10^{-9} due to its optimal phase interval detection scheme described in [9]. This unique phase detection method keeps the CDR phase from dithering.

III. Circuit Implementations

A. Regenerative Latch with Embedded Summer

Fig. 5 shows the circuit schematic of the regenerative latch that also performs signal summation without dissipating static current. The circuit is basically a StrongARM latch with multiple input pairs connected in parallel. When the clock (clk) rises, the current steered by each of the input pairs according to its respective differential input discharges the internal nodes (X and X') of the comparator. The individual currents from the input pairs are linearly added and hence the comparator makes the final decision based on the sum of the input differences. It is noteworthy that even though the parallel input pairs increase the capacitance (C) on the

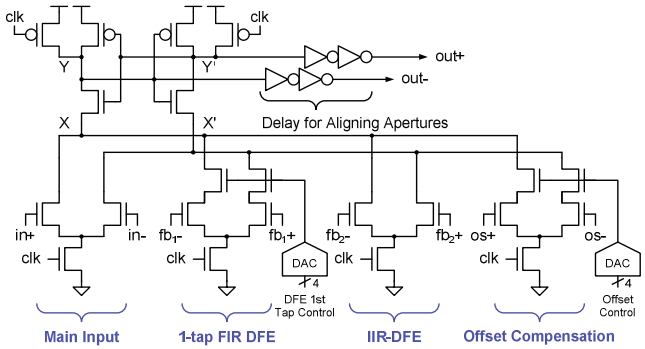


Fig. 5. Regenerative latch with embedded summer.

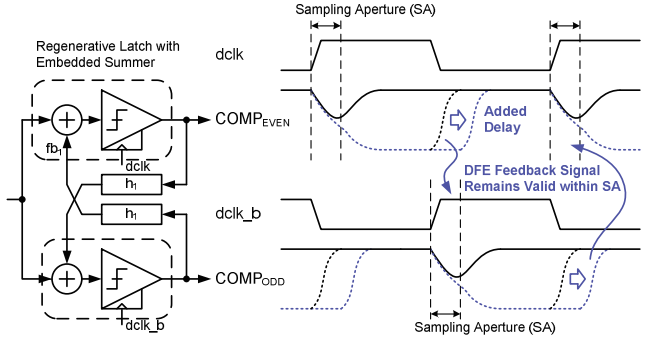


Fig. 6. Direct-feedback 1-tap FIR DFE and its timing diagrams.

internal nodes X/X', the total discharging current (I) also increases, keeping the sampling aperture of the comparator roughly the same. In addition, the regeneration bandwidth and power dissipation is largely determined by the capacitance on the nodes Y/Y', which is weakly dependent on the number of input pairs [10]. Therefore, the signal summation can be done at much lower costs in power and speed than the current-mode summation stage in Fig. 1. For the inputs that are binary (fb_1 and os; where os is the offset polarity input), their weighting factors are digitally controlled by adjusting the bias voltages to the current-starving devices via 4-bit resistor-ladder based DACs, respectively.

B. 1-tap FIR DFE via Direct Feedback

The proposed receiver adopts direct-feedback DFE instead of loop-unrolling DFE in order to avoid the high-speed selection logic that consumes power. The speed-bottleneck of the conventional direct-feedback DFE is overcome by deliberately creating overlaps between the evaluation periods of the two half-rate regenerative latch stages, so that the settled output signal of one latch can be fed directly to the input of the other while it is in the sampling phase, as illustrated in Fig. 6.

The two inverters added at the outputs of the first-stage latch in Fig. 5 play the role of creating these overlaps between the evaluation periods. Basically, they delay the reset of the signals fed to the other comparator's fb_1-input, so they can keep the previously settled data values while the comparator is still in sampling phase. Once the sampling phase is over, the signals can be reset without affecting the results. These inverters also serve as buffers presenting smaller loads to the latch stage, improving its regeneration bandwidth. This way, the direct-feedback 1-tap DFE can be realized with minimal impacts on the speed and area. As mentioned earlier, the tap coefficient of this DFE is controlled by adjusting the bias voltage to the current-starving devices using a DAC.

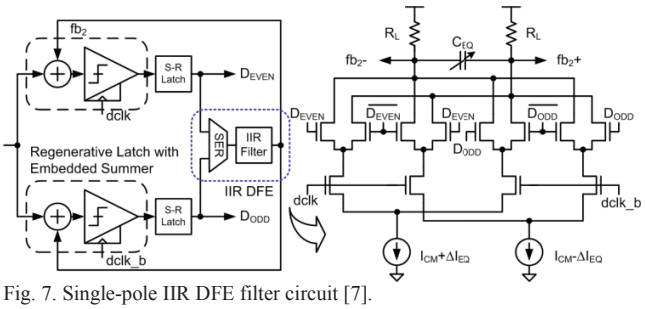
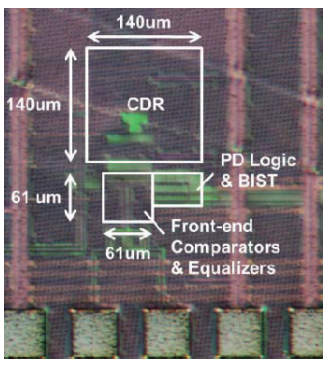


Fig. 7. Single-pole IIR DFE filter circuit [7].



Technology	65nm CMOS
Data rate	5-Gbps
Power	2.3mW (front-end)
	6.8mW (CDR)
Supply	1.2V
Area	0.0036 mm^2
Channel loss	-15dB at 2.5GHz
Data pattern	2^7-1 PRBS
BER	$<10^{-9}$

Fig. 8. The die photograph and performance summary of the prototype equalizing receiver fabricated in 65nm CMOS.

C. Single-Pole IIR DFE

The trailing post-cursor ISI taps after the first one are cancelled by an IIR DFE, assuming that the trailing trajectory of the single-bit response can be well approximated as a single-pole exponential decay. The decision feedback signal is generated by feeding the serialized data stream into a single-pole low-pass filter, adopting the circuits described in [7] and shown in Fig. 7. The gain and pole frequency of the filter are adjustable by tuning the difference between the two bias currents (ΔI_{EQ}) and switching the capacitance (C_{EQ}), respectively. Although this filter stage has static current consumption, the current level can be low since the stage does not require a high bandwidth.

D. Post-Cursor ISI Reduction via Timing Adjustment

As mentioned earlier, the precursor ISIs are mitigated by shifting the data sampling points to the earlier positions, rather than using a CTLE. While this is not a broadly applicable equalization scheme, most high-speed backplane channels indeed exhibit relatively short and sharp preceding edges in their single-bit responses where this method can be found effective. As the timing shift also reduces the main cursor, the optimal shift amount maximizes the net reduction in the pre-cursor ISI offset by the main cursor reduction.

The data sampling points are adjusted by changing the spacing between the data sampling clock (dclk) and edge sampling clocks ($eclk_1$, $eclk_2$) in Fig. 4. The nominal spacings are 4 and 5 steps (4/9- and 5/9-UI), respectively, and increasing these digitally-controlled values will shift the data sampling clock towards the earlier position. As can be seen, this is an attractive way of reducing the precursor ISIs with very little increase in the hardware and power dissipation.

IV. Measurement Results

The prototype equalizing receiver along with the supporting CDR is implemented in a 65nm low-power CMOS technology. The chip's photograph and performance characteristics are listed in Fig. 8. While receiving a 5-Gb/s, 2^7-1 PRBS pattern, the receiver front-end including the total of 8 comparators for data, edge, and eye sampling consumes 2.3-mW from a single 1.2V supply and is able to compensate -15dB of channel loss. The rest of the CDR circuits including the multi-phase PLL, phase DACs, phase detection (PD) logic, and digital loop filter consume 6.8mW in total. The operating bitrate was mainly limited by the maximum clock frequency supported by the CDR employing a ring oscillator, not by the receiver front-end itself. Fig. 9 shows the frequency characteristics of the channel used during the test and the measured eye diagram at its output, which is completely closed.

Fig. 10 shows the effective eye diagram measured at the input of the comparator after the DFE feedback signals, canceling the post-cursor ISIs, have been applied. This is measured by an on-chip eye opening monitor, which is basically an additional data sampling comparator with the adjustable timing and voltage offsets. By comparing the outputs from this additional comparator and the main data comparator, one can find the largest timing and voltage shifts that still recover the correct data, and thus the eye opening.

With the described equalization techniques applied, the worst-case eye opening with a BER of 10^{-9} was 112-mV_{pp} and 0.66-UI_{pp}. In this case, the optimal shift in the data sampling positions was 1/9-UI. Fig. 10 also shows the eye opening without the shift, which has a much smaller eye opening of 0.33-UI_{pp} and 88mV_{pp}, demonstrating the effectiveness of the technique in reducing the precursor ISI.

To assess the optimality of the equalizer settings, Fig. 11 plots the change in the vertical eye opening as functions of the four equalizer parameters: the FIR DFE tap coefficient (α_{DFE}), the shift in the data sampling timing (ΔT_{sample}), and the differential bias current (ΔI_{EQ}) and capacitive load (C_{EQ}) of the IIR filter, respectively. The optimal parameter values found by exhaustive sweeping were α_{DFE}=45mV, ΔT_{sample}=1/9-UI, $\Delta I_{EQ} = I_{CM}/15$, and C_{EQ}=9.6fF.

V. Conclusions

This presented work demonstrated that a low-power equalizing receiver can be realized by adopting a set of circuit techniques that can compensate the channel losses without incurring high power dissipation. The key to the achieved 0.46mW/Gbps efficiency was the design of regenerative latch with embedded summer, which enabled the effective combination among the direct-feedback FIR DFE, IIR DFE, and CDR timing adjustment for pre-cursor ISI reduction.

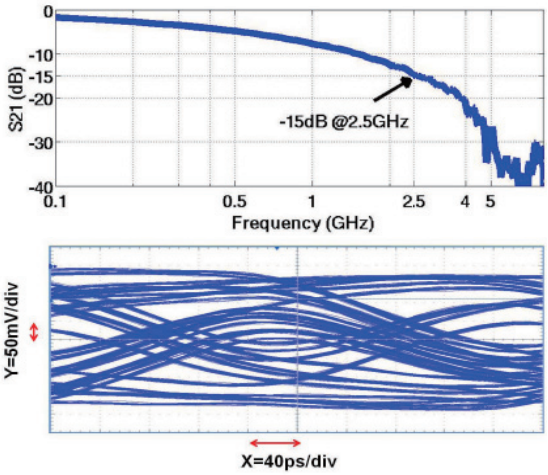


Fig. 9. The frequency response of the channel and the eye diagram of 5-Gb/s, 2^7-1 PRBS NRZ data stream measured at the channel output.

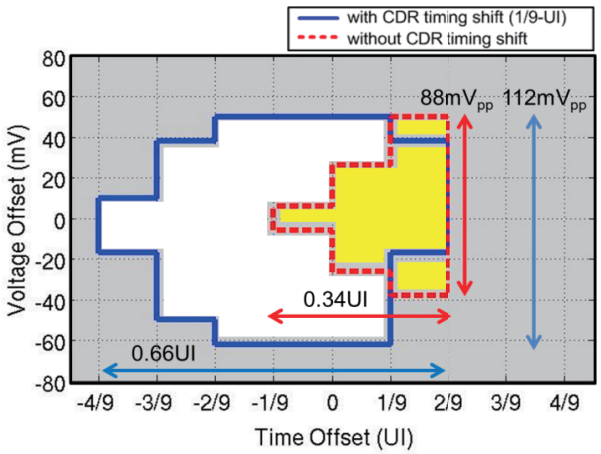


Fig. 10. The effective eye diagram at the comparator input after the DFE subtraction, measured by an *in-situ* eye-opening monitor [8].

Acknowledgement

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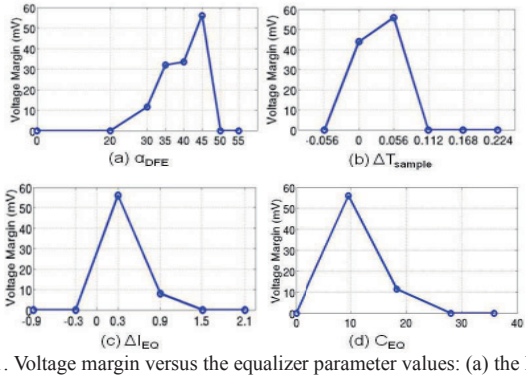

Fig. 11. Voltage margin versus the equalizer parameter values: (a) the FIR DFE tap coefficient (α_{DFE}), the shift in the data sampling positions (ΔT_{sample}), and the differential bias current (ΔI_{EQ}) and capacitive load (C_{EQ}) of the IIR filter.

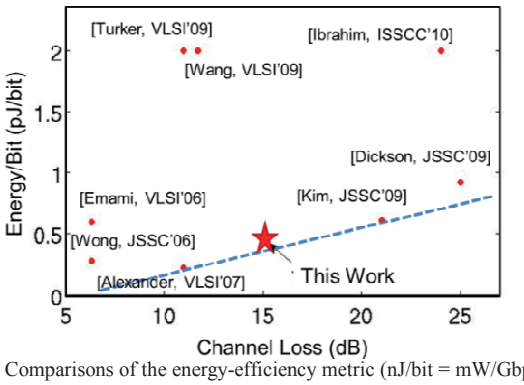

Fig. 12. Comparisons of the energy-efficiency metric (nJ/bit = mW/Gbps).