A 55nm, 0.6mm^2 Bluetooth SoC Integrated in Cellular Baseband Chip with Enhanced Coexistence

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***Abstract*—This paper describes a 55nm, 0.6mm^2 Bluetooth SoC integrated in cellular baseband. Several techniques are used to enhance co-existence performance of Bluetooth with cellular and Wi-Fi. First is the design of current-mode interfaces from LNA to complex BPF for better linearity and the additional anti-aliasing LPF placed before ADC for outband rejection in the RX. Second is the use of a passive voltage sampling mixer to lower out-of-band emission noise floor in TX. Moreover, only two inductors are used, one of which is a field-cancelling inductor used in VCO layout to achieve a spur-free LO signal, minimizing magnetic coupling from other parts of SoC. The TX output power is +11dBm at BDR mode and +8dBm at EDR3 mode, with 1.5-kHz frequency drift and <6% RMS DEVM. The RX sensitivity is better than -96.5dBm and -89.2dBm for BDR and EDR3 modes respectively. The measured BT RX sensitivity is -57dBm at BDR mode while co-existing with -5dBm of Wi-Fi 54Mbps OFDM.**

Keywords—Bluetooth, co-existence, CMOS integrated circuit, transceivers.

I. INTRODUCTION

In recent years, the wide popularity of mobile devices, such as smart phones and tablets, has driven the demand of integrating multiple radios either on a single chip or on the same device so that people can surf the internet while on a phone call through the Bluetooth (BT). Among multiple radios, BT and Wi-Fi have been the basic and must-have features in mobile devices. While concurrent operation of multiple radios brings excellent user experience, there exist great challenges in dealing with radio co-existence either in an SoC or in the same mobile platform, or even in the proximity. For example, concurrent operation between BT and Wi-Fi, both in the common 2.4GHz band, sets additional requirements in RF front-end circuit (e.g., TX far-out noise floor, RX linearity, ADC clock harmonics) and system control (e.g., non-overlapping channels spaced 25MHz apart) [1].

This paper describes a cellular-combo SoC that integrates the BT RF transceiver with the analog/digital interfaces (ADC and DAC), and the cellular digital baseband in a 55nm 1P5M CMOS process. The integration of the digital and RF circuits into a single chip needs to deal with several issues such as receiver de-sensitization and LO impurity caused by digital clocks and TX spectrum purity. The corresponding design techniques are conducted through the transceiver circuits to overcome the process limitation and keep high co-existence performance. Section II presents the architecture of transceiver. Key building blocks of the transceiver and measurement results are described in Section III and IV. Conclusion in summarized in Section V.

II. ARCHITECTURE

The transceiver architecture is composed of a LIF receiver, a DCT, a LO generator, and a frequency synthesizer. The frequency plan of the frequency synthesizer highly impacts for the transceiver's performance, its level of integration, and power consumption. With an offset-LO frequency plan, the synthesizer is designed to lock at 6.0GHz, which is not at the harmonics of the desired 2.4GHz band, hence preventing VCO pulling by the PA and improving the transmission quality.

In the RX chain, an integrated balun converts the single-ended signal to differential form and a variable-gain LNA preceding the quadrature mixer amplifies the voltage signal with current-mode interface to improve concurrent operation with cellular and Wi-Fi systems. A complex band-pass filter (BPF) following the mixer performs channel selection and image rejection. The filtered IF signal is then digitized by two successive-approximation (SAR) ADCs before further signal processing in the digital domain. To cover a wide signal dynamic range, six gain modes are distributed over the entire chain.

Fig. 1 shows the block diagram of receiver chain and illustrates the inquiry/inquiry scan issue in BT system. In a BT radio network, the master device entering the inquiry state sends an inquiry message with only a general access code. The nearby slave device periodically executes the inquiry scan and issues an inquiry response with its own unique BT address and its channel. Normally, once gained correct information about the slave device with which the master device starts paging and then sets up a synchronized connection. In real case, however, if the inquiry signal is located at the RX LO with an offset frequency at ADC sampling rate, then after reception and down-conversion, the IF signal is aliased by ADC sampling and falls in-band, hence falsely triggering RX to issue an inquiry response with wrong channel. To reduce ADC aliasing effect, a 2nd-order anti-aliasing LPF placed before ADC is designed to further improve the inquiry/inquiry scan successful rate. Moreover, spur mixing due to TX and/or LO spurs also causes BT connection failed after inquiry/inquiry scan.

978-1-4799-0280-4/13/$31.00

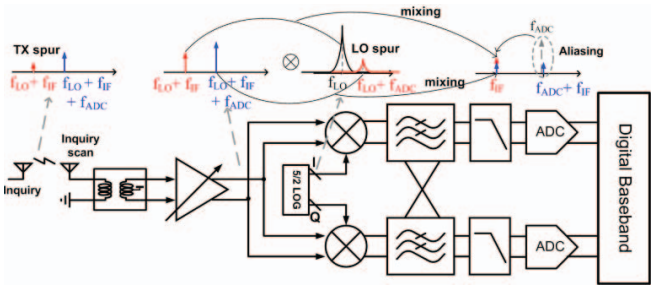

Fig. 1. Receiver chain block diagram

For the TX, the 5/2-LO frequency plan enables DCT architecture without suffering frequency drift during high-power transmission. The digital quadrature signals coming from the baseband are first converted to analog form by two 9-bit current-mode DACs. The signal is then filtered by a first-order LPF and up-converted to RF by the quadrature mixer. A integrated PA follows and delivers maximally 12dBm power to the on-chip balun. Instead of conventional Gilbert mixer, a passive voltage sampling mixer is adopted to achieve lower far-out noise floor for co-existence of BT system with other radios [2]. In addition, the larger voltage output swing of the passive voltage sampling mixer also gives another benefit to save the load inductor, typically used in Gilbert mixer. The TX chain has 32dB gain control range. Several calibration techniques are embedded to reduce analog impairments such as I/Q mismatch, TX LO leakage, biasing current accuracy, and filter corner frequency control.

III. CIRCUIT DESCRIPTION

A. RX

As shown in Fig.2, the LNA is a complementary fully-differential design with source degeneration inductor, Ls. To minimize the area of passive devices, the Ls is put inside the balun, forming an nested transformer. With proper connection, the current flowing in Ls produces magnetic flux with the same direction as that produced by the balun, increasing the inductance without any extra area penalty. The total effective inductance of Ls increases from 0.6nH to 1.1nH with k=0.3 between balun and Ls. Input impedance and noise matching is achieved by utilizing Ls and the transformation ratio offered by the balun. The balun is shared and co-designed in the LNA and PA. A higher turn ratio offers voltage gain before LNA to lower the noise contribution from the LNA. For PA, a high-ratio balun provides a higher load impedance with better efficiency for a given target power. However, a higher turn ratio also increases the loss from the balun itself. The final design of differential impedance is around 325Ω at the combined point of LNA and PA. Because of the short distance between two metal layers, the balun is realized by stacked structure to maximize the magnetic coupling between the two coils. With an balun area of 250x250um^2 and 2.5dB insertion loss, the whole RX chain NF is 5.3dB-5.8dB.

To co-exist with cellular and Wi-Fi systems, the interfaces from the LNA to complex BPF are all in current mode for better linearity. Following the LNA is the current-mode passive I/Q mixer. Since I and Q switching quads share one LNA, a non-overlapping duty-cycle LO is required to avoid I/Q cross-talk and IM2 distortion. A 2nd-order complex BPF following the mixer provides required rejection for the image, adjacent channel interferences, and out-of-band blockers. In addition, a 2nd-order LPF is inserted before ADC to reduce ADC aliasing effect and improve the BT inquiry scan. Finally, the IF signal is digitized by two SAR ADCs with 32MHz sampling rate and 1.1mA current consumption before being processed by digital baseband modem. The measured peak SNR and dynamic range is 62dB and 69dB, respectively.

B. TX

The block diagram of a direct up-conversion transmitter is shown in Fig. 3. It is composed of two 9-bit DACs, a LPF, a passive voltage-sampling I/Q mixer (IQM), a PA, and a loopback calibration for analog impairments. Following the current-mode DAC is a current-to-voltage IF buffer to convert the IF signals from current mode to voltage mode with enough driving capability for IQM. In addition, the embedded low-pass function in the IF buffer helps to suppresses unwanted DAC images at the harmonics of 64MHz sampling frequency, and also attenuates the IF far-out noise for co-existence with cellular and Wi-Fi. Instead of using Gilbert mixer, a passive IQM driven by 25% duty-cycle LO is used to achieve lower far-out noise floor and save the inductor area. To improve the linearity and cross-talk effect of the passive IQM under large input voltage swing, a digitally tunable passive-RC LPF is inserted before the passive IQM to control the output voltage swing of IF buffer. On the other hand, the finite LO slew and non-zero switch time of mixer switches result in a short over-lapping period. During this transition, an IF current loop between I and Q paths occurred, degrading the IQM linearity and gain. Therefore, a non-overlapping LO is designed for better linearity. Although the non-overlapping LO benefits higher conversion gain in passive IQM and save the area for inductor load commonly used in active mixer, it also comes with large harmonics due to the wider low-pass bandwidth characteristic, degrading in-band IM3 and IM5 performance.

The PA is essentially a pseudo-differential configuration for better linearity, operating at class-AB mode. The bias point is carefully chosen for the driving and cascode transistors, in order to achieve an output P1dB near 12dBVp at the PA/LNA interface. With 2.5dB balun loss, the output P1dB of TX chain is >11dBm at balun single-ended port. The TX chain offers a total gain control range of 32dB with resolution of 4dB. A finer gain step of 0.5dB is provided by digital setting through DACs. For better power efficiency, the PA bias current is designed to scale with the output power.

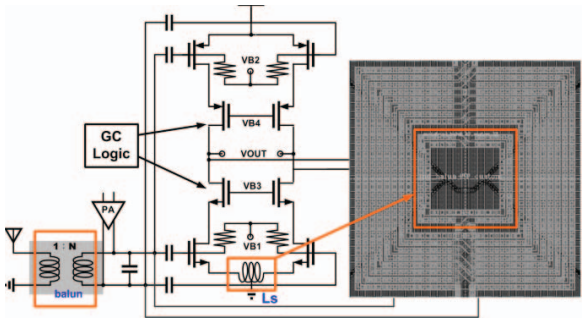

Fig. 2. Simplified LNA schematic

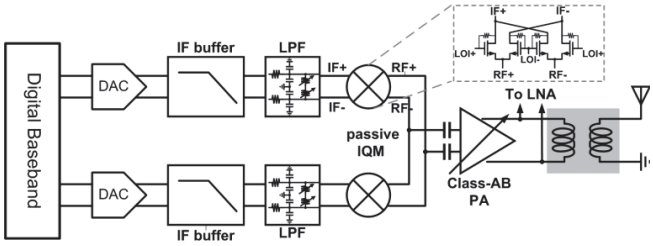

Fig. 3. Transmitter chain block diagram

C. Synthesizer

A fully integrated synthesizer is designed using a 3rd-order Δ-Σ fractional-N PLL, operating at 6.0GHz. The VCO adopts a complementary cross-coupled pair and a field-cancelling inductor with L=1.63nH and Q=11. By careful device sizing and maximizing the Q*L product, the VCO operates at an optimal swing and has phase noise better than -126dBc/Hz at 3-MHz offset. In layout floor planning, the filed-cancelling inductor should be carefully aligned to the center of balun to minimize magnetic coupling between these two structures. A buffer follows the VCO and drives a feedback divider (FB-DIV) and an inductor-less LO generator. The FB-DIV consists of several 2/3 cells. The 2/3 cell can be configured as a divided-by-2 or a divided-by-3 according to a modulus selection. Moreover, FB-DIV is also re-used as a frequency calibration (FCAL) counter. A MASH 1-1-1 SDM is used for quantization noise shaping. The measured LO locked at 2.402GHz is shown in Fig. 4. Fig. 5 shows the measured LO spurs at 26MHz and 32MHz away, which are -102dBc and -72dBc, respectively.

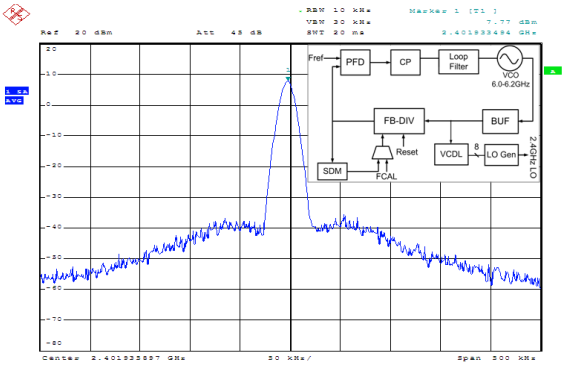

Fig. 4. Measured LO signal locked at 2.402GHz

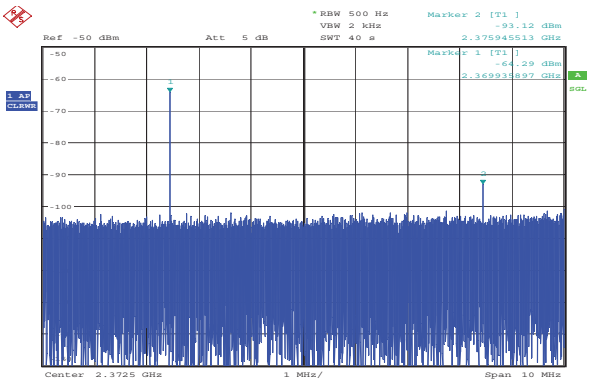

Fig. 5. Measured LO spurs at 26MHz and 32MHz away

D. LO generator

With the advantage of high-speed devices in advanced process, an inductor-less LO generator is introduced to converting the incoming 6.0GHz VCO clocks to 2.4GHz LO clocks. The 2/5 frequency conversion is realized by selecting clock phases at different instances. Fig. 6 shows the block diagram of the voltage-controlled delay line (VCDL) and the 2/5 LO generator. The VCDL is responsible for generating eight evenly-spaced clock phases. Due to PVT variation and different channel frequencies, the VCDL needs to be calibrated before every TX/RX burst to ensure its evenly-spaced output phases. The eight incoming clock phases generated by the VCDL are grouped into four complementary pairs and fed into the phase selector. Following the phase selector are four connected D-flip-flops (DFF) which generates the S signals. The phase selector is controlled by the S signals to properly select four out of eight incoming clock phases at any moment. The output LO signals are 2.4GHz non-overlapping quadrature clocks to feed into the RX and TX mixers.

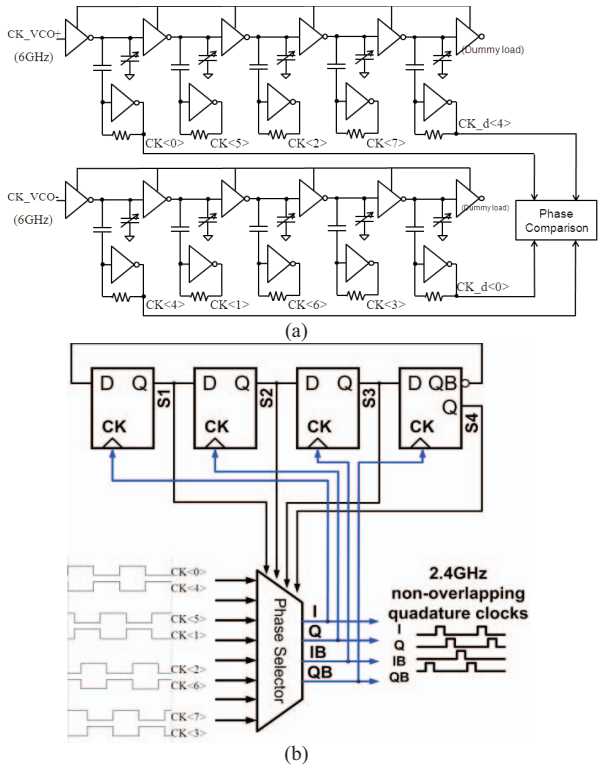

Fig. 6. Block diagram of (a) VCDL and (b) 2/5 LO generator

IV. Measurement Results

The fully integrated Bluetooth SoC is fabricated in 55nm 1P5M CMOS process. It is packaged in the form of ball grid array (BGA). The die photograph of the chip is shown in Fig. 7. The die size is 9.4 mm^2, of which only 0.6mm^2 is occupied by the BT transceiver. The Bluetooth SoC achieves high level of integration, in which only two inductors are used.

The performance of the SoC is summarized in Table I. The TX output power is +11dBm and +8dBm at BDR and EDR3

modes respectively, with 1.5-kHz frequency stability and <6% rms DEVM. The RX sensitivity is better than -96.5dBm and -89.2dBm for BDR and EDR3 modes respectively. DC current consumption for continuous TX transmission at +11dBm output power is 127.3mW, and is 44.4mW for continuous RX reception at reference sensitivity level.

Fig. 8 records the out-of-band (OOB) blocker power when BER reaches 0.01%. In this measurement, the desired BT signal is fixed at 2460MHz, with input power of -67dBm. Both desired signal and OOB CW blocker are injected into the receiver. To qualify the BT/WiFi co-existence performance, a BER/PER test is conducted under a controlled environment to emulate simultaneous operation. When BT is in RX mode, a constant Wi-Fi TX signal is applied at a 25MHz frequency spacing with power range from -5dBm to -70dBm. At each of Wi-Fi TX power level, the BT RX signal is swept from -5dBm to -70dBm, and BER is recorded. The result is shown in Fig. 9.

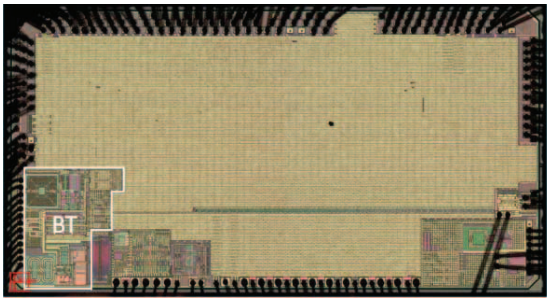

Fig. 7. Die photo

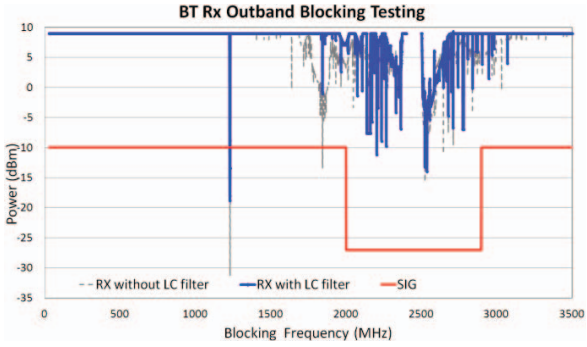

Fig. 8. RX OOB blocking performance

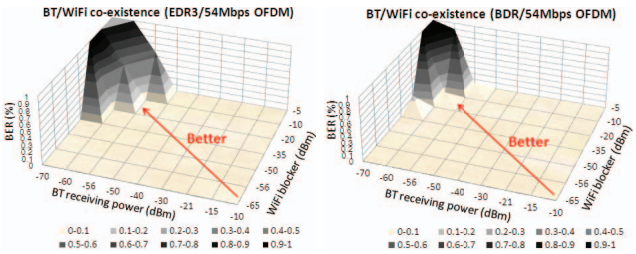

Fig. 9. Measured BT/WiFi co-existence performance

TABLE I. TX/RX PERFORMANCE SUMMARY

	this work	ISSCC 2012 [1]	JSSCC 2012 [3]	ISSCC 2010 [4]
Technology	55nm	65nm	110nm	65nm
TX power (dBm)				
BDR	11	13	10	10
EDR3	8	8	7	8
TX EDR3 DEVM				
rms	5.7%	-	6%	6%
peak	13.8%	-	15%	-
Sensitivity(dBm)				
BDR	-96.5	-95.5	-95.5	-91
EDR3	-89.2	-89.5	-89.0	-
RX EDR3 C/I (dB)				
CCI	14.0	-	15.0	-
ACI +/ - 1M	-8.0	-	-6.0	-
ACI +/- 2M	-41.5	-	-43.0	-
ACI +/- 3M	-46.5	-	-44.0	-
Image ratio	-34.0	-	-22.0	-
Image +/- 1M	-48.0	-	-44.0	-
TX current w/i DAC (mA) (1.35V/3.3V)	21.2 / 29.9	23 / 41	- / 43	33 / -
RX current w/i ADC (mA) (1.35V/3.3V)	21.6 / 4.6	23 / 3	27.5 / -	21 / -
Die Size (RF-Only)	0.6mm^2	1.46mm^2*	1.8mm^2	2.7mm^2*

*Estimated area from reference.

V. CONCLUSION

In this paper, a 55nm, 0.6mm^2 Bluetooth SoC integrated in cellular baseband is presented. The proposed transceiver circuit topologies enhance the co-existence performance with the Wi-Fi and cellular and increase the successful rate of BT inquiry scan under large inquiry power, resulting in better user experience.

ACKNOWLEDGMENT

The authors would like to thank these various teams at MediaTek who supported this work including RF/DE, SE, WCN/CD, SA, and CSD/SD.

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