Low-Power DFE Design

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(JSSC, June 2011)

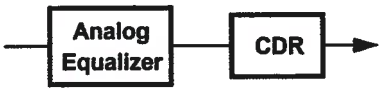
Outline

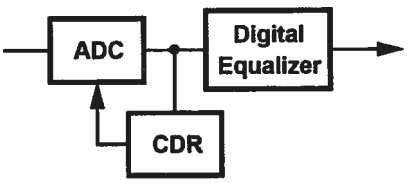
- Motivation
- Background
- Scaling limits of DFEs
- Proposed architecture
- Design of building blocks
- Experimental results

Equalizer Categories

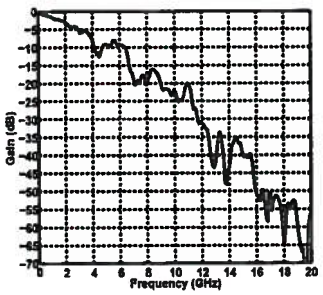
- TX vs. RX Equalization

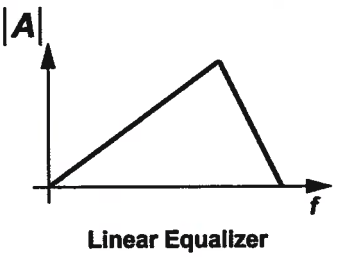
- Digital vs. Analog



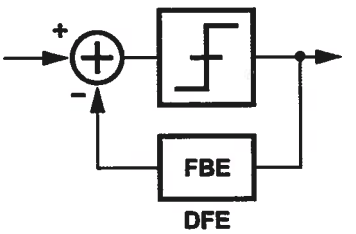


- Linear vs. Non-Linear





Linear Equalizer

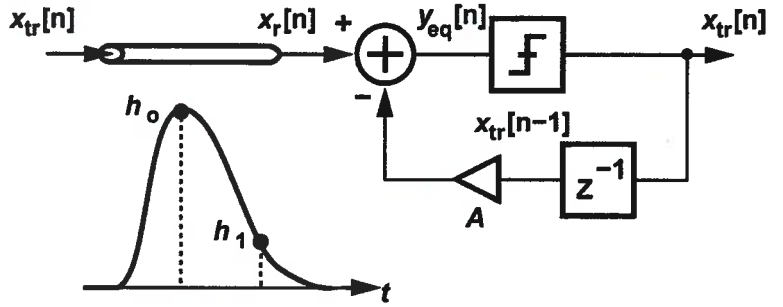


DFE

Prior Art

Reference	Bit Rate	CMOS	Loss	Topology
[ChenISSCC09]	10 Gb/s	32 nm	10 dB	4-Taps integrating DFE
[LiuISSCC09]	10 Gb/s	65 nm	23.2 dB	DFE-IIR
[HidakaISSCC09]	10.3 Gb/s	90 nm	35.8 dB	Linear equalizer + 1-Tap Speculative DFE
[BulzacchelliISSCC09]	11.1 Gb/s	65 nm	16 dB	1-Tap speculative DFE + 4-Tap DFE
[LiaoISSCC08]	40 Gb/s	90 nm	10 dB	Linear Equalizer
[LuVLSI08]	40 Gb/s	0.13 μm	14 dB	Linear Equalizer
[LeeJSSC06]	20 Gb/s	0.13 μm	20 dB	Linear Equalizer
[SunagaISSCC09]	18 Gb/s	90 nm	14 dB	4-Taps DFE, 1st tap assisted by CDR
[TurkerVLSI09]	19 Gb/s	90 nm	11 dB	1-Tap speculative DFE
[WangVLSI09]	21 Gb/s	65 nm	11.7 dB	Linear equalizer + 1-Tap DFE

Decision Feedback Equalizer



$$x_r[n] = h_o x_{tr}[n] + h_1 x_{tr}[n-1]$$

$$y_{eq}[n] = x_r[n] - A x_{tr}[n-1]$$

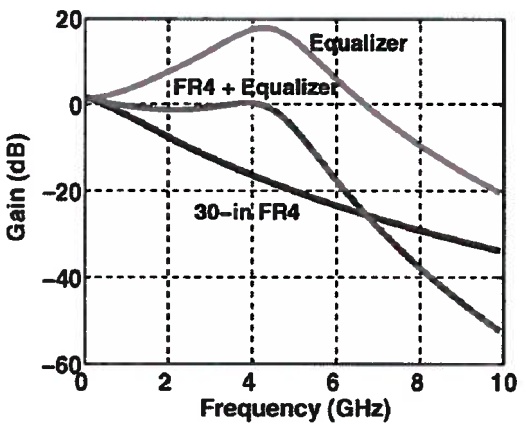
$$= h_o x_{tr}[n] + h_1 x_{tr}[n-1] - A x_{tr}[n-1]$$

☺ Corrects both loss and reflections
☺ Does not increase cross-talk

☹ High power (especially, digital)
☹ Tight timing constraints

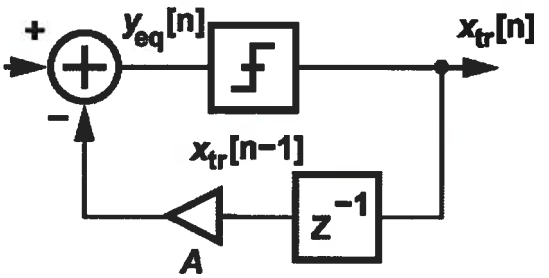
Comparison of Linear Eq. and DFE

Linear Equalizer



- No feedback → high speed
- But cannot compensate for notches in freq. response.
- Amplifies noise and crosstalk.

DFE

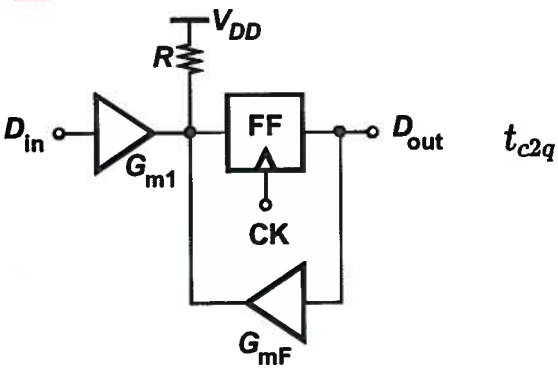


- Cancels tail of impulse response.
- But feedback delay limits the speed.
- Clips noise and crosstalk.

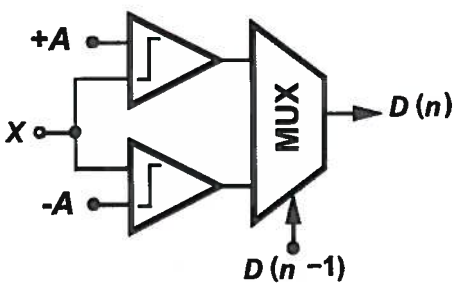
→ Use ~5-10 dB of linear equalization followed by a DFE.

- Direct Full-Rate DFE
- Unrolled Full-Rate DFE
- Direct Half-Rate DFE
- Multiplexed-Half-Rate DFE
- Unrolled Half-Rate DFE

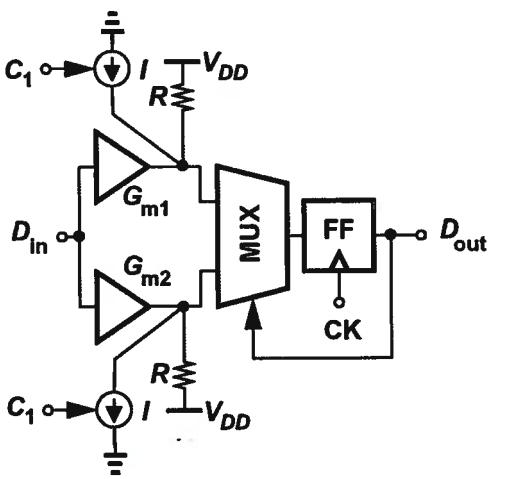
Direct and Unrolled Full-Rate DFEs



$$t_{c2q} + t_{setup} + t_{FB} < UI = 50\ ps$$

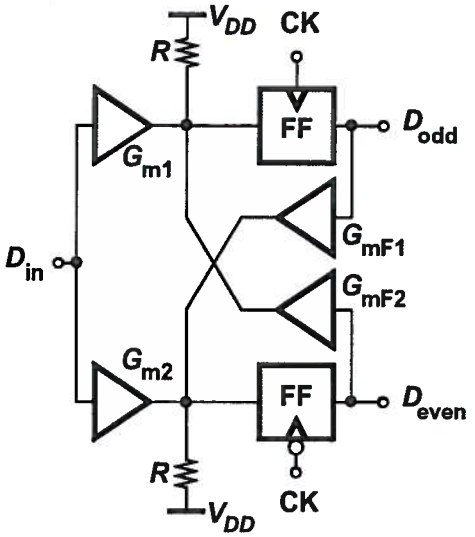


$$y_{eq}[n] = x_r[n] - Ax_{tr}[n-1]$$

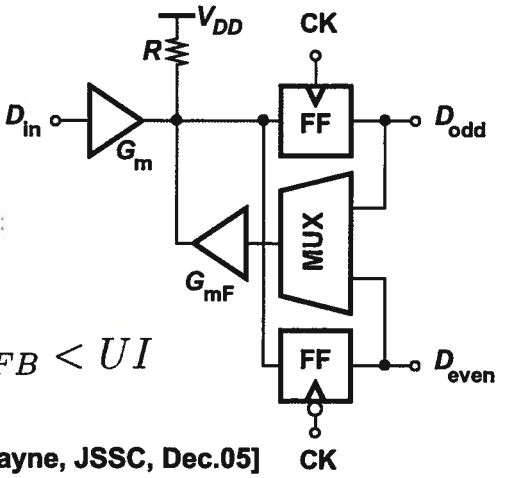


$$t_{cq,FF} + t_{setup} + t_{cq,MUX} < UI$$

Direct and MUXed Half-Rate DFE



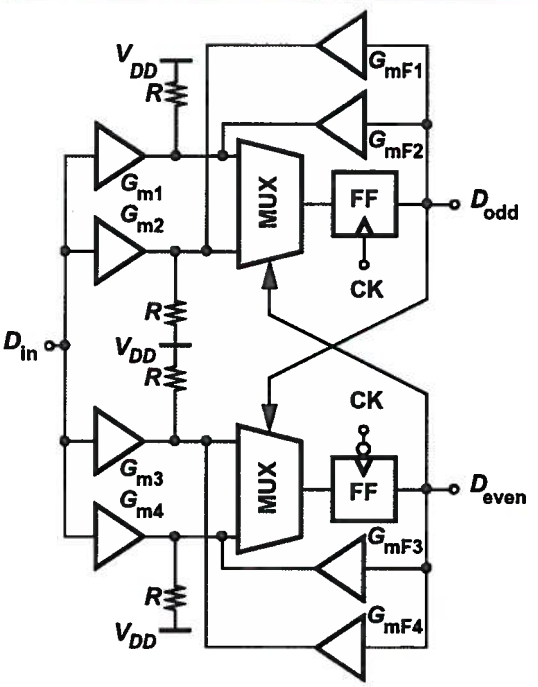
$$t_{cq} + t_{setup} + t_{FB} < UI$$



$$t_{cq,FF} + t_{setup} + t_{p,MUX} + t_{FB} < UI$$

[Payne, JSSC, Dec.05]

Half-Rate Unrolled DFE

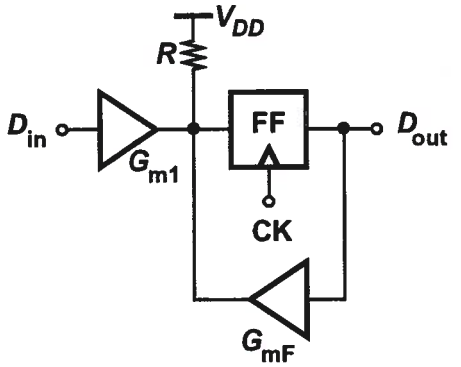


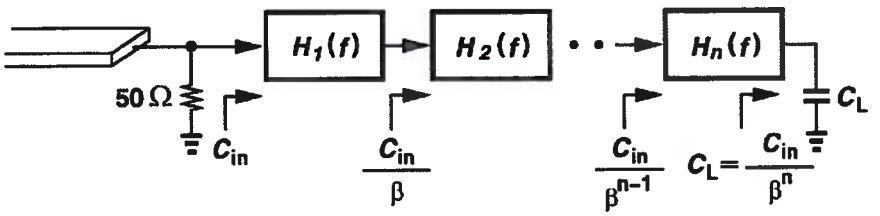
$$t_{cq,FF} + t_{setup} + t_{cq,MUX} < UI$$

[Bulzacchelli, JSSC, Dec.06]

Scaling Limits of DFEs

- How far can we reduce the power dissipation of a DFE?
- How do we systematically scale without degrading:
  - Speed
  - Voltage Headroom
  - Gain
- Can't apply reverse scaling:





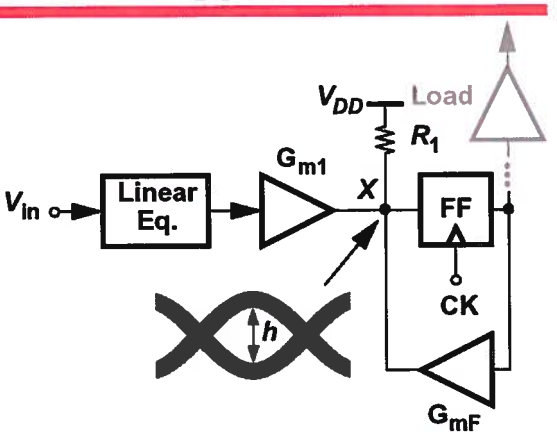
[Gondi & Razavi, JSSC, Sep. 07]

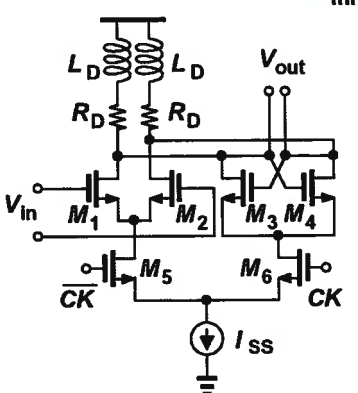
Scaling Methodology

- Scale:
  - Transistor Widths by M
  - Bias Currents by M
  - Load Resistors and Inductors by 1/M.

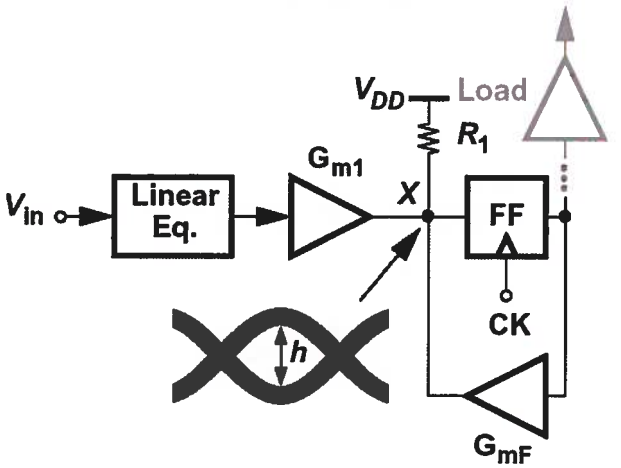
As a result,

- Speed relatively constant if load stage (e. g., CDR) can be driven.
- Voltage headroom and gain are constant.
- Power dissipation falls by 1/M.





Linear Scaling Limitations



- Electronic Noise
- Offset Voltage
- Flipflop Sensitivity

Effect of Noise on BER

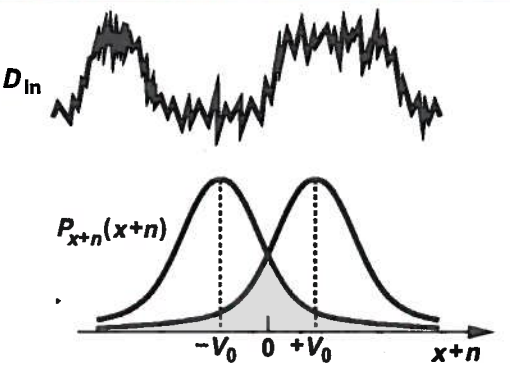
- With only noise present:

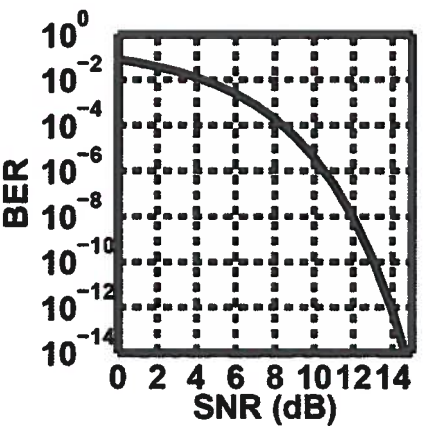
$$BER = Q\left(\frac{V_{pp,eq}}{2\sqrt{V_{n,eq}^2}}\right)$$

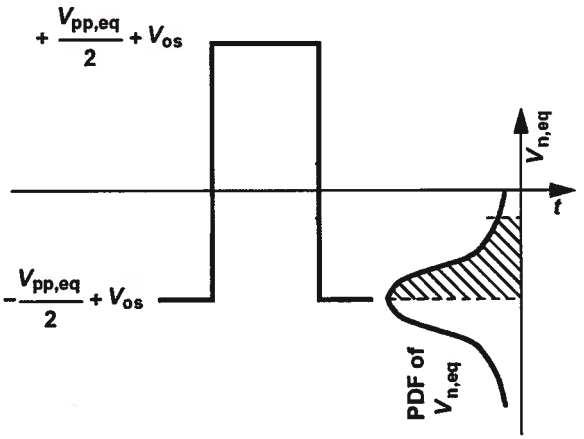
- For BER = 10^{-14}

$$V_{pp,eq}/2\sqrt{V_{n,eq}^2} = 7.6$$

What happens if the circuit has offset?







- **Half of the bits see an effective peak swing of $V_{pp,eq}/2 - V_{os}$ and the other half $V_{pp,eq}/2 + V_{os}$**

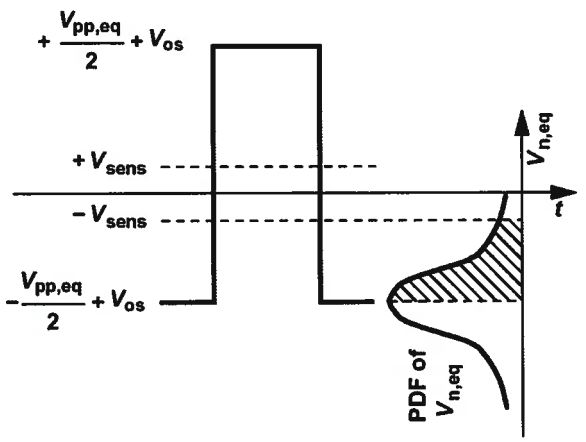
$$BER = \frac{1}{2}Q\left(\frac{V_{pp,eq}/2 - V_{os}}{\sqrt{V_{n,eq}^2}}\right) + \frac{1}{2}Q\left(\frac{V_{pp,eq}/2 + V_{os}}{\sqrt{V_{n,eq}^2}}\right) \approx \frac{1}{2}Q\left(\frac{V_{pp,eq}/2 - V_{os}}{\sqrt{V_{n,eq}^2}}\right)$$

Effect of FF Sensitivity

- **Sensitivity is defined as the minimum input voltage that guarantees regeneration to approximately 80% of the full latch output swing in half clock cycle.**

$$V_{sens} = \frac{0.8I_{SS}}{G_{m1}}\exp\left(-\frac{G_{m3}R_D - 1}{2R_D C_L f_{CK}}\right)$$

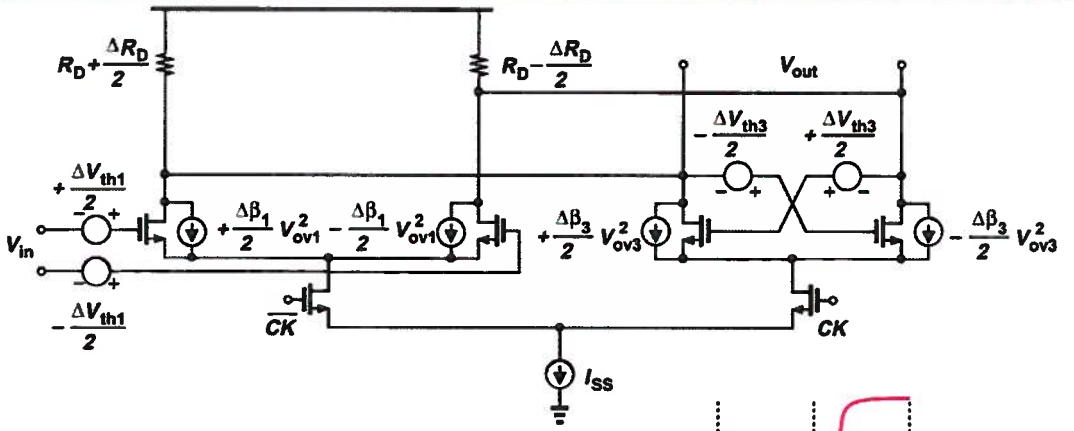
- **What happens if the peak input swing is equal to V_{sens}?**

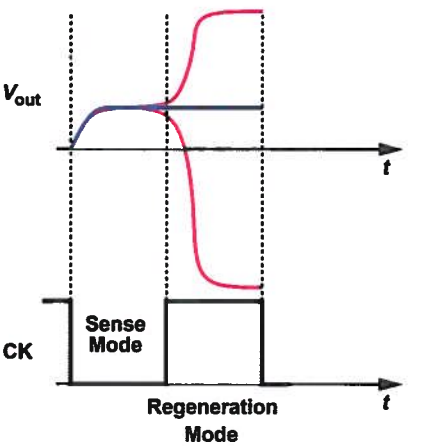


$$BER = \frac{1}{2}Q\left(\frac{V_{pp,eq}/2 - V_{os} - V_{sens}}{\sqrt{V_{n,eq}^2}}\right)$$

$$V_{pp,eq} \geq 15\sqrt{V_{n,eq}^2} + 2(V_{os} + V_{sens})$$

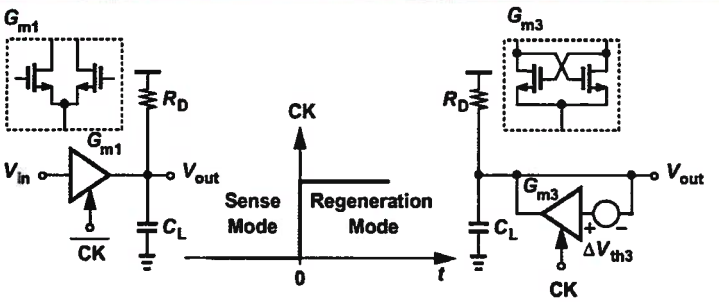
Latch Offset: Definition





- **Input offset voltage is the voltage that produces no regeneration (i.e., keeps the latch metastable).**

Latch offset: Abrupt Clock Edge



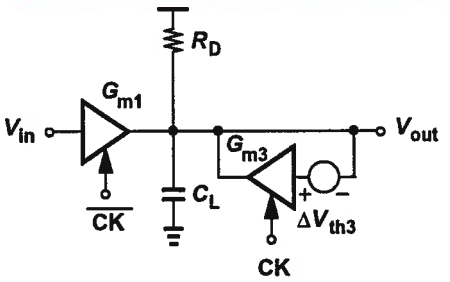
- **At the end of sense mode:** $V_{out}(0) = G_{m1}R_D V_{in}$
- **During regeneration:**

$$G_{m3}(V_{out} + \Delta V_{TH3}) = \frac{V_{out}}{R_D} + C_L\frac{dV_{out}}{dt}$$

$$V_{out}(t) = \frac{G_{m3}R_D\Delta V_{TH3}}{G_{m3}R_D - 1}\left(\exp\frac{G_{m3}t}{C_L}\exp\frac{-t}{R_DC_L} - 1\right) + G_{m1}R_DV_{in}\exp\frac{G_{m3}t}{C_L}\exp\frac{-t}{R_DC_L}.$$

- **For no regeneration:** $\frac{G_{m3}R_D}{G_{m3}R_D - 1}\Delta V_{TH3} = -G_{m1}R_DV_{in} \Rightarrow V_{in} = \frac{-\Delta V_{TH3}}{G_{m1}R_D - \frac{G_{m1}}{G_{m3}}}$

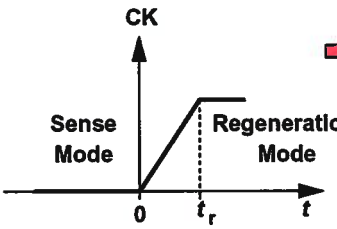
Latch Offset: Gradual Clock Edge



$$g_{m1}(t) = G_{m1}\sqrt{1-\frac{\alpha t}{t_r}}$$

$$g_{m3}(t) = G_{m3}\sqrt{\frac{\alpha t}{t_r}},$$

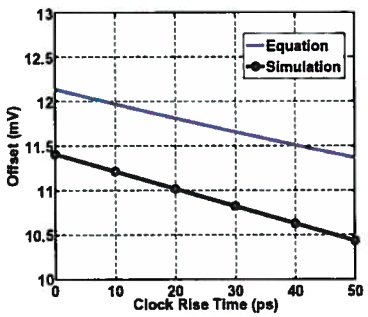
$$\alpha = V_{CK,pp}/(\sqrt{2}V_{ov,CK})$$



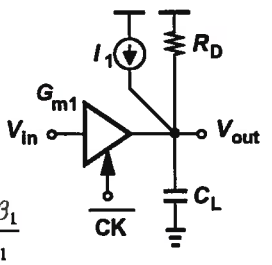
$$\Rightarrow G_{m3}\sqrt{\frac{\alpha t}{t_r}}(V_{out}+\Delta V_{TH3}) + G_{m1}\sqrt{1-\frac{\alpha t}{t_r}}V_{in} = \frac{V_{out}}{R_D} + C_L\frac{dV_{out}}{dt}$$

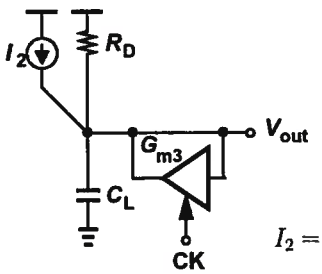
- **No closed-form solution**
- **Use a correction factor:**

$$V_{in} = \frac{-\Delta V_{TH3}}{G_{m1}R_D - \frac{G_{m1}}{G_{m3}}\exp\frac{(G_{m3}R_D-2)t_r}{2\alpha R_D C_L}}$$



Overall Latch Offset





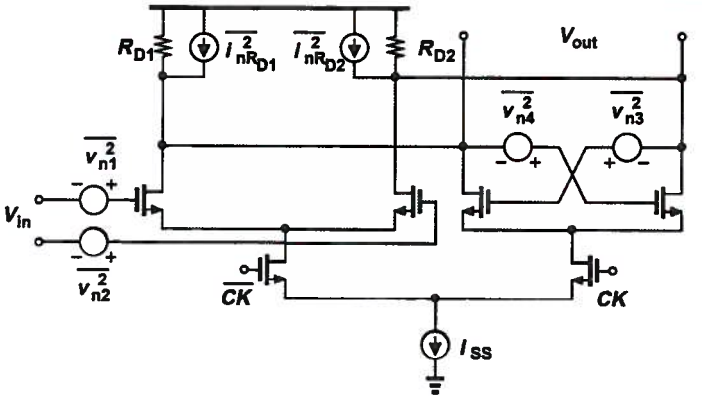
$$I_1 = \begin{cases} G_{m1}\Delta V_{TH1} \\ G_{m1}\dfrac{(V_{GS}-V_{TH})_2}{2}\dfrac{\Delta\beta_1}{\beta_1} \\ \dfrac{I_{SS}}{2}\dfrac{\Delta R_D}{R_D}, \end{cases}$$

$$I_2 = \begin{cases} G_{m3}\Delta V_{TH3} \\ G_{m3}\dfrac{(V_{GS}-V_{TH})_3}{2}\dfrac{\Delta\beta_3}{\beta_3} \\ \dfrac{I_{SS}}{2}\dfrac{\Delta R_D}{R_D}, \end{cases}$$

$$\begin{aligned} V_{OS,L}^2 = {} & (\Delta V_{TH1})^2 + \frac{(V_{GS}-V_{TH})_1^2}{4}\left(\frac{\Delta\beta_1}{\beta_1}\right)^2 \\ & + \frac{\Delta V_{TH3}^2 + \frac{(V_{GS}-V_{TH})_3^2}{4}\left(\frac{\Delta\beta_3}{\beta_3}\right)^2}{\left[G_{m1}R_D - \frac{G_{m1}}{G_{m3}}\exp\frac{(G_{m3}R_D-2)t_r}{2\alpha R_D C_L}\right]^2} \\ & + \left(\frac{\Delta R_D}{R_D}\right)^2 \frac{(V_{GS}-V_{TH})_3^2}{4\left[G_{m1}R_D - \frac{G_{m1}}{G_{m3}}\exp\frac{(G_{m3}R_D-2)t_r}{2\alpha R_D C_L}\right]^2} \\ & + \left(\frac{\Delta R_D}{R_D}\right)^2 \frac{(V_{GS}-V_{TH})_1^2}{4}. \end{aligned}$$

- **Analysis applicable to both offset and noise**

Overall Latch Noise

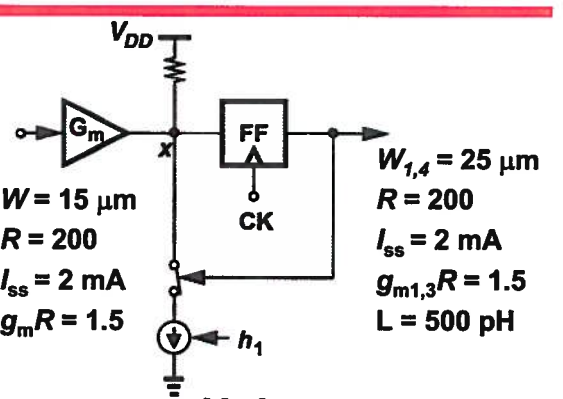


- **Input noise voltage is that random voltage waveform that keeps the latch metastable.**

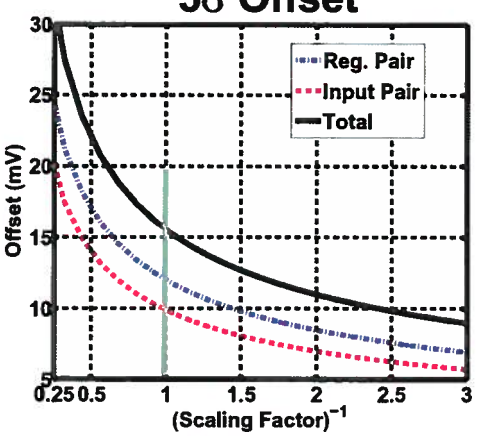
$$\overline{V_{n,in}^2} = \frac{8kT\gamma B_n}{g_{m1}} + \frac{\dfrac{8kT\gamma B_n}{g_{m3}} + 8kTR_D B_n}{\left[g_{m1}R_D - \dfrac{g_{m1}}{g_{m3}} \exp \dfrac{(g_{m3}R_D - 2)t_r}{2\alpha R_D C_L}\right]^2}$$

Scaling Example in 90-nm CMOS

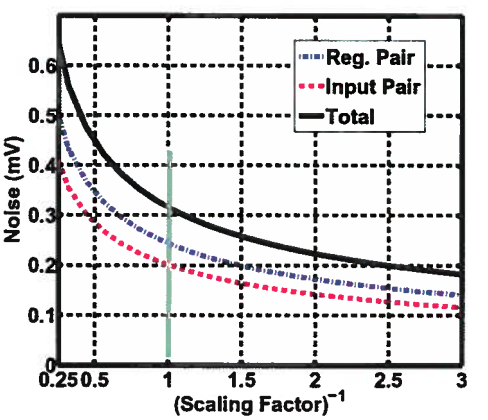
Reference Design:
10-Gb/s 1-Tap Full-Rate DFE



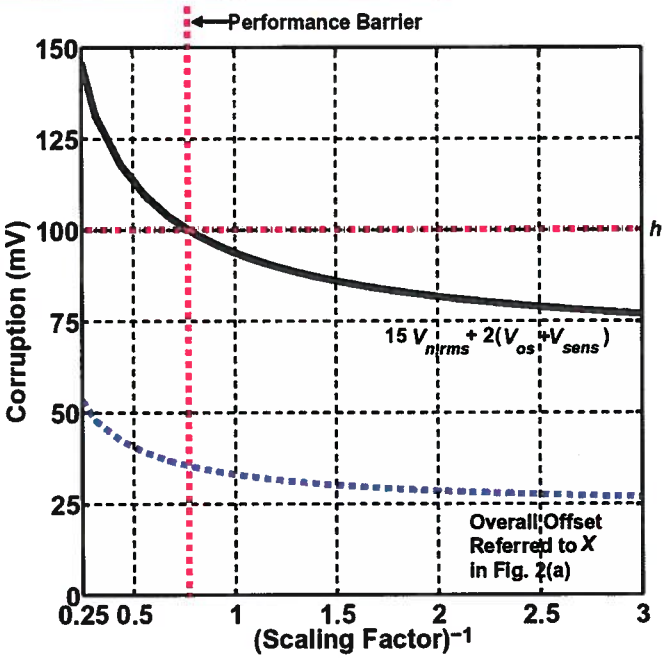
5σ Offset



Noise



Performance Barrier

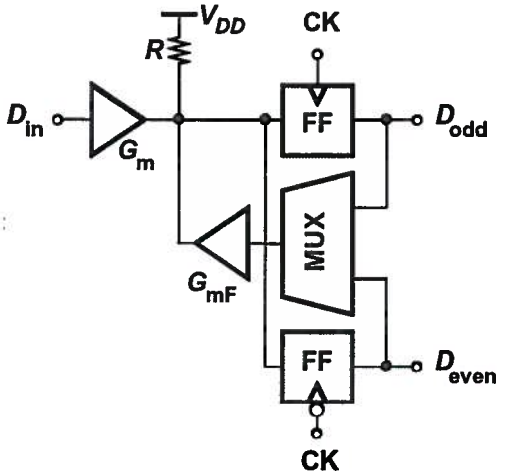


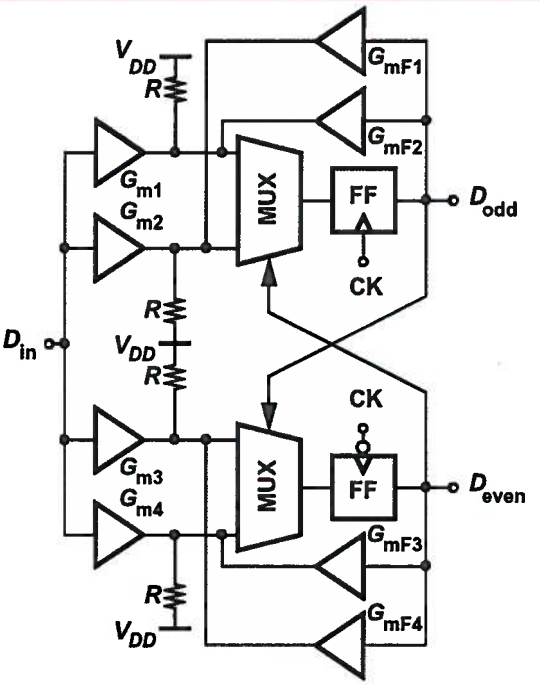
- Offset cancellation can help but it also slows down the critical path.
- Drive capability still good.

Outline

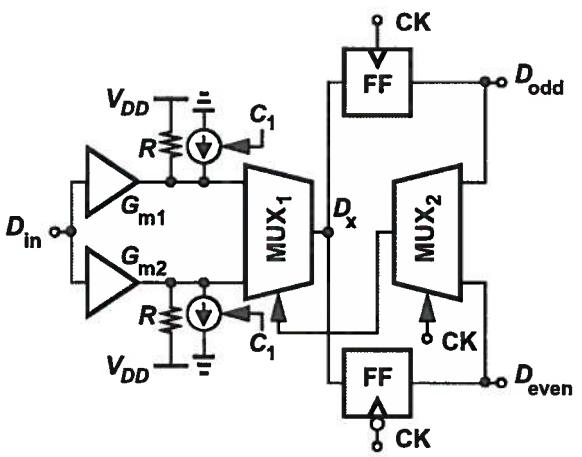
- Motivation
- Background
- Scaling limits of DFEs
- **Proposed architecture**
- **Design of building blocks**
- **Measurement results**

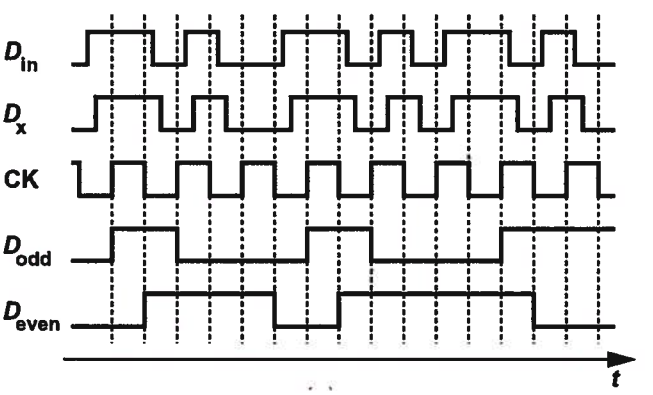
Begin with Two Half-Rate Architectures





Multiplexed Unrolled Half-Rate (MUHR) Arch.



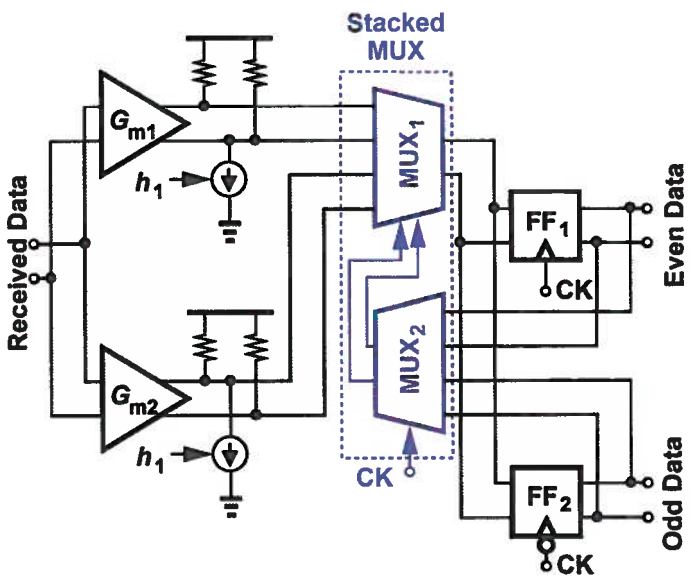


- **Two FFs sample Dx on opposite CK edges.**
- **MUX2 reproduces full-rate data and selects one of MUX1 inputs.**

$$t_{cq,FF} + t_{setup} + t_{cq,MUX_1} + t_{p,MUX_2} < UI$$

- Stack the MUX's.
- Replace flipflops by latches.
- Add gain stage before MUX.
- Use inductive peaking.

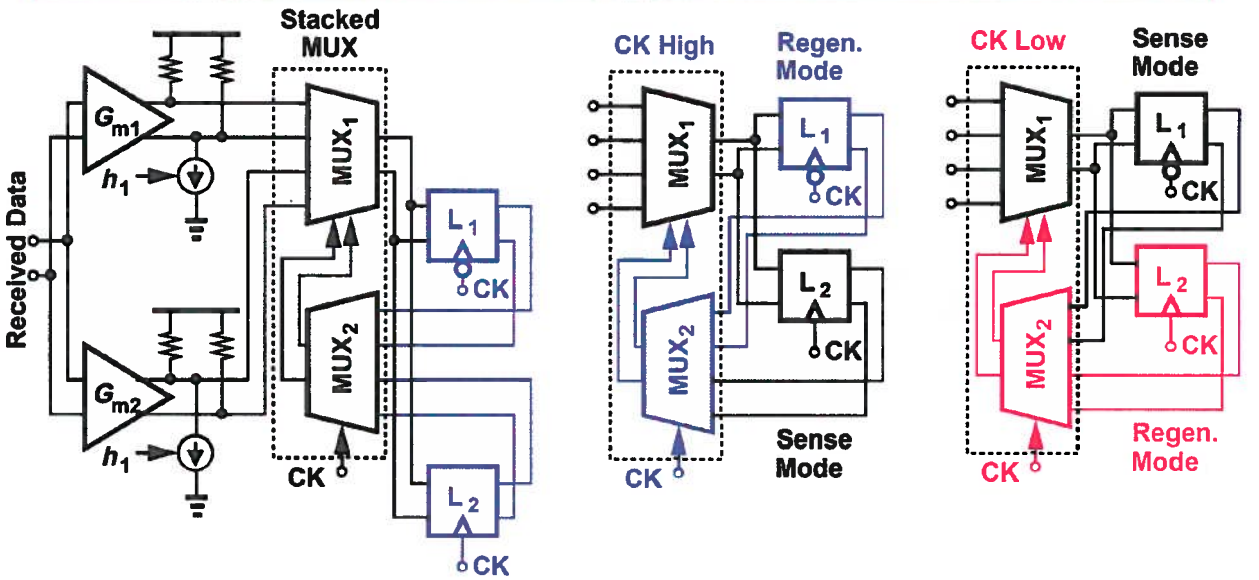
MUX Stacking



☺ Removes the delay of one MUX

☺ Reduces power consumpton and number of inductors.

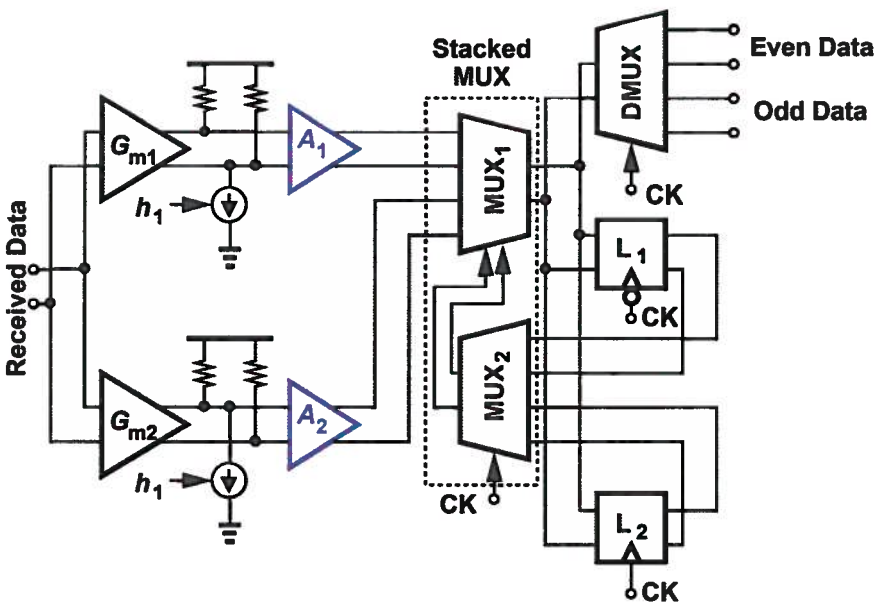
Feedback Simplification



☺ **Reduces delay of critical path to:**

$$t_{D,latch} + t_{d,SMUX} < UI$$

Addition of Gain Stages

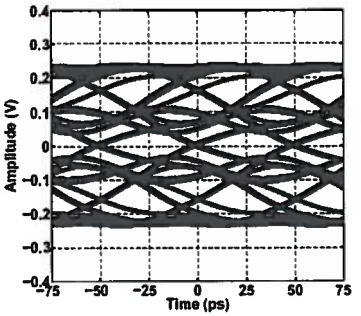


☺ **Larger swings → Faster current steering**

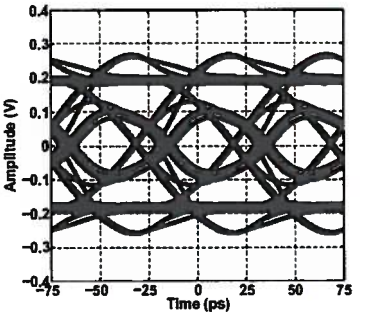
☺ **Still a better trade-off even with higher taps**

Progressive Improvement

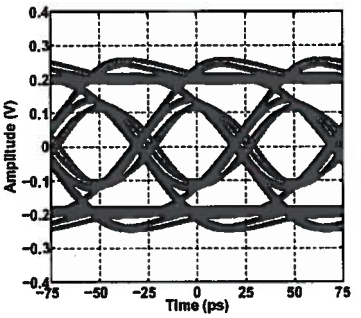
MUXed Half-Rate



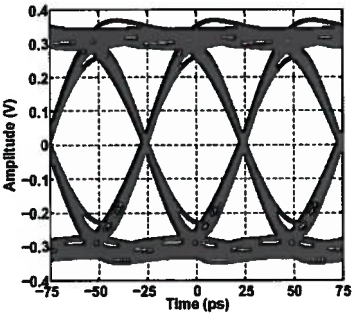
Original MUHR



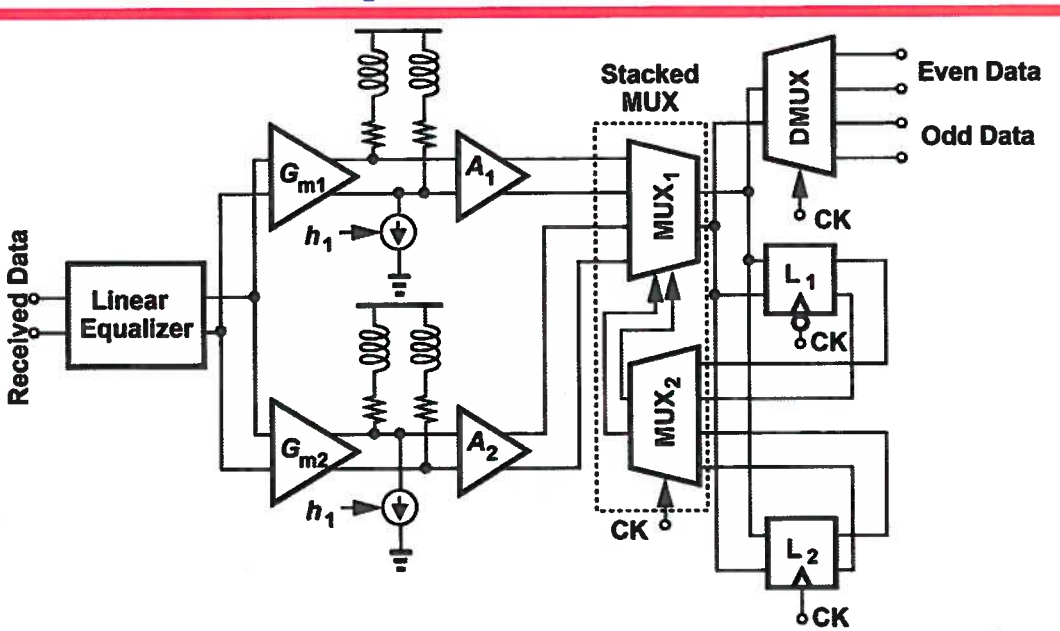
MUHR with Stacked MUX



Use of Inductive Peaking

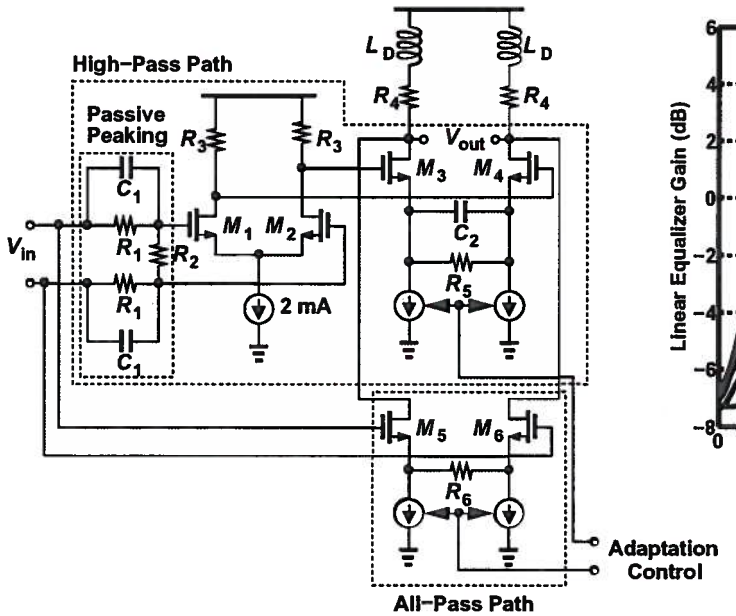


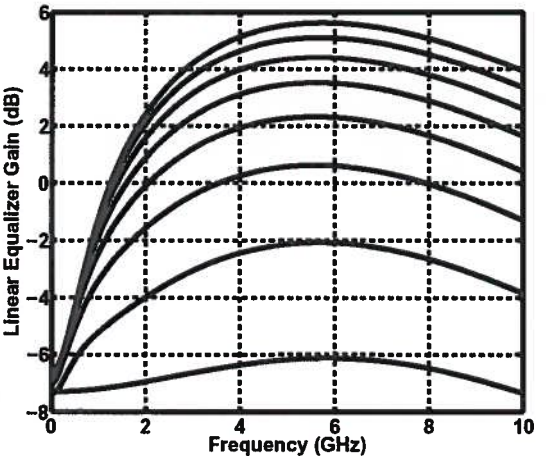
Overall Equalizer Architecture



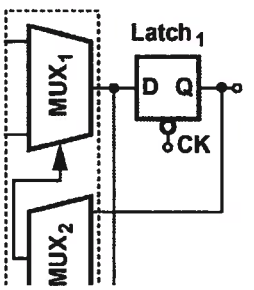
- ☺ Inductive peaking improves speed at summing nodes and latches.
- ☺ Linear equalizer assists equalization (9 dB of boost required). [Ibrahim&Razavi, ISSCC, Feb.10]

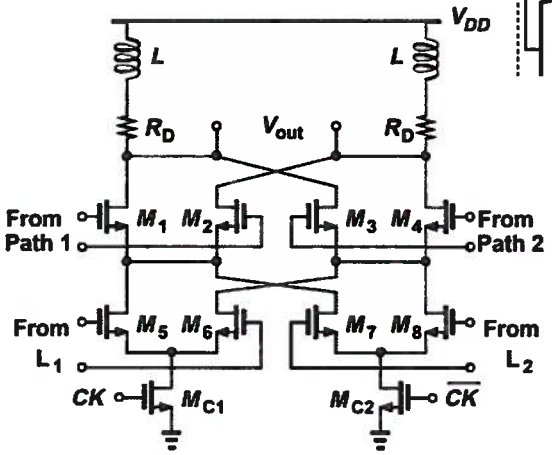
Linear Equalizer

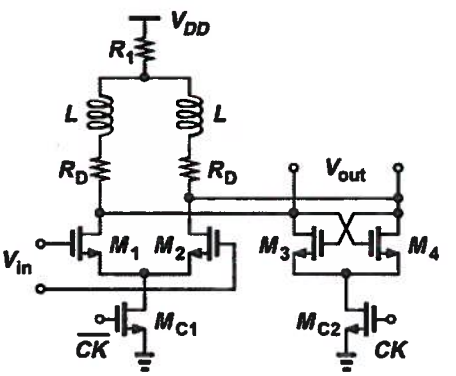




Multiplexer and Feedback Latch



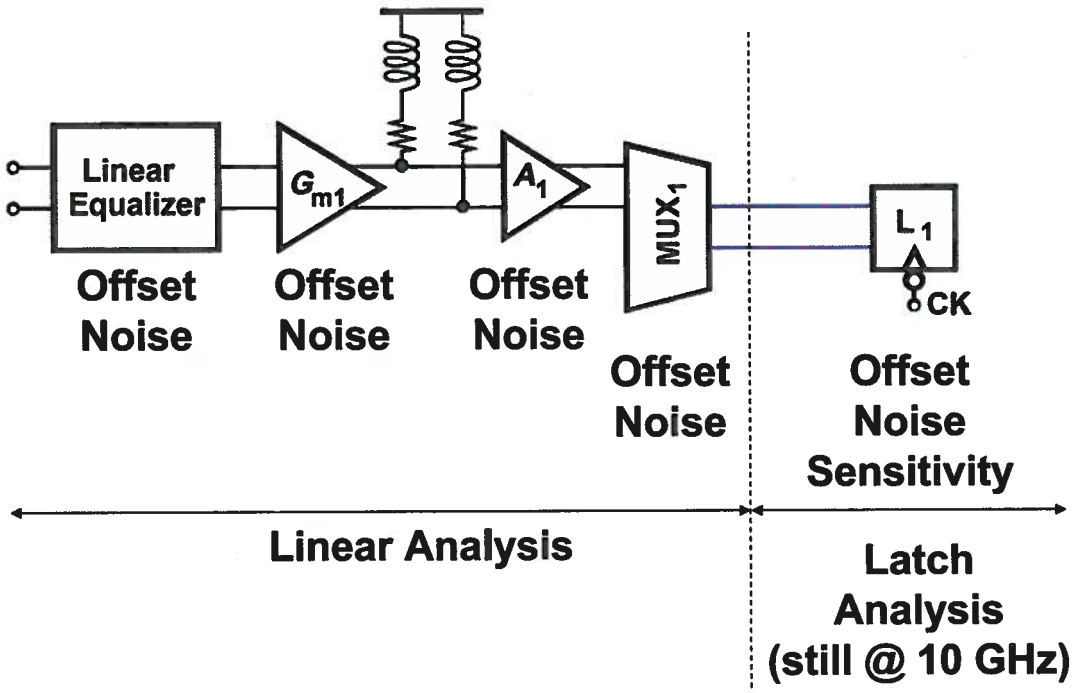




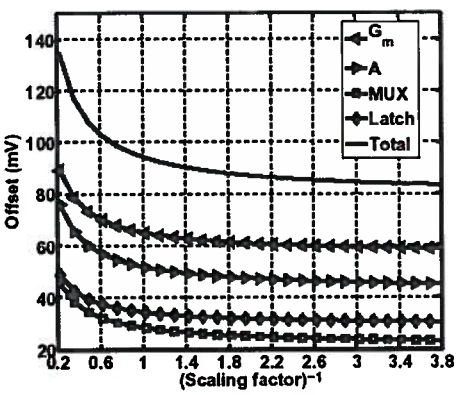
- Class-AB Clocking
- Inductive Peaking

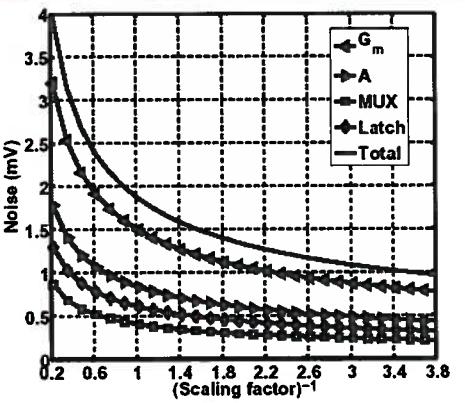
- Class-AB Clocking
- R_1 to shift output CM

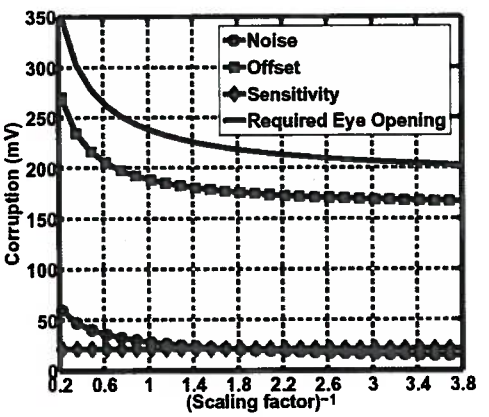
Scaling Limits of Proposed Architecture



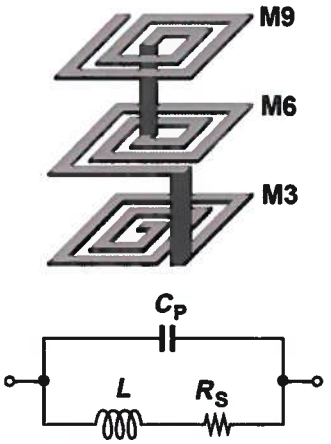
Required Eye Opening

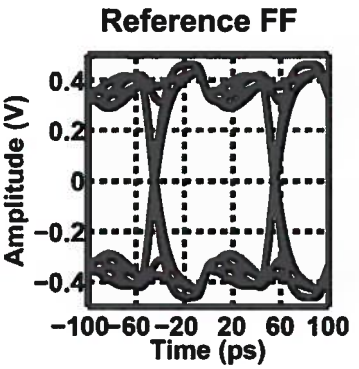


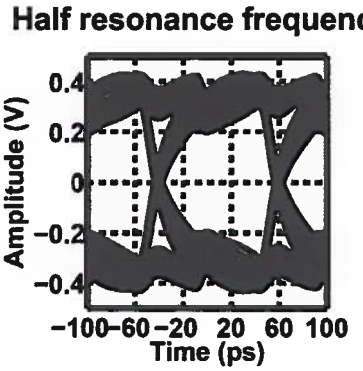




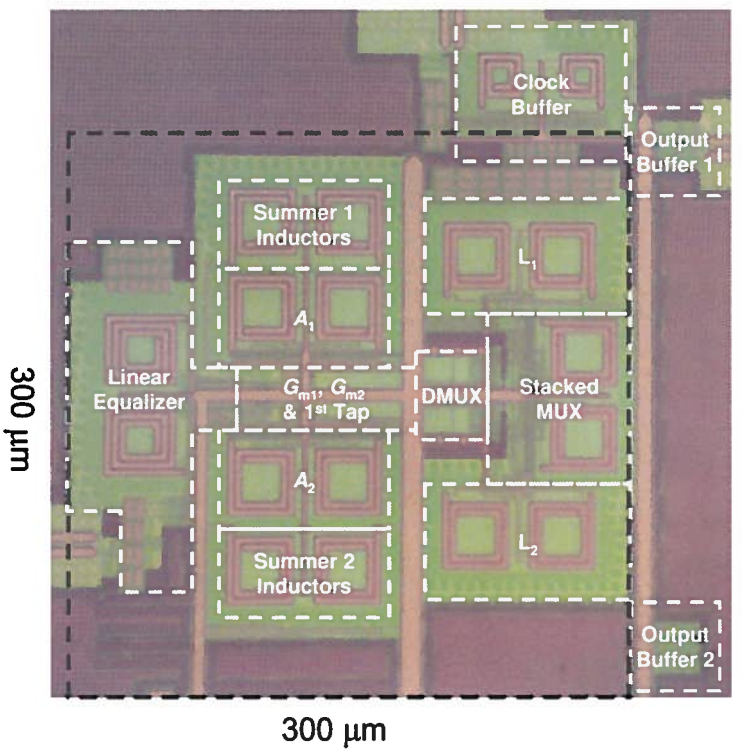
Effect of Scaling on Inductors





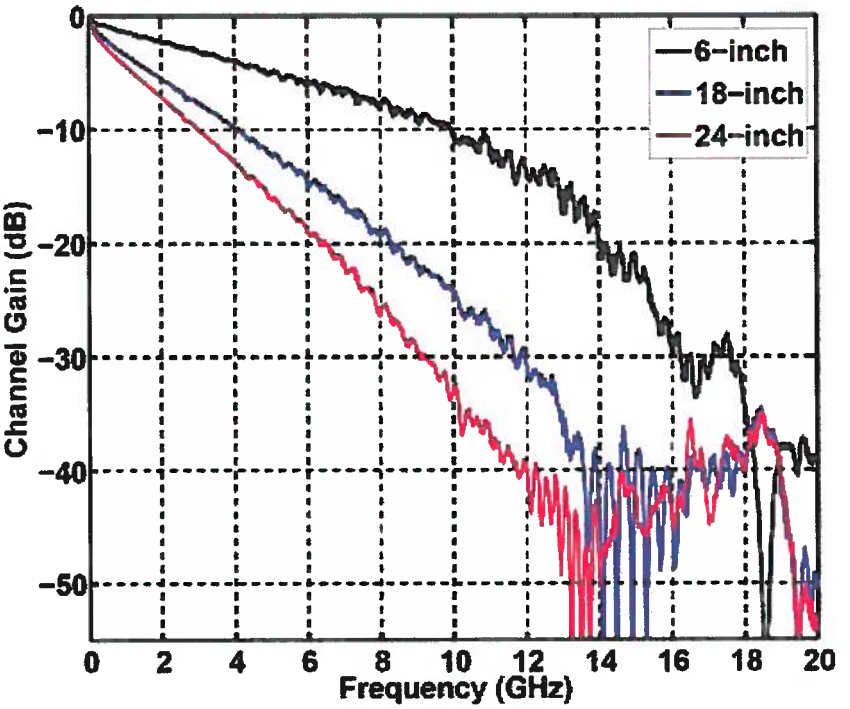


Die Photo

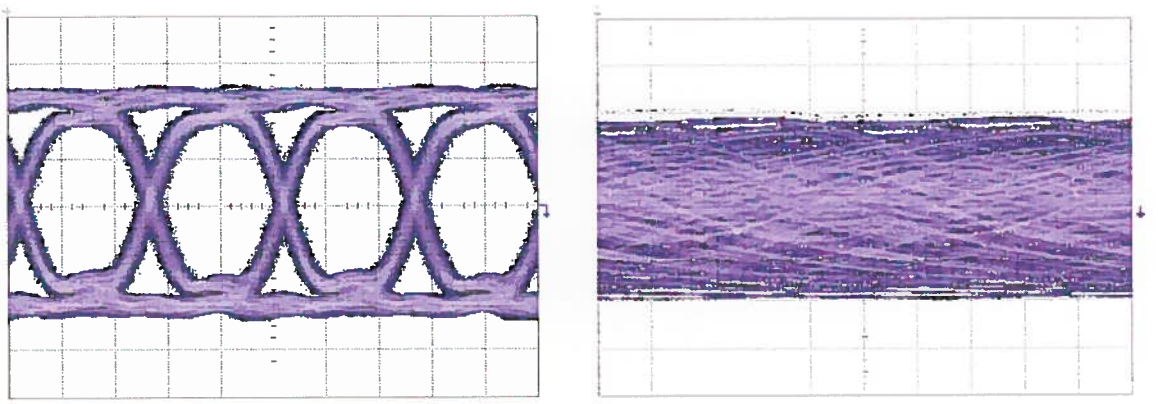


Fabricated in TSMC 90-nm CMOS technology

Measured Channel Response

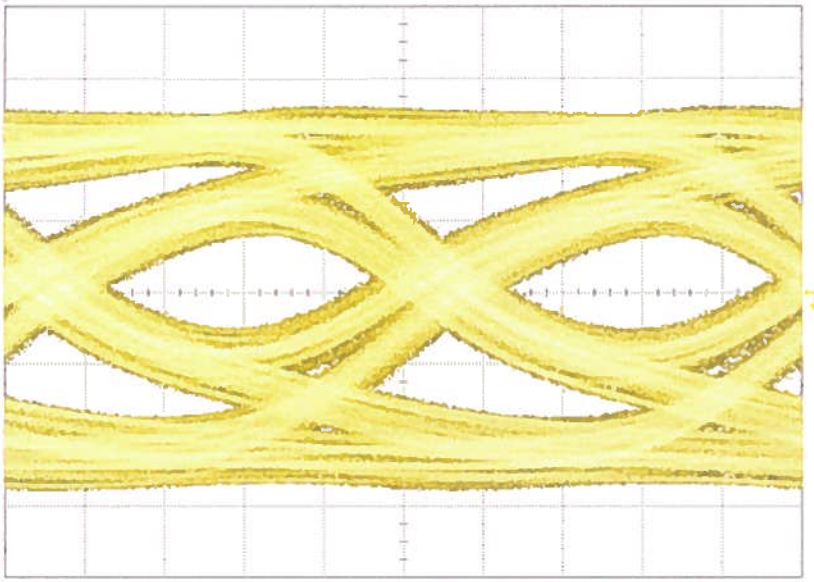


Channel Input & Output



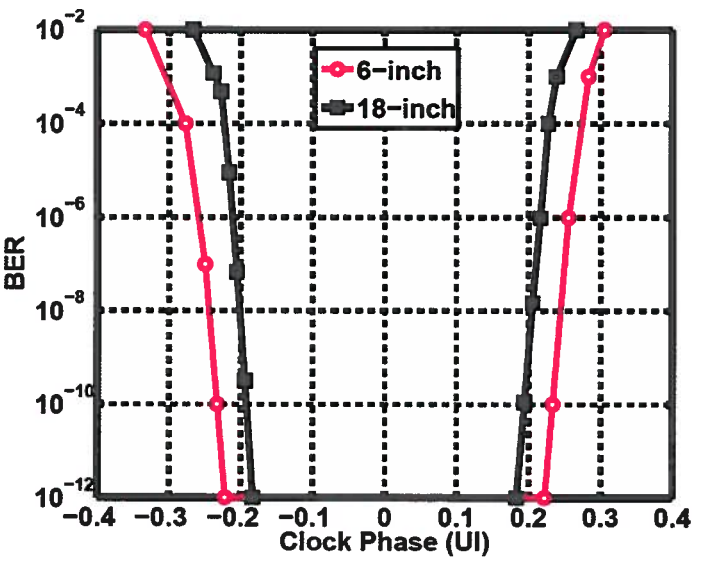
Horizontal scale: 20 ps/div
Vertical scale: 100 mV/div
20-Gb/s PRBS7 data
18-inch FR4 trace
10-ps input jitter (pp)

DMUX Output Eye



Horizontal scale: 20 ps/div
Vertical scale: 50 mV/div
20-Gb/s PRBS7 input – 10-Gb/s output

Bathtub Curves



20-Gb/s PRBS7 data
0.44 UI eye opening for 6-inch FR4 trace
0.36 UI eye opening for 18-inch FR4 trace

Power Breakdown

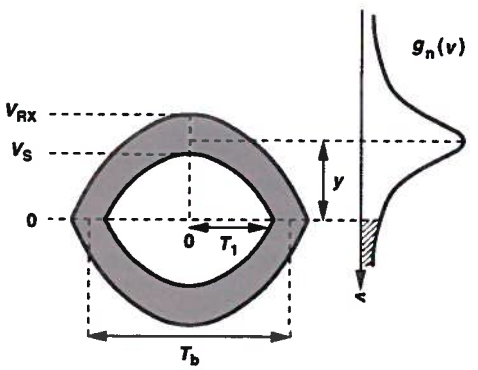
Block	Power	Delay
Linear Equalizer	5 mW	
Transconductor	3 mW x 2 = 6 mW	
Tap	30 μW x digital word	
Amplifier	4 mW x 2 = 8 mW	5 ps
SMUX	5 mW	10 ps
Latch	5 mW x 2 = 10 mW	17 ps
DMUX	20 mW	

BER Estimation

Need to consider:

- Additive Noise
- ISI
- CDR Skew
- Jitter

Effect of Noise and ISI



- **ISI Distribution:**

$$g_{ISI}(y) = \frac{1}{2(V_{RX} - V_S)} \qquad V_S < y < V_{RX},$$
$$= 0 \qquad y < V_S \text{ or } y > V_{RX}$$

- **Noise Distribution:**

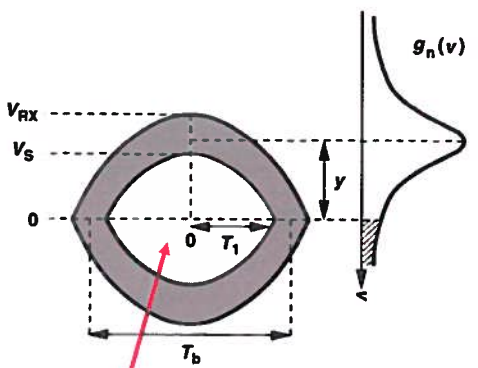
$$g_n(y) = \frac{1}{\sqrt{2\pi}\sigma_n} \exp \frac{-y^2}{2{\sigma_n}^2}$$

- **Probability of Error:** $P_e = \int_{V_S}^{V_{RX}} g_{ISI}(y) \left[\int_y^{\infty} g_n(v) dv \right] dy$

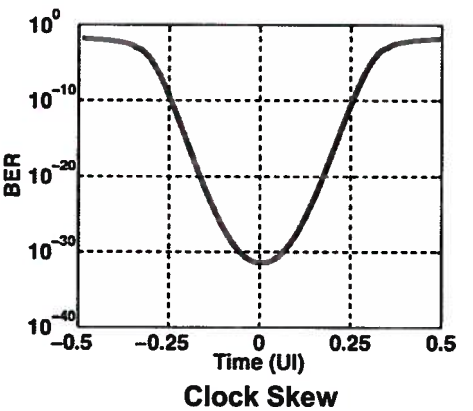
$$P_e \approx \frac{\sigma_n}{V_{RX} - V_S} \left(0.0284 \left[Q\left(\frac{V_S}{\sigma_n}\right) - Q\left(\frac{V_{RX}}{\sigma_n}\right) \right] \right.$$
$$+ 0.0118 \left[\frac{V_S}{\sigma_n} \exp\left(\frac{-V_S^2}{2\sigma_n^2}\right) - \frac{V_{RX}}{\sigma_n} \exp\left(\frac{-V_{RX}^2}{2\sigma_n^2}\right) \right]$$
$$\left. + 0.1023 \left[\exp\left(\frac{-V_{RX}^2}{2\sigma_n^2}\right) - \exp\left(\frac{-V_S^2}{2\sigma_n^2}\right) \right] \right).$$

[Gondi, JSSC, Sep. 07]

Effect of Clock Skew



$$V_{S,\text{eff}} = V_S[-(t/T_1)^2 + 1]$$



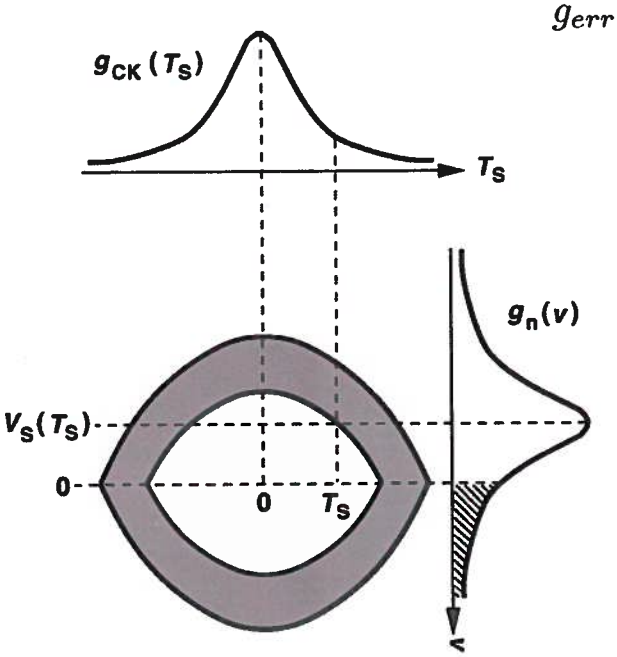
Clock Skew

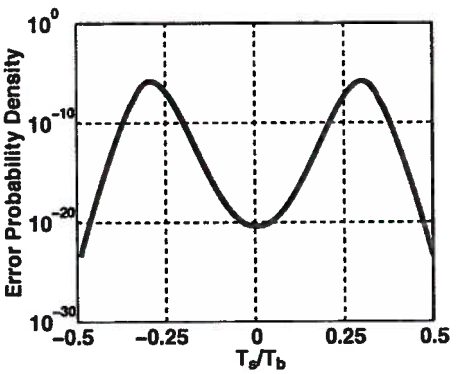
[Gondi, JSSC, Sep. 07]

Effect of Clock Jitter

- Weight P_e according to clock jitter distribution, $g_{CK}(T_s)$:

$$g_{err}(T_S) = P_e|_{V_S(T_S)} \cdot g_{CK}(T_S)$$





[Gondi, JSSC, Sep. 07]