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具有可調斜率特性的補償斜波之電流型降壓穩壓器

A Current-Mode Buck Regulator with an Adjusted-Slope Compensation Ramp

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A Current-Mode Buck Regulator with an Adjusted-Slope Compensation Ramp

by

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摘 要

包含積體功率開關和可調斜率斜波的方式的一個電流型降壓穩壓器在本論文是被實行。在電流型控制中，當工作週期大於 0.5 時，次諧波震盪是一個眾所皆知的問題。對於次諧波震盪問題的補償來說，本篇論文提及一個不同於傳統固定斜率的可調斜率補償斜波方式。這個方式可以隨著輸出電壓的不同調整適當但不會太多餘的補償斜波斜率。它不但可以像傳統一樣避免次諧波震盪的問題而且在內迴路的增益和頻寬上可以比傳統的擁有更好的效能。另外，這個方式可以有在電流感測器上節省功率的額外優點。這樣便可以減輕由於電流感測器上的功率消耗使電流型控制在效率上劣於電壓型控制的固有缺點。

這個電流型降壓穩壓器是使用台灣積體電路製造股份有限公司所提供的 0.35um 2P4M 3.3V/5V 混合訊號互補式金氧半製程來製造。晶片的全部面積大約 $1.27\times1.16mm^2$。詳細的量測和效能將在稍後幾章被描述。

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A Current-Mode Buck Regulator with an Adjusted-Slope Compensation Ramp

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Abstract

A current mode buck regulator with integrated power switches and an adjusted-slope ramp scheme is implemented in this thesis. Sub-harmonic Oscillation is a well-known problem in current mode control with the duty ratio larger than 0.5. For the compensation of sub-harmonic oscillation problem, this thesis proposes an adjusted-slope compensation ramp scheme which is not like the traditional constant-slope scheme. This scheme makes the slope of the compensation ramp appropriate but not too much for different output voltage. It not only can avoid the sub-harmonic oscillation problem like the traditional scheme but also have better gain and bandwidth in inner loop than traditional scheme. Further, this scheme has additional advantage of power-saving in current sensor. This will ease the inherent disadvantage of less efficiency in current mode control than voltage mode control due to the power dissipation of current sensor.

This current mode buck regulator is fabricated with TSMC 0.35um 2P4M 3.3V/5V Mixed Signal CMOS process. The total chip area is about $1.27 \times 1.16 mm^2$. The detailed measurement and performance is described in the following chapter.

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*The author

**The adviser

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Chapter 1

Introduction

With the rapid progress in the semiconductor technology, the chip density and operation frequency have greatly increased, making the power consumption in digital circuits also have the same trend. For battery-operated portable electronic devices, although the rapid progress can make their size and weight smaller and lighter, extra high power consumption will greatly reduce the battery life and increase inconvenience for people.

An effective method for low-power design is to reduce the supply voltage while satisfying the performance constraints. This voltage scaling method [1] typically present in portable electronic devices shown in Fig.1.1 scales the supply voltage through a step-down DC/DC regulator to a lower voltage in order to reduce power dissipation [2].

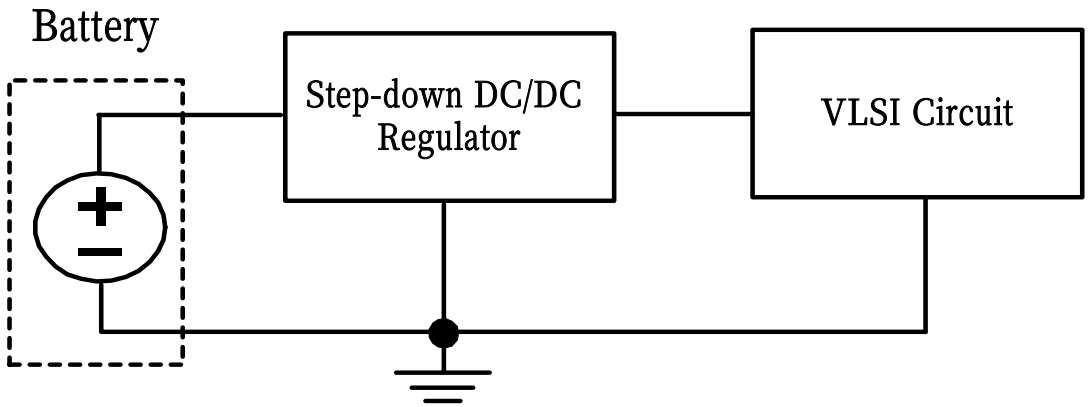


Fig.1.1 An integrated model of portable electronic devices

From Fig.1.1, it can be seen that the step-down DC/DC regulator plays an important role in

the aspect of lengthening the battery life. Therefore, how to choose an appropriate step-down DC/DC regulator to optimum the performance, efficiency and so on of the system will be a major concern for VLSI designers.

1.1 Motivation

Generally, the step-down DC/DC regulator can distinguish into two categories. One is the linear regulator shown in Fig. 2.1 (a) and the other is the switching regulator shown in Fig. 2.1(b) [3] [4].

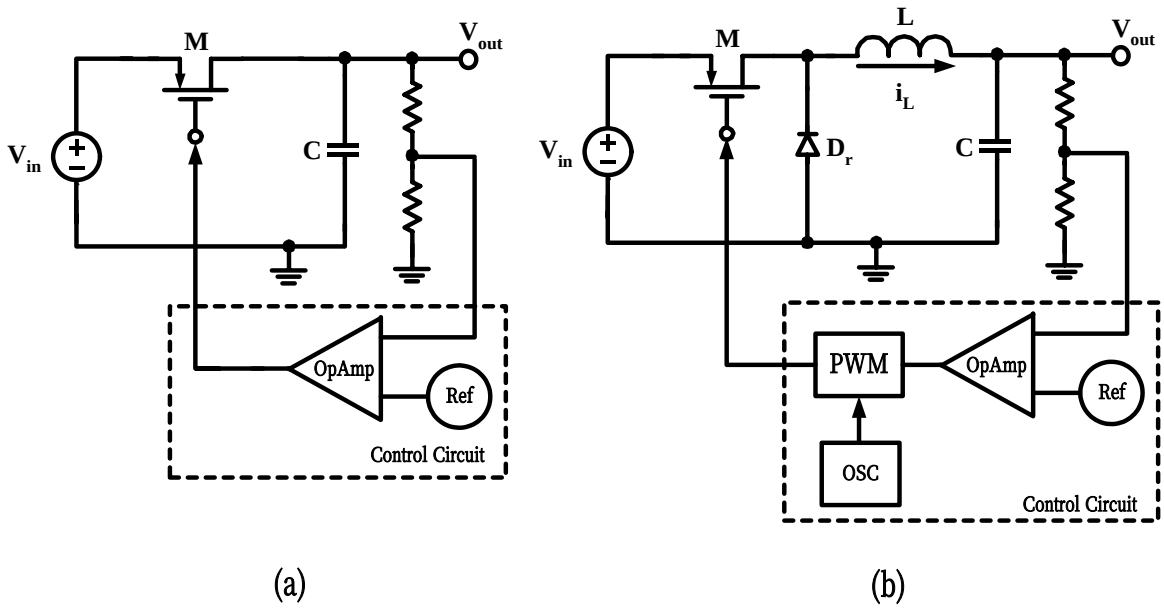


Fig.1.2 The structure of (a) the linear regulator (b) the switching regulator

In the aspect of structure, both the core circuit and the control circuit of the switching regulator are more complex than that of the linear regulator. In the aspect of speed, the switching regulator due to the limitation of switching frequency is slower than the linear regulator. In the aspect of output voltage, due to the driving signal which is analog in the linear regulator but is digital in the switching regulator of the transistor 'M1', the output voltage of the linear regulator is more noiseless than that of the switching regulator. But it is well known that the switching regulator is characterized by its high efficiency and large density of power by volume unit, surpassing actual possibilities of the linear regulator. The conversion efficiency of the switching regulator is typically 70~90% as opposed to 30~50% for linear regulator. Consequently, the switching regulator is more suitable for portable application than the linear regulator. So the research topic of my thesis

concentrates on the switching regulator.

In this thesis, a current mode buck regulator is implemented. The buck regulator scales a supply voltage to a lower output voltage in order to lengthening the life of the supply source. The current mode control for the switching regulator has the advantages of faster line-to-output transient response and easier design of compensation than the voltage mode control [5], [7]. For inherent sub-harmonic oscillation [5], [6], [7] in current mode control, this thesis proposes an adjusted-slope ramp scheme which is not like the traditional constant-slope one. This scheme adjusts the slope of the ramp which is enough but not too over to follow different output voltage. It not only can avoid the sub-harmonic oscillation problem like the traditional one but also have better performance of gain and bandwidth than traditional one. Further this scheme has additional advantage of power-saving in current sensor. This phenomenon will reduce power loss in current mode control and ease the inherent disadvantage of the efficiency in current mode control which is worse than voltage mode control due to the power dissipation of current sensor. As a result, this regulator in my design, the conversion efficiency can be up to 92% and it is suitable for the application of portable products.

1.2 Organization

This thesis is organized as six chapters. Brief content of each chapter is described as follows. In chapter 2, the fundamental concepts of the switching regulator are described. Firstly, some specification of the switching regulator is introduced. Secondly, three basic topology of the dc/dc switching regulator are presented. Finally, various control scheme in feedback are illustrated and comparison. In chapter 3, firstly, the current mode buck regulator stage which is implemented in this thesis is explained including large signal and small signal in detail. Secondly, the proposed improvement is described and implemented in this system. Finally, the stability of the whole system is considered. Chapter 4 extends this design into circuit level. Every circuit in this system is described and analyzed. And simulation results are also shown and described in this chapter. Chapter 5 presents the physical consideration and the results of measurement in this design. Chapter 6 offers some conclusions and recommendations for future work.

Chapter 2

Fundamentals of Switching Regulator

2.1 Specification of Switching Regulator [5]

2.1.1 Input Voltage

This index means the some input voltages which let the performance of this regulator conform to the desired specification. It is usually specified, whether ac or dc, together with the voltage range.

2.1.2 Output Voltage Ripple

In dc/dc regulator, the output voltage ripple is mainly decided by output filter capacity, switching frequency and voltage spike. It is normally expressed as peak-to-peak voltage. Sometimes it is given as a percentage of the nominal output voltage or as a root mean square voltage. As for the reduction of output voltage ripple, it can be implemented by increasing the output filter capacity, increasing the switching frequency, decreasing the effect of the inductance in fast transient large current ports etc.

2.1.3 Regulation

This is an index about influence of outside environment on output voltage. It is the measurement of how close the output voltage stays to its nominal value over full range of operating conditions. In general, it is divided into three components: line, load, and temperature regulation.

1. Line Regulation

Line Regulation is a measurement of the effect of changes in the input voltage on the output voltage. There are usually two methods to define line regulation. The first definition is percentage of changes in output voltage versus changes in input voltage. It is defined as

$$\text{Line Regulation 1} \equiv \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\% \quad (\%/V) \tag{2-1}$$

The second definition includes the parameter of output nominal voltage into the first definition. So its value is highly related to output dc voltage. It is defined as

$$\text{Line Regulation 2} \equiv \frac{\Delta V_{out}}{\Delta V_{in}} \times \frac{1}{V_{nom}} \times 100\% \quad (\%/V) \tag{2-2}$$

2. Load Regulation

Load Regulation is the percentage change in steady output voltage when load current is in different condition. (It usually considers maximum current and minimum current) There are usually two methods to define load regulation. The first definition is as

$$\text{Load Regulation 1} \equiv \frac{\Delta V_{out}}{\Delta I_{load}} \times 100\% \quad (\%/A) \tag{2-3}$$

The second definition includes the parameter of output nominal voltage into the first definition. So its value is highly related to output dc voltage. It is defined as

$$\text{Load Regulation 2} \equiv \frac{\Delta V_{out}}{\Delta I_{load}} \times \frac{1}{V_{nom}} \times 100\% \quad (\%/A) \tag{2-4}$$

3. Temperature Regulation

Temperature Regulation is the effect of change in environmental temperature on the output voltage. There are usually two methods to define temperature regulation. The first definition is as

$$\text{Temperature Regulation 1} \equiv \frac{\Delta V_{out}}{\Delta T} \times 100\% \quad (\%/°C) \tag{2-5}$$

The second definition includes the parameter of output nominal voltage into the first definition. So its value is highly related to output dc voltage. It is defined as

$$\text{Temperature Regulation 2} \equiv \frac{\Delta V_{out}}{\Delta T} \times \frac{1}{V_{nom}} \times 100\% \quad (\%/°C) \tag{2-6}$$

Although many factors influence regulation of output voltage, the regulator usually

has a feedback circuit to compensate for such changes and keep output voltage within desired limits.

2.1.4 Transient Response

Transient Response is defined as a variation of output voltage when load current suddenly changes from one level to other level. In past, this parameter is often ignored in industry. But in present age of high speed electronic manufactures, this parameter is more and more important because most kinds of electronic manufacture need a large number of current in few microseconds even in few nanoseconds. If the regulator does not keep its output voltage which is supplied to electronic manufactures not change drastically in a big variation of load current, it will highly affect performance of electronic manufactures. So the consideration of transient response is more and more critical.

The transient response is mainly influenced by the bandwidth of regulator, output capacitor, and equivalent series resistance of output capacitor. There are two definitions to show characteristics of the transient response. One is “Deviation of Output Voltage”, and the other is ”Recovery Time ”. The two definitions will be explained in Fig.2.1 and Fig.2.2. Fig.2.1 shows a basic switching regulator and a dynamic output load. Fig.2.2 shows characteristics of the transient response.

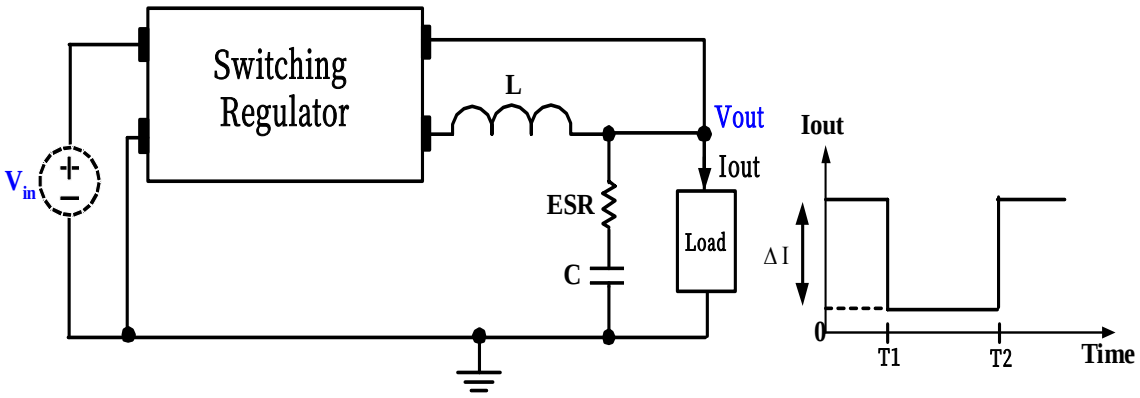


Fig.2.1 A basic switching regulator and a dynamic output load

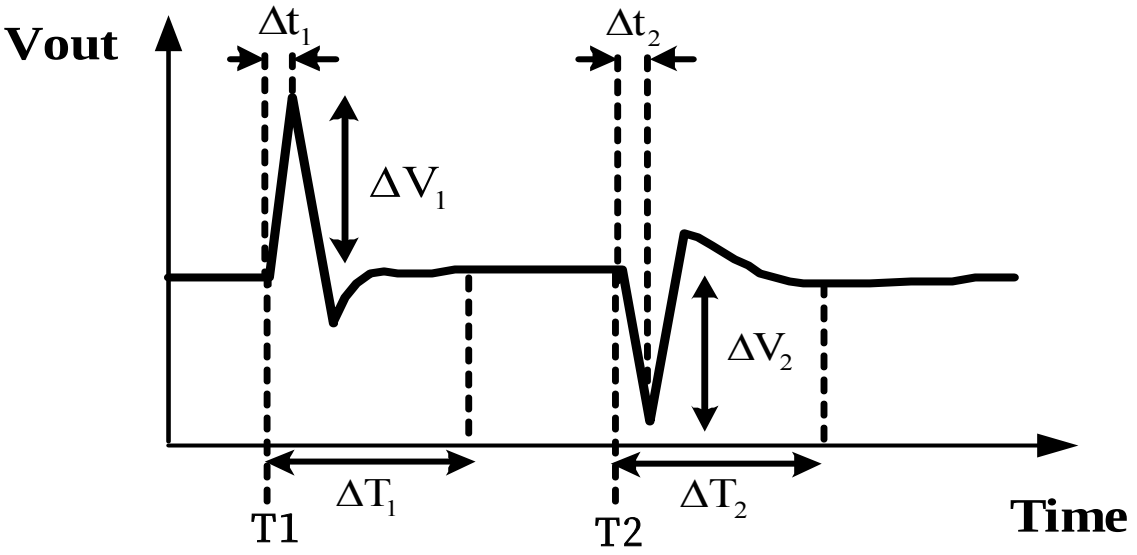


Fig.2.2 The Transient Response of Output Voltage

Fig.2.1 shows that a load current of switching regulator suddenly change from full load to light load at T1 and from light load to full load at T2. Fig.2.2 shows the transient response of output voltage to sudden changes in load current. This figure is divided to two conditions.

Condition 1: full load to light load

$$\text{Deviation of output voltage} = \Delta V_1 = \frac{\Delta I \times \Delta t_1}{C} + \Delta I \times ESR \quad (2\text{-}7)$$

$$\text{Recovery time} = \Delta T_1 \quad (2\text{-}8)$$

Condition 2: light load to full load

$$\text{Deviation of output voltage} = \Delta V_2 = \frac{\Delta I \times \Delta t_2}{C} + \Delta I \times ESR \quad (2\text{-}9)$$

$$\text{Recovery time} = \Delta T_2 \quad (2\text{-}10)$$

In general, Deviation of output voltage and recovery time is chosen maximum value between condition1 and condition 2. So the result is defined as

$$\text{Deviation of output voltage} = \max(\Delta V_1 , \Delta V_2) \quad (2\text{-}11)$$

$$\text{Recovery time} = \max(\Delta T_1 , \Delta T_2) \quad (2\text{-}12)$$

2.1.5 Efficiency

The efficiency of regulator is very important topic in electronic system. In general, the regulator converts a dirty voltage and current into a clean voltage and current. So the

regulator is equal to a medium in electronic system. Since it is only a medium, the power loss is as less as it can be. The less energy the regulator requires, the more energy the other main electronic circuits can obtain. If the regulator has low efficiency, not only power is wasted but also unnecessary heat is produced, which will increase extra weight and cost.

The efficiency in switching regulator as Fig.2.3 is defined as the ratio of the output power to input power.

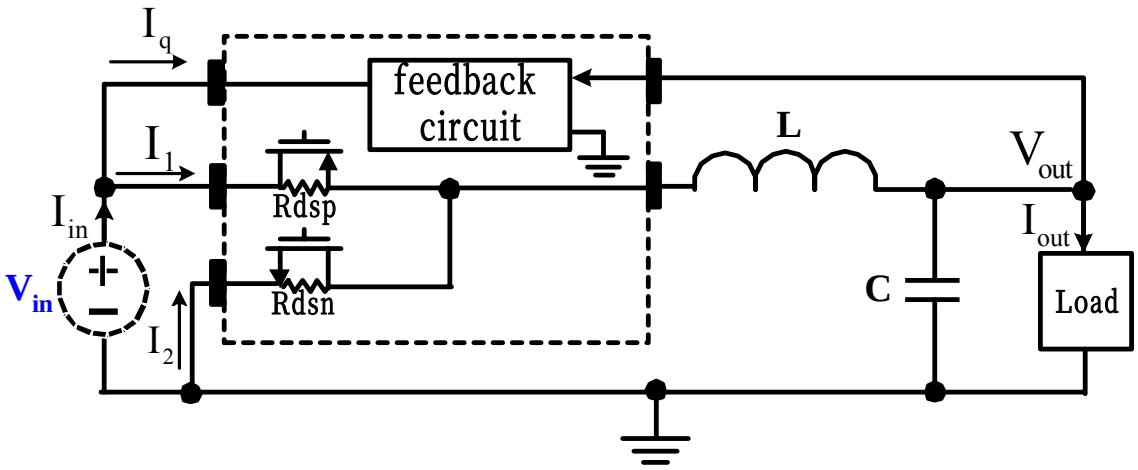


Fig.2.3 The basic switching regulator

From Figure.2.3, the efficiency is calculated as follows:

$$\text{Efficiency} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} \times 100\%$$

$$\Rightarrow \text{Efficiency} = \frac{V_{out} \times I_{out}}{(V_{out} \times I_{out}) + (V_{in} \times I_q) + (I_1^2 \times R_{dsp} + I_2^2 \times R_{dsn})} \times 100\% \quad (2\text{-}13)$$

In denominator, the first term $V_{out} \times I_{out}$ means output power consumption, and the second term $V_{in} \times I_q$ means quiescent power consumption which means the power consumption in the chip when no output current is desired, and the third term $(I_1^2 \times R_{dsp} + I_2^2 \times R_{dsn})$ means power consumption in power transistor which includes conduction loss and switching loss. According to the above equation, the second term and the third term in denominator must be minimized to improve efficiency. Saving power consumption in feedback circuit can decrease the value of the second term. Adopting a transistor with large W/L ratio can decrease the resistance of transistor, and then decrease the value of the third term. By doing more, the efficiency will be improved better.

2.1.6 Electromagnetic Interference (EMI)

This problem normally does not happen in linear regulator or low frequency switching regulator, but the problems associated with EMI increase with frequency. EMI is spurious electromagnetic energy that pollutes the local environment around a noise-generating source. This electromagnetic energy generates both electric and magnetic fields, which can propagate into the environment in two ways. One way is via the high frequency noise currents that flow through the interface lines (conducted emissions). The other way is via radiation through the atmosphere surrounding the noise-generating source (radiated emissions). In this thesis, we focus on the conducted emissions and construct the input filter to reduce the influence of conducted emissions.

2.2 Summary of Basic Switching DC-DC Regulators [5] [6] [7]

2.2.1 Three Circuits

Switching DC-DC regulator is divided to three circuits as Table 2.1 by their dc conversion ratios.

Table 2.1 The characteristics of switching DC-DC regulators

Circuits	**Output vs. Input**	**Polarity of output**
Buck	Step-down	Same polarity
Boost	Step-up	Same polarity
Buck-Boost	Step-down or Step-up	Inverse polarity

1. Buck regulator

The buck regulator, Fig.2.4(a), is a well-known switching regulator that is capable of producing a dc output voltage smaller in magnitude than the dc input voltage.

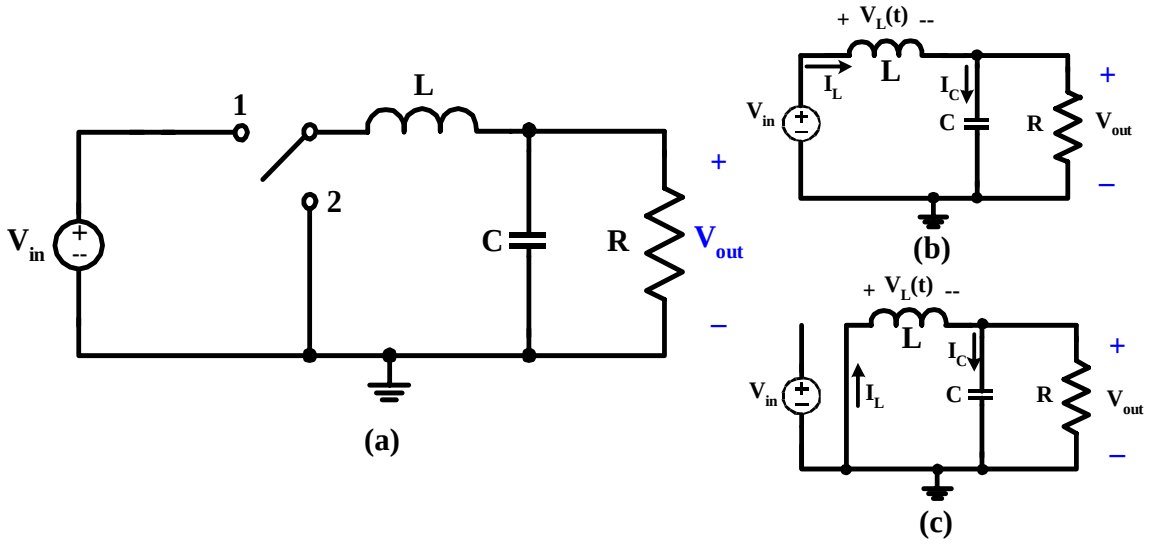


Fig.2.4 Buck regulator: (a) circuit (b) the switch in 1 (c) the switch in 2

From Fig.2.4, with the switch in position 1, the inductor voltage is equal to V_{in} - V_{out}, and with the switch in position 2, the inductor voltage is equal to - V_{out}, as shown in Fig.2.5.

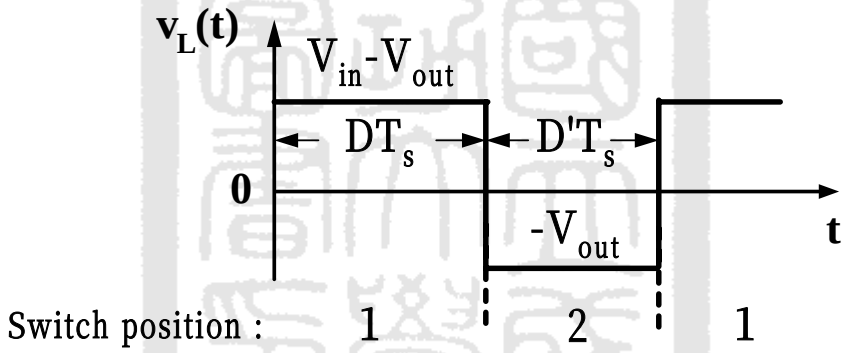


Fig.2.5 Steady-state inductor voltage waveform, buck regulator

In steady state, the net volt-seconds applied to an inductor must be zero. By equating $\langle v_L \rangle$ to zero, and noting that $D+D' = 1$, one obtains $D(V_{in}-V_{out})+D'(-V_{out}) = 0$ .Solution for conversion ratio yields conversion ratio = V_{out}/V_{in}=D as shown in Fig.2.6

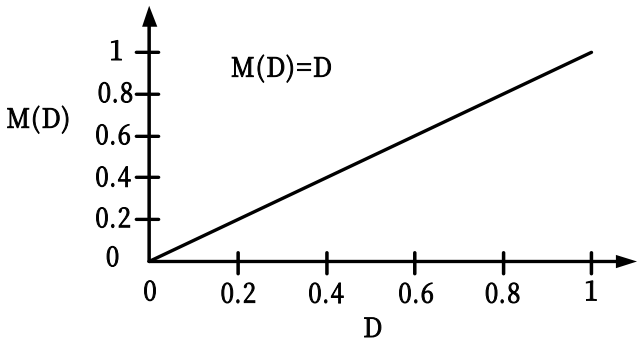


Fig.2.6 Conversion ratio of buck regulator M(D)=V_{out}/V_{in}

2. Boost regulator

The boost regulator, Fig.2.7(a), is another well-known switching regulator that is capable of producing a dc output voltage greater in magnitude than the dc input voltage.

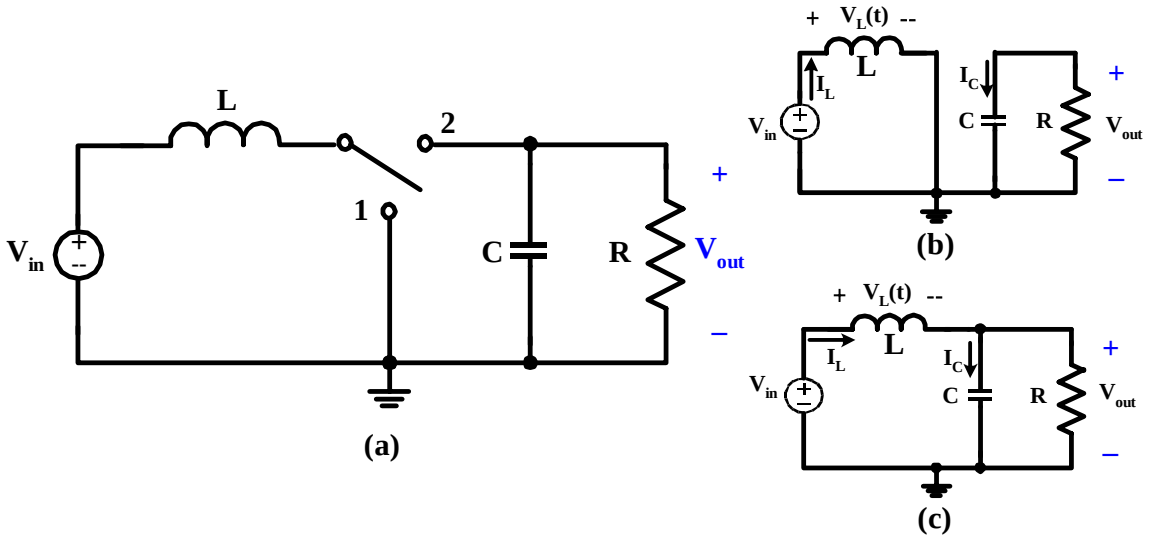


Fig.2.7 Boost regulator: (a) circuit (b) the switch in 1 (c) the switch in 2

From Fig.2.7, with the switch in position 1, the inductor voltage is equal to V_{in}, and with the switch in position 2, the inductor voltage is equal to V_{in} - V_{out}, as shown in Fig.2.8.

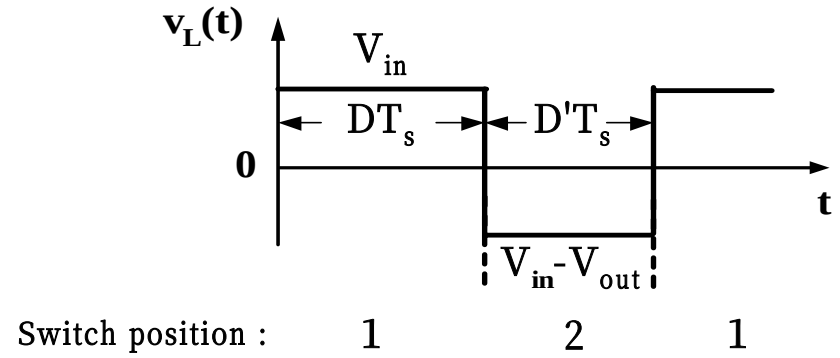


Fig.2.8 Steady-state inductor voltage waveform, boost regulator

In steady state, the net volt-seconds applied to an inductor must be zero. By equating $\langle v_L \rangle$ to zero, and noting that $D+D' = 1$, one obtains $D(V_{in})+D'(V_{in}-V_{out}) = 0$ .Solution for conversion ratio yields conversion ratio = $V_{out}/V_{in}=1/D'$ as shown in Fig.2.9

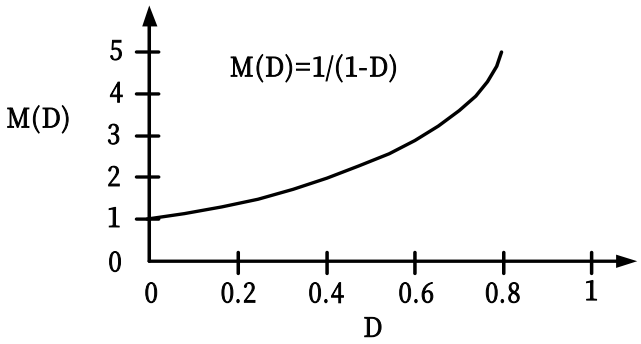


Fig.2.9 Conversion ratio of boost regulator $M(D)=V_{out}/V_{in}$

3. Buck-boost regulator

The buck-boost regulator, Fig 2.10(a), is capable of producing a dc output voltage either greater or smaller in magnitude than the dc input voltage, and it inverts the polarity of dc output voltage.

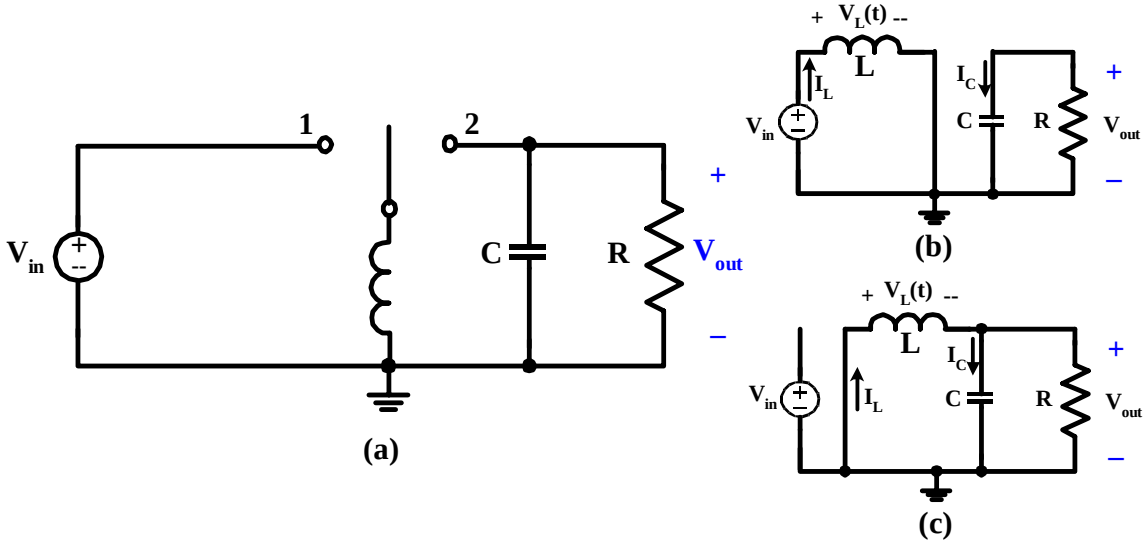


Fig.2.10 Buck-Boost regulator : (a) circuit (b) the switch in 1 (c) the switch in 2

From Fig.2.10, with the switch in position 1, the inductor voltage is equal to V_{in}, and with the switch in position 2, the inductor voltage is equal to V_{out}, as shown in Fig.2.11.

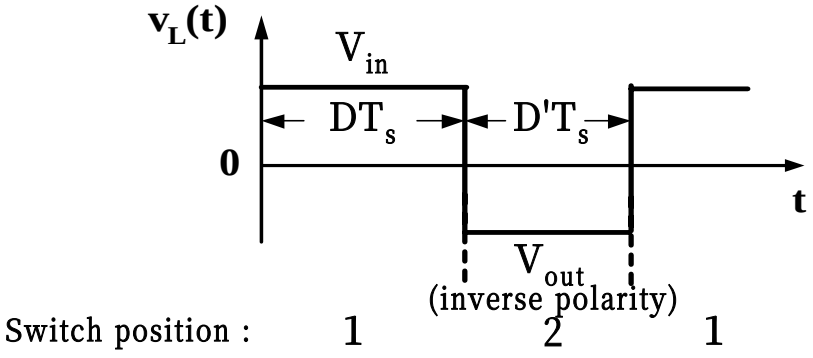


Fig.2.11 Steady-state inductor voltage waveform, buck-boost regulator

In steady state, the net volt-seconds applied to an inductor must be zero. By equating $\langle v_L \rangle$ to zero, and noting that $D+D' = 1$, one obtains $D(V_{in})+D'(V_{out}) = 0$ .Solution for conversion ratio yields conversion ratio = V_{out}/V_{in} = - D/D' as shown in Fig.2.12

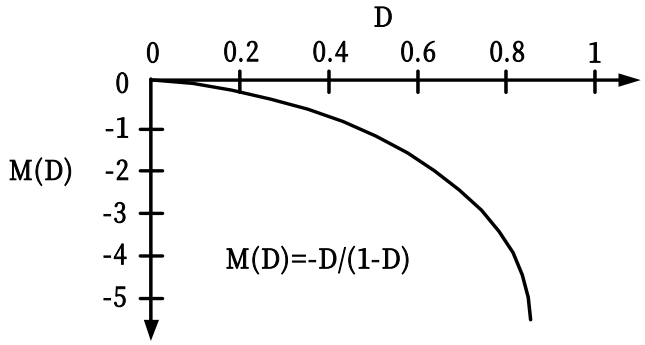


Fig.2.12 Conversion ratio of buck-boost regulator $M(D)=V_{out}/V_{in}$

2.2.2 Estimation of Output Voltage Ripple

Consider the buck regulator of Fig.2.13(a). The inductor current $i_L(t)$ contains a dc component I and linear ripple of peak magnitude Δi_L as shown in Fig.2.13(b).

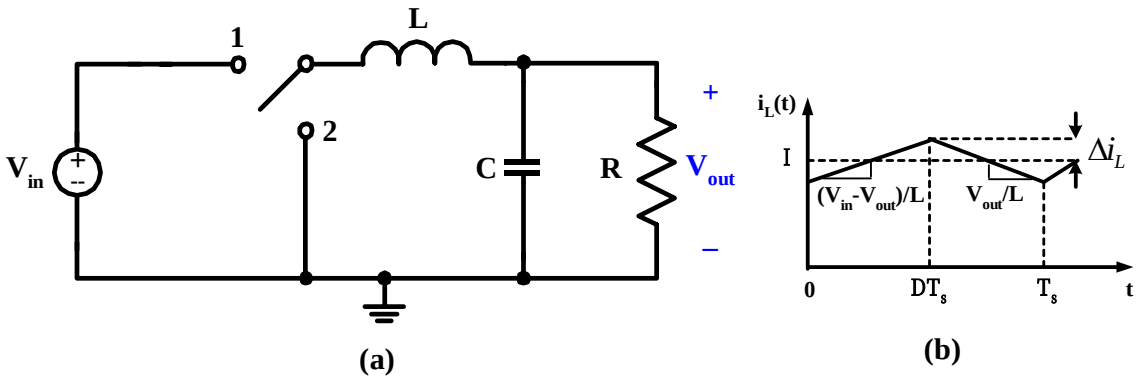


Fig.2.13 Buck regulator: (a) circuit (b) steady-state inductor current waveform

In a well designed converter, in which the capacitor provides significant filtering of switching ripple, the capacitance is chosen large enough that its impedance at the switching frequency is much smaller than the load impedance. Hence nearly all of the inductor current ripple flows through the capacitor, and very little flows through load. The capacitor current is equal to the inductor without dc component as Fig.2.14 (a). The current ripple is linear, with peak value Δi_L.

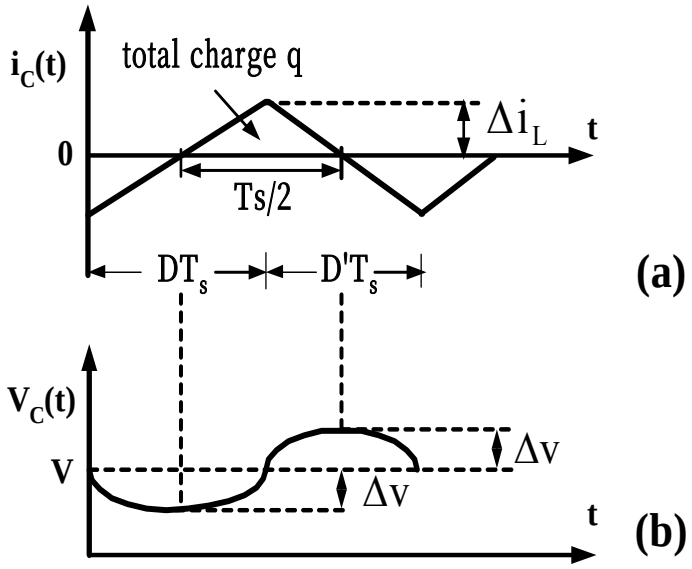


Fig.2.14 Buck regulator, (a) output capacitor current (b) output capacitor voltage

From Fig.2.14, by the capacitor relation Q=CV, q of the Fig.2.14 is calculated as

$$q = C(2\Delta v) \text{ ...(1) and } q=\frac{1}{2}\Delta i_L \frac{T_s}{2} \text{...(2)} \qquad (2\text{-}14)$$

By make (1) and (2) of (2-14) equal, the solution for the voltage ripple peak magnitude Δv yields

$$\Delta v = \frac{\Delta i_L T_s}{8C} \qquad (2\text{-}15)$$

This expression is used without consideration of capacitor equivalent series resistance (ESR). In practice, the additional voltage ripple caused by ESR must be included. The voltage ripple with ESR is calculated as

$$\Delta v = i_C(t) \times ESR + \frac{\Delta i_L T_s}{8C} = \Delta i_L T_s \times (ESR + \frac{Ts}{8C}) \qquad (2\text{-}16)$$

In general, the ripple caused by first term 'ESR' is much greater than caused by second term'Ts/8C'. So consideration of ESR is essential for estimation of output voltage ripple in switching regulator.

2.2.3 The Discontinuous Conduction Mode

The discontinuous conduction mode arises when the switching ripple in an inductor current or capacitor voltage is large enough to cause the polarity of applied switch current or voltage to reverse. Let us consider how the inductor current waveforms change as the

load current is reduced. Let's use the buck regulator (Fig.2.15(a)) as a simple example.

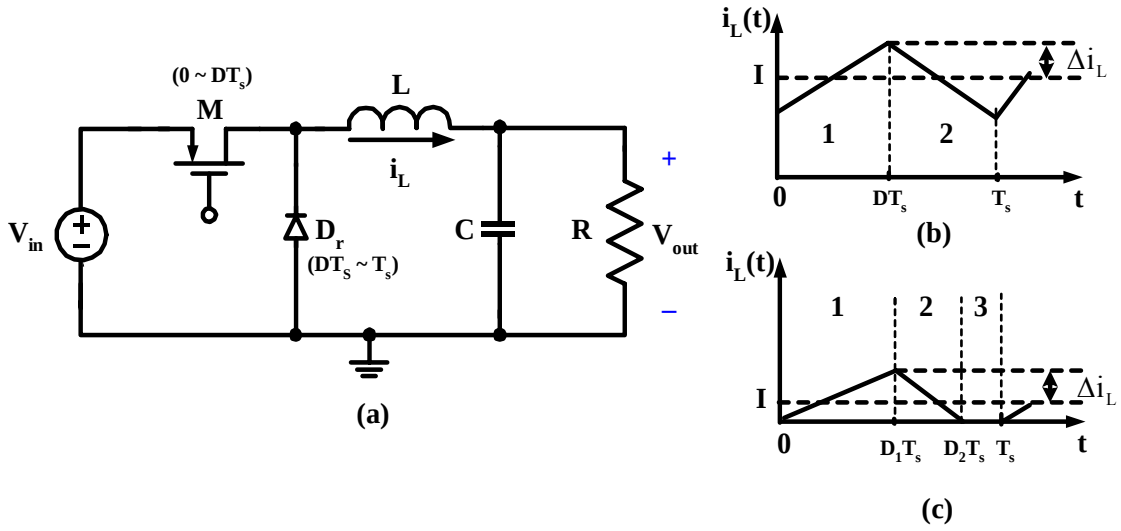


Fig.2.15 Buck regulator, (a) circuit (b) inductor current in CCM (c) inductor current in DCM

The inductor current $i_L(t)$ waveforms are sketch in Fig.2.15(b) for continuous conduction mode. As described in former sections, the inductor current waveform contains a dc component I, plus switching ripple of peak amplitude Δi_L. Approximately, the inductor current dc component I is equal to the load current: $I = \frac{V_{out}}{R}$. The switching ripple peak amplitude is: $\Delta i_L = \frac{(V_{in}-V_{out})}{2L} DT_s = \frac{V_{in} DD' T_s}{2L}$. Suppose now that the load resistance R is increased, so that the dc load current is decreased. The dc component of inductor current I will then decrease, but the ripple magnitude Δi_L will remain unchanged. If we continue to increase R, eventually the point is reached $I < \Delta i_L$, illustrated in Fig.2.15(c). In Fig 2.15(c), there are three subintervals during each switching period T_s. During the first subinterval the transistor conducts, and the diode conducts during the second subinterval. At the end of the second subinterval the diode current reaches to zero, and during the remainder of switching period neither the transistor nor the diode conduct. The regulator operates in the discontinuous conduction mode.

From above argument, we know that I and Δi_L are key point to distinguish the conditions for operation in the continuous and discontinuous conduction mode. The conditions is :

$$\begin{aligned} I &> \Delta i_L \quad \text{for CCM} \\ I &< \Delta i_L \quad \text{for DCM} \end{aligned} \tag{2-17}$$

Insertion of $I = \frac{V_{out}}{R}$ and $\Delta i_L = \frac{V_{in} DD' T_s}{2L}$ into I > or < Δi_L yields the following condition for operation in the continuous or discontinuous conduction mode:

$$I > \Delta i_L \Rightarrow \frac{V_{out}}{R} > \frac{V_{in} DD' T_s}{2L} \Rightarrow \frac{2L}{RT_s} > D' \Rightarrow K > K_{crit}(D) \text{ for CCM} \tag{2-18}$$

$$I < \Delta i_L \Rightarrow \frac{V_{out}}{R} < \frac{V_{in} DD' T_s}{2L} \Rightarrow \frac{2L}{RT_s} < D' \Rightarrow K < K_{crit}(D) \text{ for DCM} \tag{2-19}$$

where $K=2L/RT_s$ and $K_{crit}(D)=D'$. The other expression in terms of the load Resistance R is follows:

$$I > \Delta i_L \Rightarrow \frac{V_{out}}{R} > \frac{V_{in} DD' T_s}{2L} \Rightarrow R < \frac{2L}{D'T_s} \Rightarrow R < R_{crit}(D) \text{ for CCM} \tag{2-20}$$

$$I < \Delta i_L \Rightarrow \frac{V_{out}}{R} < \frac{V_{in} DD' T_s}{2L} \Rightarrow R > \frac{2L}{D'T_s} \Rightarrow R > R_{crit}(D) \text{ for DCM} \tag{2-21}$$

where $R_{crit}(D)=2L/D'T_s$. A similar analysis can be performed for other converter. The results are listed in Table 2.2

Table 2.2 Boundary of CCM and DCM for the buck, boost, buck-boost regulators

Regulator	$K_{crit}(D)$	$R_{crit}(D)$
Buck	$(1 - D)$	$\frac{2L}{(1-D)T_s}$
Boost	$D(1 - D^2)$	$\frac{2L}{D(1-D)^2 T_s}$
Buck-boost	$(1 - D)^2$	$\frac{2L}{(1-D)^2 T_s}$

After the discussion about boundary of CCM and DCM, let us analyze the conversion ratio V_{out}/V_{in} of the buck regulator (Fig.2.15(a)) in DCM. The inductor voltage in different subinterval is shown as Fig.2.16 (a). During subinterval 1, the transistor conducts, and the inductor voltage $v_L(t)=V_{in}-V_{out}$. During subinterval 2, the diode conducts, and the inductor voltage $v_L(t)=- V_{out}$. During subinterval 3, both transistor and the diode is in the off state, and the inductor voltage $v_L(t)=0$. According to the principle of inductor volt second balance, the dc component in the inductor must be zero.

$$< v_L(t) > \;=\; D_1(V_{in}-V_{out}) + D_2(-V_{out}) + D_3(0) = 0 \tag{2-22}$$

Solution for conversion ratio yields

$$\text{Conversion ratio} = \frac{V_{out}}{V_{in}} = \frac{D_1}{D_1+D_2} \tag{2-23}$$

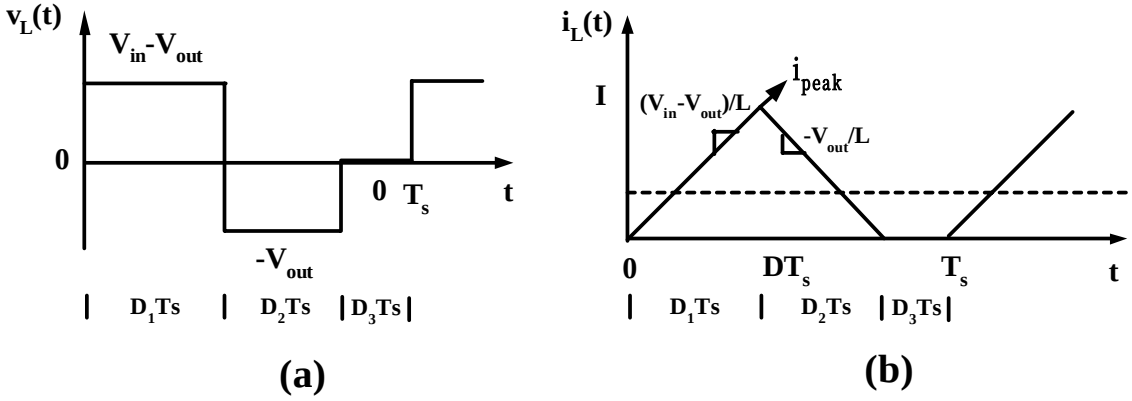


Fig.2.16 Buck regulator in DCM , (a) inductor voltage (b) inductor current

From Fig.2.16 (b), the average inductor current is calculated:

$$\frac{1}{T_s}\int_0^{T_s} i_L(t)dt = \frac{1}{T_s}[\frac{1}{2} i_{Peak}(D_1+D_2)T_s]$$
$$\text{Average inductor current} = \frac{V_{out}}{R} = (V_{in}-V_{out})(\frac{D_1 T_s}{2L})(D_1+D_2) \tag{2-24}$$

Elimination of D_2 from conversion ratio equation and average inductor current equation, and solution for the conversion ratio V_{out}/V_{in}, yields

$$\frac{V_{out}}{V_{in}} = \frac{2}{1+\sqrt{1+\frac{4K}{D_1^2}}} \quad \text{,where } K=2L/RT_s \tag{2-25}$$

A similar analysis can be performed for other converter. The results of conversion ratio M(D) are listed in Table 2.3

Table 2.3 Conversion ratio of CCM and DCM for the buck, boost, buck-boost regulators

Regulator	DCM M(D)	CCM M(D)
Buck	$\frac{2}{1+\sqrt{1+4K/D^2}}$	D
Boost	$\frac{1+\sqrt{1+4D^2/K}}{2}$	1/(1-D)
Buck-boost	$\frac{-D}{\sqrt{K}}$	-D/(1-D)

Where K is equal to $2L/RT_s$, and D is the time in which the transistor conducts.

2.3 Control Scheme: Current Mode vs. Voltage Mode [8] [9]

In all switching regulators, the output voltage $V_{out}(t)$ is a function of input voltage $V_{in}(t)$, the duty cycle d(t), and the load current $I_{Load}(t)$, as well as the regulator circuit element values. In a DC/DC regulator application, it is desired to obtain constant output voltage $V_{out}(t)=V$, in spite of distribution in $V_{in}(t)$, $I_{Load}(t)$, and other element values of the regulator circuit. So we can not except to simply set duty cycle to a single value, and obtain a desired constant output voltage under all conditions. The idea behind the use of negative feedback is to build a circuit that automatically adjusts the duty cycle as necessary, to obtain the desired output voltage with high accuracy, regardless of distribution in $V_{in}(t)$ or $I_{Load}(t)$ or variations of component. This is a useful method to do whenever there are variations and unknowns that otherwise prevent the system from attaining the desired performance.

The feedback circuit for switching regulator is commonly split up into two methods: voltage mode control and current mode control.

Voltage mode control :

In voltage mode control, the output voltage V_{out} is controlled by comparing the output voltage V_{out} with a reference voltage V_{ref}, and the resulting error voltage is compared to a saw-tooth ramp to control the duty cycle of the power transistor switch. A simple buck regulator with voltage mode control is shown in Fig.2.17 (a).

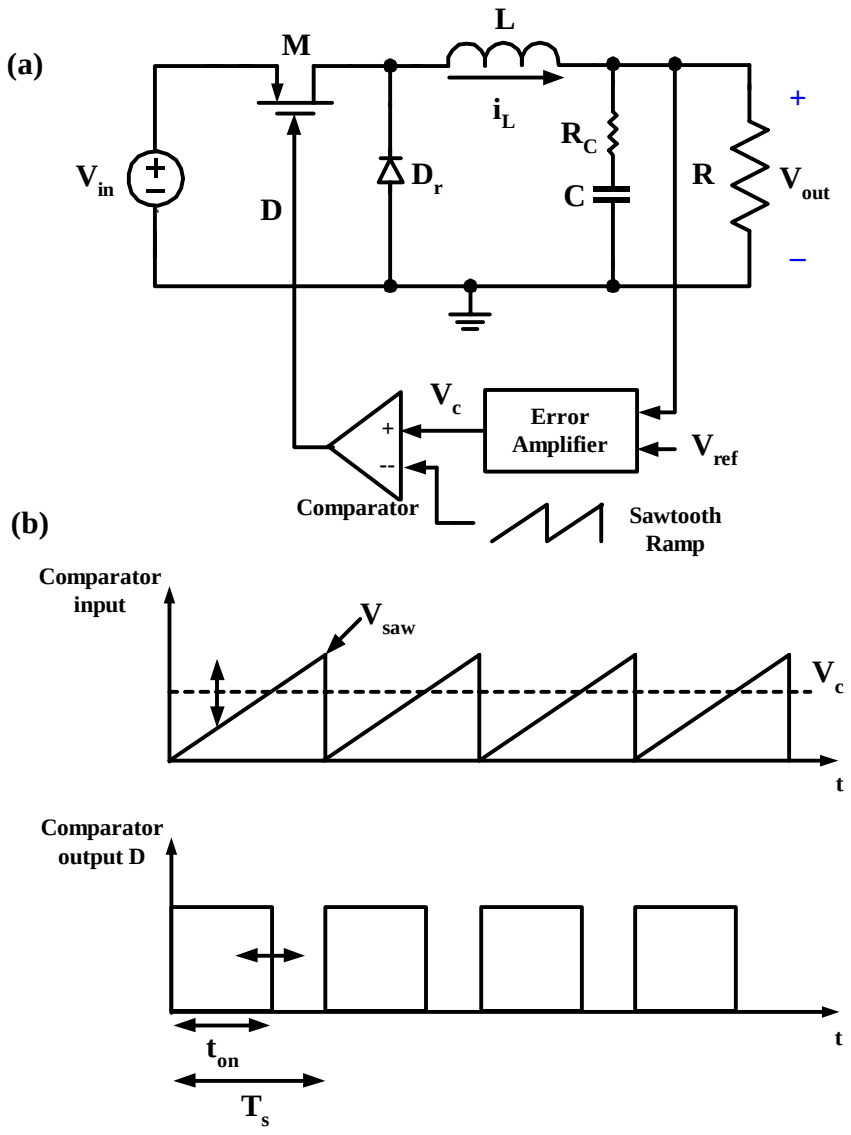


Fig.2.17 Buck regulator, (a) with voltage mode control (b) control circuit waveform

From Fig.2.17 (b), D is obtained by comparing the control signal V_c with a fixed frequency saw-tooth voltage. Thus:

$$D=\frac{t_{on}}{T_s}=\frac{V_c}{V_{saw}} \tag{2-26}$$

In the views of frequency domain, the control to output transfer function for buck regulator looks like a typical filter characteristics:

$$\frac{V_{out}}{V_c}=K_V\frac{1+sCR_c}{1+\frac{s}{\omega_0 Q}+\frac{s}{\omega_0^2}} \qquad \text{where } \omega_0=\frac{1}{\sqrt{LC}} \tag{2-27}$$

Current mode control:

A buck regulator with current mode control is shown in Fig.2.18 (a). Instead of comparing the control voltage V_c to a saw-tooth ramp with fixed amplitude and frequency. The control signal V_c is compared to a voltage derived from the inductor, forming an inner loop.

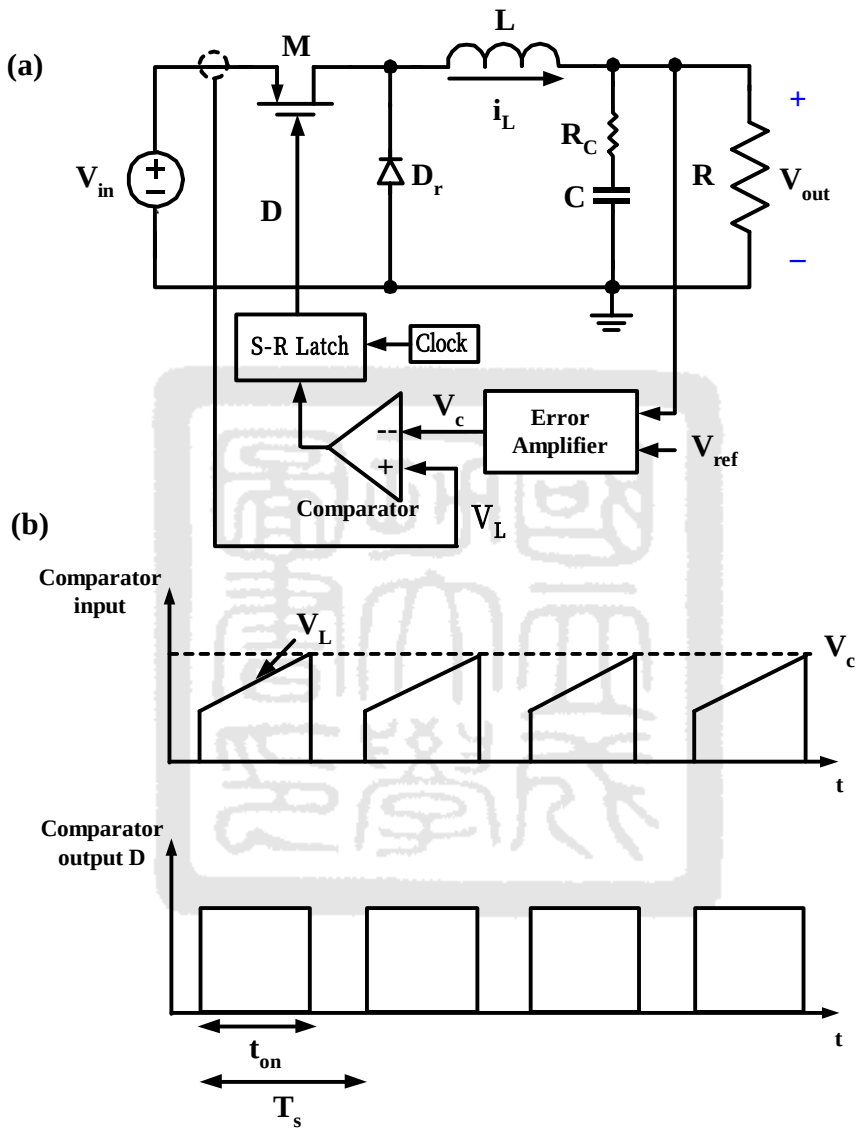


Fig.2.18 Buck regulator, (a) with current mode control (b) control circuit waveform

In the buck regulator shown in Fig 2.18(a) (b), initially, the clock sends a pulse to S-R latch which sets D to logic "High", thus the transistor switch conducts. Signal V_L will build up in a linear fashion.

$$\text{slope of } V_L = \frac{V_{in} - V_{out}}{L} \tag{2-28}$$

When V_L reaches the control voltage V_c, the comparator output changes to logic “High”, resetting the S-R latch output to logic “Low”, hence the transistor switch is in off state. Those actions are periodically carried out to regulate output voltage. In the views of frequency domain, the control to output transfer function for buck regulator with current mode control looks like the single pole system in low frequency:

$$\frac{V_{out}}{V_c}=K_i\frac{1+sCR_c}{1+sCR}F_h(s) \qquad (2\text{-}29)$$

where $F_h(s)$ is a second-order pairs of poles at half the switching frequency.

The comparison of voltage mode control and current mode control are summarized in the below.

1. Compensation : (current mode control is better than voltage mode control)

Voltage mode control:

Voltage mode control looks like a typical two pole filter. The sharp phase drop happens after resonant frequency, so the system requires a type three compensator to make itself stable.

Current mode control:

Current mode control looks like a single pole system at low frequency, since the inductor has been controlled by inner loop. This improves the phase margin, and a type two compensator is adequate to make the system stable.

Fig .2.19 shows a simple example of the power stage gain and phase of the buck regulator with voltage mode control and current mode control. From this figure, we can know that how much easier the current mode control is to compensate.

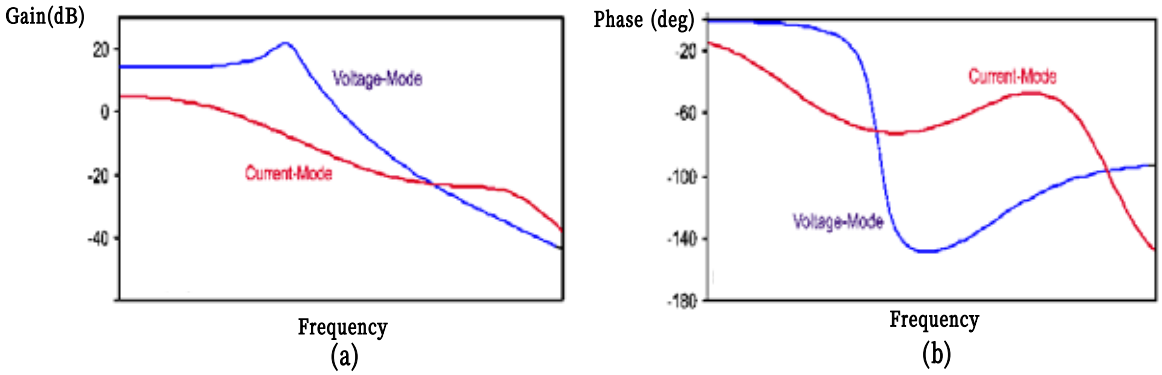


Fig.2.19 Voltage mode control and current mode control (a) gain (b) phase

2. Design of right-half plane zero converters: (Current mode control is better than voltage mode control)

Voltage mode control:

With voltage mode control, crossover has to be well above the resonant frequency, or the filter ring. In a converter where the crossover frequency is restricted by presence of a right-half plane zero, this is impossible.

Current mode control:

With current mode control, it is not a problem to have a control loop crossover at or below the output filter resonant frequency. So it is possible to configure crossover below the presence of right-half plane zero, this will make the effect of right-half plane zero decrease.

3. CCM and DCM operation: (current mode control is better than voltage mode control)

Voltage mode control:

When the operation moves from continuous-conduction mode (CCM) to discontinuous conduction mode (DCM), the gain and phase of switching regulator (the buck regulator is brought up as a simple example) with voltage mode control are drastically different as shown in Fig. 2.20 (a) and (b). It is difficult to design a compensator with voltage mode control that can provide good performance in both CCM and DCM.

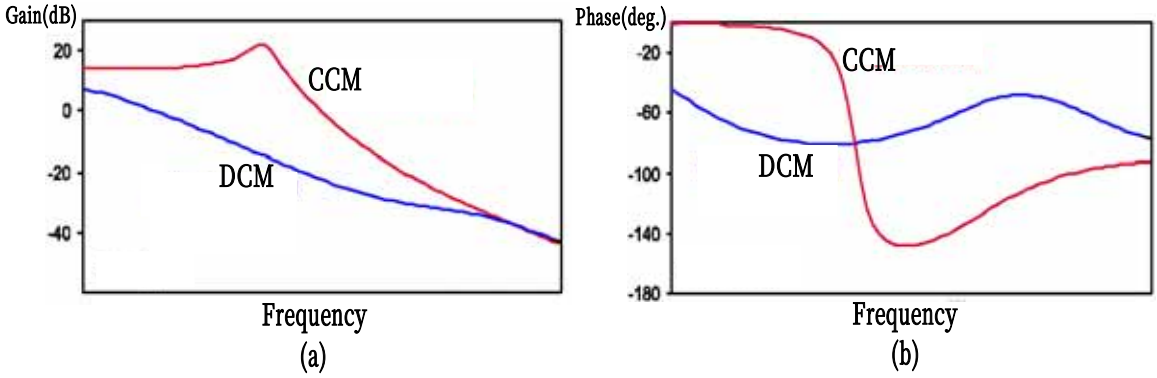


Fig.2.20 Voltage mode control with CCM and DCM (a) gain (b) phase

Current mode control:

With current mode control, the gain and phase of switching regulator (the buck regulator is brought up as a simple example) are almost constant in CCM and DCM as shown in Fig. 2.21 (a) and (b). This makes us easily design a compensator with current mode control that can provide optimal response in both modes.

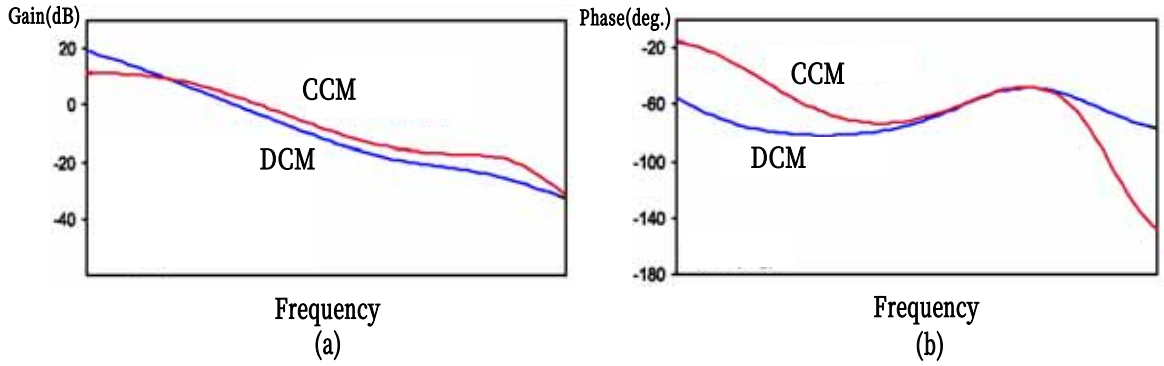


Fig.2.21 Current mode control with CCM and DCM (a) gain (b) phase

4. Line Rejection: (current mode control is better than voltage mode control)

Voltage mode control:

The switching regulator with voltage mode has a poor closed loop transient response to changes in input voltage, as a change in input voltage will result in a compensating change in duty cycle delayed by the output filter. The influence of changes in input voltage with voltage mode control is mainly limited by the gain of feedback loop and delay time of output filter.

Current mode control:

With current mode control, even if there is only a moderate gain in the voltage feedback loop, the attenuation of input ripple is usually adequate because of current loop. It is even possible to null the influence of changes in input voltage for the buck regulator. In order to achieve same performance of line rejection, the switching regulator with voltage mode control needs far more gain in the main feedback loop than with current mode control.

5. Current Sensing: (voltage mode control is better than current mode control)

Voltage mode control:

In theory, the switching regulator with voltage mode control does not need the current sensing circuit because entire operation is carried out without using either the switch current or inductor current. But in practice, the current sensing circuit is usually needed to avoid over current condition. However, the current sensing circuit is not requested high accuracy, so the design about this circuit is simple.

Current mode control:

The operation with current mode control needs either accurate switch current or accuracy inductor current, so the current sensing circuit must be very wideband to

accurately reconstruct the current signal. In general, the current sensing circuit needs a bandwidth several orders of magnitude above the switching frequency to work appropriately. This shows that the current sensing circuit with current mode control is more difficult to design than with voltage mode control.

6. Stability: (voltage mode control is better than current mode control)

Voltage mode control:

In an aspect of stability, switching regulator with voltage mode control requires an appropriate three type compensator to make whole voltage loop reach enough gain and phase conformed to desirable specification.

Current mode control:

With current mode control, we only need a simple type two compensator to stabilize its voltage loop, but in addition to stability of voltage loop we must pay attention to stability of current loop.

Sub-harmonic oscillation is a well-known problem of stability in current loop for switching current mode regulator with the duty cycle D larger than 50% as shown in Fig 2.22 (a), (b)

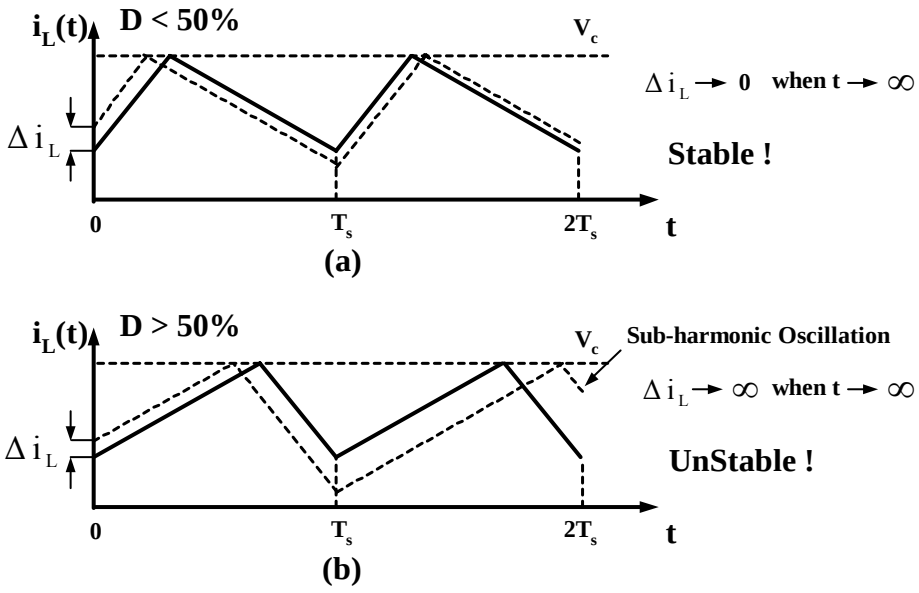


Fig.2.22 Current mode control (a) D < 50% (b) D > 50% without the compensation ramp

In order to avoid sub-harmonic oscillation, we must choose a compensation ramp to add with inductor current signal. The slope of compensation ramp m_a must be large than half of the slope of inductor current m_2 during the second subinterval $D'T_s$ as shown in Fig.2.23.

By choosing an appropriate compensation ramp, the influence on stability of the sub-harmonic oscillation is reduced or avoided.

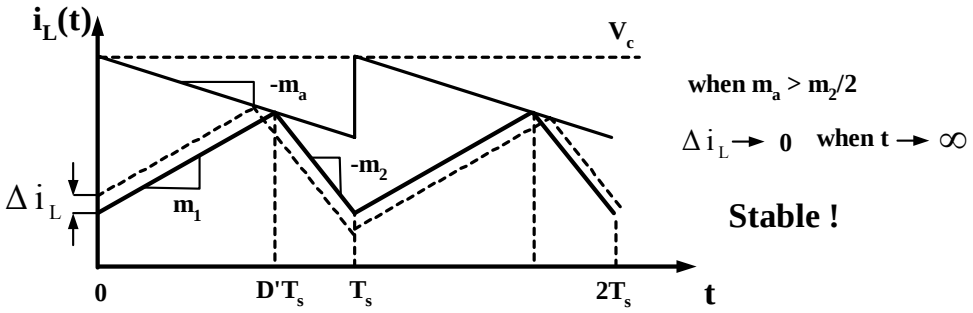


Fig.2.23 Current mode control with compensation ramp

7. Signal-to-Noise ratio : (voltage mode control is better than current mode control)

Voltage mode control:

With voltage mode control, the signal for control is decided by V_c/V_{saw} as shown in Fig. 2.17(b). We can reduce influence of noise by increase amplitude of V_{saw}.

Current mode control:

The noise on current sense signal is the biggest problem in almost every current-mode regulator. In many regulators, there is simply not enough signal to control the whole system smoothly over full range of operation. In the view of ideal current waveform as shown in fig. 2.24(a), we know that the signal available for control is very small versus whole current signal. In reality as shown in fig. 2.24(b), the current waveform with spikes and ringing will make control of system more difficult.

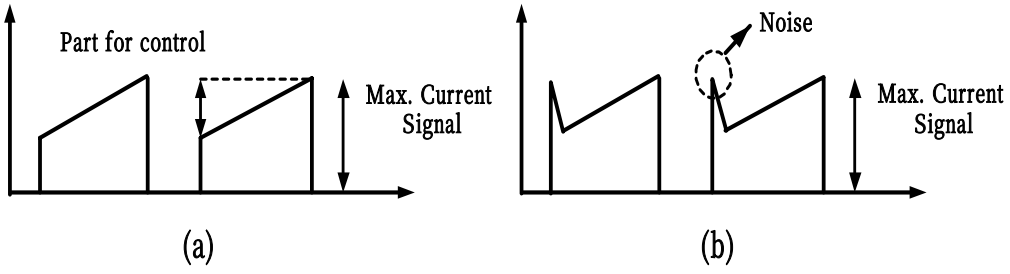


Fig.2.24 Current signal (a) ideal waveform (b) real waveform

Chapter 3

Issue of Current Mode Buck Regulator

3.1 Current Mode Buck Regulator [10] [11] [20]

3.1.1 Structure

Fig. 3.1 illustrates a general structure of a current mode buck regulator.

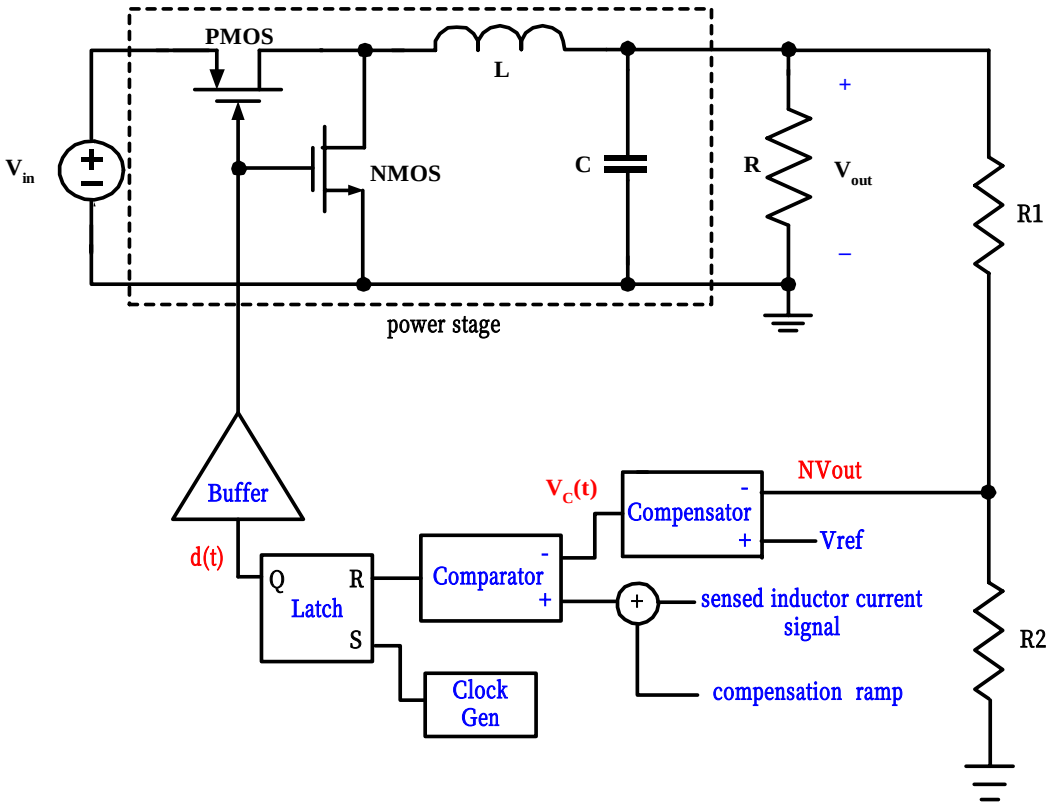


Fig. 3.1 Structure of current mode buck regulator

The regulator is composed of power stage and a feedback network. The power stage is the

topology of buck regulator whose characteristic is introduced in chapter 2. It contains a pair of switching elements, which consists of the power PMOS and NMOS transistors, and an output filter, which consists of an inductor L and a capacitor C. In feedback network, the difference of NV_{out} which the output voltage is scaled down by resistor series to and the reference voltage V_{ref} is fed to the compensator. And then the output of the compensator and the addition of the sensed inductor current signal and the compensation ramp will pass through the comparator and the digital control block to define the duty cycle d(t). The duty cycle d(t) controls the duration of the conducted time between the PMOS and the NMOS to achieve desired voltage such that the feedback is finished to regulate the output voltage V_{out}.

With current mode control, the biggest difference from voltage mode control is to build inner current loop by using information of inductor current. The building of inner current loop makes not only transient response of line-to-output faster but also compensation of outer voltage loop easier in system. But it has an inherent instability called “sub-harmonic oscillation” introduced in chapter 2. In order to avoid this instability, the general way is to sum inductor current signal with a compensation ramp as shown in Fig. 3.1. Thus with current mode control, in addition to stability of outer voltage loop, we must choose appropriate compensation ramp for stability of inner current loop.

3.1.2 Small-Signal Model

The PWM switch has been provided a flexible small signal model which replaces the nonlinear switching action of the regulator with a simple equivalent circuit as shown in Fig.3.2. This model can be used invariably in different topology of regulators.

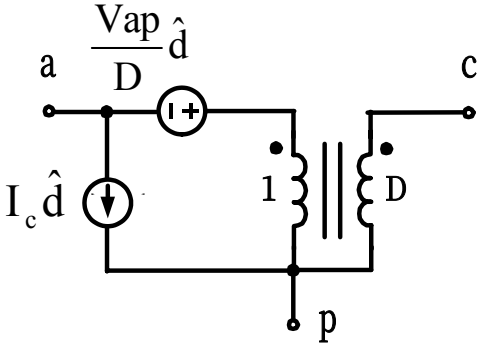


Fig. 3.2 PWM three-terminal small signal switch model

To quote Fig.3.2, the small signal model of the buck regulator is shown as Fig.3.3

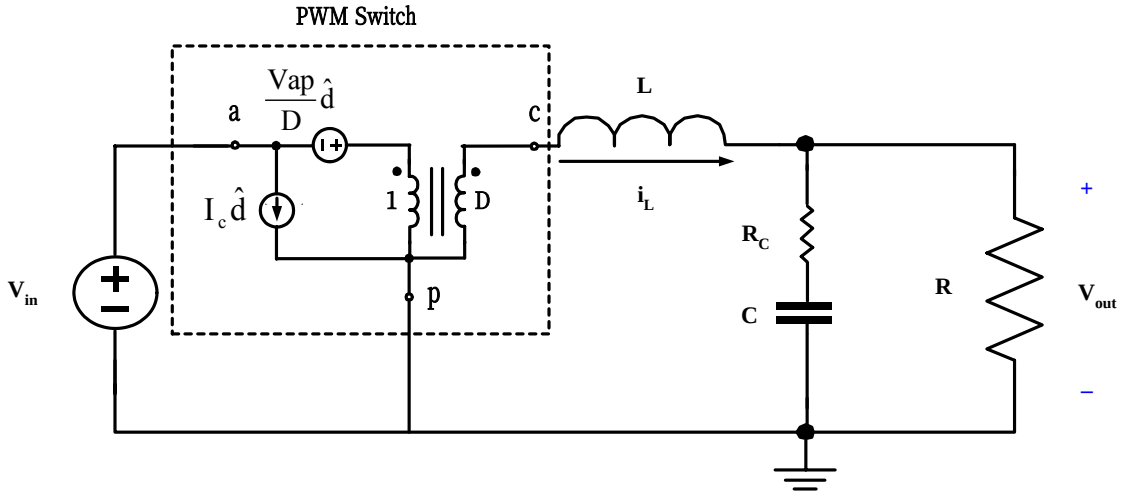


Fig. 3.3 Small signal model of the buck regulator

After discussion of power stage, Fig.3.4 shows a simple current mode control modulation scheme. A constant frequency clock initiates the on-time and the sensed inductor current signal interests a control signal V_c to decide when is off-time. The duration of on-time and off-time is the duty cycle to control operation of the system. A compensation ramp is added to sensed inductor current signal to provide design flexibility and stabilize the current loop.

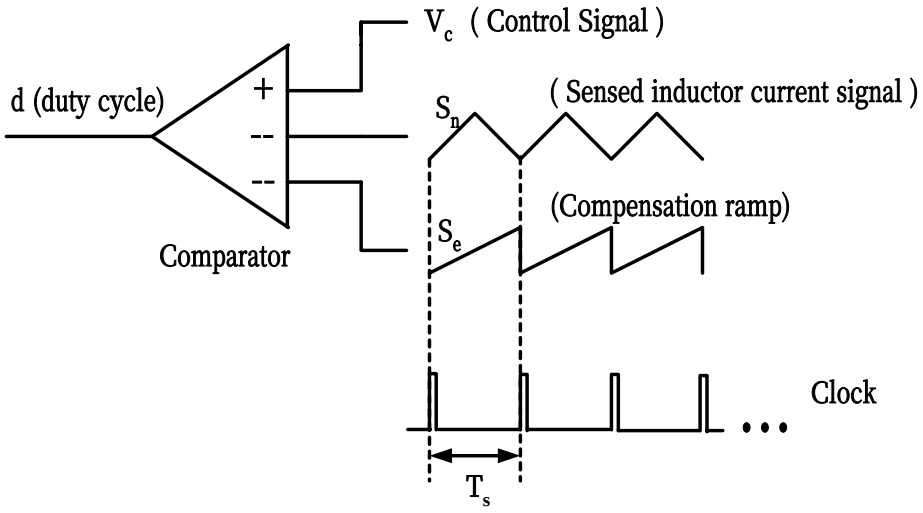


Fig. 3.4 Current mode control modulator

The modulator gain of the circuit is:

$$F_m = \frac{1}{(S_n + S_e)T_s} \qquad (3\text{-}1)$$

Where S_n is the on-time slope of sensed inductor current signal and S_e is the slope of compensation ramp.

From viewpoint of Fig.3.4, we can construct the small signal model of current feedback loop and combine Fig.3.3 to realize a complete block diagram as shown in Fig.3.5 for PWM circuits with current mode control.

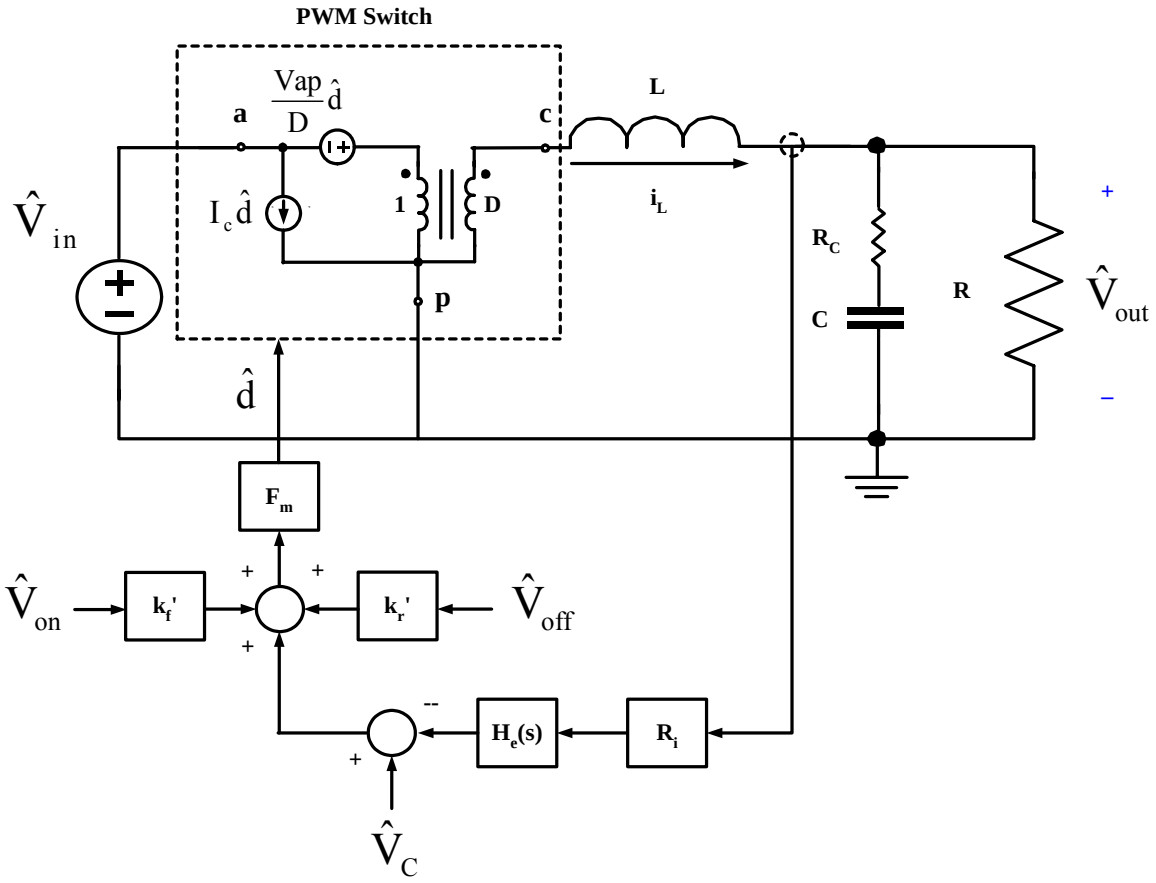


Fig. 3.5 Complete small-signal model for buck regulator with current mode control

Gain R_i and $H_e(s)$ represent the current feedback. R_i is the linear gain of current-sensing circuit, and $H_e(s)$ is the model of sampling action in current mode control. By viewpoint of sample-and-hold systems, $H_e(s)$ is calculated:

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1} \tag{3-2}$$

However, this expression has an infinite number of poles and zeros. In fact, there is no need to model the transfer function beyond half the switching frequency. We will use a simple second-order transfer function to approximate the exact function:

$$H_e(s) \approx 1+\frac{s}{\omega_n Q_z}+\frac{s^2}{\omega_n^2} \quad , \text{ where } Q_z=-\frac{2}{\pi} \text{ and } \omega_n=\frac{\pi}{T_s} \tag{3-3}$$

Gain k_f' and k_r' provide feedforward of voltage across the inductor during the on-time and off-time of the regulator, respectively. These gain paths are created by feedback of the inductor current, the slope of which depends on the voltages applied to the inductor. As For F_m, it's the gain of control modulator as shown in Eq.(3-1). The compensation ramp added to the circuit mainly affect this term, F_m. In conclusion, the model as shown in Fig.3.5 can provide a complete model which accurately predicts characteristics from dc to half switching frequency, including low-frequency effects, and high-frequency phenomenon of sub-harmonic oscillation. This will make entire design more effective and conform to reality.

3.1.3 Transfer Function

By Fig.3.5, we can obtain some information of frequency response such as current loop gain, control to output gain, audio susceptibility, and output impedance and so on. Here we will give an example of buck regulator with following parameters to show those characteristics of frequency response.

Table 3.1 Buck regulator parameters (1)

V_{in}	V_{out}	L	C	R	R_c	R_i	T_s
11V	5V	37.5uH	400uF	1Ω	14mΩ	0.33	20us

1. Current Loop Gain $T_i(s)$:

It can be shown that gain blocks k_f' and k_r' have little effect on the current-loop gain. Ignoring these gains, the approximate current-loop gain of the buck converter is:

$$T_i(s) \approx \frac{L}{RT_s m_c D'} \frac{1+sCR}{1+\frac{s}{\omega_0 Q_{ps}}+(\frac{s}{\omega_0})^2} H_e(s)$$

$$\text{where } Q_{ps}=\frac{1}{\omega_0[\frac{L}{R}+CR_c]}, \omega_0=\frac{1}{\sqrt{LC}} \text{ and } H_e(s) \text{ is equal to Eq.(3 - 3)} \tag{3-4}$$

The gain and phase of current loop gain with different values of compensation ramp is

shown in Fig.3.6. In Fig.3.6, it shows the two RHP zeros are apparent at half the switching frequency which let the gain increase after this frequency, while the phase drop down an additional ninety degrees. If insufficient compensation ramp is added, there is very little phase margin in this loop gain.

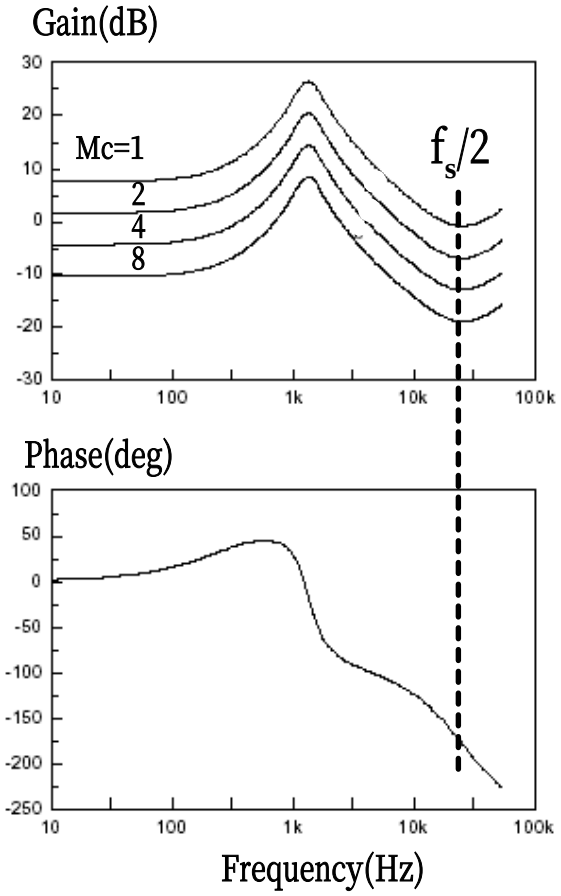


Fig. 3.6 Gain and phase of current loop gain

Where S_n is the on-time slope of sensed inductor current signal and S_e is the slope of compensation ramp.

2. Control-to-Output :

The approximate control-to-output transfer function of the buck regulator with current mode control is given by

$$\frac{\hat{v}_o}{\hat{v}c} \approx \frac{R}{Ri} \frac{1}{1+\frac{RT_s}{L}[m_c D'-0.5]} \frac{1+sCR_c}{1+\frac{s}{\omega_p}} \frac{1}{1+\frac{s}{\omega_n Q_p}+(\frac{s}{\omega_n})^2}$$

$$\text{where } \omega_p = \frac{1}{CR} + \frac{T_s}{LC}(m_c D'-0.5), \text{ and } Q_p = \frac{1}{\pi(m_c D'-0.5)} \qquad (3\text{-}5)$$

Fig.3.7 shows a plot of control to output of buck regulator with different values of

compensation ramp. In this figure, we know that as more compensation ramp, S_e, is added, the effect of the high-Q double pole is damped but that characteristic of buck regulator from current mode control to voltage mode control.

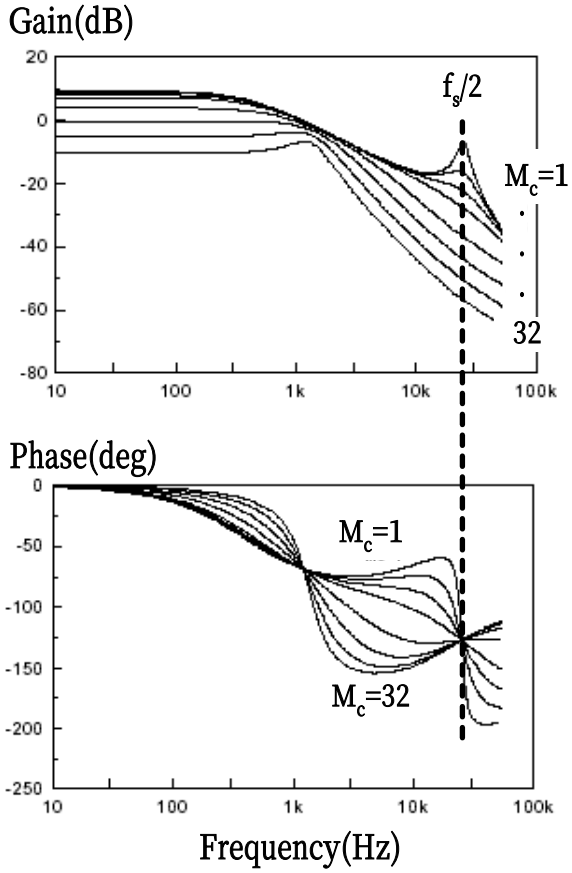


Fig. 3.7 Gain and phase of control to output

3. Audio Susceptibility :

The audio susceptibility of the buck regulators shows one of the most interesting properties of current mode control. Since the gain term, k_f', has a negative value, it is possible to completely null the circuit response to input-voltage perturbations with a compensation ramp value $S_e=S_f/2$, where S_f is the off-time slope of sensed inductor current signal. The approximate audio transfer function for the buck regulator is

$$\frac{\hat{v}_o}{\hat{v}_{in}} \approx D \frac{[m_c D'-(1-D/2)]}{\frac{L}{RT_s}+[m_c D'-0.5]} \frac{1+sCR_c}{1+\frac{s}{\omega_p}} \frac{1}{1+\frac{s}{\omega_n Q_p}+(\frac{s}{\omega_n})^2}$$

$$\text{where } \omega_p = \frac{1}{CR}+\frac{T_s}{LC}(m_c D'-0.5), \text{ and } Q_p = \frac{1}{\pi(m_c D'-0.5)} \qquad (3\text{-}6)$$

Fig.3.8 shows a plot of audio susceptibility of buck regulator with different values of

compensation ramp. The audio susceptibility of buck regulator is a special case where the input voltage perturbation can actually be nulled by the addition of the compensation ramp. The audio susceptibility is a very sensitive function of compensation ramp around the null value.

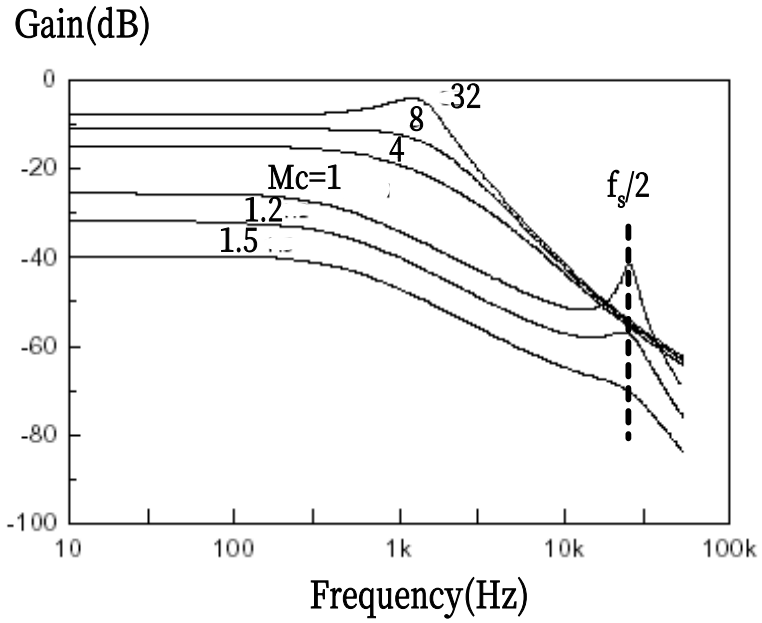


Fig. 3.8 Audio susceptibility

4. Output Impedance :

The approximate output impedance transfer function of the buck regulator with current mode control is given by

$$Z(s) \approx \frac{R}{1+\frac{RT_s}{L}[m_c D'-0.5]} \frac{1+sCR_c}{1+\frac{s}{\omega_p}}$$

$$\text{where } \omega_p = \frac{1}{CR} + \frac{T_s}{LC}(m_c D'-0.5) \qquad (3\text{-}7)$$

Fig.3.9 shows the output impedance of the buck regulator with different compensation ramp. Closing the current feedback loop makes the output impedance of the buck regulator look like the impedance of just the load capacitor and resistor. The significant differences from output impedance of the open loop regulator are high dc value and absence of the resonant peak.

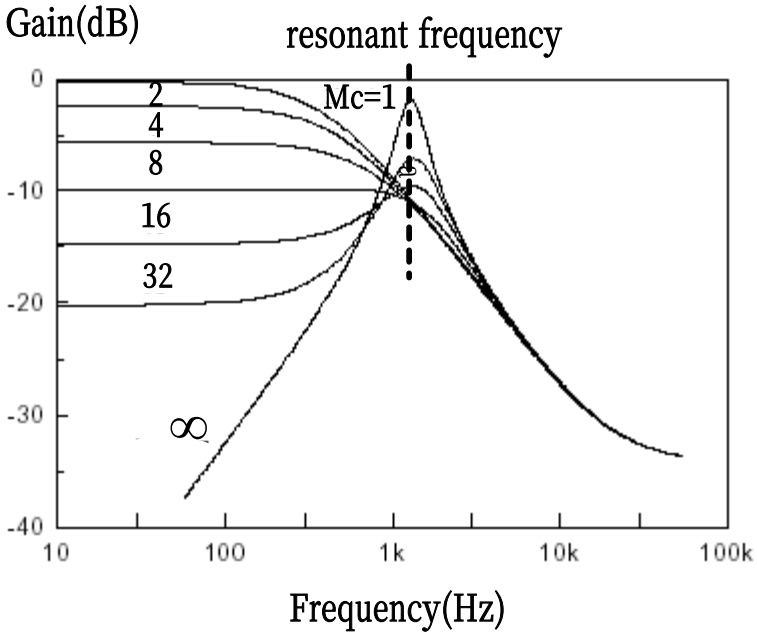
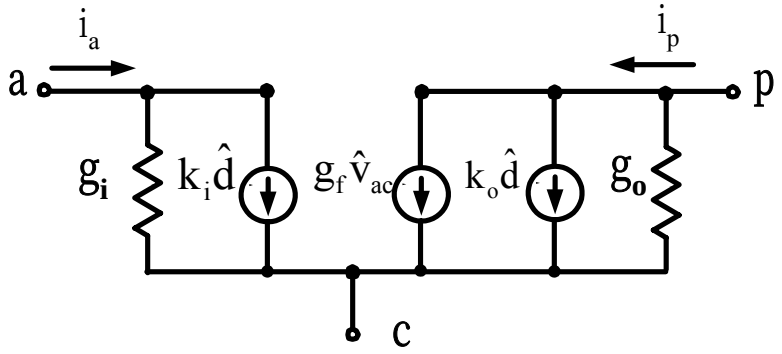


Fig. 3.9 Output impedance

The above discussion is suitable for use in continuous-conduction mode. As for discontinuous-conduction mode, the method is approximately the same except the model of the switch elements. The model of the switch elements is shown in Fig.3.10.



$g_i=I_a/V_{ac}$ $k_i=2I_a/D$ $g_f=I_p/D$ $k_o=2I_p/D$ $g_o=I_p/V_{cp}$

Fig. 3.10 PWM switch model for discontinuous conduction mode

We can obtain small signal model and transfer function of the discontinuous conduction mode by quoting this switch model in Fig. 3.10 as above method. The detailed description in this thesis is omitted but can be obtained in [11].

3.2 Proposed Improvement

Regulator with current mode control is subject to sub-harmonic oscillation if two conditions are met: the converter operates in continuous conduction mode (CCM) and duty cycle is close to or above 50%. When these two conditions occur, the regulator produces an oscillation at half the switching frequency. Fig.2.22 shows an extended perturbation can propagate through the cycles. In order to avoid sub-harmonic oscillation, the appropriate compensation ramp is added. The perturbation propagation with compensation ramp can be described via a simple formula

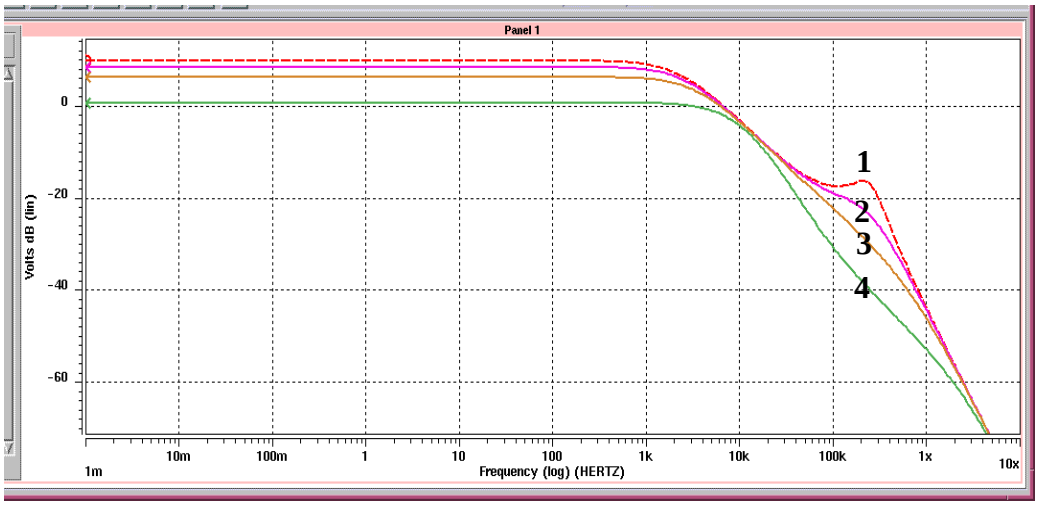
$$\hat{i}_L(nT_s) = \hat{i}_L(0)(-\frac{m_2 - m_a}{m_1 + m_a})^n \qquad (3\text{-}8)$$

Where $\hat{i}_L(nT_s)$ is the perturbation of inductor current signal at time nT_s, $\hat{i}_L(0)$ is the perturbation of inductor current signal at initial time, m_1 is the on-time slope of inductor current signal, m_2 is the off-time slope of inductor current signal, and m_a is the compensation ramp slope of inductor current signal. From Eq.(3-8), we can reduce propagation of perturbation by making the term $(-\frac{m_2 - m_a}{m_1 + m_a}) < 1$. One common choice of compensation ramp slope mathematically is $m_a >= m_2/2$. How many values of m_a should we choose? An example of control-to-output to output about specification of my design listed in Table 3.2 is shown in Fig.3.11.

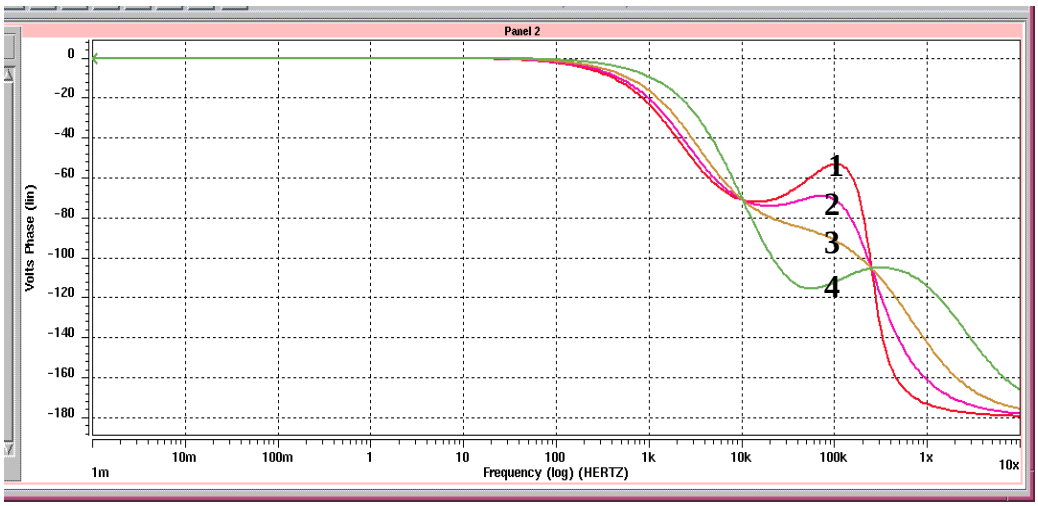
Table 3.2 Buck regulator parameters (2)

V_{in}	V_o	L	C	R	R_c	R_i	T_s
3.3V	1.8V	10uH	22uF	3.6Ω	100mΩ	1	2us

It shows that when more compensation ramp slope is added, the whole system is more stable, but gain and bandwidth is reduced and the transition from current mode control to voltage mode control to lose the original advantage of using current mode control.



(a) Gain



(b) Phase

The slope of the compensation ramp ➔

1. $1/2*m_2 = 0.09V/us$ **2.** $1*m_2 = 0.18V/us$ **3.** $2*m_2 = 0.36V/us$ **4.** $6*m_2 = 1.08V/us$

Fig. 3.11 Control-to-output (a) gain (b) phase

In conclusion, the more slope of the compensation ramp is not better. Appropriate slope of the compensation ramp will make performance of the system better than over large one.

In practice, the regulator usually has a range of output voltage level for convenience. Because the output voltage level is more than one value, it is not well considered to optimize the system in any output voltage level. The current mode switching regulator is an obvious example. In current mode switching regulator, the compensation ramp is usually chosen to conform to a demand for the stability of the most output voltage level because it is the least stable and needs the most slope of the ramp to compensate whole loop. Although by this compensation ramp the system can reach the requirements for stability in

every condition, the performance is reduced in lower output voltage level because of over large slope of the ramp. In order to alleviate this question, I will propose a new technique to achieve the effect of adjusted-slope compensation ramp which follows the output voltage level. Fig.3.12 shows a general addition of the sensed on-time inductor current signal and the compensation ramp.

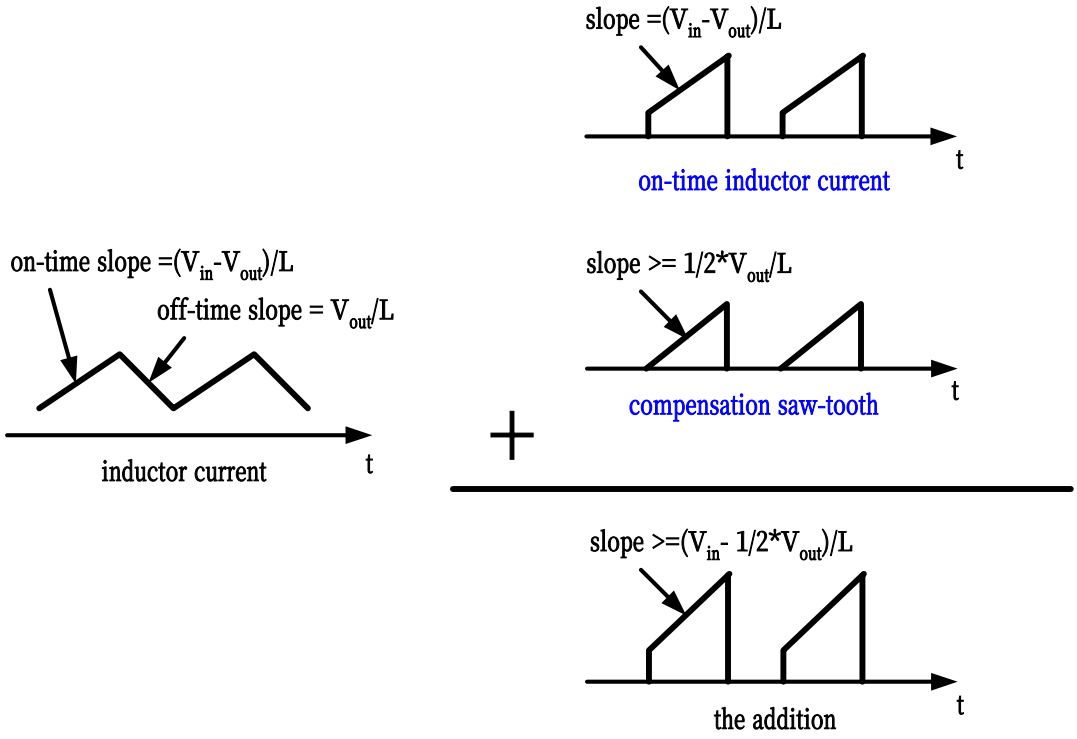


Fig. 3.12 Common case: compensation ramp slope m_a >= 1/2*V_{out}/L, the addition of the sensed on-time inductor current and compensation ramp

The slope of the compensation ramp which is larger than half off-time slope of inductor current is mathematically chosen to let the system stable. When we choose the slope of the compensation ramp to be equal to off-time slope of inductor current $m_a=V_{out}/L$, the slope of the addition wave as shown in Fig.3.13 is:

$$m_d = \frac{(Vin - Vout)}{L} + \frac{(Vout)}{L} = \frac{Vin}{L} \qquad (3\text{-}9)$$

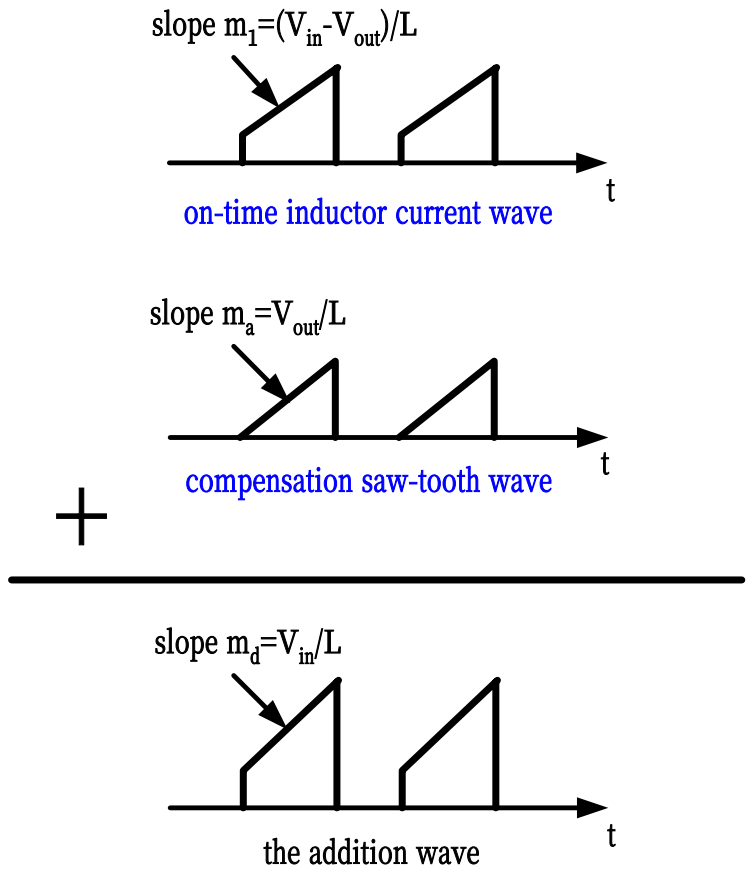


Fig. 3.13 Special case: the slope of the compensation ramp $m_a = V_{out}/L$, the addition of the sensed on-time inductor current and compensation ramp

Eq.(3-9) shows the slope of the addition wave has no relationship with output voltage level. By using this characteristic, we can reduce addition of sensed on-time inductor current and compensation ramp as tradition and directly produce this addition wave. In this way, not only we can ignore the usage of the addition circuit but also the slope of the compensation ramp V_{out}/L follows the output voltage V_{out} to adjust its value to achieve the adjusted-slope effect.

The circuit produces the wave with the slope V_{in}/L is shown in Fig3.14 (a). The operation of this circuit can be understood in Fig.3.14 (b). Firstly, conducting the switch 1 passes the initial sensed inductor current signal to capacitor C. Secondly, conducting the switch 2 produces a signal V_c with slope V_{in}/L in the capacitor C. Thirdly, conducting the switch 3 resets the capacitor voltage V_c when the signal V_c intersects the control signal. And then the system repeats these actions in the next period. As for how to obtain the desired slope value we can make I/C be equal to V_{in}/L by choosing suitable current source

I and capacitor C.

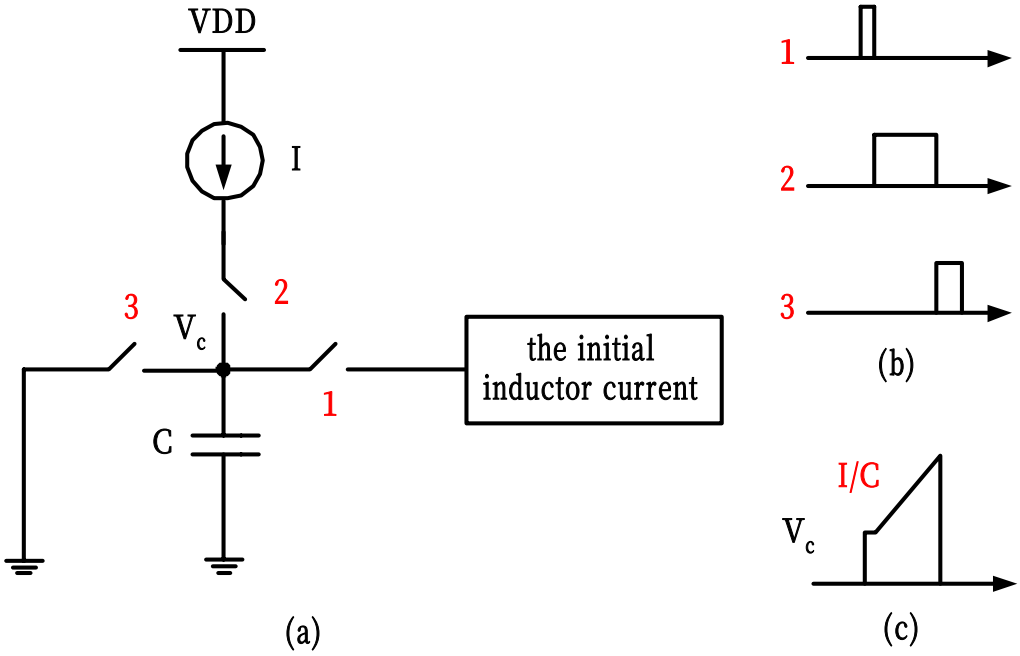


Fig. 3.14 (a) circuit (b) conducting time of the switch 1, 2, 3 (c) the voltage of the capacitor V_c

3.3 Stability in Whole System [3] [8]

When the feedback loop is closed, the gain and phase in itself are not enough to make whole system achieve desired performance and stability. The general method is to add a compensator in the loop to compensate insufficient gain and phase of whole system. Next, two types of compensator will be introduced. The first is type II shown in Fig.3.15 (a), and it has two poles and one zero. The transfer function is calculated as:

$$\frac{V_1}{V_2} = -\frac{1+sR_2C_1}{sR_1(C_1+C_2)(1+sR_2\frac{C_1C_2}{C_1+C_2})} \approx -\frac{1+sR_2C_1}{sR_1(C_1+C_2)(1+sR_2C_2)} \quad ,\text{assume } C_1 >> C_2 \tag{3-10}$$

The poles locate at the origin and the frequency $f_p = \frac{1}{2\pi R_2C_2}$', and the zero locates the frequency $f_z = \frac{1}{2\pi R_2C_1}$. The gain and phase of this compensator is shown in Fig. 3.15

(b), (c). This type compensator is mainly used in the regulator with current mode control, because this kind of the regulator looks like a single-pole at low frequency.

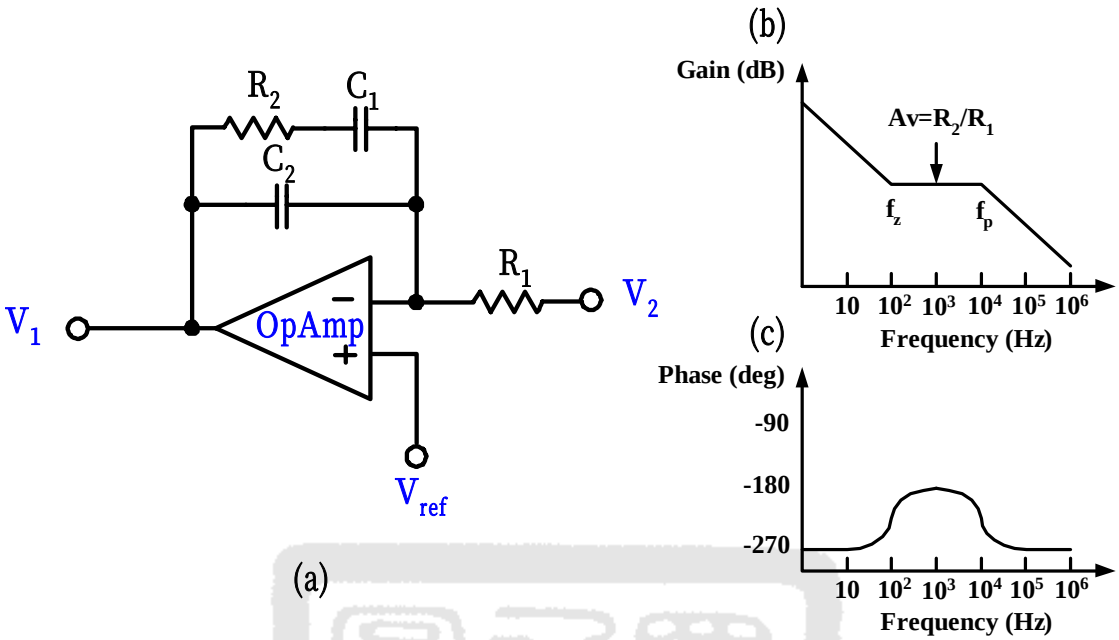


Fig. 3.15 Type II compensator (a) circuit (b) gain (c) phase

The second is type III, it is shown in Fig.3.16 (a), and it has three poles and two zeros. The transfer function is calculated as:

$$\frac{V_1}{V_2} = -\frac{(1+sR_2C_1)(1+s(R_1+R_3)C_3)}{sR_1(C_1+C_2)(1+sR_3C_3)(1+sR_2\frac{C_1C_2}{C_1+C_2})} \quad (3\text{-}11)$$

$$\approx -\frac{(1+sR_2C_1)(1+sR_1C_3)}{sR_1(C_1+C_2)(1+sR_3C_3)(1+sR_2C_2)} \text{ , assume } C_1 >> C_2 \text{ , and } R_1 >> R_3$$

The poles locate at the origin, the frequency $f_{p1} \approx \frac{1}{2\pi R_2C_2}$ and the frequency $f_{p2} \approx \frac{1}{2\pi R_3C_3}$. The zeros locate at the frequency $f_{z1} \approx \frac{1}{2\pi R_2C_1}$ and the frequency $f_{z2} \approx \frac{1}{2\pi R_1C_3}$. The gain and phase of this compensator is shown in Fig. 3.16 (b), (c). This type compensator is mainly used in the regulator with voltage mode control, because this kind of the regulator which has two poles at low frequency needs two zeros to compensate the sharp phase drop to stabilize the system.

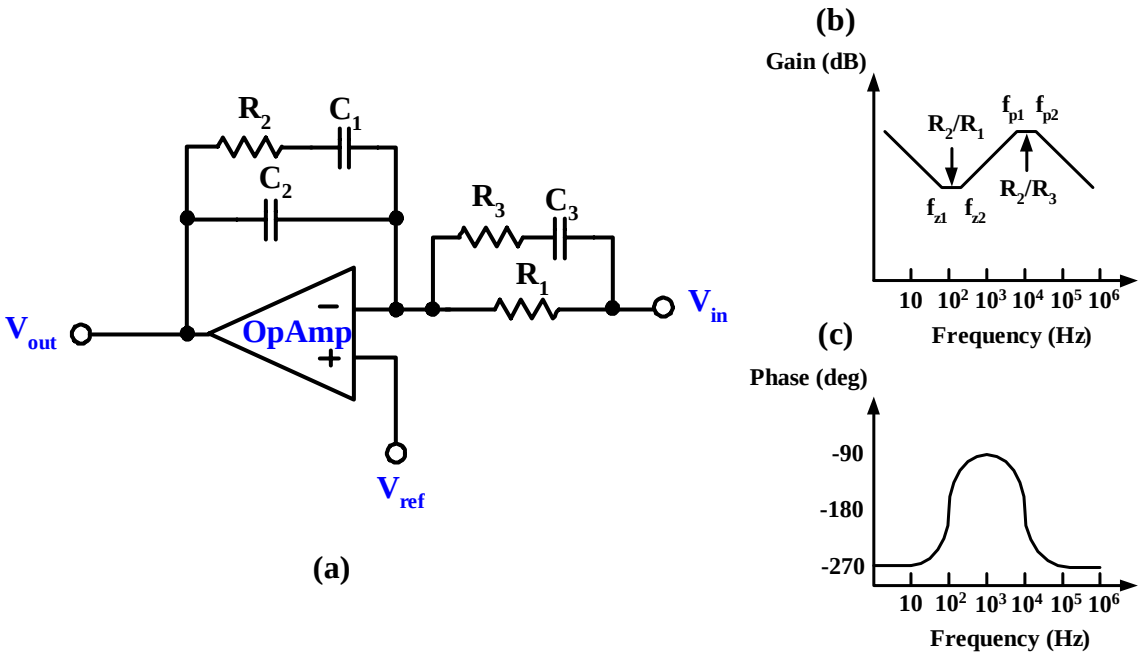


Fig. 3.16 Type III compensator (a) circuit (b) gain (c) phase

In summary, the maximum phase boost in type II compensator is 90 degrees, and in type III compensator is 180 degrees. According to stability and cost, the system will use the appropriate compensator to achieve desired performance.

My design belongs to the topology of current mode control, so I only need a simple type II compensator to stabilize the system. The parameters of the regulator are shown in Table 3.3.

Table 3.3 Current mode switching regulator

V_{in}	V_{out}	L	C	R_L	R_c	T_s	I_L
3.3V	0.5V~ 3V	10uH	22uF	100mΩ	100mΩ	2us	~550mA

The gain and phase of control-to-output is shown in Fig.3.17 while V_{out}=3V and I_L=550mA. Firstly, I suppose that R_1=150kΩ. Secondly, I set the loop gain crossover frequency 'f_{co}=1/5*f_s=100 kHz' and then obtain R_2 by this setting and R_1. Thirdly, I set zero locate at the desired settling time constant ($\approx$7kHz) and then obtain C_1 by this setting and R_2. Finally, I set second pole locate at frequency ($\approx \frac{1}{3} f_s \sim \frac{1}{2} f_s$) and then obtain C_2 by this setting and R_2. The value of R_2, C_1 and C_2 is modulated lightly and shown in Table 3.4.

Table 3.4 The parameter of type II compensator

R_1	R_2	C_1	C_2
150kΩ	1500 kΩ	15pF	500fF

Because the resistor of R_2 and the capacitors of C_1 and C_2 are integrated inside the chip in order to save the usage of the passive components outside the chip, the deviations of these components must be considered in stability. The deviation of +10% ~ -10% in capacitor and the deviation of +20% ~ -20% in resistor are assumed. A Monte Carlo simulation with 60 times by SPICE is implemented in my simulation. The simulation results is shown in Fig.3.17

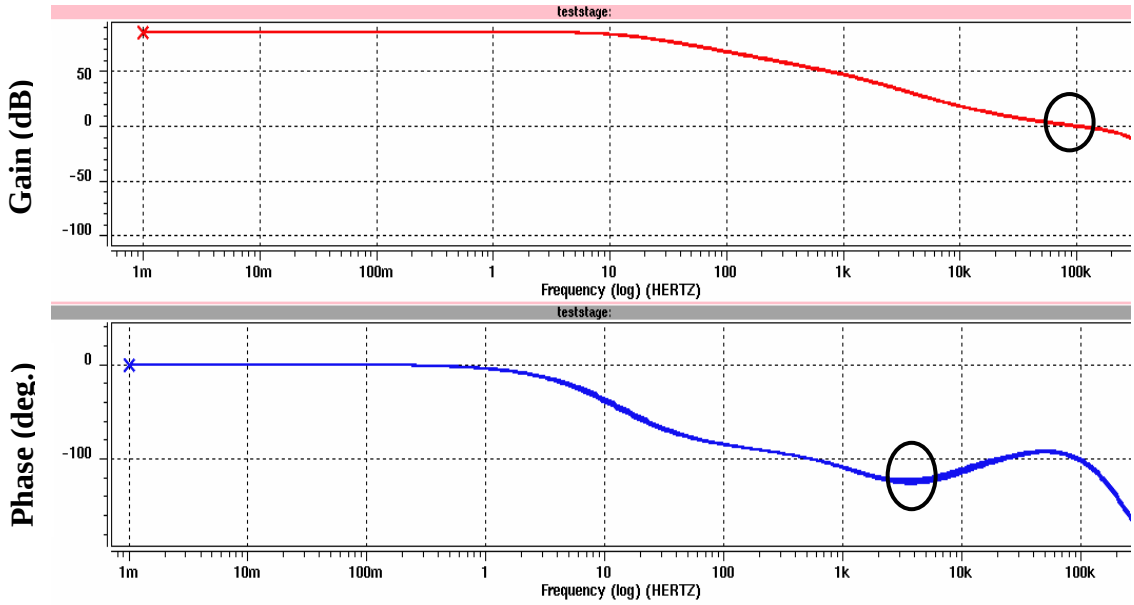


Fig. 3.17 Gain and Phase of whole system

The DC gain is approximately 82dB. The unity gain bandwidth is approximately 100 kHz. As for the stability, the phase margin of unity gain bandwidth is considered in general case. However, in my case the least phase margin is located at the circle site shown in the phase picture of Fig.3.17. Therefore, the phase margin in this circle site is considered for stability of the whole system. Fig.3.18 enlarges the circle site to show the unity gain bandwidth and the phase margin in detail.

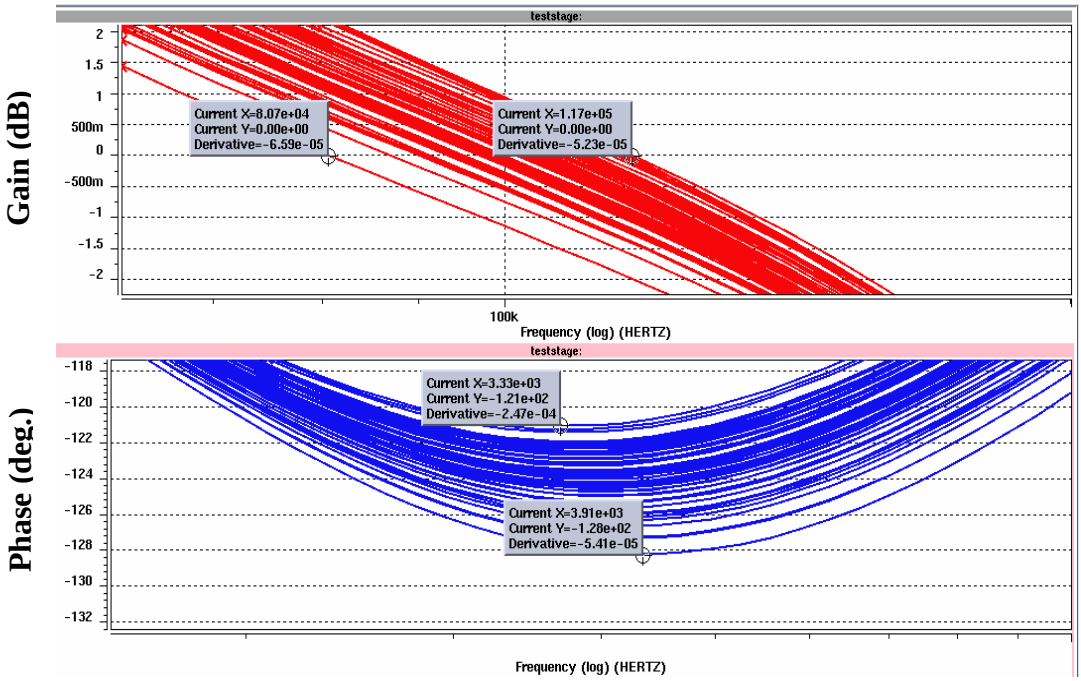


Fig. 3.18 The enlarged Gain and Phase of whole system

From Fig3.18, we can know that the unity gain bandwidth is 80.7MHz ~ 117 MHz and the phase margin is 51 degree ~ 59 degree. These results can be accepted in the operation of whole system.

Chapter 4

Circuit Design

In this chapter, the designed architecture of current mode buck regulator is introduced at first. Then each block of this regulator is presented and the circuit design is discussed in detail.

4.1 The Architecture of Current Mode Buck Regulator

The design of whole system in this thesis is presented in this section. The system block diagram of this current mode buck regulator is shown in Fig.4.1

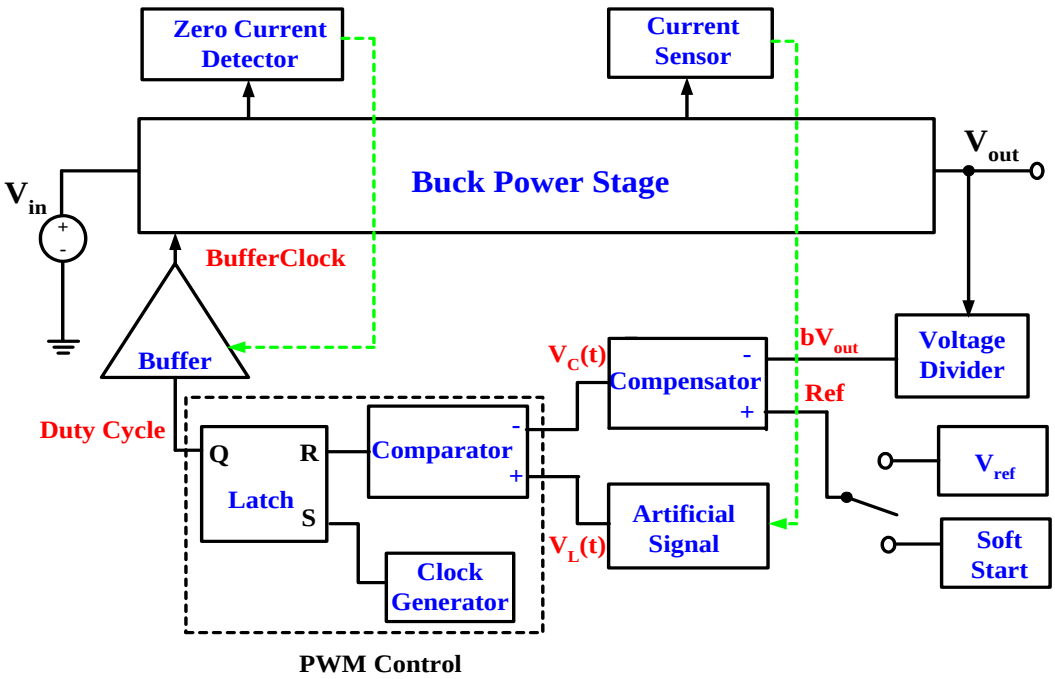


Fig.4.1 Block diagram of this current mode buck regulator

1. **Buck Power Stage:**

It transforms input voltage V_{in} into lower output voltage V_{out}. It is mainly composed of two transistors, one inductor and one capacitor. The two transistors which consist of power PMOS and NMOS are regarded as switching elements. By choosing appropriate conducting duration of the switching elements, we can obtain desired output voltage. The inductor and the capacitor constitute a loop pass filter which can filter high-frequency noise and retain low-frequency dc signal.

2. **Voltage Divider:**

It is commonly composed of resistor series. Output voltage V_{out} is scaled down to bV_{out} by the ratio of this resistor series and compared with a reference voltage. It is usually carried out outside of chip in order to adjust desired output voltage conveniently.

3. **V_{ref}:**

It is regarded as a reference value of output voltage. In order to certainly regulate the output voltage, it is desired to design V_{ref} constant and independent of the influence of the outside environment.

4. **Soft Start:**

In the beginning, this circuit will work instead of V_{ref} circuit and be compared with V_{out} until the output voltage reaches the desired voltage level. This action can avoid the beginning inrush inductor current caused by excessive large output signal of the compensator to damage the inner components of the system.

5. **Compensator:**

This circuit is composed of the operational amplifier, some resistors, and some capacitors. It provides extra gain and phase to compensate insufficient frequency response of whole loop. This appropriate compensation will make the system have more stability and performance.

6. **Artificial Signal:**

This circuit is proposed in the section 3.2. It mainly produces the addition of the sensed inductor current signal and the compensation ramp. And then by the comparison of this addition and the control signal $V_c(t)$ the desired duty cycle is created. In this thesis, I propose an improvement to make original constant slope of the compensation ramp become adjusted one to let frequency response of the system better.

7. PWM Control:

This control block is composed of the Comparator, the Clock Generator, and the SR Latch. It transforms the analog difference signal of output voltage and reference voltage to the digital pulse waveform to control on-time and off-time duration of the switch elements. And by this action, the system can adjust output voltage to desired voltage level.

The Clock Generator circuit provides a period pulse equal to switching frequency to initiate the on-time. The Comparator circuit provides a pulse produced by the comparison of $V_c(t)$ and $V_L(t)$to initiate the off-time. And then through SR Latch the both pulses create the desired duty cycle to regulate the output voltage of the system.

8. Buffer:

Because the size of both power transistors is large, the duty cycle produced by PWM Control block has no ability to drive both transistors. In order to pass efficiently the duty cycle signal on to power transistors, the buffer with enough driving ability is used. This buffer not only has large driving ability but also can prevent shot through current from occurring and damaging the inner circuits.

9. Current Sensor:

The inductor current signal is needed in the switching regulator with current mode control. So we need a Current Sensor circuit to obtain the information of the inductor current. The common method is to use a sensing resistor in series with inductor or power transistors. Although the sensed signal is accuracy, this circuit has high power dissipation. In this thesis, I use the mirror method to gain the signal which not only is proportional to on-time inductor current signal but also has low power loss.

10. Zero Current Detector:

In my thesis, in order to save power, I use power NMOS to substitute for original diode. Diode has an ability to block reverse inductor current automatically, but the power NMOS does not. If we disregard the occurrence of the reverse current, we will have an extra power loss in reverse current. So we must use a circuit “Zero Current Detector” to detect the reverse current in the inductor and then turn off the power NMOS to block the reverse current in this condition.

4.2 Power Transistors of Buck Power Stage [12]

The regulator is a bridge between supply source and load circuit. In theory, it is desirable that the regulator dissipates no power and power from supply source will completely delivers to load circuit, but in reality, it is impossible because it is not composed of real components. From above description, we can know that reducing the power dissipation of the regulator to increase conversion efficiency is an objective in circuit design.

The power transistors as the switching elements play an important role to decide output voltage by the duty ratio of on-time to off-time. When the transistor is at on-time state, the large current will flows through it to cause an extra power dissipation which is undesirable. The on-resistance of the power transistor can be approximately calculated as:

$$R_{onp} = \frac{1}{\mu_p C_{ox} (\frac{W}{L})_p \left| V_{gs} - V_t \right|} \quad \text{or} \quad R_{onn} = \frac{1}{\mu_n C_{ox} (\frac{W}{L})_n \left| V_{gs} - V_t \right|}$$

The power dissipation due to the on-resistance is calculated as:

$$\text{power dissipation} = D \times I_{Load} \times R_{onp} + D' \times I_{Load} \times R_{onn}$$

In order to decrease this power dissipation, the only way is to reduce the R_{onp} and R_{onn}. By the efficiency requirement > 80%, the ratio W/L must be several ten thousands. The huge sizes of power transistors occupy very large area and are almost 1/2 or 2/3 in whole layout. Therefore, if we can effectively reduce the area of the transistors by layout scheme, the whole layout area will be notably lowered and the cost also decreases for this reason. A lateral transistor scheme is proposed shown in Fig.4.2 (b). It does not need any additional processes, and it can shrink the transistor size compared with the multi-finger transistor scheme shown in Fig.4.2 (a).

Form Fig.4.2 (b), we can know that the lateral transistor scheme uses the lateral side areas, which the traditional multi-finger transistor scheme does not use, to form the extra transistors. Therefore, the more transistors can be constructed in the same area.

Fig.4.3 shows a comparison of lateral transistor scheme and multi-finger transistor scheme in transistor type. In Fig.4.3, the (a) has the 6units and (b) has the 12 units with the same active region. It shows that the lateral transistor scheme is two times area-saving of the multi-finger scheme. But in reality, the area-saving is impossible good to two times because of the arrangement and configuration of whole layout. However, it is fact that the

lateral transistor scheme is indeed more area-saved than the multi-finger transistor scheme.

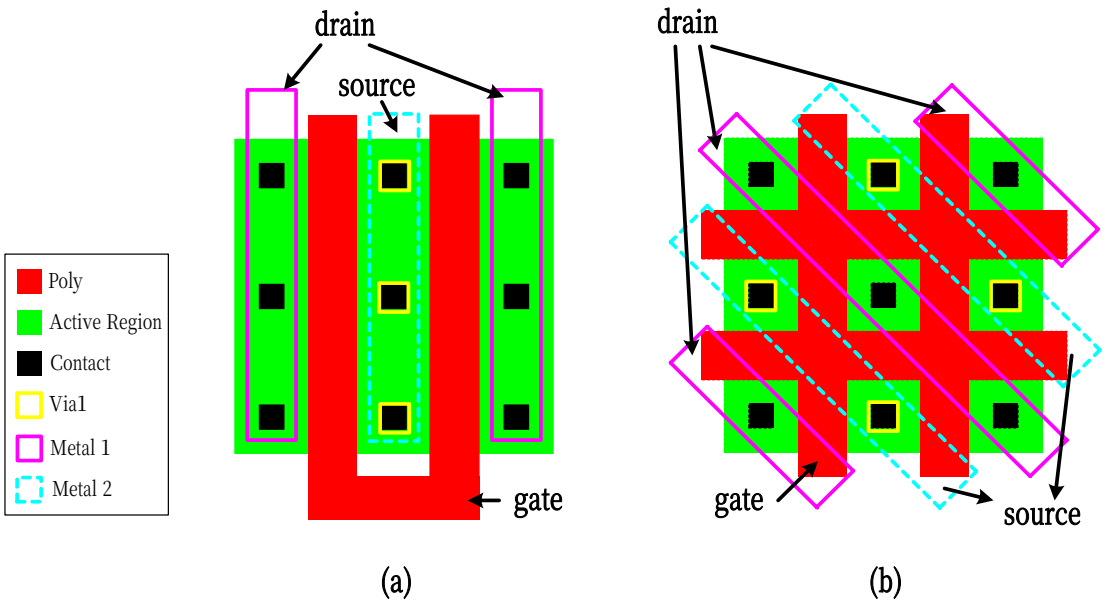


Fig.4.2 (a) multi-finger transistor scheme (b) lateral transistor scheme

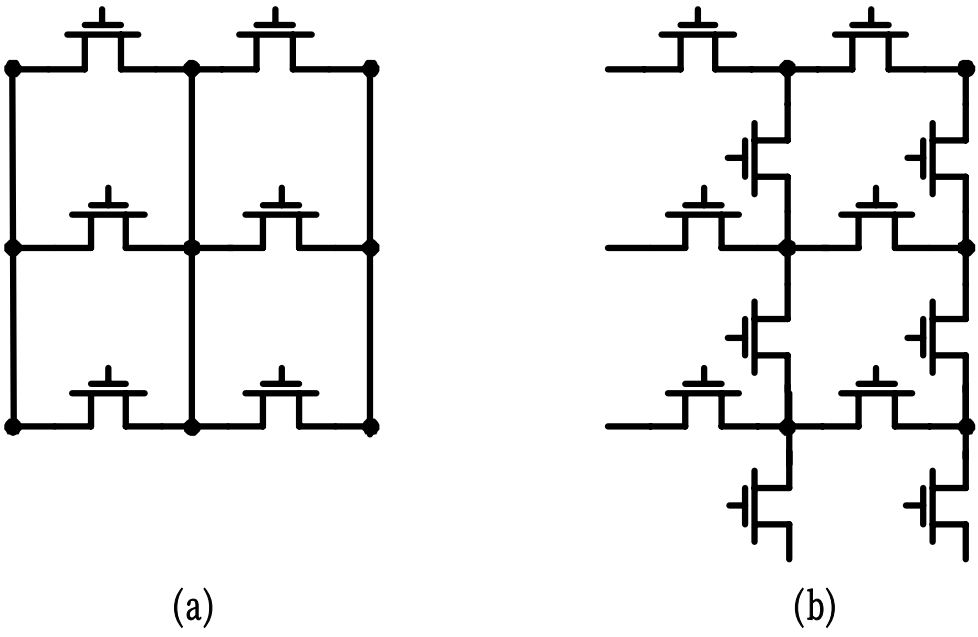


Fig.4.3 Transistor Type (a) multi-finger transistor (b) lateral transistor

4.3 Bandgap Voltage Reference Circuit [13] [14] [15] [16]

In the feedback circuit, the output voltage is scaled down to bV_{out} to be compared with the V_{ref}. In order to efficiently regulate output voltage, the V_{ref} must be constant, and independent of the influence of outside environment. So the bandgap voltage reference circuit is used to achieve desired effect.

The bandgap voltage reference commonly exhibits little dependent on temperature prove essential in many analog circuits. Because most processes parameters vary with temperature, if a reference is temperature-independent, then it is usually process independent as well.

In convenience, a dc voltage independently of temperature is achieved by adding a voltage, which is proportional to the absolute temperature (PTAT), to a base-emitter voltage inverse proportional to the absolute temperature in order to compensate for its first-order temperature dependency as shown in Fig.4.4.

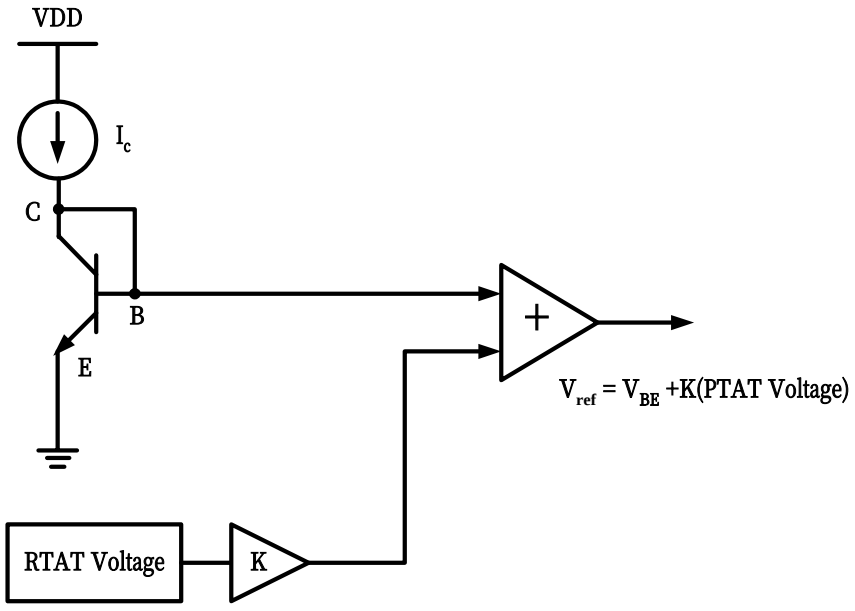


Fig.4.4 General principle of bandgap voltage reference

This PTAT voltage is commonly recognized as V_T*lnN the difference of the base-emitter voltages of two bipolar transistors which operate at unequal current densities. Since at room temperature $\frac{\partial V_{BE}}{\partial T} \approx -1.5\text{mV/}^{\circ}\text{K}$ whereas $\frac{\partial V_T}{\partial T} \approx +0.087\text{mV/}^{\circ}\text{K}$, we can obtain V_{ref} with zero temperature coefficients, indicating that

$$V_{ref} \approx V_{BE} + K(V_T \ln N) \approx 1.25V \qquad (4\text{-}1)$$

From Eq.(4-1), we know that the output voltage of traditional reference circuit independent of temperature is only one value ($\approx 1.25V$). In order to conform to the specification required, the traditional reference circuit is not used in my design because the reference voltage must be lower than 0.5V.

A bandgap voltage reference can provide a voltage lower than 0.5V by resistive subdivision shown in Fig.4.5.

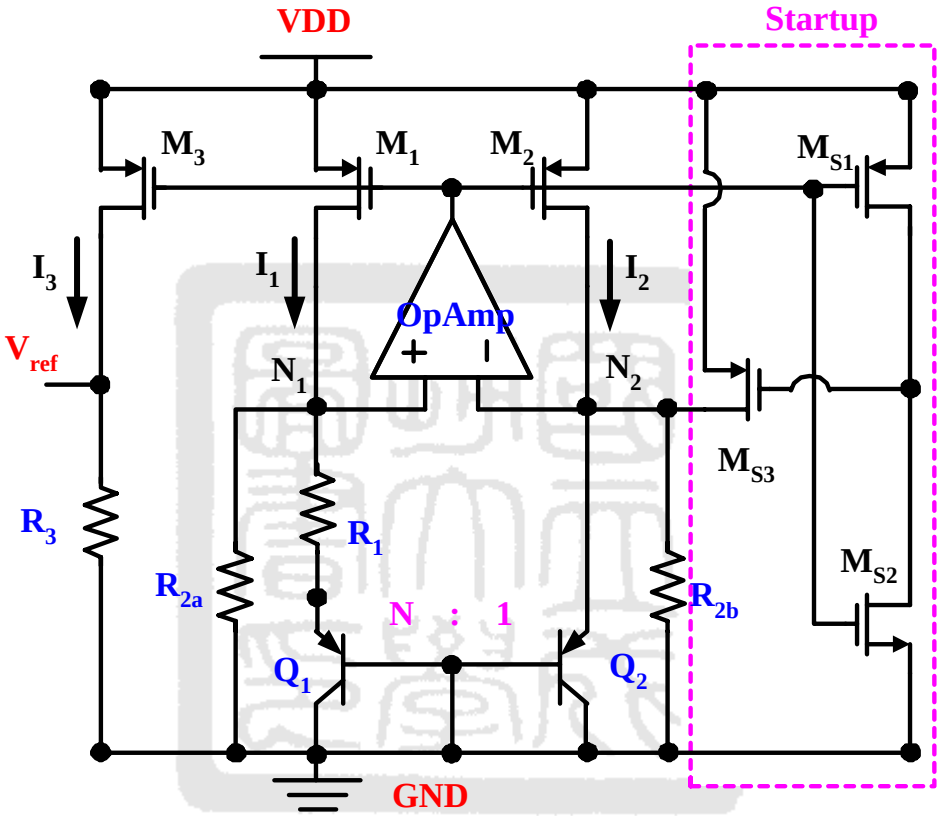


Fig. 4.5 The circuit of bandgap voltage reference

As illustrated in Fig.4.5, the operational amplifier (OpAmp) enforces nodes N1 and N2 to have the same potential. Therefore, the loop formed by Q_1, Q_2, R_1, R_{2a}, R_{2b} generate a current I_1 given by

$$I_1 = \frac{V_{EB2}}{R_2} + \frac{V_T \times \ln(N \times I_2/I_1)}{R_1} \qquad (4\text{-}2)$$

Where N is the emitter area ratio, V_T is the thermal voltage, and $R_{2a}=R_{1a}=R_2$. The current $I_1=I_3$ is injected to R_3 by current mirror formed by M_1, M_3, and this gives the reference voltage as follow:

$$V_{ref} = \frac{R_3}{R_2} \times [V_{EB2} + \frac{R_2}{R_1} \times V_T \times \ln(N \times I_2/I_1)] \quad (4\text{-}3)$$

Not only a scaled-down voltage of bandgap circuit can be obtained by an appropriate resistor ratio of R_3 to R_2, but also a good temperature coefficient can be achieved by the other resistor ratio of R_2 to R_1.

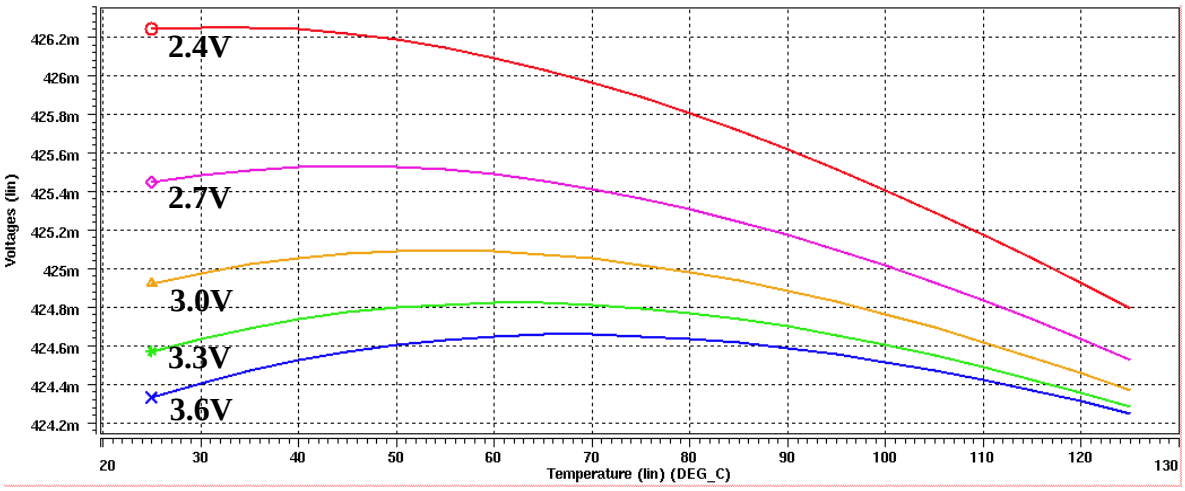
The startup circuit in bandgap voltage reference plays an important role to make this circuit operate in correct condition. It is composed of M_{s1}, M_{s2}, and M_{s3} shown in right side of Fig.4.5. The three transistors including M_{s1}, M_{s2}, and M_{s3} mainly form a function of inverter. The W/L value of M_{s2} is chosen be much less than one, and the W/L value of M_{s1} are the same as those of M_1~M_3 to eliminate the variation on threshold voltage due to geometry effect. When the circuit starts initially, the gate voltages of M_1~M_3 and M_{s1} are pulled high to near VDD. And then the drain voltages of M_{s1} and M_{s2} are pulled low to turn on Ms3 to inject current to bandgap core circuit. By the operation of startup circuit, the core circuit will work in correct condition, not in zero state. When core circuit already works in steady-state, the operational amplifier (OpAmp) forces the drain voltage of M_1 to increase by pulling down the gate voltages of M_1~M_3 to inject current. Once the gate voltage of M_{s1} decreases, the drain voltage of M_{s1} and M_{s2} pulls high and cut off M_{s3}. This action is to stop the work of the startup circuit in order to avoid influencing the accuracy of the core circuit.

After the description of whole circuit, we will consider the effect of offset voltage and noise. Bandgap voltage reference in MOS technology suffers from the effect of transistor size and threshold. This may influence absolute reference voltage and temperature coefficient and lower its original performance. The effect of the offset voltage (V_{offset}) of the operational amplifier (OpAmp) is considered as follows:

$$Vref = \frac{R_3}{R_2} \times \{V_{EB2} + \frac{R_2}{R_1} \times [V_T \times \ln(N \times I_2/I_1) + V_{offset}]\} \quad (4\text{-}4)$$

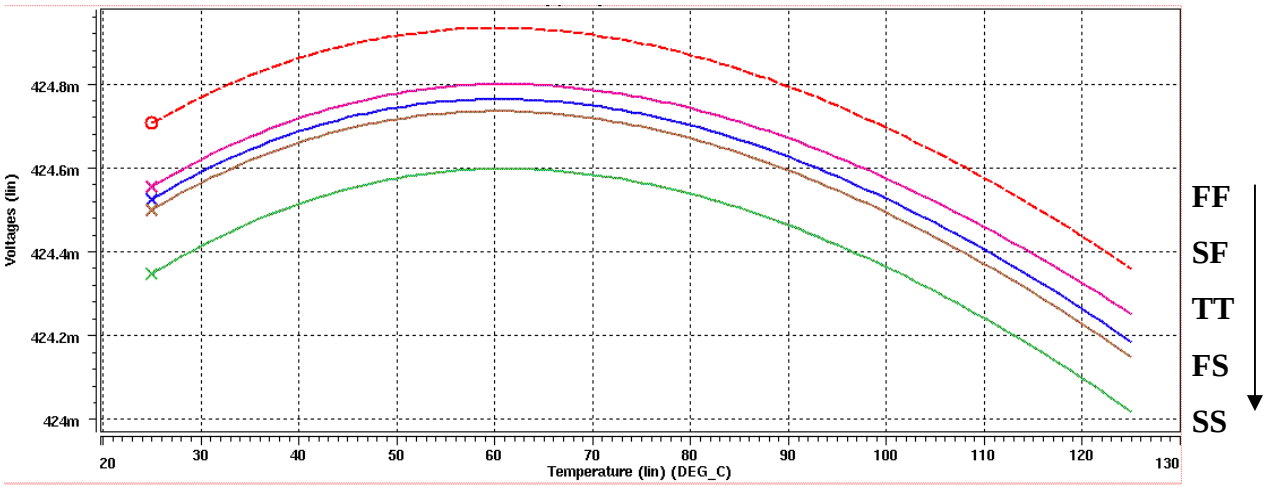
However, this effect can be reduced by increasing the term value of $\ln(N \times I_2/I_1)$. The value of $(N \times I_2/I_1)$=100 is chosen in my design. In general way, I_2=I_1 and the emitter area ratio N=100 may be used to save power. But it occupies quite large area in layout. So I use I_2=10I_1 and N=10 which increases some power loss but occupies very small area to achieve the same effect. The simulation result of the bandgap voltage reference is shown in Fig.4.6 and Fig.4.7. Fig.4.6 shows the Temperature coefficient (TC) from 25 ˚ C to 125 ˚ C

at different supply voltage. The TC at V_{supply} = 3.6V is 12ppm/ ° C and increases slightly to 33ppm/ ° C at V_{supply}=2.4V. Fig.4.7 shows the value of reference value at different corner. The maximum deviation at different corner is approximately 0.4mV. These results are enough to conform to my requests.



Five supply voltage (V_{supply}): 2.4V, 2.7V, 3.0V, 3.3V ,3.6V

Fig.4.6 The reference voltage vs. temperature at different supply voltage



Five corner: FF, SF, TT, FS ,SS corresponding to Up-wave → Down-wave

Fig.4.7 The reference voltage vs. temperature in V_{supply} = 3.3V at different corner

4.4 Soft Start Circuit [17]

If the regulator has no soft-start action, when the supply is turned on, initially the output voltage of the regulator is in zero state and then slowly charges to desired voltage level. In this duration, the difference of the plus input of the compensator V_{ref} which is a constant voltage and the minus input bV_{out} which is proportional to V_{out} will be much large

to let the output of the compensator remain in high level. This phenomenon makes the system work in on-time state (PMOS on & NMOS off) and continues to charge current to an exaggerated degree. This possibly causes the EMI problem, the damages of inner components, and input voltage drops when a battery or a high-impedance power source is connected to the input of the regulator. So in order to eliminate this large inrush current, the soft-start action must be realized to avoid the initial continued on-time state.

The Soft Start circuit is shown in Fig.4.8. It is composed of a current source, a capacitor, and a comparator. The current I and the capacitor C mainly decide the soft start duration. If it is too short, the effect of eliminating inrush current is bad but if it is too long, the capacitor C must be large size. So how long the duration is must be considered appropriately to get good performance and cost.

As illustrated in Fig.4.8, when the source starts initially, the comparator output is low and the slowly charging capacitor output voltage V_{soft} is used as a reference voltage for the regulator. After the regulator reaches a predetermined threshold, the comparator output goes high and the dynamic control signal enables the reference signal V_{ref} to control the dc–dc regulator.

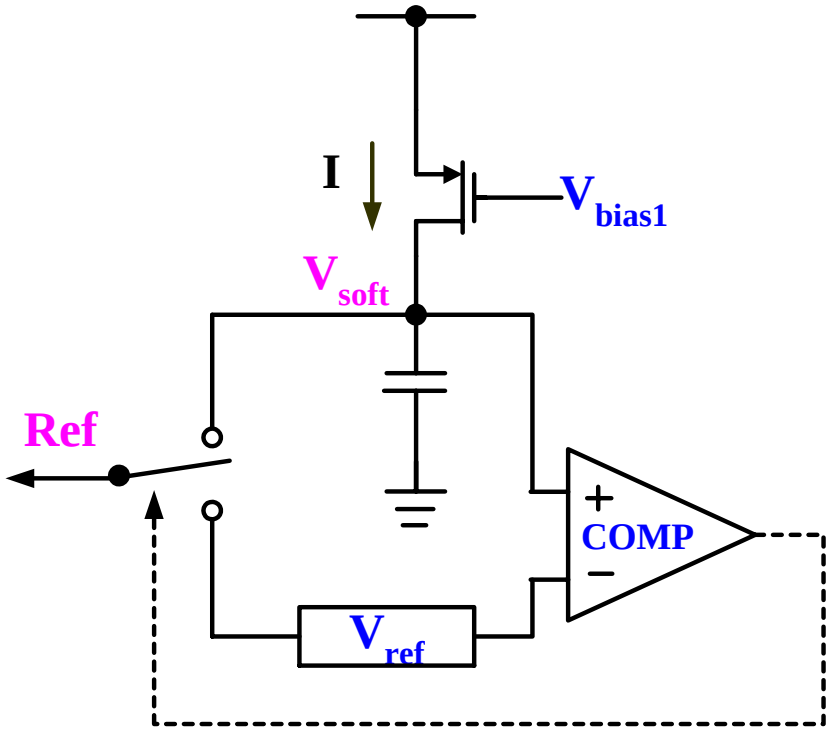


Fig. 4.8 The circuit of Soft Start Circuit

Fig 4.9 shows the simulation waveform of V_{ref}, V_{soft}, and Ref.

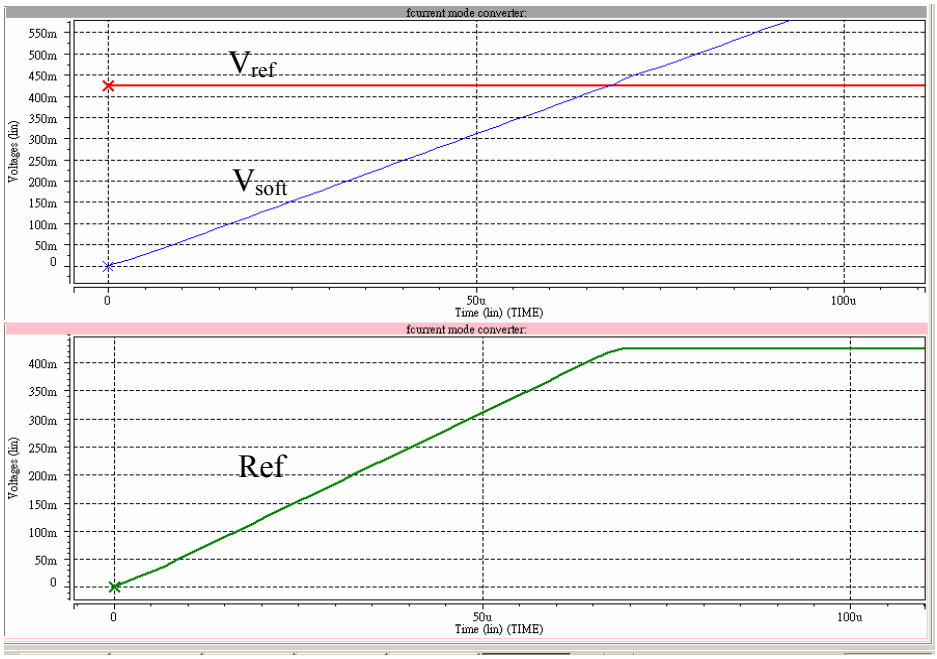


Fig. 4.9 The simulation results of the soft start circuit

4.5 Operational Amplifier Circuit for Compensator [14] [15]

The design of compensator is already investigated in section 3.3. The appropriate resistors and capacitors are chosen to produce a type II compensator to compensate insufficient gain and phase of the whole loop. After accomplishing the design of passive elements, in this section the focus is how to implement an operational amplifier suitable for this compensator.

A two-stage operational amplifier is used in my design. A block diagram of a typical two stage operational amplifier is shown in Fig.4.10. ”Two-stage” refers to the number of gain stages in the operational amplifier.

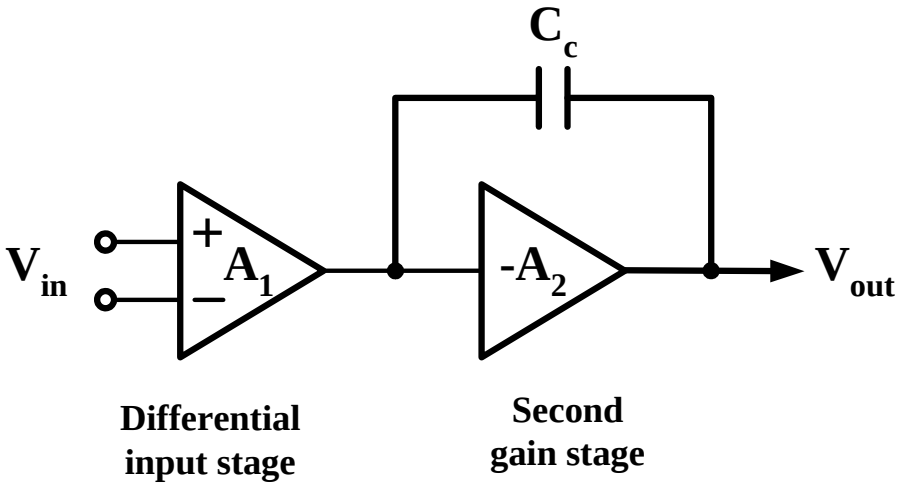


Fig. 4.10 A block diagram of two-stage operational amplifier

The first gain stage is a differential-input single-ended output stage. The second gain stage is normally a common-source gain stage that has an active load. Capacitor C_c is included to ensure stability when the operational amplifier is used with feedback. Because C_c is between the input and the output of the second stage, it is called Miller capacitance since its effective capacitive load on the first stage is larger than its physical value.

The practice two-stage operational amplifier circuit is adopted as shown in Fig.4.11. Firstly, the overall gain of operational amplifier is discussed. For dc-to-dc regulator application, the low frequency gain is one of the most critical parameters. The more this gain value, the better the performance of voltage regulation. The gain of first stage is:

$$A_{v1}=g_{m1}\,(r_{ds2}||r_{ds4}) \tag{4-5}$$

The second gain stage is simply a common-source stage with a p-channel active load 'M6'. Its gain is:

$$A_{v2}=-g_{m7}\,(r_{ds6}||r_{ds7}) \tag{4-6}$$

Where the approximation values $g_{mp}=\sqrt{2\mu_p C_{ox}(\frac{W}{L})I_D}$, $g_{mn}=\sqrt{2\mu_n C_{ox}(\frac{W}{L})I_D}$ and $r_{dsi}=5*10^6\frac{L_i}{I_{Di}}\sqrt{V_{DGi}+V_{ti}}$ are used to estimate the desired gain value. Secondly, the frequency response of operational amplifier is discussed. The second stage introduces primarily a capacitive load on the first stage due to the Miller effect of the capacitor Cc. By this relation and some calculations, we can obtain a simple overall gain in middle frequency as follows.

$$A_v(s)=\frac{g_{m1}}{sC_c} \tag{4-7}$$

This equation can be used to find the approximate unity-gain frequency.

$$\omega_{ta}=\frac{g_{m1}}{C_c} \tag{4-8}$$

Note here that the unity-gain frequency is directly proportional to g_{m1} and inversely proportional to C_c. By the equation of gain and unity-gain frequency, we can obtain the approximate size values of all transistors except M8. This transistor operates in triode region and as a resistor. The resistor value is given by

$$r_{ds8} \approx \frac{1}{\mu_n C_{ox} (\frac{W}{L})_8 (V_{GS} - V_t)_8} \tag{4-9}$$

It is included in order to realize a left-half-plane zero at frequencies around or slightly above unity-gain frequency. Without the transistor M8, we have a right-half plane zero which makes the compensation much more difficult. The addition of such an extra left-half-plane zero is what is commonly called “lead-compensation”. The common choice of r_{ds8} according to

$$r_{ds8} = \frac{1}{1.2 g_{m1}} \approx \frac{1}{1.2 \omega_t C_C} \tag{4-10}$$

This choice will increase the unity-gain frequency by ~ 20%, leaving the zero near to the final resulting unity-gain frequency, which will end up ~15% below the equivalent second pole frequency.

Some frequency characteristics about gain and phase of operational amplifier are arranged in Table. 4.1

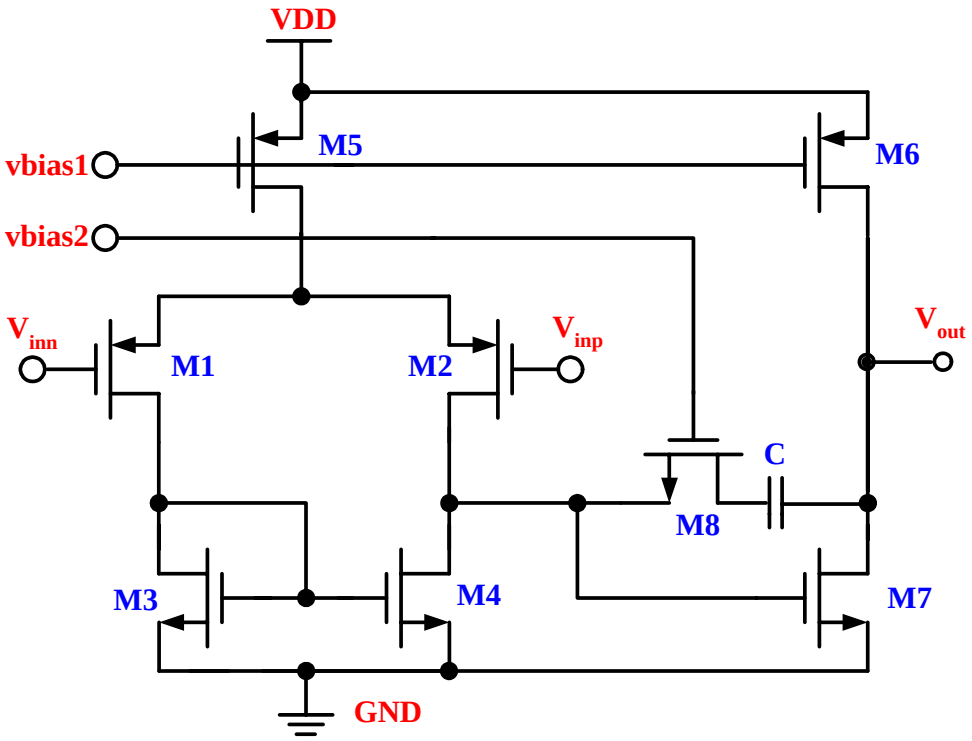


Fig. 4.11 The circuit of two-stage operational amplifier

Table.4.1 The frequency characteristics of the operational amplifier (a)TT-55 ˚C (b) SS- 125 ˚C (c) FF-25 ˚C

(a) TT-55 ˚C

TT-55 ˚C/ supply voltage(V)	2.4	2.7	3.0	3.3	3.6
DC gain (dB)	73.84	74.08	74.20	74.26	74.26
Unity gain bandwidth (MHz)	44.40	45.59	46.64	47.58	48.44
Phase margin (˚)	82.61	82.63	82.64	82.64	82.64

(b) SS-125 ˚C

SS-125 ˚ / supply voltage(V)	2.4	2.7	3.0	3.3	3.6
DC gain (dB)	71.27	71.58	71.76	71.85	71.89
Unity gain bandwidth (MHz)	44.92	45.70	46.46	47.62	47.81
Phase margin (˚)	80.32	80.61	80.77	80.89	82.98

(c) FF-25 ˚C

FF-25 ˚C/ supply voltage(V)	2.4	2.7	3.0	3.3	3.6
DC gain (dB)	74.64	74.78	74.85	74.86	74.83
Unity gain bandwidth (MHz)	42.92	44.22	45.42	46.55	47.59
Phase margin (˚)	83.37	83.29	82.16	83.02	82.88

4.6 Artificial Signal Circuit

In current mode regulators, the compensation ramp needs to add with the inductor current signal in order to avoid sub-harmonic oscillation. The Artificial Signal circuit is used to implement this function in my design.

There are commonly two ways to implement the addition of the inductor current signal and the compensation ramp. One way is that the two signals are summed in voltage form. This way needs higher impedance between two signals to block the mutual influence. Therefore, this way shown in Fig.4.12 (a) is usually implemented outside chip. The other way is that the two signals are summed in current form. Current signals are summed easily and accurately without high impedance, so this way shown in Fig.4.12 (b) is usually implemented inside chip.

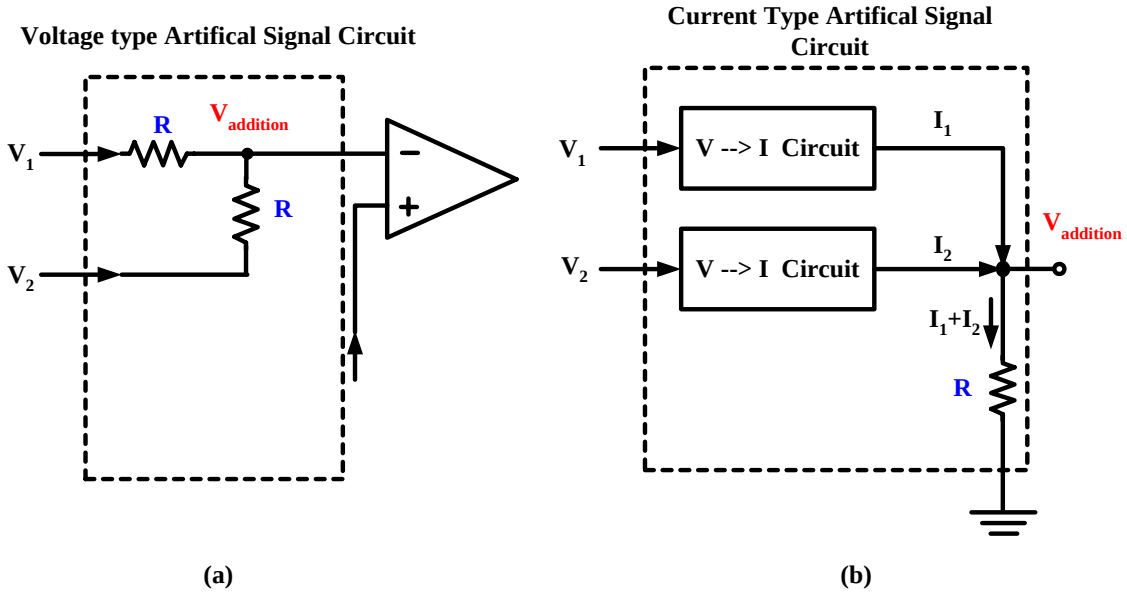


Fig. 4.12 The circuit of the addition (a) voltage type (b) current type

My way is implemented inside chip and can reach the effect of adjusted-slope compensation ramp discussed in section 3.2. From section 3.2, we can know that by choosing the slope of the compensation ramp equal to off-time slope of the inductor current V_{out} / L, the slope of the addition wave must be proportional to input voltage V_{in} and equal to V_{in}/L. Therefore, this way is not like the way shown in Fig.4.12 (b) which needs V-I converter and only needs a current source proportional to input voltage V_{in} to directly produce the addition wave. The detailed circuit is shown in Fig.4.13 (a).

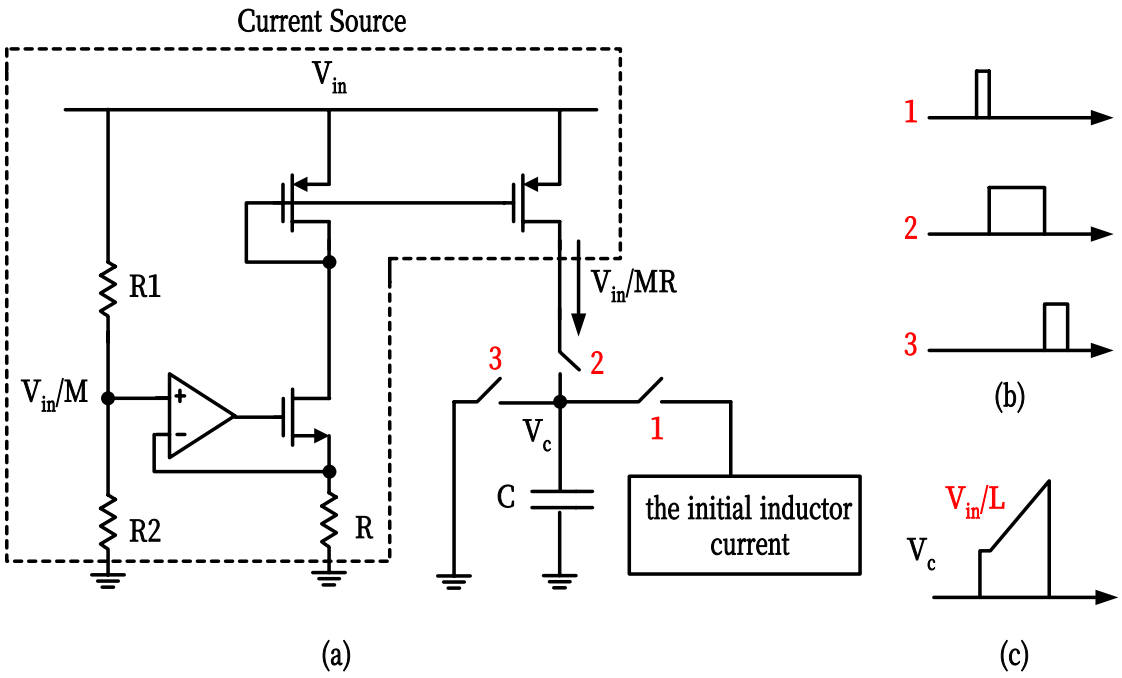


Fig. 4.13 (a) circuit (b) conducting time of the switch 1, 2, 3(c) the voltage of the capacitor V_c

A current source proportional to V_{in} is built as shown in Fig.4.13. An OpAmp is used to enforce V_A to be equal to V_B. Due to $V_A=V_B$ and $V_A=V_{in}/M$, M_1 has a current equal to V_{in}/MR and proportional to V_{in}. And then by mirror method, M_2 can obtain a same current as the current in M_1. Finally, choosing appropriate the values of the resistor R1, R2, R, and the capacitor C makes the charging slope of the capacitor C equal to the value V_{in}/L to conform to my requirement. In the aspect of power dissipation, this circuit only needs a low-speed OpAmp which enforces the same DC voltage in two nodes, so its power dissipation is very small and smaller than Fig.4.12 (b). As for the operation of this circuit, it is shown in Fig.4.13 (b), (c) and described in section 3.2.

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4.7 PWM Control Circuit [14] [18]

The function of this circuit is to transform the comparison of control signal $V_c(t)$ and inductor current signal $V_L(t)$ in Fig.4.1 into an appropriate duty cycle which can adjust the output voltage of the system to desired voltage level. It is composed of the comparator, the clock generator, the SR-latch. These circuits will be introduced below the sections

4.7.1 Comparator Circuit

Comparators are the second most widely used components in electronic circuits after operational amplifier. A comparator is a circuit that compares the instantaneous value of an input signal with a reference voltage and produces a logic output level depending on whether the input is larger or smaller than the reference level.

The comparator is used in my design shown in Fig.4.14. It is implemented by three stages. The first stage has an n-channel differential input pair with the positive feedback circuit. The second stage has a p-channel differential input pair with an n-channel current mirror active load. The third stage is an inverter chains.

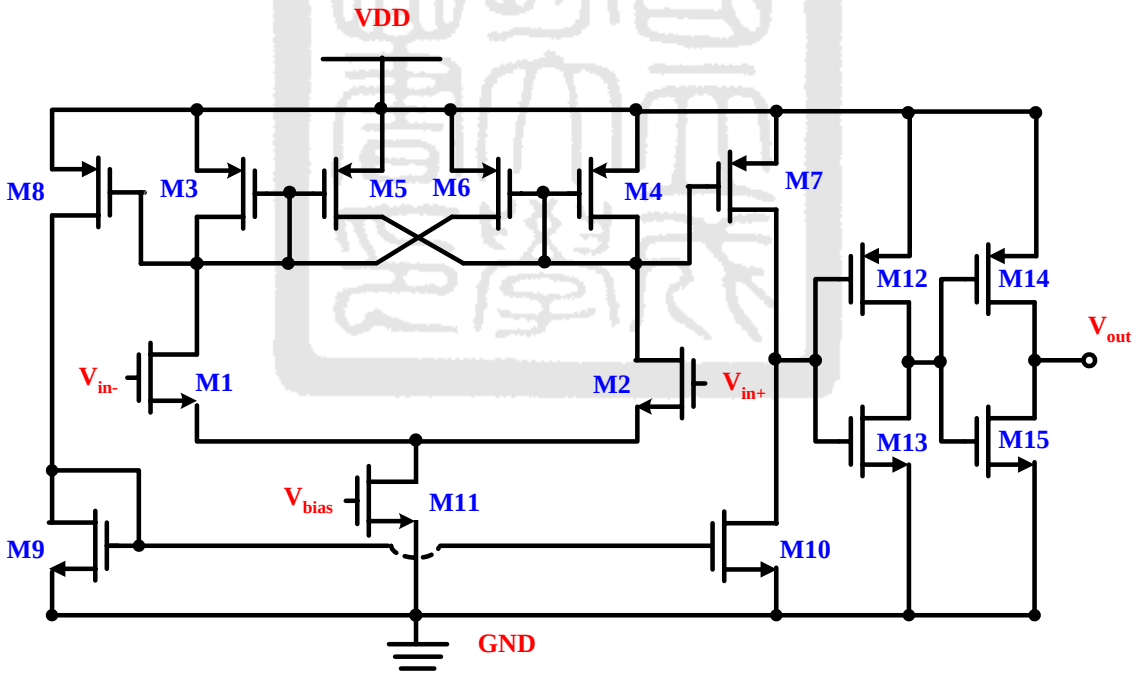

Fig. 4.14 The circuit of the comparator

The transistors of M3, M4, M5, and M6 form the positive feedback gain stage. The gain of the positive feedback gain stage is given by

$$A_v = \sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_3}} \frac{1}{1-\alpha} \qquad (4\text{-}11)$$

Where $\alpha = (W/L)_5 / (W/L)_3$ is the positive feedback factor that is responsible for increasing the gain. The value of α is determined by the ratio of the load device dimensions, and although it is a reasonably well controlled parameter, for α beyond 0.9, mismatches due to process variations may cause this value to approach unity. This will make the stage operate as a cross-coupled latch. The transistors of M7, M8, M9, and M10 constitute the second stage. This stage mainly contributes some gain in whole circuit. The gain of the second stage is:

$$A_{v2} = g_{m7}(r_{ds7} // r_{ds10}) \qquad (4\text{-}12)$$

The third stage constituted by the inverter chains M12, M13, M14, and M15 are used to increase the response of output signal. With the usage of this stage, the size of M7 and M8 can be reduced to achieve same performance and due to the reduction of M7 and M8, the effect of the parasitic capacitance at gates of M7 and M8 is decreased which results in a faster response.

The simulation results of the comparator are shown in Fig.4.15 and Fig.4.16.

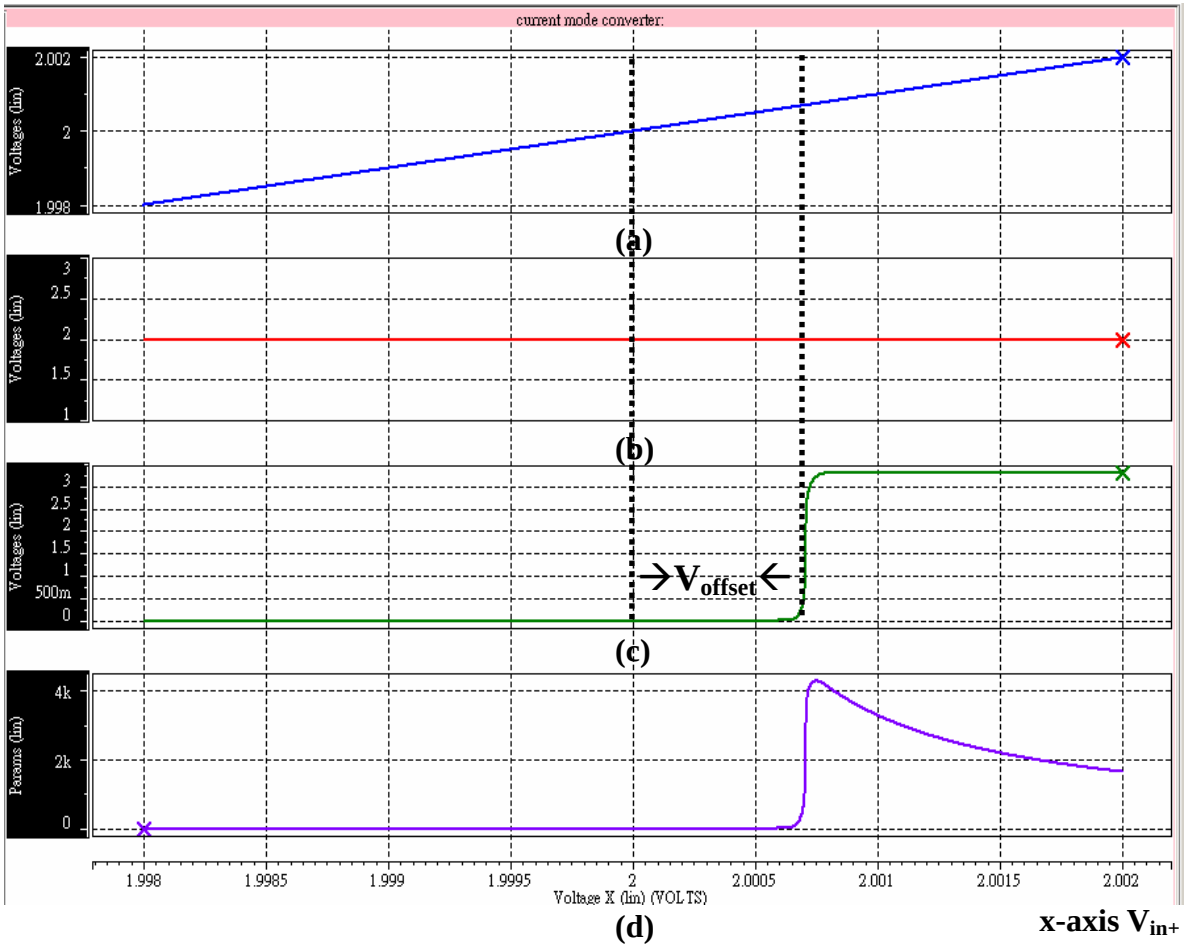

Fig. 4.15 DC characteristic of the comparator (a)V_{in+} (b)V_{in-} (c)V_{out} (d)Gain

Fig.4.15 shows the dc characteristics of comparator when V_{in-} holds at 2V and V_{in+} is swept form 1.998V to 2.002V. Fig.4.15 (c) shows that the offset voltage of the comparator is approximately 0.7mV. Fig4.15 (d) shows that the gain of the comparator is approximately 4300.

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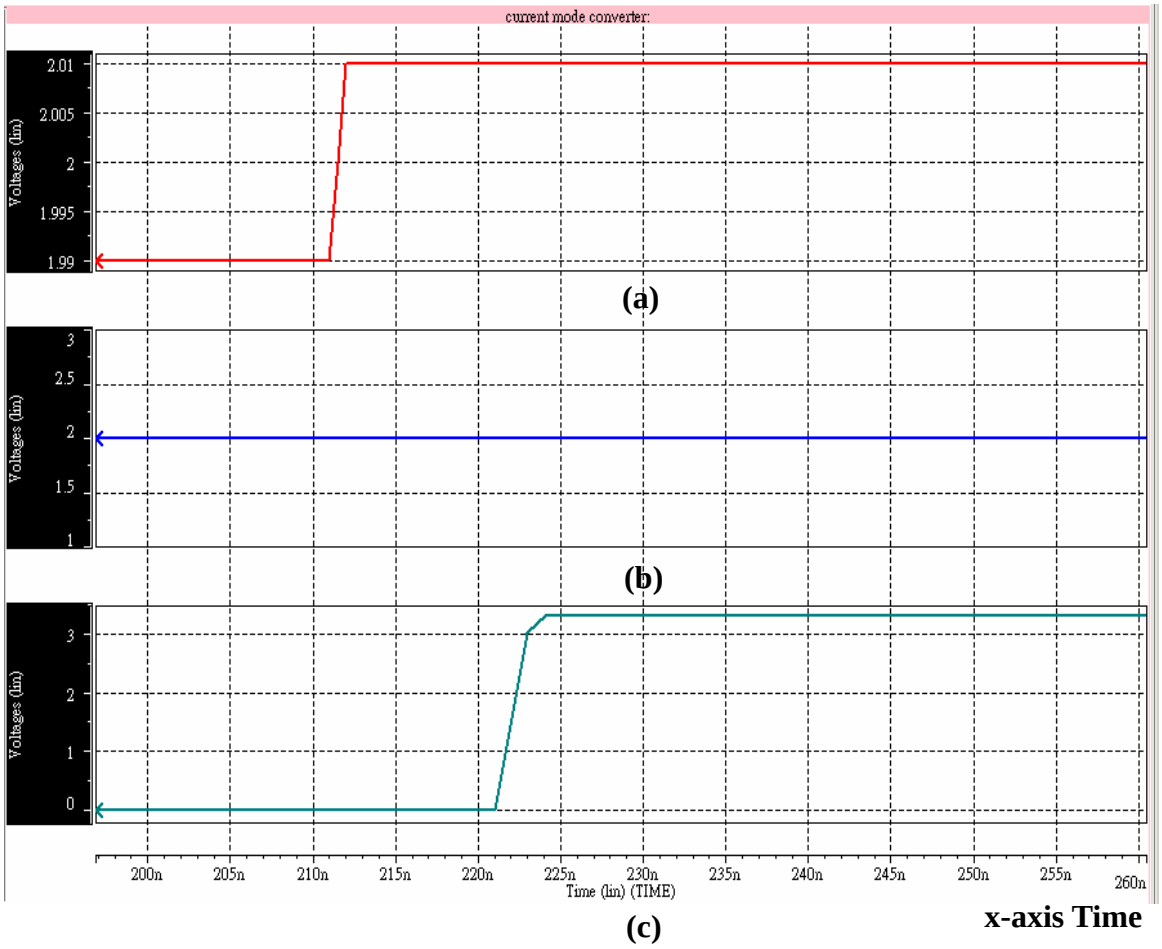


Fig. 4.16 Transient characteristic of the comparator (a)V_{in+} (b)V_{in-} (c)V_{out}

Fig.4.16 shows the Transient characteristics of comparator when V_{in-} holds at 2V and V_{in+} is swept form 1.99V to 2.01V. Fig.4.16 (c) shows that the delay time of the comparator is around 13ns, which is adequate for my application with switching frequency 500 kHz.

4.7.2 Clock Generator Circuit

The clock frequency inside my chip is needed about 500kHz. The circuit with this frequency in IC design is commonly regarded as the low-speed application. For low-speed application, the ring oscillator circuit is not suitable for use because the extreme stages will make design complex and cost a lot of chip area. In order to produce this clock frequency,

a small current source is used to charge and discharge a large capacitor shown in Fig.4.17

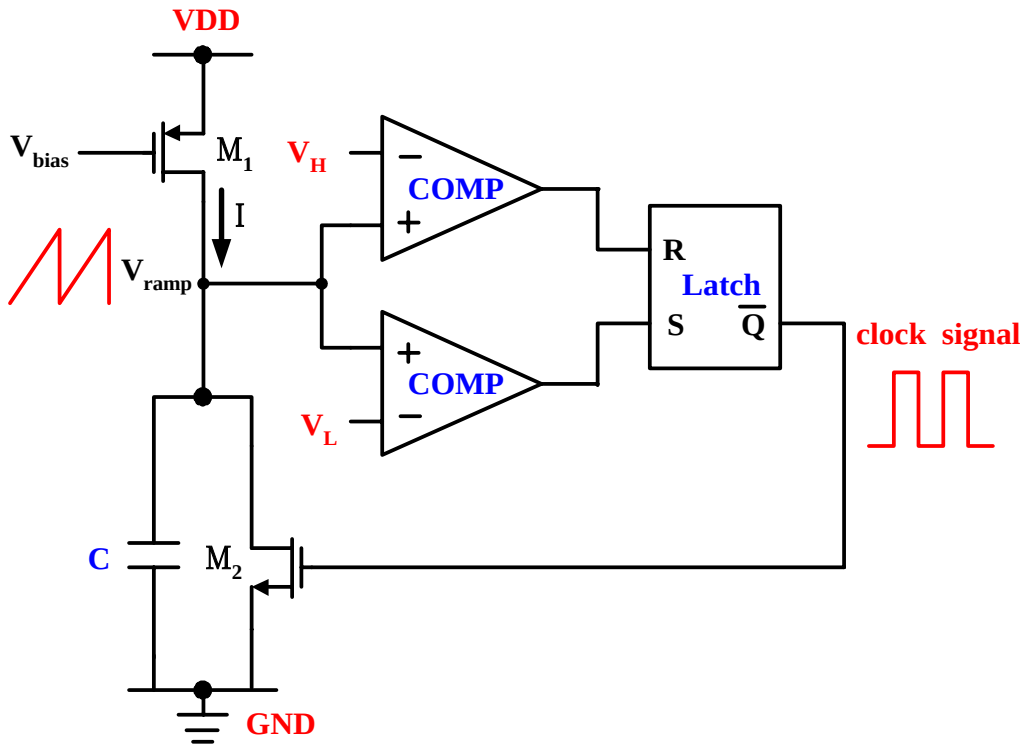


Fig. 4.17 The circuit of the clock generator

This circuit works with two states. One is charging state. The other is discharging state. Initially, the charging state is starting. A current source M_1 produces a nearly constant current to charge the capacitor C. When the voltage of the capacitor charged V_{ramp} reaches the V_H, the comparator changes the state and then the transistor M_2 turns on to discharge the capacitor C to start the discharging state. Normally, the discharging current is much larger than the charging current. When the capacitor is discharged, the voltage of the capacitor V_{ramp} continues to drop until it reaches V_L and then the comparator changes the state to turn off transistor M_2 to begin the charging state again. These actions will produce a period pulse with fixed frequency. This fixed frequency can be designed as:

$$\text{frequency} = \frac{I}{C} \times \frac{1}{(V_H - V_L)} \tag{4-13}$$

Where current I is produced by a constant current source M_1 which is mirrored by bandgap reference. The voltage V_H and V_L is also produced by bandgap reference. So the deviations of I, V_H, and V_L are almost ignored. As for the capacitor, in order to reduce the usage of the outside passive components, it is integrated into chip. Due to the factors of technology, temperature and so on, the deviation of the capacitor C is approximately equal to -10% ~

+10%. So the practice clock frequency possibly is not just 500 kHz and distributes over the range of 450 kHz and 550 kHz but this deviation is still tolerated in my design.

The comparators used in this clock generator circuit belong to p-type comparator. The design is similar to the design of the n-type comparator illustrated in the section 4.7.1. The circuit and the true table of SR latch used in this circuit are shown in Fig.4.18 and Table 4.2.

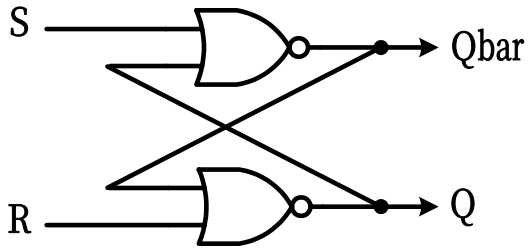


Fig. 4.18 The circuit of SR latch

Table.4.2 The truth table of SR latch

SR Latch Truth Table				
	S	**R**	**Q(n+1)**	**Qbar(n+1)**
State 1	**0**	**0**	**Q(n)**	**Qbar(n)**
State2	**1**	**0**	**1**	**0**
State3	**0**	**1**	**0**	**1**
State4	**1**	**1**	**Forbidden**	

From truth table in Table.4.2, we can know that the state 4 must be forbidden because when S=1→0 and R=1→0, the output of the SR latch will oscillate. In order to make the circuit stable, this state must be avoided in any condition. In my clock generator circuit, the SR latch mainly operates in three states of stae1, stae2, and state3 which do not cause oscillation and instability.

4.7.3 SR Latch Circuit

The SR latch illustrated in section 4.7.2 is used for the pulse-width generator in PWM control circuit in Fig.4.1. In the steady state operation of the current mode buck regulators, both inputs of SR latch may not be high simultaneously. But during the startup, the one input R namely the output of compensator is possibly at high level state because in this moment the system needs large current to charge output voltage to a desired level. The other input S fed by clock generator becomes high level periodically. So the two inputs of

SR latch are possibly at high level simultaneously during the startup time. In order to avoid this condition, the implementation of the advanced SR latch is shown in Fig.4.19 [18].

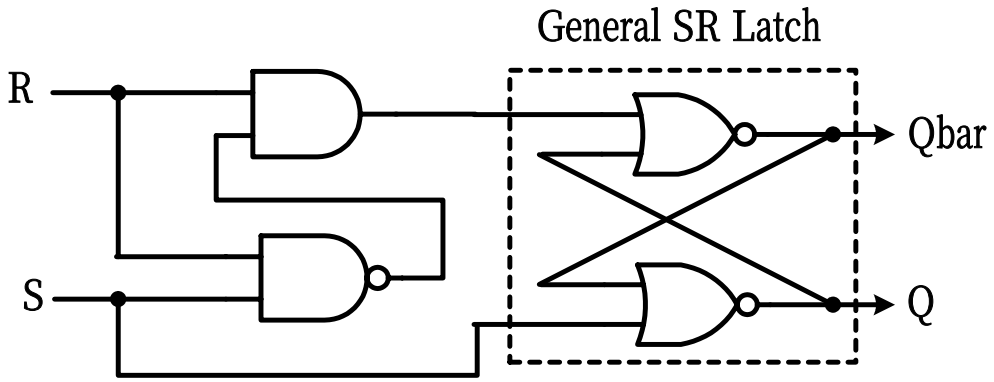


Fig. 4.19 The circuit of advanced SR latch

AND and NAND logic gates are added with general SR latch to implement an advanced SR latch. These two logic gates can ensure that both inputs of general SR latch are not high simultaneously. The new truth table is shown in Table.4.3

Table.4.3 The truth table of advanced SR latch

SR Latch Truth Table				
	S	**R**	**Q(n+1)**	**Qbar(n+1)**
State 1	**0**	**0**	**Q(n)**	**Qbar(n)**
State2	**1**	**0**	**1**	**0**
State3	**0**	**1**	**0**	**1**
State4	**1**	**1**	**1**	**0**

From table.4.3, we know that when both inputs are high, the state of the latch is set which is equal to state 2. So by this implementation, the oscillation and instability problem can be avoided.

4.8 Buffer Circuit [18]

In switching regulators, the size of the two power transistors as switching elements must be large in order to reduce conduction loss. Due to the large size of these two transistors, it does not have enough ability to drive so large loads by only the PWM control. Therefore, a buffer with the enough driving ability is needed. Generally, the buffer is designed by a simple inverter chains. This inverter chains is constituted by the cascaded inverter stage with a tapering factor of 3 to 4. But if the buffer is poorly designed to let two power transistors conduct simultaneously, a shoot-through current will occur and large current which passes through the power transistors will cause the damages of inside components and an extra large power loss. So a buffer with dead-time which avoids shoot-through current is needed as shown in Fig.4.20

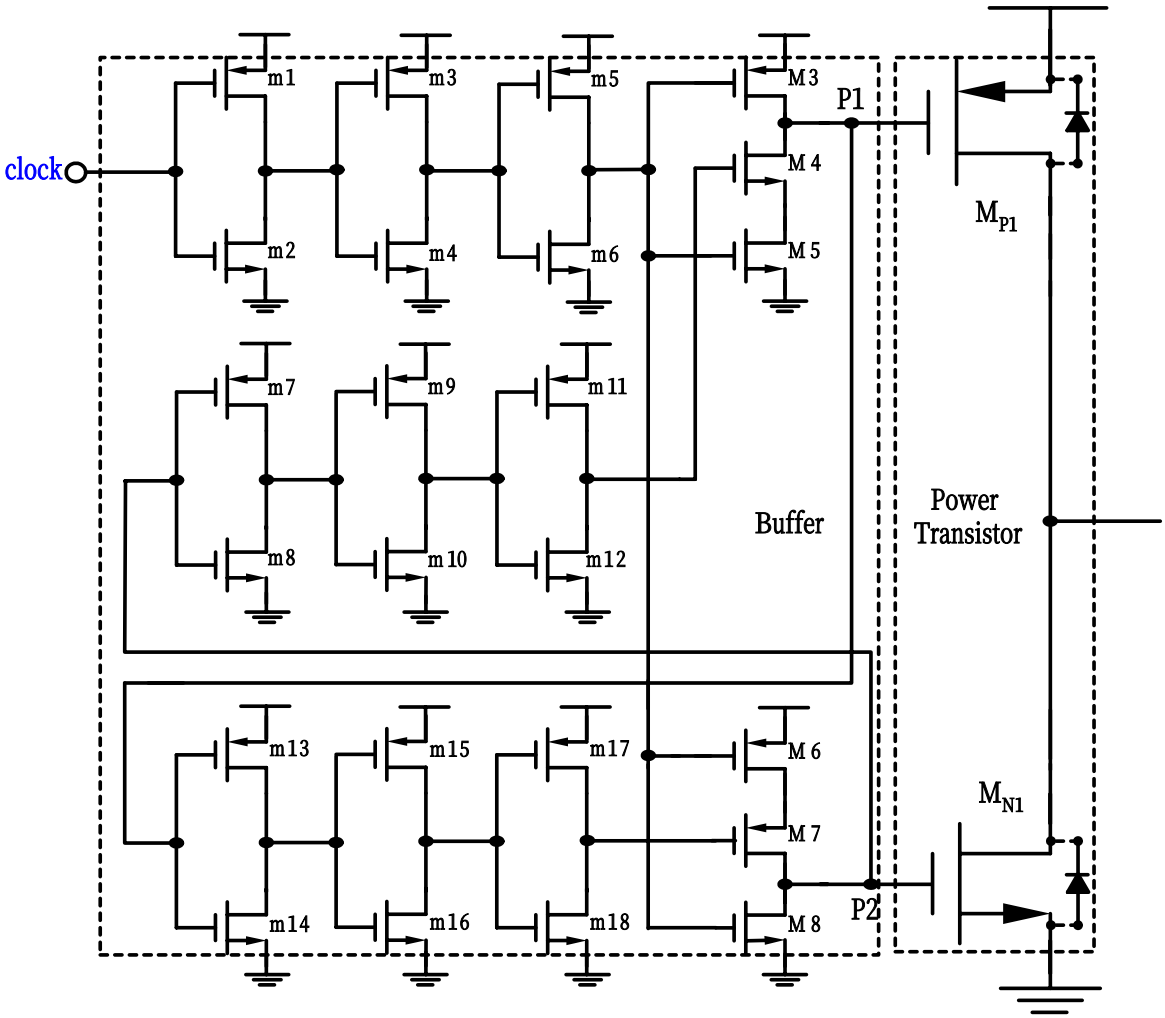


Fig. 4.20 The circuit of buffer

This buffer shown in Fig.4.20 refers to [18]. The basic operation principle of this buffer is to confirm that one power transistor turns on after the other power transistor turns off by

using the feedback signal at P1, P2 and the special inverter with the control stage. Therefore, the power transistors do not turn on simultaneously and then the shoot-through current is not caused in any condition.

In my design, I propose an improvement about dead-time. When the power transistor M_{P1} turns off gradually, the body diode of power transistor M_{N1} will turn on to supply some current to inductor because in this time the M_{P1} does not provide enough current to inductor. Until the M_{P1} turns off completely, the feedback signal at P1 of buffer just tells the M_{N1} to ready to turn on. In this short duration, the body diode of the M_{N1} will play an important role to supply current. Because for the same current, the power loss of body diode is larger than the designed M_{N1}, the less this time of body diode conducting will make power dissipation smaller. This buffer with an improvement is shown in Fig.4.21.

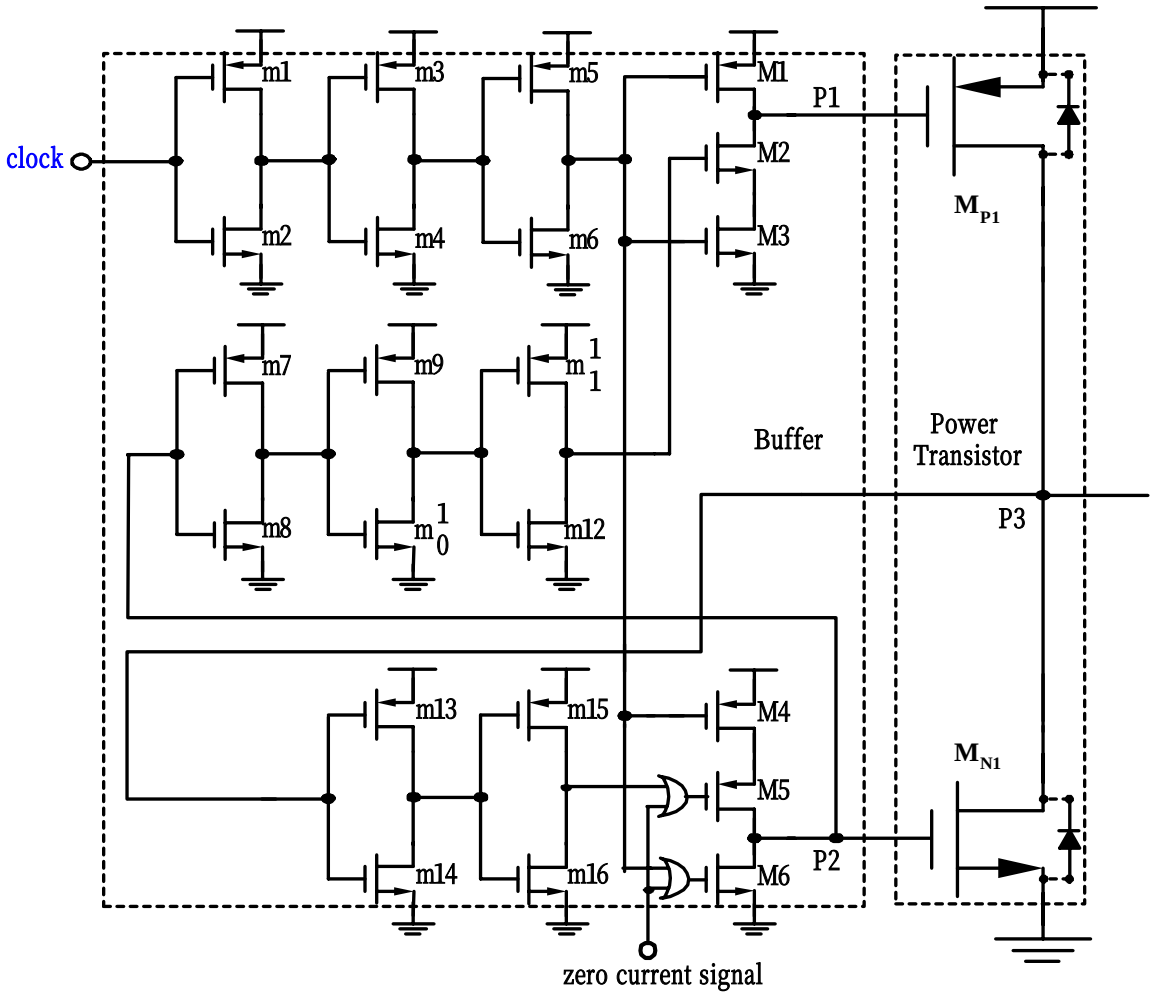


Fig. 4.21 The circuit of buffer with an improvement

The main difference of Fig.4.20 and Fig.4.21 is the feedback circuit. The original path of the feedback signal at P1 is replaced by P3. This new feedback path tells the M_{N1} to ready

to turn on when the body diode turns on. By this way it will make M_{N1} turn on timely to reduce the time of body diode conducting. Therefore, it can gain the effect of power-saving. Moreover, the DCM control is added by the signal 'zero current signal'. When "zero current signal" is low level, the regulator operates in CCM and the buffer works normally. When "zero current signal" is high level, the buffer will turn off both power transistors of M_{N1} and M_{P1} to prevent reverse current and make the regulator operate in DCM properly.

4.9 Current Sensor Circuit [20]

In regulators with current mode control, it must obtain the information of the inductor current signal to compare with control signal V_c in Fig.4.1 to decide desired duty cycle. Therefore, a current sensor is essential for sensing inductor current signal in current mode regulators. In my design, a CMOS on-chip current scheme is used shown in Fig.4.22

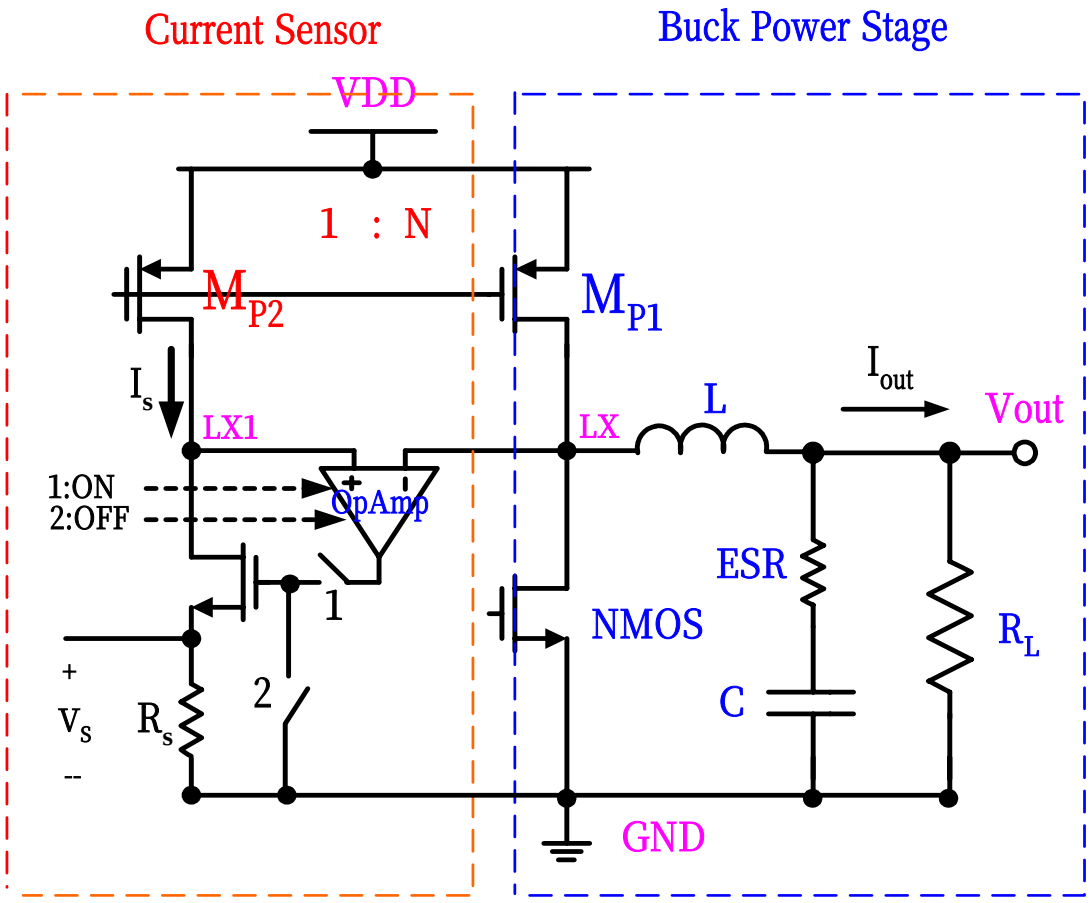


Fig. 4.22 The circuit of current sensor

Form section 4.6, we can know that I only need the initial inductor current signal. There are two states "sensing" and "sleeping" in a period. In state 1 "sensing", this circuit senses

the initial current signal and sends this signal to the artificial signal circuit. In state 2 "sleeping", this circuit turns off all components and sleeps to wait for next state 1. By this way, the power dissipation of this current sensor will be enormously lowered due to the short working time. The power losses of general and my condition are explained mathematically as follows.

Assume Period= 2us, D = 0.2 ~ 0.9, I_{Load} = 10mA~500mA, Current of OpAmp $\approx$ 600uA (for high speed and high slew rate application), R_s=1kΩ, M_{P2}= (1/1000)*M_{P1}.

1. General condition: the current sensor works in the duration of M_{P1} conducting.

In a period (=2us):

$$\text{Max power dissipation:} \approx \frac{0.9}{1} \times [(\frac{500\text{mA}}{1000})^2 \times 1\text{K}\Omega + 600\text{uA} \times 3.3\text{V}] \approx 2.01 \times 10^{-3} \text{ (W)}$$

$$\text{Min power dissipation: } \approx \frac{0.2}{1} \times [(\frac{10\text{mA}}{1000})^2 \times 1\text{K}\Omega + 600\text{uA} \times 3.3\text{V}] \approx 3.96 \times 10^{-4} \text{ (W)}$$

$$\text{Average power dissipation: } \approx \frac{\text{Max} + \text{Min}}{2} \approx 1.2 \times 10^{-3} \text{ (W)} \qquad \text{(4-14)}$$

2. My condition: the current sensor works in initial short period ($\approx$ 50ns).

In a period (=2us):

$$\text{Max power dissipation: } \approx \frac{50\text{ns}}{2\text{us}} \times [(\frac{500\text{mA}}{1000})^2 \times 1\text{K}\Omega + 600\text{uA} \times 3.3\text{V}] \approx 5.58 \times 10^{-5} \text{ (W)}$$

$$\text{Min power dissipation: } \approx \frac{50\text{ns}}{2\text{us}} \times [(\frac{10\text{mA}}{1000})^2 \times 1\text{K}\Omega + 600\text{uA} \times 3.3\text{V}] \approx 4.95 \times 10^{-5} \text{ (W)}$$

$$\text{Average power dissipation: } \approx \frac{\text{Max} + \text{Min}}{2} \approx 5.27 \times 10^{-5} \text{ (W)} \qquad \text{(4-15)}$$

From above Eq.(4-14) and Eq.(4-15), we can know that the saving of power dissipation is approximately 22 times in my condition. Therefore, this shows that the power dissipation in the current sensor circuit almost can be ignored in whole system. This makes the power dissipation of the current mode regulator have smaller inferiority than the voltage mode regulator.

After the discussion of power dissipation, the operation of this current sensor circuit is described. The current sensor is realized by a matched transistor M_{P2} with the aspect ratio much smaller than that of the power transistor M_{P1} in the power stage. In order to achieve an accurate current sensor, an OpAmp is used to enforce the same voltage at node LX and

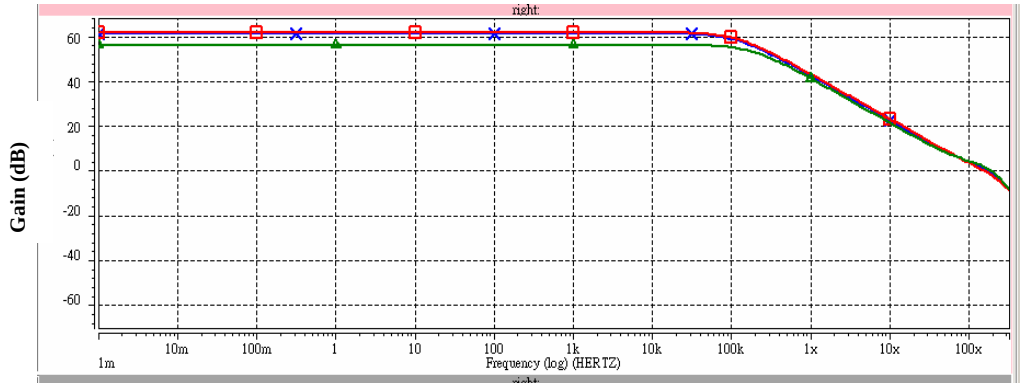
LX1. L and C are off-chip inductor and capacitor of the buck regulator.

In state 1 “sensing”, the OpAmp is turned on and the switch 1 is conducted. In this time, M_{P1} and M_{P2} turn on with Q tied to ground and the drain voltages of M_{P1} and M_{P2} are enforced to same voltage by the OpAmp to make two transistors operate in same condition. Therefore, the output current I_{Load}, which flows through the power transistor M_{P1}, is mirrored to the transistor M_{P2}. The current I_s on the transistor M_{P2} is designed smaller than and proportional to the current I_{Load} on the transistor M_{P1} by the size ratio of M_{P2} to M_{P1}, 1:1000 in my design. So the power dissipation in this scheme is much smaller than traditional one which uses a sensing resistor in series with the inductor or the power transistor. Finally, the sensing current I_s pass through the resistor R_s to produce the sensing signal V_s which will be used in artificial signal circuit. The sensing signal V_s is given by

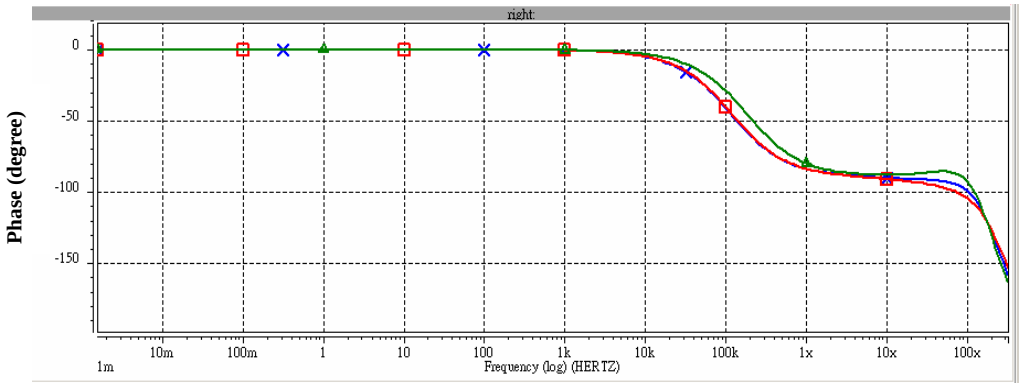
$$V_s = I_s \times R_s = \frac{I_{Load}}{1000} \times R_s \qquad (4\text{-}16)$$

The ratio of V_s to I_{Load} can be adjusted by the size ratio of M_{P2} to M_{P1} and R_s. After state 1 “sensing” finishes, the state 2 “sleeping” starts. In this state, the OpAmp and the switch 1 are turned off and the switch 2 is conducted to close the current I_s path. By this way, this current sensor circuit will operate in no-working state and not loss any power. Therefore, it is to gain the effect of power-saving.

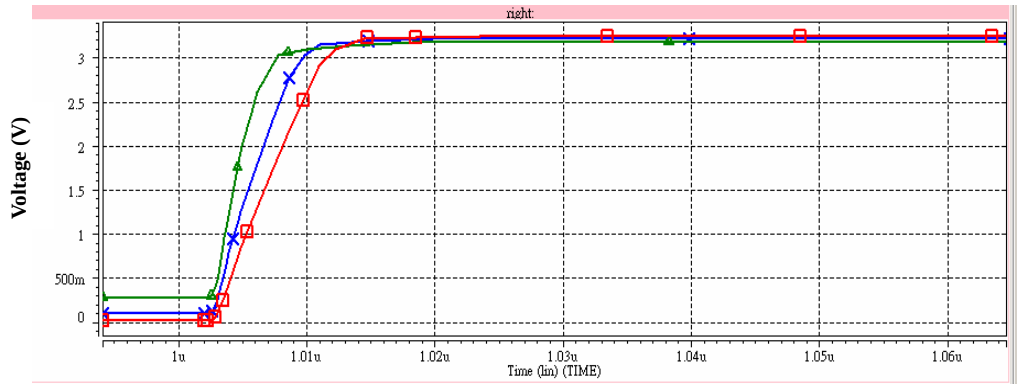
In this circuit, The OpAmp is an important role to produce the accurate current mirror. In order to achieve a good effect of the virtual short-circuit, the gain of this OpAmp is designed larger than 60 dB. And because the sampling time is smaller than 50 nao-second, it would be best to has the slew rate larger than 3.3V/ (1/2*50ns). The gain, phase and slew-rate of this OpAmp are shown in Fig.4.23 and arranged in Table.4.4.



(a) Gain



(b)Phase



(c)Slew-Rate

Fig.4.23 The OpAmp (a) Gain (b) Phase (c) Slew-Rate

Table.4.4 The frequency characteristics of the operational amplifier (OpAmp)

Corner/Temperature	FF/25 ° C	SS/125 ° C	TT/55 ° C
Waveform symbol	□	Δ	X
Dc gain	61.8dB	56.3dB	61.4dB
Unity-gain frequency ω_t	158MHz	185MHz	175MHz
Phase margin in ω_t	64 ° C	55 ° C	60 ° C
Slew-Rate (V/us)	334	610	432

The simulation results conform to my requirement except SS/125 ° C corner. Al though the gain and phase margin in SS/125 ° C are little not enough, these can be tolerated in my system.

4.10 Zero Current Detector Circuit [20]

In order to save power, a NMOS transistor with a small on-resistance is used instead of the diode in my design. The regulator with the diode has no reverse current from the output capacitor through the diode to ground in light load mode because the diode belongs to the single-direction switch element which only permits single-direction current to pass. But if we use the NMOS transistor instead of the diode as the switch element, this advantage will be lost because the transistor belongs to the bi-direction switch element and the reverse current from the capacitor through the NMOS transistor to ground will cause an extra power loss. In order to make the switch characteristic of the transistor be like to the diode, a zero current detector is used as shown in Fig.4.24 to avoid the reverse current.

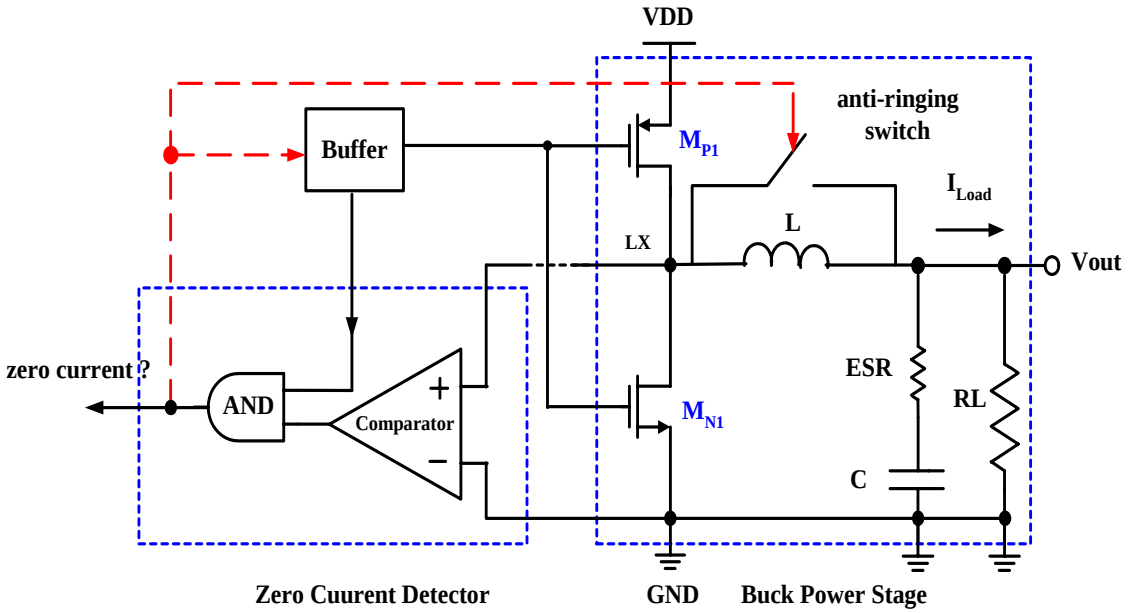


Fig.4.24 The circuit of the zero current detector

As illustrated in Fig.4.24, when the reverse current appears, this current from the output capacitor through the power transistor M_{N1} will make the drain voltage to the source voltage V_{DS} of the power transistor M_{N1} become positive voltage. The main operation principle is to obtain the time of the zero current by detecting whether the voltage V_{DS} of the power NMOS M_{N1} becomes positive or not. This circuit is composed of a comparator circuit and a AND gate. The comparator is responsible for the comparison of drain voltage and source voltage of the power transistor M_{N1}. The AND gate decides when this comparison is valid. (It is designed that it is valid in the duration of M_{N1} conducting). Further, an anti-ringing switch [20] is used. When the zero current signal is high, the buffer

will turn off all power transistors. The inductor L and the output capacitor C then form an oscillatory circuit. Large ringing occurs at node LX, causing large switching noise and EMI. In order to avoid this phenomenon, an anti-ringing switch is incorporated with the present design. When all power transistors are off, the anti-ringing switch will conduct to short the inductor L. By this way, the oscillation loop will be broke and the oscillation happened in the node LX will not occur.

4.11 Simulation Results

This section describes some critical simulation results of the designed current mode buck regulator with adjusted-sloop compensation ramp. From this simulation results, the functions and specifications of the designed regulator can be verified mostly. Some parasitic components are also included into the whole system to make this simulation more realistic and believable. The simulation results are as follows.

1. The comparison of the system without and with soft start

>> V_{in} =3.3V, V_{out}=3V, I_L=500mA

>> The first picture: the output voltage V_{out}

>> The second picture: the inductor current I_L

A. without soft start :

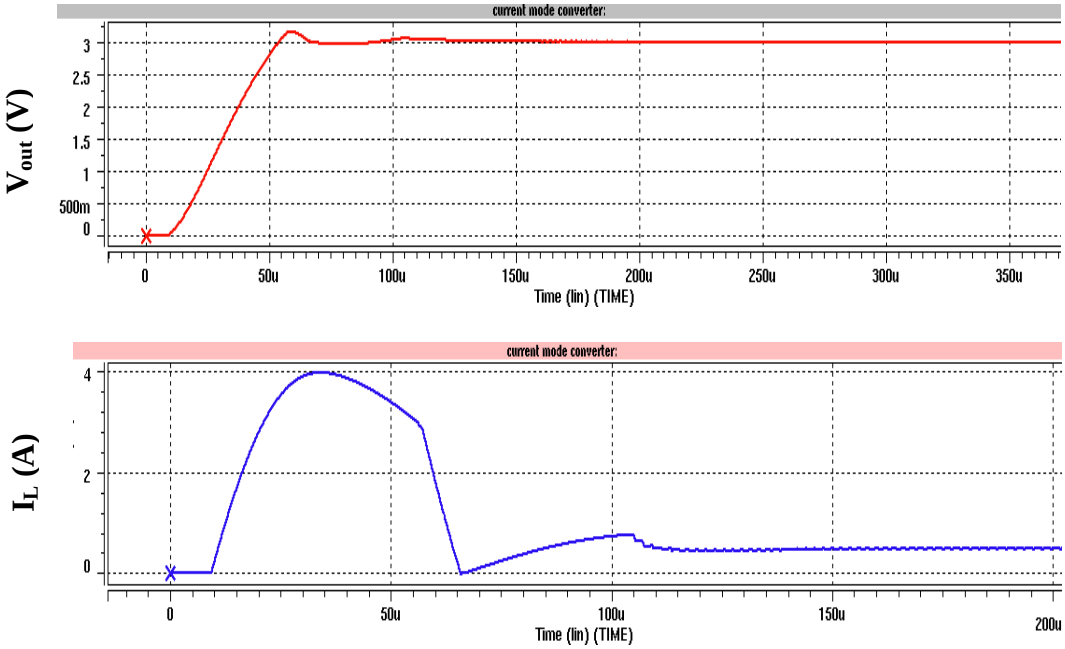


Fig.4.25 The system without the soft start

B. with soft start :

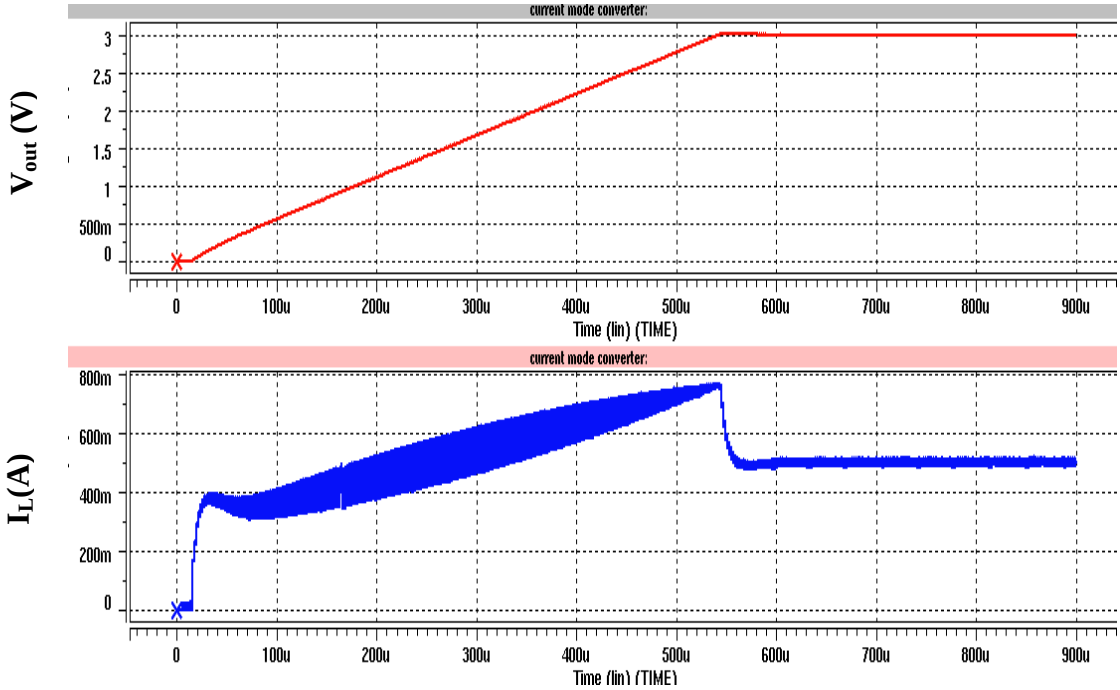


Fig.4.26 The system with the soft start

The system without soft start will have an enormous current to 4A in startup as shown in Fig.4.25. This enormous current possibly causes the damages of the inner components and EMI problem. Therefore, a soft start circuit is incorporated into the whole system shown in Fig.4.26. The charging current in Fig.4.26 is not so exaggerated like that in Fig.4.25 in startup. Although this condition in Fig.4.26 will make startup time become longer than in Fig.4.25, the damages of the inner components and EMI problem can be effectively avoided.

2. The comparison of the system without and with zero current detector

>> V_{in} =3.3V, V_{out}=1.8V, I_L=10mA

>> The first picture: the output voltage V_{out}

>> The second picture: the inductor current I_L

A. without zero current detector

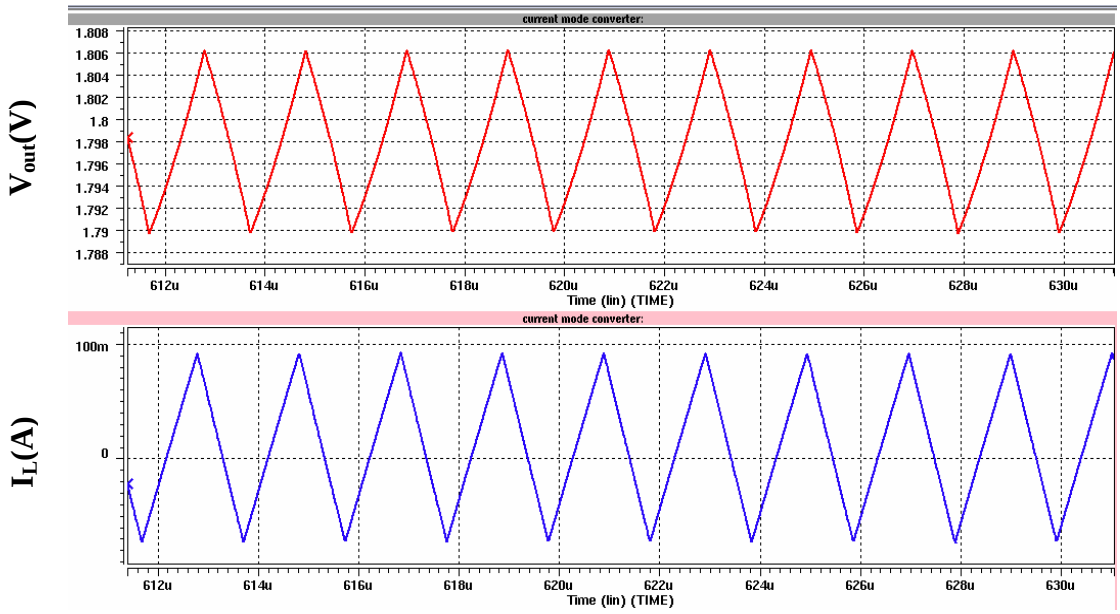


Fig.4.27 The system without the zero current detector

B. without zero current detector

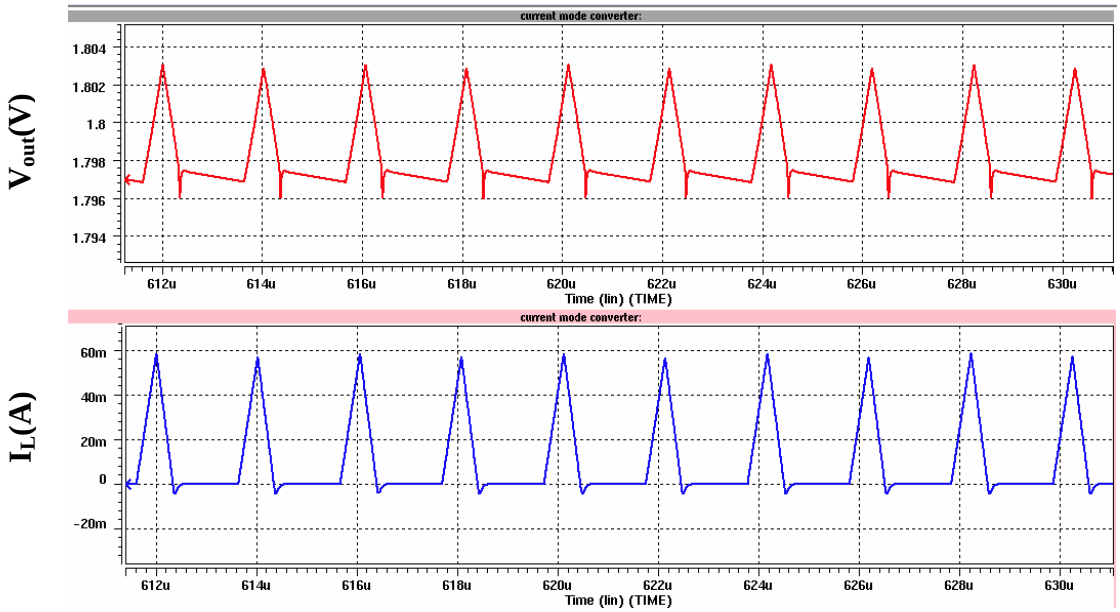


Fig.4.28 The system with the zero current detector

The system without the zero current detector will have an inverse inductor current through power transistor NMOS to ground as shown in Fig.4.27. This inverse current will cause an extra power loss. Therefore, in order to save power, a zero current detector is incorporated into the whole system to sense when the zero current happens and to block the inverse current. As shown in Fig.4.28, with the zero current detector, the inverse current is

effectively blocked and it can obtain an extra advantage of smaller output voltage ripple.

3. The comparison of the system without and with anti-ringing switch

>> V_{in} =3.3V, V_{out}=1.8V, I_L=10mA

>> The first picture: the output voltage V_{out}

>> The second picture: the connection point of two power transistors lx

A. without anti-ringing switch

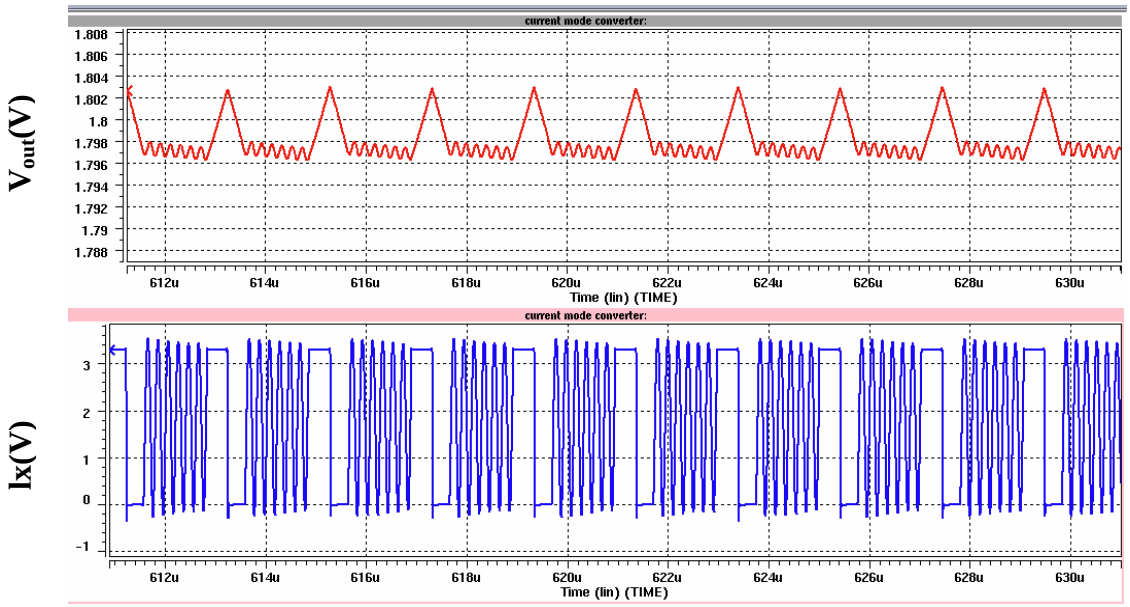


Fig.4.29 The system without the anti-ringing switch

B. with anti-ringing switch

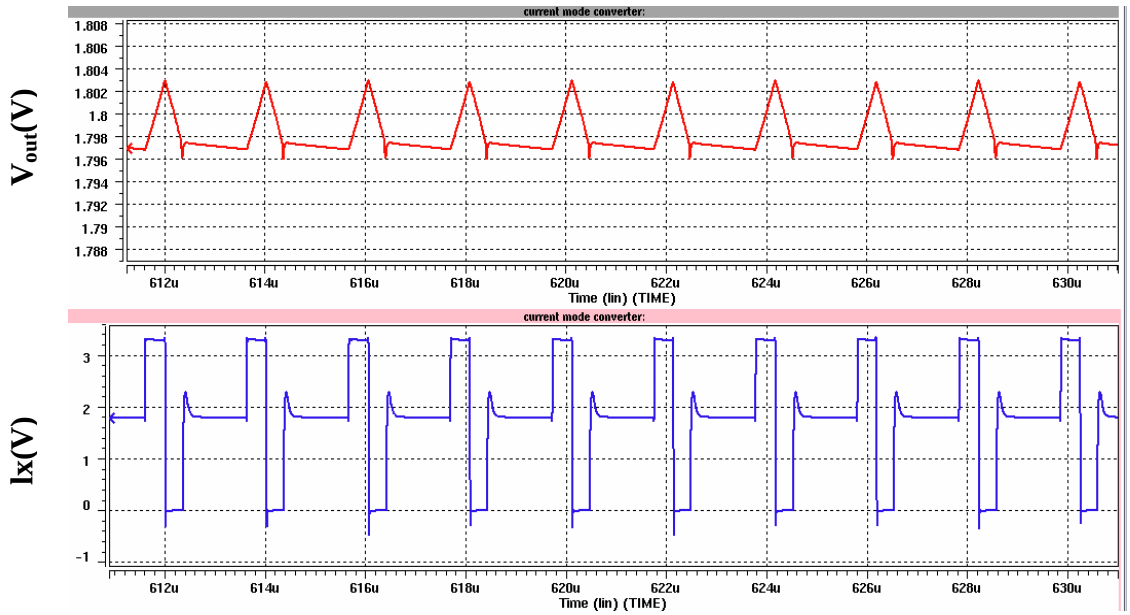


Fig.4.30 The system with the anti-ringing switch

If the system has no the anti-ringing switch, the output capacitor and the filter inductor will constitute an oscillatory circuit in DCM. This will cause the ringing in the connection point of two power transistors ‘lx’ as shown in Fig.4.29. Although this phenomenon do not influence on the operation of the system, it causes the serious EMI problem. Therefore, an anti-ringing switch must be used in order to avoid this problem. As shown in Fig.4.30, the system with the anti-ringing switch will not have the ringing in DCM.

4. The Max. output voltage 3V

A. (TT-55 ˚ C)

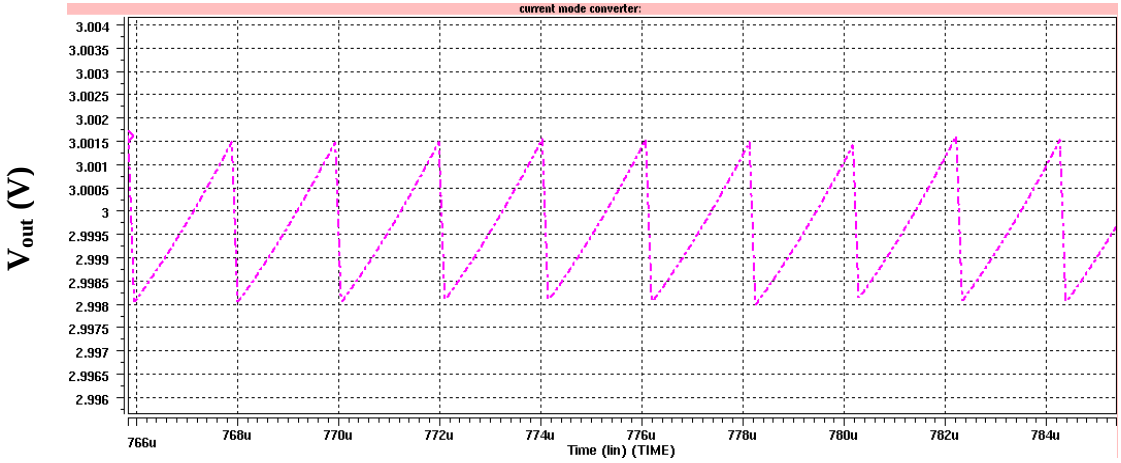


Fig.4.31 The Max. output voltage in TT corner at 55 ˚ C

B. (FF-25 ˚ C)

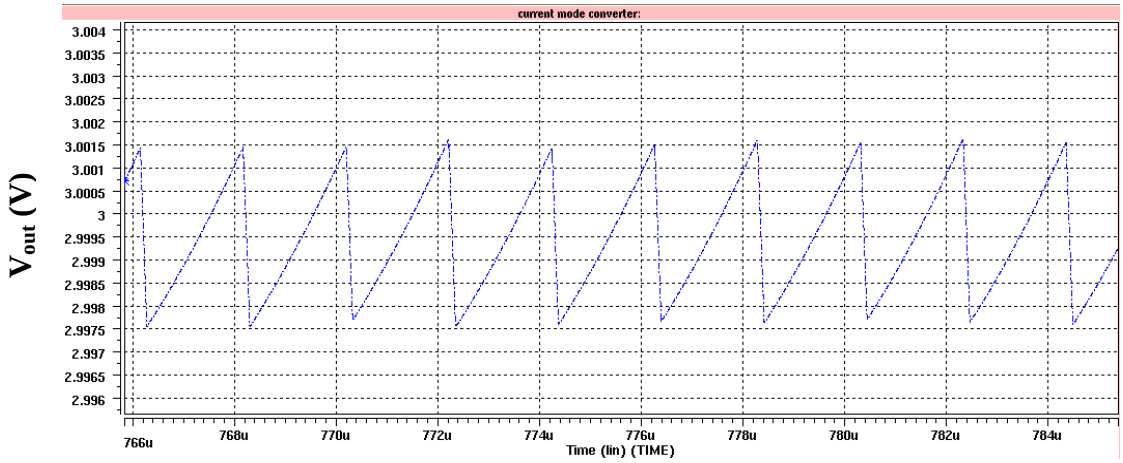


Fig.4.32 The Max output voltage in FF corner at 25 ˚ C

C. (SS-125 ˚ C)

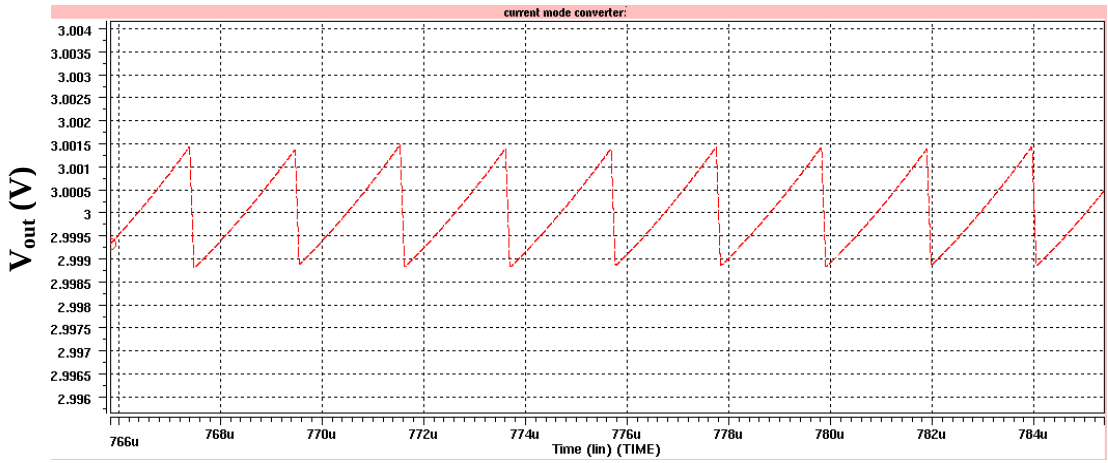


Fig.4.33 The Max. output voltage in SS corner at 125 ˚ C

Table.4.5 The arrangement of the Max output voltage

Figure	output voltage	Output voltage ripple (peak to peak)
Fig.4.31 (TT-55 ˚ C)	≈3V	≈ 3.5mV
Fig.4.32 (FF-55 ˚ C)	≈3V	≈ 4mV
Fig.4.33 (SS-125 ˚ C)	≈3V	≈ 2.5mV

Fig.4.31, 4.32, and 4.33 are the simulation results of the Max. output voltage. Some specification is arranged shown in Table.4.5.

5. The Min. output voltage 424mV

A. (TT-55 ˚ C)

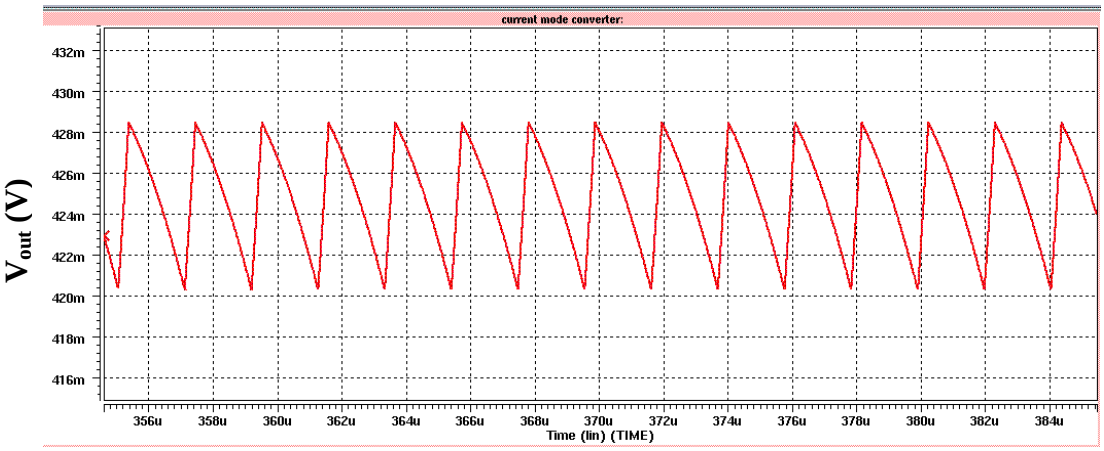


Fig.4.34 The Min. output voltage in TT corner at 55 ˚ C

B. (FF-25 ˚ C)

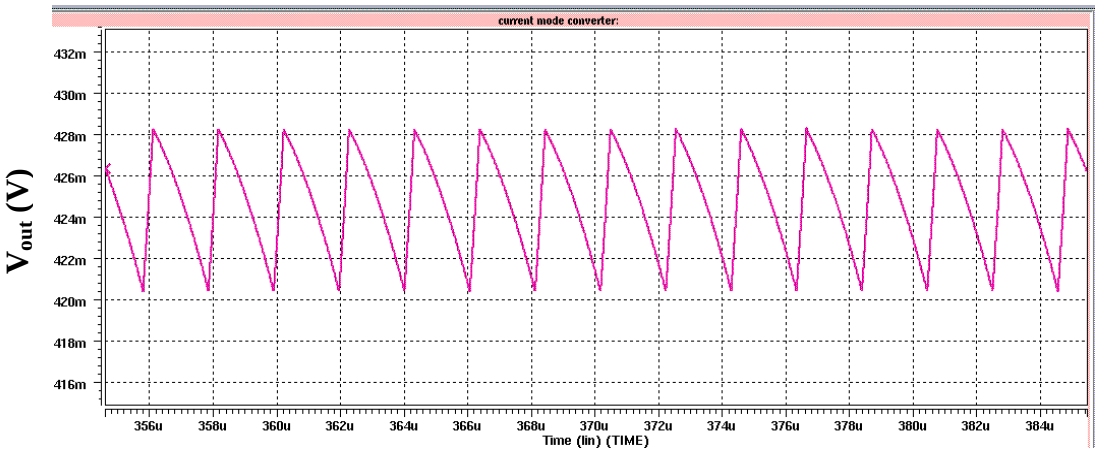


Fig.4.35 The Min. output voltage in FF corner at 25 ˚ C

C. (SS-125 ˚ C)

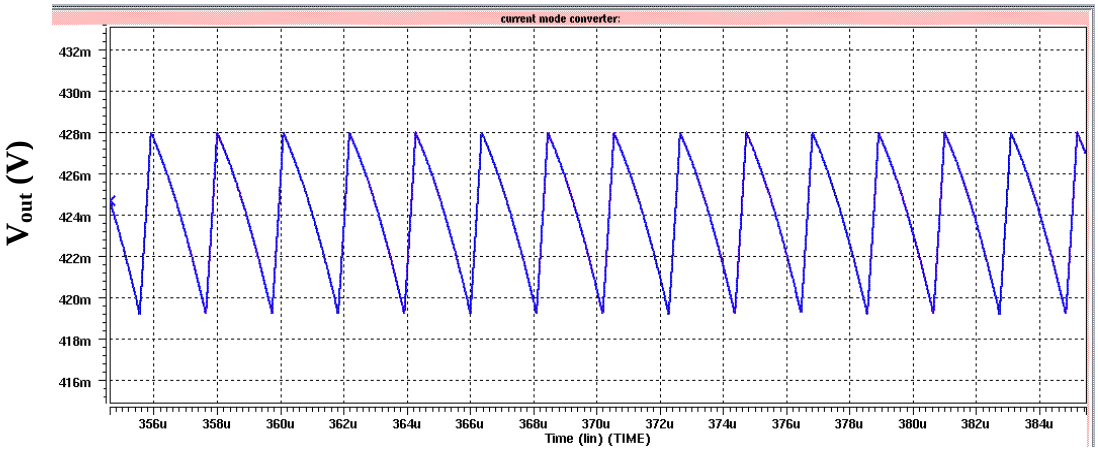


Fig.4.36 The Min. output voltage in SS corner at 125 ˚ C

Table.4.6 The arrangement of the Min output voltage

Figure	output voltage	Output voltage ripple (peak to peak)
Fig.4.34 (TT-55 ˚ C)	≈424mV	≈ 8mV
Fig.4.35 (FF-55 ˚ C)	≈424mV	≈ 8mV
Fig.4.36 (SS-125 ˚ C)	≈424mV	≈ 9mV

Fig.4.34, 4.35, and 4.36 are the simulation results of the Min. output voltage. Some specification is arranged shown in Table.4.5.

6. Transient Response(V_{in} =3.3V, V_{out}=1.8V, I_{Load}= 100mA→600mA→100mA)

>> The first picture: the output voltage V_{out}

>> The second picture: the inductor current I_L and the load current I_{Load}

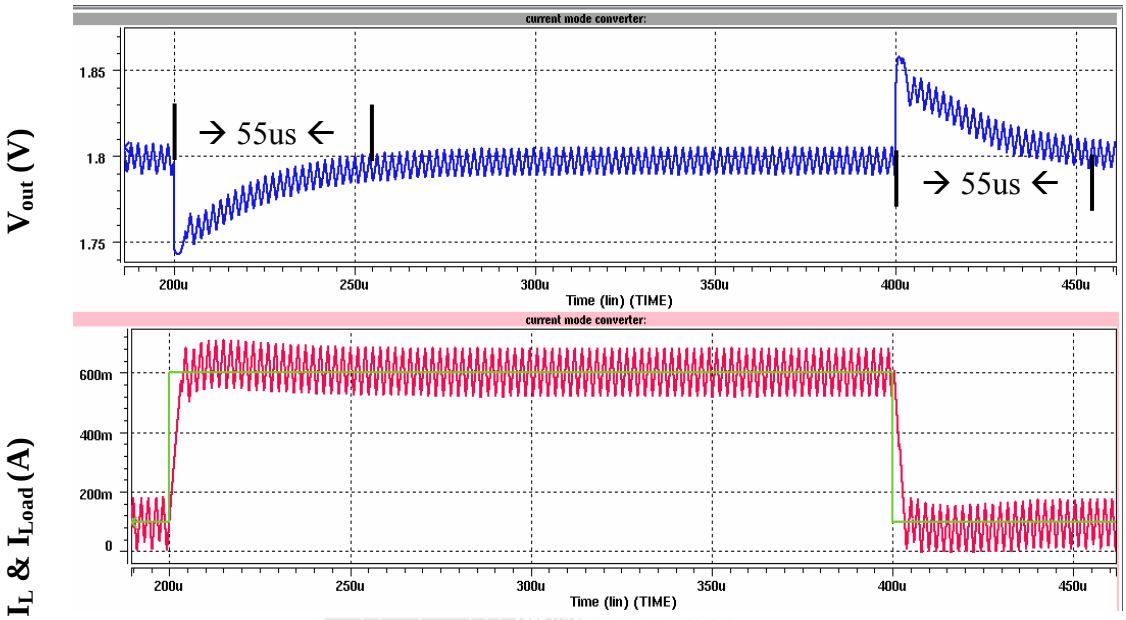


Fig.4.37 The Transient Response in V_{in}=3.3V and V_{out}=1.8V

Fig.4.37 shows that the variation of the output voltage when the load current varies form 100mA to 600mA and from 600mA to 100mA. The maximum deviation voltage in output voltage is approximately 60mV and the recovery time which is the duration from the maximum deviation to 99.9% nominal voltage is approximately 55 micro seconds.

7. Comparison of adjusted-slope and constant-slope compensation ramp

Two differences are shown in Table4.7. I will do some comparison of two schemes by implementing two circuits as in Table.4.7.

Table.4.7 The difference of the adjusted-slope and the constant-slope

Scheme	(dif. 1) Artificial Signal Block	(dif. 2) The sensing time of Current Sensor
Adjusted-slope	My design	Initial
Constant-slope	V-I converter Ramp generator	The up-slope state of the inductor current

7.1 Transient Response (Load current 100mA→ 600mA)

>> The first picture: the inductor current I_L and the load current I_{Load}

>> The second picture: the output voltage V_{out}

A. (V_{out} =1.8V)

>> Δ: adjusted-slope (compensation slope = $V_{out}/L = 1.8*10^{-5}$)

>> □: constant-slope (compensation slope = Max. $V_{out}/L = 3*10^{-5}$)

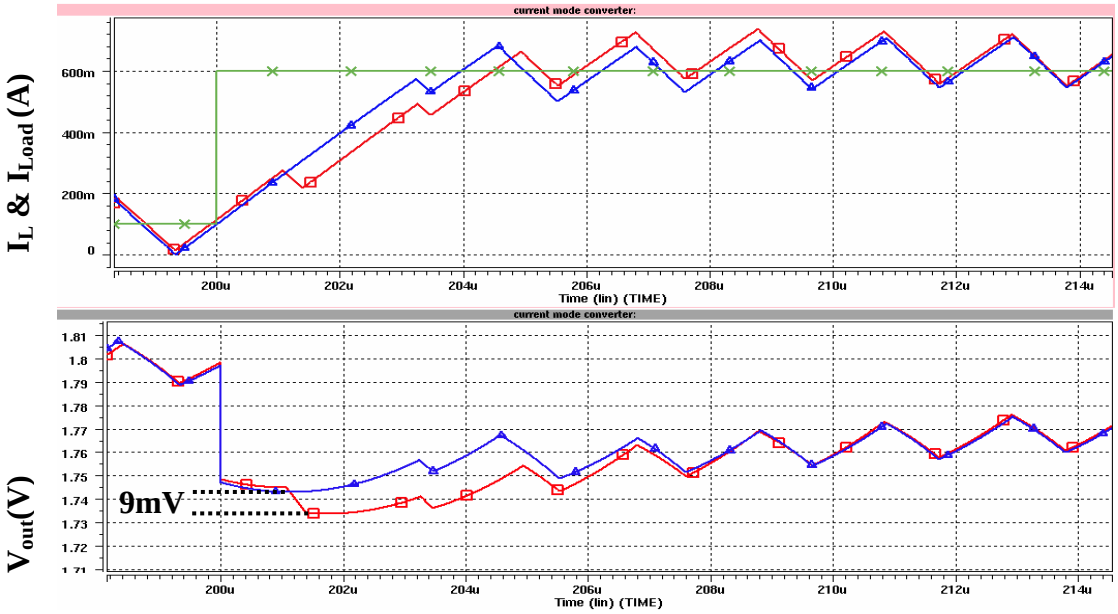


Fig.4.38 The comparison of transient response in V_{out}=1.8V

B. (V_{out} =424mV)

>> Δ: adjusted-slope (compensation slope = $V_{out}/L = 0.424*10^{-5}$)

>> □: constant-slope (compensation slope = Max. $V_{out}/L = 3*10^{-5}$)

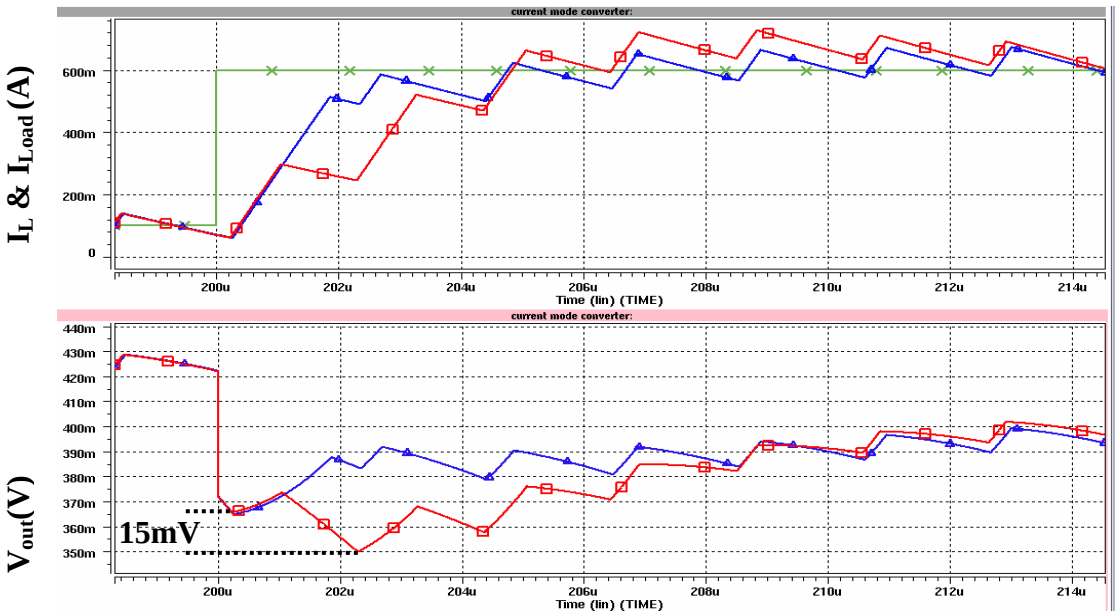


Fig.4.39 The comparison of transient response in V_{out}=424mV

When the output voltage is equal to 3V, the slope of compensation ramp is the same in two conditions, so the variations of the output voltage and the inductor current are also the same. When the output voltage is equal to 1.8V, the slope of the compensation ramp in adjusted-slope scheme is smaller than that in constant-slope scheme ($1.8*10^{-5} < 3*10^{-5}$). The transient response of the load current form 100mA to 600mA in V_{out}=1.8V is shown in Fig.4.38. Form Fig.4.38, we can know that the transient time of the inductor current is faster and this fast transient current makes the deviation of the output voltage smaller (~ 9mV) in adjusted-slope scheme than in constant-slope scheme. The same case in V_{out}=424mV is shown in Fig.4.39. Form Fig.4.39, we can know that this phenomenon is more obvious and it also reduce more deviation of the output voltage (~ 15mV).

7.2 Efficiency

>> V_{in}=3.3V V_{out}=1.8V

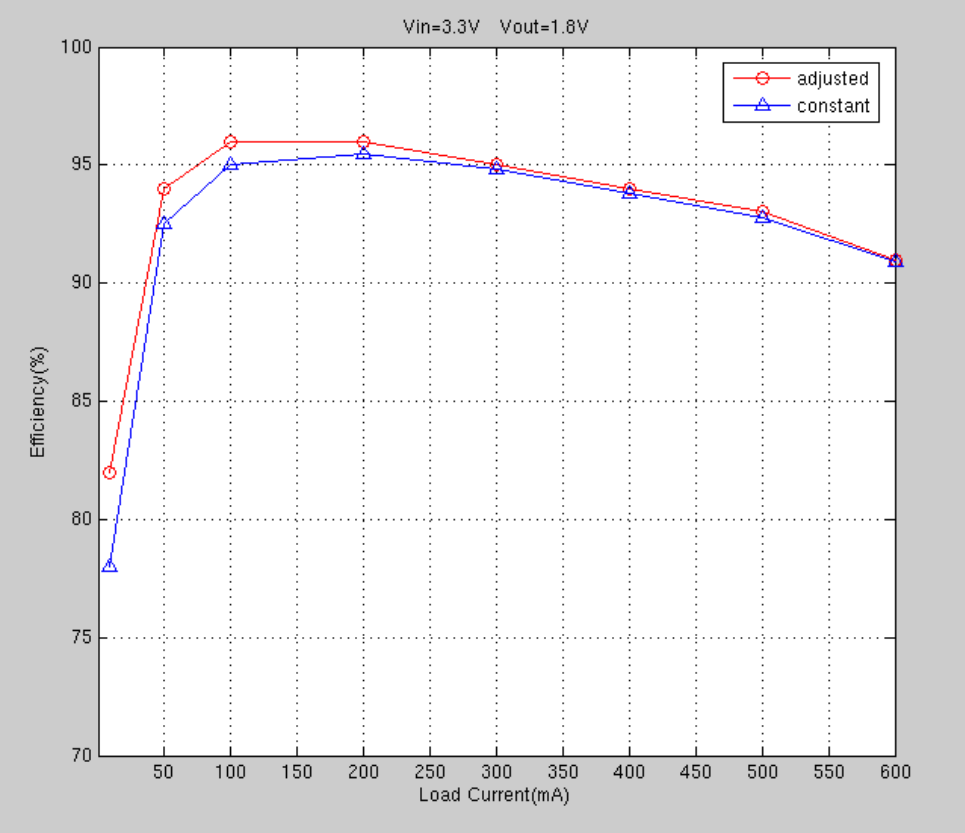


Fig.4.40 The comparison of the efficiency

Fig.4.40 shows the efficiency in two conditions. From Fig.4.40, we can know that the efficiency of adjusted-slope scheme is better than the constant-slope scheme. The main reason is possibly that the conducting duration of the current sensor is much shorter in

adjusted-slope scheme than in constant-slope scheme. .

8. Performance Summary in simulation

Table.4.8 The performance summary in simulation

Performance Summary	
Input Voltage	2.4V~3.6V
Output Voltage	0.424 V ~ 3V
Switching frequency	500kHz
Output Voltage Ripple	< 20mV
Load current	< 600mA
Recovery time	≈ 55us (100mA→600mA) or (600mA→100mA)
Line regulation	0.58% V/V (4.72mV/0.8V)
Load regulation	0.18% V/A (0.73mV/400mA)
Efficiency	Max 96% (at load 100mA)
Chip Area	1.27 x 1.16 (mm^2)

Chapter 5

Layout and Measurement

5.1 IC Layout

The layout arrangement of the floor plan is shown as Fig.5.1. The power transistors and the buffer are located at the upper side. The main feedback circuits are located at the lower side. The power transistors and the buffer belong to high noise components because the large amount of current in transient through them would generate high temperature and

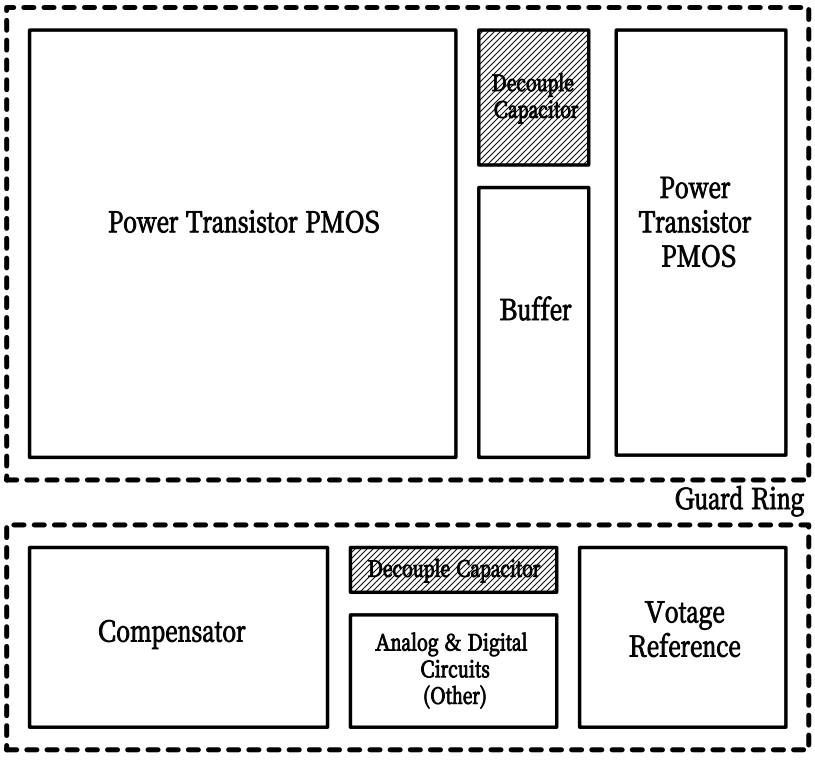


Fig.5.1 The floor plan of the switching regulator

serious noise. Therefore, in order to alleviate the influence on the feedback circuit, I use guard ring to surround these high noise components and lengthen the distance between the upper-side and the lower-side. The guard ring is also used in feedback circuits to achieve the better effect in blocking noise.

The layout photo is shown in Fig.5.2. The chip is fabricated by 0.35 μm 2P4M CMOS technology. The active area of the DAC is about 1×0.9 mm^2 and the total area is about 1.27×1.16 mm^2.

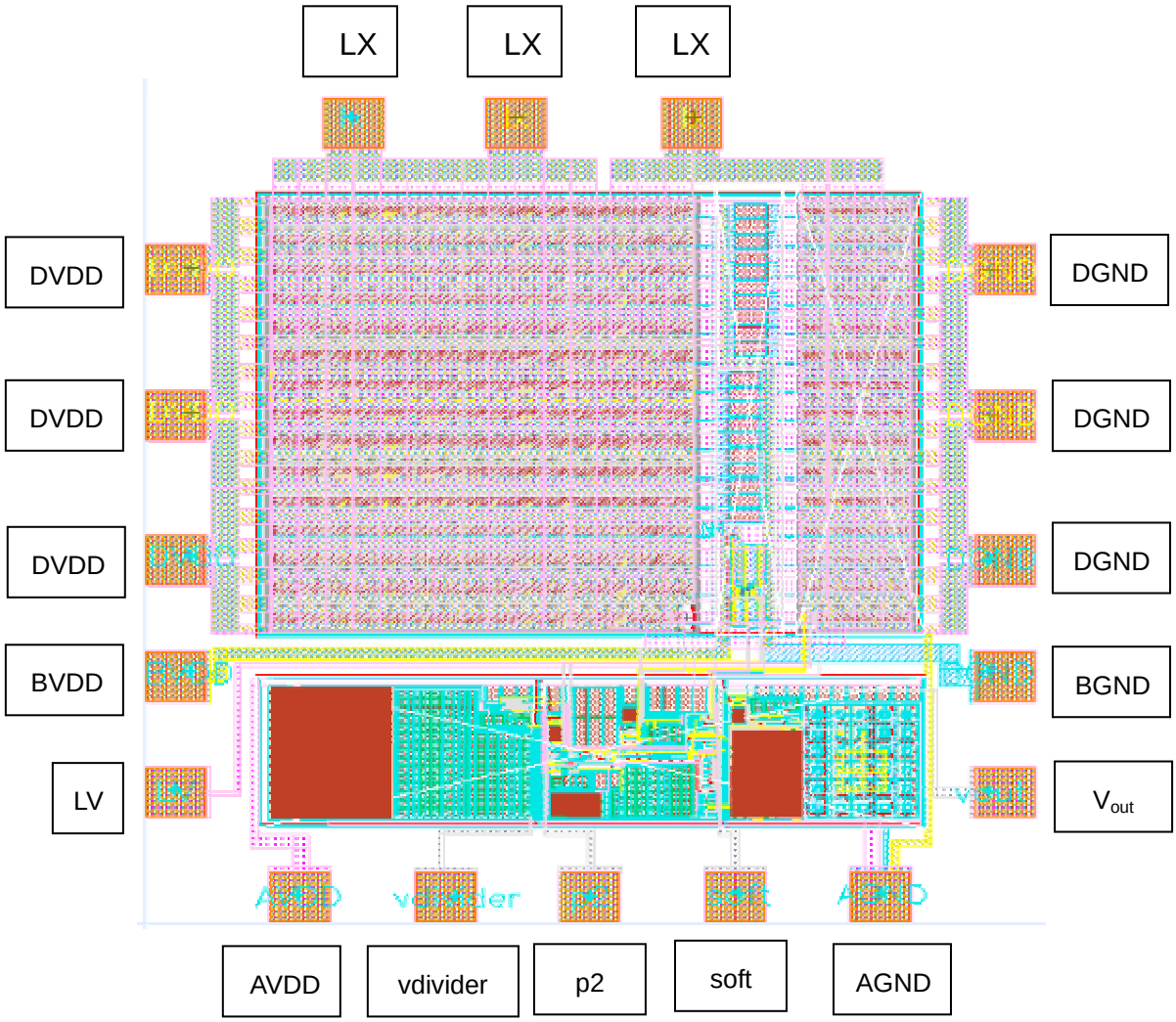


Fig.5.2 The layout photo of the switching regulator

5.2 Measurement Setup

Fig.5.3 shows the measurement setup of the overall switching regulator testing. Referring to Fig.5.3, the Angilent 66332A is used to provide the power supply of this chip. The Angilent N3301A and N3302A constitute the electronic load. This electronic load instrument is mainly regarded as the equivalent load of this switching regulator. It can change its impedance value statically and dynamically to measure the load regulation and the transient response. The voltage probe and the current probe belong to the Angilent 54846A oscilloscope and are used to measure the output voltage and the inductor current. As for some extra passive components, they are configured according to the requirement shown in Fig.5.3

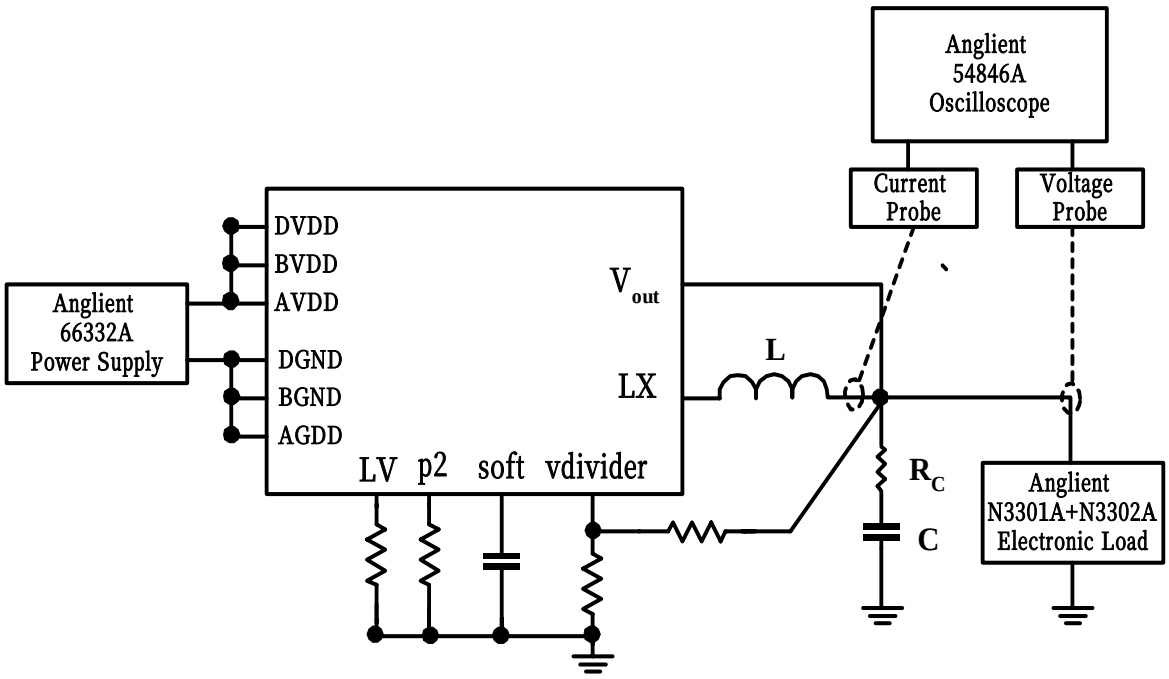
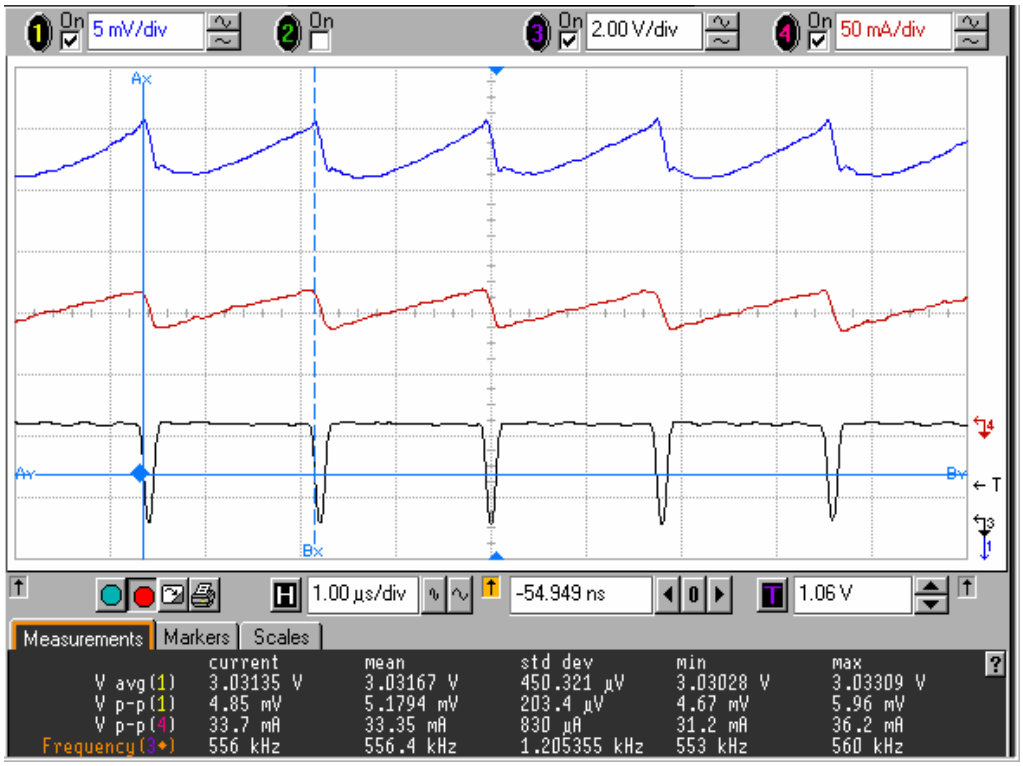


Fig.5.3 The measurement setup

5.3 Measurement Results

This section will describe some measurements such as static measurement, dynamic measurement and some performance etc. The measurement results are shown as follows.

1. The maximum output voltage 3V

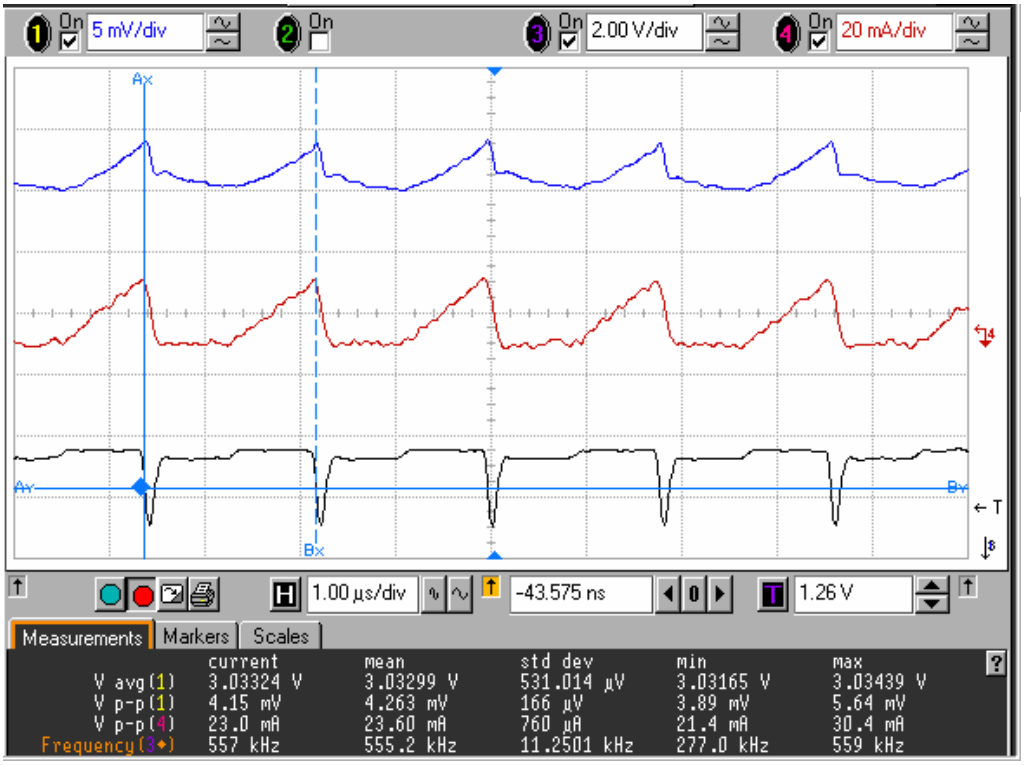


1 V_{out}

4 I_L

3 LX

(a)



1 V_{out}

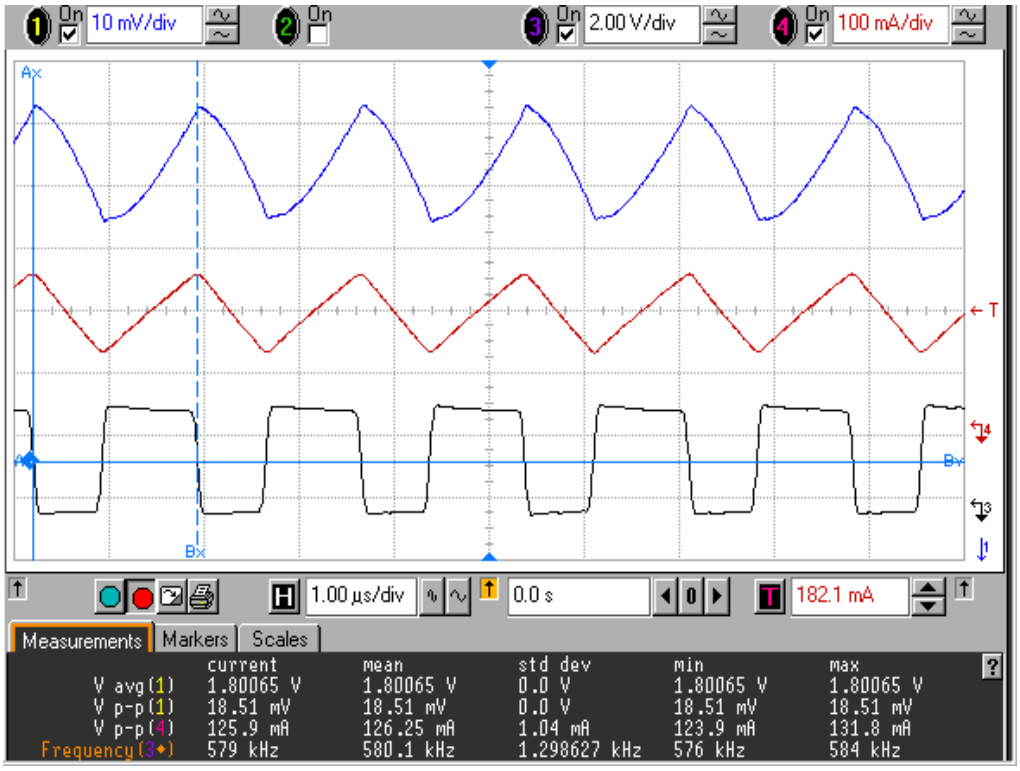
4 I_L

3 LX

(b)

Fig.5.4 V_{out}=3V @ V_{in}=3.3V (a) CCM (b) DCM

2. The medium output voltage 1.8V

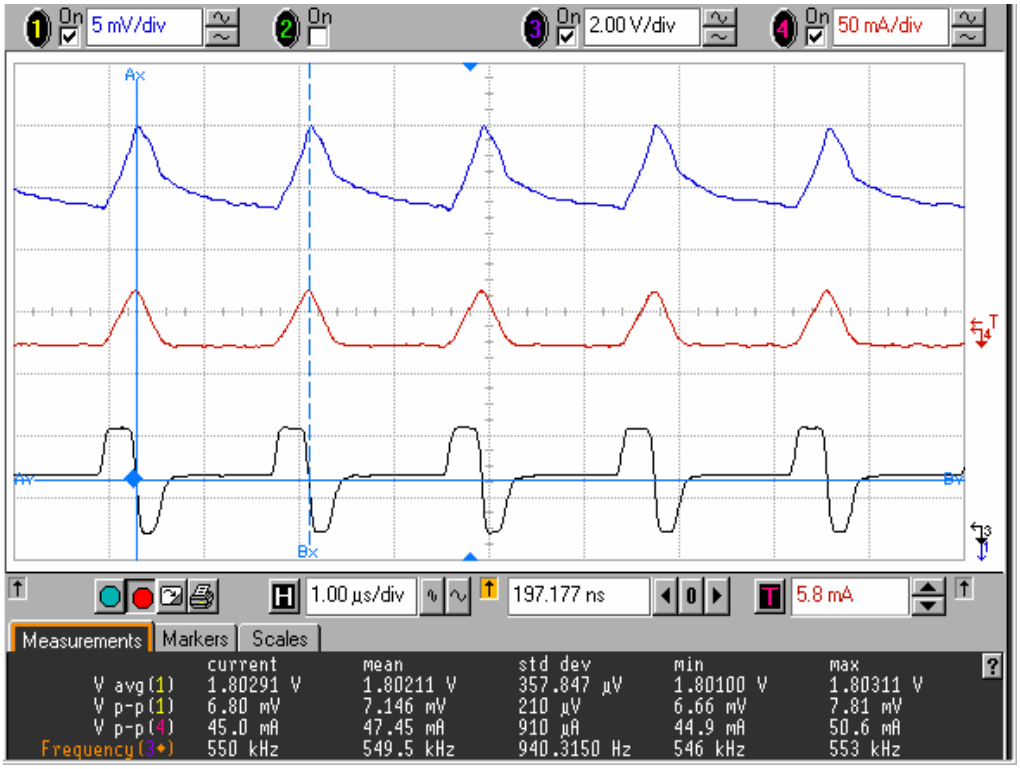


1 V_{out}

4 I_L

3 LX

(a)



1 V_{out}

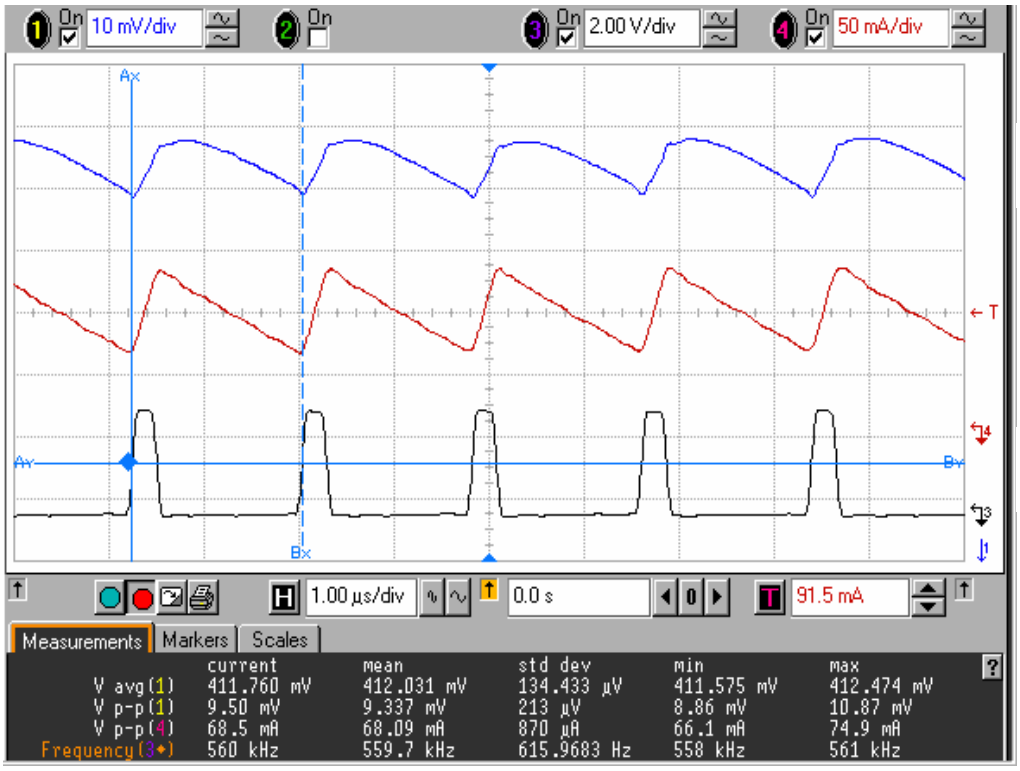
4 I_L

3 LX

(b)

Fig.5.5 V_{out}=1.8V @ V_{in}=3.3V (a) CCM (b) DCM

3. The minimum output voltage 412mV

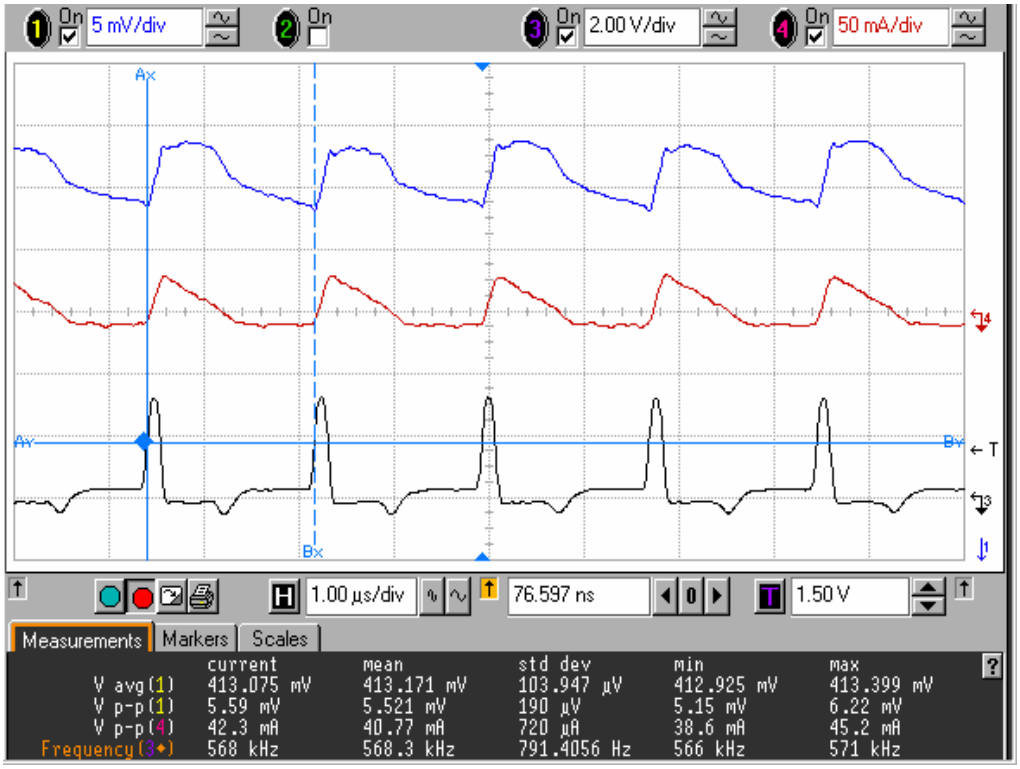


1 V_{out}

4 I_L

3 LX

(a)



1 V_{out}

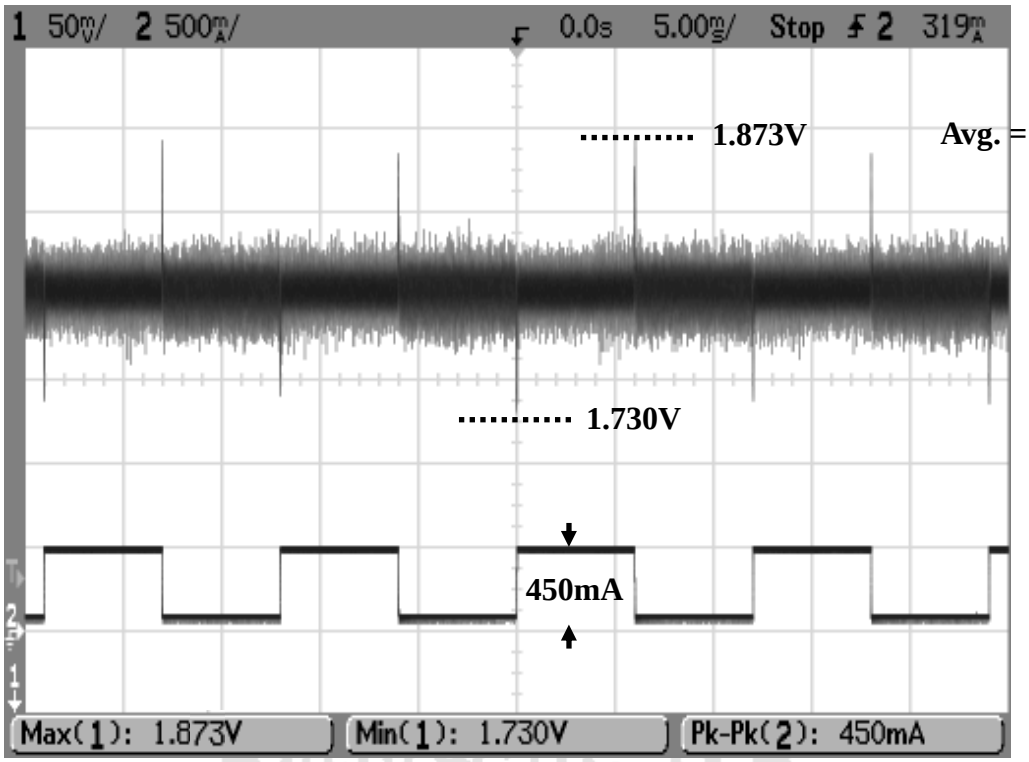
4 I_L

3 LX

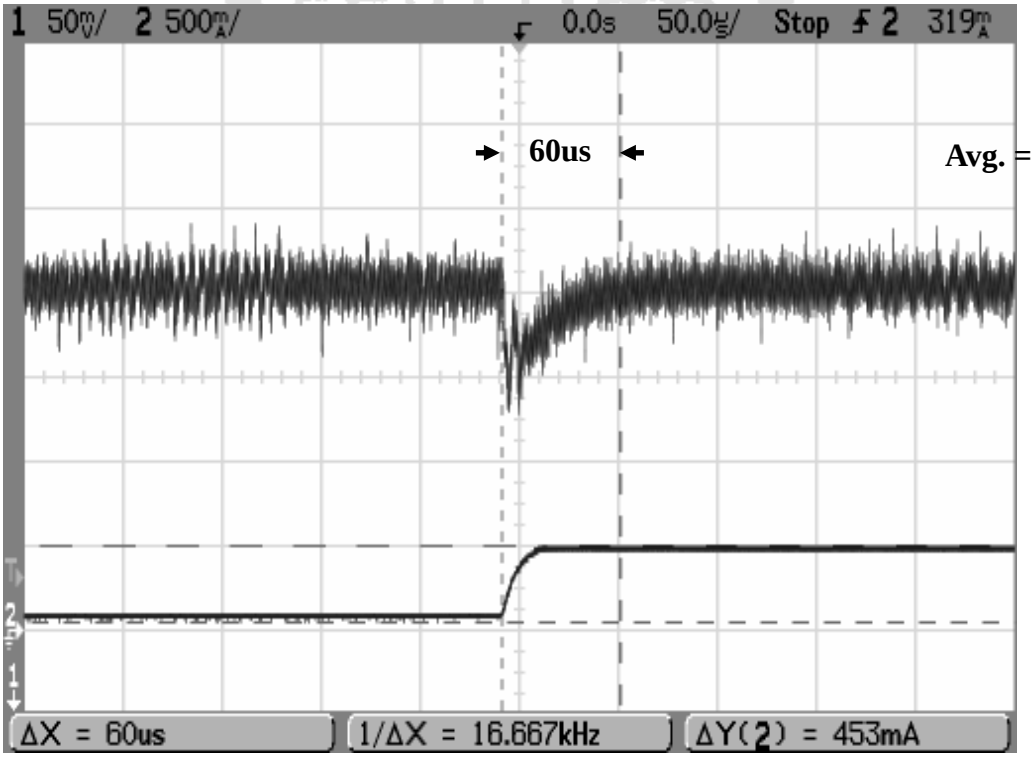
(b)

Fig.5.6 V_{out}=412mV @ V_{in}=3.3V (a) CCM (b) DCM

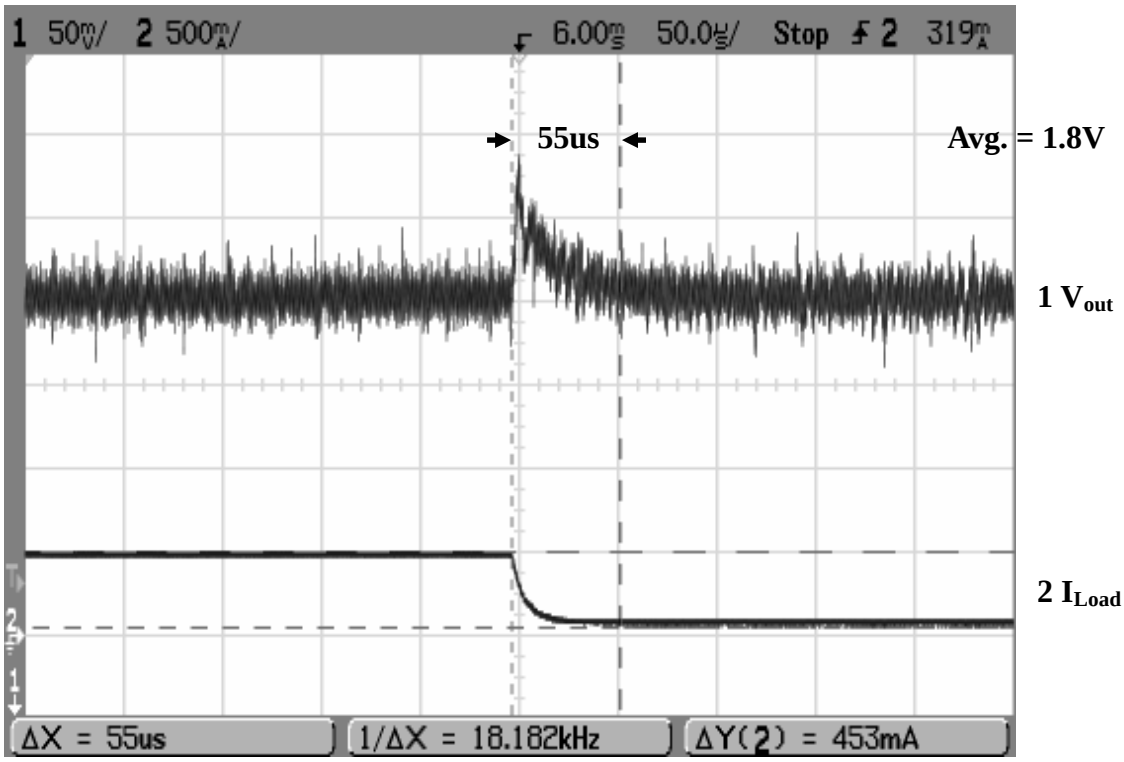
4. Transient Response (I_{Load} from 100mA → 550mA → 100mA @V_{out}=1.8V)



(a)



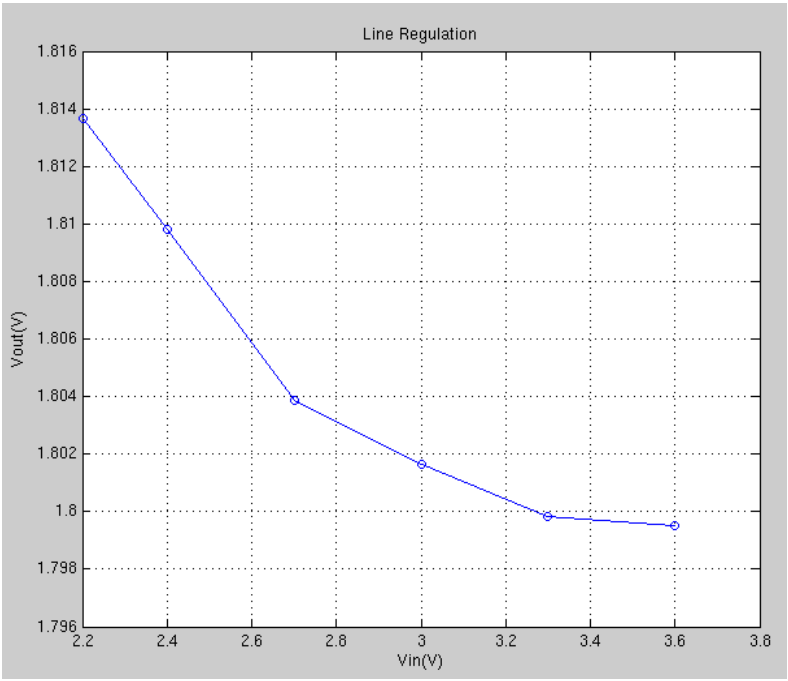
(b)



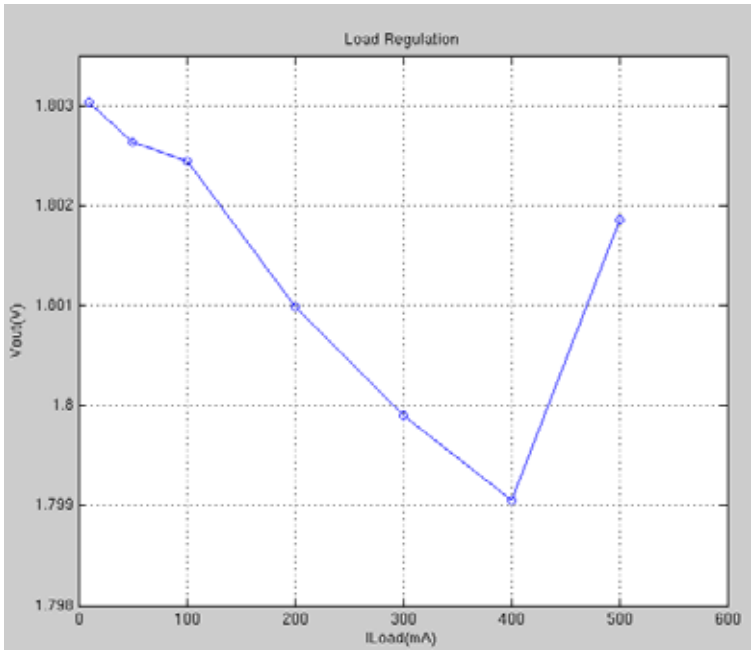
(c)

Fig.5.7 Transient response (a) global view: 100mA→550mA→100mA (b) local view: 100mA→550mA (c) local view: 550mA→100mA

5. Regulation



(a)



(b)

Fig.5.8 Regulation (a) Line Regulation @ I_{Load} = 300mA (b) Load Regulation @ Vin = 3.3V

6. Efficiency

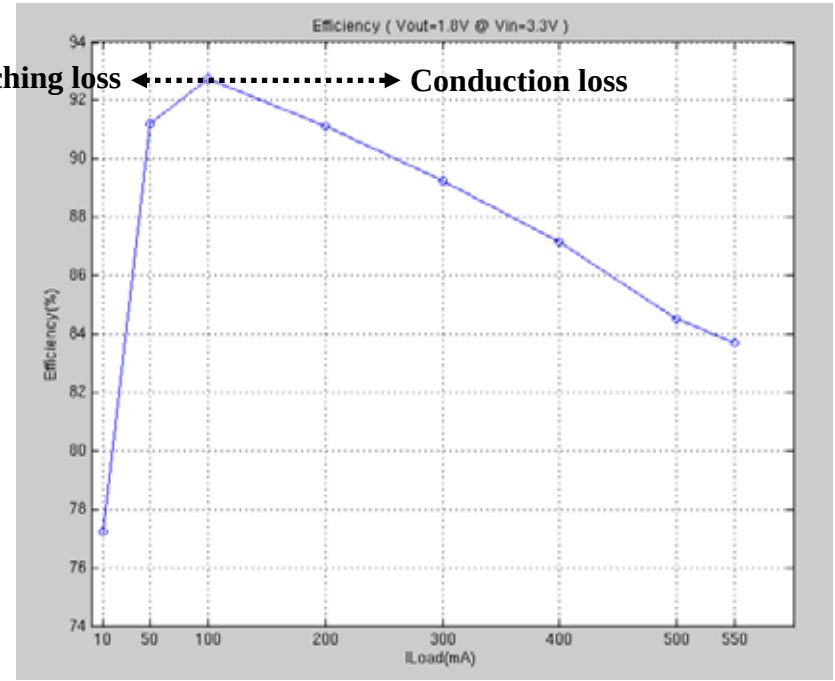


Fig.5.9 Efficiency in V_{out}=1.8V@ V_{in}=3.3V

To synthesize above measurements, the detailed data are token down to Table.5.1. Table.5.1 also shows the comparison of the simulation and measurement results. Because of the influence of process variation in IC and the parasitic effects in PCB layout, the practical measurement results are slightly different from and worse than the simulation results. Although the practical results are worse than the simulation results, the difference is quite small and can be accepted.

Table.5.1 Summary of measurement results

	Simulation	**Measurement**
Input Voltage	2.4V~3.6V	2.2V~3.6V
Output Voltage	0.424 V ~ 3V	0.412 V ~ 3V
Switching frequency	500kHz	≈550kHz
Output Voltage Ripple	< 20mV	< 20mV
Load current	< 600mA	< 550mA
Recovery time	≈55us (100mA→600mA) ≈55us (600mA→100mA)	≈60us (100mA→550mA) ≈55us (550mA→100mA)
Deviation Voltage	≈60mV (100mA→600mA) ≈60mV (600mA→100mA)	≈70mV (100mA→550mA) ≈73mV (550mA→100mA)
Line regulation	0.58% V/V	1% V/V
Load regulation	0.18% V/A	0.89% V/A (10mA→400mA) 0.24% V/A (10mA→500mA)
Efficiency	Max 96% (at 100mA)	Max 92.3% (at 100mA)

Finally, the measurement of conducted emission is mentioned as follows. The limits is described in Table 5.2

Table.5.2 Conducted emission limit (a) FCC (b) EN 55022

FCC		
Frequency (MHz)	Class A (dBuV)	Class B (dBuV)
0.45~1.705	60	48
1.705~30	69.5	48

(a)

EN55022				
Frequency (MHz)	Class A (dBuV)		Class B (dBuV)	
--	QP	AVG	QP	AVG
0.15~0.5	79	66	66-56	56-46
0.5~5	73	60	56	46
5~30	73	60	60	50

(b)

In measurement setup of conducted emission, the spectrum analyzer 3589A which I use is not the special instrument for the measurement of the EMI. Thus, it has no unit such as dBuV and function such as quasi-peak and average. The problem about unit can be solved by the conversion of dBuV to dBm (dBm = dBuV-107). The other problem about function can be not solved by mathematical way. So the design of input filter may be over design. But fortunately, this over-design margin can be regarded as the safe margin to avoid the influence of other factor. Fig.5.10 shows the frequency spectrum without input filter.

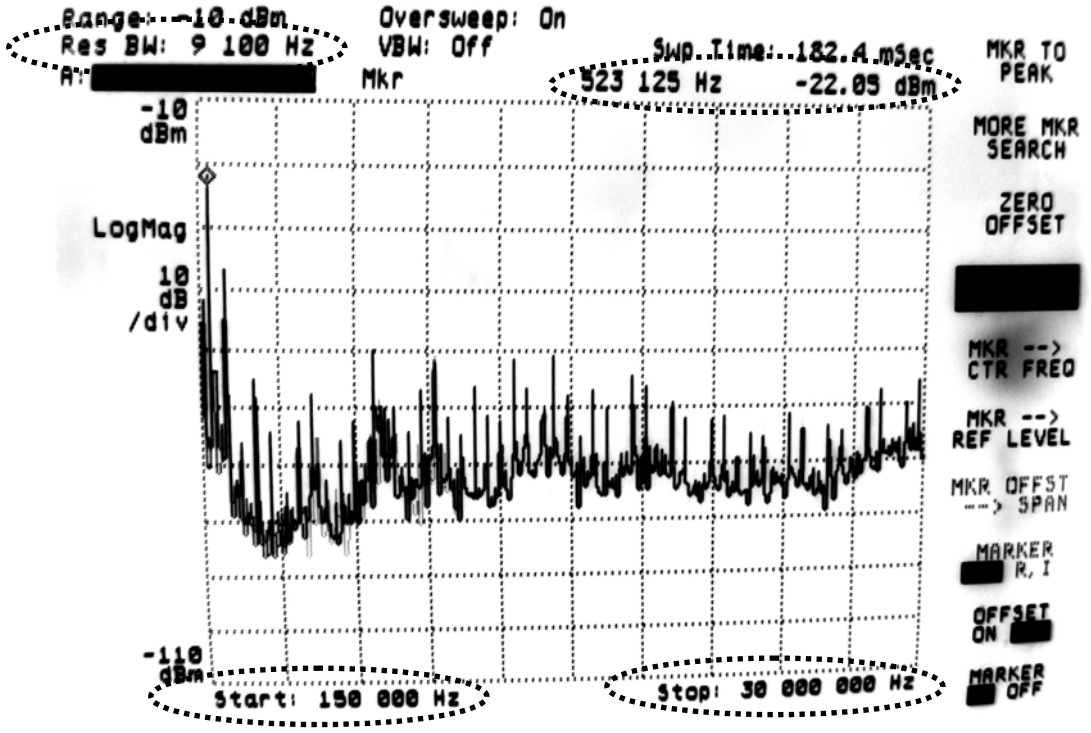


Fig.5.10 Frequency spectrum without input filter in V_{out}=1.8V and I_{Load}=550mA

The peak value is approximately -22dBm in 523 kHz. -22dBm is equal to 85 dBuV. In this thesis, the class B is the target. Form Table.5.2, The attenuation can be calculated to achieve this target.

FCC: 85 – 48 = 37 (dBuV) (5-1)

EN55022: 85 – 56= 29 (dBuV) (5-2)

Result: attenuation = 37 (dBuV) (5-3)

The input filter can be designed according to Eq.(5-3) and [22]. The circuit of this input filter is shown in Fig.5.11

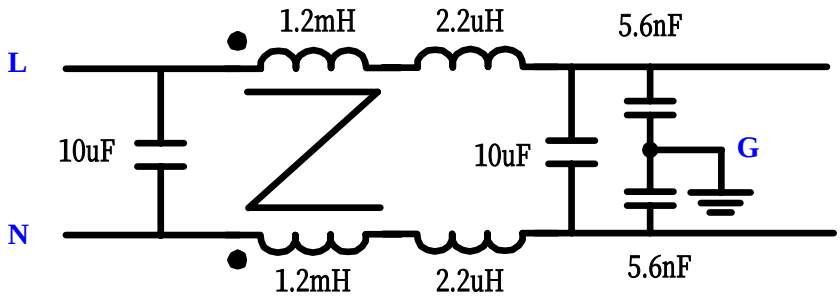


Fig.5.11 The complete input filter

Fig.5.12 shows the frequency spectrum with this input filter. The peak value is approximately -61.63dBm in 523 kHz. -61.63dBm is equal to 45.37 dBuV. With this input filter the conducted emission can effectively conform to the class B limits of FCC and EN55022.

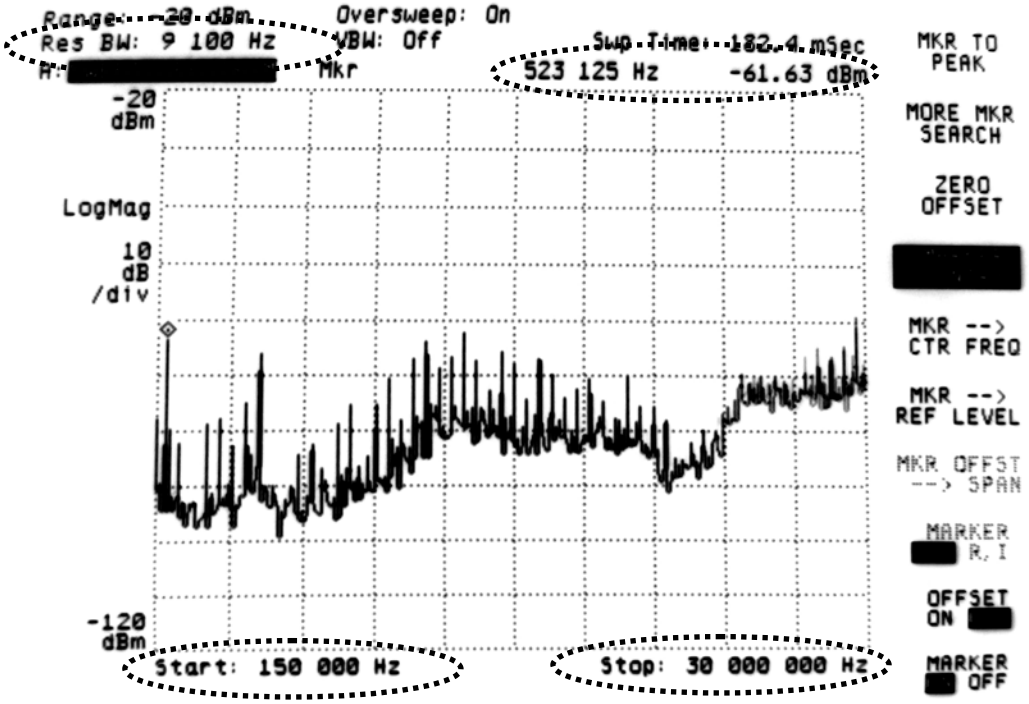


Fig.5.12 Frequency spectrum with input filter in V_{out}=1.8V and I_{Load}=550mA

Chapter 6

Conclusions and Future Work

In this thesis, a current mode buck regulator with an adjusted-slope compensation ramp scheme is implemented, including the analysis, circuit implementations and measurement results. Experimental results show this regulator can work properly in desired output voltage regardless of D>0.5 or D<0.5. By this adjusted-slope scheme, it can have not only better performance of gain and bandwidth but also higher efficiency than traditional constant-slope regulator. And the complexity of circuit design is also reduced due to omit the addition of sensed inductor current signal and compensation ramp. This regulator is built with TSMC 0.35um 2P4M 3.3V/5V Mixed Signal CMOS process. In the measurement, the output current can be up to 550mA and the conversion efficiency can be up to 92%. Thus, it is suitable for the application of portable products.

This regulator is implemented in this thesis successfully. But some shortcomings must be improved for better performance. From efficiency in Fig.5.9, we can know the efficiency is bad in light load ($\approx$10mA). Thus, a PFM mode which is suitable for adjust-slope scheme must be instituted in my system. In addition, the protection circuits are also needed to set up in my regulator in order to ensure the safe operation of the regulator and prevent the loading devices from damage. By increasing these considerations, this regulator will be reliable in practical application.

References

[1]. Horowitz, M.; Indermaur, T.; Gonzalez, R., " Low-power digital design " Low Power Electronics, 1994. Digest of Technical Papers., IEEE Symposium 10-12 Oct. 1994

[2]. Pedram, M.; Qing Wu, " Design considerations for battery-powered electronics " Design Automation Conference, 1999. Proceedings. 36th 21-25 June 1999

[3]. Marty Brown, "POWER SUPPLY COOKBOOK" 2nd ed., Butterworth-Heinemann, 2001

[4]. "Linear & Switching Voltage Regulator Handbook" ON Semiconductor Inc., Feb 2002

[5]. H. W. Whittington; B. W. Flynn; D. E. Macpherson; "SWITCHED MODE POWER SUPPLIES: design and construction" 2nd ed., Research Studies Press Ltd., 1997

[6]. Robert W. Erickson; Dragan Maksimovic, "Fundamentals of Power Electronics" 2nd ed., Kluwer Academic Publishers., 2001

[7]. "HISTORY AND DEVELOPMENT OF SWITCHED-MODE POWER SUPPLIES PRE 1987", http://www.steve-w.dircon.co.uk/fleadh/mphil/history.htm

[8]. Abraham I. Pressman, " Switching power supply design " New York: McGraw-Hill, 1991

[9]. Dr. Ray Ridley "Current mode or Voltage Mode?" Switching Power Magazine, October 2000

[10]. Ridley, R.B.,"A new, continuous-time model for current-mode control", Power Electronics, IEEE Transactions on Volume 6, Issue 2, April 1991

[11]. Ridley, R.B.,"A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM" Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE 11-14 June 1990

[12]. Darwish, M.; Huang, J.; Liu, M.; Shekar, M.S.; Williams, R.; Cornell, M., "Scaling issues in lateral power MOSFETs" Power Semiconductor Devices and ICs, 1998. ISPSD 98. Proceedings of the 10th International Symposium on 3-6 June 1998

[13]. "TPS62000 High-Efficiency Step-Down Low Power DC-DC Converter" Texas Instruments Inc. September , 2003

[14]. Roubik Gregorian, “Introduction to CMOS OP-AMP and Comparators ” New York: Wiley, 1999

[15]. David A. Johns and Ken Martin, “Analog Integrated Circuit Design” John Wiley & Sones, Inc. 1997

[16]. Ka Nang Leung; Mok, P.K.T.,“A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device“ Solid-State Circuits, IEEE Journal of Volume 37, Issue 4, April 2002

[17]. Sahu, B.; Rincon-Mora, G.A.,“A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications” Power Electronics, IEEE Transactions on Volume 19, Issue 2, March 2004

[18]. Cheung Fai Lee; Mok, P.K.T., “A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique” Solid-State Circuits, IEEE Journal of Volume 39, Issue 1, Jan. 2004

[19]. Lam, H.Y.H.; Wing-Hung Ki; Dongsheng Ma, “Loop gain analysis and development of high-speed high-accuracy current sensors for switching converters“ Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 5, 23-26 May 2004

[20]. Dongsheng Ma; Wing-Hung Ki; Chi-Ying Tsui; Mok, P.K.T.,” Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode” Solid-State Circuits, IEEE Journal of Volume 38, Issue 1, Jan. 2003

[21]. Ridley, R.B.; Cho, B.H.; Lee, F.C.Y.,” Analysis and interpretation of loop gains of multiloop-controlled switching regulators” Power Electronics, IEEE Transactions on Volume 3, Issue 4, Oct. 1988

[22]. Fu-Yuan Shih; Chen, D.Y.; Yan-Pei Wu; Yie-Tone Chen, “A procedure for designing EMI filters for AC line applications” Power Electronics, IEEE Transactions on Volume 11, Issue 1, Jan. 1996