F1: *High-Speed Interleaved ADCs*


Organizer: **Stéphane Le Tual,** *STmicroelectronics, Crolles, France*

Co-organizer: **Borivoje Nikolic,** *University of California, Berkeley, CA*

Committee: **Tetsuya Iizuka,** *University of Tokyo, Tokyo, Japan*
Ichiro Fujimori, *Broadcom, Irvine, CA*

Time-interleaved ADCs have become critical components in high-speed wireline and wireless communication systems. This forum will deliver a comprehensive treatment of state-of-the art design techniques for high-speed interleaved ADCs. Topics include transistor-level design techniques, calibration (estimation & correction), as well as the link between system specifications and required ADC performance.

Agenda

Time	Topic
8:00 AM	**Breakfast**
8:20 AM	**Introduction**

8:30 AM **Interleaved ADCs Through the Ages**

Ken Poulton, *Keysight Laboratories, Santa Clara, CA*

Research on interleaved samplers and ADCs goes back to work first published in 1980 by Hewlett Packard and UC Berkeley. Products such as oscilloscopes used small numbers of interleaved ADCs to reach the highest sampling rates available in the 1980s and 1990s. In 2002, the massive time-interleaving revolution was kicked off, which later gained further momentum with low-power ADC slice architectures such as SARs. Frequency interleaving provides another recent technology branch. This talk will present the history of ADC interleaving, focusing on major achievements and some of their problems and the solutions that were invented to solve them.

Ken Poulton received a B.S. in Physics and an M.S. in Electrical Engineering from Stanford University in 1980. He then joined Hewlett-Packard Laboratories (now Keysight Laboratories in Santa Clara, CA) where he has developed integrated circuits for data conversion in GaAs MESFET, GaAs HBT, silicon bipolar, BiCMOS and CMOS technologies. He became a project manager in 2000; he is now a master engineer. Ken has published papers on eight "world's-fastest" data converters, including "A 1 GHz 6-bit ADC System," which won the JSSC Best Paper Award for 1987. He was a member of the ISSCC International Technical Program Committee and a Guest Editor for JSSC. He holds 11 patents and is an IEEE Fellow.

9:20 AM **Mismatch Error Correction for High-Resolution, GS/s Time-Interleaved ADCs**

Per Löwenborg, *Signal Processing Devices, Linköping, Sweden*

After more than 35 years of research and development, the level of commercial and academic interest in time-interleaved ADC arrays is now higher than ever. With the possibility to extend the sampling rate beyond the limits of single-core ADCs, time-interleaving is now being deployed in high-resolution ADC designs. However, mismatch between the ADCs in the array and the resulting aliasing distortion that degrades the effective resolution is a challenge in these systems.

This presentation compares a select set of methods for mismatch error correction and highlights some possibilities and limitations. These methods involve the process of reconstructing new samples with less aliasing distortion as well as techniques for computing estimates of the mismatch needed for the correction. Measurement results of digital mismatch error correction applied to high-resolution time-interleaved GS/s ADC arrays are presented. Finally, the close connection between I/Q-balancing in quadrature demodulators and mismatch error correction in time-interleaved ADC is illustrated.

Per Löwenborg was born in Oskarshamn, Sweden, in 1974. He received Ph.D. and Docent degree in Electronics Systems from Linköping University, Sweden, in 2002 and 2009, respectively. He has more than 15 years post-graduate experience in R&D work within the field of analog and digital filters and filter banks, data converters, and signal processing enhancement of mixed-signal circuits. He is the author or co-author of about 75 international journal and conference papers, one textbook, and holds four patents. He was awarded the 1999 IEEE Midwest Symposium on Circuits and Systems best student paper award and the 2002 IEEE Nordic Signal Processing Symposium best paper award and has served as Associate Editor for IEEE Signal Processing Letters. Since 2006, Dr. Löwenborg is Chief Technology Officer at Signal Processing Devices Sweden AB which is an electronics company specializing in signal-processing enhancement solutions of analog and mixed-signal circuits as well as high-performance digitizers.

10:10 AM **BREAK**

10:35 AM **Highly Accurate Adaptive Digital Calibration for High-Speed High-Resolution Time-Interleaved ADC**

Takashi Oshima, *Hitachi, Tokyo, Japan*

Purely digital post-calibration for time-interleaved A/D converters is presented with theoretical analysis and experimental results. It can correct all kinds of mismatches (gain, DC offset, sampling timing and bandwidth) among sub-converters assisted by the reference converter. It can compensate for the higher-order effects of sampling-timing and bandwidth mismatches with minimum complexity, which is essential to achieve both very-fast sampling rates and very-high effective resolution. The proposed calibration technique works successfully for both Nyquist-sampling and sub-sampling time-interleaved A/D converters. Therefore, it can be applied to both direct-sampling and direct-sub-sampling next-generation receivers.

Takashi Oshima received B.S., M.S. and Ph.D. in physics from University of Tokyo in 1996, 1998 and 2001, respectively. He joined Central Research Laboratory of Hitachi Ltd. in Tokyo in 2001, where he has been developing A/D converters, PLL, wireless-transceiver circuits and various sensor circuits. He developed many commercial ICs so far including the RF-ICs for Bluetooth, UHF RF-ID readers and multi-mode cellular phones. From 2005 to 2006, he was a visiting researcher at Berkeley Wireless Research Center of University of California at Berkeley, USA, where he made a research on digitally assisted A/D converters. From 2009 to 2012 he served as treasurer and secretary of IEEE Solid-State Circuits Society Japan Chapter. As the secretary of IEEE Solid-State Circuits Society Japan chapter, he organized several technical meetings and seminars in Japan. He currently serves as a Technical Program Committee member of ESSCIRC. He is a co-recipient of 2010 Best Invited Paper Award of IEICE Electronics Society in Japan and a co-recipient of 2003 R&D 100 Award from R&D Magazine. He also received the contribution awards from IEICE in 2011 and 2013. He holds 7 patents of wireless transceivers and PLL and 8 patents of A/D converters. His current research interests include the next-generation wireless transceiver design and the digitally assisted A/D converters. He is a member of IEEE, IEICE and Physical Society of Japan.

11:25 AM **ADC Interleaving Errors Corrected by Adaptive Post-Processing**

Asad Abidi, *University of California, Los Angeles, CA*

All interleaving errors express themselves with a particular structure in the frequency domain. By extending well-known methods of adaptive interference cancellation, errors can be detected and suppressed using only digital signal processing at the ADC output. The system adapts rapidly on sets of discrete tones, but requires sophisticated sub-band adaptation and coefficient diffusion to track wideband stationary waveforms.

Asad Abidi is Distinguished Professor of Electrical Engineering at UCLA. He is Fellow of IEEE and Member of the National Academy of Engineering.

12:15 PM **LUNCH**

1:20 PM **Specifications vs. Applications: Driving Architectural Choices**

Aaron Buchwald, *InPhi, Irvine, CA*

Time interleaving gives designers an additional degree-of-freedom to solve problems of achieving ultra-fast quantization at reasonably high resolution. The technique is not free and certainly not without problems. For as soon as multiple paths are encountered in the signal chain, a myriad of errors become apparent, often glaring. It turns out that in a non-interleaved ADC, a lot of non-idealities hid under our noses, but were "mixed" to DC where we weren't even aware they existed. Multi-path design modulates these "hidden" errors and their harmonics with sub-multiples of the sample rate quickly producing a "spur farm."

Mitigating all possible time-interleaved errors comes at a heavy cost in complexity, risk, power and performance. Knowing which errors are most important and which can be neglected in any given application is essential for picking an appropriate architecture and calibration scheme. This talk will review specification requirements for various applications where time-interleaved ADCs might be used. Different types of error sources will be treated separately to determine their impact on overall system performance. Careful analysis of all classes of errors will ultimately drive key decisions and trade-offs in the choice of architecture, digital signal processing and circuit design.

Aaron Buchwald has 32 years experience in the field of analog integrated circuit design. He is currently a Fellow at Entropic Communications after the acquisition of Mobius Semiconductor, where he was CEO and founder. Prior to Mobius, Dr. Buchwald worked at Broadcom, where he helped build a world-class analog team emphasizing design in a mixed-signal environment. Dr. Buchwald's work on embedded CMOS Analog-to-Digital Converters (ADCs) enabled the production of single-chip cable set-top boxes and cable modems with integrated analog front ends and DSP circuitry. His work with Klaas Bult was awarded the best paper prize in 1997 at ISSCC. Later, Dr. Buchwald was responsible for development of high-speed serial transceivers (XAUI, CX4 and Fiber Channel) at Broadcom. The initial XAUI transceivers were some of the first to employ adaptive receive equalization. Dr. Buchwald was formerly an Assistant Professor at the Hong Kong University of Science and Technology (HKUST). In his early career, Dr. Buchwald spent two years as an analog IC designer at Siemens in Munich, Germany. Prior to that, he spent four years at Hughes Aircraft Company in El Segundo, CA. Dr. Aaron Buchwald was born in Ames, Iowa and received a B.S.E.E. from the University of Iowa, Iowa City, Iowa, and an M.S. and Ph.D. from the University of California, Los Angeles. He is co-author of the book Integrated Fiber-Optic Receivers. He has taught professional short-courses and tutorials on data converters and serial transceivers.

2:10 PM **GS/s Time-Interleaved ADCs for Broadband Multi-Carrier Signal Reception**

Kostas Doris, *NXP, Eindhoven, The Netherlands*

Today's low-to-medium resolution extensively interleaved analog-to-digital converters (ADC) are an excellent fit for the conversion of GHz broadband signals. They are amalgams of algorithmic concepts and circuit techniques that adapt the successive-approximation search algorithm to the properties of nanometer CMOS technologies. But, are extensively interleaved ADCs capable to meet the challenges posed by multi-carrier communication and radar applications that typically require very low noise and spurs, absence of signal images, high linearity, and large bandwidth?

This presentation starts by showing the impact of time interleaving on the conversion of multi-carrier broadband signals, such as those encountered in cable and short-range wireless communication systems. Key circuit issues and design tradeoffs are then presented, linking them to the properties of multi-carrier signal reception using the DOCSIS standard as an example. The presentation then shows how the introduction of architectural concepts such as hierarchy, redundancy, frequency translation and extensive digital calibrations can offer new degrees of freedom to enable low power GS/s broadband multi-carrier signal reception.

Kostas Doris was born in Thessaloniki, Greece in 1973. He received the M.Sc. Physics and Radio-Electronics degrees from Aristotle University of Thessaloniki, Greece, in 1996 and 1998, respectively. In 2004, he received his Ph.D. degree from the Technical University of Eindhoven, The Netherlands. He joined Philips Research in 2003, and subsequently NXP Semiconductors in 2006. He is currently heading the department of High-speed Data Acquisition in Central Research & Development in NXP. His area of interest includes high-speed high-resolution data converters, mm-wave receivers and high-speed serial interfaces. He is the author and co-author of a multitude of papers, patents and books in the field of data converters.

3:00 PM **BREAK**

3:20 PM **Embedded CMOS ADCs for Optical Communications**

Yuriy M. Greshishchev, *Ciena, Ottawa, Canada*

Optical communications has been undergoing revolutionary transformations, where CMOS DSP ASICs and embedded interleaved ADCs are main reason for its success. Time interleaving is a holy grail of CMOS design to satisfy high sampling rate requirements. Less known and popular is frequency interleaving, which tackles the bandwidth limitations. Potentially, these two interleaving techniques may help to fulfil ever-rising requirements for the optical communication ADCs.

Yuriy Greshishchev received the M.S.E.E. in 1974 and Ph.D. in 1985, both in the Ukraine. He held a Post- Doctoral Fellow position at the University of Toronto, Canada in 1994-1995. He joined Nortel (now Ciena), Ottawa, Canada in 1996, where he is currently a Sr. Technical Advisor and Data Converter Architect for optical transport product. His frontier contributions to multi-gigabit SiGe and CMOS circuits reflected in numerous IEEE SSCS publications, workshops, and tutorials. Dr. Greshishchev served on the ISSCC International Technical Program Committee (2001-2009). He was a Guest Editor for the IEEE Journal of Solid-State Circuits (Dec. 2005). Dr. Greshishchev was co-recipient of an ISSCC 2008 award for the panel topic "Trends and Challenges in Optical Communications Front-End." He is now a TPC member for the Compound Semiconductors IC Symposium.

4:10 PM **PANEL**

Moderators: ***Bora Nikolic*** *(UC Berkeley),*
Dave Robertson *(ADI)*

5:00 PM **CLOSING REMARKS BY CHAIR**

Interleaved ADCs Through the Ages

Ken Poulton → since 80's
Keysight Laboratories

Topics

- What is Time Interleaving
- History of Time Interleaving
- ADCs for Oscilloscopes (and Other Instruments)
- Frequency Interleaving
- Issues in Interleaved ADCs and Some Solutions

But not really in that order…

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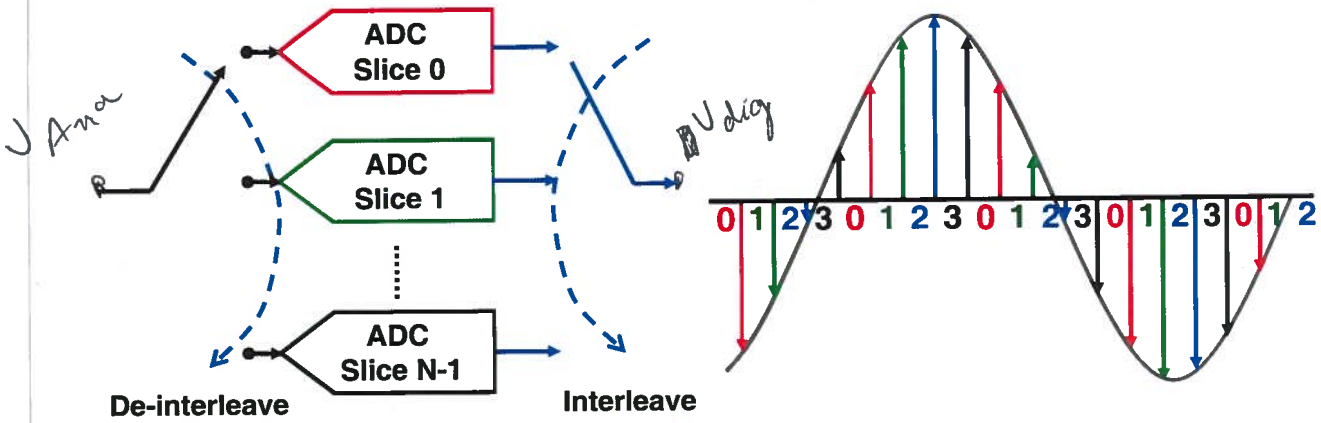
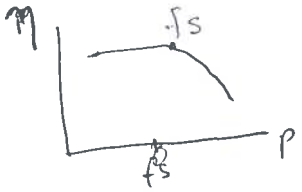
Time Interleaving Idea



- Unit (slice) ADC speed is limited by comparator and amplifier speed
- Interleave multiple ADC slices to increase total sampling rate

Reasons for Time Interleaving

- Speed
  - Sample rate multiplied by N_{slices}
  - Nyquist BW multiplied by N_{slices}
- Power Efficiency
  - The ADC slice can operate at its most *efficient* sample rate
- Process choice
  - Can use a slower process for a given total sample rate



Issues with Time Interleaving

- Analog Bandwidth goes *down*
  - Many slices connected to the analog input
- Interleaving errors due to slice-to-slice mismatch
- Complexity
  - N times as much ADC hardware
  - Additional clock generation, much of it critical
  - Additional circuits to improve the BW and interleaving errors

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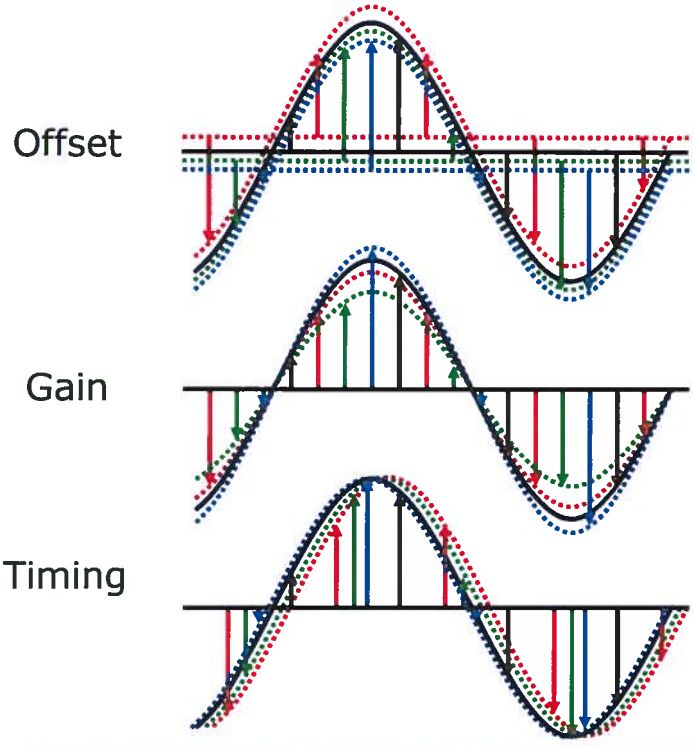
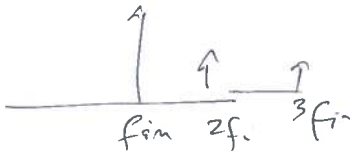
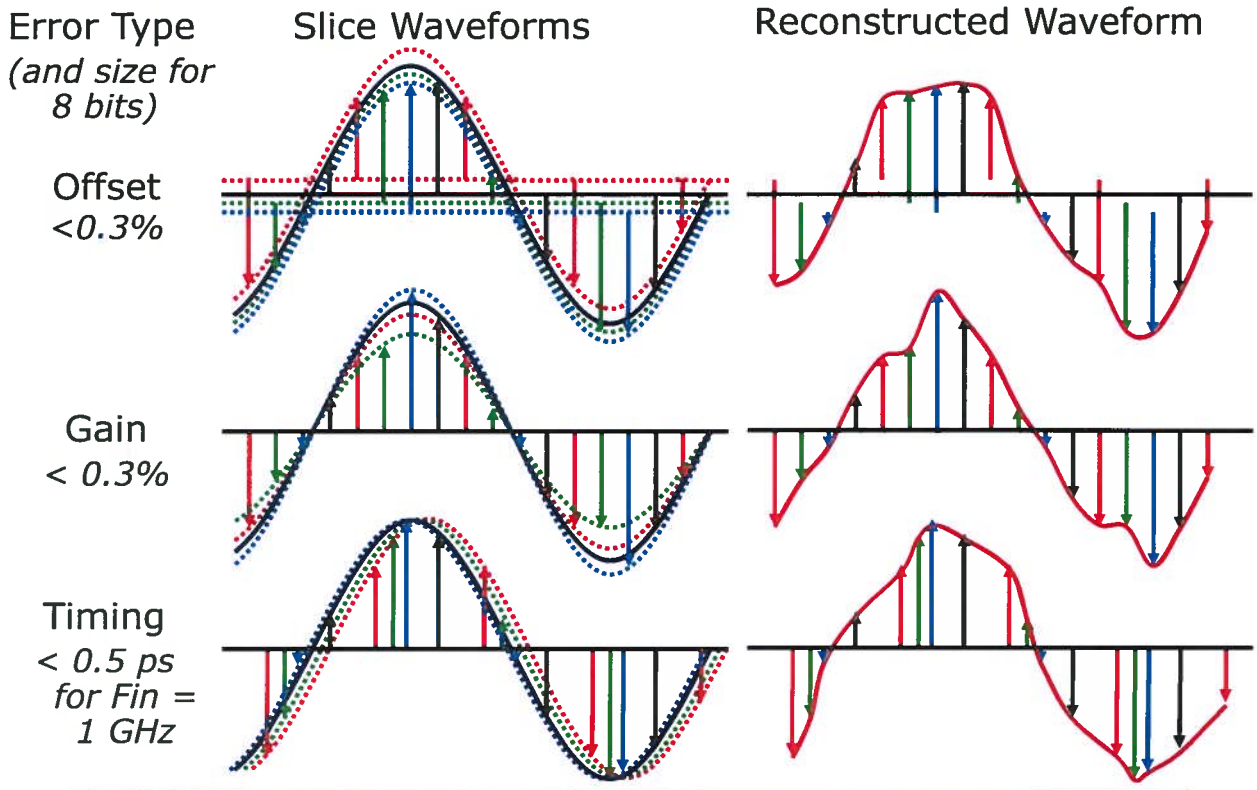
Types of Interleaving Errors

Due to Slice-to-Slice Mismatch





Results of Interleaving Errors



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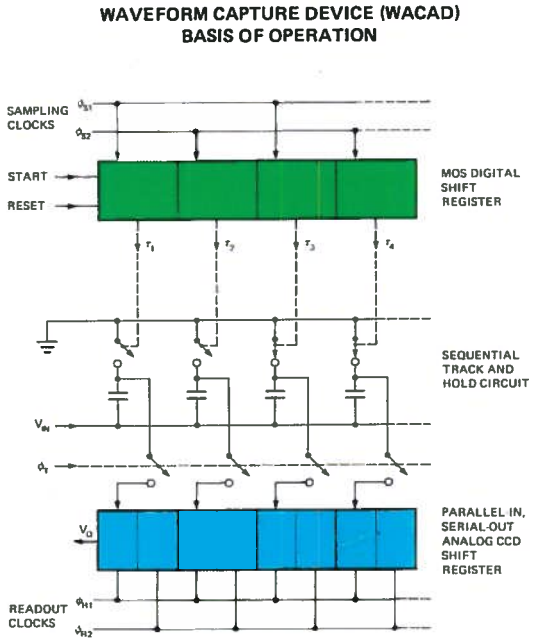
1980: First Interleaving - Analog Storage

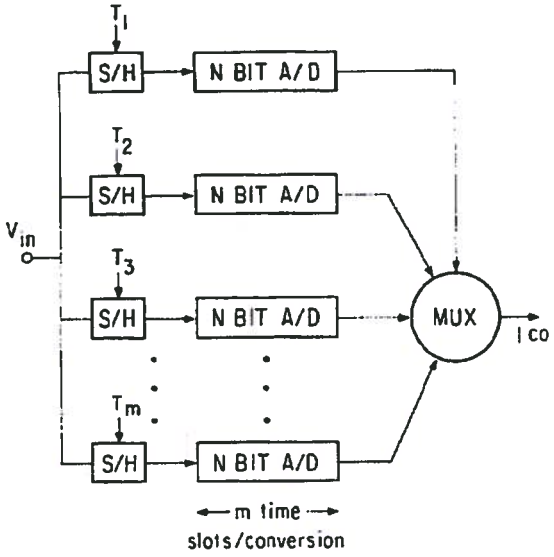
- First known publication on time interleaving (but not an ADC)
- Slice:
  - 200 parallel charge samplers triggered at 40 ns intervals
  - CCD shift register shifts out the analog samples slowly
- Off-chip ADC
- Four slices interleaved for 100 MSa/s total
- Correction for interleaving errors and CCD charge transfer effects
  - Captured waveform recycling
- 6 effective bits up to 30 MHz



"A 100 MS/s Waveform Digitizer with Comprehensive Error Correction", John Corcoran, Tom Hornak, 1980

1980: First Interleaved ADC

- Slice: 7-stage SAR pipeline at 0.625 MSa/s
- Four-way interleaved for 2.5 MSa/s
- Implemented in 10 um CMOS
- 6.2 effective bits at 100 kHz in
- Identified and analyzed effects of offset, gain and timing mismatches



"Time interleaved converter arrays", Black, W., Jr. ; Hodges, D., ISSCC 1980 and JSSC 1980

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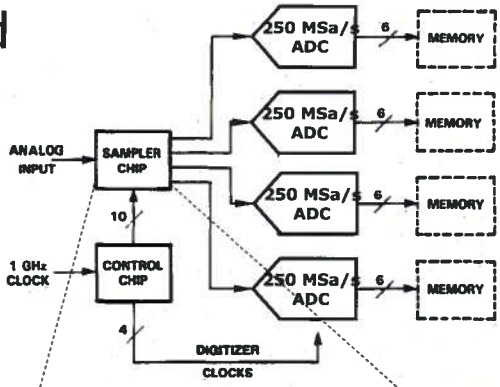
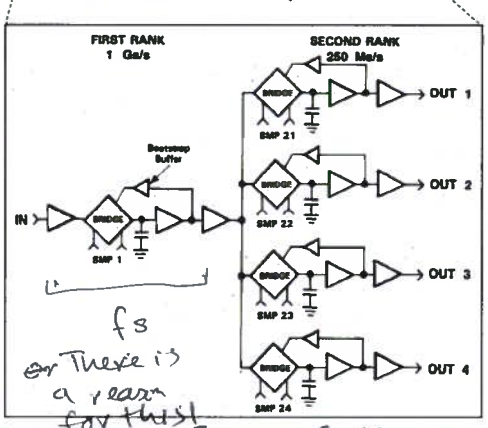
1987: The First Interleaved ADC Product

- HP 54111D Digital Oscilloscope
- Approach
  - 6-bit bipolar ADC at 250 MSa/s
  - 4-way interleaving
  - 2-rank GaAs T/H chip
  - Custom NMOS memory chip
  - Mix technologies for speed vs complexity
- Mismatch control
  - Offset and gain alignment DACs
  - Single front-end sampler avoided timing calibration

"A 1 GHz 6-bit ADC System", Ken Poulton, John J. Corcoran, Thomas Hornak, IEEE Journal of Solid State Circuits, Dec 1987





Gaining Resolution From Interleaving

Limitations of 6-bit ADC resolution

– 6-bit LSB steps visible on the display

– Better DC resolution desired

Solution:

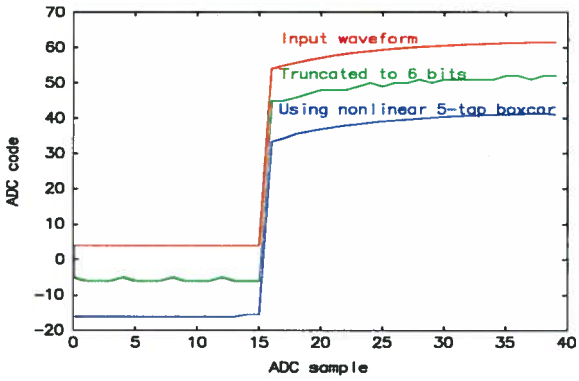
1. Offset the 4 ADCs by ¼ LSB each
2. Apply a nonlinear boxcar filter:
   - Compute linear 5-tap boxcar
   - Limit the change to 0.5 LSB from the original value

Issues:

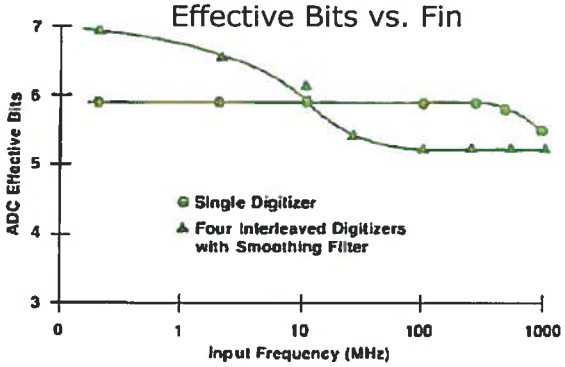
– "preshoot" on steps, quenching of fast near-LSB signals

Not needed in 8-bit scopes

Effect of Filter on Time Record



Effective Bits vs. Fin



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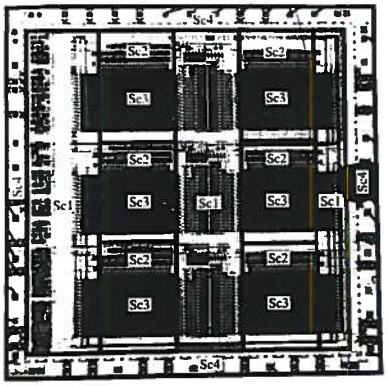
Analog Storage Products

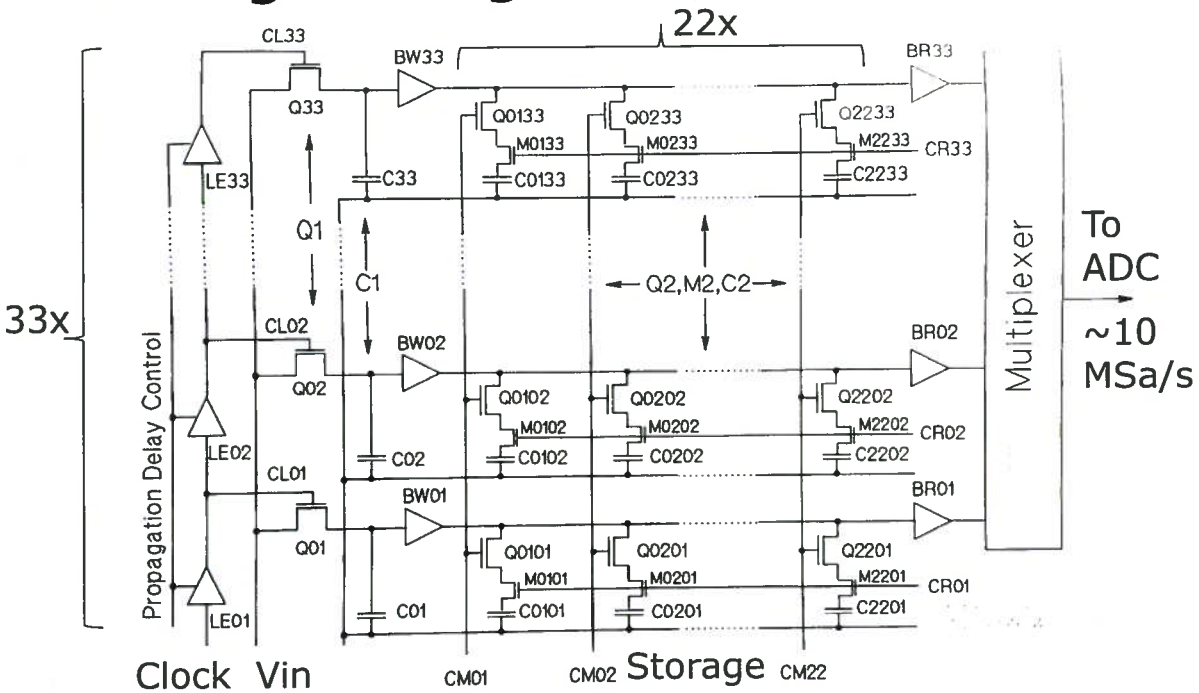


- Analog storage chip
  - 33 interleaved samplers
  - 60.6 MHz clock -> 2 GSa/s
  - 22 storage caps per sampler
  - 2178 samples
- Readout to external ADC ~10 MSa/s

- ~1991: Tektronix TDS 350 Scope
  - 200 MHz BW = high end
  - 1 GSa/s, 2 channels
  - 180 ps pp timing errors
    => ~4 eff bits at 200 MHz

- Today: handhelds apparently still use analog storage
  - 200 MHz BW = low end
  - 1.25 GSa/s
  - 10,000 samples

Analog Storage Chip Schematic



Clock 60.6 MHz

Vin 0-200 MHz

US 4,271,488 "High-Speed Acquisition System Employing an Analog Memory Matrix", 1981 "Investigation of an Analog Sampling and Storage Chip", HP internal report, ca. 1995

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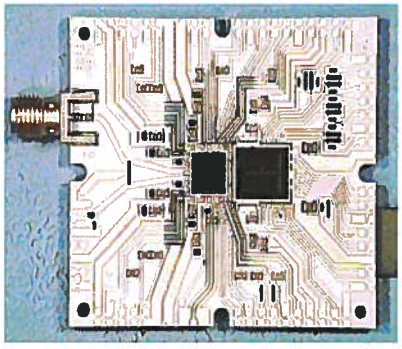
Interleaved ADCs in the 90s

- Mostly for Scopes
- Bipolar ADC
  - High Speed
  - Threshold Accuracy
- Low transistor count
  - Yield
  - High power per transistor
- High slice sample rate
  - Time-interleaving of 2-8 unit ADCs
- Front-end T/H topologies:
  - Diode Bridge
  - Switched Emitter Follower
  - Sample + Filter
- High Power
- Custom Packaging

E.g.: 1997 4 GSa/s Module

- 4 GSa/s, 7-bit bipolar ADC
  Folding + Interpolating
- 2-way interleaving on chip -> 4 GSa/s
  4-way interleaving on PCB -> 8 GSa/s
- Custom CMOS Memory
- Thick-film package,13 W, expensive



Timing Calibration Methods

- S. Takeuchi, et al (Sony/Tektronix) used sawtooth waveforms
  - Hard to make accurate at high frequencies
  - "Analog-to-digital conversion method and apparatus", US 4345241, Aug 1982
- H. Katusmata (Sony/Tek) used pulse waveforms at a beat frequency where each slice sampled the same voltage on the waveform
  - Only uses the zero crossing information, needs precise control of the cal frequency.
  - H. Katsumata, et al, "Method and apparatus for calibrating an analog-to-digital conversion apparatus", US 4736189, Apr 1988
- John Corcoran (HP) used the two-rank T/H architecture to avoid timing calibration
  - Requires a full-rate sampler that adds power, noise, distortion
- Y.C. Jenq (Tektronix) used a DFT-based method
  - Uses DFT of the waveforms. Needs precise control of the cal frequency.
  - "Interleaved digitizer array with calibrated sample timing", US4763105, Jul 1987
- John Corcoran (HP) devised a way of measuring timing and amplitude errors based on per-slice best-fit analysis.
  - Allows a non-frequency-locked cal source for low-cost instrument self-cal.
  - "Timing and amplitude error estimation for time-interleaved analog-to-digital converters", US 5294926, 15 Mar 1994

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Some Scope ADCs in the 90s

- HP in 1991
  - 500 MSa/s per slice, 1 GSa/s per chip, 13-GHz silicon BJT, folding ADC
  - 4, 8-way interleaved to up 4 GSa/s

  Rush & Byrne, "A 4GHz 8b Data Acquisition System", ISSCC 1991
- HP in 1994
  - 4 GSa/s, 6 bits, 50-GHz GaAs HBT, folding ADC
  - Did not go into a product

  Poulton, et al, "A 6-bit, 4 GSa/s ADC Fabricated in a GaAs HBT Process",1994 GaAs IC Symposium
- HP in 1997
  - 2 GSa/s per slice, 4 GSa/s per chip, 7 bits, 25-GHz silicon BJT, folding and interpolating
  - 2, 4-way interleaved to 8 GSa/s

  Poulton, et al,"An 8-GSa/s 8-bit ADC System", VLSI Symposium, 1997
- Other scope manufacturers
  - developed bipolar ADCs, but did not publish
  - followed the fast-slice, low-interleaving paradigm

Calibration and Correction Choices

- Corrections = analog and digital circuits that improve the accuracy
  - E.g., Voltage adjust DACs, delay DACs, DSP
- Calibrations = the processes that set the correction parameters

- To Cal or Not To Cal
  - *Accurate by Design (no calibration and correction)*

    -- Full matching and linearity requirements must met by design
  - Calibration and Correction

    \+ Can relax analog performance requirements

    \+ Analog circuits can be limited only by SNR, not matching
    - Smaller, lower power circuits

    -- Added power for correction circuits

    -- Added complexity for corrections and for calibrations

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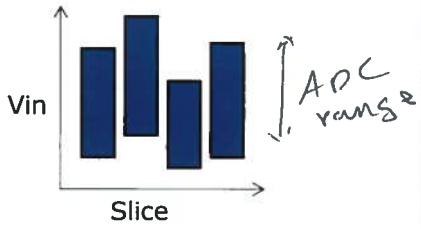
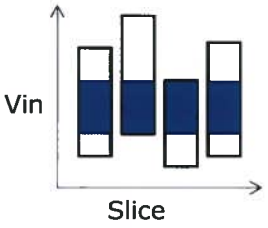
Analog vs. Digital Corrections

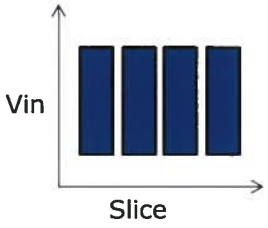
As fabricated:
Usable analog range of each slice is different



Digital correction:
Use only the voltage range that overlaps in all slices.
+ Calibration is digital and simple
-- SNR and resolution degraded



Analog correction:
DACs adjust the offset and gain of all slices to match
+ Preserves slice ADC resolution and SNR
-- More analog circuits to design



Correction Circuits

- Offset and gain corrections are simple in digital: just an adder and a multiplier per slice.
- Timing corrections in digital circuits require a delay filter
  - Bandwidth limited (e.g., 80% of Nyquist)
  - Significant complexity and power
- Timing corrections in analog require variable delays
  - Power can be high, proportional to delay/jitter
- Either analog or digital *or both* can be used
- More digital has been used in recent years

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Calibration Choices

- On-chip vs off-chip calibration (parameter computation)
  - Off Chip:
    + lower chip cost
    + lower design risk
  - On Chip
    + Simpler for the ADC user

- Foreground calibration vs. Background calibration
  - Foreground (offline)
    + Independent of the input signal
    -- ADC user needs to provide cal signals
    -- Dead time during calibration
  - Background (online)
    + Can be simpler for ADC user
    -- More complex chip
    -- Often places requirements on the input signal characteristics

"A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration", Shafiq Jamal, et al, JSSC, Dec 2002, pp1618-1627

IC Process Trends in the 90's

- Consolidation of fabs
  - In 1990, lots of captive IC fabs (e.g., 10 fabs in HP)
  - Late 1990's: $1B fab cost squeezed out many players
  - Rise of commercial foundries with leading-edge CMOS
- Bipolar and BiCMOS
  - Increasingly a niche technology, focused on performance
  - Investment driven by specific market trends
    - ~1990: CPUs, ~2000: RF, ~2010: 25+ Gb/s comms & uW
    - Investment fades as CMOS gets fast enough for a given application
    - => Less predictable progress in bipolar
- CMOS
  - Following Moore's Law
  - Lower wafer costs
  - Higher integration can reduce system costs
  - More predictable progress in performance

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Could We Use CMOS for Scope ADCs?

- "Don't be stupid"
  - CMOS ADCs (ca 1995) were 25x slower than bipolar
  - CMOS transistors are 10 times less accurate than bipolars
- "But..."
  - CMOS chips are cheap and transistors are virtually free
  - Could integrate with DSP and memory
  - Might be lower power

"If we don't do [ADCs] in CMOS, someone else will."
-- Dave Robertson, ADI, ISSCC ca 1995

Architecture: Massive Interleaving of Low-Power ADCs

- Focus on the strengths of CMOS: low power and high integration
- Start with a power-efficient CMOS ADC slice
- Time-interleave like crazy to get the required sample rate
- Fix up analog accuracy through calibration

- Challenges:
  - Track/Hold : Bandwidth, Signal distribution
  - Clock generation
  - ADC: Trading Sample Rate, Power, area, # of slices
  - Many Places for Mismatch

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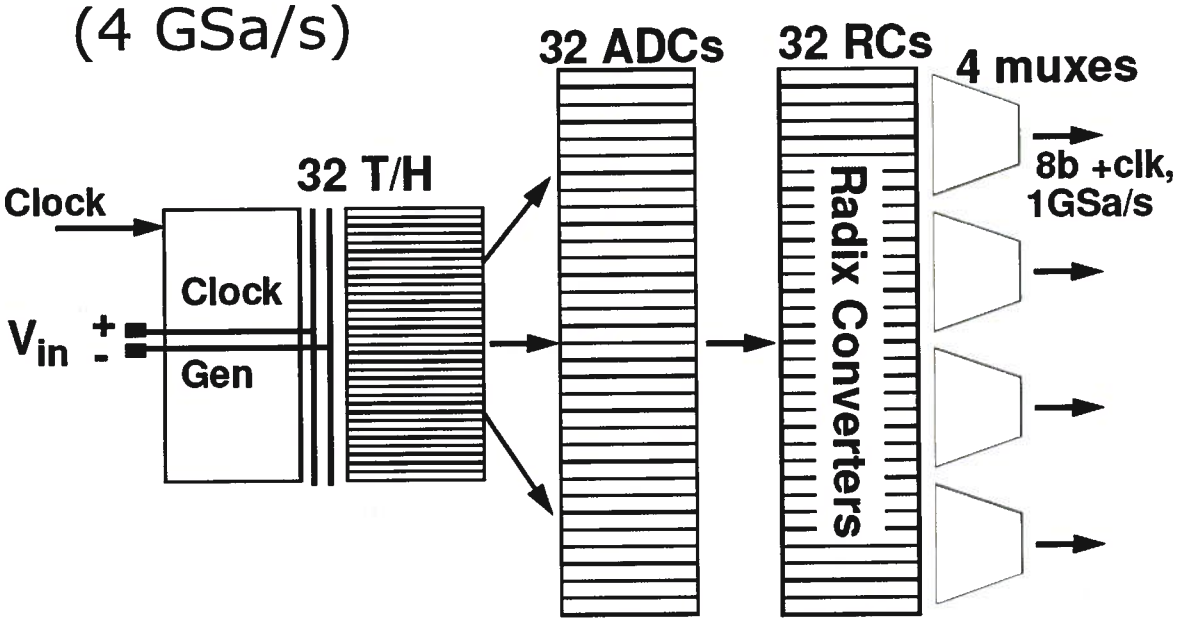
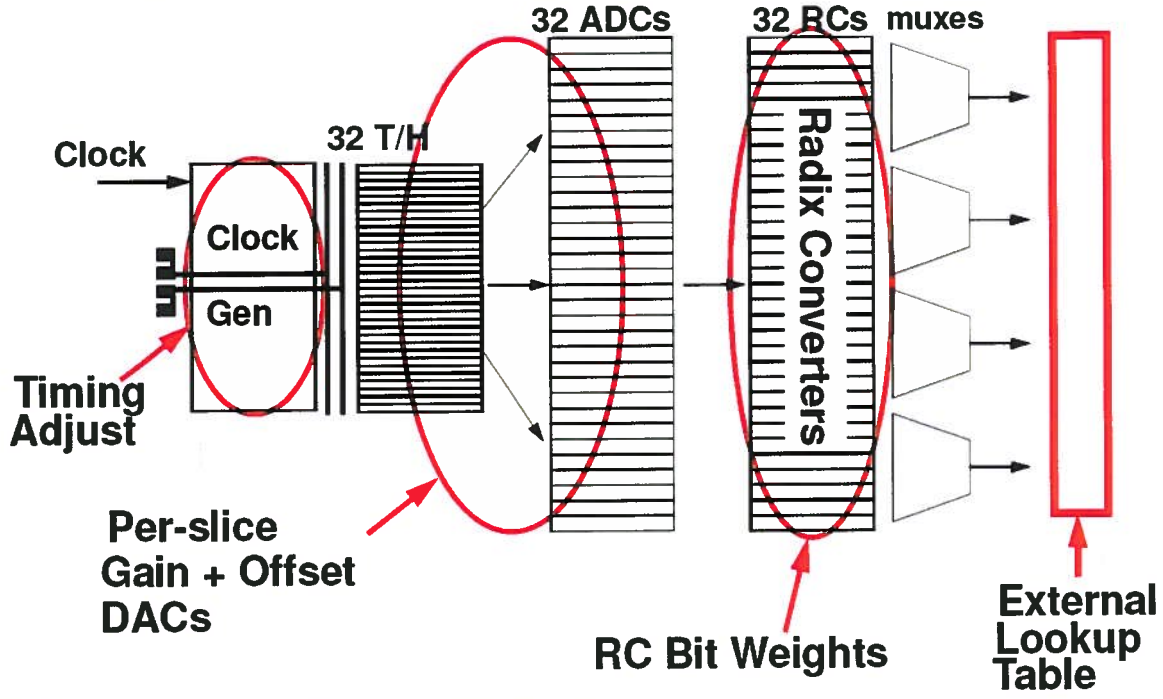
2002: CMOS ADC Chip Architecture (4 GSa/s)



- 32 time-interleaved pipeline ADCs at 125 MSa/s
- Net sample rate is 4 GSa/s

What Is Calibrated?



- Foreground (offline) Calibration with DC and Pulse sources

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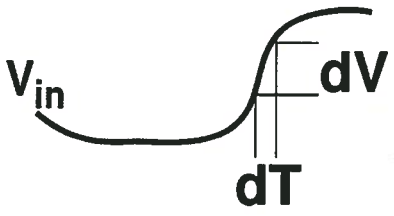
Advantages of a Calibration Approach

- Device mismatch tolerance increased
  - In this case, from ~0.25% to ~10% mismatch
  - Can design for SNR rather than mismatch
  - Smaller transistors
  - Lower power
- Second-order effects can be covered by the same calibrations
  - Smaller device mismatch effects (e.g., layout-related delta W)
  - Delay and gain mismatches due to layout asymmetries
- Adjust DACs need not be tightly matched, merely have enough resolution

Timing Errors

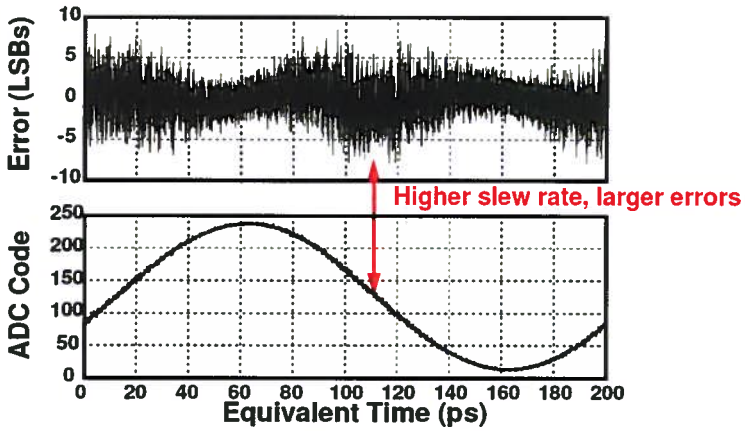
- Fast input signal converts a sample timing error (dT) to an apparent voltage error (dV).



Rule of Thumb:

1 ps rms @ 1 GHz Fin

--> 7 effective bits



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Clocks for Front-End Samplers

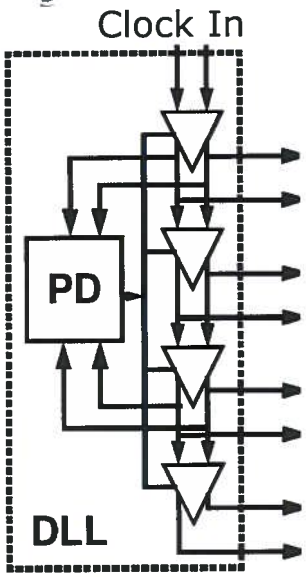
- Single Front-end Sampler
  - **One** low-jitter clock (30-1000 fs rms jitter, dep. on application)
  - N reduced-accuracy clocks (1-10 ps rms jitter and alignment)
    - Second rank requires fairly accurate clocks due to analog settling effects
- Interleaved front-end samplers
  - **N** Full-accuracy clocks
    - 30-1000 fs rms jitter ***and alignment***

Using Lower Input Clock Frequencies

P vs. Jitter trade off

- Full-rate clock
  - Used by earlier bipolar designs
  - Just divide the input clock down to get the slice clocks
  - Low jitter, modest calibration
  - High-frequency clock sources are expensive
- Low-rate clock
  - Fclock << Fs (e.g., 500 MHz << 4 GSa/s)
    - Saves power
    - Full rate just infeasible for some CMOS ADCs
  - N parallel samplers requires N full-accuracy clocks
- DLL for N clocks, constant jitter spec
  - N/2 stages
  - Stage power scales as N to maintain jitter
  - => DLL power scales as N2

"Delay Lock Loop"!



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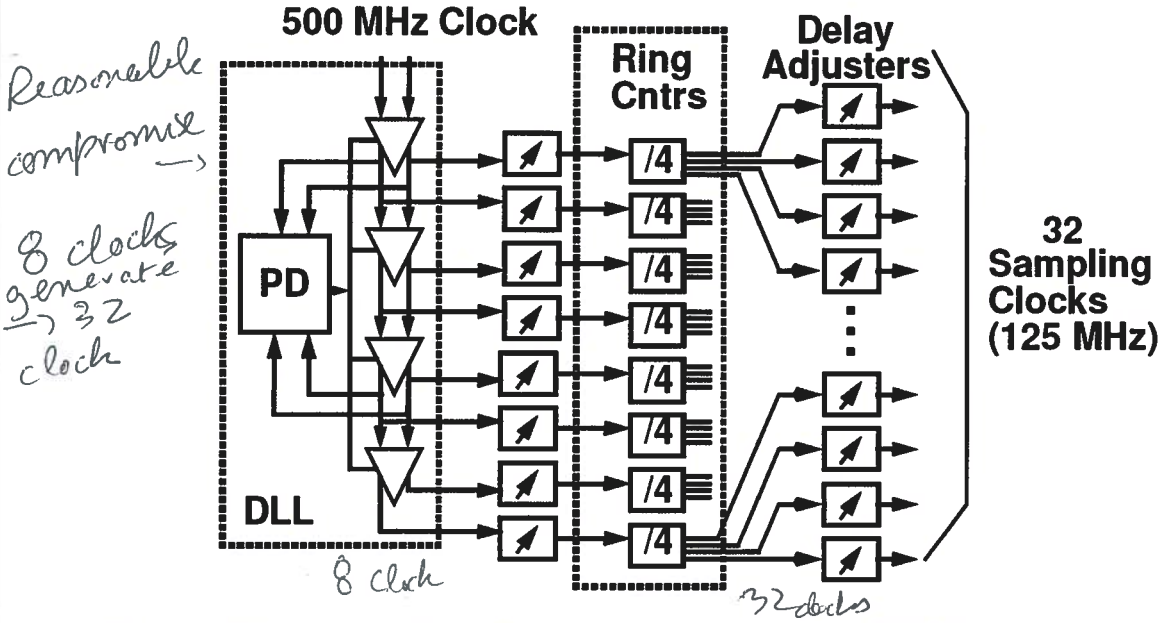
Hybrid Clock Generator

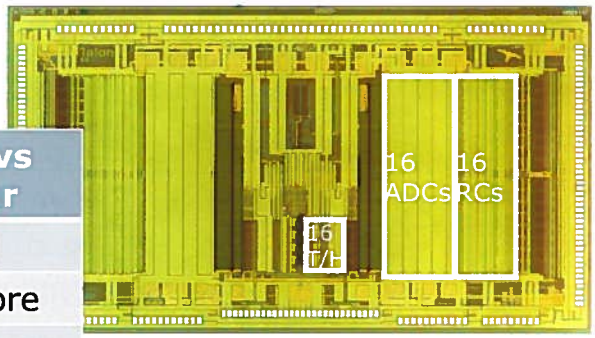


- 4 GSa/s, ~ 1 ps thermal jitter in 0.35 um CMOS
- Timing errors: before cal 10 ps rms, after cal 0.8 ps rms

US 6,956,423 "Interleaved clock signal generator having serial delay and ring counter architecture", Oct 2005, Robert Neff

4-GSa/s 8-bit ADC Results

	CMOS ADC	CMOS vs bipolar
Sample Rate	4 GSa/s	same
Resolution	8 bits	1 bit more
SNDR	7.0 effbits	0.5 bit more
BW	1 GHz	50%
Interleave	32-way	16x more
Transistors	300K	100x
Area	28 mm^2	~75%
Power	4.6 W	1/3
Cost		1/5



0.35-um CMOS
7.1 mm x 4.0 mm
300,000 FETs
4.6 W

"A 4-GSample/s 8b ADC in 0.35-um CMOS", Ken Poulton, Robert Neff, Art Muto, Wei Liu, Andy Burstein, Mehrdad Heshami, ISSCC, pp 166-167, Feb 2002

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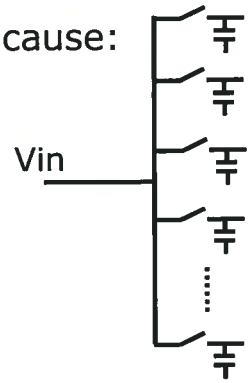
Issue: Coping With Wide Inputs

- Many parallel samplers connected to Vin cause:
  - High capacitance, e.g., 2 pF
  - Physical distribution challenges
    - Binary tree has matched lengths, but much more C
- Approaches:
  - Lower the source impedance
    - e.g., 25 ohms Rin
    - Add a buffer amplifier
  - Reduce the sampler count connected to Vin
    - Each sampler feeds multiple ADC slices
    - Each sampler feeds multiple second-rank samplers



Issue: The Digital Firehose

- Current gigasample ADCs spew out 4 to 500 Gb/s
  - I/O power can be as much as ADC power
- Separate Receiver Chip
  - FPGAs with 50+ SerDes can cost $1000's apiece
  - Custom data capture chips cost millions for design
    - Much lower power and per-chip cost
- On-chip storage
  - Can reduce system cost and power
  - Limited memory size
    - Reduces the range of products possible
  - Slower readout leads to ~90+% deadtime
- On-chip DSP
  - Can reduce the data rate by 2-10x for applications such as datacomm

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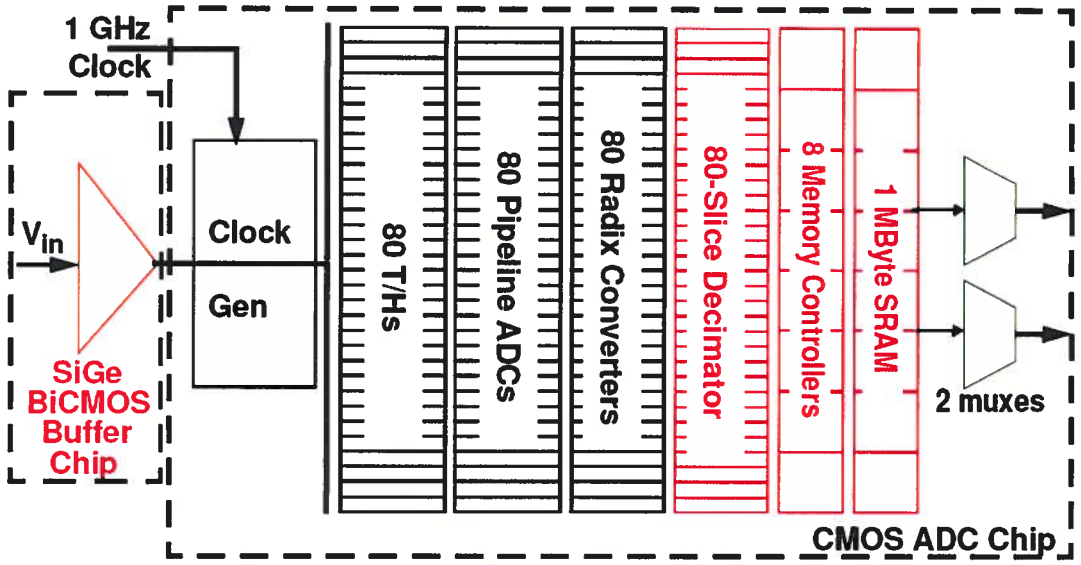
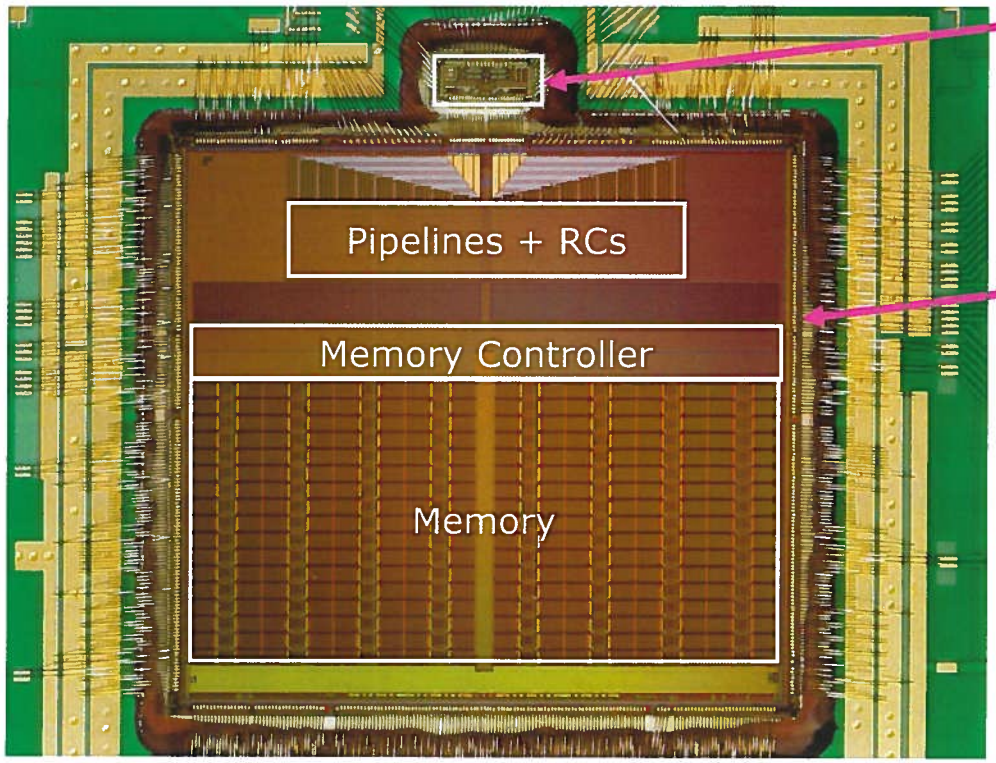
2003: 20-GSa/s 8-bit ADC, 0.18 um CMOS



- 2x faster process, 5x higher sample rate, 6x higher BW
- 80 ADC slices, larger Cin --> SiGe input buffer chip
- 160 Gb/s data rate --> 1 MB on-chip sample memory

"A 20 GS/s 8 b ADC with a 1 MB memory in 0.18-um CMOS", Poulton, Neff, Setterberg, Wuppermann, Kopley, Jewett, Pernillo, Tan, Montijo, ISSCC, pp 318-319, Feb 2003

20 GSa/s ADC Module



Buffer:
40 GHz SiGe
1 x 2 mm
1000 transistors
1 W

ADC:
0.18-um CMOS
14 x 14 mm
50M transistors
9 W

Package:
438-ball BGA
35 x 35 mm

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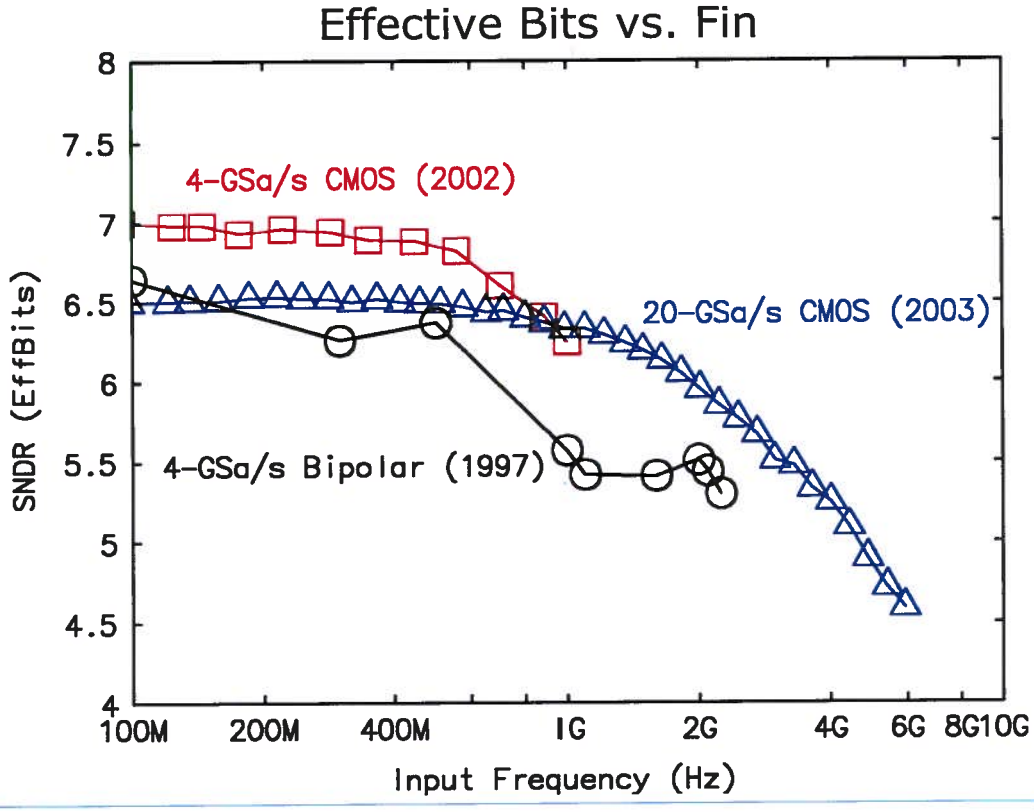
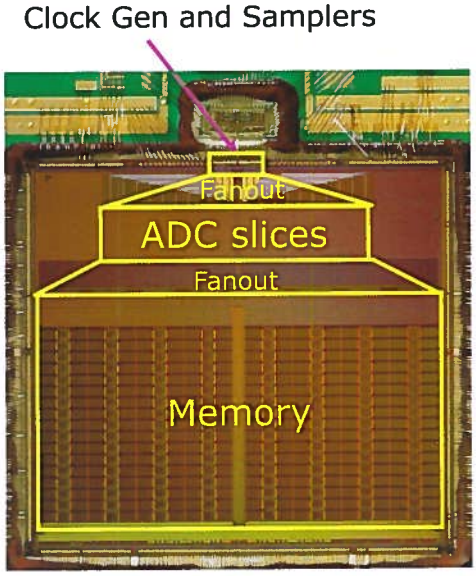
Performance of Bipolar and CMOS ADCs



Issue: Clock and Signal Distribution

- Multiple samplers requires distributing clocks
- Tradeoff between dense samplers and larger size of the ADC slices
- Both clock and analog signal distribution can take a lot of area and power
- Example: 80-slice ADC:
  - samplers: 1.9 mm wide
  - ADCs: 9 mm
  - Memory 13 mm



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Other Issues for Massive Interleaving

- Frequency-dependent mismatch
  - Small BW mismatches can be mostly corrected as timing mismatches
  - Larger BW or rolloff shape mismatches won't work this way
    - Electromagnetic modeling of Vin distribution network
    - Digital time-varying filter can provide correction **
- Kickback into analog input
  - When a T/H reconnects to the input, kickback (from previous sample) is injected into the input network
    - Can cause an "echo" from ~N samples earlier
    - Can create a high-slew disturbance while another T/H is sampling
- Crosstalk among slices
  - Power supplies and shared bias lines
  - Clock networks
  - Analog sample fanouts

** "A Polynomial-Based Time-Varying Filter Structure for the Compensation of Frequency-Response Mismatch Errors in Time-Interleaved ADCs", Johansson, IEEE Sig Processing, 2009

Time Interleaving for High Dynamic Range

- Application area: RF receivers
- Key Specs for instruments

	Scopes	*RF Instruments*
SFDR	40-50 dB	60-80 dB
SNR	~7 bits	~10 bits
BER**	1/year	1/year

Peak Detector in spec Analyzer → Make sure ADC does not produce such errors.

** BER = Bit Error Rate = Metastable Error Rate

- Instruments require very low rates, e.g., 10^{-17}
  - Due to peak detect mode
- Communications channels can allow rates as high as 10^{-8}
  - Use of DSP and error correction

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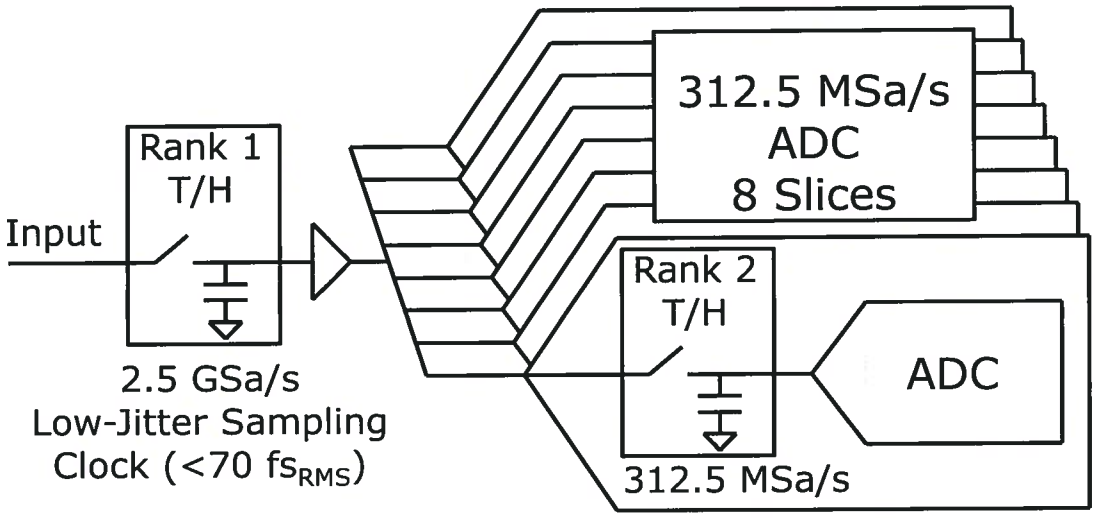
A 14-bit 2.5-GSa/s 8-Way-Interleaved ADC

Goals and resulting design decisions

- 10^{-17} Metastable error rate
  - Interleaved
  - Low slice sample rate (312.5 MSa/s), 8 slices
- 80 dB SFDR
  - Single full-rate first sampler to suppress timing mismatch
  - Background calibration for gain and offset mismatch
  - Digital Dynamic Linearity Corrector (DLC)
- 60 dB SNR
  - Background calibration for pipeline inter-stage gain parameters
- No assumptions about input signal
  - Background cal injects its own dither signals

"A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction", Setterberg, et al, ISSCC 2013

Minimize Sampling Time Errors with a 2-rank Track and Hold



- Sample timing defined by first T/H

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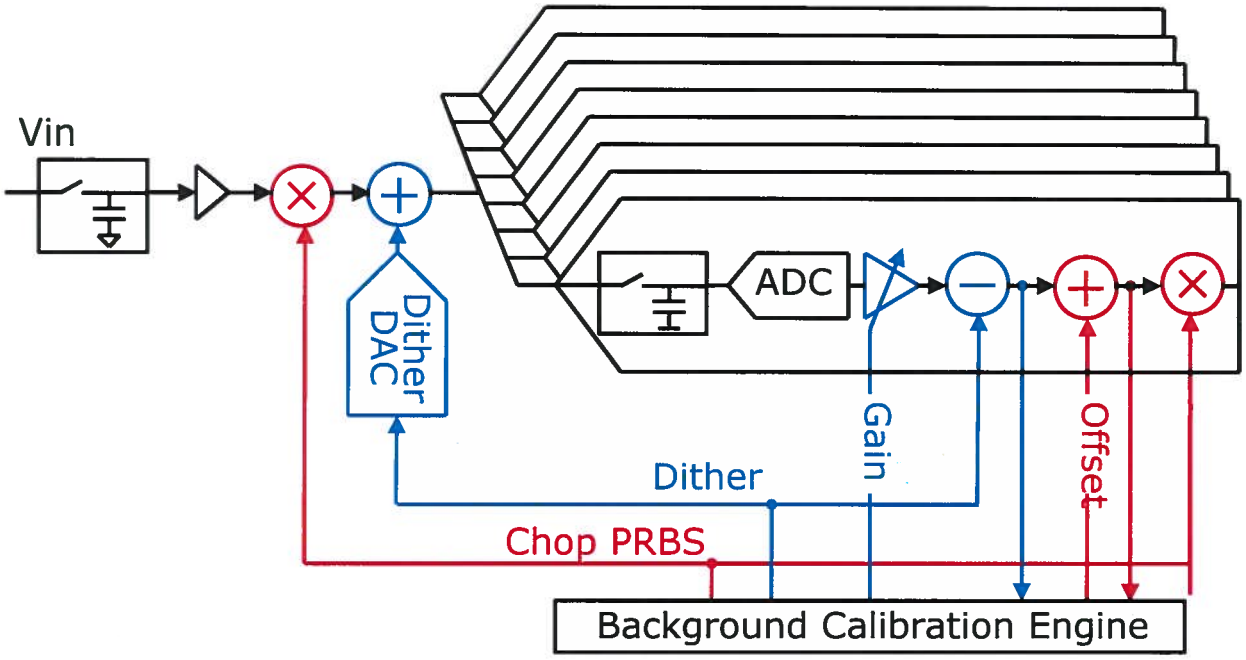
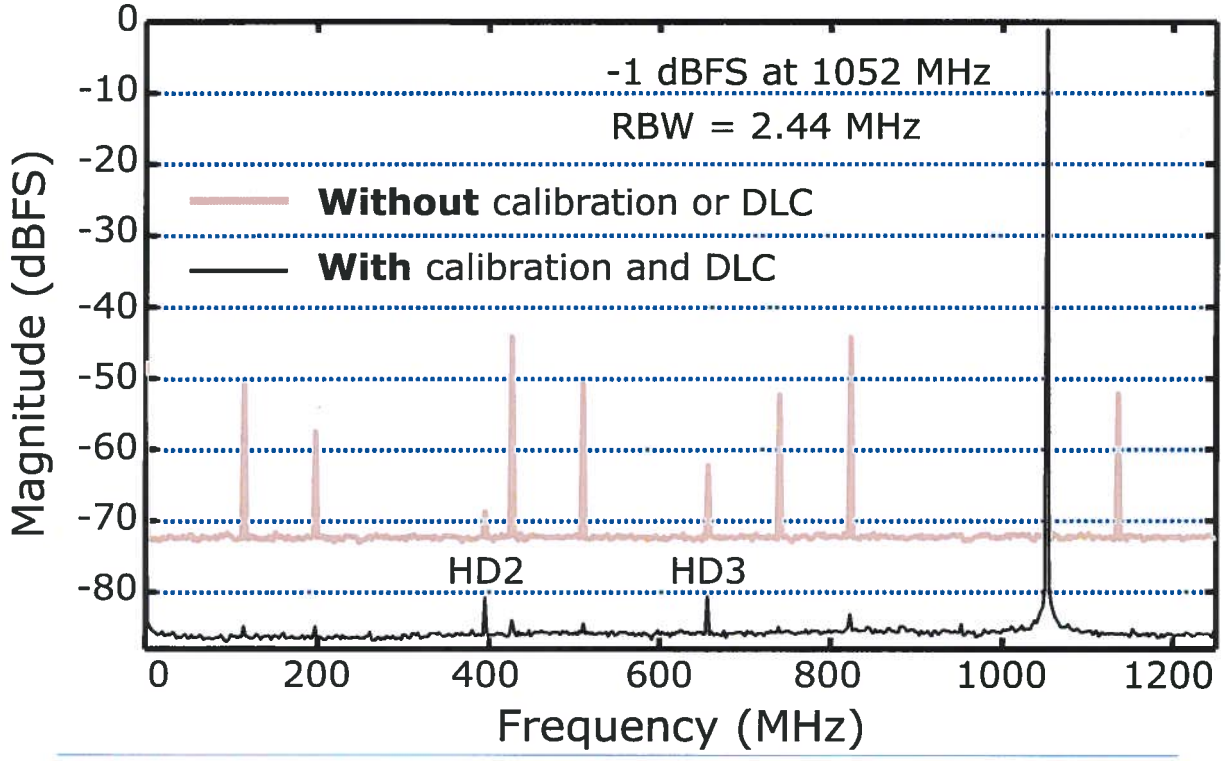
Slice-to-Slice Gain & Offset Alignment



- Injected dither provides an absolute gain reference
- Chopping allows offset calibration
- Both are independent of the input signal

Power Spectrum



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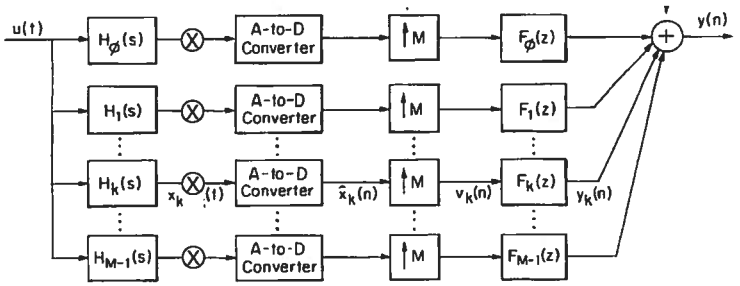
Frequency Interleaving (Early 90's)



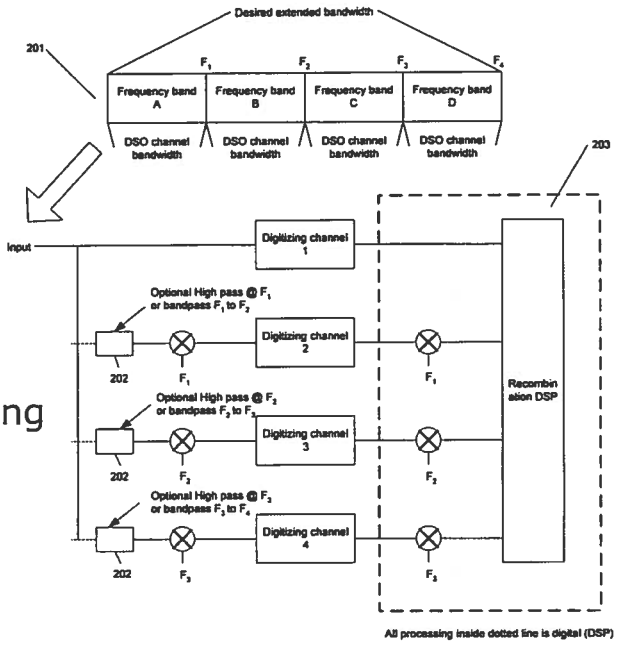
- Basic Idea
  - Use filters to separate input into one frequency band per channel
  - Mix each channel down to baseband
  - Perform A/D Conversion and combine channels
- Pros and cons vs. time interleaving
  - + Reduced jitter sensitivity for ADC clocks
  - + Some ADC noise and distortion can be filtered out after the ADC
  - -- Filters and mixers don't integrate well
  - -- Tricky to align band edges, especially in phase

"High speed A/D Conversion using QMF banks", A Petraglia, S.K. Mitra, ISSCC 1990

"System for converting a signal between continuous-time and discrete-time", US 5568142, Velazquez, Nguyen, Broadstone, Oct 1994

First Frequency Interleaving Product

LeCroy SDA 11000 2005
- Two 6-GHz slices
- 2-way frequency interleaving
- 11 GHz, 40 GSa/s



"High bandwidth real-time oscilloscope", US 7058548, Peter J. Pupalaikis, David C. Graef, June 2006

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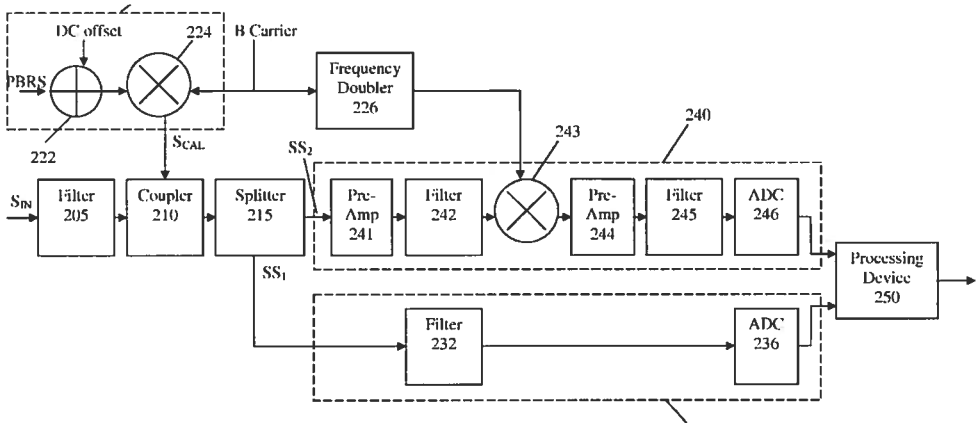
Cal Methods for Frequency Interleaving

- LeCroy describes using phase-locked tone(s) in crossover region
  - foreground cal
- Keysight describes using a PRBS comb in the crossover region
  - allows background cal

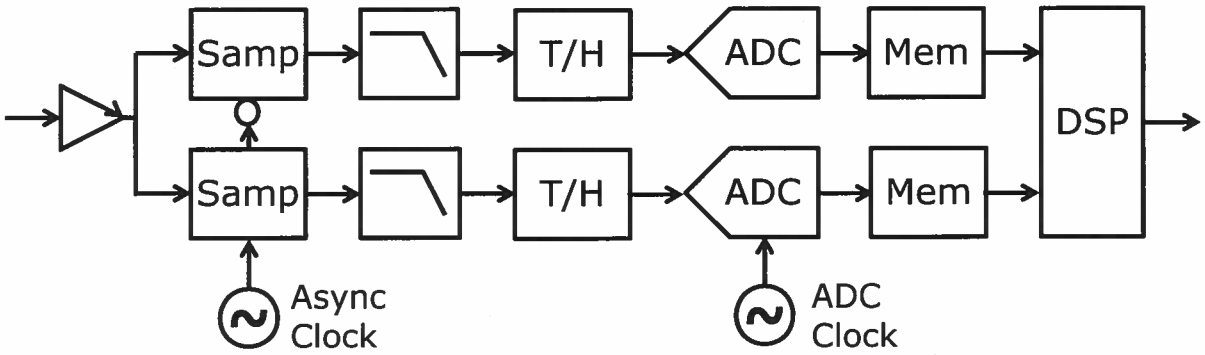


"Method of crossover region phase correction when summing signals in multiple frequency bands", US 7711510, Pupalaikis, et al, May 2010
"Calibrating reconstructed signal using multi-tone calibration signal", US 8849602, Ken Nishimura, Ken Rush, Oct 2014

High End Products

☐ Keysight	63 GHz BW	2-way freq int	Shipped in 2012
☐ LeCroy	100 GHz BW	3-way freq int	2015?
☐ Tek	70 GHz BW	2-way ATI	2015?

☐ Tek Asynchronous Time Interleaving (ATI):
- Upper-half frequencies are aliased into two baseband channels with two phases of an asynchronous clock.



"Techniques for Extending Real-Time Oscilloscope Bandwidth", tek.com, 2013

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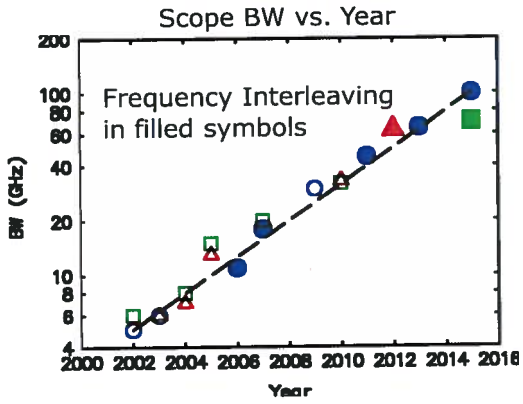
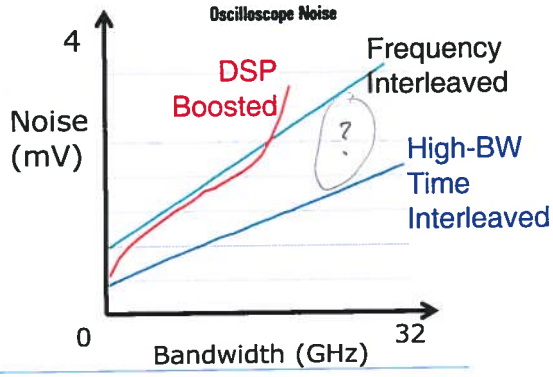
Frequency Interleaving in Scopes

- Scope BW bandwidth has been doubling every 2.8 years
  - Frequency interleaving hasn't changed that
- Cost of high-end scopes near $10K/GHz/2-channels for 10 years
  - Due to small volumes, increasing scope complexity and increasing chip NRE
- In 30 GHz oscilloscopes, the time-interleaved scope had substantially lower noise than the frequency-interleaved scope.
  - Comparative data not available for the 60+ GHz scopes yet





Why gap? Not sure!

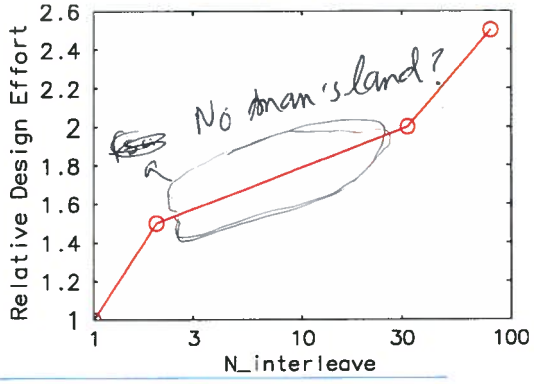
Overhead Factors for Interleaved ADCs

- Power:
  - Power in ADC slices can be a fraction of total ADC power
  - Example: 32-way, 4-GSa/s ADC

32 ADC slices	1.6 W	38%
Samplers + clocks	0.9 W	21%
Multiplexors and outputs	1.7 W	41%
Total	4.2 W	

- Design Overhead:
  - More optimization variables
  - More circuits that interact
  - More clocks
  - V_{IN} and clock distribution
  - Data collection and multiplexing
  - Calibration
  - Optional: Memory and/or DSP

Historical Data:
Relative Design Time vs. Interleave Factor



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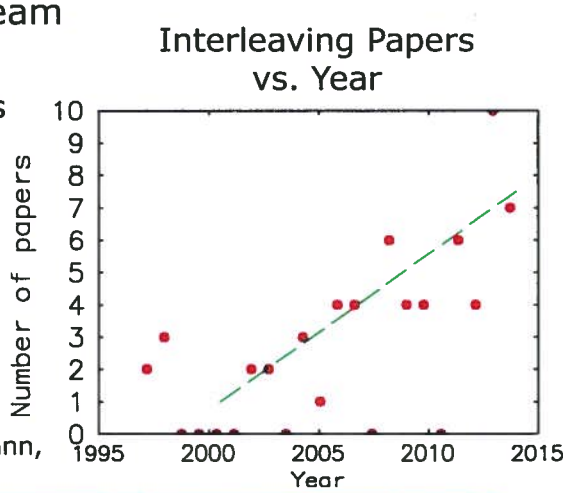
Interleaved ADC Trends

- Much more power-efficient core slices
  - Power-Efficiency FOM has dropped by ~10x since 2002
  - Use of interleaving has propelled SARs to prominence
- More background cal
  - Making the transition from academia to industry
- Interleaving has become mainstream
  - Lots of papers at ISSCC
  - Massive interleaving for 12+ Gb/s wireline link products
  - Becoming "just another ADC topology"



"ADC Performance Survey 1997-2014", B. Murmann, web.stanford.edu/~murmann/adcsurvey.html

The Future for Interleaved ADCs

- When will all ADCs be interleaved?

  Never!
  - Design complexity
  - Overhead for power and design time
- The Skyrocketing Price of Moore's Law
  - Interleaving decouples process choice from sample rate requirements

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Highly Accurate Adaptive Digital Calibration for High-Speed High-Resolution Time-Interleaved ADC

Takashi Oshima
Hitachi Ltd., Central Research Laboratory

ISSCC 2015 Forum

Outline

1. Introduction of time-interleaved ADC
2. Calibration of time-interleaved ADC assisted by reference converter
3. Calibration of higher-order effects of sampling-timing mismatch
4. Calibration of bandwidth mismatch
5. Differentiators for timing calibration
6. Extension to sub-sampling time-interleaved ADC
7. Measurement results
8. Summary and conclusion

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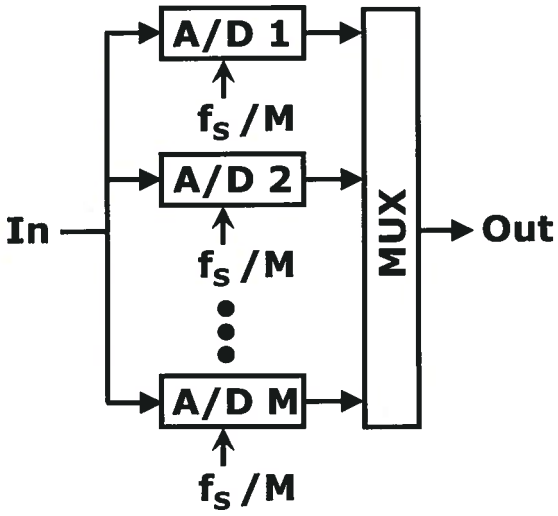
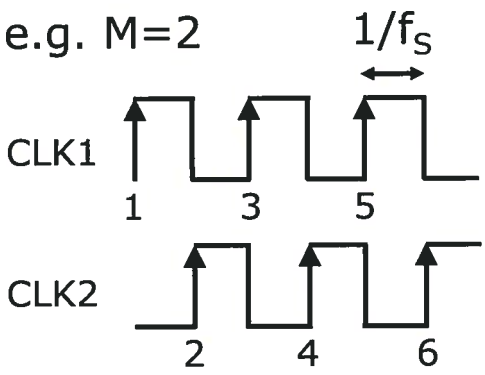
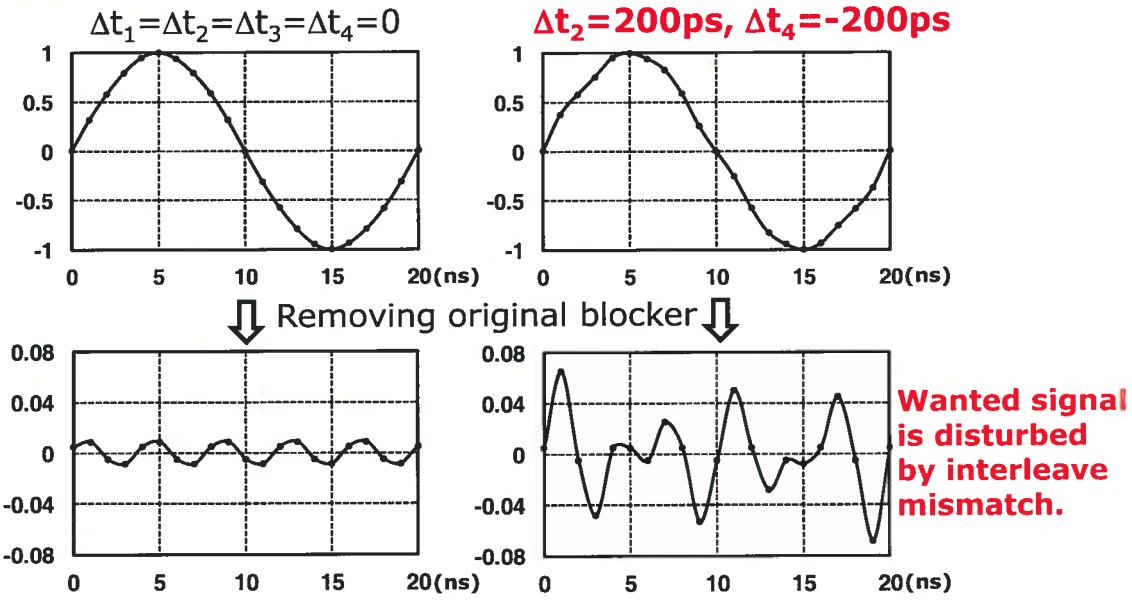
1-1 Operation of time-interleaved ADC





- Interleaving M converters achieves M-times faster sampling rate.

1-2 Interleave mismatch in time domain



e.g. 1% 250-MHz wanted signal and 99% 50-MHz blocker converted by 1-GS/s 4-way time-interleaved ADC

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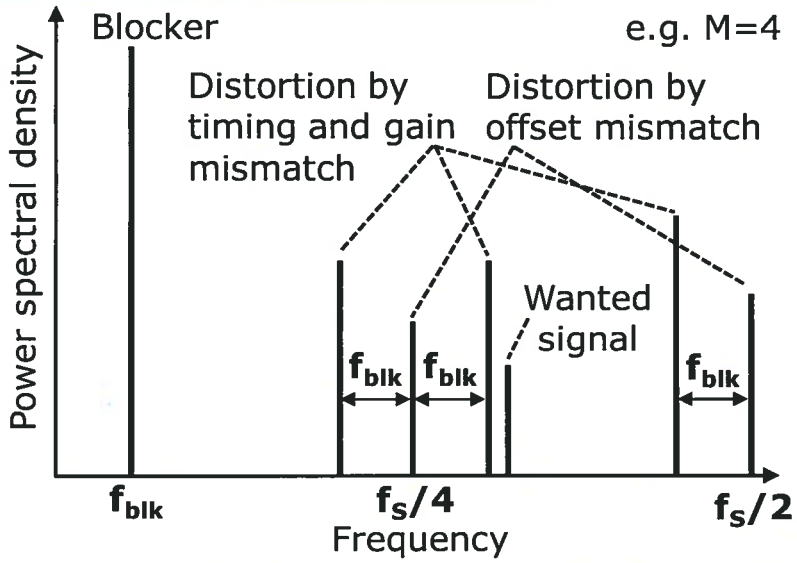
1-3 Interleave mismatch in spectral domain



- Mismatches among unit converters generate distortion tones at $N/M*f_S-f$, $N/M*f_S+f$ and $N/M*f_S$ (f: input frequency, N: integer).
- Wanted signal is disturbed by interleave tone of large blocker.

Outline

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4. Calibration of bandwidth mismatch
5. Differentiators for timing calibration
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8. Summary and conclusion

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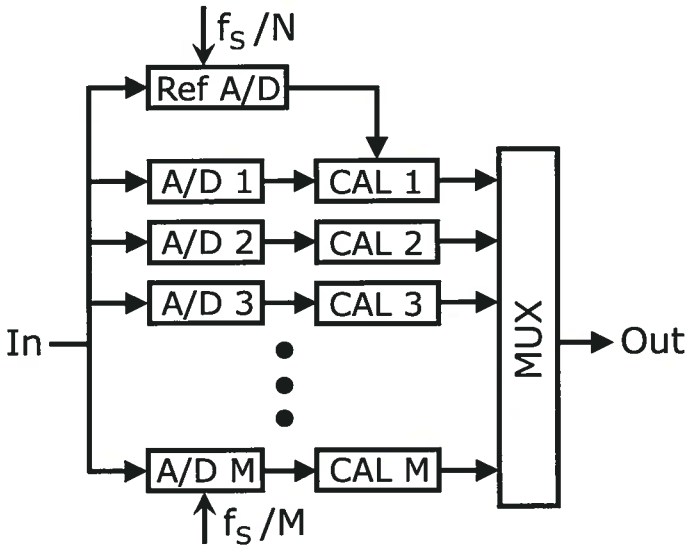
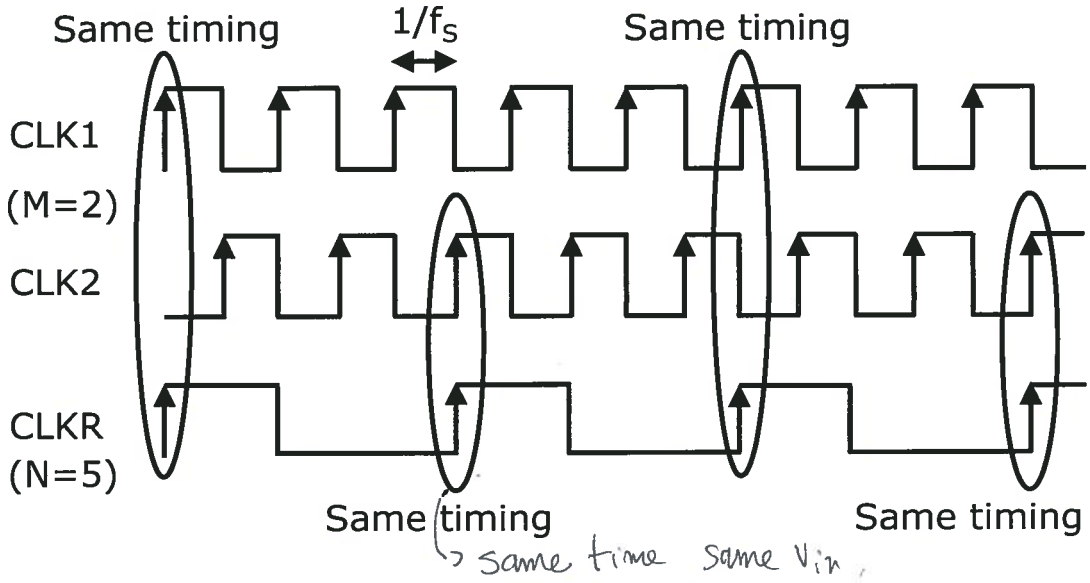
2-1 Post digital calibration assisted by reference converter



- Using reference converter output, each CAL block compensates mismatch of unit converter.
- M and N are selected not to have a common divisor.

M=2 → Two ADC

2-2 Timing chart of operation



- Each converter can 'meet' reference converter periodically.

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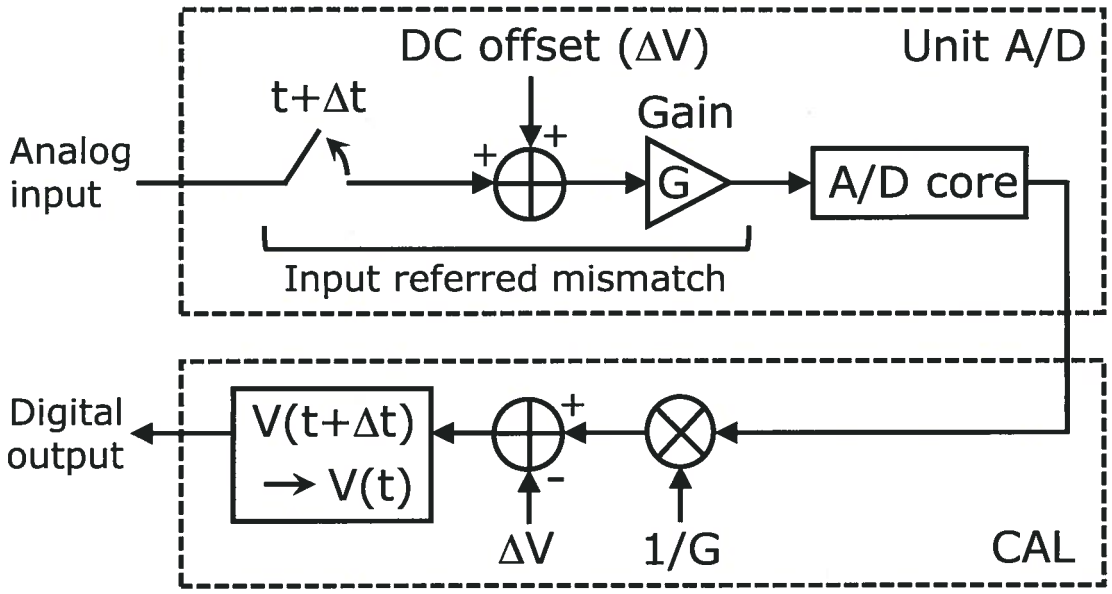
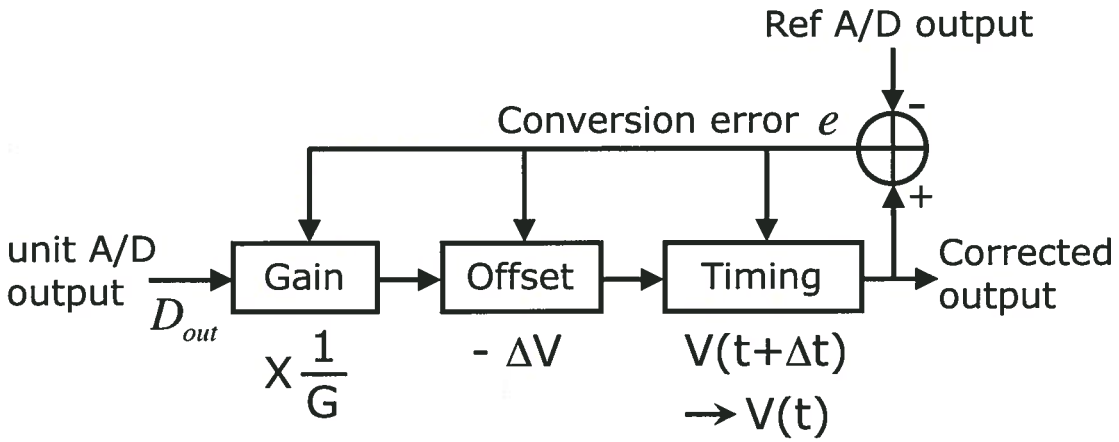
2-3 Modeling of operation



- CAL compensates analog degradation in reverse.

2-4 Adaptive calibration



$$(1/G)_{NEW} = (1/G)_{OLD} - \mu_G \cdot e \cdot D_{out}$$

$$\Delta V_{NEW} = \Delta V_{OLD} + \mu_{\Delta V} \cdot e \qquad \Delta t_{NEW} = \Delta t_{OLD} + \mu_1 \cdot \frac{dV}{dt} \cdot e$$

- Mismatch parameters are searched by LMS algorithm.

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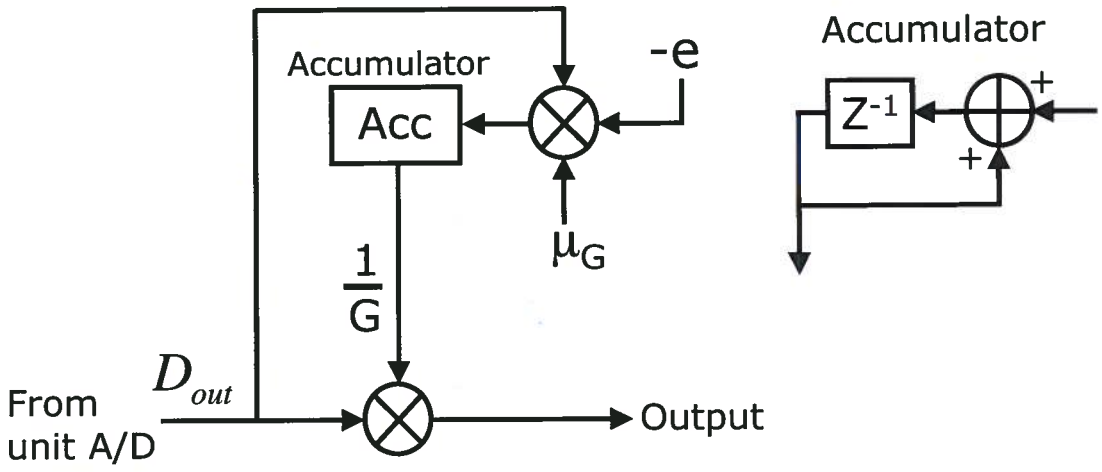
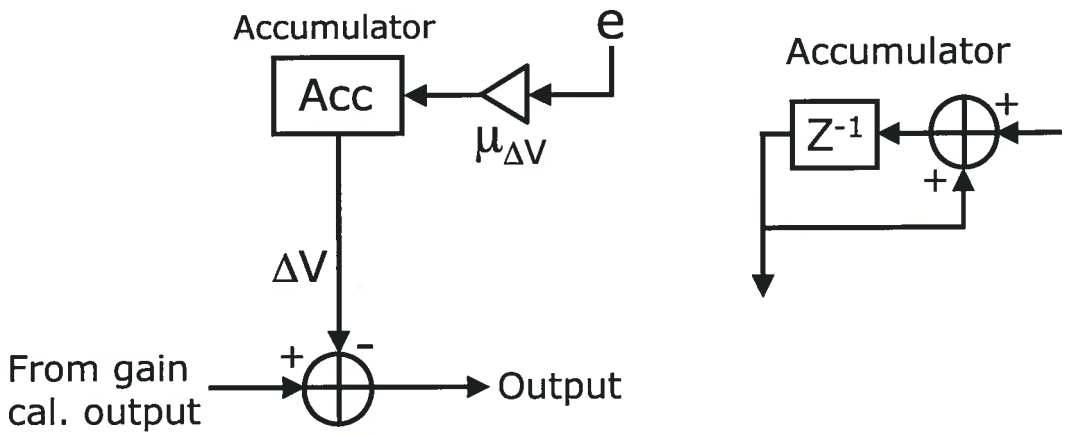
2-5 Calibration of gain mismatch



$$(1/G)_{NEW} = (1/G)_{OLD} - \mu_G \cdot e \cdot D_{out}$$

2-6 Calibration of DC-offset mismatch



$$\Delta V_{NEW} = \Delta V_{OLD} + \mu_{\Delta V} \cdot e$$

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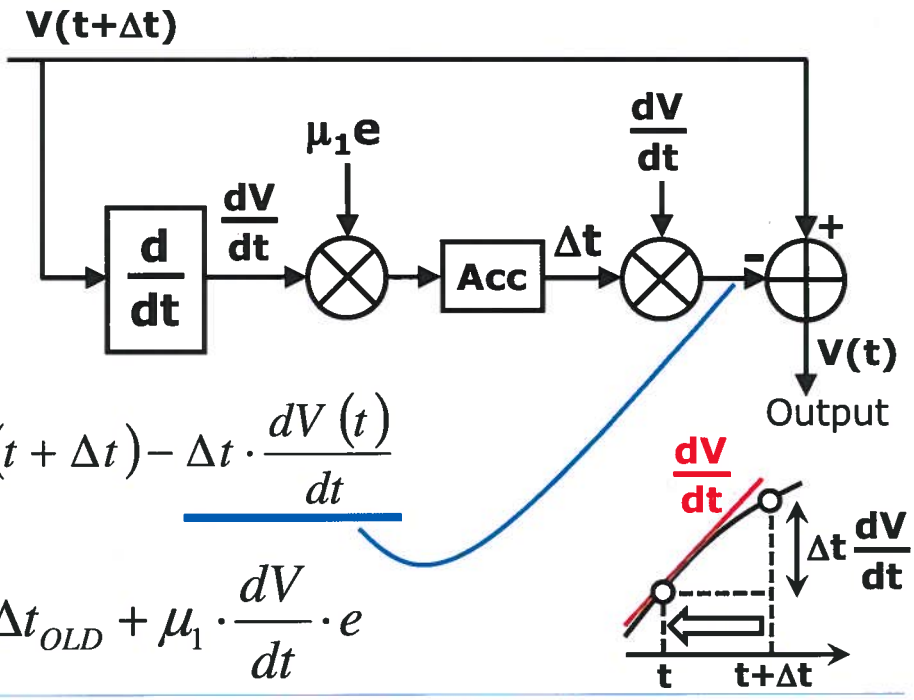
2-7 Calibration of sampling-timing mismatch

From offset cal. output



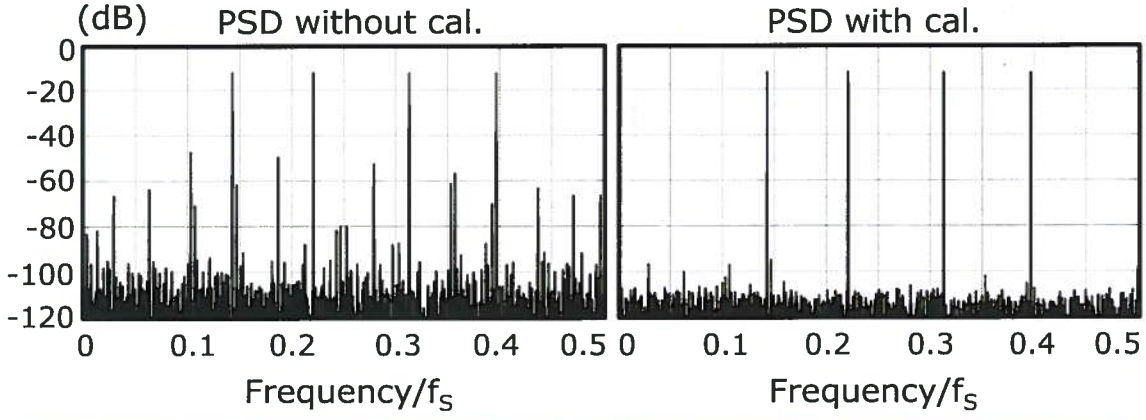
$$V(t) \approx V(t+\Delta t) - \Delta t \cdot \frac{dV(t)}{dt}$$

$$\Delta t_{NEW} = \Delta t_{OLD} + \mu_1 \cdot \frac{dV}{dt} \cdot e$$

2-8 Simulation results: Spectrum

f_S=4GHz, M=4, N=5 with 25-Tap FIR differentiator

A/D1: G=1.02, ΔV=-0.003FS, Δt=0.004/f_S
A/D2: G=0.97, ΔV=0.002FS, Δt=-0.006/f_S
A/D3: G=1.04, ΔV=-0.004FS, Δt=0.008/f_S
A/D4: G=0.99, ΔV=0.001FS, Δt=-0.010/f_S



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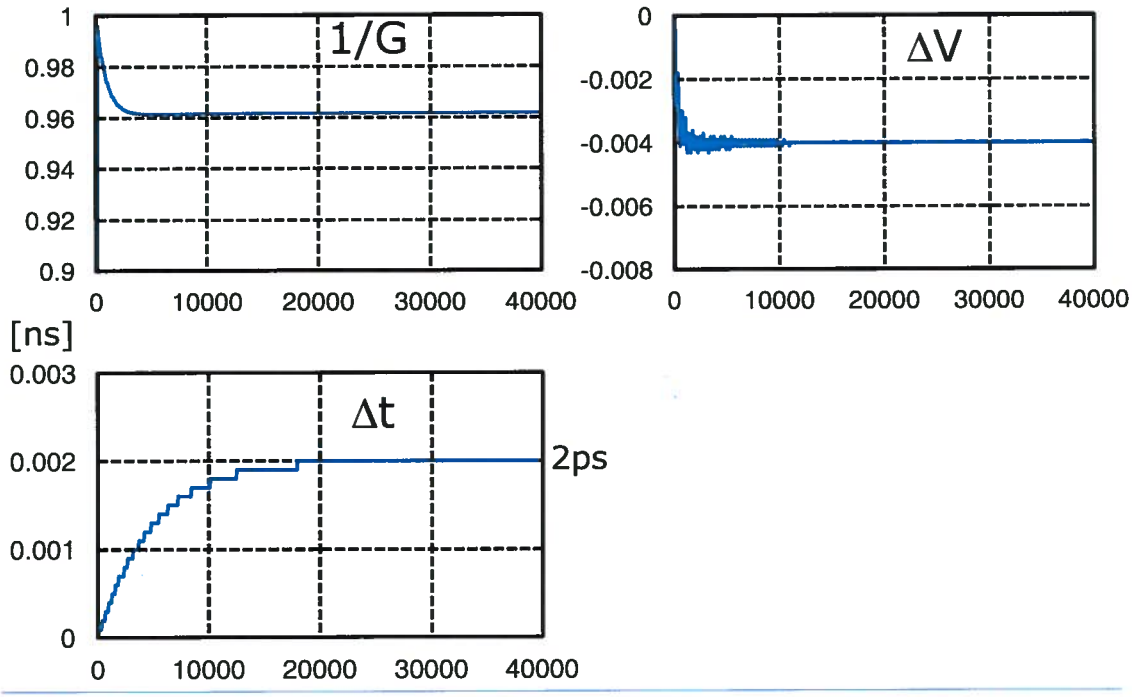
2-8 Simulation results: CAL3 convergence



Outline

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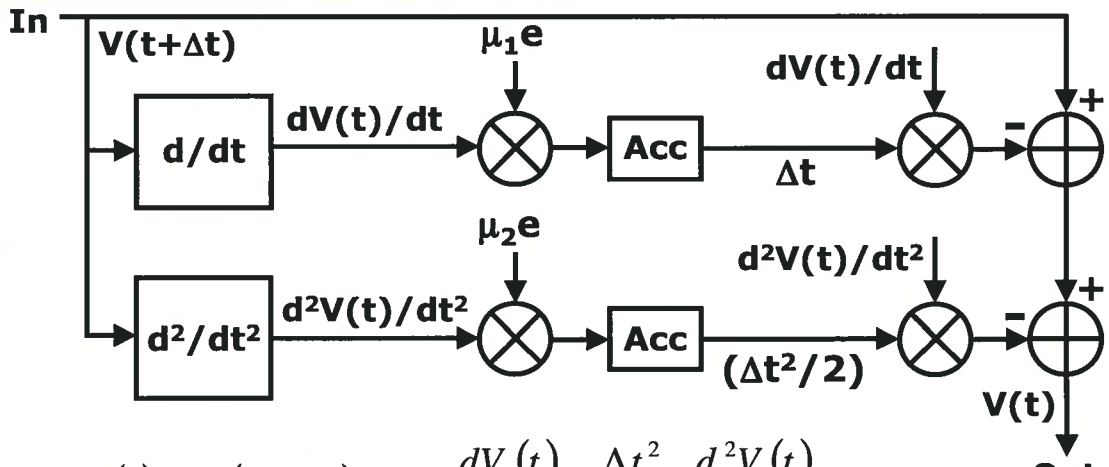
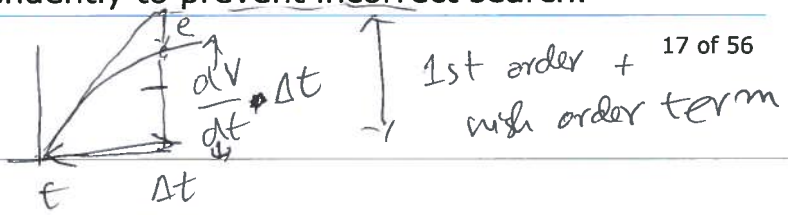
3-1 2nd-order sampling-timing calibration



$$V(t) \approx V(t+\Delta t) - \underbrace{\Delta t \cdot \frac{dV(t)}{dt}}_{1^{st}\text{ order term}} - \underbrace{\frac{\Delta t^2}{2} \cdot \frac{d^2V(t)}{dt^2} - \ldots}_{\text{Higher-order terms}}$$

- Higher-order parameters (Δt^2, Δt^3,...) of sampling-timing mismatch are searched independently to prevent incorrect search.



3-2 Independent LMS search

- Each order of timing mismatch is searched independently.

$$\Delta t_{NEW} = \Delta t_{OLD} + \mu_1 \cdot \frac{dV}{dt} \cdot e$$

$$\left(\frac{\Delta t^2}{2}\right)_{NEW} = \left(\frac{\Delta t^2}{2}\right)_{OLD} + \mu_2 \cdot \frac{d^2V}{dt^2} \cdot e$$

- For n-th-order calibration, dV/dt must be accurate up-to (n-1)-th order of Δt leading to 'cascaded' calibration.

$$V(t) \approx V(t+\Delta t) - \Delta t \cdot \frac{dV(t)}{dt} - \frac{\Delta t^2}{2} \cdot \frac{d^2V(t)}{dt^2} - \ldots$$

Need to be accurate up-to (n-1)-th order of Δt.

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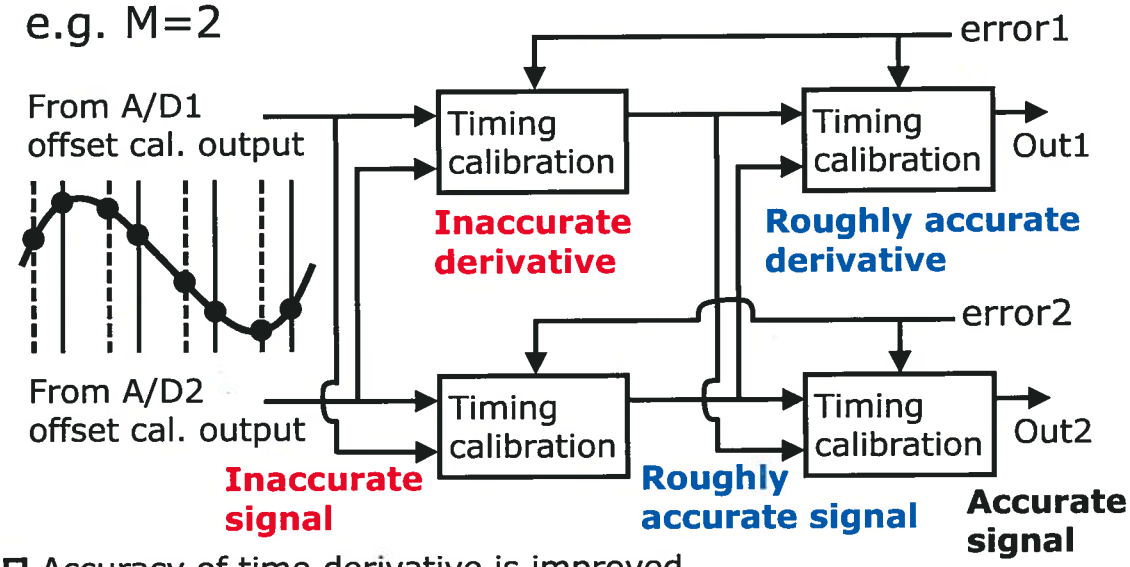
3-3 Cascaded timing calibration

e.g. M=2

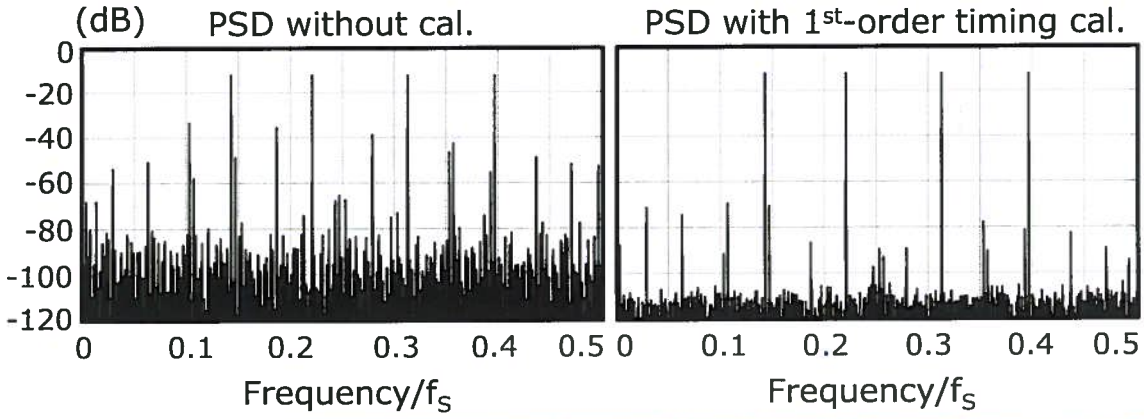


- Accuracy of time derivative is improved by cascading timing-calibration stages.
- N-th-order calibration needs N cascaded stages.

3-4 Simulation results: Spectrum

f_S=4GHz, M=4, N=5
with 25-Tap FIR differentiators & 2 cascaded stages

A/D1: G=1.02, ΔV=-0.003FS, Δt=0.02/f_S
A/D2: G=0.97, ΔV=0.002FS, Δt=-0.03/f_S
A/D3: G=1.04, ΔV=-0.004FS, Δt=0.04/f_S
A/D4: G=0.99, ΔV=0.001FS, Δt=-0.05/f_S



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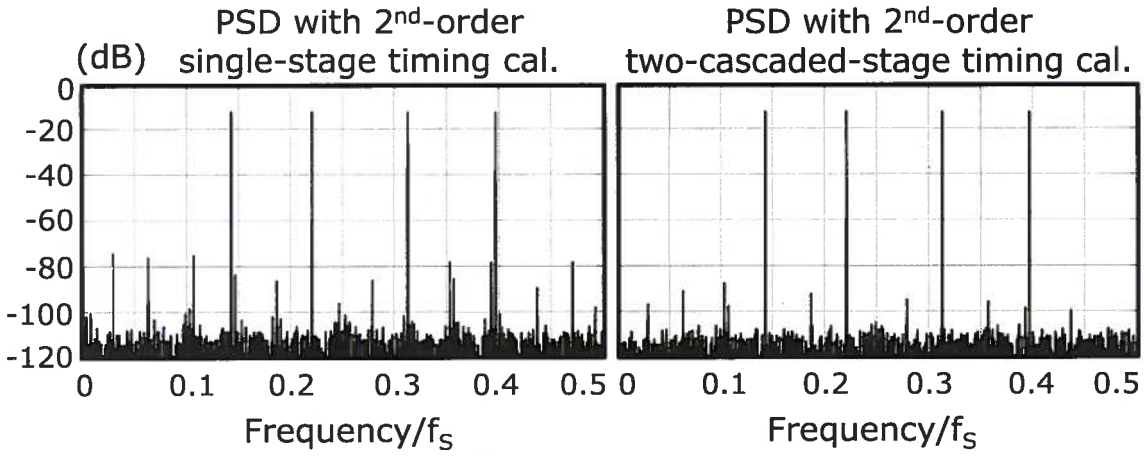
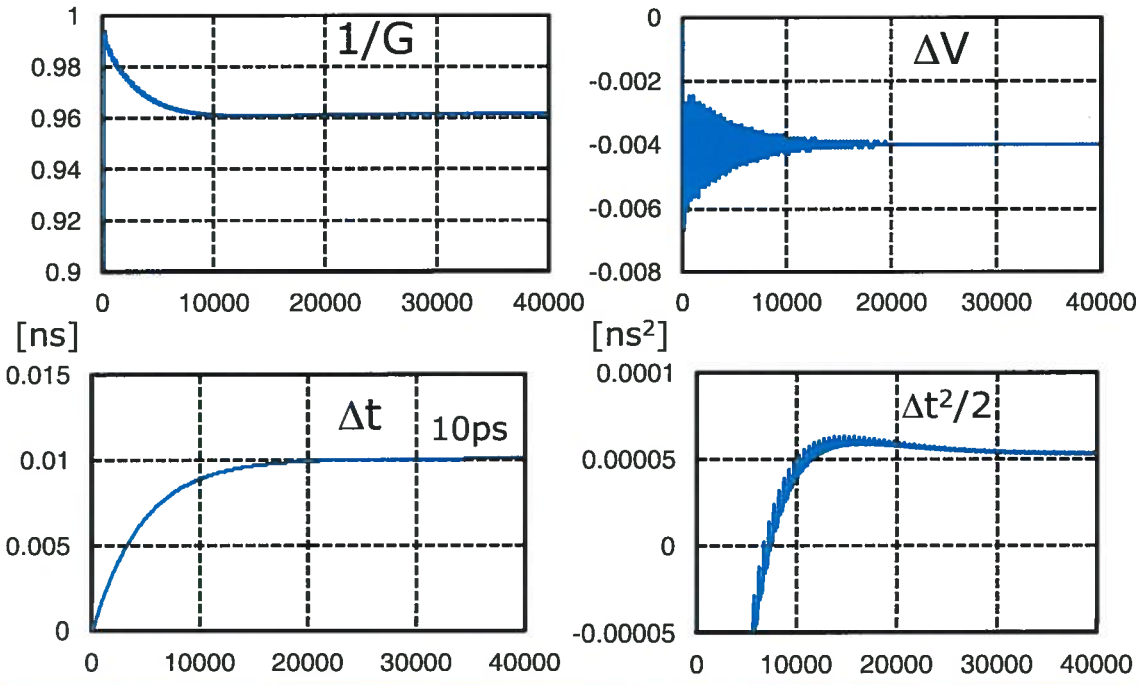
3-4 Simulation results: Spectrum



3-4 Simulation results: CAL3 convergence



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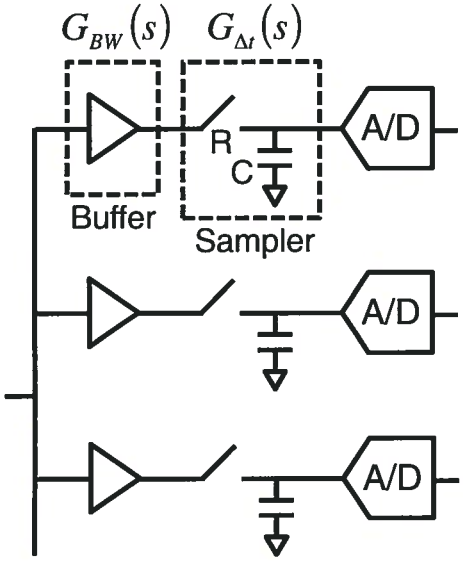
4-1 1st-order pseudo timing mismatch



$$G_{BW}(s) = \frac{1}{1+\frac{s}{\omega_{BW}}} \approx 1 - \frac{s}{\omega_{BW}}$$

$$G_{\Delta t}(s) \approx 1 + \Delta t \cdot \frac{d}{dt} = 1 + \Delta t \cdot s$$

$$G_{BW}(s) \cdot G_{\Delta t}(s) \approx 1 + \left(\Delta t - \frac{1}{\omega_{BW}}\right) \cdot s$$

Δt_{pd}=Pseudo timing mismatch

- Finite bandwidth is equivalent to sampling-timing mismatch.
- The combined effect is regarded as 'pseudo' timing mismatch.

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4-2 2nd-order pseudo timing mismatch

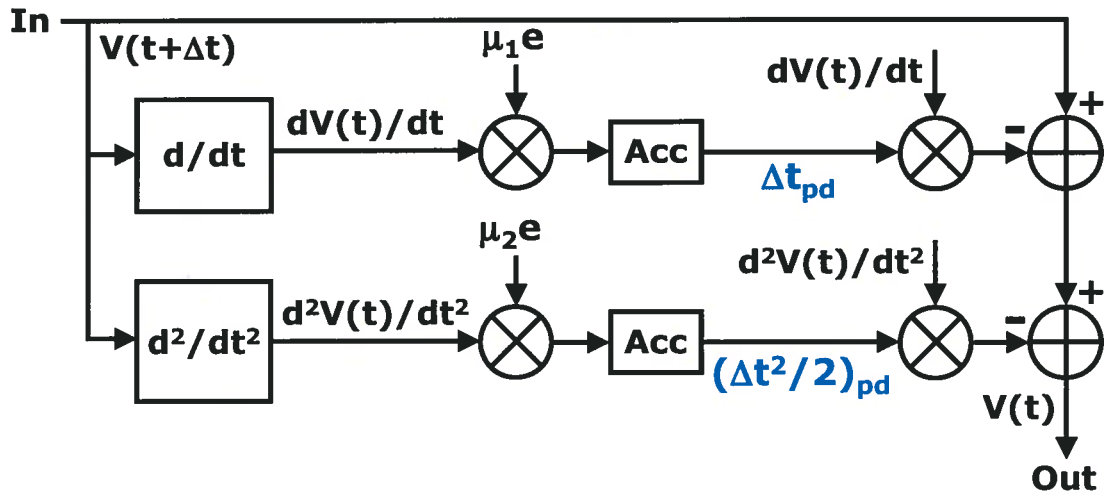
$$G_{BW}(s)\cdot G_{SW}(s)\cdot G_{\Delta t}(s)\approx \frac{1}{1+\frac{s}{\omega_{BW}}}\cdot\frac{1}{1+RC\cdot s}\cdot\left(1+\Delta t\cdot\frac{d}{dt}+\frac{\Delta t^2}{2}\cdot\frac{d^2}{dt^2}\right)$$

$$\approx 1+\Delta t_{pd}\cdot s+\left(\frac{\Delta t^2}{2}\right)_{pd}\cdot s^2$$

$$\begin{cases}\Delta t_{pd}=\Delta t-\dfrac{1}{\omega_{BW}}-RC\\ \left(\dfrac{\Delta t^2}{2}\right)_{pd}=\dfrac{\Delta t^2}{2}-\Delta t\cdot\left(\dfrac{1}{\omega_{BW}}+RC\right)+\dfrac{RC}{\omega_{BW}}+\left(\dfrac{1}{\omega_{BW}}\right)^2+(RC)^2\end{cases}$$

2nd-order pseudo timing mismatch

4-3 2nd-order pseudo-timing calibration



- Same structure corrects 'pseudo' timing mismatch instead of 'pure' timing mismatch.

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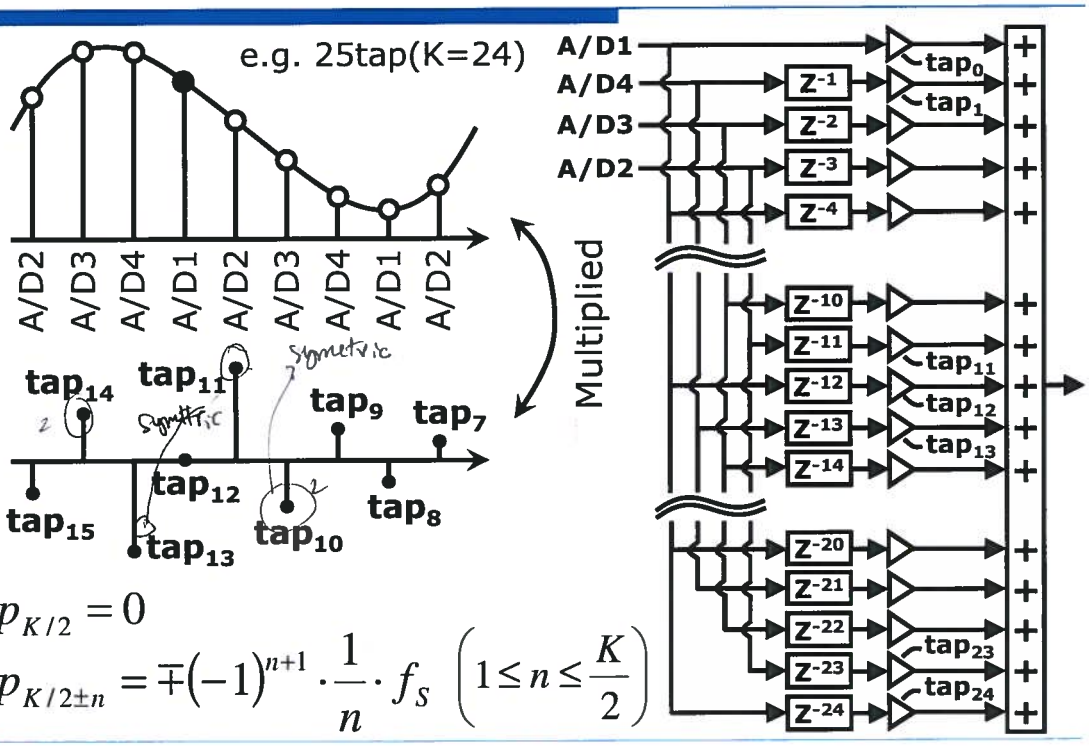
5-1 1st-order FIR differentiator



$$tap_{K/2} = 0$$

$$tap_{K/2\pm n} = \mp(-1)^{n+1} \cdot \frac{1}{n} \cdot f_S \quad \left(1 \le n \le \frac{K}{2}\right)$$

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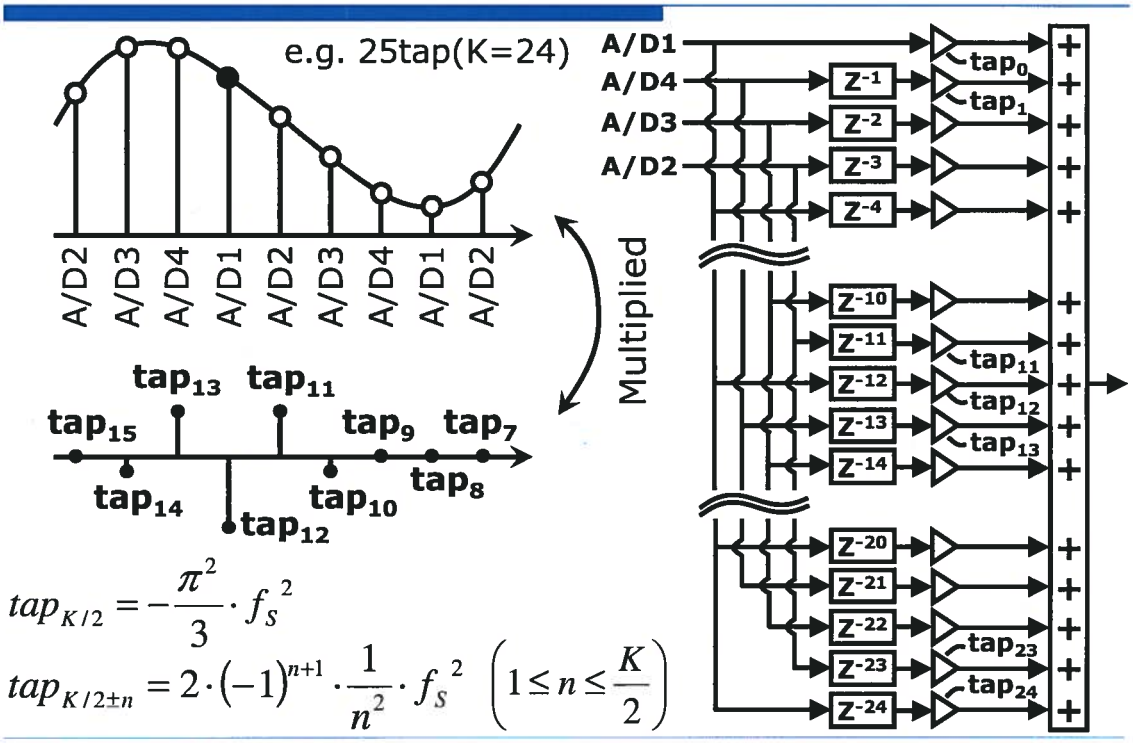
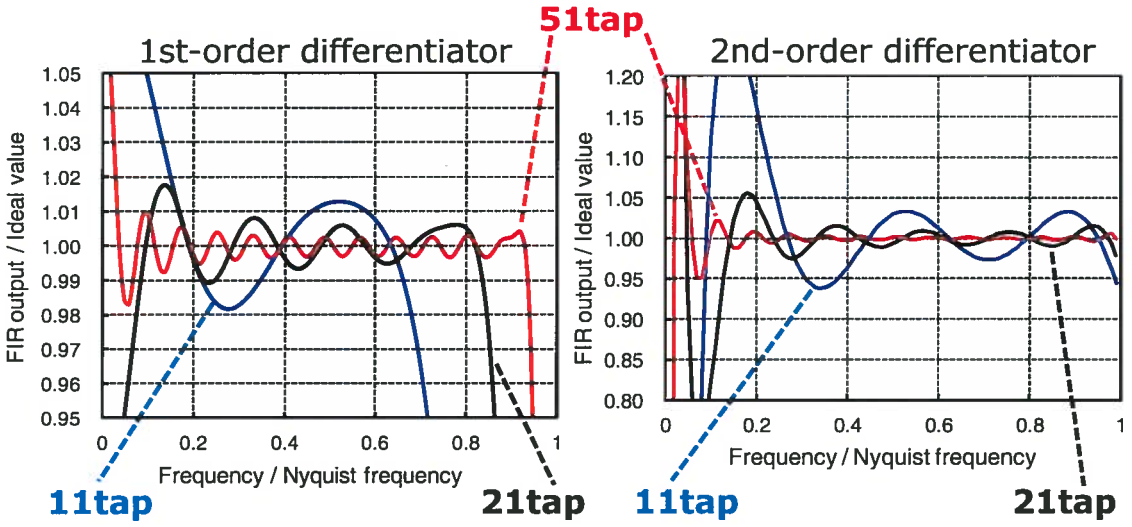
5-2 2nd-order FIR differentiator



$$tap_{K/2} = -\frac{\pi^2}{3} \cdot f_S{}^2$$

$$tap_{K/2\pm n} = 2 \cdot (-1)^{n+1} \cdot \frac{1}{n^2} \cdot f_S{}^2 \quad \left(1 \le n \le \frac{K}{2}\right)$$

5-3 Effect of finite tap counts



- Tap count of around 20 is sufficient.

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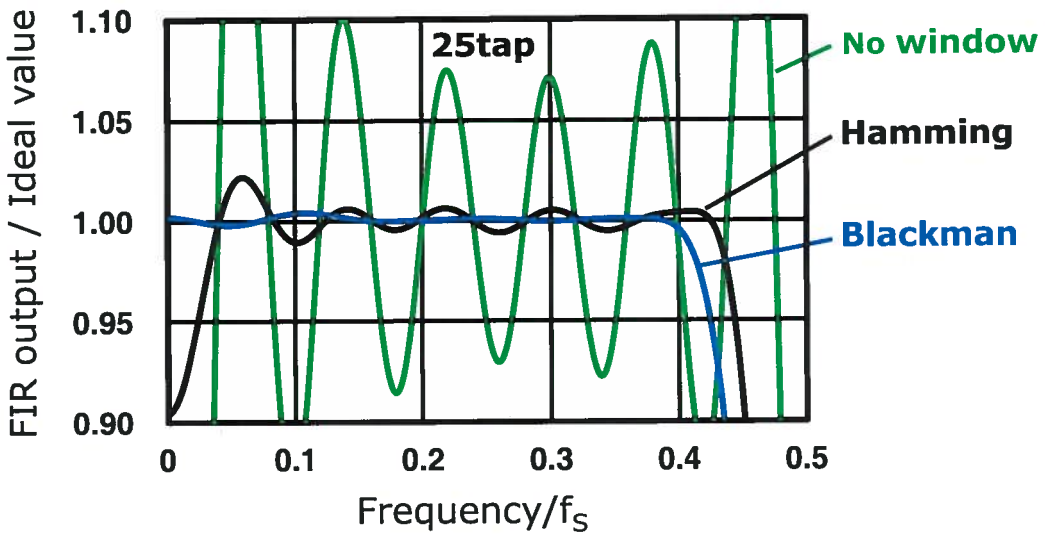
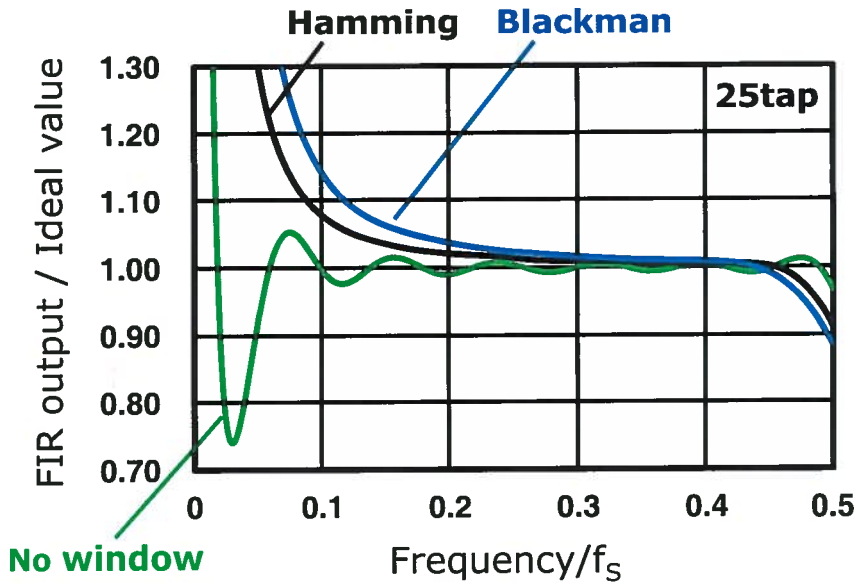
5-4 Effect of window function on 1st-order differentiator



$$tap_{K/2\pm n}^{(final)} = W_{K/2\pm n}^{Hamm} \cdot tap_{K/2\pm n} \qquad W_{K/2\pm n}^{Hamm} = 0.54 - 0.46\cos\left\{2\pi\left(\frac{1}{2} - \frac{n}{K}\right)\right\}$$

5-5 Effect of window function on 2nd-order differentiator



- Window function is not applied for 2nd-order differentiator.

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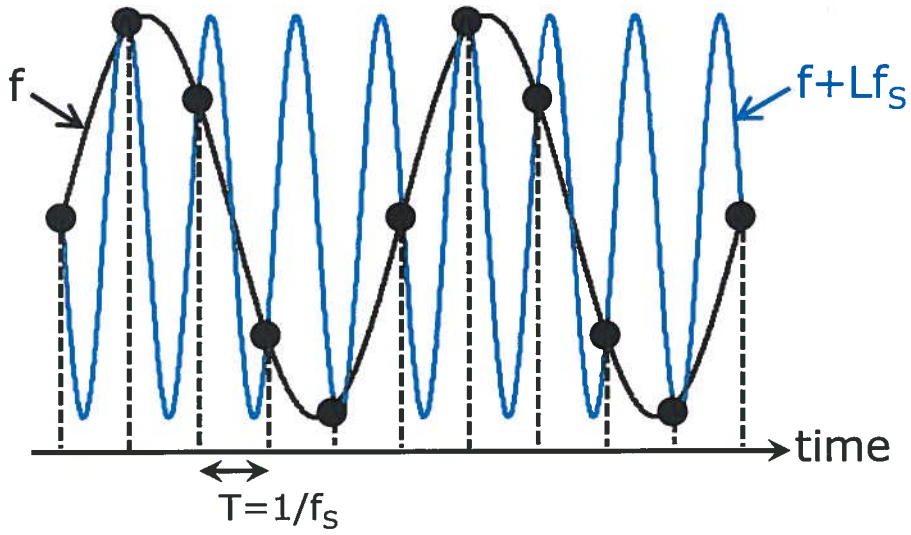
6-1 Frequency conversion by sub-sampling



$$\sin\{2\pi(f + L\cdot f_S)\cdot nT\}$$
$$= \sin(2\pi\cdot f\cdot nT + 2\pi\cdot L\cdot n) = \sin(2\pi\cdot f\cdot nT)$$

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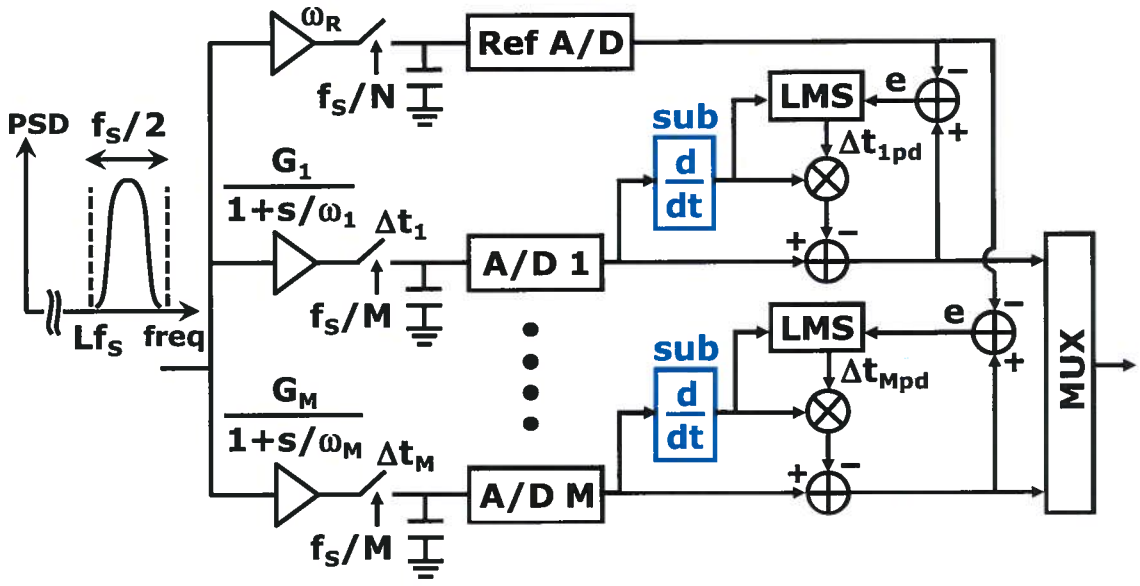
6-2 Sub-sampling time-interleaved ADC



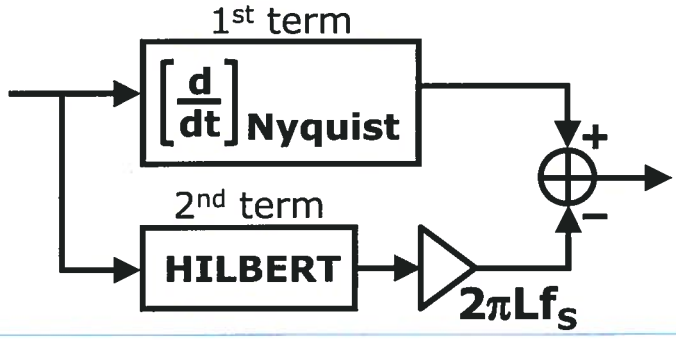
- Same structure can be used with 'sub-sampling' differentiator.

6-3 1st-order sub-sampling differentiator

$$\left(\frac{d}{dt}\sin\{2\pi(f+L\cdot f_S)\cdot t\}\right)_{t=nT}$$

$$=2\pi\cdot f\cos(2\pi\cdot f\cdot nT)+2\pi\cdot L\cdot f_S\cos(2\pi\cdot f\cdot nT)$$

$$=\frac{d}{dt}\sin(2\pi\cdot f\cdot nT)+2\pi\cdot L\cdot f_S\cos(2\pi\cdot f\cdot nT)$$



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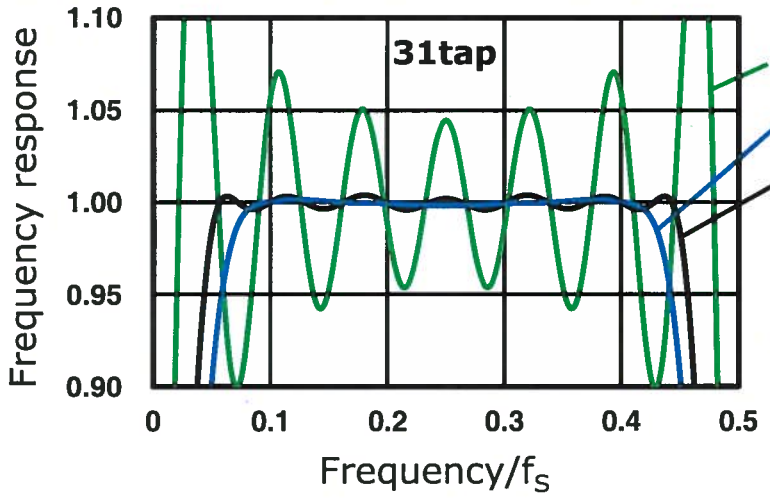
6-4 Hilbert filter for 1st-order differentiator



$$tap_{K/2\pm n}^{(final)} = W_{K/2\pm n}^{Hamm} \cdot tap_{K/2\pm n}^{(HIL)}$$

$$tap_{K/2}^{(HIL)} = 0 \qquad tap_{K/2\pm n}^{(HIL)} = \frac{\pm 2}{\pi \cdot n} \cdot \left\{ \sin\left(\frac{\pi \cdot n}{2} \right) \right\}^2 \quad \left(1 \le n \le \frac{K}{2} \right)$$

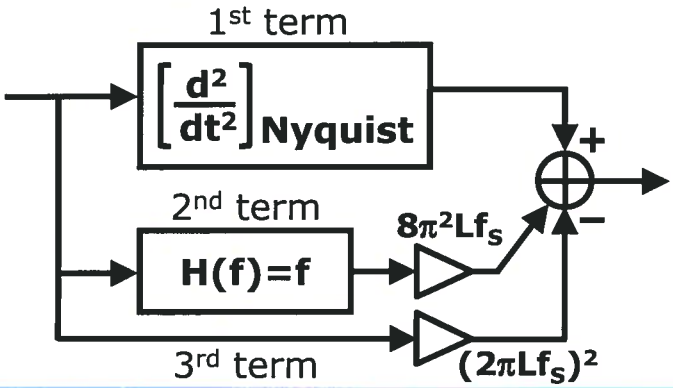
- Hilbert filter converts 'sin' to '-cos'.

6-5 2nd-order sub-sampling differentiator

$$\left(\frac{d^2}{dt^2} \sin\{2\pi(f + L \cdot f_S) \cdot t\} \right)_{t=nT}$$

$$= \underline{\frac{d^2}{dt^2} \sin(2\pi \cdot f \cdot nT)}$$

$$-8\pi^2 \cdot L \cdot f_S \cdot \underline{f \cdot \sin(2\pi \cdot f \cdot nT)} - (2\pi \cdot L \cdot f_S)^2 \underline{\sin(2\pi \cdot f \cdot nT)}$$



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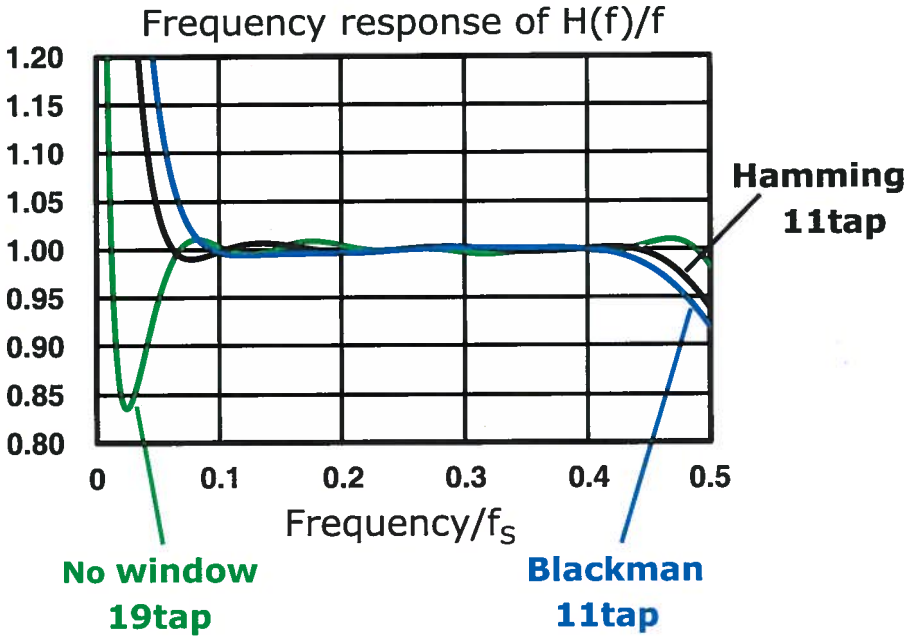
6-6 H(f)=f filter for 2nd-order differentiator

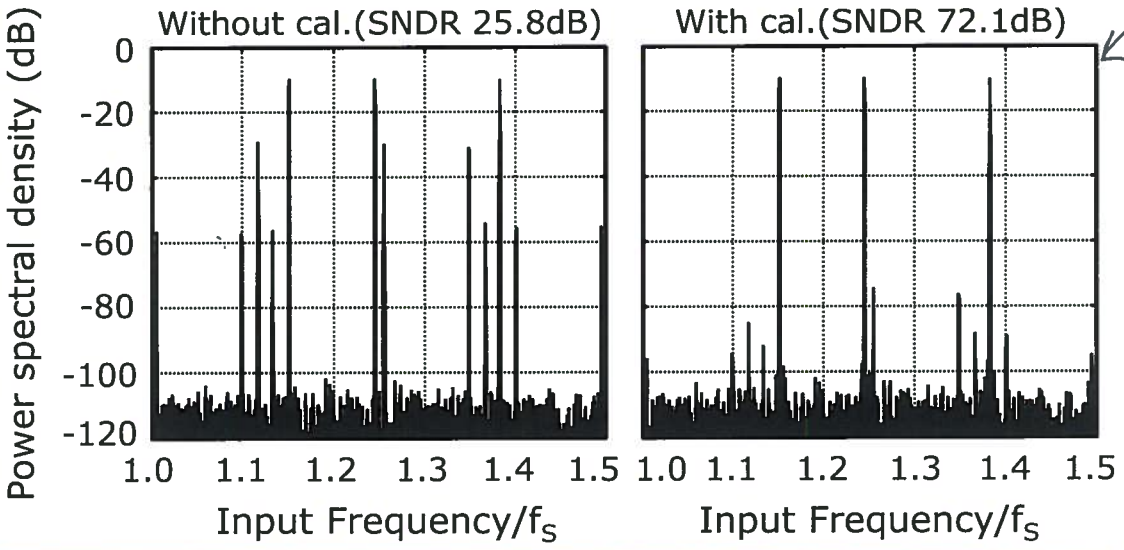


6-7 Simulation results

Input BW mismatch and Δt mismatch compensated

3-tone input
Sub-sampling(L=1)

A/D1: $f_{BW}=f_S*4/1.15$, $\Delta t=0.04*0.85/f_S$
A/D2: $f_{BW}=f_S*4/0.85$, $\Delta t=0.04*1.15/f_S$
A/D3: $f_{BW}=f_S*4/1.05$, $\Delta t=0.04*0.95/f_S$
A/D4: $f_{BW}=f_S*4/0.95$, $\Delta t=0.04*1.05/f_S$



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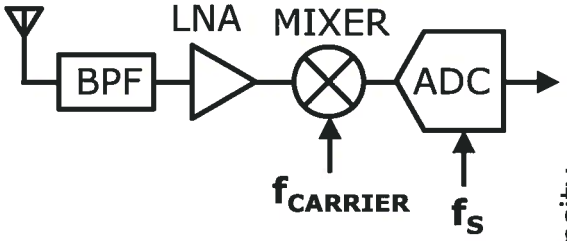
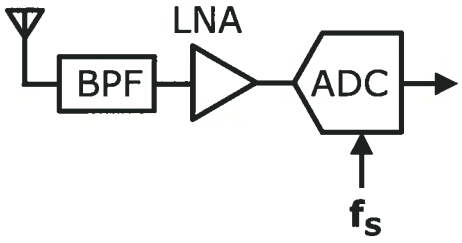
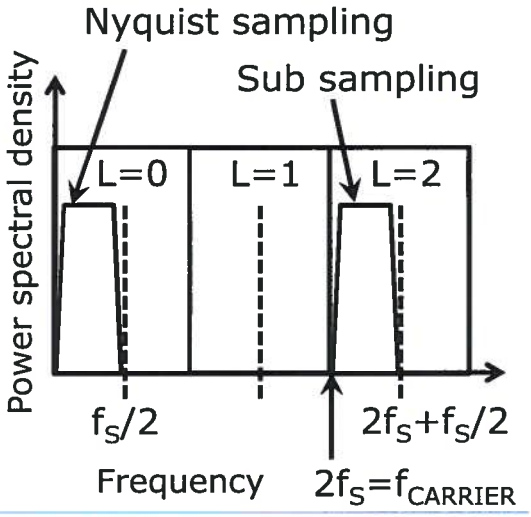
6-8 Sub-sampling receiver

Nyquist-sampling receiver

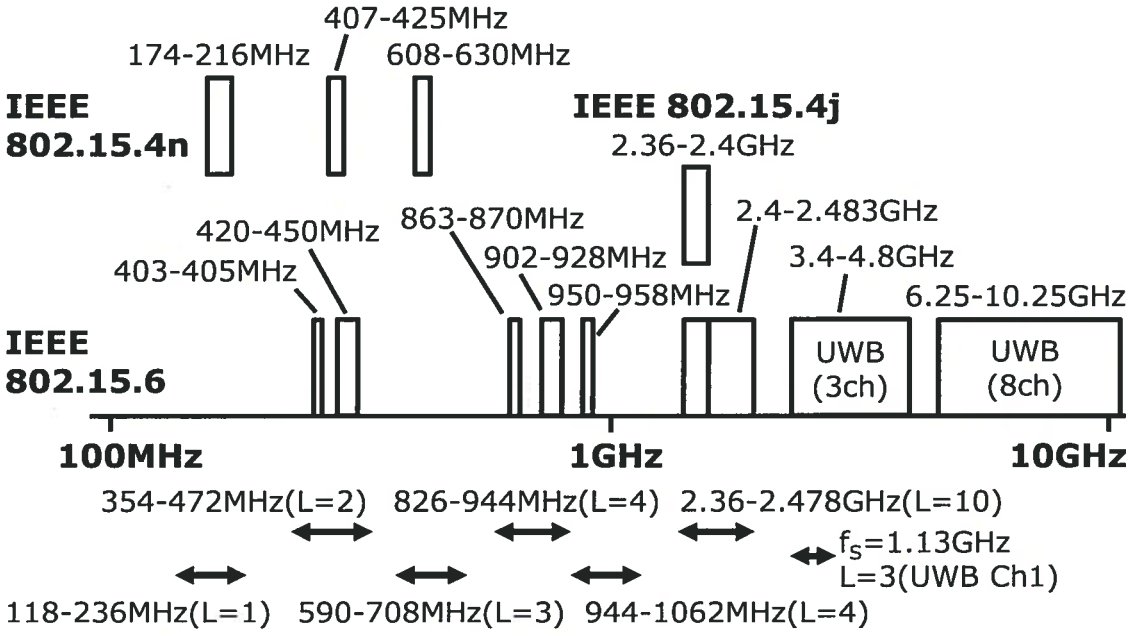


Sub-sampling receiver





6-9 Application to wireless BAN



☐ By setting f_S to 236MHz, most of WBAN bands can be covered.

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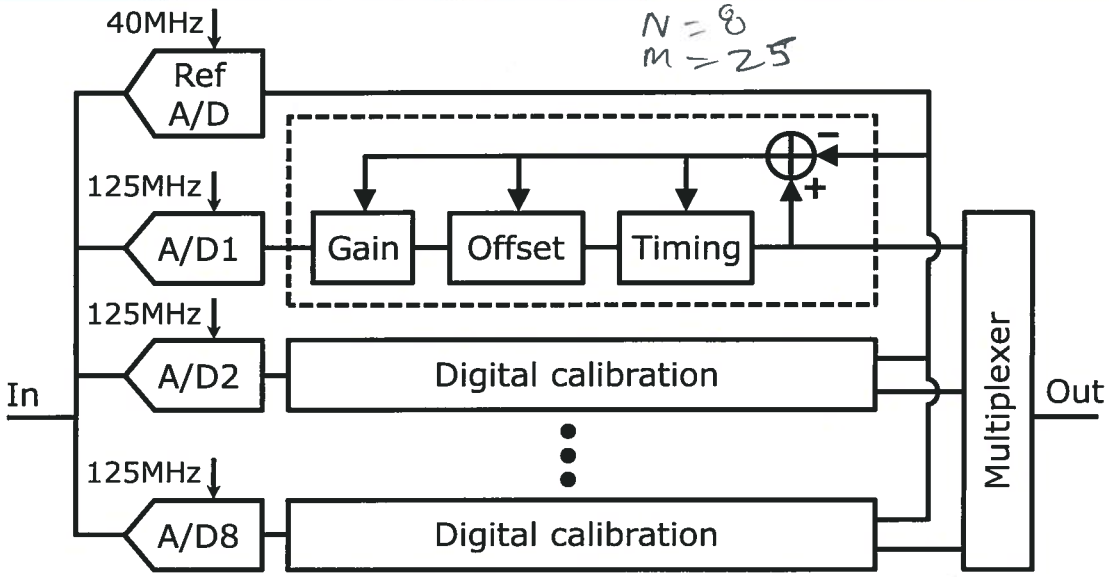
Outline

1. Introduction of time-interleaved ADC
2. Calibration of time-interleaved ADC assisted by reference converter
3. Calibration of higher-order effects of sampling-timing mismatch
4. Calibration of bandwidth mismatch
5. Differentiators for timing calibration
6. Extension to sub-sampling time-interleaved ADC
7. Measurement results
8. Summary and conclusion

7-1 1GS/s 14b 8way time-interleaved ADC



- 8-way 1-GS/s (125MS/s X 8) time-interleaved ADC using the above digital calibration has been demonstrated.

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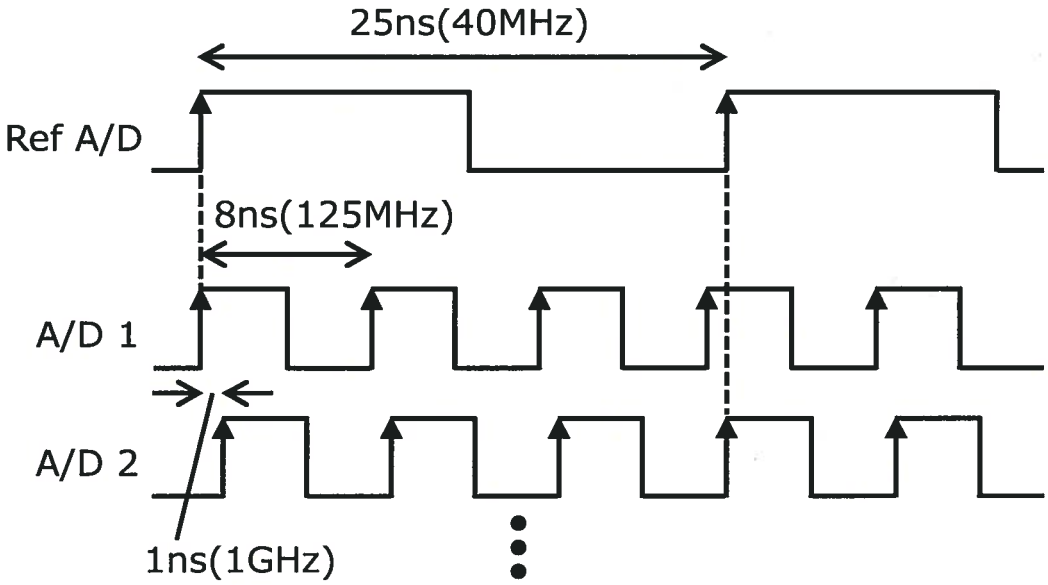
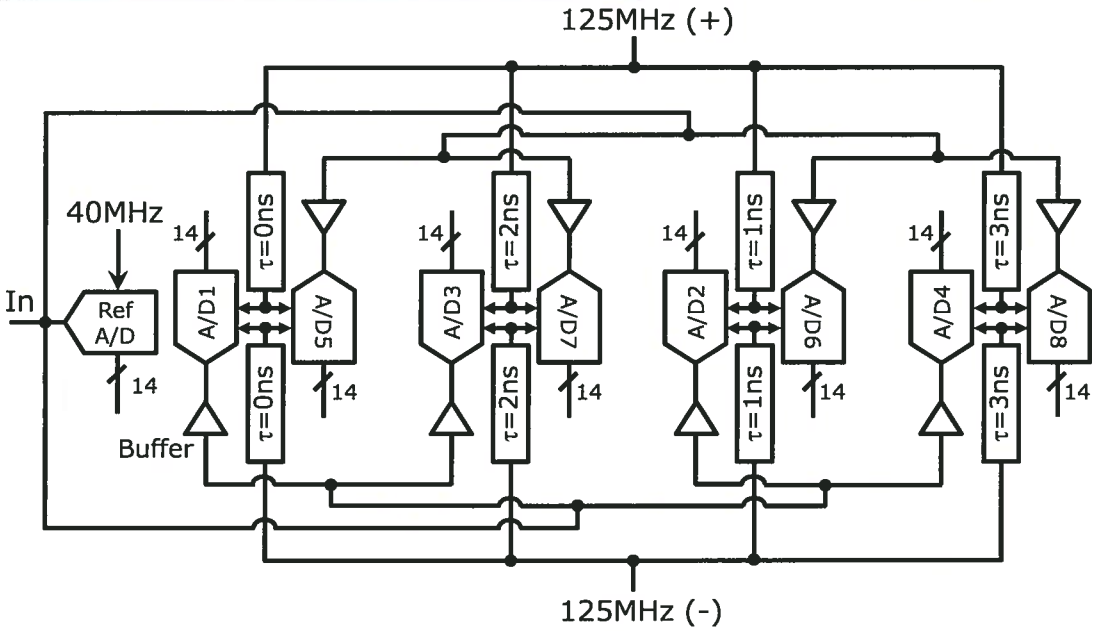
7-2 Timing chart



- Sampling rate of reference converter is 40MHz (N=25).

7-3 Differential-clock-sharing structure



- Commercially available 125-MS/s 14-bit ADC chips were used with 'differential-clock-sharing' structure.

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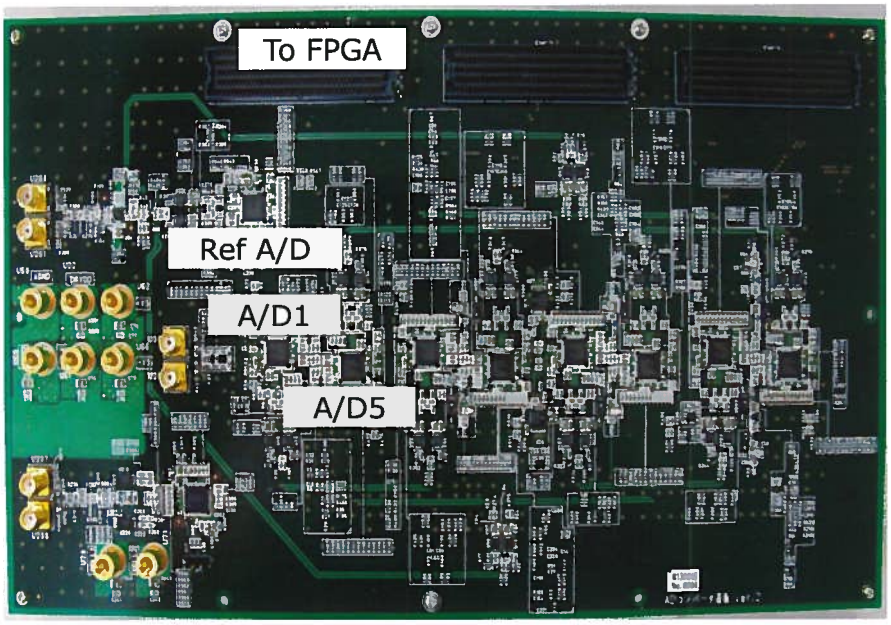
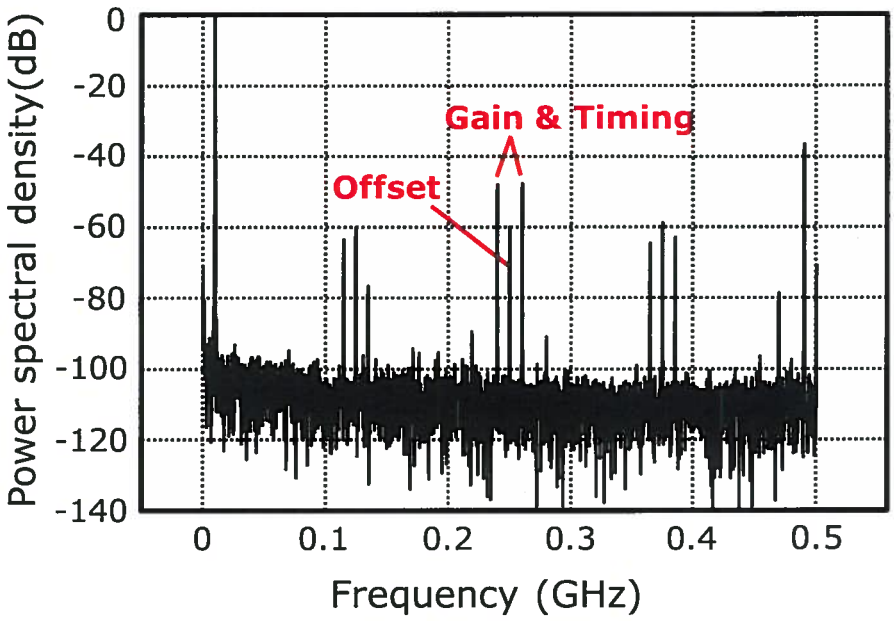
7-4 Photograph of analog board



7-5 FFT result before calibration



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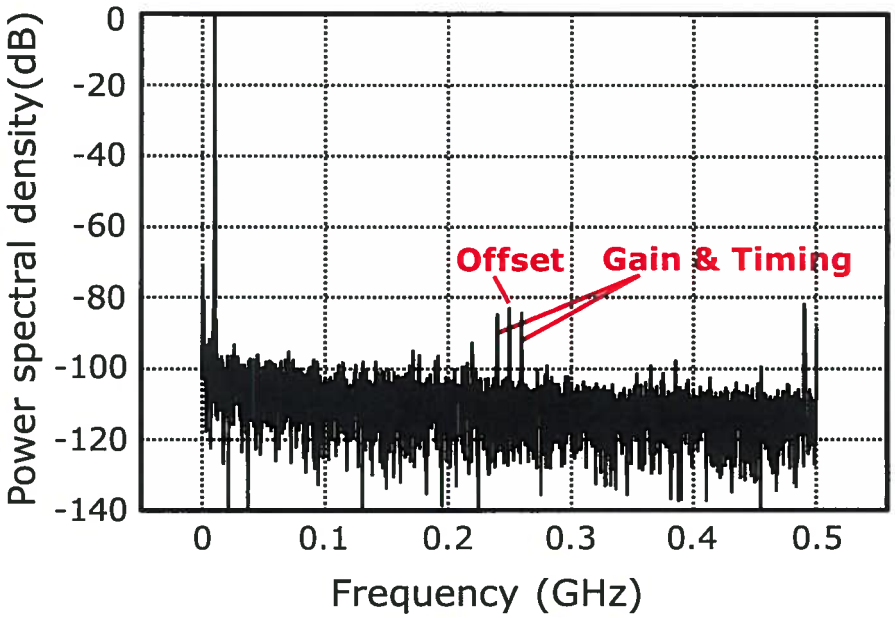
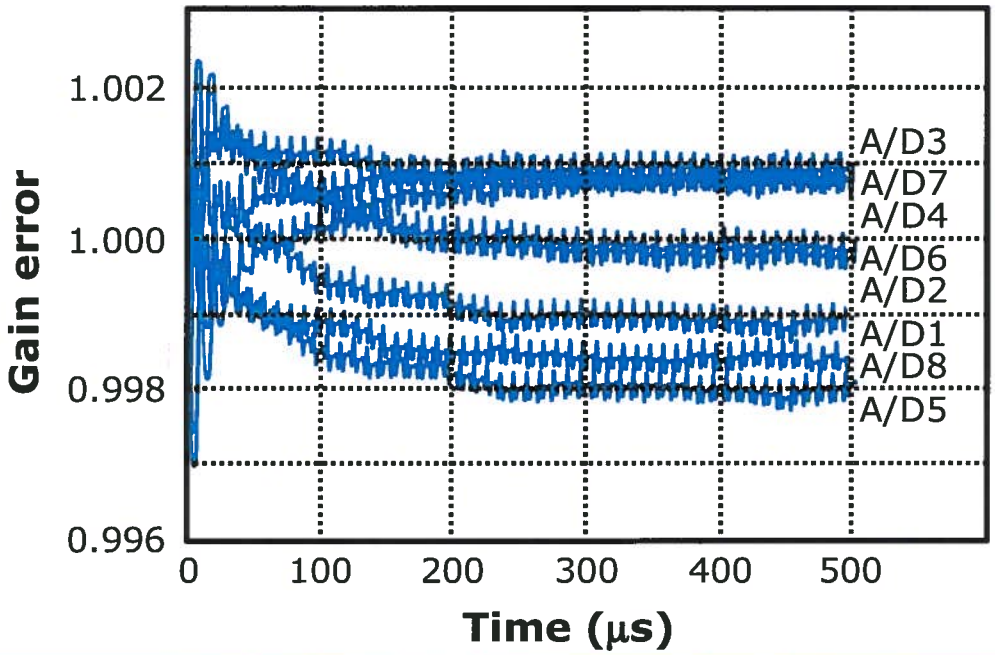
7-6 FFT result after calibration



- 71-dB SNDR and 82-dB SFDR were achieved for 50-MHz input.

7-7 Convergence behavior: Gain



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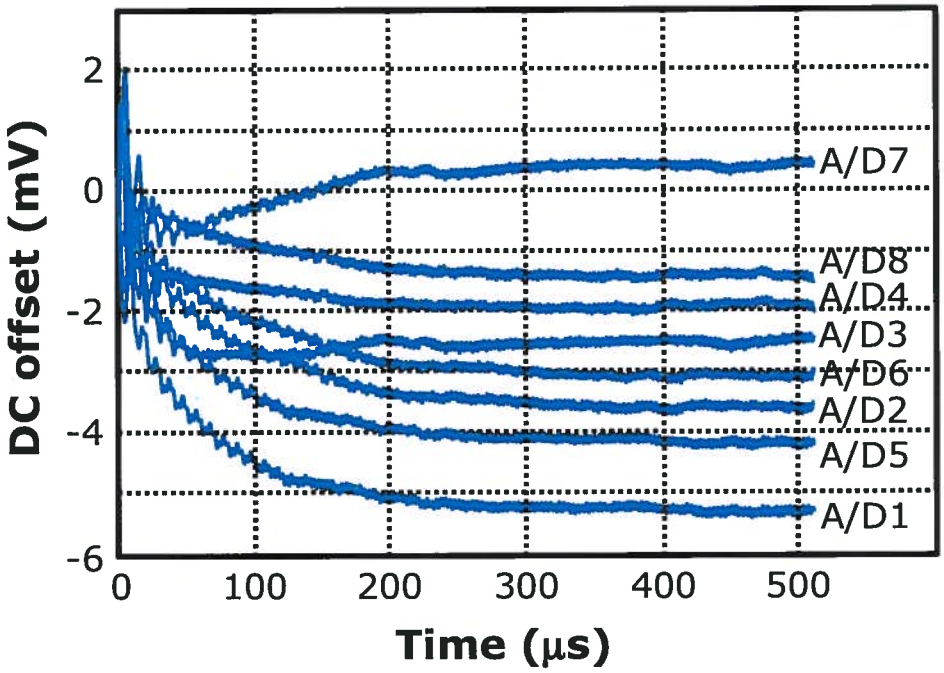
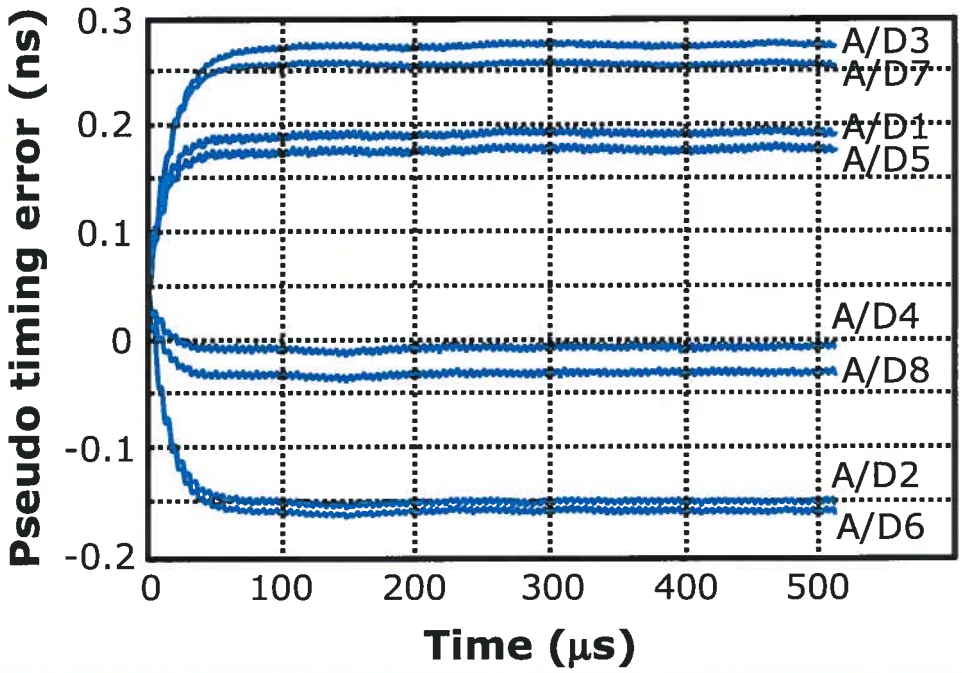
7-7 Convergence behavior: DC offset



7-7 Convergence behavior: Timing



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Estimation of area and current of CAL

	0.35 μm	0.18 μm	0.13 μm	90 nm	65 nm
Implementation Density (kG/mm^2)	20	100	200	400	800
Current density (μA/kG/MHz)	35	4.2	1.4	0.70	0.35
Gate count for CAL (kG) @12b *	58	58	58	58	58
Area for CAL (mm^2) @12b	2.9	0.58	0.29	0.15	0.07
Current for CAL (mA) @12b,200MS/s	410	49	16	8.1	4.1

* Including 2nd-order timing calibration with two cascaded stages

Gate count of CAL = 34kG for multipliers + 11kG for adders + 13kG for DFFs = 58kG/unit converter

References

[1] T. Oshima, T. Takahashi and T. Yamawaki, "LMS calibration of sampling timing for time-interleaved A/D converters," Electronics Letters, Vol. 45, pp. 615-617, Jun. 2009.

[2] T. Oshima, T. Takahashi and T. Yamawaki, "Novel sampling timing background calibration for time-interleaved A/D converters," IEEE 52nd International Midwest Symposium on Circuits and Systems, pp. 361-364, Aug. 2009.

[3] T. Takahashi and T. Oshima, "Highly accurate on-chip background calibration for time-interleaved A/D converters," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences (Japanese Edition) J93-A, pp. 613-625, Sep. 2010.

- Some delays are necessary to compensate the fixed delay by FIR differentiator as shown in the above references.

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Summary and conclusion

- ✓Adaptive digital calibration for time-interleaved ADC assisted by reference converter is presented.
- ✓It can calibrate the higher-order effects of sampling-timing mismatch and pseudo-timing mismatch caused by the finite input bandwidth.
- ✓The calibration works even for sub sampling by applying 'sub-sampling' differentiator.
- ✓The differentiators can be implemented by simple FIR filters.
- ✓The proposed techniques were demonstrated by the prototype measurements.

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Adaptive Calibration of Time-Interleaved A/D Converters

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January 22, 2015

Motivation and Problem to be Solved

- Problems of Time-interleaved ADC (TI-ADC)
  - Offset, gain, and timing mismatch between linear sub-ADCs
- Unsatisfactory existing calibration approaches
  - From signal processing community : too complicated, not intuitive, seldom realized on ICs
  - From circuit community : not general, not expandable
- Research objective
  - Intuitive, effective, and expandable calibration schemes that can be efficiently realized.

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Modeling a Time-interleaved ADC

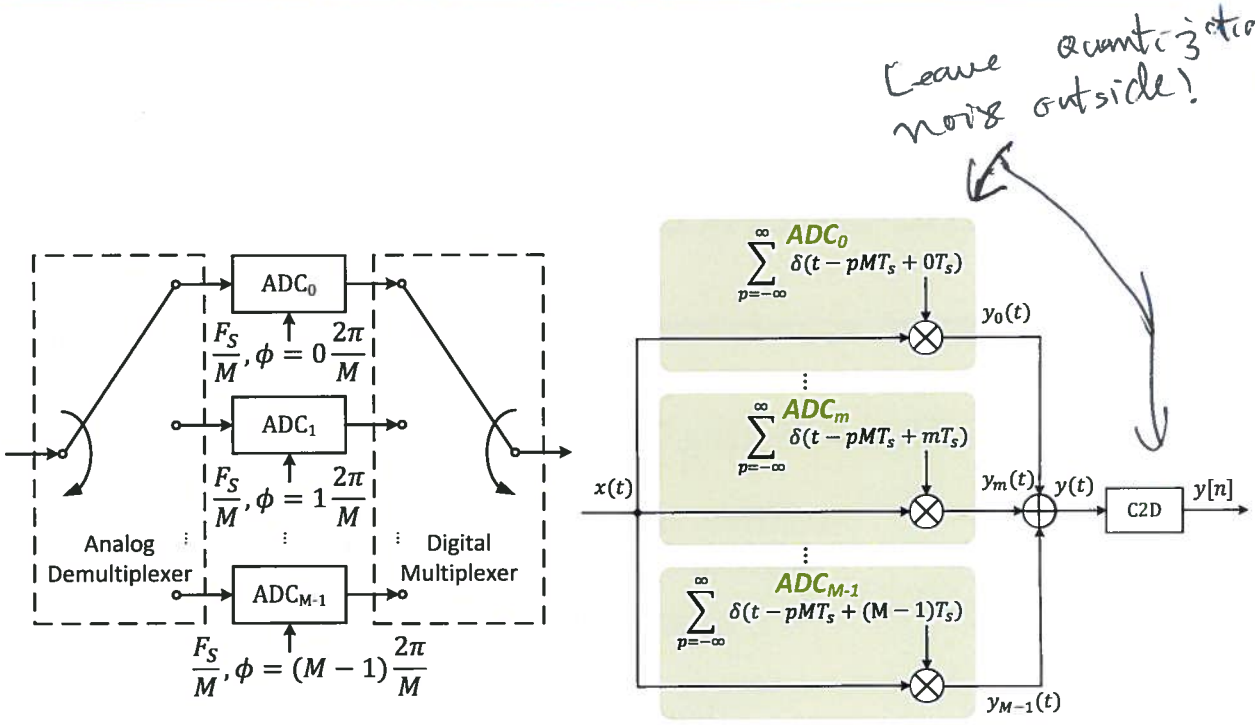
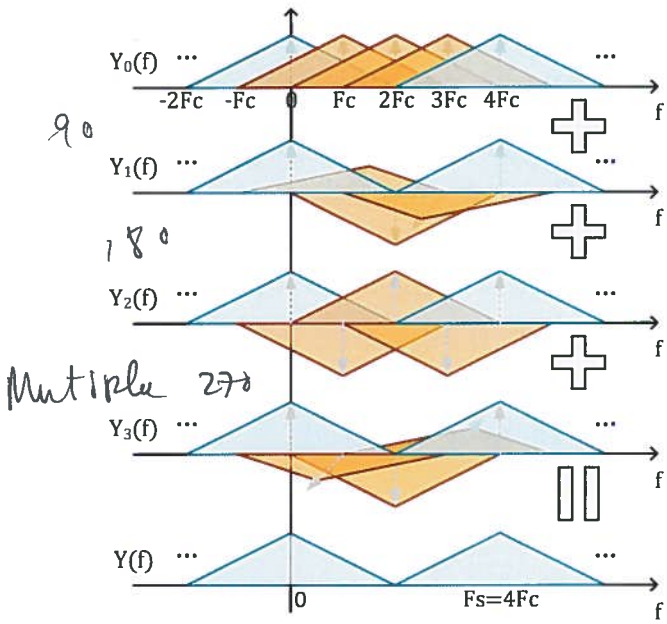


Illustration of Image Spectra

- Image spectra : frequency-shifted and rotated input spectrum
- Spectrum of each channel is aliased by images
- Final output spectrum of ideal TI-ADC is alias-free in the ideal case



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Modeling of Channel Non-idealities

pole freq mismatch

- Each channel : gain, timing skew, and bandwidth
- Represent all three non-idealities in a Channel Transfer Function (CTF), $H_m(f)$:

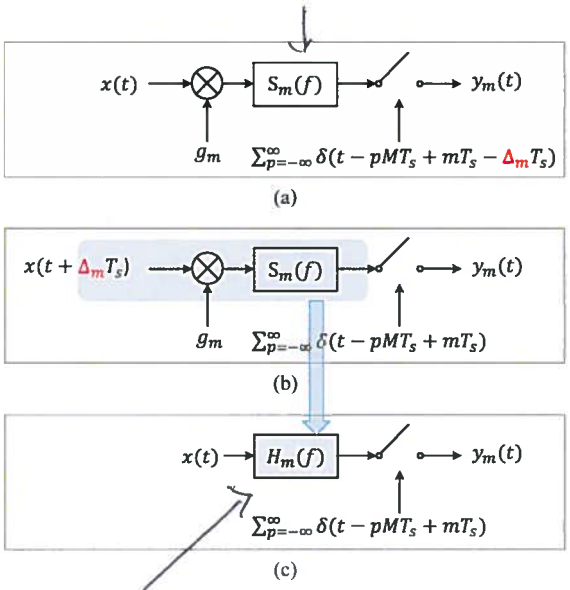
$$H_m(f) = g_m S_m(f) e^{j2\pi f \Delta_m Ts}$$

in c.t. domain

$$H_m(e^{j\omega}) = g_m S_m(e^{j\omega}) e^{j\omega\Delta_m}$$

in d.t. domain

where $\omega = 2\pi\frac{\Omega}{\Omega_s}$, $\Omega_s = 2\pi F_s = \frac{2\pi}{T_s}$



lumped non idealities here

Output Spectrum Formulation – Discrete Time

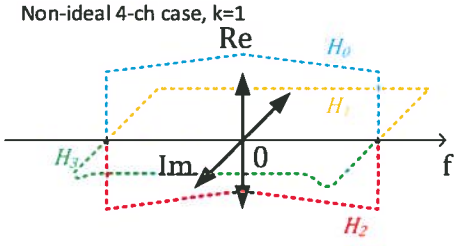
- Output spectrum:
  - Linear combination of input spectra filtered and frequency-shifted to each $k\frac{F_s}{M}$
  - For each k, CTFs of ALL channels are rotated and aggregated to Error Transfer Functions, ETF, $\breve{H}_k(e^{j\omega})$
  - Ideal case: $\breve{H}_0 = 1, \breve{H}_k = 0$ for $k \neq 0$
- If mismatches in H_m exist, $\breve{H}_k$ causes residual image → error spectrum

$$Y(e^{j\omega}) = \sum_{k=0}^{M-1} X(e^{j(\omega - k\frac{2\pi}{M})}) \breve{H}_k(e^{j(\omega - k\frac{2\pi}{M})})$$

$$\breve{H}_k(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} H_m(e^{j\omega}) e^{-jkm\frac{2\pi}{M}}$$

alias TF

signal TF



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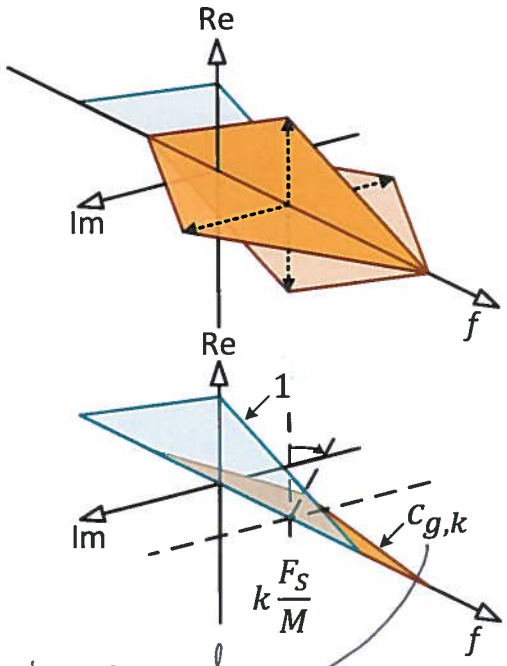
Error Spectrum due to Gain Mismatch

- ETF can be simplified as

$$\breve{H}_k(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} g_m e^{-jkm\frac{2\pi}{M}} = c_{g,k}$$

  where $c_{g,k}$ is a lumped complex coefficient
- Error spectrum
  - Scaled/rotated and frequency shifted version of input signal spectrum



gain scales, phase and freq

Error Spectrum due to Timing Skew

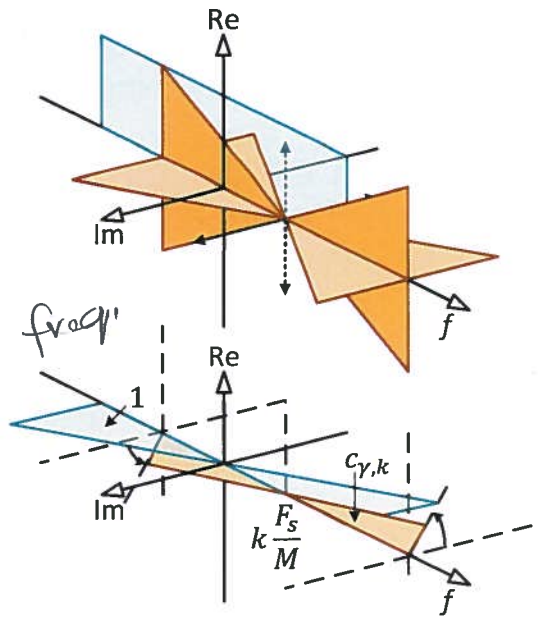
- CTF: $e^{j\omega\Delta_m} \simeq 1 + j\omega\Delta_m$ → Taylor approx.
- ETF:

$$\breve{H}_k(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} e^{j\omega\Delta_m} e^{-jkm\frac{2\pi}{M}}$$

$$\simeq j\omega c_{r,k}$$

→ error prop to freq

- Error spectrum: scaled/rotated and frequency-shifted version of the spectrum of input signal's derivative



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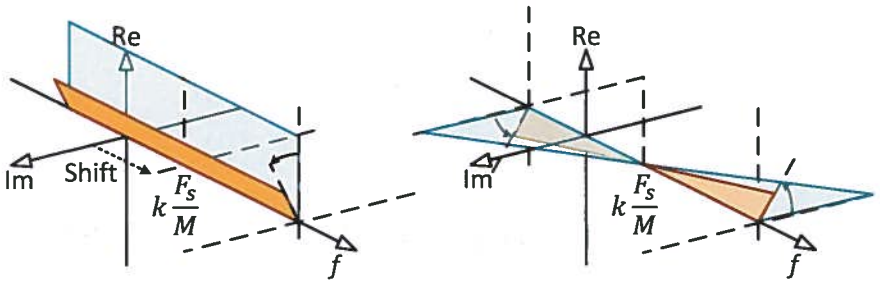
Mismatch Parameters to be Extracted

- Express error components from gain mismatch / timing skew mismatch in a linear form

$$E_k(e^{j\omega}) = X(e^{j(\omega-k\frac{2\pi}{M})})\breve{H}_k(e^{j(\omega-k\frac{2\pi}{M})})$$
$$\approx X(e^{j(\omega-k\frac{2\pi}{M})})(c_{g,k}+j(\omega-k\frac{2\pi}{M})c_{r,k})$$
$$= X_{\vec{k}}c_{g,k}+X'_{\vec{k}}c_{r,k}$$
$$\Rightarrow e_k[n] = x_{\vec{k}}c_{g,k}+x'_{\vec{k}}c_{r,k}$$

where $X' = j\omega X$ and $e_k \overset{\mathcal{F}}{\leftrightarrow} E_k, x_{\vec{k}} \overset{\mathcal{F}}{\leftrightarrow} X_{\vec{k}}, x'_{\vec{k}} \overset{\mathcal{F}}{\leftrightarrow} X'_{\vec{k}}$

- Illustration of $X_{\vec{k}}$, $X'_{\vec{k}}$, and E_k for a white input X



Parameter Extraction by Correlation

- Cross-correlation of y and x (both complex) is defined as

$$R_{y,x}(\tau) = \int_{-\infty}^{\infty} y(\tau)\cdot x^*(t+\tau)dt$$

- At 0 delay,

$$R_{y,x}(0) = \int_{-\infty}^{\infty} y\cdot x^* dt$$

- If $y = cx$,

$$R_{y,x}(0) = \int_{-\infty}^{\infty} cx\cdot x^* dt = c\int_{-\infty}^{\infty} x\cdot x^* dt$$

then c (complex) can be extracted by

$$\Rightarrow c = \frac{R_{y,x}(0)}{\int_{-\infty}^{\infty}|x|^2 dt} = \frac{R_{y,x}(0)}{R_x(0)}$$

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Correlation in Time-/Frequency-domain

- From Parseval's theorem [Oppenheim 1998],

$$R_{x,y}(0) = \sum_{n=-\infty}^{\infty} x[n] \cdot y^*[n] = \int_{2\pi} X(e^{j\omega}) \cdot Y^*(e^{j\omega}) \frac{d\omega}{2\pi}$$

- From Parseval's relation for the DFT,

$$R_{x,y}(0) = \sum_{n=0}^{N-1} x[n] \cdot y^*[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] \cdot Y^*[k]$$

- Parameters can be extracted either in the time domain or in the frequency domain:

$$\Rightarrow c = \frac{R_{y,x}(0)}{R_x(0)} = \frac{R_{Y,X}(0)}{R_X(0)}$$

↳ works for freq domain!

Applying Direct Correlation to TI-ADC

Input is Stationary!

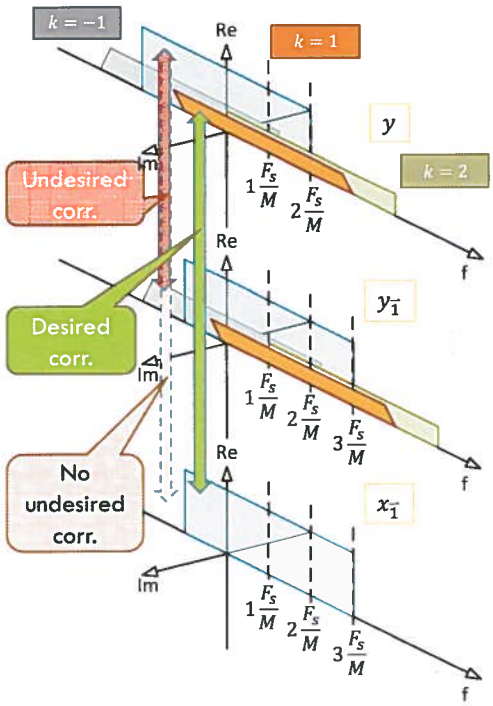
- TI-ADC output spectrum Y:

$$Y = X + E_1 + E_2 + \ldots + E_{M-1}$$
$$E_k = X_{\overrightarrow{k}} c_{g,k} + X'_{\overrightarrow{k}} c_{r,k}$$

- If x is WSS, $X_{\overrightarrow{i}}$, $X_{\overrightarrow{l}}$ are uncorrelated for $i \neq l$, and so are $X_{\overrightarrow{i}}$, $X'_{\overrightarrow{i}}$ for any i [Baskakov 1990], then $c_{g,k}$ and $c_{r,k}$ can be extracted by :

$$c_{g,k} = \frac{R_{Y,X_{\overrightarrow{k}}}}{R_{X_{\overrightarrow{k}}}}, c_{r,k} = \frac{R_{Y,X'_{\overrightarrow{k}}}}{R_{X'_{\overrightarrow{k}}}}$$

- Use Y ($Y_{\overrightarrow{i}}$, $Y'_{\overrightarrow{i}}$) to approximate X ($X_{\overrightarrow{i}}$, $X'_{\overrightarrow{i}}$) ⇒ undesired cross-correlation will appear
- Example: A 4-ch TI-ADC with gain mismatch only is shown to the right



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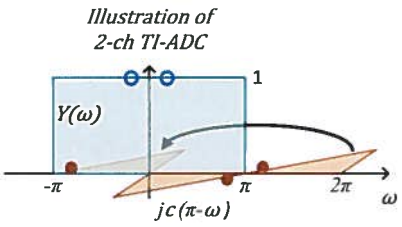
Undesired Cross-correlation

- Output of TI-ADC

$$Y = X + \sum_{i=0}^{M-1} E_i = X + \sum_{i=1}^{M-1} \left(X_{\overrightarrow{i}} c_{g,i} + X'_{\overrightarrow{i}} c_{r,i} \right)$$

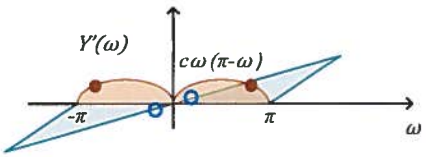
if $c_{g,0}$ and $c_{r,0}$ are reasonably assumed to be 0



- After passing the output through derivative filter:

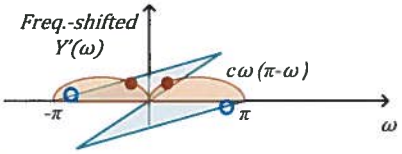
$$Y' = j\omega Y = j\omega X + j\omega \sum_{i=1}^{M-1} \left(X_{\overrightarrow{i}} c_{g,i} + X'_{\overrightarrow{i}} c_{r,i} \right)$$

$$= X' + \sum_{i=1}^{M-1} \left(j\omega X_{\overrightarrow{i}} c_{g,i} + j\omega X'_{\overrightarrow{i}} c_{r,i} \right) \text{ for } -\pi < \omega < \pi$$



- After frequency shifting:

$$Y'_{\overrightarrow{k}} = X'_{\overrightarrow{k}} + \sum_{i=1}^{M-1} \left(j\omega X_{\overrightarrow{i}} c_{g,i} + j\omega X'_{\overrightarrow{i}} c_{r,i} \right)_{\overrightarrow{k}} \text{ for } -\pi < \omega - k\frac{2\pi}{M} < \pi$$

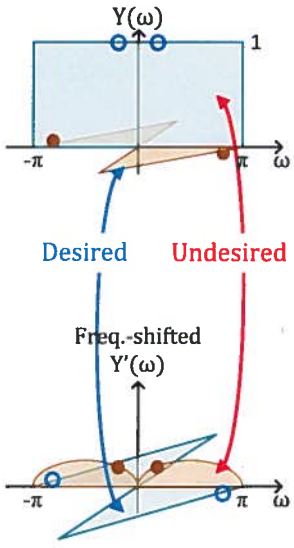


Undesired Cross-correlation (Cont'd)

- To extract $c_{r,k}$, for example, perform cross-correlation:

$$R_{Y,Y'_{\overrightarrow{k}}}(0) = \int_{2\pi} Y \cdot \left(Y'_{\overrightarrow{k}} \right)^* \frac{d\omega}{2\pi} = \int_{2\pi} \left(X + \sum_{i=1}^{M-1} \left(X_{\overrightarrow{i}} c_{g,i} + X'_{\overrightarrow{i}} c_{r,i} \right) \right)$$

$$\cdot \left(X'_{\overrightarrow{k}} + \sum_{l=1}^{M-1} \left(j\omega X_{\overrightarrow{l}} c_{g,l} + j\omega X'_{\overrightarrow{l}} c_{r,l} \right)_{\overrightarrow{k}} \right)^* \frac{d\omega}{2\pi}$$



- Since $R_{X_{\overrightarrow{i}},X_{\overrightarrow{l}}} = 0$ for $i \neq l$, and $R_{X_{\overrightarrow{i}},X'_{\overrightarrow{l}}} = 0$ for any i and l, and let $\left(j\omega X'_{\overrightarrow{M-k}} \right)_{\overrightarrow{k}} = U_k(\omega) X_{\overrightarrow{M}}$

$$R_{Y,Y'_{\overrightarrow{k}}} = c_{r,k} \int_{2\pi} |X'_{\overrightarrow{k}}|^2 \frac{d\omega}{2\pi} + c_{r,M-k} \int_{2\pi} X U_k(\omega) X^*_{\overrightarrow{M}} \frac{d\omega}{2\pi} + \mathcal{O}(c_{r,i}, c_{r,l})$$

$$\frac{R_{Y,Y'_{\overrightarrow{k}}}}{R_{Y'}} \simeq c_{r,k} \left(1 + \frac{c_{r,M-k}}{c_{r,k}} \frac{\int_{2\pi} U_k(\omega) |X_{\overrightarrow{M}}|^2 d\omega}{\int_{2\pi} |X'|^2 d\omega} \right) = c_{r,k} \left(1 + \text{Bias} \right)$$

where $X'_M = X'$, $\int_{2\pi} |X'|^2 d\omega = \int_{2\pi} |X'_{\overrightarrow{k}}|^2 d\omega$, U_k is distorting function

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Remove Undesired Cross-correlation

Options to remove the undesired cross-correlation terms:

- Calculate it with prior knowledge of input spectrum, such as
  - known single-tone sinusoidal signal as a training signal
  - known bandwidth for white input
- Mismatch parameter estimation/error correction loop to blindly remove such bias gradually.
  - General procedure of adaptive loop

Update estimates of $\hat{c}_{g,k}$ and $\hat{c}_{r,k}$

$$\hat{e}_k[n] \simeq \hat{x}_{\overrightarrow{k}}[n]\hat{c}_{g,k} + \hat{x}'_{\overrightarrow{k}}[n]\hat{c}_{r,k}$$

$$\hat{x}[n] = y[n] - \sum_{k=1}^{M-1} \hat{e}_k[n-1]$$

  - Adaptive Interference Cancellation can serve as a problem-solving framework

"Adaptive" Interference Cancellation

Interference model:

$$y[n] = e[n] + x[n]$$

$$e[n] = \vec{x}^T c_g + \vec{x'}^T c_r$$

$$= \boldsymbol{u}^T \boldsymbol{w}$$

$$\Rightarrow y = \boldsymbol{u}^T \boldsymbol{w} + x$$

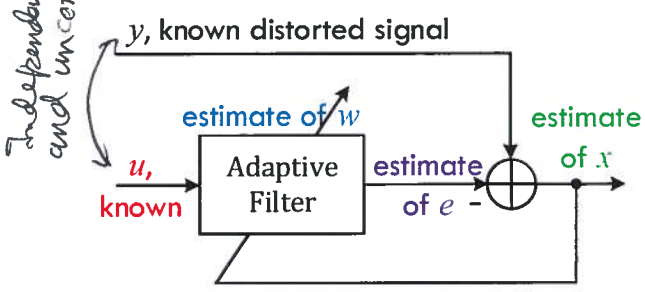
$$\boldsymbol{u}\ (\text{interference}) = \begin{bmatrix} \vec{x} \\ \vec{x'} \end{bmatrix}$$

$$= \begin{bmatrix} x_{\overrightarrow{1}} & \cdots & x_{\overrightarrow{M-1}} & x'_{\overrightarrow{1}} & \cdots & x'_{\overrightarrow{M-1}} \end{bmatrix}^T$$

$$\boldsymbol{w}\ (\text{unknown weights}) = \begin{bmatrix} c_g \\ c_r \end{bmatrix}$$

$$= \begin{bmatrix} c_{g,1} & \cdots & c_{g,M-1} & c_{r,1} & \cdots & c_{r,M-1} \end{bmatrix}^T$$

Block diagram :



Do argmin $E\left\|y - \boldsymbol{u}^T \hat{\boldsymbol{w}}\right\|^2$ via LMS :

$$\hat{\boldsymbol{w}}_n = \hat{\boldsymbol{w}}_{n-1} + \mu \boldsymbol{u}_n (y_n - \boldsymbol{u}_n^T \hat{\boldsymbol{w}}_{n-1})$$

$$= \hat{\boldsymbol{w}}_{n-1} + \mu \boldsymbol{u}_n \cdot \hat{x}_n$$

$\Rightarrow$ When the loop reaches steady-state,

$$\hat{w} \approx w^o = R_{yu} R_u^{-1}$$

This *is* the sought estimate

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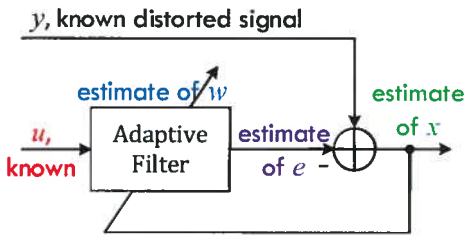
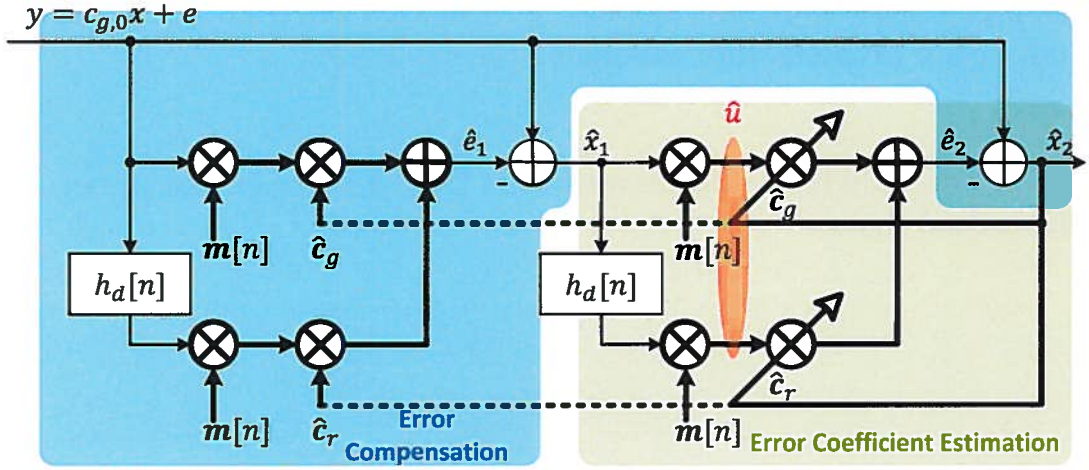
UCLA Method – Time-domain Implementation

- Use LMS adaptive interference cancellation to estimate mismatch coefficients
- To approximate interference u, use reconstructed error $\hat{e}_1$ and first corrected $\hat{x}_1$
- Use second corrected $\hat{x}_2$ as final output



A/D output signal + errors



Limiting Factors of SNR Performance

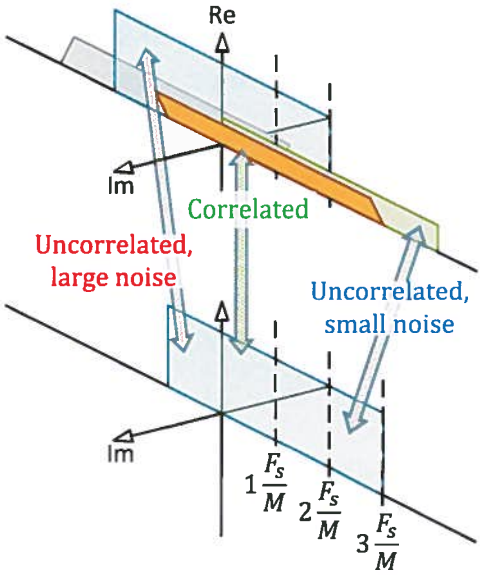
- Accuracy of $\hat{w}$ from LMS [Sayed 2008]: Mean-Square-Deviation (MSD) of $\hat{w}$ is given by

$$MSD \approx \mu\sigma_v^2(M-1)$$

assuming small μ and large M

  - Accuracy / convergence time trade-off.
  - Large background spectrum causes large MSD ⇒ Slows convergence
  - Solution: Training tones + adaptive μ "gearshift" (see table)

μ: step size of LMS algorithm
σ_v^2 : background noise observed, σ_v might be σ_x or $\sigma_{x'}$
M : No. of channels



Coeff. est.	Foreground	Background
Input	Training signal	Actual signal
μ	large	small

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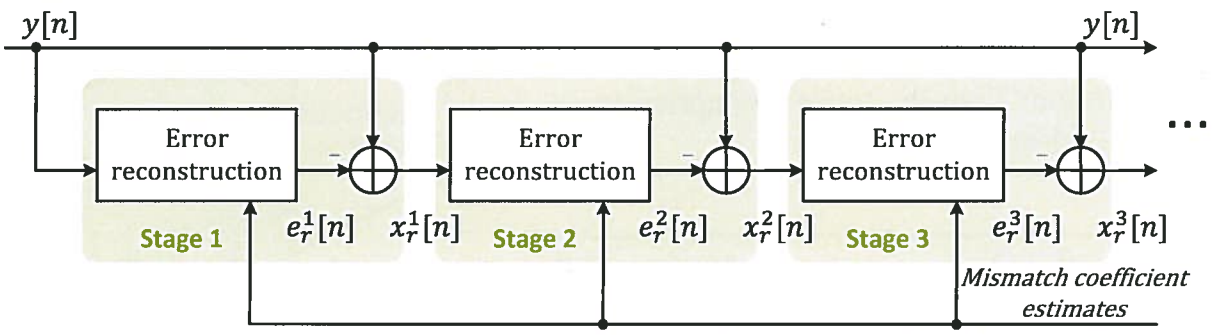
Consideration of Training Tones

- Frequency, can be anywhere other than:
  - too low → the error signals from timing skew would be too small to facilitate fast and accurate convergence.
  - out-of-band (OOB) → aliasing will cause false skew parameter extraction
  - multiples of sub-sampling frequency $\frac{F_S}{M}$ → Images will overlap with input itself, giving wrong info for calibration [Santin 2012]
- Waveform
  - Single tone, multi tones, square wave with OOB harmonics filtered out, narrow band signals

Limiting Factors of SNR Performance (Con't)

- Accuracy of $\hat{u}$: more accurate with more cascaded correction stages.
  - Each stage reconstructs the error and subtract it from the output.
  - Required no. of stages depends on the mismatch and the target SNR performance.



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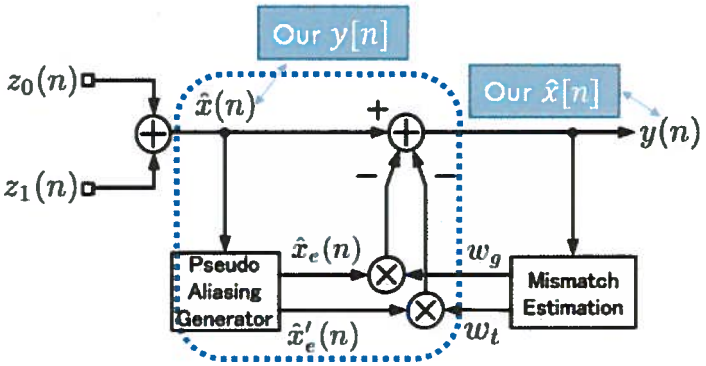
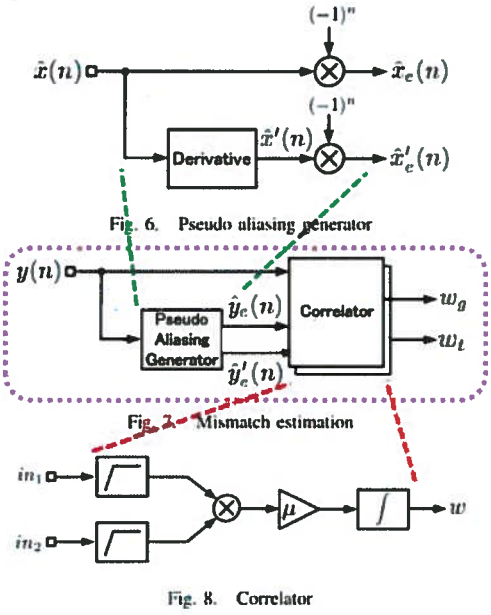
Prior Work-1: Tracking Remaining Correlation

[Matsuno 2013]

This work is close to the time-domain implementation of our independent research

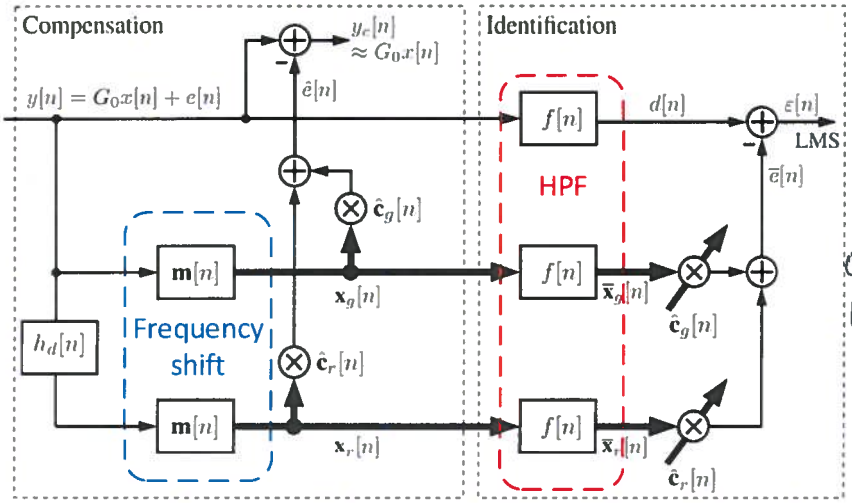
- Idea: Tracking remaining correlation + Error reconstruction/subtraction
- Major issue: (1) Accuracy-convergence speed trade-off ⇒ Slower convergence and worse SNR with wide-band input as in ours. (2) Only first corrected output with comparable hardware

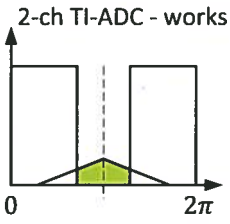


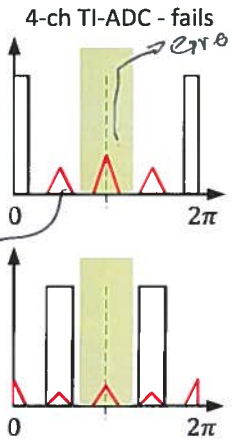


Prior Work-2: Mismatch Estimation using Monitor Band [Vogel 2008]

- Idea: Error reconstruction/subtraction + energy sensing at monitor band
- Major issue: constraints on input spectrum → all the error spectra must fall in the monitor band.







errors outside Monitor Band!

error in monitor band!

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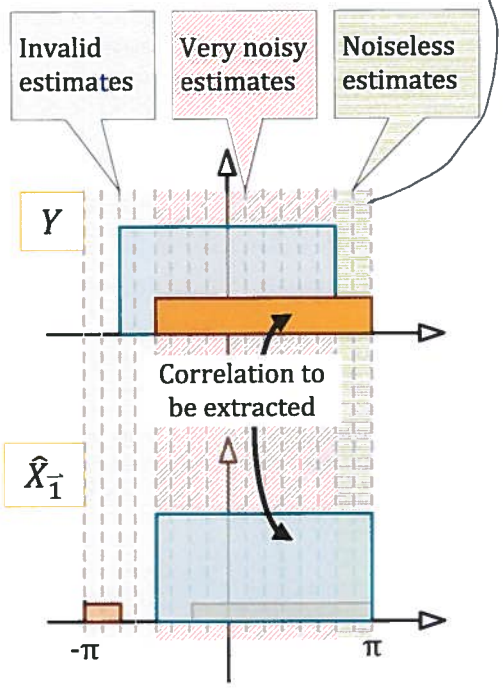
Faster and More Robust Convergence - Subband Adaptive Filtering

- Target: find the corr. between error spectrum and shifted main spectrum.
- Wide-band input causes large background estimation noise. Use good estimates after channelization.
- Diffusion strategy of adaptation [Sayed 2012]
  - Each subband runs LMS algorithm to find its own estimate of the same coeff.
  - Subbands with more/less background noise are given smaller/larger μ step.
  - Estimated coeff. of subbands with more/less shifted spectrum energy are weighted more/less.

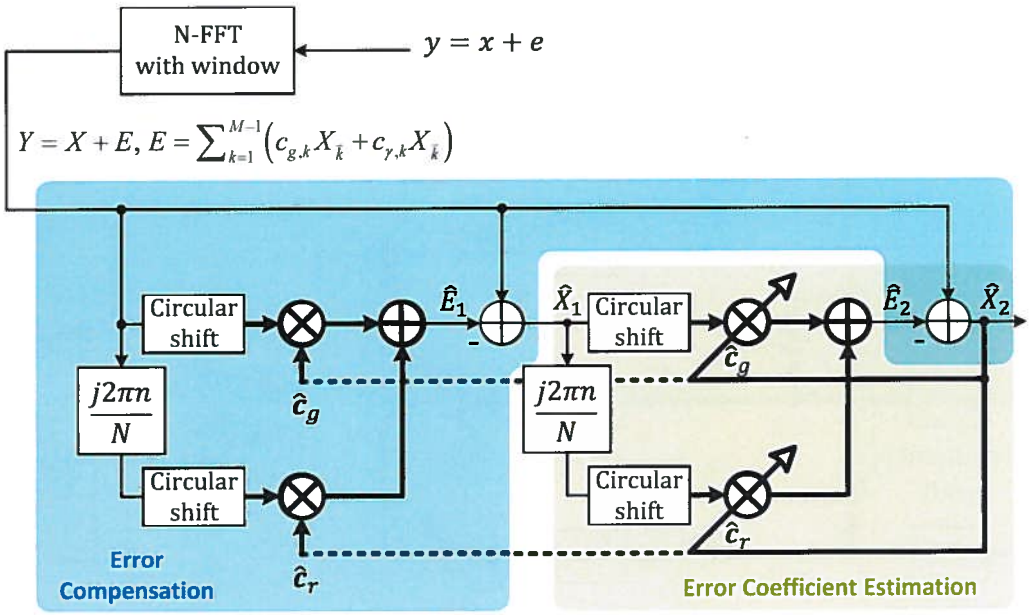
less background noise



UCLA Method - Frequency-domain Implementation

Data stream is translated to the frequency domain by N-FFT first.

- Complex multiply with $e^{j\omega n}$ replaced with circular shift
- Derivative filter replaced with multiply by frequency index



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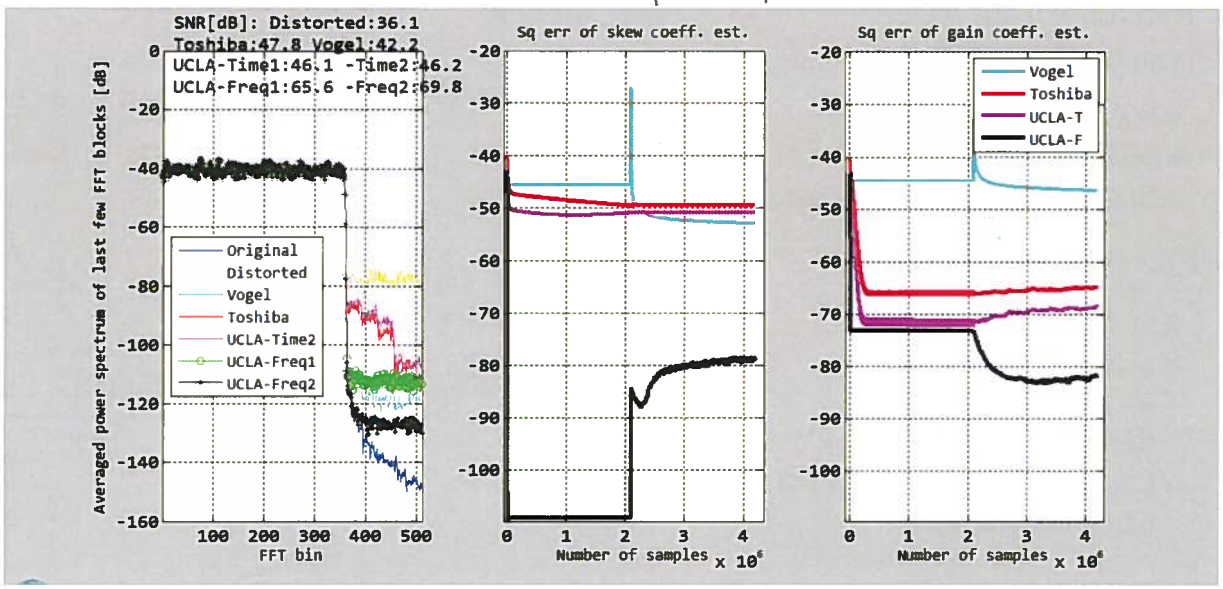
Simulation - Frequency-domain Approach

32-Ch with training tone + μ gear shifting

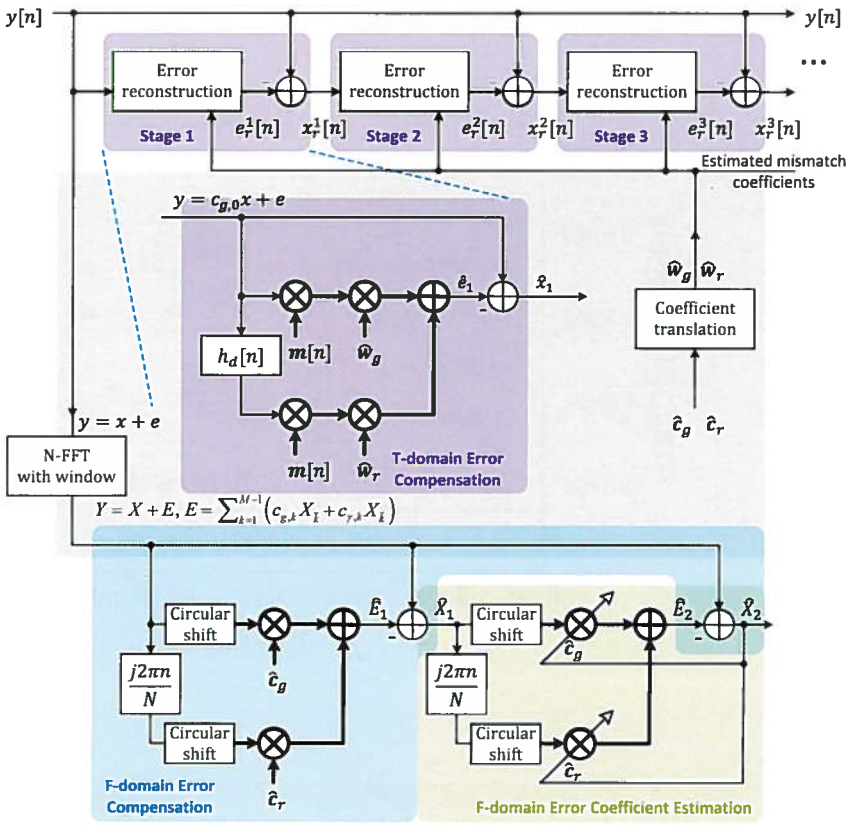
- Training tone at $F_s/3$, gear shifting μ by 2000 ↓
- Uncorrected=36dB, Toshiba=48dB, Vogel=42dB, UCLA T-domain=46dB, **UCLA F-domain=70dB**

Track slow drift



UCLA Method - Hybrid domain Approach

- Estimation in frequency domain; correction in time domain to retrieve real-time data
- Speed of estimation can be slowed down → reduce hardware overhead
- Time-domain and frequency-domain blocks can use different error basis signals via coefficient translation
- SNR of both domains is comparable after coefficient translation



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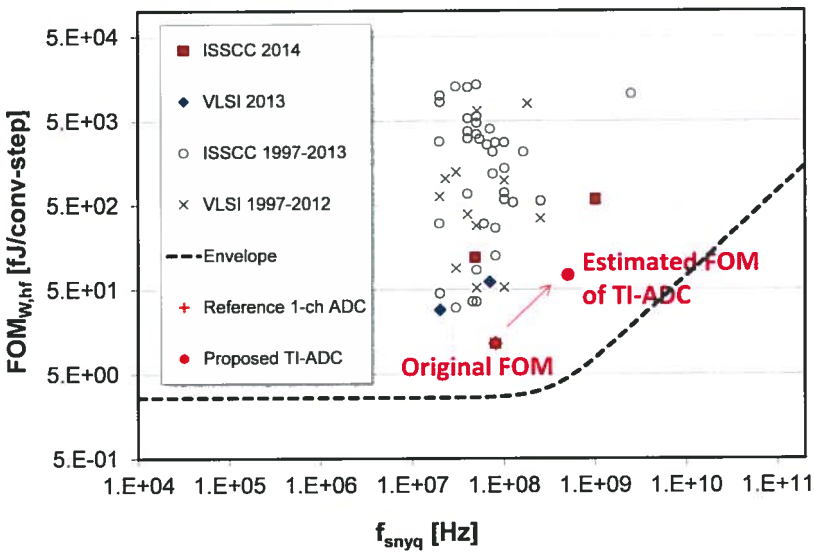
Hardware Cost Analysis

- Design Target:
  - 500MSPS
  - >65dB SNDR
- Reference 1-ch ADC [van der Goes 2014]
  - 80MSPS Pipelined SAR
  - 66dB SNDR
  - State-of-the-art 1.5mW power
- Power/Area analysis
  - $M = 8$
  - assum 20% power/area overhead for FE after time-interleaving
  - Cost is estimated using STM 65nm GP process

Block	Power(mW)	Area (mm^2)
FE 8-ch ADC	14.4	1.3
BE Time-domain correction	17.4	0.08
BE 1024 FFT	20	1.4
BE Freq.-domain Coeff. Extraction	7.6	0.7
Total (BE Cal.)	**59.4 (45)**	**3.5 (2.2)**

Walden / Schreier FOM Plot



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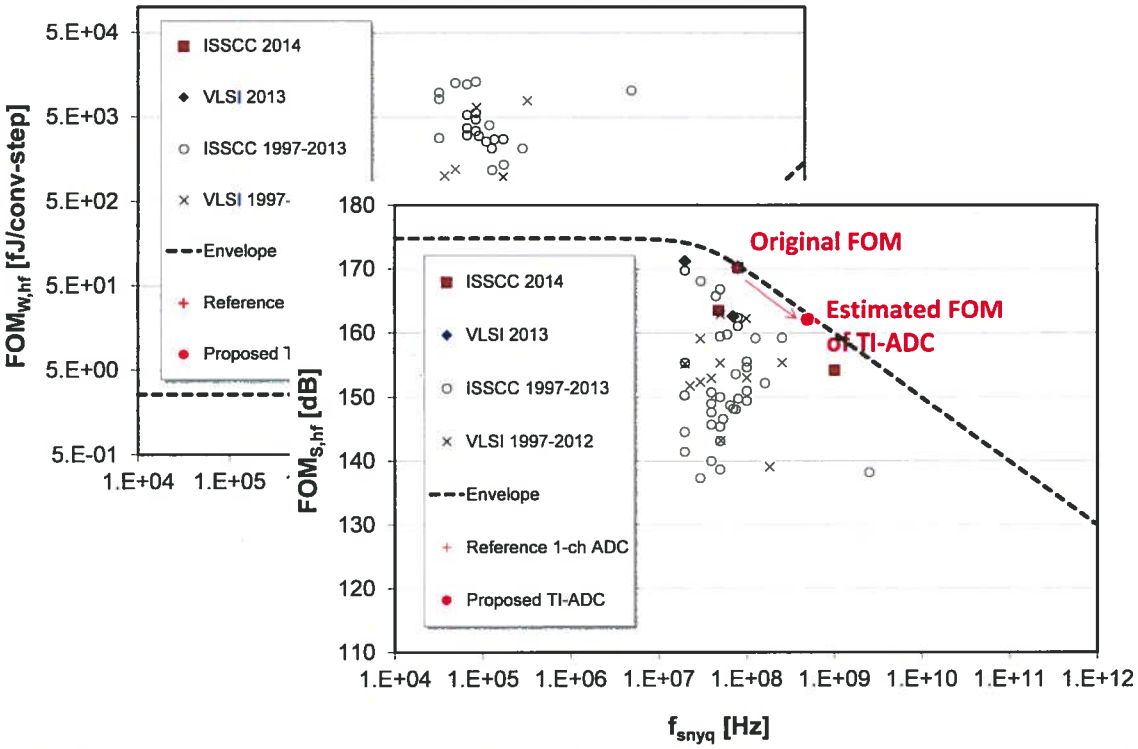
Walden / Schreier FOM Plot



Applying UCLA Calibration on Commercial IC

Commercial TI-ADC IC info:

- 12b 2.0/2.5GSPS Monolithic ADC (4-ch Time-interleaving)
- Embedded in-house individual channel non-linearity **AND** interleaved channel mismatch calibration
- Typical FFT plot SFDR = 75dBc @ 1800MHz Fin, 2.5GSPS

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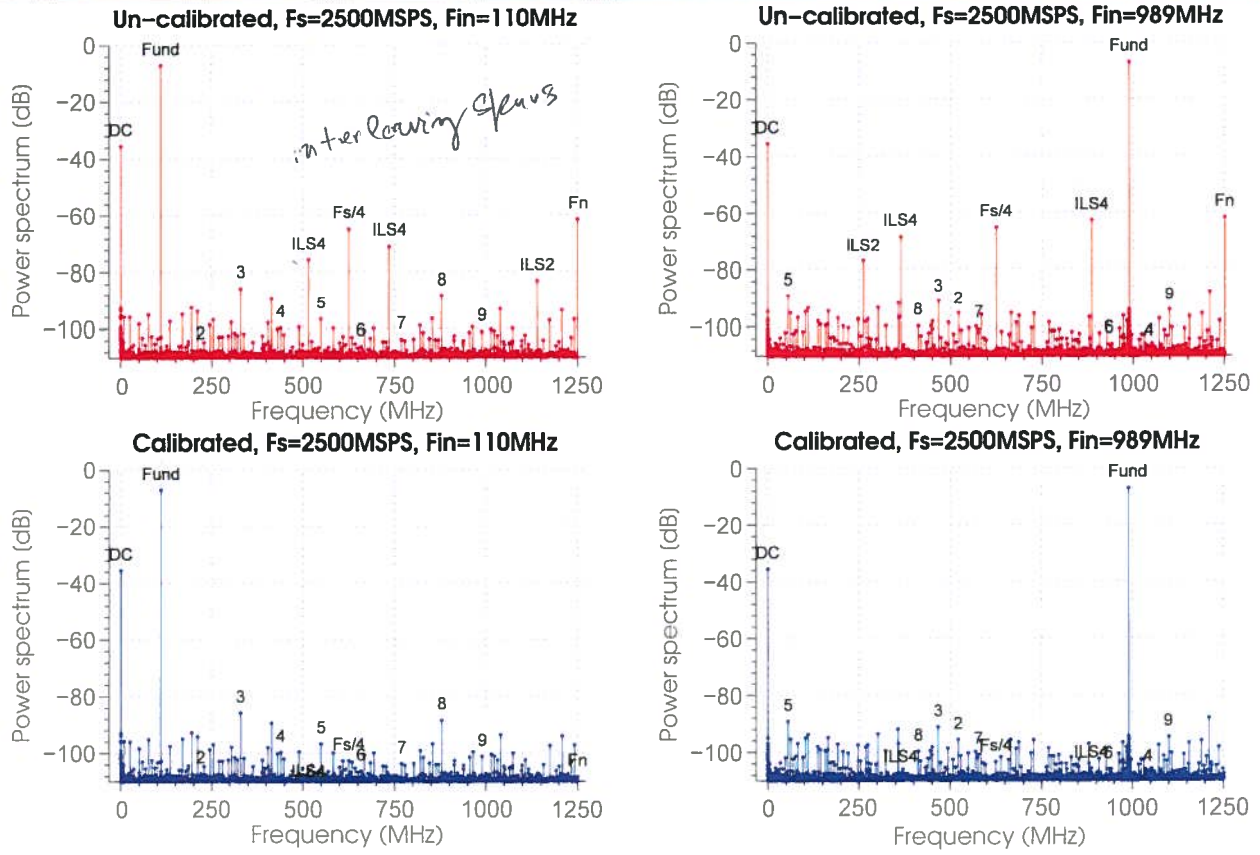
Performance Summary of Calibration Results

- Uncalibrated TI-ADC raw data from commercial ADC
  - single-tone sinusoidal signal
  - F_{in} = 110 / 1000 / 1800 / 3000 MHz
  - F_S = 2.0 / 2.5 GSPS
  - Individual channel non-linearity has been corrected is pre-calibrated
- Channel mismatch is calibrated using UCLA adaptive TI-ADC calibration approach. Tabular results(dBc) : AC spec. / Un-calibrated / Calibrated
  - AC spec: SFDR excluding 2nd or 3rd harmonic (from datasheet)
  - Un-calibrated / calibrated: worst interleaved error before / after calibration

F_{in}	$F_S = 2.0$ GSPS	$F_S = 2.5$ GSPS
110MHz	80/57/100	77/55/95
1000MHz	83/57/80**	82/56/96
1800MHz*	85/54/93	81/51/83
3000MHz*	*n.a.*/52/63**	*n.a.*/48/92

* Extracted coefficients for beyond-Nyquist frequencies are incorrect, but the error is still correctly calibrated.
** Correction of near-Nyquist frequency is limited due to derivative filter.

FFT Spectrum - Fs=2.5G, Fin@1st Nyquist



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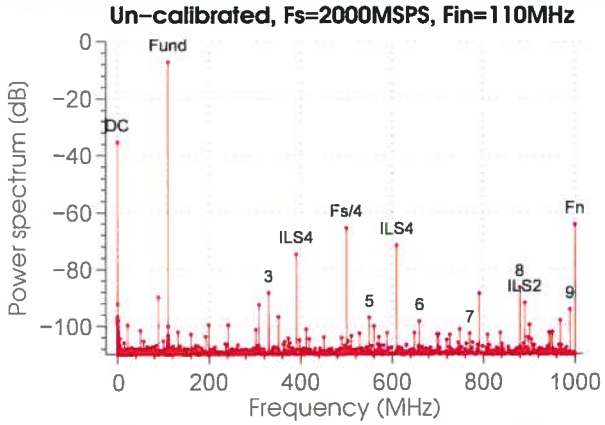
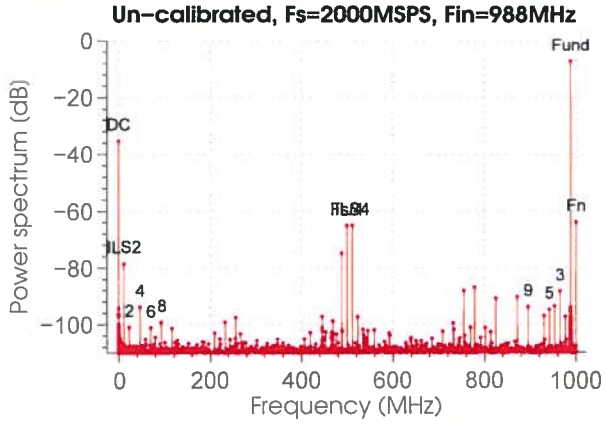
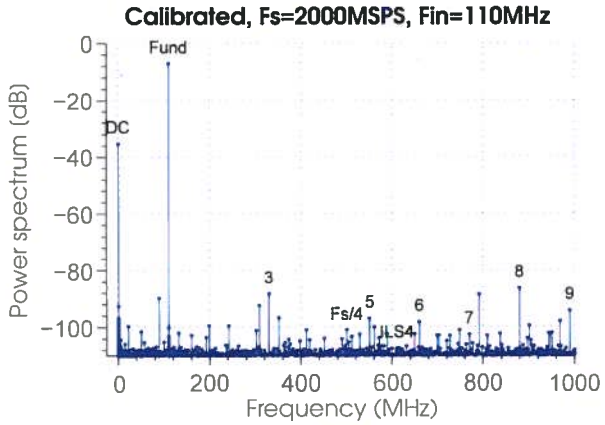
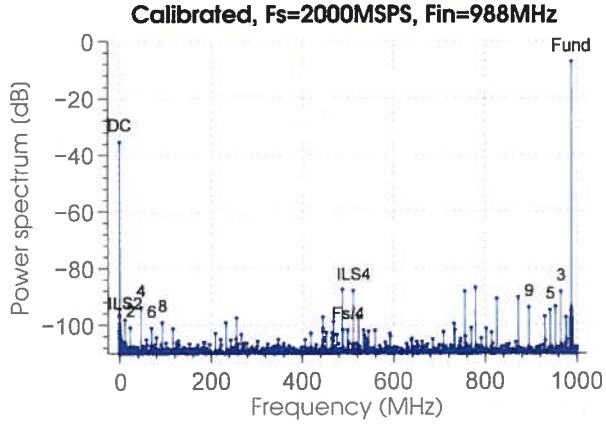
FFT Spectrum - Fs=2.0G, Fin@1st Nyquist

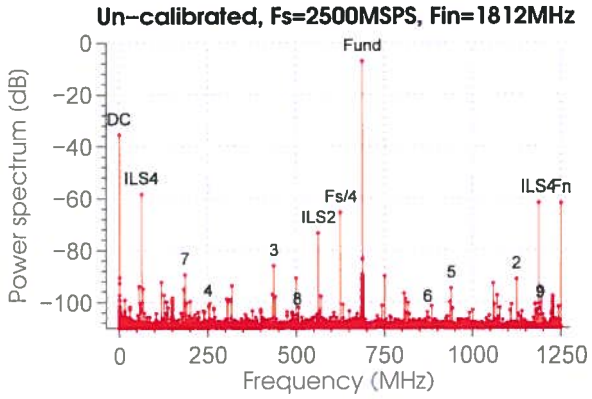


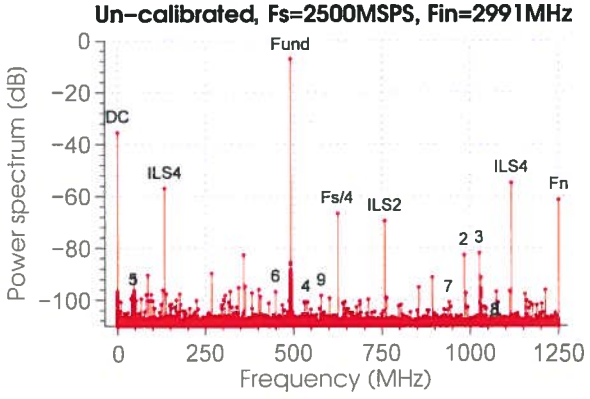


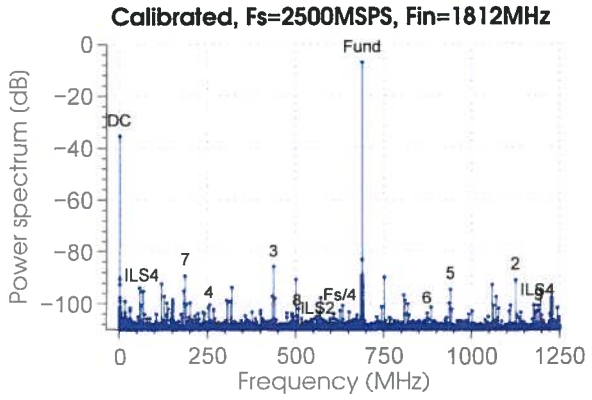


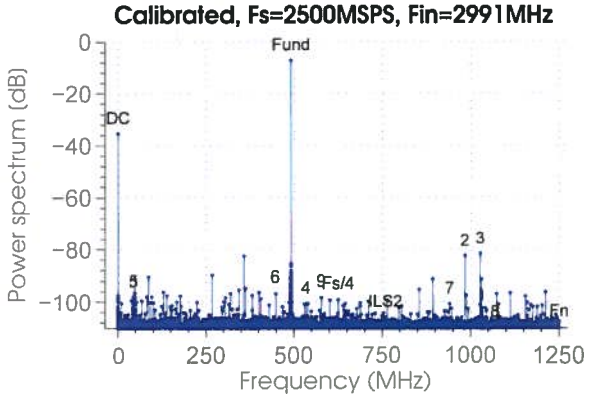


FFT Spectrum - Fs=2.5G, Fin@2nd/3rd Nyquist Band









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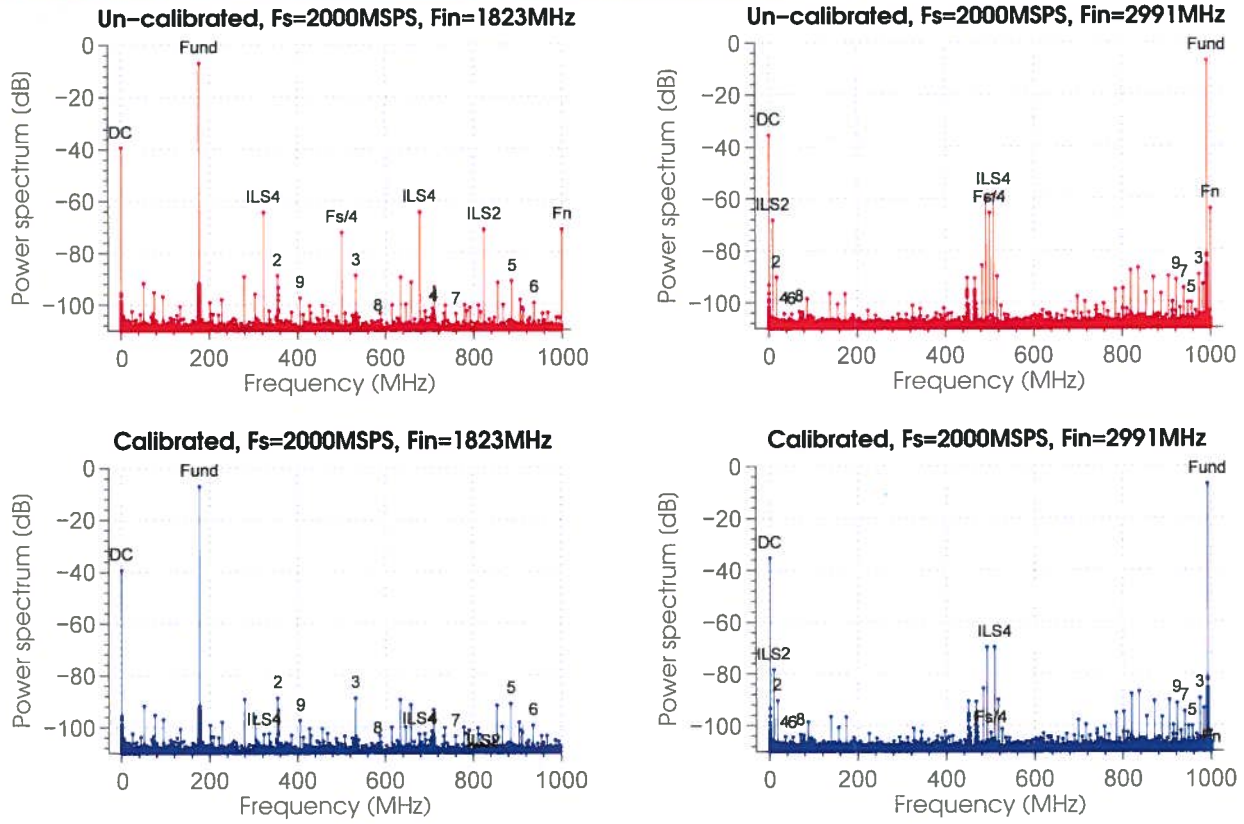
FFT Spectrum - Fs=2.0G, Fin@2nd/3rd Nyquist Band



Discussion on Calibration Results

- The interleaving error for all frequencies @ 2.5GSPS are suppressed to sub -83dBc and meets the specification.
- Near-Nyquist performance
  - 988MHz/2991Mhz @ 2.0GHz has less superior performance due to the deviation of regenerated errors.
    - Larger ripple and the magnitude response roll-off at corner frequency of the derivative filter.
    - The corner frequency is designed as $0.99F_N$ for these two cases while $0.9F_N$ for others with the same number of taps
  - Deviation of the regenerated errors will be relaxed for wide-band signals.
  - To improve it to sub -80dBc for these two cases, we need to increase the number of taps of the derivative filter to reduce the ripple.
- Over-Nyquist calibration
  - Mismatch coefficient estimation for Over-Nyquist frequencies are done as if the input falls in the 1st Nyquist band.
  - Calibration still works well for single tone even though the extracted coefficients are wrong due to the 1st Nyquist band assumption.
  - The current scheme cannot solve multi-tone or wide-band over-Nyquist input, and requires redesign of the error regeneration scheme. (under development)

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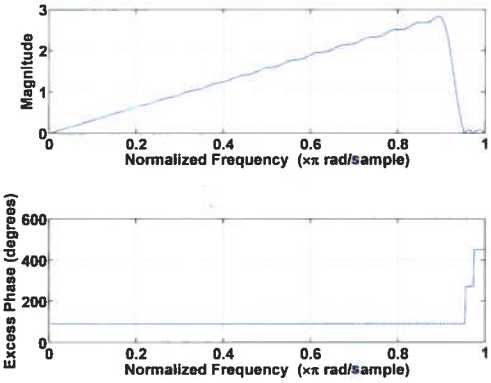
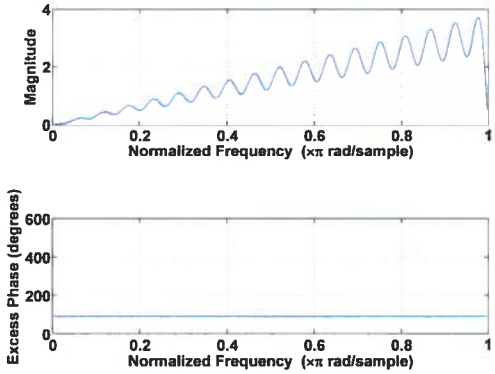
Limitation of Near-Nyquist Calibration

- Frequency responses of designed derivative filter are shown
  - Order = 70
  - Group delay = 35 cycles
- Large ripples are due to the small transition band designed for near-Nyquist input.





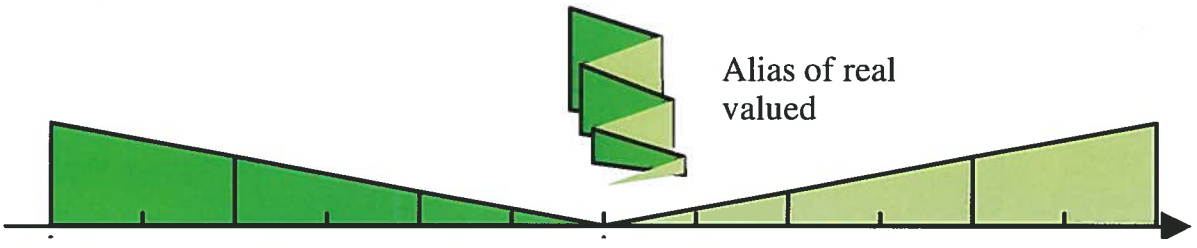
Corner frequency $= 0.9F_N$
Transition band $= 0.9 \sim 0.95F_N$

Corner frequency $= 0.99F_N$
Transition band $= 0.99 \sim 0.995F_N$

Over-Nyquist Calibration for Timing Mismatch

Some observations:

- Each Nyquist band aliases back to the 1st after sampling by TI-ADC.
- The same timing skew mismatch causes different amount of mismatch errors.
- The timing mismatch errors of over-Nyquist input is shown below(assuming flat input spectrum)



Some ideas:

- Input signal can fall in one of the Nyquist bands only.
- Use digital Hilbert filter plus derivative filter to regenerate timing mismatch errors
- Even Nyquist bands require reversed derivative filter, which can be realized by frequency shifting $(\times(-1)^n)$

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Calibration Procedure

Each raw data record has 262144(2^{18}) samples. A total of two replicated records are used for each case

- 1st record: extracted coefficients are settled during the first record.
- 2nd record: FFT analysis to validate the effectiveness and compare against manufacturer's plots

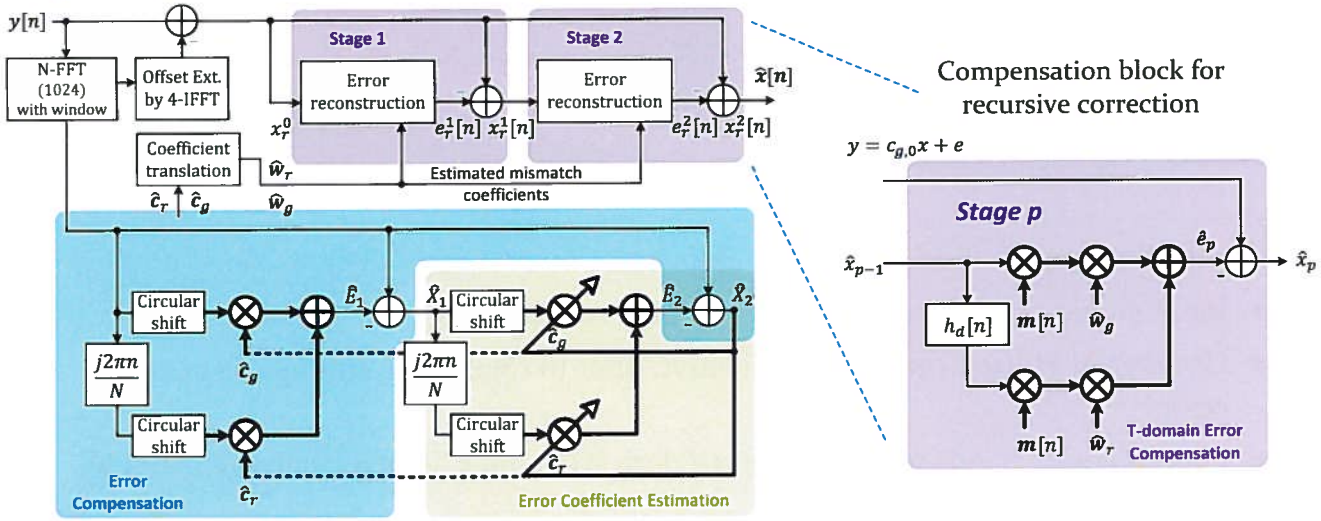
Hybrid-domain approach

- Mismatch estimation in the frequency domain; mismatch error correction in the time domain
- Aforementioned diffusive subband adaptive filtering are used to calibrate gain mismatch / timing skew.
- Direct offset mismatch extraction and correction for sinusoidal input signal. A more general offset mismatch calibration scheme is still under development.

Hybrid-domain Calibration Scheme

Hybrid-domain approach, concurrent offset/gain/timing mismatch calibration

- Raw data passes through FFT to frequency domain blocks. No cross-domain loops.
- 2-stage correction, 1024 subbands for high performance.
- Time-domain correction uses Hadamard transform and a different basis to regenerate errors for hardware efficiency.
- Offset "mismatch" est.: Direct extraction.



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Offset Calibration Method

Calibrate the "mismatch" of offset, not individual absolute offset since the input might have DC component.

- Offset is treated as DC input that does not undergo channel transfer function.
  - Linear combination of input spectra becomes spikes at $k\frac{F_s}{M}$
  - For sinusoidal input or sparse spectrum where $k\frac{F_s}{M}$ has no signal, $x_{OS,m}$ can be derived from IDFT
- Offset "mismatch" can be calculated similarly
  - Take 3 bins at $k\frac{F_s}{M}$ (Assume $M=4, k=1-3$)
  - set DC bin to 0
  - perform 4-IFFT
  - subtract the results from each channel

$$Y(e^{j\omega}) = \sum_{k=0}^{M-1} X(e^{j(\omega - k\frac{2\pi}{M})}) \breve{H}_k(e^{j(\omega - k\frac{2\pi}{M})})$$

$$\breve{H}_k(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} H_m(e^{j\omega}) e^{-jkm\frac{2\pi}{M}}$$

$$\Rightarrow Y_{OS,k} = \frac{1}{M}\sum_{m=0}^{M-1} x_{OS,m} e^{-jkm\frac{2\pi}{M}}$$

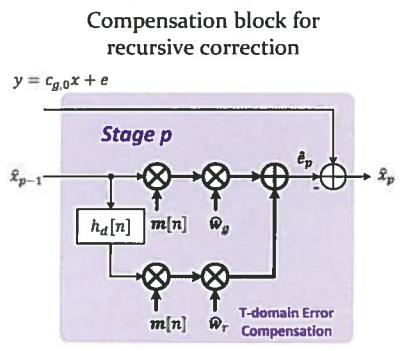
$$= DFT\{x_{OS,m}\}$$

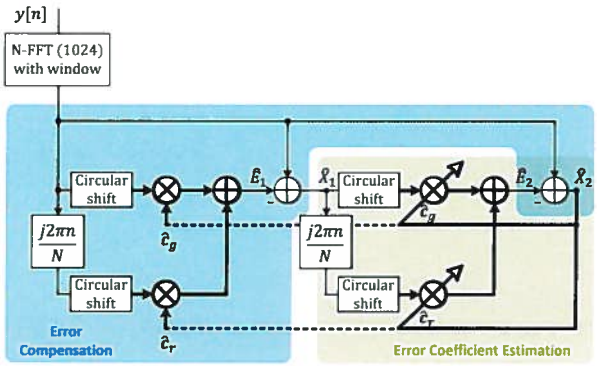
$$x_{OS,m} = IDFT\{Y_{OS,k}\}$$

For crowded spectrum with content at multiples of channel frequency, longer term averaging or adaptation is required to avoid loss of information.

Finite Word Length (FWL) Consideration

- Extra bits required on the main signal path to correct the offset mismatch.
- Benefit of Error Regeneration and Subtraction
  - Intensive computation on error regeneration path, which has much smaller dynamic range associated with the the mismatch parameters. WL can be reduced accordingly.[Matsuno 2013, Tsui 2014]
- Multiplication reduction
  - In the time domain, full multiplication for frequency shifting can be reduced by applying Hadamard transform (multiplying by 1 and -1).
  - In the frequency domain, frequency shifting is replaced by shift register.





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Summary

- RF signal processing and advanced adaptive filtering are brought in to tackle TI-ADC mismatch problem.
- Intuitive modeling of TI-ADC mismatch and spectral analysis
- Comprehensive correlation analysis and problem solving framework
- Effective and expandable correlation-based calibration schemes and techniques are developed accordingly
- Results of simulation and verification on raw data from commercial IC show the effectiveness of our calibration scheme.

Acknowledgment

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Glossary-1

Symbol	Definition
M	No. of channels of TI-ADC
F_S	Overall sampling rate of TI-ADC
x/X	TI-ADC input in the time/frequency domain
y/Y	TI-ADC output in the time/frequency domain
g_m	Individual channel gain for channel m
$S_m(f)$	Individual single-pole low-pass transfer function for channel m
Δ_m	Individual timing skew of channel m
$H_m(f)$	Channel Transfer Function (CTF) of channel m
f, Ω	Frequency in hertz / radian
k	Frequency shift index
$\breve{H}_k$	Error Transfer Function (ETF) at frequency shift index k
$c_{g,k}$	Lumped coefficient for gain mismatch at k
$c_{r,k}$	Lumped coefficient for timing skew mismatch at k
e_k/E_k	Error component caused by channel mismatch at k in the time/frequency domain
$\overrightarrow{k}$	Frequency shift to the right by $j\frac{2\pi}{M}k$

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Glossary-2

Symbol*	Definition
R	Correlation function or Covariance matrix
U_k	Hyperbolic distorting function at k
$\mathcal{O}$	Higher order terms
$\hat{}$	Estimate of the variable
$\boldsymbol{u}$	Interference vector composed of $x_{\vec{k}}$ and $x'_{\vec{k}}$
$\vec{\boldsymbol{x}}$	Interference vector composed of $x_{\vec{k}}$
$\vec{\boldsymbol{x}'}$	Interference vector composed of $x'_{\vec{k}}$
$\boldsymbol{w}$	Mismatch coefficient vector composed of $c_{g,k}$ and $c_{r,k}$
μ	Step size of LMS algorithm
$\boldsymbol{m}$	Modulating signals to perform frequency shifting
$h_d[n]$	Impulse response of a derivative filter
σ	Standard deviation
e_r^i, x_r^i	The ith reconstructed error, e, and input x
$\boldsymbol{w}_g$, $\boldsymbol{w}_r$	Mismatch coefficients when using Hadamard transform to represent errors
$x_{OS,m}$	Individual offset of channel m

* Bold fonts are used to represent vector forms.

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