# A 0.84pJ/cycle Wheatstone Bridge Based CMOS RC Oscillator with Reconfigurable Frequencies

Peiyu Chen[1], Dai Li[1], Zhanghao Yu[1], Qing Jin[2], and Kaiyuan Yang[1]
[1]Department of Electrical and Computer Engineering, Rice University, Houston, USA
[2]Xi'an Jiaotong University, Xi'an, China
peiyu.chen@rice.edu, jinqing@xjtu.edu.cn, and kyang@rice.edu

***Abstract*—A low-power CMOS RC relaxation oscillator supporting reconfigurable frequencies is presented for time-keeping in low-power Internet of Things (IoT) devices. The oscillator employs a Wheatstone Bridge (WB) scheme to relax the constraint between reference current and reference resistance existing in prior arts. In addition, adjusting the resistor ratios in WB supports reconfigurable frequencies and allows the use of smaller resistors for lower frequencies, saving chip area. Measurements of the prototype in 180nm CMOS show an average temperature coefficient down to 9.6ppm/°C at nominal 67kHz across -20°C to 100°C, with an energy efficiency of 0.84pJ/cycle and an active area of 0.145mm². Oscillations at 17kHz and 154kHz are also demonstrated by tuning the resistor ratio of WB.**

***Keywords*—CMOS; low power; RC oscillator; relaxation oscillator; frequency lock-loop; Wheatstone Bridge**

## I. Introduction

Internet-of-Things systems are usually duty cycled to save power and rely on timers to wake up, synchronize and timestamp. In order to satisfy the cost, battery lifetime and volume constraints of battery-powered IoT devices, fully integrated PVT-invariant RC relaxation oscillators have been studied as an attractive low-cost and low-power replacement for off-chip crystal oscillators [1-6]. Power consumption and frequency stability are the most important metrics. Conventional open-loop RC oscillators suffer from delay variations of the comparators and buffers (Fig. 1(a)), limiting the overall temperature stability even with various compensation techniques [1-3]. Even though excellent stability is achieved in [4] with ΔΣ-Modulator, its relatively high power consumption limits its application to many IoT-related areas. The most plausible approach for low-power kHz-range timer is the closed-loop design in [5], where a switched capacitor (acting as a frequency-dependent resistor), an amplifier, and a VCO form a frequency-locking loop to lock oscillator frequency, completely removing the impacts of comparator delay. In this architecture, the common-mode (CM) input range of the amplifier imposes a constraint on the reference current ($I_{REF}$) and the reference resistance ($R_{REF}$), leading to a trade-off between power and chip area. Because $R_{REF}$ is limited by chip area and cost, $I_{REF}$ must be large enough, making it the dominant part (~48%) of the total power (Fig. 1(b)). In this paper, we present a reconfigurable oscillator architecture using a Wheatstone-Bridge (WB) scheme that breaks the constraint on $I_{REF}$ and $R_{REF}$, which features: (1) an average temperature coefficient down to 9.6ppm/°C at nominal 67kHz; (2) an energy efficiency of 0.84pJ/cycle,

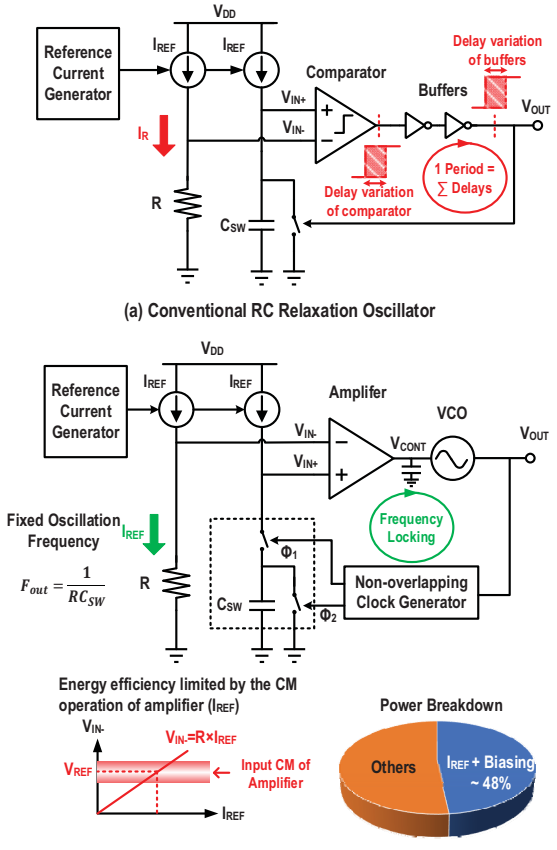


Fig. 1. Working principles of (a) the conventional relaxation oscillator [1] and (b) the current-limited frequency-locking relaxation oscillator [5].

representing a 46% reduction compared to prior arts in similar frequency range; (3) reconfigurable frequencies by adjusting resistor ratios in WB, making the design more flexible and suitable for wider applications.

## II. System Architecture

As shown in Fig. 2, the WB consists of $R_1$, $R_2$, $R_{REF}$, and a switched capacitor ($C_{SW}$). The WB, the amplifier, and the VCO forms a frequency-locking loop, which locks the output frequency ($f_{OUT}$) to $1/(R_{REF}C_{SW})\times(R_1/R_2)$. Here, the voltage across the resistors is no longer restricted by the CM input range of the amplifier. Therefore, the current passing through both

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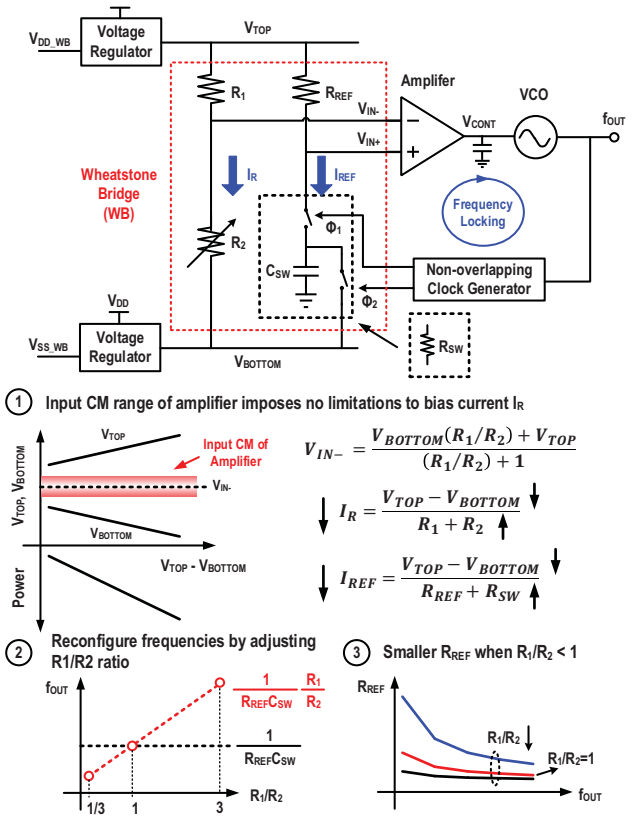


Fig. 2. Working principle and three major advantages of the proposed voltage-limited frequency-locking scheme using a Wheatstone-Bridge scheme.

branches of the bridge can be significantly reduced. Since the left branch only provides a reference voltage $V_{IN-}$, power consumption can be further reduced by increasing $R_1$ and $R_2$, as long as their ratio remains constant. The properties of $R_1/R_2$ ratio in WB bring additional advantages: (1) it provides a degree of freedom to change $f_{OUT}$; (2) when this ratio is less than 1, a smaller $R_{REF}$ can be used to produce the same $f_{OUT}$ compared with [5], which is especially beneficial for generating low-frequency reference under a given area constraint.

Frequency error against reference frequency can be analyzed and optimized through a linearized model at the stable condition: $f_{OUT} = f_{REF}$ (Fig. 3). The system is linearized by subtracting an offset of $f_{norm} - f_{REF}$, where $f_{norm}$ refers to the VCO's normal oscillation frequency when $\Delta v_{amp,out} = 0$, i.e. when the control voltage is the common-mode (CM) output of the amplifier. The impact of $\Delta v_{IN-}$ on $f_{error}$ is suppressed by the system loop gain, which includes the amplifier's gain ($A_v$), the VCO's gain ($K_{VCO}$), and the linearized gain of the frequency-to-voltage converter ($G_{FVC}$, the switched cap and $R_{REF}$ in WB). Here, $G_{FVC}$ is the derivative of $\Delta v_{IN+}$ with respect to $f_{OUT}$ at the linearization condition ($f_{OUT} = f_{REF}$). According to the system's closed-loop gain, ideally no frequency error against $f_{REF}$ exists, if $f_{norm}$ is equal to $f_{REF}$. In the proposed architecture, the WB converts $f_{OUT}$ to $V_{IN+}$. Its gain, $G_{FVC}$, is dependent on both $R_1/R_2$ ratio and the voltage across WB, i.e. $V_{TOP} - V_{BOTTOM}$. When $R_1/R_2$ deviates from one to produce a different frequency, $G_{FVC}$ is decreased but it can be compensated by increasing $V_{TOP} - V_{BOTTOM}$, with a few nano-Watts power overhead. On the other

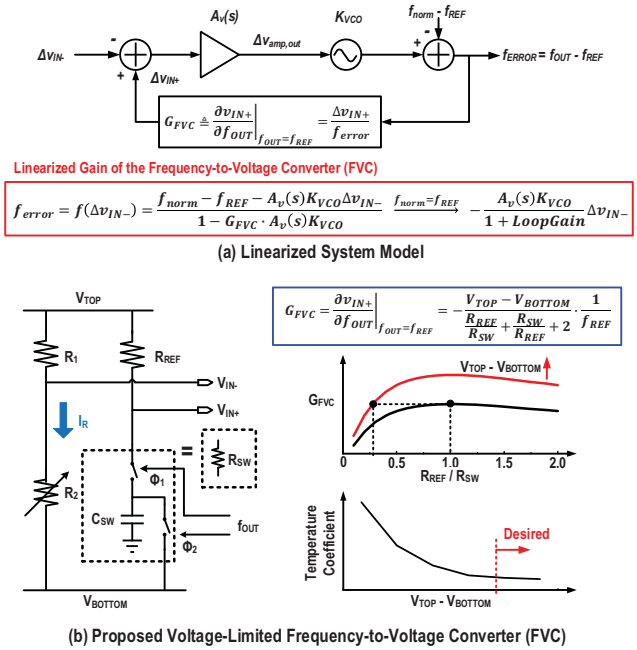


Fig. 3. (a) Linearized system model of the proposed oscillator and the close-loop gain. (b) A theoretical analysis of the linear gain in the voltage-limited frequency-to-voltage converter, which affects frequency error and depends on resistor ratio $R_{REF}/R_{SW}$, and the voltage across the WB ($V_{TOP}$ - $V_{BOTTOM}$).

hand, $V_{TOP} - V_{BOTTOM}$ must be larger than a certain value (around 150mV based on measurements) to achieve a large enough system loop gain.

## III. Circuit Implementation

Fig. 4 shows the detailed implementation of the proposed reconfigurable oscillator architecture. The WB consists of a diode chain, a temperature-resilient resistor ($R_{REF}$), and a switched capacitor ($C_{SW}$). $R_1$ and $R_2$ in the reference path (Fig. 1) are implemented with a chain of eight diode-connected high-$V_T$ PMOS transistors to minimize $I_R$. Each transistor shows an effective resistance of 23MΩ. This chain supports seven resistance ratios ($R_1/R_2$) to adjust oscillator frequency. In the other path of WB, the temperature-independent reference $R_{REF}$ is implemented with a series of negative TC P+ poly resistors without silicide and positive TC P+ diffusion resistors without silicide. $C_{SW}$ is a MIM capacitor, which shows an almost zero TC. The two switches are driven by non-overlapping out-of-phase clocks from the VCO's output to avoid short current. Two capacitors ($C_{IN}$) are added to the inputs of the core amplifier in order to filter out fluctuations due to injected charges.

Two basic voltage regulators employing single-stage amplifiers and miller capacitors generate $V_{TOP}$ and $V_{BOTTOM}$ for the bridge. Their reference voltages $V_{REF\_T}$ and $V_{REF\_B}$ are generated from a single voltage reference consisting of stacked diode-connected NMOS transistors and a native NMOS [8]. Different voltages can be selected with a multiplexer. The stability requirements on the voltage references are not stringent because only the difference between the two references is important and the two voltages track each other. The core amplifier employs a folded-cascade topology in subthreshold region [5]. A 20pF filter capacitor ($C_{FILTER}$) is added to the

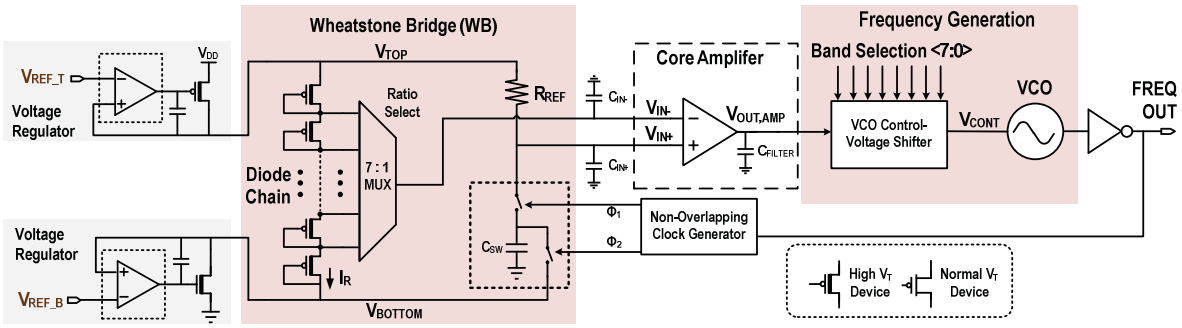


Fig. 4. System diagram of the proposed oscillator architecture based on frequency lock-loop with a WB and dual voltage supplies.

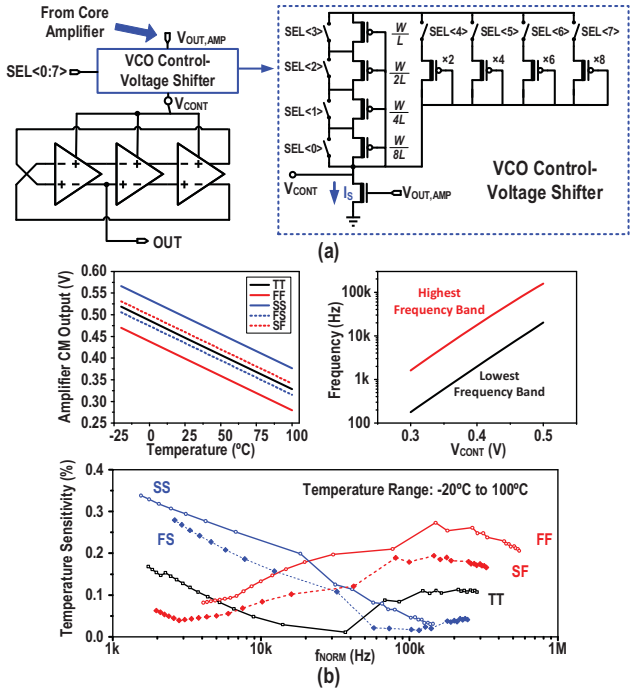


Fig. 5. (a) Circuit schematics of the VCO and its control voltage shifter to support reconfigurable $f_{norm}$. (b) Simulated temperature dependencies of the core amplifier's common-mode (CM) output and the VCO's $f_{norm}$ across -20°C to 100°C, and the sensitivity of the VCO. ($f_{norm}$ is the VCO's frequency when $V_{OUT\_AMP}$ equals CM output voltage of the core amplifier)

amplifier's output to stabilize the VCO control voltage and form a dominant pole for system stability purpose. The amplifier has an 87dB intrinsic gain and consumes 4nW. With the filter capacitor ($C_{FILTER}$) at the output, the amplifier has a -62 dB gain at the 67 kHz oscillation frequency.

In addition to the WB, frequency generation block is another critical component in the proposed architecture (Fig. 5(a)). The VCO is a three-stage ring oscillator. A constant energy-per-cycle differential stage is utilized [9]. As discussed in the linearized system analysis (Section II), frequency error can be suppressed when $f_{norm}$ is kept close to $f_{REF}$. Fortunately, since both the amplifier and the VCO operate in sub-threshold region, their temperature dependencies can cancel each other with proper sizing, providing a relatively stable frequency over temperature variations. To accommodate the core amplifier's wide CM output voltage range across PVT variations and different $f_{REF}$, a control-voltage shifter is employed, which

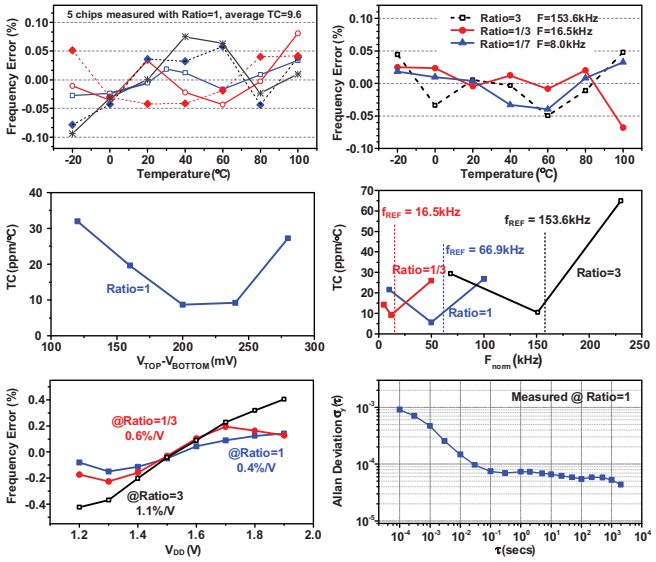


Fig. 6. Measured temperature sensitivity (TC) of the oscillator across -20°C to 100°C over five chips (top left) and at three different frequencies (by adjusting WB ratio, top right); TC with respects to $V_{TOP}$-$V_{BOTTOM}$ of the WB and the VCO's normal frequency (middle); line sensitivity under different WB ratios (bottom left), and (overlapping) Allan deviation (bottom right).

works as a tunable current mirror. Simulation results show that the VCO's $f_{norm}$, controlled by the CM output voltage of the core amplifier, has a temperature sensitivity of less than 0.35% from -20°C to 100°C across all voltage shifter settings and all five corners. Therefore, it covers frequencies from a few to hundreds of kilohertz with a temperature-insensitive $f_{norm}$ and a high VCO gain, resulting from its sub-threshold operation (Fig. 5(b)).

## IV. Measurement Results

The prototype is implemented in 180nm CMOS with an active area of 0.145mm$^2$. Measurement figures are provided in Fig. 6. When the resistor ratio ($R_1/R_2$) in WB is set to one, five measured chips demonstrate frequency errors within ±0.09% across -20°C to 100°C, with an average temperature coefficient (TC) of 9.6ppm/°C after applying standard two-point trimming. When the oscillator is reconfigured to different frequencies by adjusting the resistance ratio, it exhibits similar temperature dependencies. According to theoretical analysis in Fig. 3, the system's TC can be improved by increasing $V_{TOP} - V_{BOTTOM}$. This argument is validated by the measured results: with ratio = 1, by increasing $V_{TOP} - V_{BOTTOM}$, the measured TC starts

TABLE I. COMPARISON TABLE OF STATE-OF-THE-ART LOW-POWER CMOS RELAXATION OSCILLATORS

| | This work | | | ISSCC 16' [6] | ISSCC 13' [1] | ISSCC 14' [3] | VLSI 12' [7] | JSSC 16' [5] | ISSCC 18' [4] | ISSCC 17' [2] |
|---|---|---|---|---|---|---|---|---|---|---|
| Technology | 180nm | | | 180nm | 65nm | 65nm | 60nm | 180nm | 180nm | 65nm |
| Frequency (KHz) | 66.9 | 16.5 | 153.6 | 3 | 18.5 | 32.8 | 32.8 | 70.4 | 7e3 | 1.35e3 |
| Area ($mm^2$) | 0.145 | | | 0.506 | 0.032 | 0.015 | 0.048 | 0.26 | 1.59 | 0.005 |
| TC (ppm/°C) | 9.6[a] | 6.1 | 9.8 | 13.8 | 38.5 | 38.2[c] | 16.7[a] | 34.3[a] | 3.85[b] | 96 |
| Temperature Range (°C) | -20 to 100 | | | -25 to 85 | -40 to 90 | -20 to 90 | -20 to 100 | -40 to 80 | -45 to 85 | 0 to 150 |
| Number of Samples | 5 | | | 1 | 1 | 5 | 4 | 5 | 12 | 2 |
| Line Sensitivity (%/V) | 0.4 | 0.6 | 1.1 | 0.49 | 1 | 0.09 | 0.125 | 0.75 | 0.18 | 0.49 |
| Supply Voltage Range (V) | 1.2 to 1.9 | | | 0.85 to 1.4 | 1.3 to 3.3 | 1.15 to 1.45 | 1.6 to 3.2 | 1.2 to 3 | 1.7 to 2 | 0.9 to 1.9 |
| Power (nW) | 56 | 20 | 113 | 4.7 | 120 | 190 | 4480 | 110 | 750 | 920 |
| Energy/Cycle (pJ/Cycle) | 0.84 | 1.47 | 0.74 | 1.6 | 6.5 | 5.8 | 136.6 | 1.56 | 93.8 | 0.7 |

[a] Average value of measured samples [b] Calculated using box method [c] Max value among measured samples.

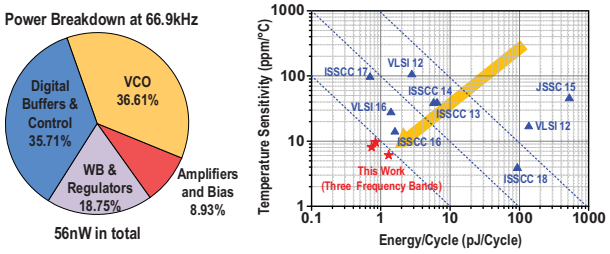


Fig. 7. Power breakdown of the prototype and performance comparison to state-of-the-art low-power CMOS relaxation oscillators.

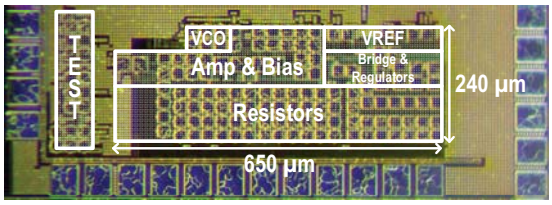


Fig. 8. Die micrograph of the reconfigurable relaxation oscillator.

decreasing until the impact of $V_{TOP} - V_{BOTTOM}$ on the system closed-loop gain becomes saturated. Restricted by the test chip tuning structure, when $V_{TOP} - V_{BOTTOM}$ is large, $V_{IN+}$ leaves the CM input range of the amplifier so that the system loop gain is reduced and TC worsens. This issue can be improved by deploying a higher-resolution voltage control scheme for the WB. The impact of another factor, $f_{norm}$, on TC is also experimentally validated at three different ratios (Fig. 6, middle right). Apart from the temperature dependencies, the prototype chip shows a measured supply voltage sensitivity of 0.42%/V when the ratio is 1. The measured Allan deviation has a noise floor around 50ppm (Fig, 6, bottom right). Thanks to the benefits introduced by the WB, the prototype chip has a measured power consumption of 56nW at 66.9kHz, corresponding to 0.84pJ/Cycle at 66.9kHz. As shown in Fig. 7, the WB and the regulators only consume 19% of the total power. Compared to prior arts, this design further improves the product of energy efficiency and temperature sensitivity, which are the two most important metrics for low-power timers. Performance summary and comparison to state-of-the-art low-power timers are presented in Table 1. The die photo is shown in Fig. 8.

## V. CONCLUSIONS

In summary, this paper presents a low-power CMOS timer with a Wheatstone Bridge based frequency-locking relaxation oscillator. Utilizing the Wheatstone Bridge with dual voltage regulators eliminates the extra power required for bias current in prior arts, and supports tunable oscillation frequencies with no area overhead. A linearized system model is introduced to analyze the frequency locking mechanism in the proposed architecture and guide the optimization. A prototype in 180nm achieves best-in-class 9.6ppm/°C temperature sensitivity and 0.84pJ/cycle energy efficiency, leading to a further improved product of these two critical metrics for low-power on-chip CMOS timers, when compared to prior arts.

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