A 1-V 99-to-75dB SNDR, 256Hz-16kHz bandwidth, 8.6-to-39µW Reconfigurable SC ΔΣ Modulator for Autonomous Biomedical Applications

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***Abstract*— The paper presents a reconfigurable Delta-Sigma Modulator (ΔΣM) suitable for three operation modes, whose application ranges from bio-potential signal monitoring to hearing aids. A feed-forward 2nd-order SC ΔΣM architecture with 4-bit quantizer is selected according to an analytic power optimization procedure. The ΔΣM features programmable sampling capacitors in the first integrator and novel reconfigurable power-gated OTAs to adjust power consumption in each operation mode. An asynchronous embedded SAR converter implements low-power quantization and passive addition in the feed-forward topology. The prototype is implemented in a 0.18µm CMOS technology and operates from a supply voltage of 1V. Measurements show peak SNDRs from 99 to 75dB for signal bandwidths spanning from 256Hz to 16kHz, achieving figures of merit which are almost constant in the different modes, and range from 0.20 to 0.27pJ/c.s.**

I. INTRODUCTION

The growing demand of autonomous sensor nodes for bio-medical applications requires the development of power-efficient analogue-to-digital converters (ADCs) [1]. There is an on-going trend to design ADCs that are power-scalable (i.e. their power consumption scales with bandwidth and resolution) and maximize energy efficiency in all their operation modes [2]-[12]. Furthermore, reconfigurable ADCs able to address a number of applications are attractive for their high added value and shared development time, while their area can be comparable to that of tailored implementations achieving similar performances. A number of reconfigurable Nyquist ADCs have succeeded in keeping state-of-the-art figure of merit (FoM) for different operation modes [2]-[3], but their resolution is typically below 12 bits, which is a limitation for high-performance bio-medical signal acquisition readouts. Reconfigurable delta-sigma modulators (ΔΣMs) offer higher resolution, but the solutions reported in literature [4]-[12] till now did not succeed in keeping the FoM minimum and constant in all modes of operation.

This paper presents a feed-forward (FF) 2nd-order switched-capacitor (SC) ΔΣM with a 4-bit quantizer that can be used for EEG, ECG, EMG and hearing aids. The experimental results show that this ΔΣM IC can be configured from 99 to 75dB peak SNDR and 256Hz to 16kHz bandwidth (BW) (see Table I). The power consumption ranges from 8.6 to 39µW, achieving best-in-class figures of merit (from 0.2 to 0.27pJ/c.s.) in the target SNDR range.

II. RECONFIGURATION STRATEGY FOR MINIMUM POWER

Table I summarizes the specifications for the different operation modes of the proposed ΔΣM: High-Resolution Low-BW (HRLB), Medium-Resolution Moderate-BW (MRMB), and Low-Resolution High-BW (LRHB) modes have been chosen to enable the digitization of bio-potential (EEG, ECG, EMG) and audio signals. Several reconfigurable ΔΣMs exist in literature [4]-[12]. A number of them employ high-order cascade architectures where stages are suitably switched on and off [5]. However, this results in increased power dissipation (to compensate for the mismatch between the cascade analogue and digital circuitry in the first stage, and

TABLE I. ΔΣM SPECIFICATIONS

	HRLB	**MRMB**	**LRHB**
Target application	EEG, ECG	EMG	Hearing aids
ENOB*	16	14	12
BW	256Hz	2048Hz	16kHz
OSR	128	64	32
Sampling frequency f_s	65kHz	262kHz	1.05MHz
First integrator $C_{s,1}$	16pF	2pF	0.5pF
OTAs' GBW	330kHz	1.3MHz	5.2MHz

*ENOB=(SNDR-1.76)/6.02

978-1-4799-0645-1/13/$31.00 ©2013 IEEE

to power the additional stages) and in area overhead (due to the additional integrators and quantizers in the last stages). Single-loop ΔΣMs can also enable power-efficient reconfigurability by suitably varying OSR, filter order, quantizer resolution, and featuring tunable passive components together with power-scalable analog core blocks [8]. The analitic-based method developed in [13] to design power-efficient single-loop SC ΔΣMs is applied here to determine the power-optimal ΔΣM architecture for each operation mode in Table I. After merging the solutions found for the three operation modes and simplifying the hardware to minimize area, the power-vs.-resolution trade-off is optimized by choosing a feed-forward (FF) 2nd-order SC ΔΣM architecture with a 4-bit quantizer. Programmable sampling capacitors in the first integrator $C_{s,1}$ and GBW-adjustable OTAs (see Figure 1) are used to scale power consumption in the different operation modes. To meet the required BW and resolution, the sampling frequency is tuned between 65kHz and 1.05MHz, implementing OSRs between 128 and 32.

III. Circuit Implementation

In our approach to reconfigurability, the sampling capacitors $C_{s,1}$ and the OTA of the first integrator are programmed to optimize the energy efficiency. Therefore, the ΔΣM is designed as thermal-noise-limited in each mode of operation while the equivalent load of the first integrator is minimized. The specifications listed in Table I for $C_{s,1}$ and for the GBW of OTAs are derived using the analytic approach described in [13] and verified using time-domain behavioural simulations. The ΔΣM behavioural model has been built using the blocks described in [14].

The embedded quantizer combines a 4-bit SAR ADC with passive addition [15] (see Figure 1). The SAR quantizer features a dynamic comparator so that its power automatically scales with the clock frequency. Its operation is asynchronous, so that it does not need an additional high-frequency clock. The programmable OTAs and the multi-bit SC DAC are described with more detail in the next sections.

A. Modular first-integrator C_s ($C_{s,1}$) implementation

The 4-bit feedback DAC is implemented as a capacitive array of 15 unit elements ($C_{s,1j}$ in Figure 1). The overall capacitance of $C_{s,1}$ is thus equal to the sum of the individual capacitances $C_{s,1j}$. Each $C_{s,1j}$ is programmed via two configuration bits, C_{SEL}<0:1>. The largest value of $C_{s,1j}$ (for the HRLB mode) is implemented by an array of 30 unit elements. Lower resolution modes reuse a subset of units, with no area overhead.

Three techniques are used to improve the linearity of the 4-bit DAC to a level enabling the maximum targeted SNDR. First, a data-weighted averaging (DWA) block is employed to provide a first-order shaping of the mismatch errors in the DAC capacitors [16]. The power of these errors is thus pushed to high frequencies and filtered out by the decimator filter. Second, boosting circuits [17] are used for the switches driven by f_1, f_2, $L_{p,i}$ and $L_{n,i}$ (Figure 1). Indeed, the non-linearity of the switches is mainly due to their input-voltage dependent ON-resistances (r_{ON}). An overdrive voltage as

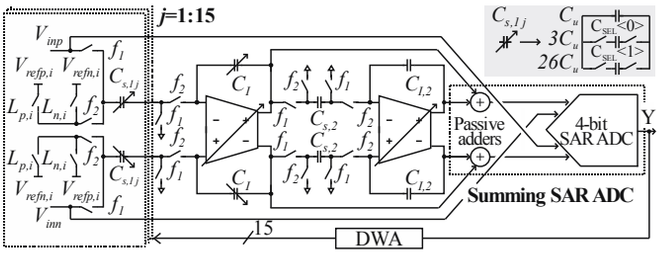
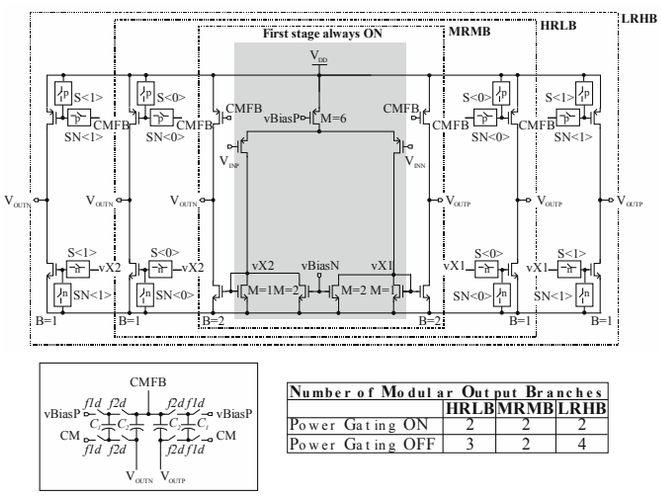


Figure 1. Implementation of the proposed reconfigurable ΔΣM.

constant as possible is thus needed to minimize the switch r_{ON} variation. Finally, transmission gates and a driving voltage larger than V_{DD} (provided by a separate 1.2-V supply, $V_{DD,SW}$) are used for the static configuration switches driven by C_{SEL}<0:1> in the programmable sampling capacitors.

B. Programmable OTA for power- and speed-scalability

A programmable OTA capable of adapting its static power consumption and GBW to the sampling speed and capacitive load required by each operation mode is used in the first integrator. The most common approach to achieve this in literature consists in choosing a fixed circuit topology, with the input stage biased in weak inversion, and tuning the bias current to scale the GBW [5]. This approach, however, is not suitable for GBWs varying more than 10 times, as required by our specifications (see Table I). Another common approach is to use identical switchable amplifier cells in parallel [8]. In our architecture, we have implemented a new power-efficient gain-enhanced current-mirror OTA in which the input pair is biased with a fixed tail current and is always kept on. The total OTA GBW, which is proportional to the number of modular output branches, is adjusted by switching on/off these branches (Figure 2). A gain-enhanced current-mirror architecture has been chosen, as this arrangement offers high power-efficiency in terms of GBW per unit of current and capacitive load [18]. The gain enhancement technique is used to increase the gain by about 10-20 dB without compromising the BW and with no extra power consumption.



Number of Modular Output Branches			
	HRLB	MRMB	LRHB
Power Gating ON	2	2	2
Power Gating OFF	3	2	4

Figure 2. Proposed programmable gain-enhanced current mirror OTA.

The current-mirror OTA is also suitable for a low-voltage design thanks to its wide output swing. The DC gain of this OTA is limited as the amplifier employs a single stage with no cascoding. However, this is not an issue in our ΔΣM, as our FF architecture requires only ~40-dB of DC gain. The output branches are sized considering the targeted GBW and the equivalent load specification of each mode. This results in reduced power and smaller area when compared to using identical switchable amplifier cells in parallel [8], since the first stage is here shared among all the configurations. The trade-off between stability and GBW requires however careful design (the nodes associated to the second pole, vX1 and vX2, are loaded by the multiplexers S<0:1> and SN<0:1>). The worst-case phase margin is 70 degrees (in LRHB mode). The first OTA is power-gated during the sampling phase *f1,* to further reduce the static power of the modulator. During the power-gating operation, all switchable output stages of the first OTA are powered down.This results in a power reduction of up to 40% (in LRHB mode) with negligible circuit overhead and without affecting the modulator stability as the common-mode feedback (CMFB) loop is never interrupted.

IV. Measurements Results

The presented ΔΣM is implemented in a standard 0.18µm CMOS process, operates from a 1-V supply and occupies a net area of 0.59mm^2 (Figure 5). Figure 3 shows the measured output spectra in HRLB, MRMB and LRHB modes at the corresponding overload levels. This figure clearly shows a reconfiguration of the noise floor thanks to the adjustment of the sampling capacitors in the first integrator. The power consumption is only 8.6, 15 and 39µW for the HRLB, MRMB and LRHB modes, respectively. The power required from $V_{DD,SW}$ is negligible as this supply only drives static switches C_{SEL}<0:1> in the input SC DAC (see Figure 1). Table II summarizes the achieved performance. Figure 4 depicts the measured SNR/SNDR curves, showing peak SNDRs of 99dB, 87dB, and 75dB in the different modes. Figure 6 and Figure 7 respectively display the area- and power-efficiency benchmarking against state-of-the-art ADCs from [19]. Note that the area occupied by this chip is similar to those achieving similar maximum SNDR (99dB) and optimized for one mode of operation only. This demonstrates the high area efficiency of the proposed strategies for reconfigurability. Figure 7 demonstrates that the implemented ΔΣM achieves best-in-class power efficiency in both HRLB and MRMB mode, even when compared to point-optimized solutions. This confirms the effectiveness of the proposed power-reconfiguration and optimization techniques.

Table III and Figure 8 summarize the overall experimental performance and compares it with state-of-the-art reconfigurable ΔΣMs [4]-[12]. It is important to note here the improved power efficiency and the almost constant FoM (between 0.20 and 0.27pJ/c.s.) achieved while varying the resolution by 4 bits, the signal bandwidth by 64 times and the power consumption by 4.5 times.

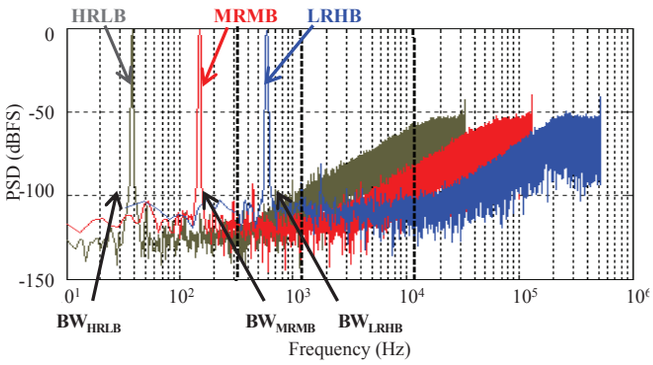


Figure 3. Measured spectra (65536 points) at overload levels.

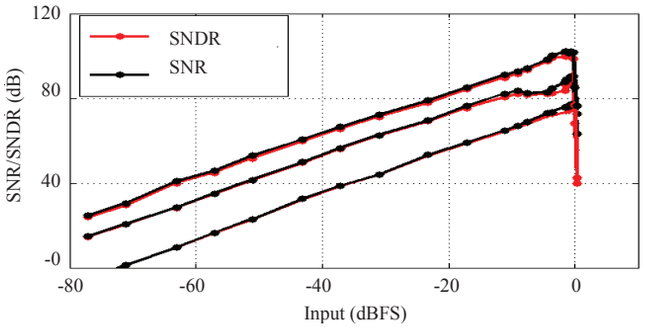


Figure 4. Measured SNR/SNDR vs. input amplitude.

TABLE II. Summary of the Measured Performance

	HRLB	MRMB	LRHB
SNR [dB]	100	90	77
SNDR [dB]	99	87	75
Power [µW]	8.6	15	39
BW [Hz]	256	2048	16k
FoM [pJ/c.s.]	0.23	0.20	0.27
Area [mm^2]	0.59		
CMOS process	0.18µm		
Supply [V]	1		

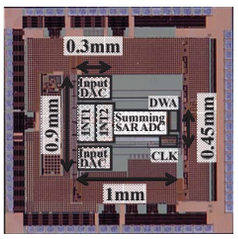


Figure 5. Chip photograph

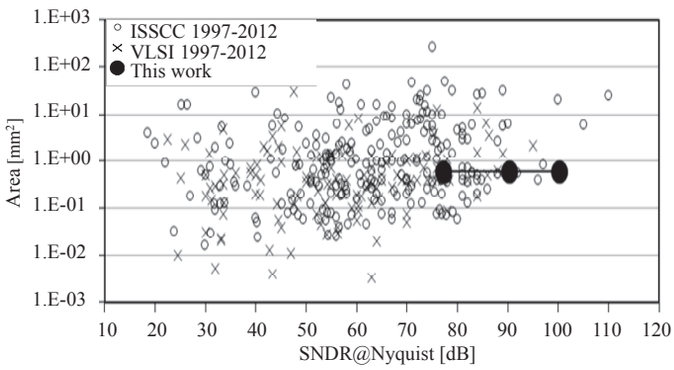


Figure 6. Area-efficiency benchmarking of state-of-the-art ΔΣMs [19].

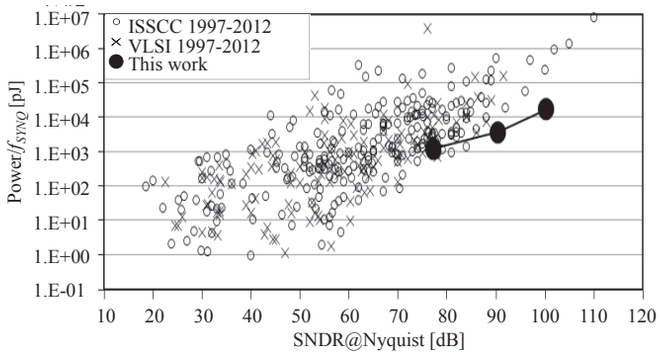


Figure 7. Power-efficiency benchmarking of state-of-the-art ΔΣMs [19].

TABLE III. SUMMARY OF PERFORMANCE AND COMPARISON WITH STATE-OF-THE-ART ΔΣMS

	SNR [bits]	SNDR [bits]	Power [µW]	BW [Hz]	FoM [pJ/c.s]	Area [mm²]	CMOS process	Supply [V]
Veldhoven [4]	15.0	15.0	2x4500	200k	0.58	2x0.18	0.18µm	1.8
	13.5	13.5	2x4100	1.228M	0.29			
	12.0	11.7	2x3800	3.84M	0.29			
Putter [7]	14.3	14.3	2600	135k	0.47	0.125	65nm	2.5
	13.3	13.3	3100	614k	0.25			
	11.8	11.8	3700	1.92M	0.26			
Crombez [8]	13.5	12.5	5000	500k	0.85	0.40	90nm	1.2
	12.7	12	6400	1.92M	0.41			
	11.5	11.2	4300	1.92M	0.49			
	11.7	11.3	5500	4M	0.27			
	10.8	10.5	6800	10M	0.24			
Ke [9]	13.8	13.3	2800	200k	0.68	0.4	90nm	1
	12.7	12.3	2600	500k	0.50			
	12.1	11.7	3600	2M	0.28			
	11.7	11.2	4900	4M	0.27			
	9.3	9	8500	20M	0.41			
This work	16.3	16.2	8.6	256	0.23	0.59	0.18µm	1
	14.7	14.2	15	2048	0.20			
	12.5	12.1	39	16384	0.27			

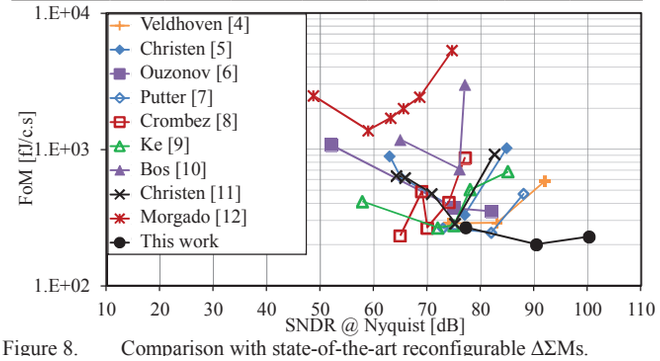


Figure 8. Comparison with state-of-the-art reconfigurable ΔΣMs.

V. CONCLUSIONS

A 1-V reconfigurable SC ΔΣM for autonomous bio-medical applications which features several strategies to achieve best in-class power and area efficiency has been presented. The OSR and the capacitance of the first-integrator sampling capacitors are changed to satisfy the specific thermal noise requirements of each operation mode. Power efficiency is guaranteed by using a 2nd-order SC architecture with a 4-bit quantizer, together with configurable sampling capacitances (Figure 1) and programmable OTAs, whose GBW and power scale with the required OSR (Figure 2). Power-efficient and power-scalable quantization is achieved using a summing SAR quantizer [15]. As shown in Figure 6, there is no area overhead despite the achieved reconfigurability. The chip achieves best-in-class FoMs both in HRLB and MRMB modes, while the FoM is kept almost constant (between 0.20 and 0.27pJ/c.s.) over the different operation modes (see Figure 7).

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