A 0.1-5GHz Dual-VCO Software-Defined ΣΔ Frequency Synthesizer in 45nm Digital CMOS

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***Abstract* — A wide-band frequency synthesizer architecture for software defined radio applications is presented, based on a dual-VCO ΣΔ phase locked loop (PLL), with a wide-range modulus programmable divider. The design combines high flexibility to cover several wireless standards, with a scalable implementation, exploiting the capabilities of advanced digital technologies at reduced area costs. The prototype in 1.1-V 45-nm digital CMOS achieves a 4.3 to 10GHz PLL tuning range, with programmable K_{VCO}, bandwidth, between 110 and 320 KHz, and current consumption, ranging from 20 to 29 mA. Measured phase noise is -122dBc/Hz at 2-MHz offset from a 7.2GHz carrier.**

***Index Terms* — software-defined radio, phase locked loops, voltage controlled oscillators, programmable dividers.**

I. Introduction

Evolution in wireless communications keeps on driving RF-IC design based on the requirements of next-generation transceivers. Ubiquitous connectivity and the continuous addition of new standards are pushing towards a reconfigurable, Software-Defined Radio (SDR) platform to cover a broad range of noise and linearity specifications, while offering optimal power/performance trade-offs [3]-[5]. Moreover, cost reduction requires RF circuitry to be integrated with digital processors in the latest CMOS technology, with no analog options [1][2]. Nanometer technologies (≤45nm) are, however, well-known to only bring faster operation (improved device transition frequency) to analog designs. In fact, scaling adversely affects most other relevant parameters (e.g. gain, signal-to-noise ratio and passive device quality) so that building high-performance systems out of practically impaired technology has become a big challenge.

An SDR local oscillator (LO) should combine the most demanding requirements (e.g. low phase noise for cellular standards) with large frequency tuning range while being competitive to dedicated single-mode implementations with respect of power consumption and cost. The recently proposed digitally-intensive approaches to advanced frequency synthesizer design, culminating into "all-digital" phase-locked loop (PLL) architectures, are very promising to address the challenges delineated above [6]. On the other hand, in this paper, we show how, starting from a "classical" analog architecture, multi-mode *programmability* can be combined with *scalable design* techniques to exploit the speed capabilities of scaled digital technologies at limited area overhead due to passive devices.

We describe the concept, design and measurement results of a fully reconfigurable ΣΔ frequency synthesizer in 45-nm digital CMOS, which has been embedded in the SDR receiver in [3]. The main aspects of our architecture include: (i) two LC voltage-controlled oscillators (VCOs) to cover a full octave frequency band, up to 10GHz (feasible in 45-nm CMOS); (ii) low-complexity quadrature frequency generation based on compact, cascaded divide-by-2 cells, to avoid analog-intensive techniques such as poly-phase filters or single-side-band (SSB) mixing; (iii) a modular PLL divider architecture supporting seamless ΣΔ dithering on a wide-range modulus; (iv) hybrid CMOS/current-mode logic (CML) implementation of both PLL and LO distribution dividers, to optimally trade speed with phase noise and power consumption. In what follows, all these aspects will be illustrated together with the frequency synthesizer building blocks.

II. Frequency Synthesizer Architecture

To generate the LO quadrature signals, we discard power-hungry techniques, such as poly-phase filters, multiplication, or SSB mixing [4][8], which tend to generate spurious tones, in favor of cascaded divide-by-2 circuits (Fig. 1). In fact, in 45-nm CMOS, a fundamental VCO frequency up to 10 GHz is obtainable, whereas 2 parallel VCOs centered at different frequencies can cover up to a full octave tuning range. Since at these high frequencies only small inductors are used, the area overhead is also limited. We therefore propose a dual-VCO, fourth order, type-2 ΣΔ fractional-N PLL, where all building blocks can be programmed for different carrier

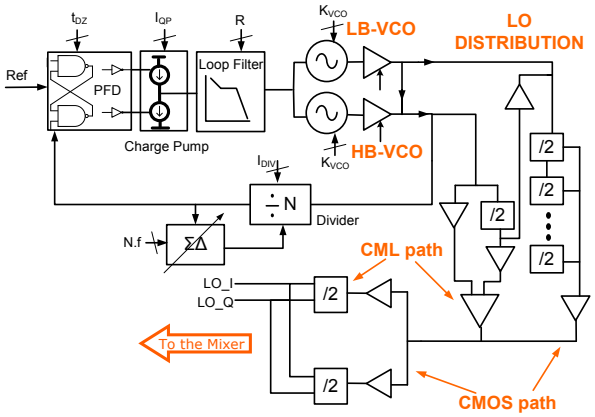

Fig. 1. Simplified diagram of the proposed dual-VCO, reconfigurable, fractional-N ΣΔ frequency synthesizer

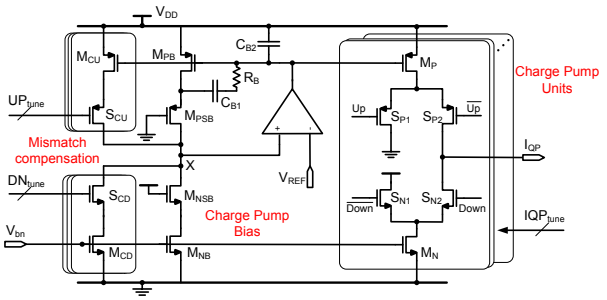

Fig. 2. Basic diagram of the PLL charge pump (V_{REF}=0.5V)

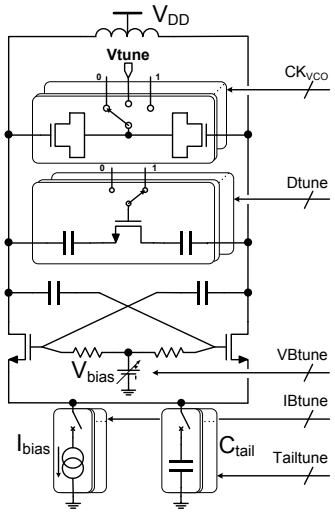

Fig. 3. Simplified reconfigurable LC-VCO schematic

frequencies, VCO sensitivities, loop bandwidths, phase noise and power consumptions. Based on the application, a CML multiplexer selects the desired VCO. The frequency distribution and division-in-quadrature circuit (FDDQ) generates LO signals in the whole 0.1-5 GHz band of interest, using a dual CMOS/CML path of up to 6 divide-by-2 blocks, with the constraint that the VCO never runs at the RF frequency, to avoid the well-known pulling problem in direct conversion radio architectures. The CMOS path provides full swing, for lower phase noise, and small power consumption, while the CML path is also implemented for the highest frequencies.

The PLL leverages a phase-and-frequency detector (PFD) architecture robust to crossover distortion [10], with programmable dead-zone delay t_{DZ} between 0.86 ns and 1.55 ns, to allow fine tuning for different charge pump current settings. The charge pump (CP) current I_{QP}, also programmable between 45µA and 360µA, is obtained by using 8 parallel units mirroring the current of a replica biased circuit (Fig. 2). Since 2.4% mismatch in the up and down currents can increase the integrated noise by 5dB, binary-weighted switchable NMOS and PMOS current units are added to allow mismatch compensation by pushing (pulling) additional current into node X (Fig. 2). I_{QP} is fed into the low impedance input of a 3rd order reconfigurable active RC filter [10]. While keeping the total amount of capacitance constant (~200pF), the filter configures its resistors to allow for cross-over frequency tuning between 110 and 320 KHz. VCO and divider architectures are described in the following sections.

III. Voltage Controlled Oscillators

The LC-VCOs (Fig. 3) adopt a power efficient class-C NMOS differential-pair topology [9] to produce the largest oscillation amplitude for a given bias current in the current limited regime. In both the 7–10GHz high-band (HB) and 4.3-7.2GHz low-band (LB) VCOs, the tank inductor is a center-tapped single U-turn coil, drawn in the topmost metal, shunted with the superficial aluminium redistribution layer. Using the same inductor leads to larger power consumption, but also lower phase noise, in the LB-VCO, a desirable trade-off for the SDR cellular mode. Low phase noise values, for a given tank amplitude, call for larger tank capacitance and smaller inductance (0.4nH in our case) based on analysis in [9]. A small inductance value is also preferred to increase the tuning range.

We use coarse frequency tuning to split a large tuning range into smaller bands. This allows covering our range of interest without increasing the VCO sensitivity K_{VCO}, which would increase the level of the PLL spurs and phase noise. Coarse frequency band selection is done with a 6-bit low-cost MOM capacitor array, programmed by *Dtune*. Within each band, the tank capacitance is then finely tuned through an array of 15 differential NMOS varactors. Based on the value of CK_{VCO}, these can be switched on or off for fine band selection, or connected to the tuning voltage *Vtune* to control the VCO gain for optimal PLL design [7]. For instance, K_{VCO} can be

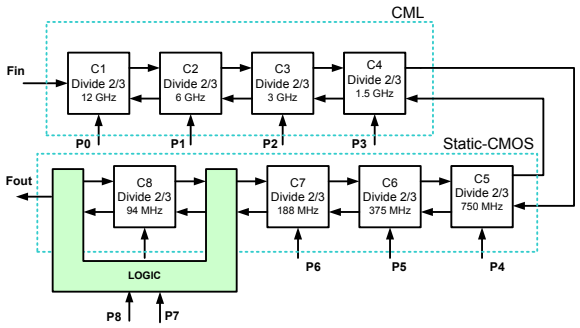

Fig. 4. Enhanced Range Divider supporting seamless ΣΔ divide modulus dithering

programmed to linearly scale with the PLL frequency to provide constant bandwidth. Each VCO can further trade performance for power consumption, by also adjusting the bias current, the gate bias voltage, as well as the tail capacitance C_{tail} regulating transistors' operation region. A 4-bit DAC, ac-coupled with the gates of the transistor pair, generates the gate voltage V_{bias}. The VCO active core negative resistance is therefore also tuned through the bias current and the gate voltage V_{bias}. However, differently than in [7], the active core is never switched, since changing transistor dimensions does not help improve noise [9]. On the other hand, it will increase circuit complexity and may even compromise performance due to the addition of the switches.

IV. Enhanced Divider Architecture

With a few tens of MHz reference crystal, a divider with a wide programmable range, e.g. from 128 to 511, is needed after a 4-10GHz VCO. The PLL divider, based on [11], adopts a modular, adaptable architecture consisting of a cascade of divide-by-2/3 cells (Fig. 4). Since M cells provide division ratios from 2^M to 2^{M+1}-1 (controlled by inputs P), we need 8 cells to cover a 256-511 range. Moreover, by shunting out cell *C8* (using an additional control bit *P8*) we can use the first 7 cells to cover ratios in [128-255]. While the above structure is enough for integer division, additional logic is needed for correct fractional-N mode operation. In fact, with a third order ΣΔ modulator, we expect the modulus to vary in the [N-3 N+4] interval because of dithering. Therefore, for N in [252-258], swapping between 7-cell and 8-cell configuration should be smooth. If no precautions are taken when switching dynamically from 7-cell to 8-cell mode, the division factor during the first period will not be defined. This effect would ruin the intended operation of the ΣΔ control. To support seamless switching, we employ bit *P8* to control a multiplexer that mutually

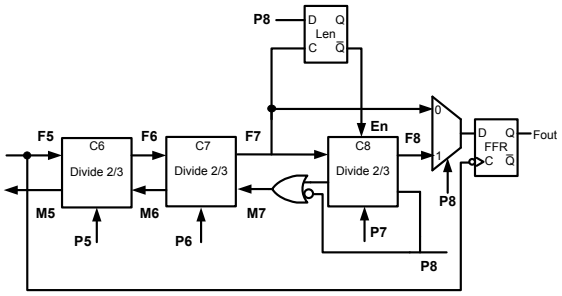

Fig. 5. Additional logic to support seamless switching between 7-cell and 8-cell architecture

selects the divider output *F8* or *F7*. Moreover, *P8* is also complemented and latched by *F7* (output of *C7*) to cell *C8* as an additional input *En* such that *F8* is 0 when *En* is 1. With these modifications, when *P8* moves from 0 to 1, both outputs *F7* and *F8* are 0 and there is no glitch at the multiplexer output. When *P8* moves from a 1 to 0, the output *F8* is preset to 0 for future switching. Finally, the divider output is also re-timed by the higher frequency output *F5* to reject jitter and compensate for divide-modulus dependant delays between *C7* and *C8*. The four highest frequency cells adopt differential CML, whereas the remaining ones leverage full-swing single ended static-CMOS. A buffer after *C4* performs differential-to single-ended conversion.

The sigma-delta modulator driving the divider modulus is MASH 1-1-1 with 24-16-8 bit accumulators [12], but can also be configured as a MASH 1-1. Moreover, a 22-bit LFSR is included for dither addition to the LSBs.

V. Measurement Results

The synthesizer has been fabricated in plain vanilla 45nm CMOS (Fig. 6) and occupies, without decoupling, about 1.02×0.4mm^2, of which approximately 53% are occupied by the VCOs and 30% by the filter. All configuration bits are sent through a serial link to a network-on-chip. VCO outputs are brought off chip for testing after a buffer designed in CMOS logic. Points in Fig. 7 represent all available (overlapping) coarse and fine tuning curves, after programming the LB and HB VCOs to provide a constant K_{VCO}/f_0, using a procedure adapted from [7]. The combined VCOs cover a 4.3 to 10GHz band providing 51% (LB) and 32.4% (HB) tuning ranges. Fig. 8 shows the measured PLL phase noise around 7.2GHz in both integer and fractional mode. Integrated phase noise in a 10MHz bandwidth is -31dBc. Even if the measured inductor Q was only 9 (40% worse than expected from simulations), –122dBc/Hz phase noise was measured at 2MHz offset, which can be extrapolated to –160dBc/Hz at 20MHz from a 900MHz carrier. Although the LB-VCO is not optimized for power efficiency in these conditions, it

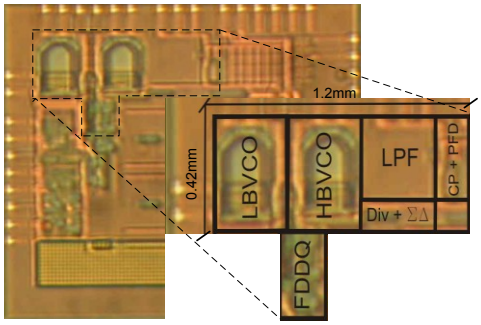

Fig. 6. Frequency synthesizer micrograph

TABLE I
PLL POWER AND PHASE NOISE AT DIFFERENT CARRIER FREQUENCIES

Freq. (GHz)	$\mathcal{L}${2MHz} (dBc/Hz)	P_{VCO} (mW)	P_{PLL} (mW)
5.12	-125	19.8	31.3
6	-123	16.5	28
7.2	-122	11	22.5
8	-118	13.2	24.7
9	-116	9.9	21.4

consumes around 10mA, which implies a phase noise figure-of-merit [9] of 183dBc/Hz. Table 1 reports PLL phase noise and power at different carrier frequencies.

VI. Conclusion

We have presented a frequency synthesizer in 45-nm CMOS for software defined radio applications. A wide range of carrier frequencies is generated through a chain of divide-by-2 cells from a fully reconfigurable dual-VCO, fractional-N PLL. We have reported details for the low phase noise VCO and the divider providing seamless sigma-delta dithering over a wide modulus range. Although used in an analog architecture, our solutions are general and can be applied to all-digital PLLs.

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References

[1] R. Staszewski et al., "A 24mm^2 Quad-Band Single-Chip GSM Radio with Transmitter Calibration in 90nm Digital CMOS," *ISSCC Dig. of Technical Papers*, pp. 208-209, Feb. 2008.

[2] S. Kousai et al., "A 1.2V 0.2-to-6.3GHz transceiver with less than -29.5dB EVM@-3dBm and a choke/coil-Less Pre-Power Amplifier," *ISSCC Dig. of Tech. Papers*, pp. 214-215, Feb. 2008.

[3] V. Giannini, P. Nuzzo, C. Soens, K. Vengattaramane, M. Steyaert, J. Ryckaert, *et al.*, "A 2mm^2 0.1-5GHz SDR Receiver in 45nm Digital CMOS," *ISSCC Dig. of Technical Papers,* Feb. 2009.

[4] J. Craninckx, M. Liu, D. Hauspie, *et al.*, "A Fully Reconfigurable Software-Defined Radio Transceiver in 0.13µm CMOS," *ISSCC Dig. of Technical Papers,* pp. 346-347, Feb. 2007.

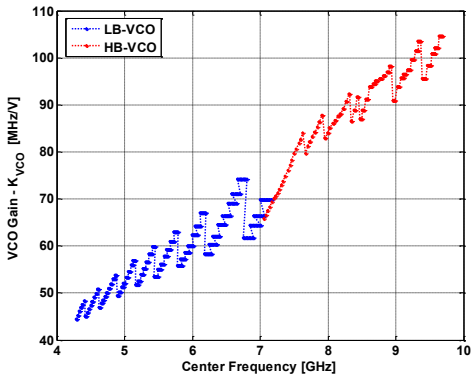

Fig. 7. Total frequency range spanned with a VCO gain programmed to be proportional to the center frequency

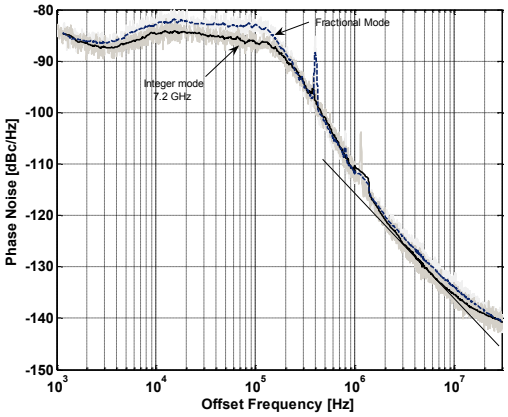

Fig. 8. PLL phase noise from a 7.2GHz (integer mode) and 7.2004 GHz (fractional mode) carrier

[5] M. Ingels et al., "A CMOS 100 MHz to 6 GHz Software Defined Radio analog front-end with integrated Pre-Power Amplifier", *Proc. of Europ. Solid-State Cir. Conf.*, pp. 436-439, Sept. 2007.

[6] R. B. Staszewski, *et al.,* "Digitally Controlled Oscillator (DCO)-Based Architecture for RF Frequency Synthesis in a Deep-Submicrometer CMOS Process," *IEEE Trans. on Cir. and Syst.—II*, vol. 50, no. 11, Nov. 2003.

[7] D. Hauspie, E.-C. Park and J. Craninckx, "Wideband VCO with Simultaneous Switching of Frequency Band, Active Core and Varactor Size," *IEEE Journal of Solid-State Circuits,* July 2007.

[8] J. Van Driessche, J. Craninckx and B. Come, "Analysis and Key Specifications of a Novel Frequency Synthesizer Architecture for Multi-Standard Transceivers," *IEEE Radio and Wireless Symposium*, pp. 481-484, January 2006.

[9] A. Mazzanti, P. Andreani, "Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise," *IEEE Journal of Solid-State Circuits,* vol.43, no.12, pp. 2716-2729, Dec. 2008.

[10] J. Craninckx and M. Steyeart, *Wireless CMOS Frequency Synthesizer Design*, Kluwer Academic Publishers, Dordrecht, the Netherlands, 1998.

[11] C. S. Vaucher, *et. al.*, "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35-µm CMOS Technology", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1039-1045, July 2000.

[12] Y.-C. Yang, *et. al.*, "A Quantization Noise Suppression Technique for Fractional-N Frequency Synthesizers", *IEEE Journal of Solid State Circuits*, Vol. 41, No. 11, pp.2500-2510, Nov. 2006.