18.1 A Fully Integrated 24GHz UWB Radar Sensor for Automotive Applications

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Radar-based advanced safety systems are crucial to reduce road accidents caused by driver inattention. An actual and pervasive adoption of radar technology requires the development of low-cost Silicon-integrated sensors, including microwave, analog, and digital blocks on a single chip, able to replace existing discrete electronics based on compound semiconductors. Indeed, the considerable advantage of Silicon lies in its natural capability for integration that will enable a higher level of complexity in such sensors. Recent Silicon implementations [1, 2] have proved the maturity of both high-speed bipolar and submicron CMOS processes for multi-GHz applications, such as 24GHz automotive short-range radar (SRR). However, the implementation of a complete radar sensor on a single chip is still very challenging and involves a proper radar architecture (i.e., continuous-wave or pulsed radar), efficient detection methodology, a robust radio front-end structure and customized local DSP. In this scenario, UWB sensors based on analog correlation RX represent an attractive solution for a cost-effective automotive SRR [3].

This paper presents a fully integrated 24GHz UWB radar sensor implemented in a 0.13µm SiGe BiCMOS process. Figure 18.1.1 shows a simplified block diagram of the proposed UWB radar sensor, which is based on a correlation detection scheme. The UWB signal generation takes advantage of a PLL. The produced 24.125GHz carrier is properly BPSK modulated to increase sensor robustness within the entire SRR sensor network. Then, it is pulsed using the switch *SW_TX* that is driven by the pulse generator (PG). The resulting 24GHz UWB signal is properly amplified by the PA to comply with emission mask regulations [4]. The RX section adopts a homodyne conversion architecture and consists of an I/Q variable-gain downconverter, a two-stage VGA and a coherent integrate-and-dump stage. The RX performs a time-gated correlation between the echo signal and a delayed replica of the TX pulse (using the switch *SW_RX),* and then integrates the correlation signal. Finally, the control unit (CU) produces all the control signals required for pulse transmission and echo detection. In particular, CU triggers the pulse generation and the BPSK modulation, controls the RX window timing, sets the pulse width T_{pulse} and modifies the RX gain. It also adjusts the integration (T_{INT}) and dump (T_{DUMP}) times to integrate multiple signal replicas, thus increasing SNR.

Figure 18.1.2 depicts the detailed schematic of the I/Q downconverter. It consists of a fully differential three-stage LNA (Q_1-Q_{18}), which is transformer-coupled to a Gilbert quad pair (Q_{21}-Q_{28}). An input single-ended-to-differential conversion is implemented on chip by the stacked transformer T_{in}. The downconverter achieves a power conversion gain as high as 30dB, while preserving linearity. The Gilbert quads are directly driven by the secondary coil signal currents of T_{L3}. The LNA also includes a variable-gain functionality to further relax the linearity requirements in case of high input levels. Each LNA stage adopts a transformer-loaded cascode topology to guarantee both high stable gain and reverse isolation. Simultaneous noise and 50Ω input impedance matching is obtained by properly sizing transistor $Q_{1,2}$, emitter inductors L_{E1} and capacitor C_{in}. Geometrical parameters of multi-layer interleaved transformers T_L were accurately designed by means of extensive electromagnetic simulations, to maximize gain performance in the whole UWB frequency range. Emitter inductors L_{E1}-L_{E3} were implemented by means of folded microstrips to maintain a complete layout symmetry, which is of utmost importance to save actual benefits of differential architecture, especially at multi-gigahertz frequencies. A reliable low-resistance/low-inductance ground plane was designed, which makes use of an appropriate multi-layer pattern to comply with stringent metal density requirements.

To mitigate the effects of FMCW radar interference at 24.125GHz, the downconverter is ac-coupled to the VGA with series capacitors. The VGA consists of two differential cascode stages with digitally-selectable load resistances. By means of control bits (b_1 to b_3), a dB-linear gain characteristic is achieved from 6 to 36dB with a 2GHz bandwidth. Finally, an analog G_m-C integrator performs a coherent collection of the received pulses, producing a target detection signal at the I/Q terminals. The output voltage of the integrator is a function of the RX gain, the G_m/C ratio and the integration time T_{INT}. Offset compensation circuitry reduces the false alarm probability due to erroneous overcoming of the detection threshold.

Figure 18.1.3 shows simplified schematics of main blocks of the TX, i.e. the BPSK modulator, the switch, the PG and the PA. The BPSK modulator is based on a simple differential pair driven by the CTRL_BPSK signal and the switch uses a current-steering topology to produce the 24GHz modulated pulse. The PG provides the baseband pulse with two different widths, i.e. 1ns and 0.5ns, according to the required radar resolution. Finally, the PA, which adopts a differential cascode topology with transformer resonant load, was designed to deliver 0dBm and 3dBm output power by setting the bias current I_{PA} for T_{pulse} of 1ns and 0.5ns, respectively. Output transformer T_{L4} adopts an interleaved coil structure with a turns ratio of 2:1. It provides differential-to-single-ended conversion of the output signal. Thanks to its inherent galvanic isolation, transformer T_{L4} guarantees robustness while avoiding common ESD protection structures, which greatly affect RF performance.

Figure 18.1.4 shows the measured PSD at the TX output considering a typical antenna gain of 10dBi for T_{pulse} of 1ns and 0.5ns. The time pulse repetition (T_{PR}) is set to 270ns and 135ns, respectively. The spectra present the main lobe centered at 24.125GHz and two nulls, whose frequency span is 2GHz and 4GHz for 1ns and 0.5ns pulses, respectively. The PSD curves are compliant with the maximum allowed EIRP defined by the ETSI mask.

Figure 18.1.5 shows the measurement of the integrator output voltage as a function of different VGA gain levels for a 1ns RF pulse. The input pulse energy (E_{pulse}) is –143dBmJ. T_{PR} is set to 270ns. T_{INT} of 885µs and a reset signal of 10µs are adopted.

Figure 18.1.6 summarizes main measured performance of the UWB radar sensor. The die micrograph is shown in Fig. 18.1.7.

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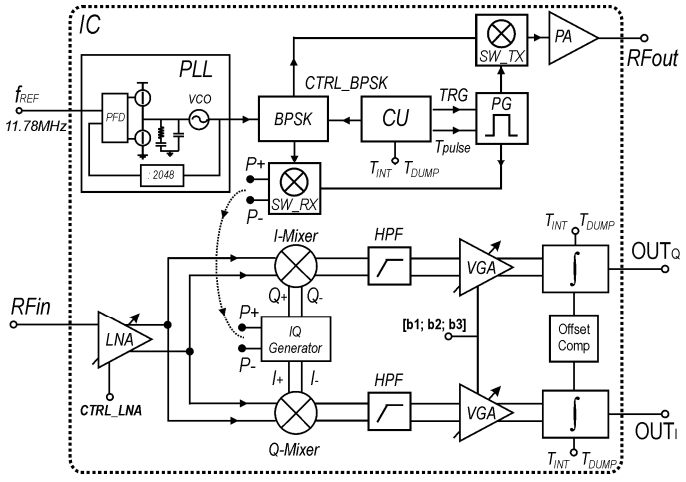

Figure 18.1.1: Block diagram of the UWB radar sensor.

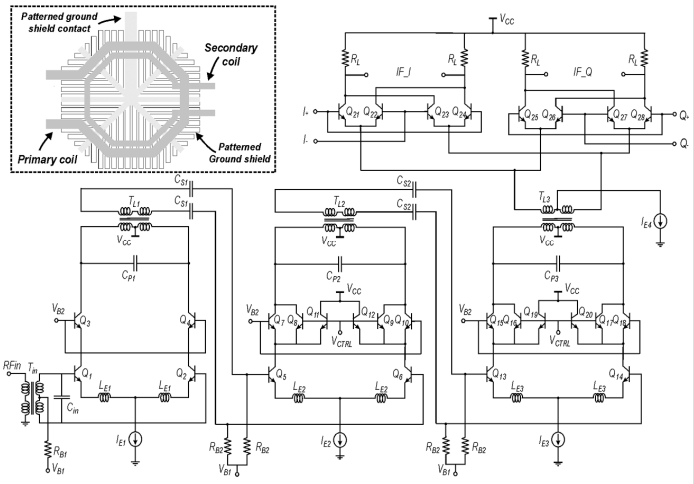

Figure 18.1.2: Detailed schematic of the I/Q downconverter and layout of transformers T_L.

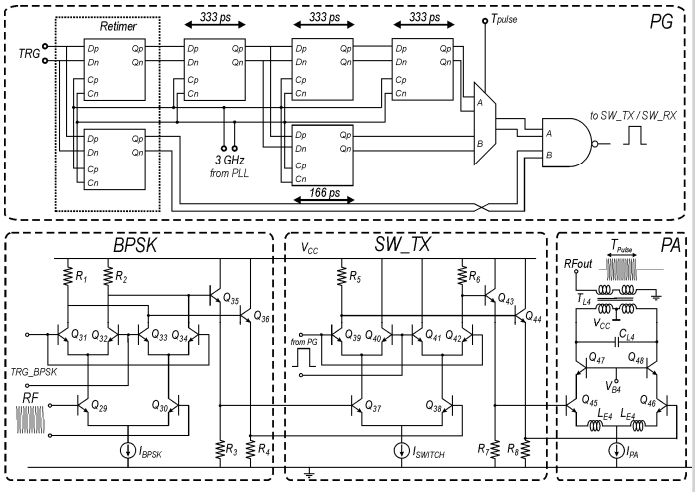

Figure 18.1.3: Simplified schematics of main blocks of the TX.

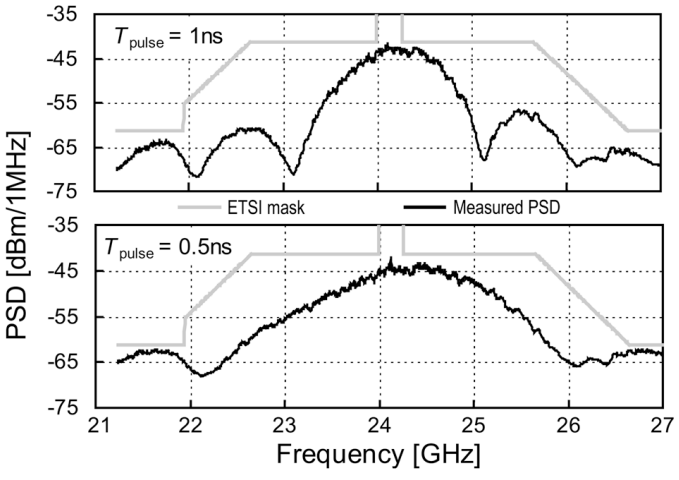

Figure 18.1.4: TX PSD with 10dBi antenna gain (T_{pulse}=1ns, T_{PR}=270ns ; T_{pulse}=0.5ns T_{PR}=135ns).

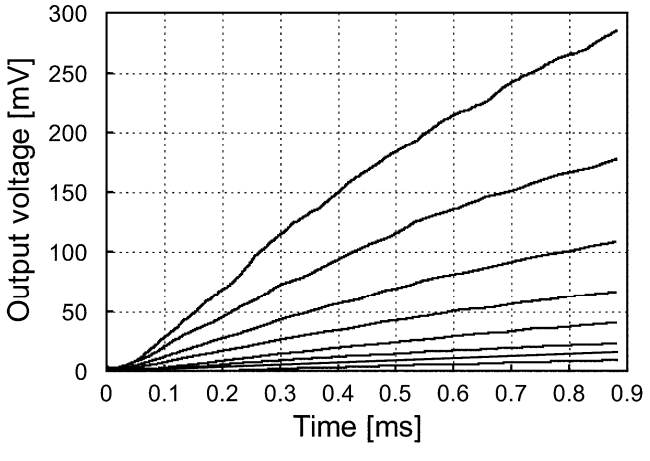

Figure 18.1.5: Target detection signal for different VGA gain levels (T_{pulse}=1ns, E_{pulse}= -143dBmJ, T_{PR}=270ns, T_{INT}=1ms, T_{DUMP}=10µm).

Down-converter max power gain [dB]	30
Down-converter NF [dB]	6
Down-converter input 1dB compression [dBm]	-15
VGA gain range [dB]	6 to 36
VCO phase noise @ 1MHz offset [dBc/Hz]	-104
VCO tuning range [GHz]	20.4 to 25.1
PLL spur level [dBc]	-50
PA max output power @ 24.125GHz [dBm]	3
UWB BW [GHz]	1.3 (T_{pulse} = 1ns, T_{PR} = 270ns) 2.1 (T_{pulse} = 0.5ns, T_{PR} = 135ns)
Current consumption [mA] (Supply voltage = 2.5V)	65 (I/Q Down-converter) 19 (VGA + Integrator) ; 32 (PLL) 7 (PA) ; 25 (BPSK + Switches)
Silicon area [mm^2]	9
Technology	0.13µm SiGe BiCMOS

Figure 18.1.6: Measured performance summary.

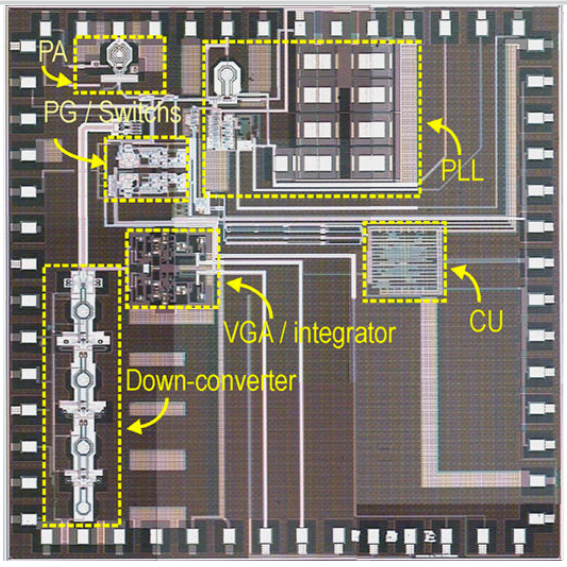

Figure 18.1.7: Die micrograph.

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