Intel 22nm FinFET (22FFL) Process Technology for RF and mmWave Applications and Circuit Design Optimization for FinFET Technology

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***Abstract*—** Intel 22FFL is a unique FinFET process technology optimized for RF and mmWave applications supporting superior RF performance to planar technologies with both f_t and f_{max} of NMOS above 300 GHz and 450 GHz respectively. Flicker noise improvement over planar technologies and excellent gain-power efficiency enabling low-power wireless applications are demonstrated.

I. Introduction

Recently, an advanced fabrication technology, known as FinFET technology [1], is needed to overcome the physical limitations of planar devices and continue the 50-year of Moore's law scaling.

In this paper, a performance summary of 22FFL process [2] and its suitability for RF/mmWave designs are demonstrated. Figure of Merits (FoMs) will be presented and contrasted with respect to planar CMOS technology. Furthermore, design methodologies to exploit advantages of FinFET technology will be briefly illustrated.

II. Overview of finFET Technology

This section will briefly introduce how FinFET technologies extend the longevity of silicon technology scaling and the difference of the FinFET devices due to the structural change.

A. Drain-Induced Barrier Lowering

As modern fabrication technology drives the device scaling to an extreme level, the drain starts interacting with the source directly through region beneath the channel regardless gate potential, which is called Drain Induced Barrier Lowering (DIBL). DIBL in planar technology starts dominating drain current beyond around 30nm process node as drain-source interaction exceeds the gate-channel control, resulting in higher leakage current. Planar technology damps the DIBL issue with high channel doping and halo channel doping, but has to sacrifice channel mobility and the noise performance.

FinFET technologies, however, virtually isolate the drain from the source by physically carving out the parasitic channel material outside of the gate influence forming a three-dimensional channel structure called 'fin' as shown in Fig. 1. Such a fully depleted fin separates the drain and source and prevents the drain field from encroaching into the source, therefore dramatically reduces DIBL effect. This enables scaling down the channel length beyond 30nm gate length without the listed degradation. At any given leakage current, transistor with stronger drive current, lower threshold voltage and higher output resistance and therefore higher intrinsic analog gain can be achieved as suggested in Fig. 2.

B. Nonlinear Gate Resistance

Unlike the planar devices, gate resistance in FinFET shows a non-linear relation with channel width as shown in Fig. 3. In addition to the horizontal components, because of the 3D nature of the 'fin', the gate material wraps around the fin generating a vertical component of the gate resistance. As channel width increases from the narrowest, the total gate resistance drops as vertical resistance, which dictates the total resistance, are connected in a parallel configuration. As the channel width continues to increase, the horizontal resistance becomes stronger, and the trend of the gate resistance turns into linear scaling by channel width as depicted in Fig. 4 [3].

As RF and mmWave circuit design are sensitive to gate resistance for quality factor (Q), stabilization and power delivery, device sizing for optimum gate resistance and performance balance will be discussed in section IV.

III. FinFET vs. Planar for RF/mmWave

This section will compare key RF performance Figure-of-Merits (FoMs) between FinFET and planar technologies to highlight the benefit of FinFET technology for RF and mmWave applications in addition to the scaling benefit.

A. Parasitic and RF Performance

One caveat of FinFET technologies is the increased lateral parasitic capacitance by the three-dimensional gate structure. The gate material between fins negatively impact on total gate capacitance without contributing to transconductance (g_m). Hence, as the poly pitch gets tighter, the parasitic capacitance increases, and thus the unity gain frequency (f_t) is lowered. Fig. 5 shows the recent f_t trend in silicon technology by process node.

FinFET technologies, however, have a potential to reach a higher maximum oscillation frequency (f_{max}) thanks to the vertical gate resistance components, and higher output resistance (R_{out}). Fig. 6 compares peak f_t and peak f_{max} between 22FFL FinFET technology and 32nm planar process technology.

B. Flicker Noise Performance

As hinted in Section II.A., halo implant (Pocket implant) is the widely used remedy to compensate the DIBL effect at the cost of flicker degradation due to V_T non-uniformity and extra traps at the interface [4]. The FinFET structure inherently suppresses DIBL effect, hence negates the need of halo implant and flicker noise improvement thereafter. Flicker noise silicon data collected from 22FFL thin oxide device are shown in Fig. 7 [2].

C. Gain-Power Efficiency

The less DIBL and fully depleted operation in FinFET technologies improves device gain per power dissipation efficiency, as FinFET devices can drive stronger drain current with less short-channel effect. The DIBL improvement drastically enhances the device current usability. Fig. 8 illustrates the gain-power efficiency FoM (GPFoM) of FinFET and Planar for comparison purpose. GPFoM is defined as GPFoM $= U \cdot g_m/I_d$ $[dB/V]$.

Note that Mason's gain (U or Unilateral gain) is used for the FoM to accommodate the performance metrics at mmWave frequency range. The current density reaching the peak FoM is the optimum bias condition for the maximum gain-power efficiency. As shown in Fig. 8, 22FFL FinFET devices offer about 600dB/V improvement over planar technologies in the gain-power efficiency at 30GHz.

22FFL process offers five flavors of RF transistor, which are low-leakage nominal and low V_T (LL_nom, LL_lvt), high-density nominal and low V_T (HD_nom, HD_lvt), and high-performance (HP). The RF performances of and HP RF transistor in peak f_t and peak f_{max} configurations are provided in Fig. 9 and Fig. 10. Both f_t and f_{max} measurement include up to Metal 2 routing; the second lowest metal layer for realistic usage condition. As shown in Fig. 9 and 10, NMOS RF transistors reach above 300GHz of f_t and 450GHz of f_{max} respectively, while PMOS achieves slight below 300GHz of f_t and f_{max}. The results demonstrate a superior f_{max} and a competitive f_t performance to leading-edge RF/mmWave silicon based technologies such as Fully-Deleted Silicon-on-Insulator (FDSOI) [5].

IV. Design Methodology with FinFET

This section introduces examples of how to utilize the distinguishable device properties of FinFET technologies for RF performance optimization, and also how to avoid reliability issue associating with FinFET structure.

A. Performance Optimization with Fin Self Heat Awareness

Fin-Self-Heat (FiSH in short) should be considered for circuit design. As FinFET strives for narrow fins for excellent electrostatics, this results in limited thermal conductance to dissipate heat generated in the channel.

Recent work has demonstrated an LNA design in 22FFL at 71 ~ 76GHz frequency range with FiSH limit consideration [6]. The authors swept MAG and NF_{min} for I_{DS} and V_{DS} accordingly under the maximum power limit for *FiSH*, and searched for the optimum supply voltage (V_{DS}) and the current (I_{DS}) for a single stage as shown in Fig. 11. The work achieves the target performance at the lower V_{DS} of 0.5V per single stage, and total two stage stacking with current sharing was suggested for higher gain performance with less power dissipation.

B. Device Sizing Consideration

The non-linear gate resistance in FinFET devices explained in section II. B. winds up various input impedance condition by the number of fin choice, despite the total equivalent device size; the product of the number of gate fingers and the number of fins. Therefore, it is strongly advised to consider the different number of fins for the device sizing in order to achieve higher correlation between optimum noise matching and the power matching by input impedance for low-noise amplifier designs.

Fig. 12 demonstrates three cases of fins configuration maintaining total device size by modulating the number of gate fingers. As one can notice, the maximum available gain G_{max} and the minimum noise figure NF_{min} are adjusted by the number of the fin, and the delta between G_{max} and NF_{min} is maximized by 4 or 6-fin device at J_d of 0.3mA/um.

V. Conclusion

FinFET technologies offer significant performance boosts for not only logic but also RF/mmWave over planar technologies. The three-dimensional fabrication technologies allow keeping Moore's law alive beyond the physical limit of the two-dimensional device fabrication. 22FFL is specially engineered to support both RF and mmWave applications with the best-in-class f_t and f_{max} reaching over 300GHz and 450GHz respectively, which provide the best opportunity to enable low-power mmWave applications in silicon technology.

Acknowledgment

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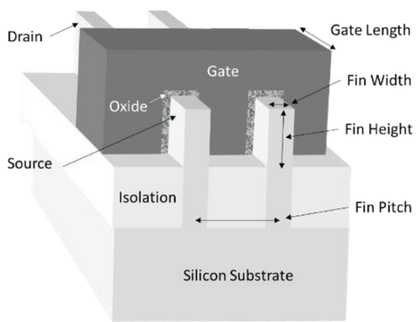


Figure 1: 3D view of FinFET device structure

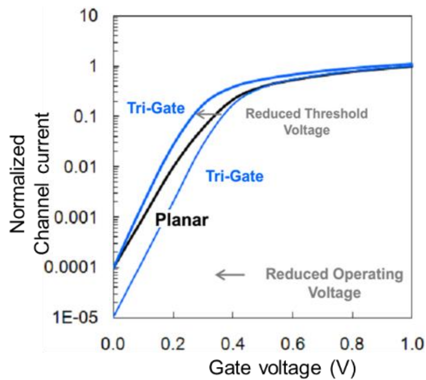


Figure 2:I-V curves of FinFET and Planar demonstrating DIBL improvement by FinFET technologies

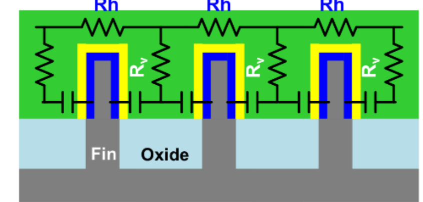


Figure 3: FinFET gate resistance structure: Horizontal resistance (R_h) and Vertical resistance (R_v) surrounding fin structures

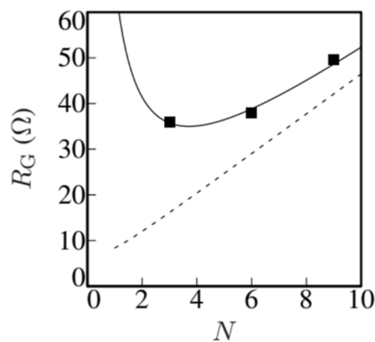
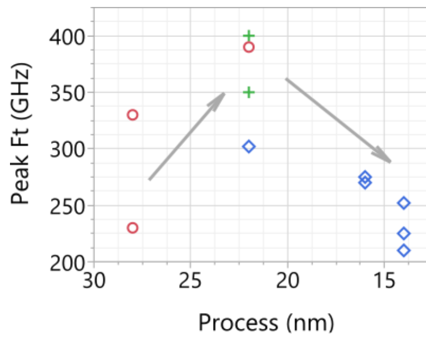


Figure 4: Gate resistance trend by channel width of FinFET devices [3]



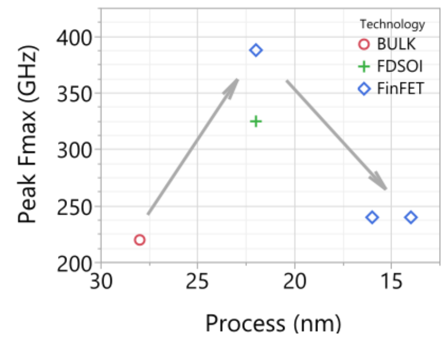
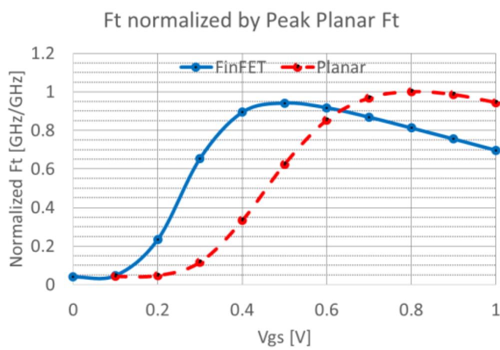


Figure 5: f_t and f_{max} trends by process node: both ft and fmax reach the peak performance around 20 ~ 25nm due to the excessive parasitic capacitance by high density interconnect



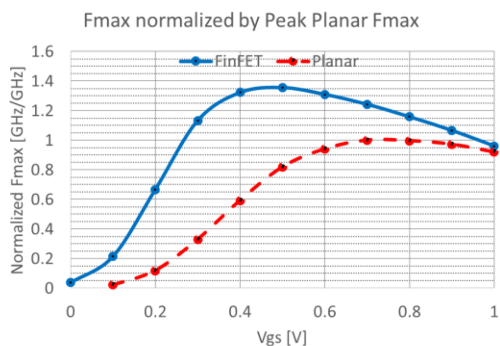


Figure 6: Peak f_t and f_{max}: Planar reaches 20% higher ft than FinFET, but FinFET reaches 40% higher fmax than Planar

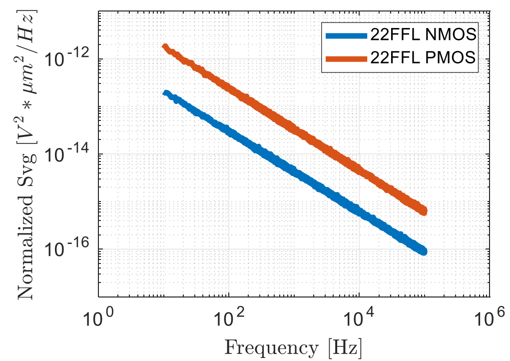


Figure 7: 1/f noise of 22FFL [2]

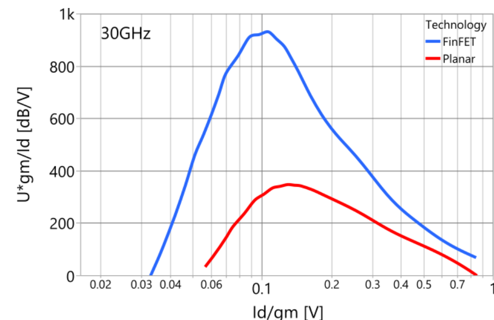


Figure 8: Gain-power efficiency FoM of 22FFL FinFET and Planar device at 30GHz

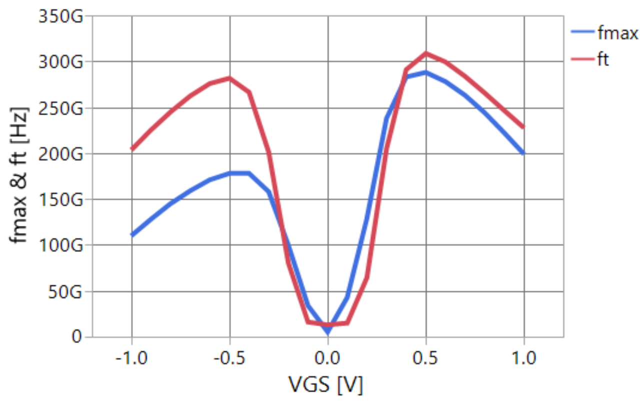


Figure 9:Optimized for peak ft of 22FFL RF transistors

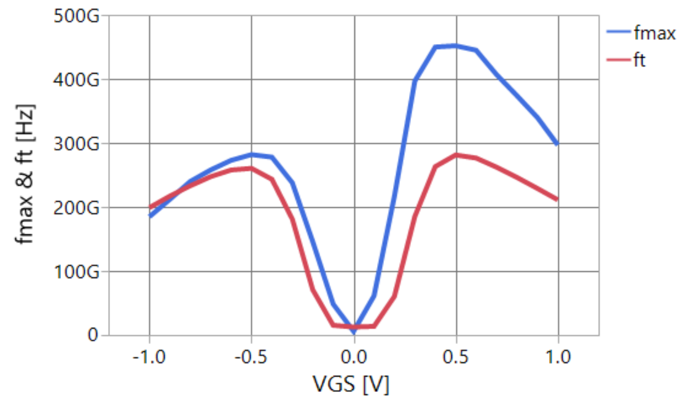


Figure 10: Optimized for peak fmax of 22FFL RF transistors

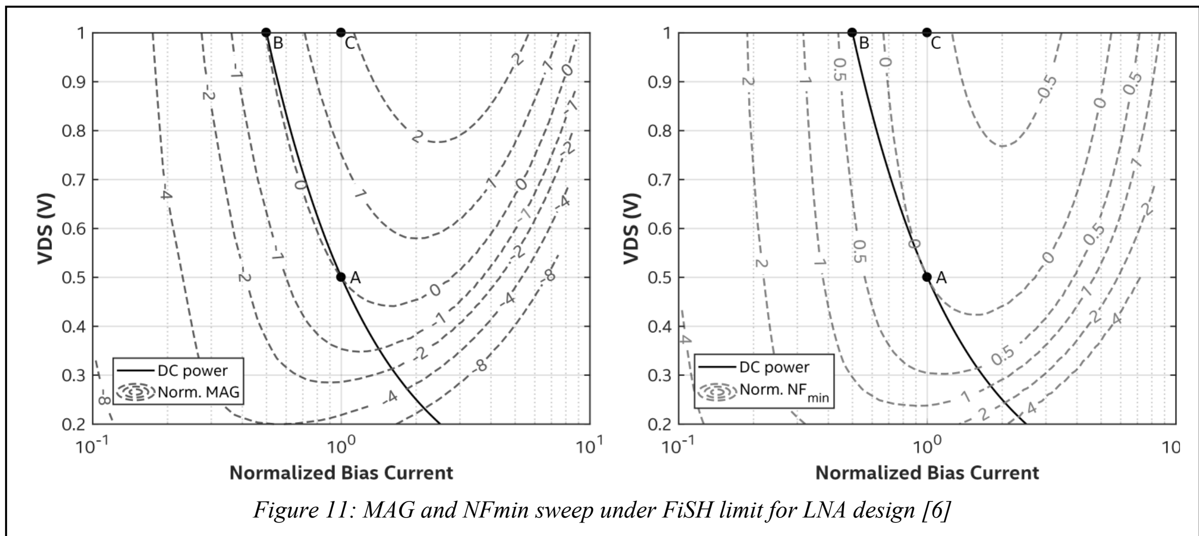


Figure 11: MAG and NFmin sweep under FiSH limit for LNA design [6]

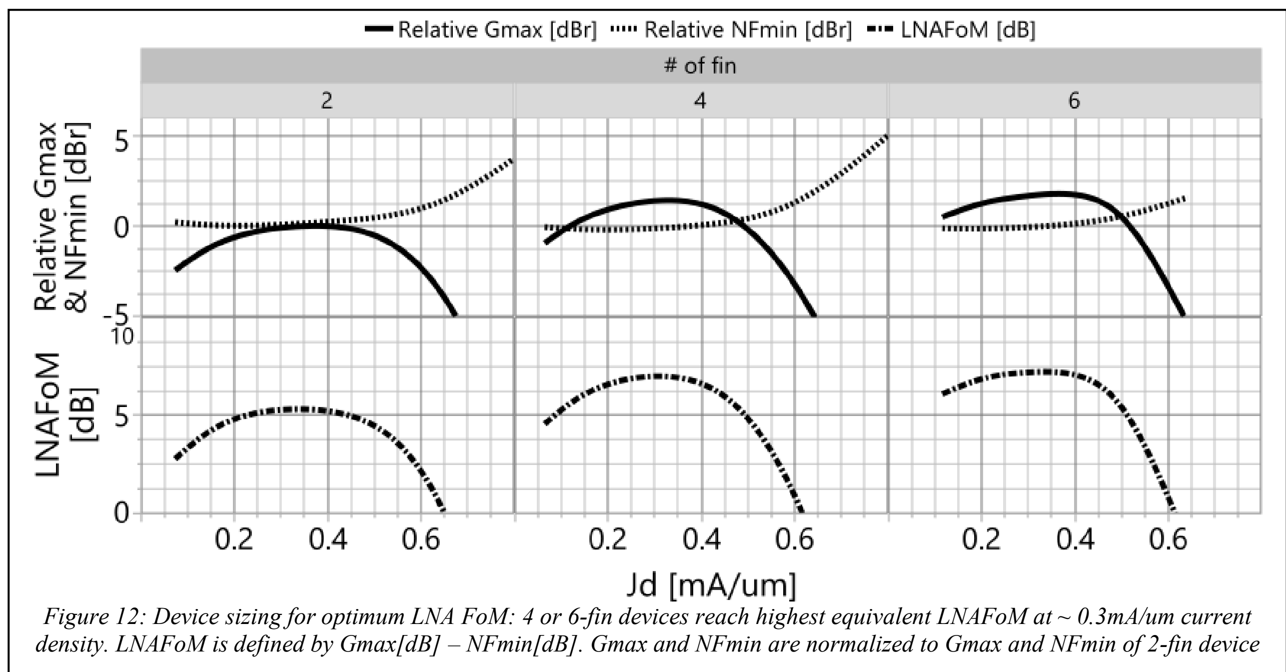


Figure 12: Device sizing for optimum LNA FoM: 4 or 6-fin devices reach highest equivalent LNAFoM at ~ 0.3mA/um current density. LNAFoM is defined by Gmax[dB] – NFmin[dB]. Gmax and NFmin are normalized to Gmax and NFmin of 2-fin device