5.8 A Fully Integrated Transformer-Based Front-End Architecture for Wireless Transceivers

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As wireless transceivers for standards such as Bluetooth and 802.11 become more prevalent, the need for lower-cost solutions becomes increasingly important. In this paper, a fully integrated RF front-end architecture is presented; it offers good RF performance, while requiring no off-chip components. This design uses one on-chip transformer to perform the functions of matching, single-ended to differential conversion, and transmit/receive (T/R) switching. While this architecture can be used in many time division duplex systems, the focus of this paper is on CMOS implementations for the Bluetooth standard.

The initial architecture of this front-end is based on an earlier design [1], and uses several off-chip components as shown in Fig. 5.8.1. There are various ways to reduce the number of off-chip components. First, the T/R switch can be brought on chip, although the best reported CMOS switches introduce around 1dB of loss [2]. Also, on-chip transformers can replace the off-chip baluns and matching elements [3]. Another approach shorts the LNA input and PA output with a common matching circuit, although some compromise between the LNA and PA impedance match may have to be made [4].

Figure 5.8.2 shows the architecture presented in this paper. It uses a multi-tap integrated transformer with one set of ports on the primary side, and two sets of differential ports on the secondary side. One end of the primary connects to the antenna, acting as an RF input/output (I/O) port, while the other end connects to AC ground. On the secondary side, one set of ports connects to the input of the LNA, while a second set of ports connects to the output of the PA. The center tap of the secondary is connected to V_{DD}, providing both AC ground and a DC current path to the PA. The TX and RX front-ends are coupled to the RF I/O port through their connections to the transformer. T/R switch functionality is achieved by powering down one path when the other is in use. The transformer also performs differential to single-ended conversion for both paths, eliminating the need for separate on- or off-chip baluns.

For proper operation of the transformer, each port must be tuned appropriately. The simultaneous loading of the PA, LNA, antenna, as well as die and package parasitics must be factored into the overall transformer design and tuning. Furthermore, the matching at each port must be maintained in both RX and TX modes. At the RF I/O port, series and shunt capacitors are used to bring the impedance to 50Ω. For best performance, both the primary ground and the secondary center tap must provide a good AC ground.

The LNA schematic is shown in Fig. 5.8.3, with the core design carried over from previous work [1]. A transformer turns ratio of 7 to 2 is selected in order to provide an appropriately large voltage gain at the LNA input. The transformer windings also act as gate inductors, replacing the off-chip inductors in the old architecture [1]. A high-Q transformer design is used to minimize the series resistance of the windings, and thus the noise figure degradation. However, even after optimization of the transformer, a 2.5dB insertion loss is incurred, which by itself would reduce sensitivity. This loss is offset by the elimination of the associated losses of the off-chip components which are not needed in the transformer based front-end. More specifically, in the initial design from Fig. 5.8.1, the off-chip balun, T/R switch, and associated board traces, have combined losses of between 2 to 3dB. Because these off-chip losses are eliminated in the fully integrated design, the sensitivity lost due to the transformer is restored. Additionally, the input impedance of the LNA remains high in both on and off states, with the total capacitance at the node dominated by other sources. This allows the loading at the RX port to be maintained in both states.

The PA schematic is shown in Fig. 5.8.4. The transformer is directly connected to the PA output devices, with the windings replacing the load inductors of the original design [1]. A cascode architecture is used so that the output resistance of the devices is always large, and the variation in output capacitance between on and off states is minimal. The transformer, at resonance, can be modeled in much the same way as an inductor, with its windings represented by an inductance and its loss by an equivalent parallel resistance. With the loss pulled out of the circuit, the transformer and its associated matching elements now appear as a lossless, two-port matching network. The loss of the transformer acts as a load at one port of the network, with the antenna load at the other. Overall, TX system efficiency is improved because the transformer replaces the on chip matching elements of the initial architecture, and the additional losses of the off-chip balun and T/R switch are eliminated.

The two sets of ports on the secondary winding are implemented by tapping the transformer at different points along its length. Since each block is connected to the transformer at different points, different turns ratios and impedances can be optimally selected for each path. The receiver and transmitter can essentially be designed as if they are independent, avoiding tradeoffs. Limitations of this architecture lie in the design of an efficient transformer which can provide the desired impedances at each port. Some challenges in the design of the transformer include accommodating the distinct turns ratios required by the LNA and PA, as well as the capacitive loading associated with the active devices.

Both front-end architectures are fabricated in 0.18μm CMOS Bluetooth transceivers, which are identical except for their front-ends. Figure 5.8.6 shows a comparison of measured results. The data confirms that the performance of the new architecture meets that of the non-integrated design. A smaller die area is achieved with the new architecture, as the transformer occupies less area than the sum of the area of the PA output inductors and die pads of the differential paths from the original design. This front-end design has been used in several Bluetooth products which have passed qualification and are in volume production.

References:

[1] Hooman Darabi et al., "A 2.4GHz CMOS Transciever for Bluetooth," *IEEE J. of Solid-State Circuits*, vol. 36, no, 12, pp. 2016-2024, Dec., 2001.

[2] Feng-Jung Huang and Kenneth O, "A 0.5μm CMOS T/R Switch for 900-MHz Wireless Applications," *IEEE J. of Solid-State Circuits,* vol. 36, , no. 3, pp. 486-492, March, 2001.

[3] Jianjun Zhou and David J. Allstot, "Monolithic Transformers and Their Application in a Differential CMOS RF Low-Noise Amplifier," *IEEE J. of Solid-State Circuits,* vol. 33, , no. 12, pp. 2020-2027, Dec., 1998.

[4] Vincent Knopik and Didier Belot, "0.18μm Thin Oxide CMOS Transceiver Front-End with Integrated Tx/Rx Commutator for Low Cost Bluetooth Solutions," *ESSCIRC*, pp. 675-678, Sept., 2003.

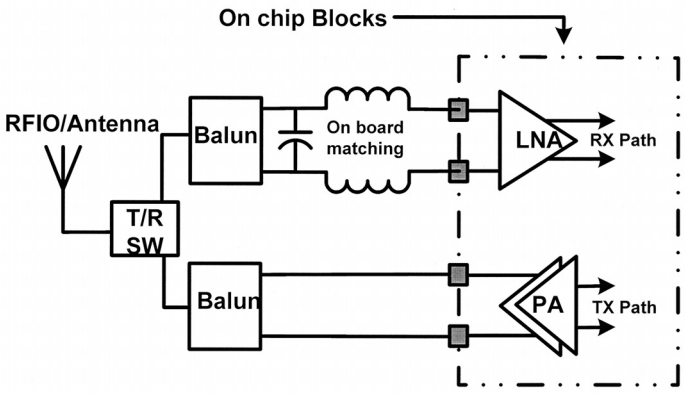

Figure 5.8.1: Original front end architecture.

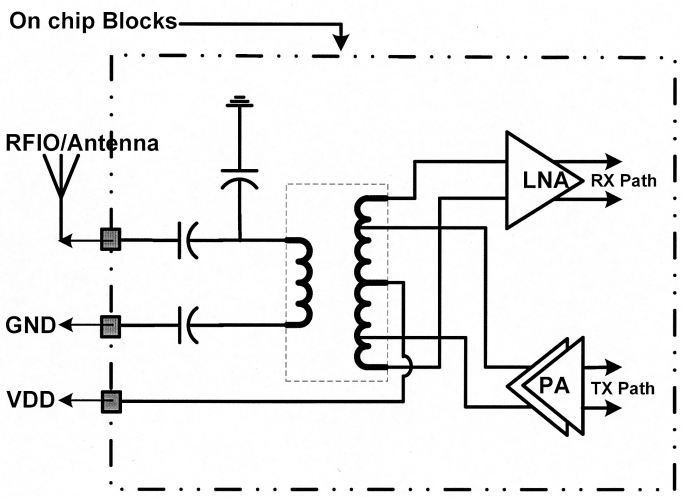

Figure 5.8.2: New front end architecture.

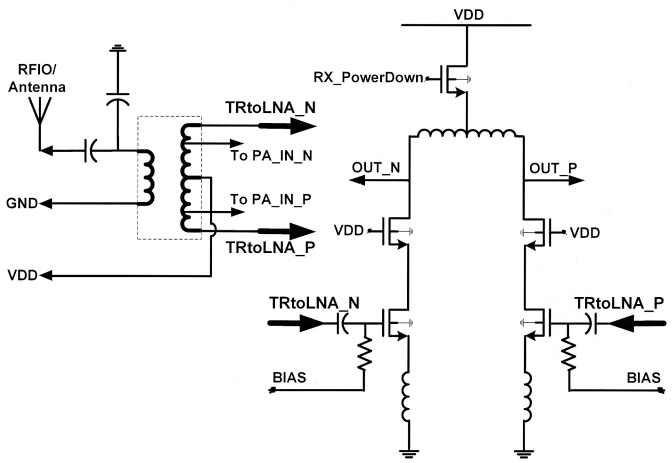

Figure 5.8.3: Transformer and LNA circuit diagram.

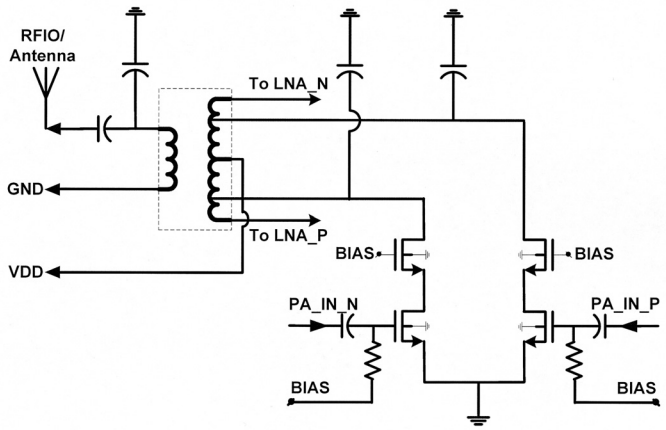

Figure 5.8.4: Transformer and PA circuit diagram.

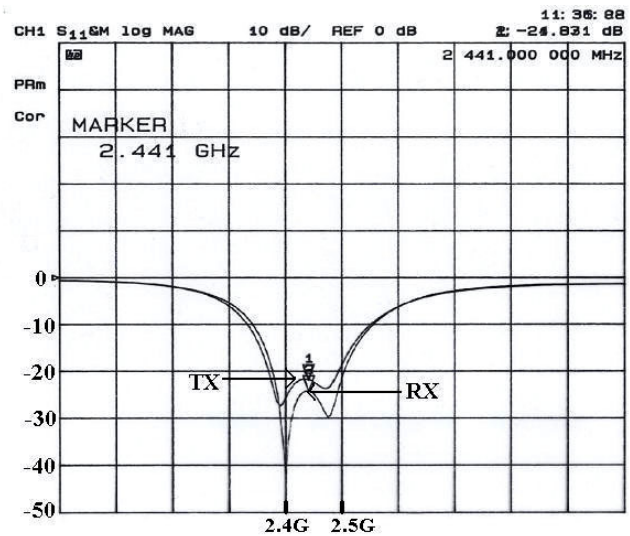

Figure 5.8.5: S11 measurement plots.

Parameter	Integrated Architecture	Original Architecture
Sensitivity	-90.0dBm	-90.3dBm
IIP3	-10dBm	-10dBm
RX Current	33mA	33mA
TX Output Power	+2.1dBm	+2.6dBm *
TX Current	35mA	43mA *
Front End Die Area	1.09mm^2	1.27mm^2
Supply Voltage	1.8V	1.8V
Technology	0.18µm 1P6M CMOS	0.18µm 1P6M CMOS

* Designed for +9dBm Max Output Power

Figure 5.8.6: Measured performance comparison.

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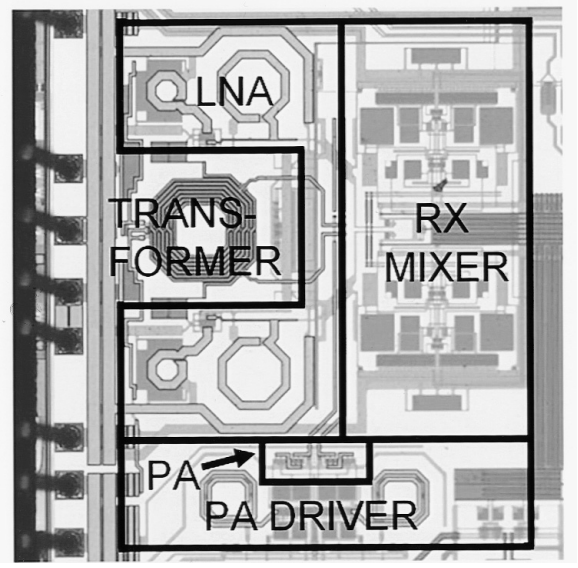

Figure 5.8.7: Die micrograph.

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