WA 18.4 A 3V Low-Power 0.25µm CMOS 100Mb/s Receiver for Fast Ethernet

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A transceiver with excellent performance is recently reported [2]. However, a higher level of integration for multi-channel transceivers for switch application and also for battery-operated laptop markets demands a device with a much lower power consumption with no performance degradation. This AGC and equalizer architecture and circuits address this demand for a low-power transceiver.

A block diagram of the receiver for the 3V CMOS 100Mb/s Fast Ethernet transceiver is shown in Figure 18.4.1 [2]. The equalizer compensates for cable attenuation over frequency to reduce intersymbol interference (ISI). AGC compensates for flat loss across the channel. The HPF and LPF simple single-pole *RC* filters placed in the feedforward and feedback loop of the architecture respectively, correct for baseline wander caused by transformer coupling (Figure 18.4.1). A HPF places a known corner frequency at least one order of magnitude larger than that of the transformer on the signal path, causing a known intentional baseline wander that can be corrected with a LPF with the same corner frequency in the feedback loop.

For a low-power receiver with single 3V power supply, g_m-based and opamp- based analog AGC techniques are compared. An R- MOSR-R T-network opamp approach for AGC uses less power and fewer active components. For the AGC and HPF a differential high-speed opamp A1 is used in the data path, and a low-frequency opamp A2 is used for the LPF and baseline wander correction (Figure 18.4.2). As shown in Figure 18.4.2, the AGC circuit uses a T-network in the feedback of the opamp A1 [3]. Representing the MOS transistor M_r shown in Figure 18.4.2, biased in triode mode and acting as a variable resistor, by R_3, the gain of the AGC circuit is:

$$G = \frac{V_o}{V_i} = \frac{R_a + R_b + \frac{R_a + R_b}{R_3}}{R_1} \tag{1}$$

The advantage of this AGC architecture in which a T-resistor network is used in the feedback of the opamp compared to the one in which a simple switchable resistor is placed in the feedback of the opamp is that it allows the use of a smaller resistor in the feedback loop. This can be readily observed from where a 1/*x* relationship between the value of the resistor R_3 and the gain of the AGC circuit exists. The smaller resistor in the feedback of the opamp is desired for high frequency to avoid unwanted peaking in the response. This is because a lower resistance in the feedback results in a lower parasitic capacitance to substrate. Parasitic capacitance adversely affects circuit performance. A simple model to introduce the distributed parasitic capacitance of each resistor in a simple opamp-R AGC circuit is shown in Figure 18.4.3. Lumped capacitors C_{p1} and C_{p2} added to the middle of resistors R_1 and R_2 model effects of resistor distributed capacitor to the substrate, respectively. Incorporating the parasitic capacitors results in the transfer function:

$$\frac{V_o}{V_i} = -\frac{2R_2 + R_2^2 C_{p2} s}{2R_1 + R_1^2 C_{p1} s} \tag{2}$$

From (2) it is apparent that an unwanted zero $z_1 = -\frac{1}{(R_2/2)C_{p2}}$ and an unwanted pole $p_1 = -\frac{1}{(R_1/2)C_{p1}}$ are introduced in the system by the parasitic capacitors. As the gain increases, i.e., as R_2 is increased, C_{p2} increases compared to C_{p1}, making the zero smaller compared to the pole resulting in unwanted peaking in the frequency domain. The AGC circuit, shown in Figure 18.4.2, requires a much smaller feedback resistance especially at high AGC settings where bandwidth is more demanding. A MOS tuning circuit shown in Figure 18.4.2 improves the AGC accuracy and reduces the parasitic capacitances further. By replacing a resistive network for R_3 with a slave MOS transistor which has an equivalent effective resistance and placing a master resistive network for controlling the MOS transistor effective resistance in a remote location, the amount of parasitic capacitance in the opamp feedback network (AGC), is substantially reduced (Figure 18.4.4). Figure 18.4.4 shows the MOS tuning circuit of Figure 18.4.2. The desired R_3 resistive network is placed between node V_1 and node V_A in Figure 18.4.4. Drain-to-source resistance of the master transistor, M_m in Figure 18.4.4, and so that of the slave transistor M_r in Figure 18.4.2 is forced equal to that of the net resistance of the R_3 resistive network in Figure 18.4.4. From Figure 18.4.2 for small V_{ref} values the effective resistance across the drain-to-source of the master MOS transistor, M_m, can be calculated as $r_{ds,m} \approx \frac{V_{DS,m}}{I_2} = \frac{R_3}{N}$ where N is the gain of the current mirror in Figure 18.4.4. The voltage developed at the output of the amplifier B_2 controls the gate of the master transistor, M_m, which controls the gate of the remote slave transistor M_r shown in Figure 18.4.2.

Transmission of a digital PAM signal through a bandlimited channel having amplitude loss variation with frequency and linear phase results in intersymbol interference. One would like to make the transfer function of the equalizer to be the inverse of the channel transfer function to re-create the same waveform at the output of the transmitter filter. From the time-domain viewpoint, an adaptation algorithm tries to minimize the ISI by adjusting the equalizer coefficients. This can be completely adaptive based on an LMS algorithm or a programmable method can be employed. In a programmable adaptation for given channel characteristics, the best transfer function among many pre-designed settings for the equalizer is chosen. This programmable approach is chosen for equalizer adaptation. This reduces the complexity of the adaptation for an analog equalizer without compromising performance [2]. A two stage opamp-*RC* network is implemented for the equalizer block. The transfer function of the equalizer compensates for cable loss and phase dispersion [2]. A model of each equalizer stage is shown in Figure 18.4.5. The transfer function of a single equalizer stage implementing a pole and a zero shown in Figure 18.4.5 is:

$$T_1(s) = \frac{1 + R_1 C s}{1 + R_2 C s} \tag{3}$$

Each resistor in the equalizer stage is actually a switched resistive network. The 2-pole and 2-zero tuning resistors are adjusted by decoders which synthesize the required trajectories for these residues for different cable lengths. Poles and zeros in both stages are tuned independently by switching the proper resistor setting. Capacitors are tuned by a process-tune circuit which locks its *RC* time constant to a stable clock frequency so time constants of all poles and zeros in the equalizer are referenced to a fixed frequency. The process-tune circuit is a closed loop system composed of two replicas of the reference pole network used in the equalizer, a differential clocked-comparator and a 9b up-down counter. Clock and clock waveforms are supplied to the *RC* networks that have switchable capacitors. The differential outputs of the *RC* networks are fed to the inputs of the differential clocked-comparator. The closed-loop system forces the output signals of the *RC* networks bounded within $\pm V_{ref}$. The 9b up-down counter acts as an integrator in the loop. Five MSBs of the up-down counter control the master capacitor network in the process-tune circuit and those in the equalizer. The tuned time constant is $RC = \frac{T}{2} / 1n\left(\frac{1+\alpha}{1-\alpha}\right)$ where $\alpha = V_{ref}/V_{id}$ and $V_{id} = V_{dd}$.

Figure 18.4.6 is a micrograph of the receiver for the Fast Ethernet transceiver in 3V, 0.25µm CMOS. The analog receiver active area is 0.984mm². Figure 18.4.7 is the eye at the equalizer output for a random packet for a randomly-selected device after a 100m CAT5 cable. The jitter and signal-to-noise ratio allow data and clock recovery.

References:

[1] "Fibre Distributed Data Interface (FDDI) - Token Ring Twisted Pair Physical Layer Medium Dependent (TP-PMD)," *ANSI X3.263-1995*, Sept. 1995.

[2] Shoval, A. et al., "A CMOS Mixed-Signal 100Mb/s Receive Architecture for Fast Ethernet," *Proceedings of IEEE Custom Integrated Circuits Conference,* pp. 253-256, May 1999, San Diego, CA, U.S.A.

[3] Banu, M., private communication.

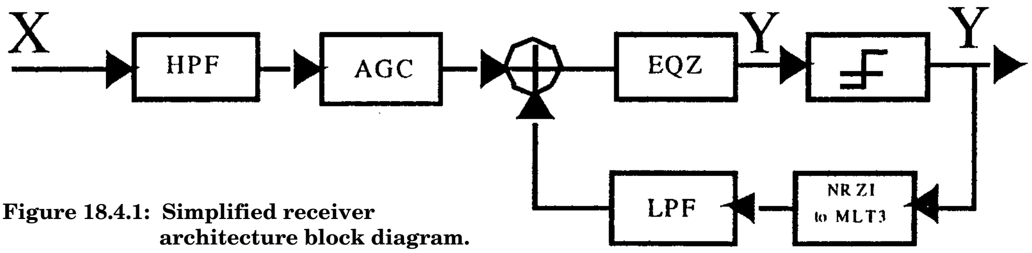

Figure 18.4.1: Simplified receiver architecture block diagram.

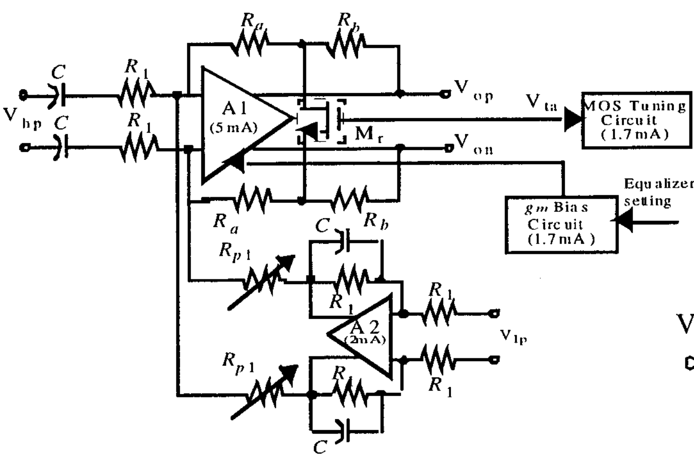

Figure 18.4.2: A simplified block diagram of the AGC, HPF and LPF loop.

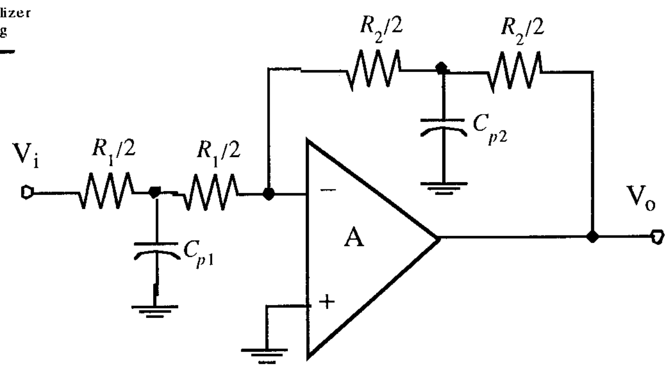

Figure 18.4.3: A lumped model for distributed parasitic capacitors in simple AGC circuit.

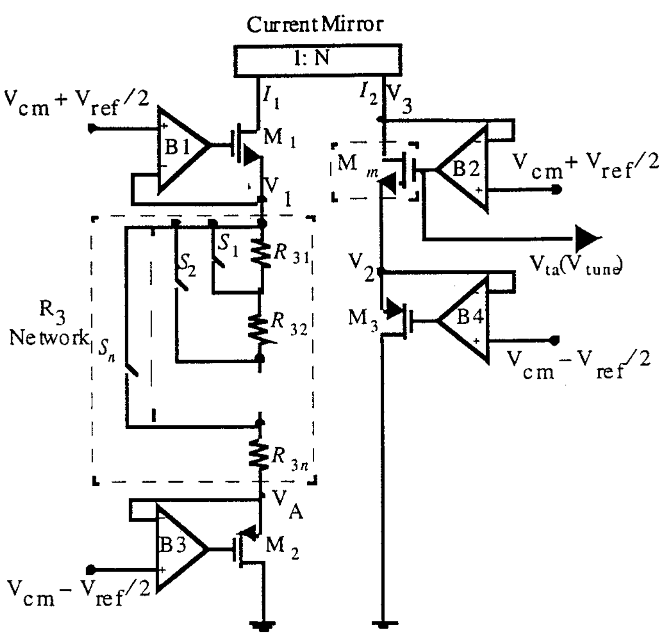

Figure 18.4.4: The master MOS tuning circuit.

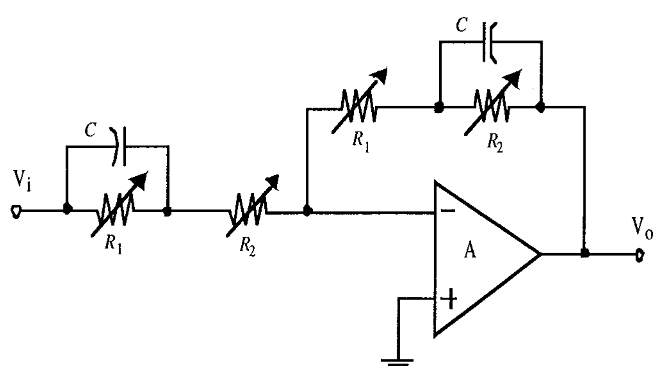

Figure 18.4.5: A single-ended version for each single equalizer stage.

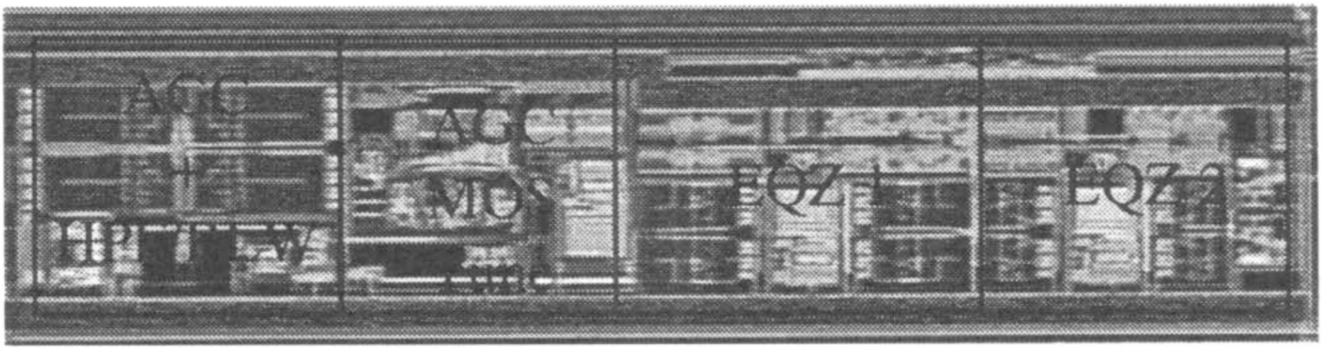

Figure 18.4.6: Fast Ethernet receiver chip micrograph.

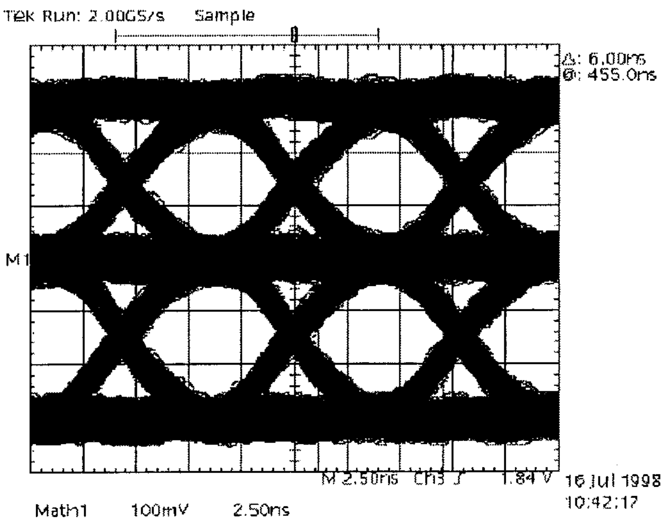

Figure 18.4.7: The eye diagram of the equalizer output for a 100m CAT5 cable.

