16.5 A Fractional-N Synthesizer with 110fs$_{rms}$ Jitter and a Reference Quadrupler for Wideband 802.11ax

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The next-generation 802.11ax WLAN standard improves the throughput by supporting 1024-QAM in a channel bandwidth of 160MHz, demanding extremely low jitter values for the transmitter (Tx) and the receiver (Rx) synthesizers. Recent work has achieved rms jitter below 200fs [1-4] with the latest rms jitter reported at 75fs [5]. The work in [5] faces a number of challenges if applied to 802.11ax: (1) with a VCO frequency of 5.7 to 7.3GHz, the circuit is prone to pulling by the PA, especially because it incorporates a single spiral inductor (rather than an 8-shaped inductor); (2) it does not provide quadrature outputs, and (3) it relies on a 10b digital-to-time converter (DTC) without calibration of its nonlinearity, which folds high-frequency ΔΣ-modulator (ΔΣM) noise unless extremely tight matching is guaranteed. Similarly, the design in [2] is prone to pulling as well.

This paper presents a fractional-N synthesizer that not only achieves a low jitter but also robustly lends itself for use in transceivers and for SoC integration. This level of performance is afforded through the use of three techniques: (1) a background-calibrated reference quadrupler, (2) a power-efficient frequency tripler, and (3) a twin-T notch filter, which is adjusted by the Rx-filter RC-calibration circuitry. Shown in Fig. 16.5.1, the proposed synthesizer is architected to address two critical issues, namely pulling by the PA and the peaking of the third-order ΔΣM noise. The former is resolved by the VCO frequency of 6 to 8GHz and a div-by-2/tripler cascade, and the latter is resolved by a reference quadrupler. In addition to standard techniques, such as a charge pump with an offset current to avoid noise folding and an 8-shaped inductor to suppress coupled noise in an SoC, the loop also incorporates a 40MHz notch filter to reduce both the out-of-band ΔΣM noise and the 40MHz spur. This filter negligibly affects the phase margin because the loop bandwidth must be small enough to limit the amplified phase noise of the crystal oscillator. The VCO includes an amplitude-control loop for optimum phase-noise performance with PVT.

The reference quadrupler plays a critical role in the performance as it lowers the ΔΣM quantization noise contribution to the synthesizer output by 15dB (from 94fs to 16.9fs) compared to a doubler. However, the quadrupler must deal with several issues: the duty cycle error of the 40MHz reference (ε_{40}), the duty cycle error of the doubled frequency (ε_{80}), and the phase noise generated by its constituent stages. This work proposes a three-point calibration method to eliminate the first two and deals with the phase noise through the use of fast edges.

As conceptually illustrated in Fig. 16.5.2, we employ a low-spur frequency-quadrupling calibration PLL (CalPLL) to create transitions that are free from deterministic modulation and compare the quadrupler output edges with these transitions. Even though designed for low power consumption, CalPLL does not contribute phase noise as the calibration routine averages its results over 8192 reference cycles. Note that the doublers must contain delay stages to generate new edges, adding their own phase noise. Taking into account both duty cycle errors, ε_{40} and ε_{80}, and the static phase offset of CalPLL, $\Delta\phi$, we can identify three types of rising edges in y(t): (1) E_{y1} incurs a constant phase error of $\Delta\phi$ with respect to the corresponding edge in x(t), E_{x1}; (2) E_{y2} inherits the duty cycle error of Doubler 1 plus $\Delta\phi$; and (3) E_{y3} inherits ε_{40} plus $\Delta\phi$. As explained below, these edges are utilized for calibration. Note that E_{y1} and E_{y3} are as clean as f_{REF} in terms of phase noise, whereas E_{y2} and E_{y4} inherit the phase noise of the delay stage in Doubler 1.

Figure 16.5.2 also illustrates that the standard delay-plus-XOR doubler topology suffers from two different effects in its output: a pulse-width error due to unequal input rise and fall times; and a pulse-position error arising from ε_{40}. Since it is difficult to calibrate both of these effects, this work introduces a doubler that operates with only rising edges and is free from the pulse-width error.

Figure 16.5.3 shows the detailed realization of the quadrupler. The 40MHz reference drives a duty-cycle-correction (DCC) circuit that generates complementary outputs A and $\overline{A}$. These signals are applied to the cascade of Doubler 1 and Doubler 2. Doubler 1 operates based on the principle that the frequency can be doubled if A and $\overline{A}$ are multiplexed by a selection command, SEL, that is 90° out of phase. This principle is realized by a self-sustained loop consisting of a delay stage, ΔT_1=6.25ns, a div-by-2 circuit, and the MUX. Doubler 1 thus processes only the rising edges of A and $\overline{A}$ as it generates g(t).

The calibration of $\Delta\phi$, ε_{40}, and ε_{80} is greatly simplified by observing that the edges E_{y2} and E_{y3} in Fig. 16.5.2 provide unique and complete information about ε_{80} and ε_{40}, respectively, if $\Delta\phi$ (the error between E_{y1} and E_{x1}) is zeroed. As shown in Fig. 16.5.3, the quadrupled output, y(t), and the CalPLL output are applied to a bang-bang phase detector (BBPD), which measures and keeps track of their phase errors on consecutive edges. The error E_{y1}-E_{x1} is averaged and applied to null $\Delta\phi$, E_{y2}-E_{x2} adjusts ΔT_1, and E_{y3}-E_{x3} adjusts the DCC circuit. After the loops settle, h(t) has a precise 50% duty cycle and very small spurs. The value of ΔT_2 is not critical, and Doubler 2 is based on the conventional topology as the PFD responds to only rising edges. It is important to note that the BBPD phase offset appears in all three measurements and is therefore absorbed by $\Delta\phi$, the DCC circuit, and ΔT_1. This background-calibration method ensures low spurs under all PVT conditions.

To avoid LO pulling, prior work has used cascaded mixing [6]. However, as shown in Fig. 16.5.4, if the waveforms are mixed in a circuit with hard switching, then the output frequency is not tripled, exhibiting a strong fundamental. The tripler proposed here utilizes rail-to-rail swings for high efficiency and employs phase interpolation and edge combing to directly generate the desired frequency while suppressing the first harmonic. Illustrated in Fig. 16.5.4, our method first generates I and Q phases by a divider, from which three phases 120° apart are created. The resulting edges are then combined to triple the frequency. For convenient device ratios, the phase interpolator (PI) approximates theses phases by three phasors equal to +6I+6Q, -8I+2Q and +2I-8Q (and their complements), incurring a maximum error of 3°. Figure 16.5.4 also shows the edge combiner circuit, which drives a negative resistance and a programmable tank to further suppress the mismatch-induced spurs.

The overall synthesizer has been fabricated in 28nm CMOS and occupies an active area of 0.47mm^2. The circuit draws 22.8mW. For ease of testing, the phase noise is measured after an additional div-by-2 stage. All of the spur values reported here are normalized to the LO frequency (f_{LO}). Figure 16.5.5 shows the measured phase noise at 2912.5MHz (f_{LO}=5825MHz) with the reference frequency doubled or quadrupled. The synthesizer achieves an integrated jitter of 110fs$_{rms}$ from 10kHz to 10MHz including all of the spurs in the quadrupler mode, which translates to an integrated phase error (IPE) of 0.23° (-48dBc) and exceeds the 802.11ax specification. By virtue of the 40MHz notch in Fig. 16.5.1, the jitter rises by only 2.6fs if integrated from 10kHz to 100MHz, showing promise for wideband 802.11ax. The measured reference spurs are -76.4dB at 40MHz, -73.4dB at 80MHz, and below -85dBc at 160MHz. The spur level at 40MHz falls by 3-to-5dB after the notch-filter calibration. All fractional spurs are below -60dBc. Table in Fig. 16.5.6 compares the performance of our prototype to that of the prior art.

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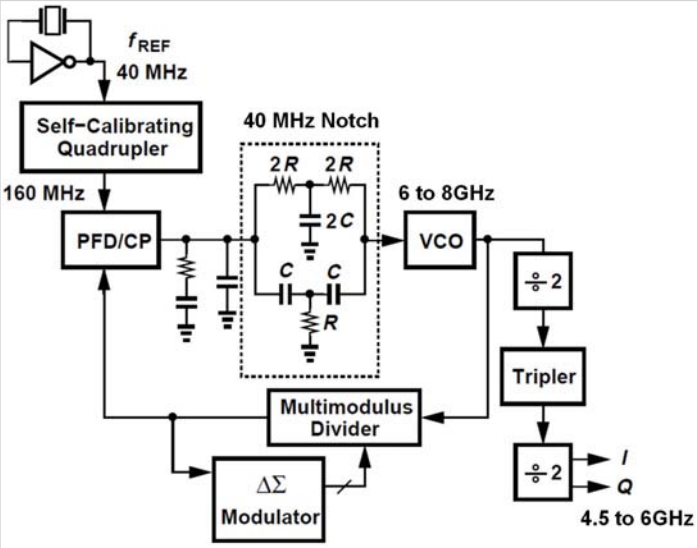

Figure 16.5.1: Proposed synthesizer architecture.

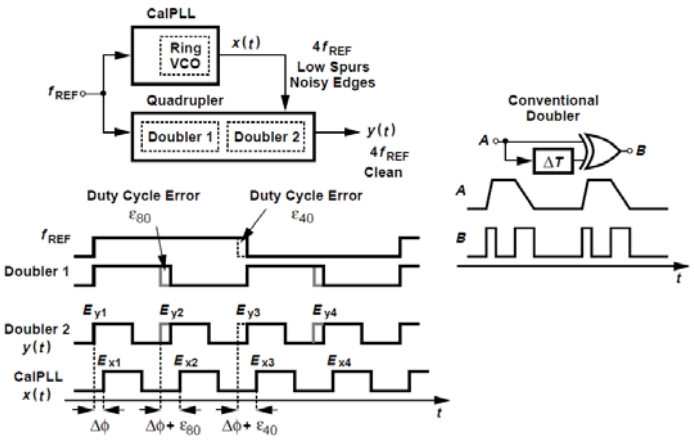

Figure 16.5.2: Quadrupler calibration concept and issues in conventional doubler.

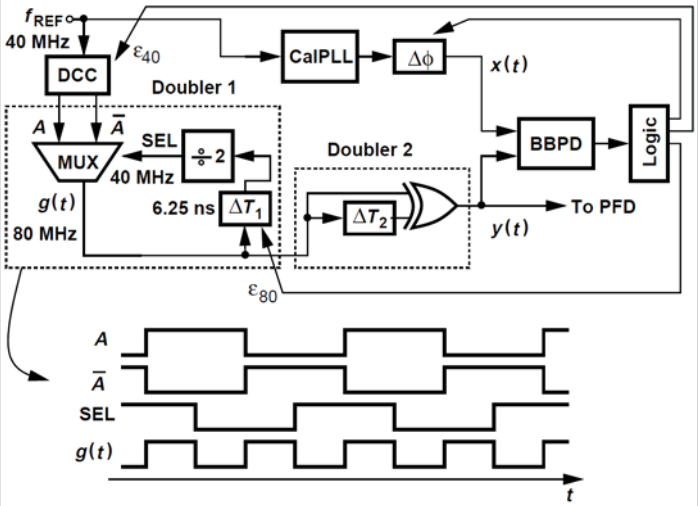

Figure 16.5.3: Detailed realization of the quadrupler.

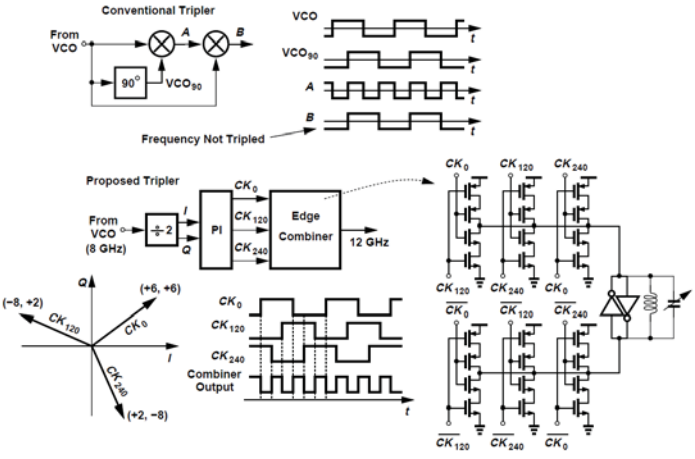

Figure 16.5.4: Conventional and proposed frequency triplers.

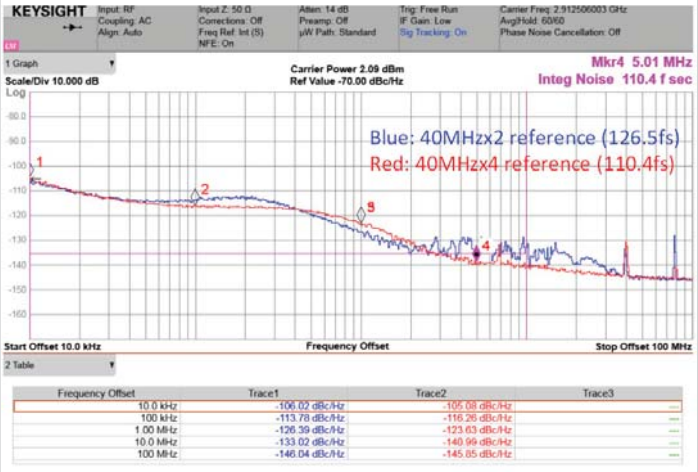

Figure 16.5.5: Measured output phase noise (after a divide-by-2 stage) at 2912.5MHz. The LO frequency is 2×2912.5MHz. Two profiles for reference quadrupling or doubling are shown.

	This Work @40MHzx4	This Work @80MHzx2	Chen. ISSCC'2017	Yao. ISSCC'2017	Gao. ISSCC'2016	Hsueh. ISSCC'2014	Wu. RFIC'2018
Process	28nm	28nm	40nm	14nm	28nm	40nm	28nm
Architecture	Analog	Analog	Analog	Digital	Digital	Analog	Analog
Reference (MHz)	40	80	40	26	40	26	52
RMS jitter (fs)	110	82	116	137	159	191	75
In-band PN Normalized to 5.825GHz (dBc/Hz)	-110.3 @100KHz	-112.7 @100KHz	-107.8 @100KHz	-106.9 @100KHz	-105.5 @100KHz	-102.0 @100KHz	-113.3 @100KHz
Reference Spur (dBc)	-73.4	-66.4	-	-87.6	-78.0	-100.0	-70.1
Power (mW)	22.8	14.7	20.0	13.4	8.2	17.5	18.9
FoM (dB)	-245.6	-250.0	-245.0	-246.0	-246.8	-242.0	-249.7
Area (mm²)	0.47	0.47	0.43**	0.26	0.30	0.29	0.50

** Estimated from die micrograph

$$FoM = 20\log_{10}\frac{\sigma}{1s} + 10\log_{10}\frac{Power}{1mW}$$

Figure 16.5.6: Performance summary and comparison table.

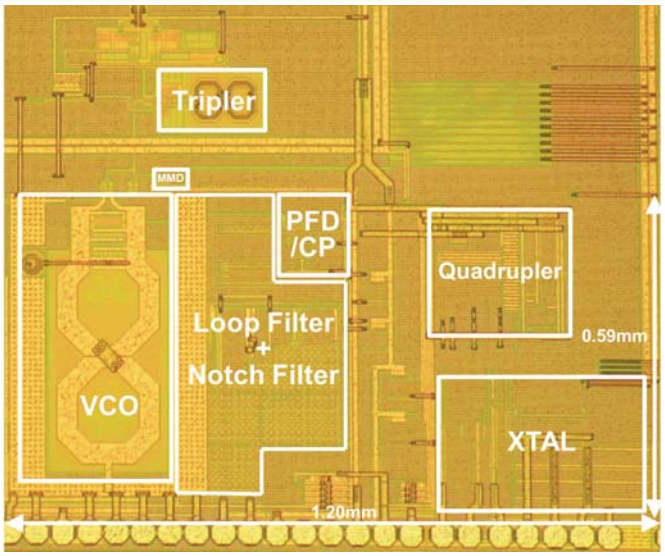

Figure 16.5.7: Die micrograph.

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