# *A 2.5Gb/s ESD-Protected Dual-Channel Optical Transceiver Array*

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***Abstract*— This paper describes the design of a dual-channel optical transceiver array realized in a standard 0.18μm CMOS technology for the applications of high-speed digital interface. The transmitter drives a 2-channel VCSEL array at 2.5Gb/s, equipped with the APC (5-15mA) and AMC (4-20mA$_{pp}$) loops for constant and reliable optical power outputs. Meanwhile, the receiver exploits the common-gate transimpedance amplifier, demonstrating 87dBΩ transimpedance gain, 1.4GHz bandwidth for 2pF input parasitic capacitance, -18dBm sensitivity for $10^{-12}$ BER, and less than –20dB crosstalk between TX and RX within the bandwidth. The whole 2-channel transceiver array chip dissipates 500mW.**

## I. Introduction

Recently, high-performance consumer electronics have been very popular due to the proliferation of living standards in modern societies. Therefore, it leads to the development of high-speed digital interface for multimedia (with audio and image signals) networks. For this purpose, optical fiber communications are well known to provide a number of advantages over copper-based cables, such as wider-bandwidth, longer transmission distance, and lower EMI interference. Hence, optical transceiver chips (e.g. VCSEL driver in TX) can be utilized even for VSR (very short reach) links [1]. In particular, DVI/HDMI applications can employ the optical fibers to greatly enlarge the transmission distance while maintaining the resolution rate between digital electronic devices such as DVD players, PC's, camcorders, etc.

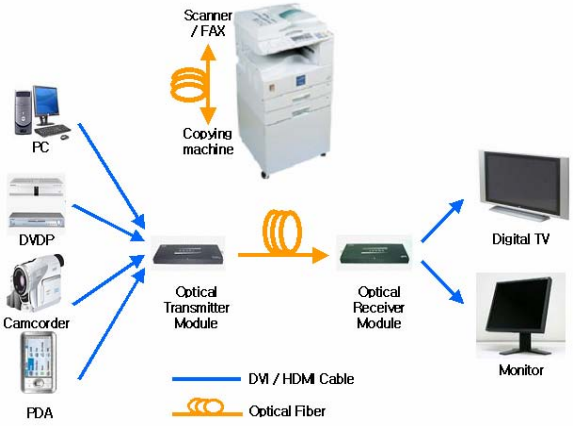


Fig. 1. Illustration of DVI/HDMI systems.

Also, they can be exploited for short-distance low-cost communication systems like LAN (Local-Area-Networks), SAN (Storage-Area-Networks), FTTH (Fiber-To-The-Home), and even optical interconnects between boards or chips.

Fig. 1 illustrates a DVI/HDMI system, where the optical links can be extensively utilized to enhance the performance. In this paper, we present a dual-channel optical transceiver array realized in a 0.18μm CMOS technology, where each channel operates up to 2.5Gb/s.

## II. Transmitter : VCSEL Driver

### *A. Circuit description*

Fig. 2 shows the block diagram of a single-channel transmitter, which consists of an input buffer, a preamplifier, a main VCSEL driver, and a single feedback loop for AMC and APC operations. The input buffer is designed to cover both LVDS (low-voltage-differential-signal) and CML (common-mode-logic) input signals. Therefore, the circuit configuration of the input buffer stage exploits the rail-to-rail fully differential folded cascade amplifier [1].

Since a conventional VCSEL driver presents a crucial design tradeoff between large current driving capability and high-speed operations, output transistors are typically designed to be very large so as to drive large output currents. However, it gives rise to large parasitic capacitance, thus resulting in limited bandwidth. Thereby, in this work, a preamplifier is inserted between the input buffer and the main driving output stage, which facilitates the demanding design tradeoff.

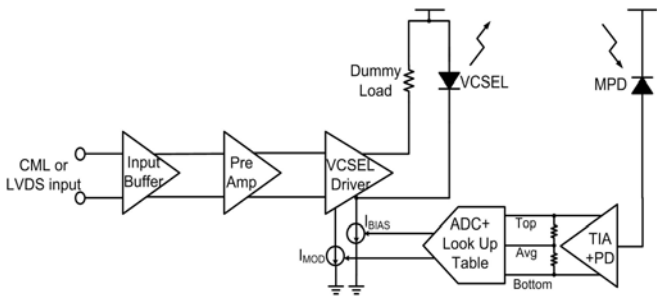


Fig. 2. Block diagram of a single-channel VCSEL driver.

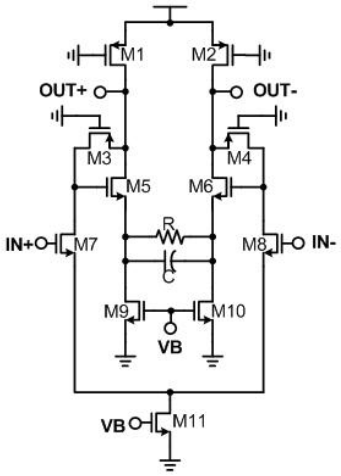


Fig. 3. Schematic diagram of the preamplifier with capacitive degeneration.

Fig. 3 depicts the schematic diagram of the modified preamplifier that shares the basic configuration of the Cherry-Hooper topology in order to achieve wide bandwidth. Also, it incorporates the capacitive degeneration technique so that the dominant pole of the circuit can be transferred to a higher frequency, therefore enlarging the gain-bandwidth with no further gain-penalty.

According to small signal analysis, the equivalent transconductance ($G_m$) of the preamplifier is given by,

$$G_m = \frac{g_m}{1+g_m\left(\frac{R}{2}\left\|\frac{1}{2Cs}\right.\right)} = \frac{g_m(1+sRC)}{sRC+\left(1+g_mR/2\right)}. \quad (1)$$

It is clearly seen that $G_m$ contains a zero at 1/RC and a pole at $(1+g_mR/2)/RC$. If the zero cancels the dominant pole occurred at the drain of $M_5$ and $M_6$, then the total bandwidth would be far more extended.

Since on-chip resistors are prone to vary ± 25% in its value, the performance degradation of the preamplifier should be estimated. Hence, HSPICE corner simulations were conducted by using the model parameters of a 0.18μm CMOS process. The results show that the performance degradations are negligible, i.e. less than ± 1.5% GBW variation, despite the significant changes of on-chip resistance values.

The main VCSEL driver, as shown in Fig. 2, consists of current mirrors and a differential current switch that modulates the input data stream. $I_{MOD}$ represents the VCSEL modulation currents, corresponding to the output swing, whereas $I_{BIAS}$ represents the VCSEL bias current that corresponds to the average transmitted optical power. $I_{BIAS}$ is selected to be slightly higher than the threshold current of the VCSEL. Thereby, fast and reliable switching operations are ensured and also turn-on delay problems are omitted. It is also necessary to optimize the size of the main transistors so that the main driver circuit provides the required modulation currents while maintaining 2.5Gb/s operations. Since the inherent resistance of a low-cost VCSEL is about 20~30Ω, we simply model the dummy load to be a 50Ω resistor.

### *B. APC and AMC loops*

Typically, the transmitted optical power of a VCSEL diode varies according to the injected current characteristics. Unfortunately, however, it decreases with time and temperature changes. Since optical transmitters are required to maintain the average transmitted optical power and the extinction ratio over a wide temperature range, the main driver circuit incorporates a couple of feedback loops to compensate the degradation of optical output data stream against the temperature and aging effects, namely APC (automatic power control) loop and AMC (automatic modulation control) loop.

In this work, we propose a novel design that controls both $I_{MOD}$ and $I_{BIAS}$ simultaneously, by using a wideband TIA with a MPD (monitoring photodiode) and peak detectors. The top and bottom peak values of the voltage signals at the output of TIA are compared with fixed voltages for modulation controls [2]. Then, the difference signals are quantized to be digital codes and the embedded look-up table selects a proper control voltage for the AMC loop in a very fine manner. Meanwhile, the average value of the monitoring TIA output is determined by a voltage divider inside the peak detector and compared with the nominal value at a difference amplifier. Also, it is quantized to be a digital code to control the APC loop.

## III. RECEIVER : CG TIA

Fig. 4 shows the block diagram of a single-channel receiver, which consists of a DC-balanced common-gate transimpedance amplifier (CG TIA), and an output buffer with DC-offset cancellation networks. All building blocks are designed to be differential so as to eliminate common-mode noises like power supply noise, substrate crosstalk, etc. The other input of the TIA is connected to an off-chip capacitor of which value is selected to be the same as the photodiode capacitance, so that the TIA inputs can be pseudo-differential.

Typically, the front-end TIA has a number of design tradeoffs between bandwidth, photodiode capacitance, transimpedance gain and sensitivity. Particularly, the bandwidth limitation occurs at the input node due to the large photodiode capacitance.

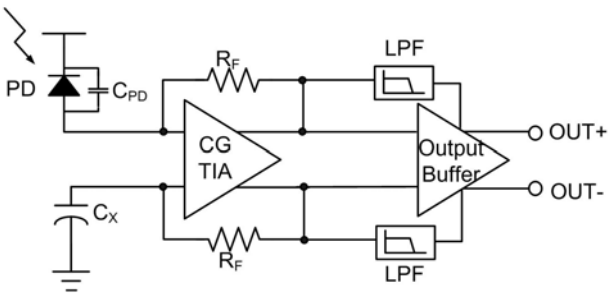


Fig. 4. Block diagram of a single-channel receiver.

Therefore, common-gate (CG) input stage is exploited in this work so as to isolate from the bandwidth determination the large input parasitic capacitance including even the parasitic capacitance of ESD protection diodes (0.5pF). HSPICE simulations were conducted by using the same model parameters of the 0.18μm CMOS process, demonstrating that the bandwidth of the CG TIA is achieved to be 1.3GHz for 2pF input parasitic capacitance. Even with 6pF input capacitance, the bandwidth shrinks to 920MHz, i.e. only 30% reduction, for the same transimpedance gain.

Fig. 5 shows the simplified schematic diagram of the CG TIA input stage. The second voltage-gain stage is two cascaded common-source differential amplifiers. Instead of utilizing on-chip resistors, active PMOS loads are exploited in the circuit and thus the significant variations of on-chip resistance due to layout or PVT variations can be avoided. Also, each gain cell in the cascaded amplifiers is carefully designed to achieve the largest possible bandwidth and the maximum feasible gain with no instability issue, so that the total ac response of TIA can be ensured to provide 2.5Gb/s operation speed.

Fig. 6 illustrates the schematic diagram of the DC-balanced output buffer, in which the DC-offset cancellation circuit is employed with a couple of low-pass filters (LPF) to match the DC-level of the differential TIA outputs. In order to facilitate the design of the following limiting amplifier, it utilizes the CML-type differential amplifier with open-drain. HSPICE simulations show that the output buffer drives 7mA current at each 50Ω termination.

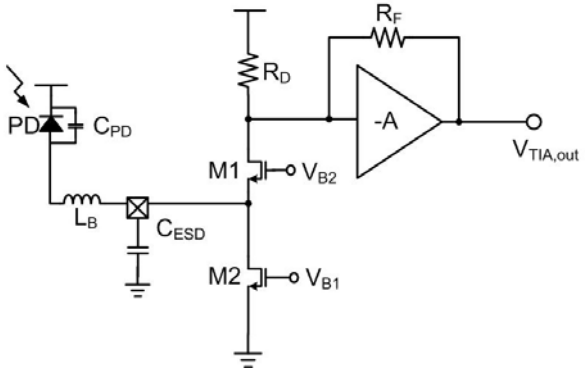


Fig. 5. Simplified schematic diagram of the CG input stage.

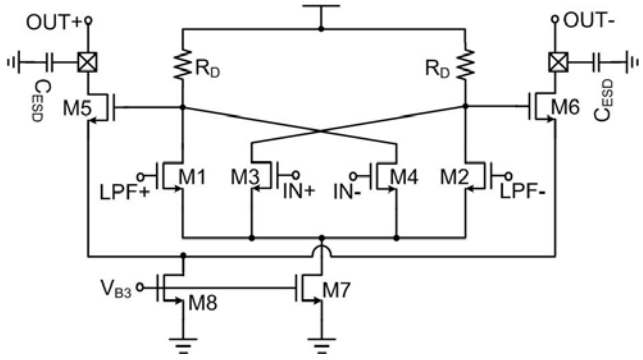


Fig. 6. Schematic diagram of the DC-balanced output buffer.

## IV. Experimental Results

Test chips of the proposed dual-channel transceiver array were implemented in a standard 0.18μm CMOS process. Fig. 7 depicts the chip microphotograph and its evaluation board, where the chip occupies the area of 1.3 x 1.4 $mm^2$.

Fig. 8 shows the measured eye-diagrams of a single-channel VCSEL driver at different data rates of 622Mb/s, 1Gb/s, 1.8Gb/s and 2.5Gb/s, respectively, for $2^{31}$-1 pseudorandom bit sequence (PRBS) input data stream. The single-ended output voltage of $300mV_{pp}$ is achieved for the modulation current of $12mA_{pp}$. The minimum and maximum modulation currents are achieved to be $4mA_{pp}$ and $20mA_{pp}$, respectively. Fig. 9 depicts the AMC operation of the VCSEL driver for 2.5Gb/s PRBS input data stream.

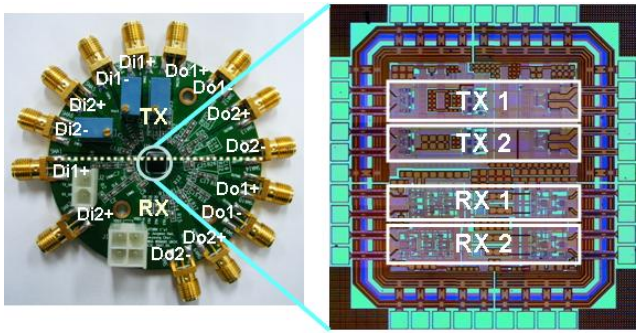


Fig. 7. Chip microphotograph of the dual-channel optical transceiver array and its evaluation board.

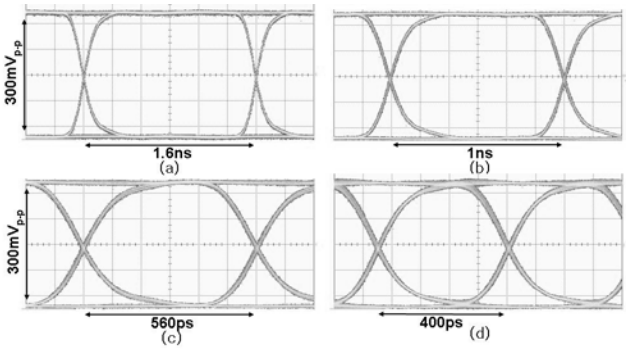


Fig. 8. Measured eye-diagrams of a single-channel VCSEL driver for $2^{31}$-1 PRBS at different data rates of : (a) 622Mb/s, (b) 1Gb/s, (c) 1.8Gb/s, and (d) 2.5Gb/s.

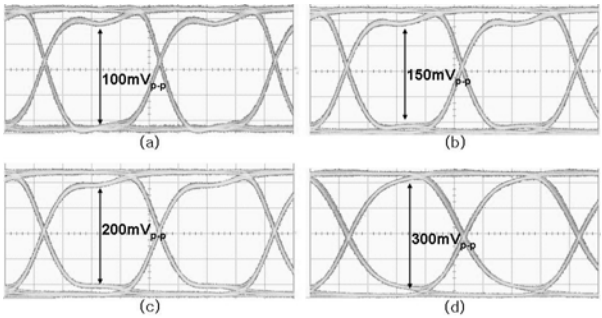


Fig. 9. Measured eye-diagrams of 2.5Gb/s VCSEL driver with AMC control loops turned on with modulation currents of : (a) $4mA_{pp}$, (b) $6mA_{pp}$, (c) $8mA_{pp}$, and (d) $12mA_{pp}$.

Fig. 10 shows the measured eye-diagrams of a single-channel CG TIA at different data rates of 622Mb/s, 1Gb/s, 1.8Gb/s and 2.5Gb/s, respectively, for $2^{31}$-1 PRBS input data stream (i.e. 12μ$A_{pp}$ input current signals). The output voltage signal is measured to be 270m$V_{pp}$. Fig. 11 demonstrates the measured AC response of the CG TIA, where the TZ gain of 87dBΩ with 1.4GHz bandwidth is obtained. Also, it shows the measured crosstalk between TX and RX, where the RX crosstalk of less than –20dB is achieved within the bandwidth when the TX array is turned on.

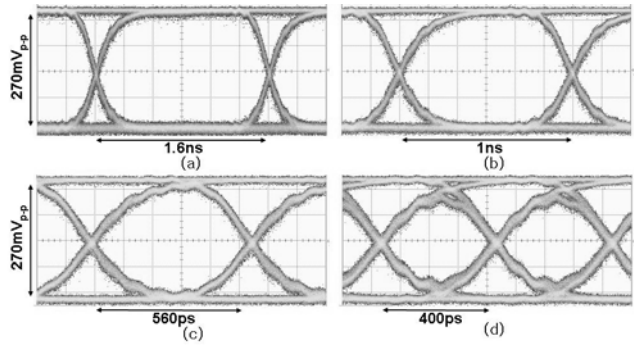


Fig. 10. Measured eye-diagrams of a single-channel CG TIA for $2^{31}$-1 PRBS at the different data rates of : (a) 622Mb/s, (b) 1Gb/s, (c) 1.8Gb/s, and (d) 2.5Gb/s.

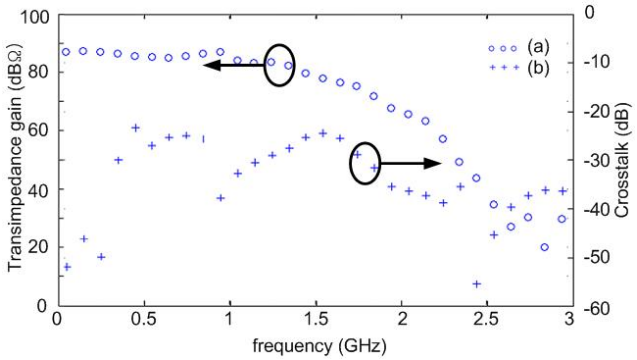


Fig. 11. (a) Measured frequency response of the CG TIA, and (b) measured crosstalk between TX and RX.

TABLE I. PERFORMANCE COMPARISON OF GIGABIT TIAS

| **Parameters** | **[1]** | **[3]** | **[4]** | **This work** |
|---|---|---|---|---|
| Technology | 0.18μm CMOS | 0.18μm CMOS | 0.18μm CMOS | 0.18μm CMOS |
| Input config. | CS | RGC & ind. peaking | CG | CG |
| TZ gain | 76dBΩ | 87dBΩ [TIA+LA] | 71dBΩ | 87dBΩ |
| BW | 724MHz | 7.6GHz | 1.8GHz | 1.4GHz |
| Input capacitance | 6pF | 0.15pF | 0.8pF | 2pF |
| Sensitivity ($10^{-12}$ BER) | -18dBm | -16dBm | -20dBm | -18dBm |
| Power dissipation | 90mW | 210mW | 40mW | 50mW |
| **FoM** | 19.2 | 4.84 | 12.8 | **79.1** |

Table 1 compares the performance of the CG TIA along with other recently published gigabit TIAs. It is clearly seen that this work shows superiority in terms of FoM (Figure of Merit) which is defined by,

$$FoM = \frac{TZ\_gain(k\Omega) \times BW(GHz) \times C_{PD}(pF)}{power\_diss.(mW) \times sensitivity(mW)}. \quad (2)$$

Table 2 summarizes the performance of the proposed transceiver array chip. DC measurements reveal that the dual-channel optical transceiver array consumes 500mW in total.

TABLE II. PERFORMANCE SUMMARY OF TRANCEIVER ARRAY CHIP

| **Parameters** | **Measured Results** | |
|---|---|---|
| | **TX** | **RX** |
| Operation speed | 2.5Gb/s | 2.5Gb/s (BW : 1.4GHz) |
| Device parasitic capacitance | 0.5pF | 2.0pF |
| Transimpedance gain | - | 87dBΩ |
| Sensitivity ($10^{-12}$ BER) | - | -18dBm |
| Total jitter(pp) | 22ps (0.055 UI) | 62ps (0.155 UI) |
| Output signal amplitude | 20m$A_{pp}$ (max.) 4m$A_{pp}$ (min.) | 270m$V_{pp}$ |
| Max. power dissipation | 200mW / ch | 50mW / ch |
| Chip size | 1.3 x 1.4mm$^2$ | |

## V. CONCLUSIONS

A dual-channel ESD-protected optical transceiver array has been realized in a 0.18μm CMOS technology for the applications of high-speed digital interface. The proposed transmitter circuit operates at 2.5Gb/s with reliable and simultaneous APC (5-15mA) & AMC (4-20m$A_{pp}$) controls, while the receiver circuit exploiting a common-gate TIA demonstrates 87dBΩ transimpedance gain and 2.5Gb/s speed for 2pF large input parasitic capacitance. Hence, the proposed transceiver array provides a feasible low-cost solution for high-speed parallel digital interface.


## ACKNOWLEDGMENT

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## REFERENCES


[1] B. –Y. Choi et al., "A 1Gb/s Optical Transceiver Array Chipset for Automotive Wired Interconnects", *IEEE Proc. of ISCAS,* pp. 181-184, May 2007.

[2] Q. Le et al., "A Burst-Mode Receiver for 1.25-Gb/s Ethernet PON With AGC and Internally Created Reset Signal", *IEEE J. of Solid-State Circuits*, Vol. 39, pp. 2379-2388, Dec. 2004.

[3] W. –Z. Chen et al., "A 1.8-V 10-Gb/s Fully Integrated CMOS Optical Receiver Analog Front-End" *IEEE J. of Solid-State Circuits*, Vol. 40, pp. 1388-1396, Jun. 2005.

[4] C. –M. Tsai et al., "A 40mW 3.5kΩ 3Gb/s CMOS Differential Transimpedance Amplifier Using Negative-Impedance Compensation", *IEEE ISSCC Tech. Digest*, pp. 52-53, Feb. 2007.