A 10b 120MS/s SAR ADC with Reference Ripple Cancellation Technique

Xiyuan Tang[1], Yi Shen[1,2], Linxiao Shen[1], Wenda Zhao[1], Zhangming Zhu[2], Visvesh Sathe[3], and Nan Sun[1]
[1]University of Texas at Austin, Austin, TX; [2]Xidian University, Xi'an, China; [3]University of Washington, Seattle, WA
Email: xitang@utexas.edu, nansun@mail.utexas.edu

***Abstract*—This paper presents a 10-bit 120MS/s SAR ADC. A novel reference ripple cancellation technique is proposed to address the reference settling issue during high-speed DAC switching. Instead of consuming power/area to ensure a fast recovery or small ripple, it provides a feed-forward path for the reference ripple and performs cancellation at the comparator input, thus guaranteeing a ripple-free signal. A 5-bit dedicated DAC is configured to emulate the ripple transfer function of the main DAC. A 40nm CMOS prototype achieves a Walden FoM of 15fJ/c-s while requiring only 3pF decoupling capacitor.**

***Index terms*— Analog-to-digital converter, successive approximation register, high speed, reference ripple.**

I. Introduction

High-speed medium-resolution analog-to-digital converters (ADCs) are widely used in measurement instruments, serial link transceivers, and wireless communication systems. Due to its scaling friendly architecture, SAR ADC has gone beyond 100MS/s with $\geq$ 10b resolution in advanced processes [1]–[4]. A critical limiter for achieving precision and speed simultaneously in SAR ADC is the reference settling due to DAC switching, which can cause wrong comparator decision. As CMOS technology scales down, it is usually limited by the package bond-wire LC resonance [5], [6], which causes ringing during reference ripple settling. Two conventional ways to address the reference ripple issue are described in Fig. 1. With an on-chip reference buffer, the ripple typically shows up as a sudden droop at the DAC switching moment. A wide-band reference buffer can ensure the droop is fully recovered before the next comparison; however, it consumes large power (4x larger than the ADC core as in [1]). The other is to place a large decoupling capacitor on the reference line to suppress the ripple amplitude to be well within 1 LSB. Although this scheme does not consume power, it costs considerable area (200x bigger decoupling capacitor than the CDAC in [2]). To reduce the power/area cost, [5] uses a smaller reservoir capacitor to stabilize the reference, but the reservoir capacitor is still 80x bigger than the CDAC. [7] introduces an additional 3-bit DAC to compensate the non-binary DAC steps caused by the passive charge sharing, while still requiring a 20x reservoir capacitor. [3] adjusts the comparator threshold to provide redundancy to tolerate ripple induced conversion error. It greatly reduces the decoupling capacitor size, but it adds an extra error detection step that slows down the SAR conversion.

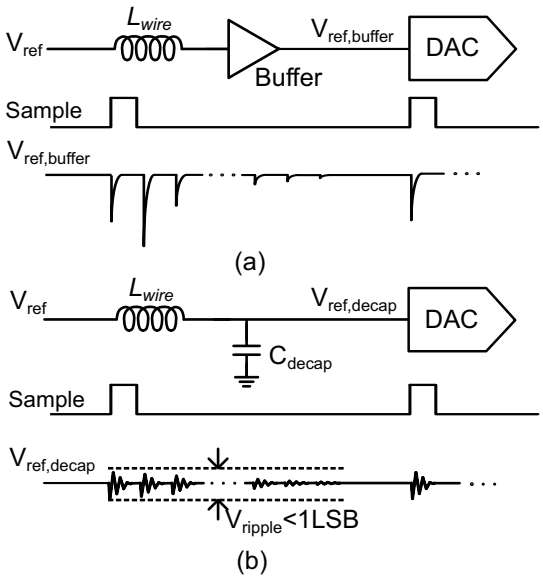

Fig. 1. Reference voltage driven by (a) wide-speed buffer and (b) large decoupling capacitor.

In addition, it cannot address any ripple induced conversion error after the error detection bit.

This paper proposes a new perspective to address the reference ripple problem. The core concept of prior approaches is to minimize the ripple, so that it does not show up at the comparator input. By contrast, this work lets the full-sized ripple to show up at the comparator input. To prevent the ripple from corrupting the comparator decision, it introduces an extra path for the ripple to reach the comparator input but with an opposite sign by inverting the polarity in a multi-path comparator, so that the effect of the ripple is cancelled. The proposed ripple cancellation technique improves the SNDR by >8dB and reduces the worst-case INL/DNL by 10x in a 10-b 120MS/s prototype ADC with only a 3pF decoupling cap.

The paper is organized as follows. Sec. II describes the proposed high-speed SAR architecture. Sec. III presents the circuit implementation including the ripple cancellation technique. Sec. IV shows measured results. The conclusion is drawn in Sec. V.

II. Proposed SAR ADC Architecture

Fig. 2 shows the block and timing diagram of the SAR ADC with the proposed ripple cancellation technique. A small

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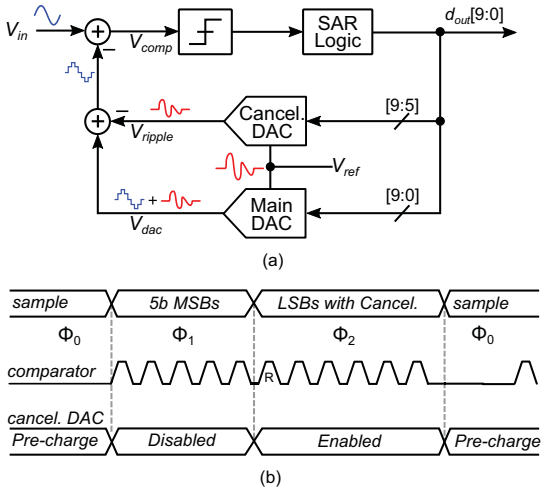

Fig. 2. Proposed ripple cancellation technique and timing diagram.

cancellation DAC is added to provide the feed-forward path for the reference ripple. Note that it only passes the ripple, but not the signal, in order to prevent any signal attenuation. Nevertheless, because the ripple transfer function from the main DAC reference to the comparator input is code dependent, the information of the MSB conversion results is still needed for the cancellation DAC to produce the same amount of ripple to achieve the maximum cancellation. In other words, although the cancellation DAC takes the MSB decisions, $d_{out}[9:5]$, they are not used to generate a proportional output; instead, they are used to guide the cancellation DAC to emulate the ripple transfer function of the main DAC.

The operation procedure is as follows. During first 5 MSB decisions, the SAR performs the normal operation. From the 6^{th} comparison, the cancellation DAC is enabled and uses $d_{out}[9:5]$ to produce the same ripple, V_{ripple}, as the MSB portion of the main DAC, so that the majority of the ripple is cancelled at the comparator inputs. The 6^{th} bit $d_{out}[5r]$ is a redundant bit which provides 32 LSB redundancy to absorb the MSB decision errors before the cancellation DAC is enabled. Although the LSB DAC updates will slightly change the ripple transfer function of the main DAC, their effects are negligible due to the small LSB DAC size, which is described in detail in Sec. III-B. Overall, the proposed technique guarantees a 16x (or 24dB) ripple cancellation throughout the LSB comparisons.

Note that the proposed technique can cancel the reference error not only due to DAC switching but also any other unwanted coupling from power supply, substrate, or adjacent clock/signal wires. This is a major advantage over redundancy-based ripple alleviation techniques (e.g., [3]) that do not provide any protection after the redundant bit. If an unwanted perturbation happens at the LSB decision, the redundancy-based technique would fail, while the proposed ripple cancellation technique still works and can ensure a correct comparator decision.

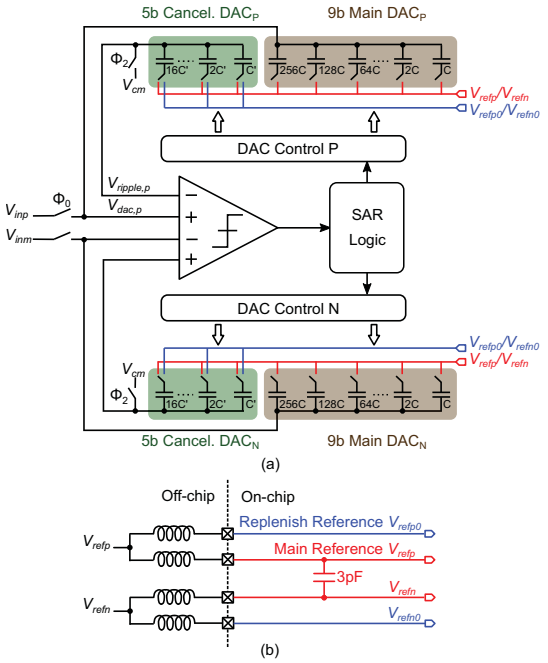

Fig. 3. Simplified SAR ADC schematic including ripple cancellation DAC.

III. Circuit Implementation

A. Proposed ADC Schematic

The schematic of the proposed ripple cancellation technique embedded 10-bit SAR ADC is shown in Fig. 3(a). It consists of a differential main DAC, a differential cancellation DAC, a 4-input comparator, and an asynchronous SAR logic. Different from a conventional SAR ADC, a dedicated pair of replenish references, V_{refp0}/V_{refn0}, is introduced to ensure the cancellation accuracy. The replenish references, along with the main references, V_{refp}/V_{refn}, are provided by four PADs separately, but connected off-chip as described in Fig. 3(b). The charge drawn from the replenish references is negligible as the cancellation DAC does not have any charge redistribution, and thus, V_{refp0}/V_{refn0} does not have any settling issue. Thanks to the proposed technique, large on-chip decoupling capacitor is not needed. A decoupling capacitor of only 3pF is loaded between the main references V_{refp} and V_{refn} to suppress its ripple to be within the redundancy coverage. The unit capacitor of the main DAC and the ripple cancellation DAC are chosen to be 2fF and 8fF, respectively, considering the kT/C requirement. A 4-input strong-arm latch is used to receive both DAC outputs and perform subtraction.

B. Ripple Cancellation DAC and Operation

Fig. 4 shows the schematic and the operation of the cancellation DAC, which is at the heart of the proposed ripple cancellation technique. It needs to be specially designed to pass the same amount of ripple as the MSB section of the main DAC while not producing any signal. The conventional CDAC does not work as it would inevitably cause charge redistribution and output voltage shift. The proposed cancellation DAC consists of two arrays of identical capacitors,

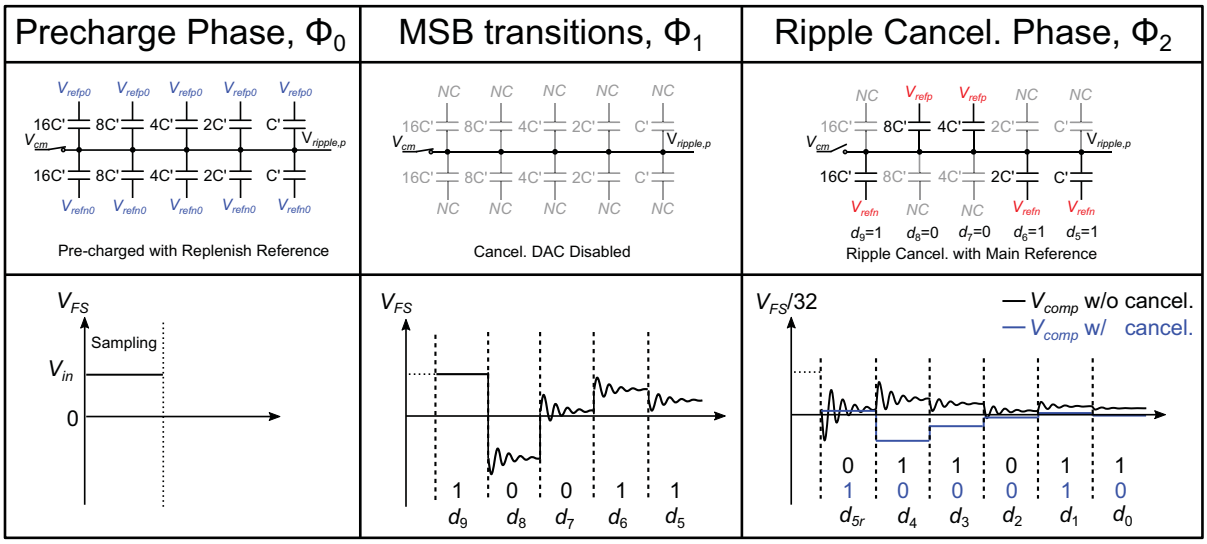

Fig. 4. Cancellation DAC operation and signal behavior of the comparator's input w/ and w/o cancellation.

which are used to pre-store an accurate reference voltage. This voltage is provided by the replenish reference, V_{refp0} and V_{refn0}, during the ADC sampling phase Φ_0. During the first 5 MSB comparisons, the bottom plates are floating to prevent the comparator kick-back noise to interfere with the reference voltage. The top plates are always connected to V_{cm} during Φ_0 and Φ_1. Once the first 5 MSB comparisons are finished, $d_{out}[9:5]$ are loaded into the ripple cancellation DAC. For example, if $d_{out}[9]=1$, the upper 16C' will be connected to the main reference V_{refp} while the lower 16C' will remain floating. On the other hand, if $d_{out}[9]=0$, the upper 16C' will remain floating, while the lower 16C' will be connected to V_{refn}. Since all capacitors have been pre-charged in Φ_0, this reconfiguration of the capacitor connection does not cause charge redistribution, and thus, the nominal output of the cancellation DAC remains at V_{cm}. Yet, if we discard the floating capacitors, the cancellation DAC indeed has the same configuration as the MSB portion of main DAC, and thus, ensures that the transfer function from the reference to the cancellation DAC output is the same as that of the main DAC, leading to the precise ripple cancellation for the MSB portion. The reference ripple induced by the LSB portion is attenuated by the capacitor ratio between LSB and MSB portions. Assuming N is the total bit of main DAC array and M is the bit of the cancellation DAC, after which ripple cancellation is enabled. The general expression of the residue reference ripple at k-th comparison can be represented as:

$$V_{ripple\_error}(k) = \frac{\sum_{i=1}^{N-M}(C_i \times D_i)}{\sum_{i=1}^{N} C_i} \times e(k) \qquad (1)$$

where $e(k)$ is the differential reference line error at k-th comparison, D_i is the decision result $\in \{-1, 1\}$, and C_i is the capacitor size of each bit. In this design, C_{M+1} is the redundant capacitor and has the same weight as C_M. The

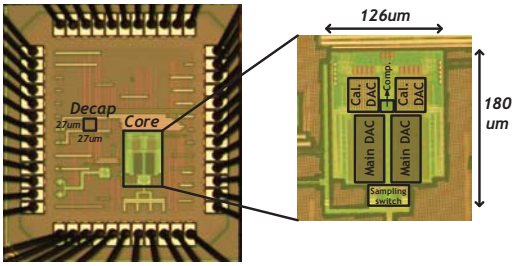

Fig. 5. Die micrograph.

residue ripple achieves maximum value when all D_i equal to same value:

$$V_{ripple\_error}(k) \leq \frac{1}{2^{M-1}+0.5} \times e(k) \qquad (2)$$

With $N=9$ and $M=5$, the reference ripple is attenuated at least by 16x at comparator input during LSB conversions. Since the ripple is smaller due to the LSB DAC size, the ripple induced error at the comparator input is negligible after the attenuation.

As shown in Fig. 4, without the ripple cancellation technique, any reference error >1LSB may cause a wrong comparison result. With the cancellation technique, the ripples during the critical LSB decisions are cancelled out, leading to correct ADC outputs.

IV. Measurement Results

As shown in Fig. 5, the prototype ADC in 40nm CMOS occupies an active area of 0.028mm^2. Fig. 6 shows the measured static performance. With the proposed ripple cancellation technique, the peak DNL and INL are reduced from +5.9/−1 LSB and +6.1/−4.3 LSB to +0.59/−0.6 LSB and +0.7/−0.73 LSB, respectively.

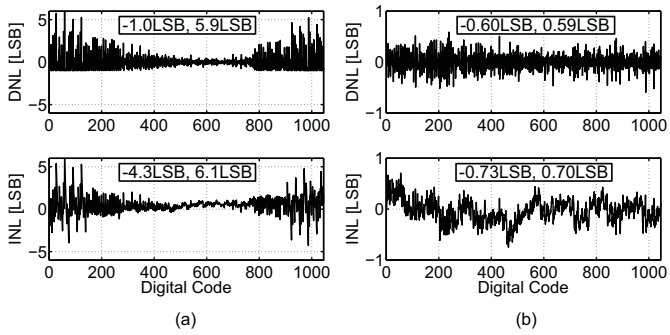

Fig. 6. Measured DNL/INL (a) without and (b) with ripple cancellation.

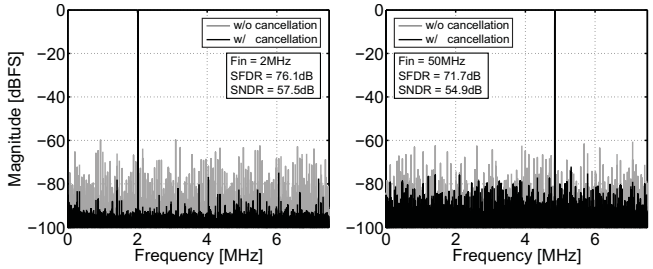

Fig. 7. Measured FFT spectrum with low frequency input and Nyquist rate input with 120MHz sampling rate (output decimated by 8).

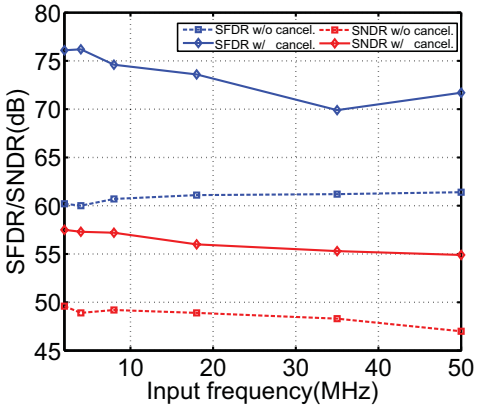

Fig. 8. Measured SFDR and SNDR versus input frequency.

As shown in Fig. 7, at low input frequency, the SFDR/SNDR are improved by 16dB/10dB to 76.1dB/57.5dB, respectively. At Nyquist frequency, the SFDR/SNDR are improved by 9dB/8dB to 71.7dB/54.9dB, respectively. Appreciable performance improvements are observed across all frequencies ranges as shown in Fig. 8. The ADC consumes 1.1mW from a 1.2V power supply. The power breakdown is as follows: 0.41mW for sampling and comparator, 0.38mW for digital circuits including extra logics for ripple cancellation, and 0.33mW for the reference. The measured peak Walden figure-of-merit (FoM) is 15.2fJ/conversion-step. As shown in Table I, the proposed ADC achieves the state-of-the-art performance. It only has a 3pF decoupling cap, which is enabled by the proposed feed-forward ripple cancellation technique.

TABLE I
PERFORMANCE COMPARISON.

	This work		[2]	[3]	[4]	[8]
Architecture	**SAR**		SAR-$\Delta\Sigma$	SAR	SAR	CI-SAR
Technology [nm]	**40**		28	65	28	40
Resolution [bit]	**10**		12	11	12	10
Sample Rate [MS/s]	**120**		600	100	100	80
Supply Voltage [V]	**1.2**		1.2 -1.5	1.2	1.1 -1.2	1.1
Area [mm^2]	**0.023**		0.076	0.011	0.007	0.08
Decap/Reservoir [F]	**3p**		20p	3p	N/A	23p
On-chip Ref. Buffer	**No**		Yes	No	Yes	No
Ref. Ripple Cancel.	**No**	**Yes**	No	No	No	No
Peak SNDR [dB]	**47.4**	**57.5**	60.7	N/A	63	54.2
SNDR@Nyquist [dB]	**46.9**	**54.9**	58	59	N/A	52.3
Power [mW]	**1.04**	**1.12**	26.5	1.6	1.6	5.54
Peak FoM [fJ/c-s]	**45.3**	**15.2**	50	N/A	13.2	85
FoM@Nyquist [fJ/c-s]	**47.9**	**20.5**	68	21.9	N/A	106

V. CONCLUSION

This paper presented a 120MS/s, 10b SAR ADC with a ripple cancellation technique. By emulating and cancelling the reference ripple at the comparator input, this proposed technique greatly relaxes the reference settling requirement, thus enabling a smaller area overhead of decoupling capacitor. The measured result demonstrates that the SNDR can be improved at least by 8dB with only a 3pF on-chip decoupling capacitor.

VI. ACKNOWLEDGMENT

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