Terahertz Imaging with CMOS/BiCMOS Process Technologies

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***Abstract*— Contrary to the common belief, silicon devices may very well operate beyond their cut-off frequency. The push towards terahertz frequencies, though, presents both challenges and opportunities for emerging applications. This paper summarizes recent attempts to use foundry-level silicon process technologies for the realization of terahertz electronic systems.**

I. Introduction

Historically, terahertz radiation was generated by optical means with the help of femto-second laser pulses and was primarily used for spectroscopic purposes in the scientific community [1]. This band, which is defined by the sub-mmWave band from 300 GHz through 3 THz, is often referred to as the *THz gap*, loosely describing the lack of adequate technologies to effectively bridge this transition region between microwaves and optics. The use of either electronic or photonic techniques has led to the subdivison in *THz Electronic* and *THz Photonic* bands with frequencies spanning from 100 GHz through 10 THz as illustrated in Fig 1.

Applications for silicon technologies may be subdivided into communication, radar, and mmWave/THz imaging and sensing applications as illustrated in Fig. 2. Emerging THz technologies could spur economic growth in the safety, healthcare, environmental and industrial control area, as well as in security applications [2]. The latter one is creating some excitement because THz radiation can penetrate a number of materials such as clothes, paper, cardboard, and many plastic or ceramic materials [3]. Industrial product and process control [4]–[6] is used in pharmaceutical product inspection [7] and biomedical imaging [8]. Terahertz radiation benefits from the fact that it's photons have low energies (1 THz equals only 4.1 meV), and thus cause no potentially harmful photo-ionization in biological tissues.

This paper summarizes the ambitious technology development efforts underway to bridge the THz-gap by electronic means in Sec. II. In particular the paper summarizes the recent attempts to use foundry-level silicon technologies for terahertz imaging (see Sec. III). This includes as summary of circuits for passive imaging in Sec. III-A and active imaging in Sec. III-B. Active imaging requires illumination sources which are described in Sec. IV. The paper further presents a comparison of direct and heterodyne detection principles. Circuit design examples present the feasibility of the presented approaches. In particular direct detection in CMOS technologies is presented

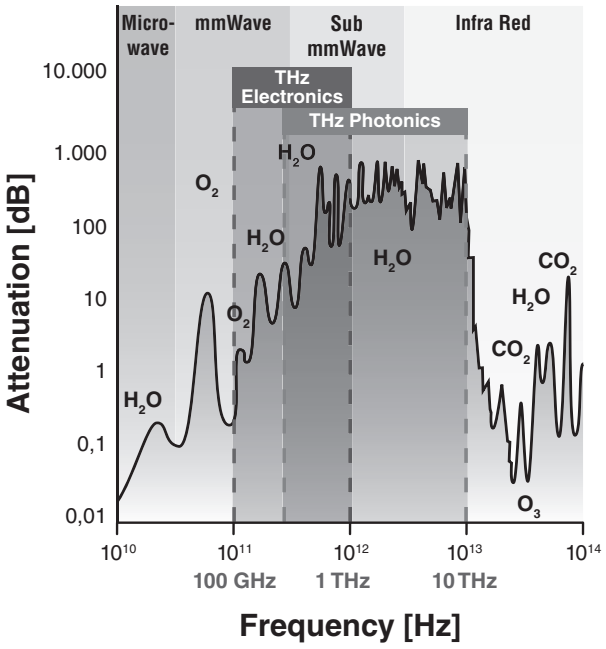

Fig. 1. Atmospheric absorption showing the terahertz spectrum and the subdivision into *THz Electronic* and *THz Photonic* bands indicating the different approaches for signal generation and detection.

in Sec. V, and a sub-harmonically pumped 650 GHz heterodyne imaging front-end in Sec. VI respectively. The fact that even low-f_T NMOS devices can be used for the detection of terahertz radiation above their cutt-off frequency is explained by non-quasi static FET device modeling of resistive mixers. Direct detection images at 650 GHz in transmission mode are finally presented in Sec. VII, which demonstrate the potential of silicon process technologies for emerging terahertz imaging applications.

II. Terahertz electronics

Electronic detection methods in the terahertz range are commonly divided into two main categories: coherent (heterodyne) detection and incoherent (direct) detection methods. Direct detectors have been around for many years and are based on the physical principle of energy/power absorption (calorimeters/bolometers [10], [11]), pneumatic detectors (Golay cells

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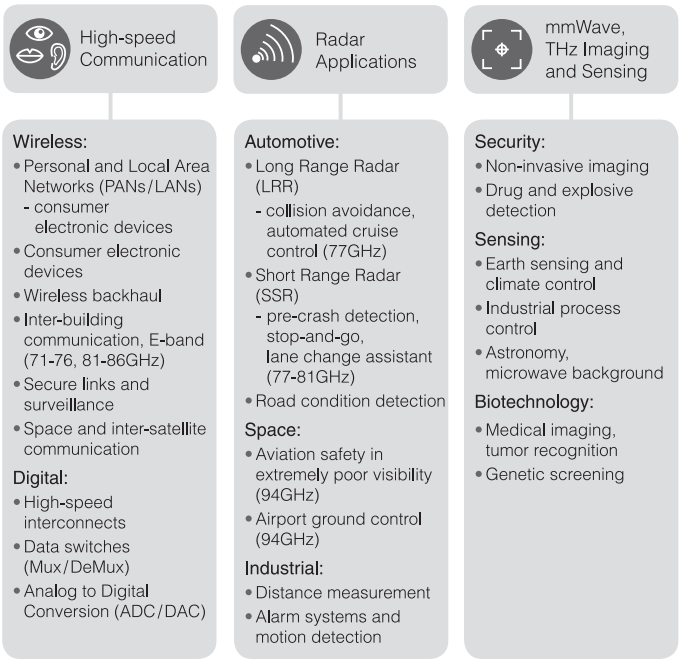


Fig. 2. Potential applications for silicon integrated mmWave and THz circuits [9].

[12]), and square-law detectors such as Schottky Barrier Diodes (SBDs). Most of them are, however, incompatible with conventional microelectronics and require cryogenic cooling and/or additional processing steps to be incorporated into today's semiconductor process technologies. Because of this, there are ambitious technology development efforts underway to bridge the THz-gap with standard circuit design techniques.

Ambitious III/V technology development efforts, funded by DARPA programs such as the TIFT (Terahertz Imaging Focal-plane Technology) and the SWIFT (Sub-millimeter Wave Imaging Focal-plane Technology) program, have recently pushed the usable frequency range of LNAs into the 600 GHz range [13]. The Fraunhofer IAF has recently published a 35nm mHEMT technology with f_T/f_{max} of 515/750 GHz for the implementation of a 220-325GHz four-stage cascode LNA with 20dB-gain and a NF of 6.9 dB in [14].

Silicon process technologies, however, continue to scale down further, bringing the advantages of silicon integrated circuits to future terahertz applications. The EU project DOTFIVE [9], for instance, targets a 500 GHz f_{max} SiGe technology and recently CMOS technologies have achieved f_T/f_{max} of 425/350 GHz [15]. Schottky barrier diodes may also be integrated in silicon with cut-off frequencies beyond 1 THz [16], [17].

III. Terahertz imaging

Terahertz imaging systems often consist of heterodyne or direct detection receivers made of monolithic microwave integrated circuits (MMICs) [18]. The high cost of MMICs, however, limit the pixel count in imaging systems and the use of LNAs is typically limited to below 200 GHz in practical applications [19].

A. Passive (radiometry) imaging

Passive radiometric imaging is the preferred method for outdoor stand-off detection and for systems working at distances of a few meters to several kilometers. Such imagers typically operate in the 50-110-GHz frequency range and rely on temperature differences of the imaged object, where the cold sky helps to improve the image contrast. The main benefit of radiometric detection of the background temperature at large imaging distances is that no high-power source is needed to illuminate the scene. Some problems associated with point-source active illumination, such as poor visibility of metal surfaces due to specular reflections, are also eliminated. On the other hand, the resolution of passive systems is limited by the comparatively long wavelengths used for minimum attenuation in the atmosphere. Due to the lack of phase information in the received signal the ability to perform ranging (radar) is also limited.

A 2D focal-plane array is the optimum configuration for a passive system since it lets all pixels continuously collect photons and thus maximizes the integration time for a certain frame rate. The individual detectors can either be based on bolometers, as addressed by the DARPA MIATA [20] program, or diode detectors equipped with low-noise amplifiers (LNAs). While non-cooled bolometers have sufficient sensitivity for active imaging [21] cryogenic cooling is needed to reach an NEP of less than 10 fW/$\sqrt{Hz}$ [11]. LNA-based systems can, by contrast, avoid the need for cryogenic cooling provided that amplifiers with a low enough noise figure (NF) are available, thus yielding field-deployable imaging solutions. Developments of suitable LNAs and diode detectors for non-cooled radiometer arrays is addressed by the DARPA THz Electronics program [13].

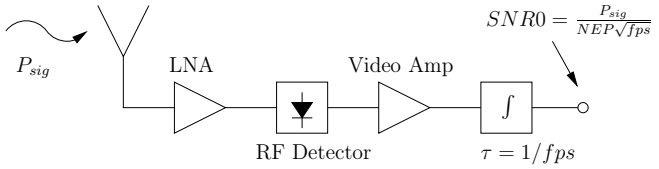
Present LNA-based passive imaging detectors are mainly implemented using InP devices with 3-5 dB noise figures at 94 GHz, thus yielding noise-equivalent temperature differences (NETD) down to 0.32K [22] with a 30-ms integration time. Radiometers based on mHEMT transistors offer similar performance [23]. A silicon-based radiometer, recently published in [24], has reached a minimum NETD of 0.69K (30 ms) using a commercial 0.12-μm f_T/f_{max} = 200/265-GHz SiGe technology. Hence, it can be seen that the performance of silicon technologies is close to fulfilling the needs of passive imaging, but further improvements of noise figure are needed to match the performance of current III-V-based systems. Advances in SiGe HBT and CMOS technology will reduce the performance gap but the advantages of highly integrated silicon detectors can only be leveraged by a system redesign as opposed to one-to-one replacement of III-V MMICs in present systems.

B. Active imaging

Active imaging systems use THz sources for illumination to achieve a higher contrast or better signal-to-noise ratio. A

fast frequency agility may also provide spectroscopic identification of materials. Active imaging distinguishes itself from *passive* (radiometry) imaging, because one often detects the radiation as electric-field amplitude and phase similar to radar applications. This enables imaging with three-dimensional and tomographical content which enhances the object detection capabilities [25], [26]. Active imaging sensors are defined in one of two ways, depending on whether the system uses (i) direct detectors as receivers where the sensitivity is defined as NEP and integration bandwidth, or (ii), heterodyne receivers where the sensitivity is determined by the noise figure and integrated bandwidth. See Fig. 3 for an illustration of the different receiver approaches.

a) Active Direct Detection



b) Active Heterodyne Detection

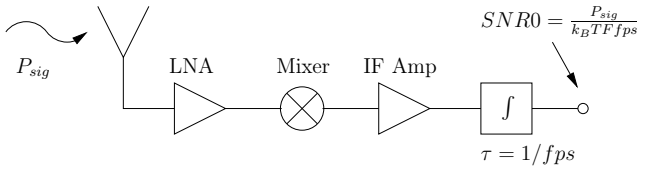


Fig. 3. Active imaging receivers. A direct detection receiver is shown in figure a), whereas figure b) shows a heterodyne receiver.

The overall system specification of an active imaging system depends greatly on the application requirements such as the imaging mode (transmission or reflection), the required spacial resolution, and the expected sensitivity. For the purpose of detector comparison, direct and heterodyne receiver architectures may be analyzed for a fixed video rate (e.g. 25 fps) and a fixed received power level (e.g. $P_{sig} = -50$ dBm, 10 nW) at the antenna port. The video rate sets a limit on the maximum available integration time per pixel ($\tau = 1/\text{fps}$).

For a given video rate (fps), the SNR0 for active direct detection can be written as,

$$SNR0 = \frac{P_{sig}}{NEP\sqrt{fps}}, \tag{1}$$

where the noise-equivalent power (NEP) is defined as the power at which the signal-to-noise ratio SNR0 is unity for a detector time constant of $\tau = 1$ s. For active heterodyne detection the SNR0 can be written as

$$SNR0 = \frac{P_{sig}}{k_B TF fps}, \tag{2}$$

where F is the noise factor and $k_B T$ is the thermal noise power at temperature T.

The results of Eqn. 1 and 2 is shown in Fig. 4. The figure shows the direct detection NEP and heterodyne NF versus the

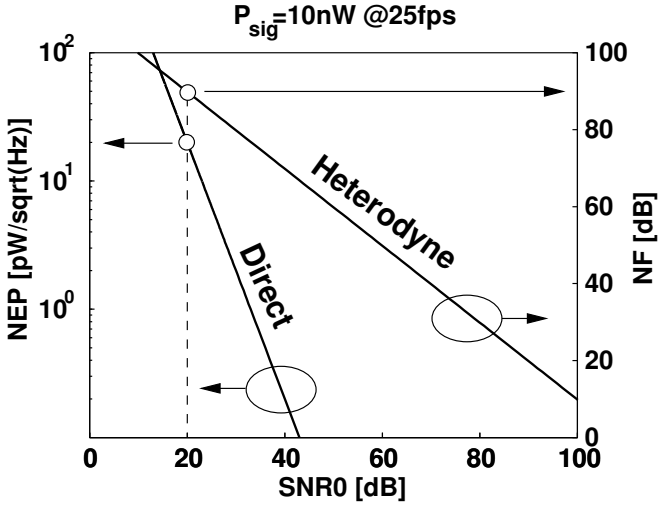


Fig. 4. Comparison of direct detection and heterodyne receiver performance for active imaging applications. To obtain images with a 20-dB SNR0 for instance, one requires a system NEP of 20 pW/$\sqrt{Hz}$ in direct detection, but a heterodyne receiver NF of only 90 dB. The comparison at room temperature is based on a 25-fps video rate with $P_{sig} = 10$ nW at the receiver pixel.

imaging SNR0. For a 20-dB SNR0 for instance, one requires a system NEP of 20 pW/$\sqrt{Hz}$ in direct detection, but a heterodyne receiver NF of only 90 dB. Note, the comparison is done for detection at room temperature with a 25-fps video rate and a $P_{sig} = 10$ nW at the receiver pixel. The details of the imaging setup, such as the physical FPA size, number of pixels, total transmit power, and the path loss may lower the received pixel power P_{sig}, but the lower received power affects both detection schemes equally.

This analysis clearly shows the superior performance of heterodyne detection in active imaging applications, because noise figures may be as low as 42 dB in silicon at 650 GHz as will be shown later in Sec. VI. However, implementation issues such as limitations of the LO drive power, the LO distribution, and the total DC power consumption limit the number of heterodyne pixels in practical applications. The CMOS direct detectors presented in Sec. V with NEPs as low as 50 pW/$\sqrt{\text{Hz}}$ at 650 GHz, therefore, present an attractive alternative which easily can support large arrays with 20.000 pixels.

IV. Submillimeter sources in silicon for terahertz imaging

At lower mmWave frequencies, where silicon devices still exhibit power gain, amplifiers suffer from their low breakdown voltages. High-performance SiGe HBTs exhibit breakdown voltages of $BV_{ceo} = 1.5$ V and $BV_{cbo} = 4.5$ V [9], while RF CMOS suffers from low drain voltages of about 1 V in 65 nm technologies [27]. At lower mmWave frequencies, state-of-the-art SiGe power amplifiers have demonstrated saturated output powers as high as 20 dBm at 60 GHz [28] and recently up to 8 dBm at 160 GHz in [29]. Submillimeter sources for terahertz imaging, however, need to operate transistors close to, or even above, their cutoff frequencies. Because of this, silicon based submillimeter wave sources have

only demonstrated comparatively low output power in the past. Power generation techniques beyond the cutoff frequency are done in one of two ways, (i) directly extracted from oscillators, or (ii), up-converted from lower frequencies by the help of frequency multiplier chains.

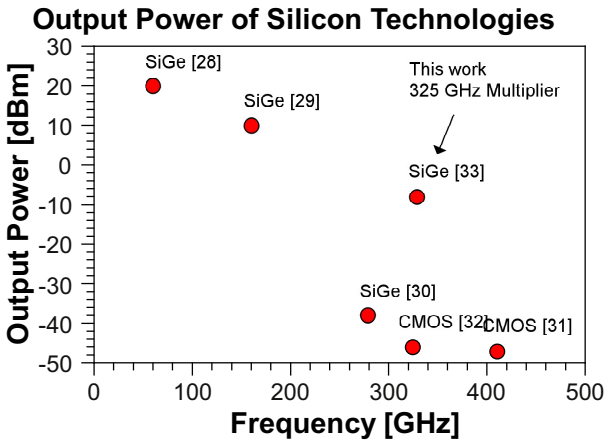


Fig. 5. Published submillimeter sources in silicon. The figure shows saturated output power versus operation frequency.

Recent publications have demonstrated silicon-based VCOs at 278-GHz with -38 dBm in [30] and -47 dBm at 410 GHz in 45-nm CMOS in [31], respectively. Linear superposition techniques in CMOS have been demonstrated up to -46 dBm at 324 GHz [32]. More applicable power levels for active imaging have recently been published in [33], where a 325-GHz x18 frequency multiplier achieves up to -8 dBm. The monolithic multiplier is implemented in an f_{max}-optimized evaluation SiGe HBT technology [9] using cascaded transistor-based multiplication and amplification stages. This result compares quite well with III/V-based mHEMT multiplier chains published in [34], [34] and demonstrates the capability of silicon technologies for active illumination up to 325 GHz. A summary of integrated submillimeter sources in silicon is shown in Fig. 5 and Table I.

Fig. 6 shows the chip micrograph of the 325 GHz frequency multiplier chain. The die size is 2.2×0.43-mm^2. The circuit consists of a 325-GHz doubler circuit fed differentially by two cascaded triplers. Each tripler is equipped with a frequency selective power amplifier at the output in order to boost the power entering the next multiplier stage and to suppress spurious frequencies. A differential amplifier is used at the input to convert a 18-GHz single-ended signal from an off-chip synthesizer.

V. Direct Detection Receiver in CMOS/SiGe

Unlike heterodyne detection, incoherent (direct) detection favors multi-pixel applications such as focal-plane arrays, where the power consumption per pixel should be minimal to enable large pixel counts. Direct detectors may consist of square-law detectors implemented in either bipolar or

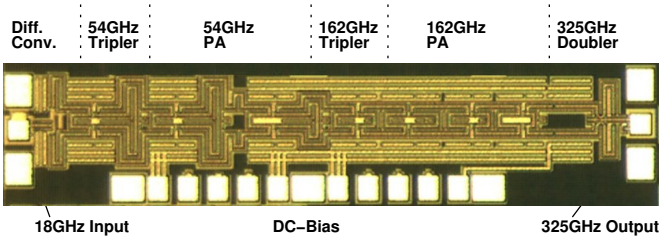


Fig. 6. Micrograph of a 325 GHz SiGe frequency multiplier chain with up to -8 dBm at 325 GHz [33].

CMOS technologies. A 600-GHz focal-plane arrays based on a differential NPN pair were first published in [36] and based on resistive mixers in [37] respectively. The high frequency noise in an SiGe HBT is dominated by the shot noise at the junctions as well as the thermal noise in the intrinsic base and emitter resistances [38]. The noise of non-biased (cold) FET transistor, however, are only limited by the thermal noise of the channel conductance and have demonstrated NEPs as low as 50 pW/$\sqrt{\text{Hz}}$ at 650 GHz in a 65-nm CMOS SOI technology [39].

This performance compares well with conventional detectors of terahertz radiation as summarized in Table II. In contrast to bolometers and diode detectors, CMOS direct detectors can be integrated with digital readout electronics and can be implemented in a standard CMOS process technology without additional processing. Fig. 7 further presents the correlation of the voltage responsivity R_v and NEP of conventional and CMOS terahertz detectors.

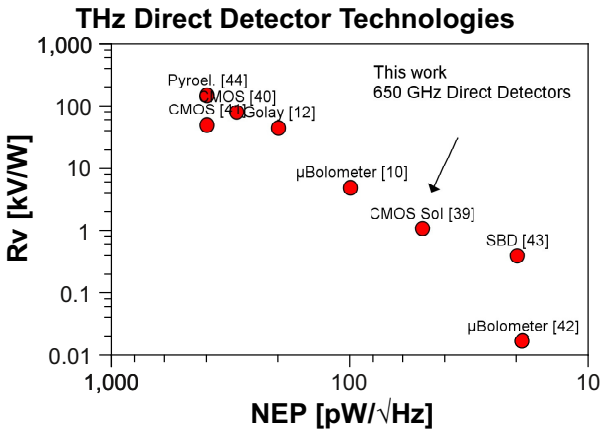


Fig. 7. Comparison of different direct detector technologies according to Table II. Current CMOS direct detector arrays have demonstrated NEPs as low as 50 pW/$\sqrt{\text{Hz}}$ at 650 GHz and compare well with conventional terahertz detector technologies.

Fig. 8 shows the chip micrograph of CMOS 650 GHz focal-plane array. The number of pixels is limited to 3×5 pixels for demonstration purposes only. Higher pixel counts are possible and are only limited by the available chip area. For instance, a 20.000 pixel array with a pixel pitch of 150×150 μm^2 would

TABLE I

COMPARISON OF INTEGRATED SUBMILLIMETER SOURCES

Technology [μm]	Circuit [μm]	BW[1]/Freq. [GHz]	Output Power[2] [dBm]	Monolithic Integration	Reference
III/V-based					
mHEMT	x6 multiplier	155-195	0	yes	[35]
mHEMT	x2 doubler	250-310	-6.4	yes	[34]
Silicon-based					
0.13-μm SiGe	x18 multiplier	317-328	-8	yes	[33]
0.45-nm CMOS	VCO	410	-47	yes	[31]
0.14-μm SiGe	VCO	278	-38	yes	[30]
90-nm CMOS	VCO	324	-46	yes	[32]

[1]3-dB output power bandwidth

[2]Peak output power

TABLE II

COMPARISON OF TERAHERTZ DIRECT DETECTOR TECHNOLOGIES

Freq. [THz]	Technology [μm]	R_v^1 [kV/W]	NEP [pW/$\sqrt{\text{Hz}}$]	Pixel [x×y]	Monolithic Integration	Cooling	Reference
0.65	65nm CMOS SOI	1.1	50	5×3	yes	no	[39]
0.65[2]	0.25 CMOS	80	300	5×3	yes	no	[40]
0.60[3]	0.25 CMOS	50	400	5×3	yes	no	[41]
0.2-30	Golay Cell	0.1-45	200-400	–	no	no	[12]
0.094	Microbolometer	0.017	19	8×8	yes	–	[42]
4.3	Microbolometer	4.97	100-300	128×128	yes	no	[10]
0.80	SBD	0.4	20	–	no	no	[43]
0.1-30	Pyroelectric	150	400	–	no	no	[44]
0.2-30	Bolometer	–	3	–	no	yes	[11]
0.65	STJ	–	–	5×5	no	0.3 K	[45]
1.6	NbN HEB	–	–	1×3	no	4.2 K	[46]

[1]Voltage responsivity

[2]Bandwidth of 45 GHz (patch antenna)

[3]Bandwidth of 125 GHz (dipole antenna)

only require a chip area of 22×22 mm^2, an area commonly occupied in visual image sensors.

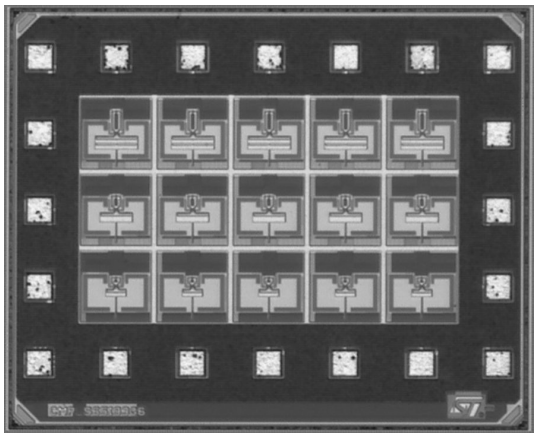


Fig. 8. Micrograph of a 650 GHz focal-plane array implemented in a 65-nm CMOS SOI technology [47]. The die has a size of 1×0.9-mm^2.

Each pixel uses a differential square-law detector made of a non-biased (cold) FET resistive self-mixer. Self-mixing is provided through the use of a gate-drain coupling capacitor. The operation principle combines low-frequency self-mixing with distributed self-mixing at very high frequencies and enables broadband detection.

The operation of the mixer at submillimeter waves, can be analyzed by the use of non-quasi-static (NQS) modeling of the resistive mixing circuit. A NQS RC-ladder model for a FET channel in the triode region was described in [40], where the channel is divided into n segments. Each segment is equipped with a variable conductance $g_n(v)$, which is controlled by the local gate-to-channel voltage $v(n)$. For strong inversion this leads to the partial differential equation of the following form:

$$\frac{\partial}{\partial x}\left[\mu(v(x,t)-V_{th})\frac{\partial v(x,t)}{\partial x}\right]=\frac{\partial}{\partial t}v(x,t) \qquad (3)$$

Equation 3 only depends on the carrier mobility μ and the bias $V_g - V_{th}$. The distributed resistive mixing response can be obtained by solving Eq. 3 for boundary conditions at the source ($v(0,t) = V_{RF}\sin\omega t + V_g$) and the drain ($v(L,t) = V_g$) side. Although Equation 3 is accurate enough for most practical circuit implementations, a more detailed hydrodynamic transistor model based on a reduced set of Boltzmann's transport equations (Euler equation of motion) may be used instead. Solutions to such equations may be found numerically with the help of the explicit finite difference discretization scheme. Results of such simulations give a deeper insight of what happens inside of the device. For instance, Fig. 9 shows the carrier density modulation at 1 THz along the channel of a 65 nm NMOS transistor. The numerical simulation was done with the help of an explicit finite difference discretization scheme for the circuit presented in [40].

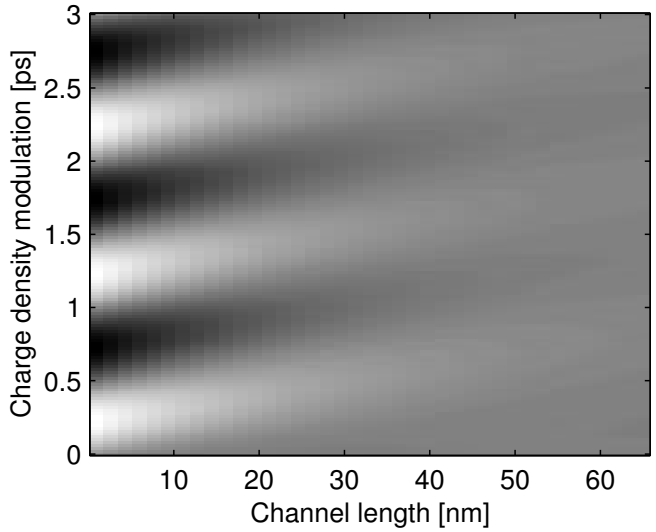


Fig. 9. Charge density modulation at 1 THz along the channel of a 65 nm NMOS transistor. The numerical simulation was done with the help of an explicit finite difference discretization scheme.

Time derivatives have been approximated with forward differences (Euler's scheme), while the spatial derivatives have been approximated with central differences. To improve spatial resolution near the source and the drain non-uniform mesh has been employed, with typical resolution of $\Delta x = 0.04 - 0.08\,\mathrm{nm}$ near the boundary of the device. Time step Δt has been chosen to ensure stability of the algorithm. For the variables not constrained with any physical boundary conditions the second order space-time extrapolation has been used to calculate their values at the boundaries.

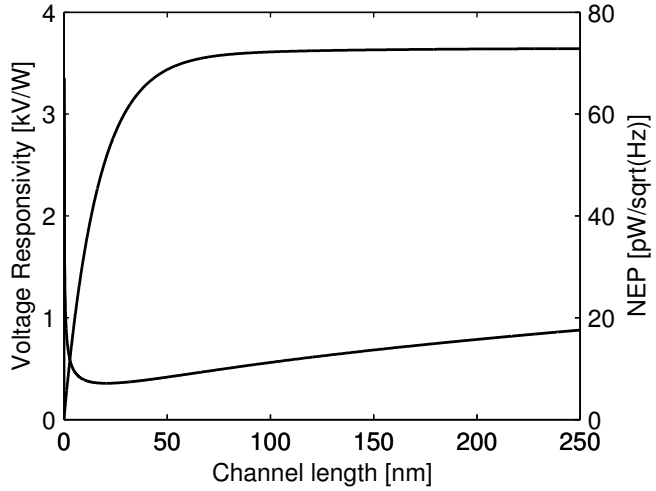


Fig. 10. Simulated voltage responsivity Rv and NEP at 1 THz up to a channel length of 250 nm. According to the results, a 1-THz CMOS direct detector should be able to achieve a minimum NEP of 10 pW/$\sqrt{(}Hz)$ in a 24 nm CMOS technology.

The direct detection response of the distributed resistive mixer builds up as a dc offset voltage along the device channel. The associated voltage responsivity R_v at 1 THz is plotted in Fig. 10 as well as the apparent NEP, which also builds up along the device channel. From the figure one can see that the R_v flattens out at about 65 nm due to damping of the carrier modulation, whereas, the NEP keeps increasing due to the continued growth of channel resistance. The simulation suggests further, that a minimum NEP of 10 pW/$\sqrt{Hz}$ at 1 THz should be feasible in a 24 nm CMOS technology.

VI. Heterodyne receiver in CMOS/SiGe

The sensitivity of active imaging systems can be significantly enhanced by the use of heterodyne detectors. A coherent receiver can filter out the continuous-wave illumination signals from the background noise with a bandwidth only limited by the required video rate (see Sec. III-B for more details on the available SNR0). Present terahertz heterodyne receivers are equipped with mixers based on Schottky diodes and waveguide technology in the front end. Such mixers can reach noise-figures of 11 dB at 590 GHz [48], but the use of discrete diodes and the requirement of a high-power LO source limit their integration capability. Quasi-optical distribution of the LO signal, as demonstrated in [49], offers a possible solution for large-scale arrays but tend to lead to low LO-drive power available to the individual mixers. Hence, MMIC-based receivers with integrated LO amplification and frequency multiplication are needed in a heterodyne imaging array in order to solve the LO distribution problem.

In the high mmWave and lower terahertz frequency range conventional transmitter and receiver circuits can be implemented in silicon technologies. Fig. 11 shows a fully integrated 160-GHz TX/RX chipset with a quadrature (I/Q) baseband interface [29], which yields a receiver NF of 11 dB and a saturated transmitter power of 5 dBm (including 2 dB of on-chip balun losses). An alternative imaging receiver front-end based on a f_T/f_{max} = 260/350-GHz SiGe HBT technology [50] provides 7.4-dB NF with the losses of the auxiliary input balun de-embedded.

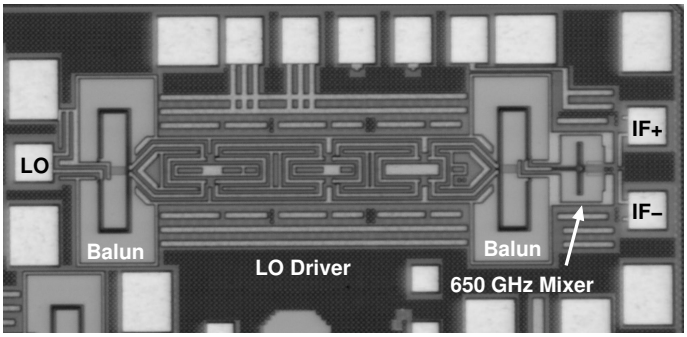


Fig. 12. Micrograph of a 650 GHz subharmonically pumped SiGe receiver presented in [47].

Frequencies above 300 GHz, where the operating frequency reaches or exceeds the f_T/f_{max} of the devices, can also be addressed by Si/SiGe technologies if a degraded performance can be accepted in the system design. Figure 12 shows a single-channel subharmonically pumped 0.65-THz imaging

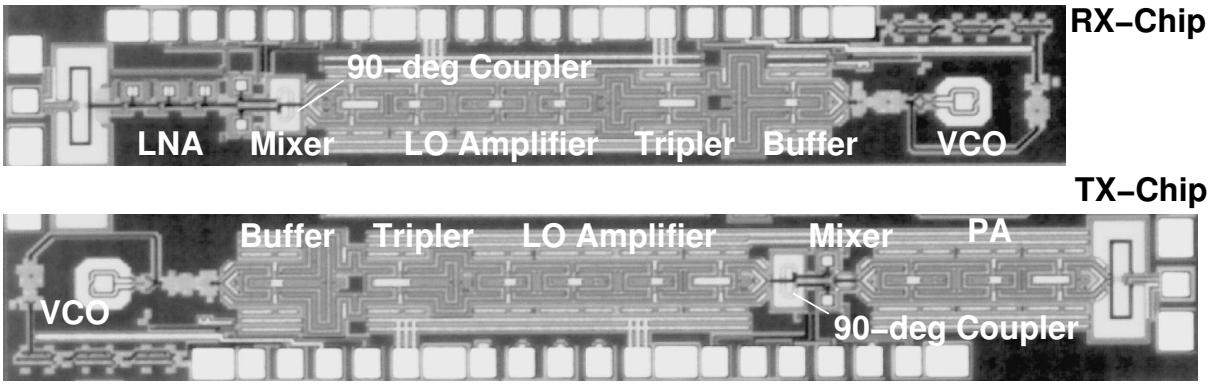


Fig. 11. A 160-GHz receiver/transmitter chipset with quadrature base band and on-chip LO generation [29].

front-end, originally presented in [47]. The receiver implements x4 subharmonic mixing with a 160-GHz LO signal and was manufactured in a 0.13-μm SiGe HBT technology. A single-balanced mixer is implemented as a differential pair, where the subharmonic LO is supplied in common-mode and the received RF signal is applied in differential mode to the HBT mixer transistors. Power combining of the free-space RF signal with the on-chip generated LO is provided by a center-fed folded-dipole antenna. The use of an integrated LO buffer and a subharmonic LO significantly simplifies the design of an imaging array and can partly compensate for the decreased noise performance compared to a fundamental frequency mixing approach. Characterization of the receiver front-end in a free-space setup yielded a conversion gain of -5 dB and 42-dB noise figure. Despite the high NF, the analysis in Sec. III-B would indicate a SNR0 of about 70 dB for an input power of $P_{sig} = 10$ nW and a $\tau = 1/25$-fps integration time. This receiver front-end, therefore, is well suited for short-range imaging applications. In addition, the use of faster devices and an optimized antenna is expected to improve the performance.

VII. Active THz Imaging Examples in CMOS

The following terahertz images were created with a 645 GHz multiplier chain for active illumination with a 0.5-mW total RF power. The carrier was amplitude modulated (electronically chopped) with a 10-kHz square-wave signal in order to facilitate the use of lock-in techniques. The power from the multiplier was radiated from an integrated horn antenna and subsequently collimated and refocused by two lenses. Objects used for transmission mode imaging were placed at the first focal point and stepper-motor actuators were used to scan objects through the focal point. A second lens system re-collimated and projected the transmitted radiation onto the CMOS 650-GHz direct detector array shown in Fig. 8 [47]. A lock-in amplifiers provide bandpass filtering around the modulation frequency with the desired video-bandwidth. Overall, this imaging setup provided an image resolution of about 1 mm with an SNR0 of about 50 dB with a $\tau = 0.3$ s integration time.

A 650-GHz image of a RFID card captured with this transmission mode imaging setup is shown in Fig. 13. The image reveals its loop antenna, the RFID chip as well as the wire bonds used to contact the antenna.

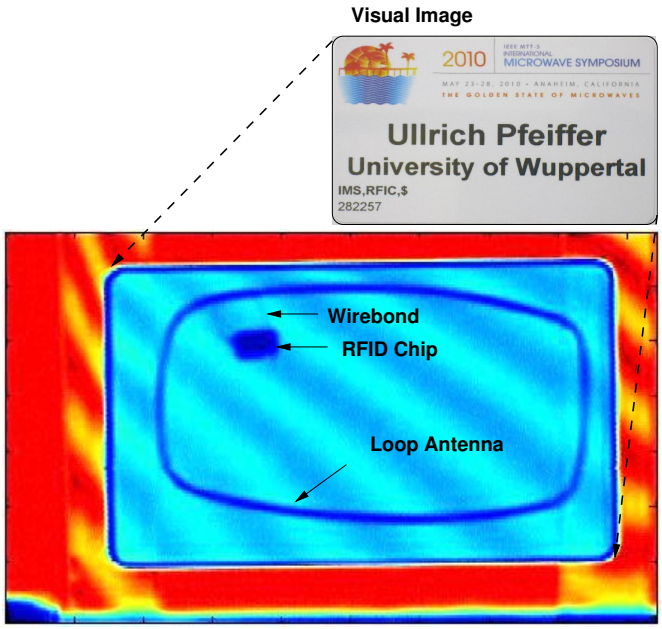


Fig. 13. A 650-GHz image of a RFID card used to enter the IMS conference. The image was captured in transmission mode and reveals its loop antenna, the RFID chip, as well as the contacting wire bonds.

Fig. 14 shows a transmission-mode image of a piece of polystyrene foam with an hidden cutter blade inside. The image contains sufficient dynamic range to resolve the structure of the foam as well as the presence of the metal cutter blade. The scanned image further reveals cracks inside the polystyrene foam caused by the insertion of the blade. The visibility of such cracks demonstrate the feasibility of the active imaging approach for industrial process control and monitoring.

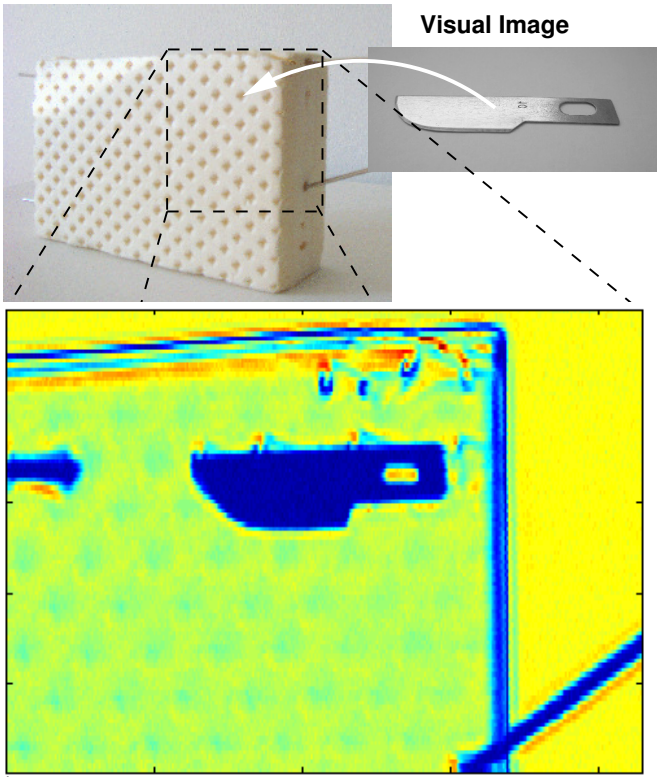


Fig. 14. A 650-GHz image of a piece of polystyrene foam with an hidden cutter blade inside. The active image not only reviels the cutter blade, but also defects inside of the sourounding form.

VIII. Summary and Conclusion

State-of-the-art CMOS and SiGe technologies have advanced to a point where *passive* imagers at 94 GHz could be realized with adequate performance. Current passive imaging systems would greatly benefit from the high integration capabilities of silicon with an increased number of pixels at a lower system cost. Additional signal processing capabilities, such as bias control and build-in self-test are coming for free and would broaden the scope of integrated passive imagers. However, the spacial diffraction limited resolution at 94 GHz is poor and requires large apertures, which in turn, limit the exploitation of such imagers.

In contrast to passive imagers, this paper presented silicon circuits for *active* imaging systems. Circuits for direct and heterodyne detection were presented at frequencies as high as 650 GHz. Active systems represent an attractive alternative to passive imagers at lower frequencies. Active systems are less demanding on noise performance and allow higher operating frequencies with a better diffraction limited resolution. Active imagers, though, require an illumination source. State-of-the-art SiGe technologies could be used for such sources, with up to -8 dBm illumination power at 325 GHz based on frequency multipliers as shown in this paper.

A room-temperature 650 GHz CMOS direct detection circuit for terahertz imaging has been presented. The detection principle has been modeled as a non-quasi-static (NQS) distributed self-mixing effect in a non-biased (cold) FET transistor. Such detectors have demonstrated NEPs as low as 50 pW/$\sqrt{\text{Hz}}$ at 650 GHz in 65 nm CMOS SOI technologies. Despite their high receiver NF, heterodyne active imaging show an increased SNR0 compared with their direct detection counterparts. A subharmonically pumped 0.65-THz imaging front-end, for instance, has demonstrated a NF as low as 42 dB and was fabricated in a 0.13-μm SiGe HBT technology.

Finally, 650 GHz transmission mode imaging examples with CMOS direct detectors have been presented, which demonstrate the potential of silicon process technologies for emerging terahertz applications.

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