SA 19.4: An EPRML Digital Read/Write Channel IC

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Extended partial-response (EPR) signaling together with suitable encoding and maximum-likelihood (ML) detection may be employed in magnetic recording systems to achieve higher storage densities than peak detection or Class 4 partial-response maximum-likelihood (PRML) methods [1, 2]. Heretofore, the complexity of a complete EPRML implementation has been deemed too high, and efforts have been directed primarily at approximating EPRML performance with modified PRML hardware. This channel IC combines extended class 4 partial response (EPR4) equalization with ML sequence detection based on the Viterbi algorithm. The EPR4 signal is well-matched to the typical readback signal in the range of normalized user densities of current and future interest, simplifying the equalizer. Anti-aliasing filtering and equalization are combined in a continuous-time filter, eliminating a FIR filter (Figure 1).

In read mode, the input signal from the pre-amp is applied to a variable-gain amplifier (VGA) to provide nominal signal level to the analog filter. During acquisition, an analog scheme based on area integration regulates normalized signal amplitude of a prescribed timing/gain preamble field between +2.0 and -2.0. During tracking, a decision-directed method estimates the gain error using equalized sample values from the A/D converter. This gain error drives a charge pump to increase or decrease VGA gain to preserve normalized sample levels [0, ±1, ±2].

The continuous-time g_m-C equalizer shapes the input waveform so, with proper timing and gain controls, the sample values obey the EPR4 signal definition, namely, x(n)=a(n)+a(n-1)-a(n-2)-a(n-3), where x(n) is the ideal sample value at time nT, T is the channel bit period, and a(n) is the binary NRZ data signal at the output of the write path. The equalizer comprises a 7th-order, 0.05° equiripple low-pass filter with independently controllable left and right s-plane zeros. The two zeros are realized by feedforward of internal differentiated signals inherent in the biquad implementation. The zeros and the cutoff frequency (fc) are programmable and can be customized during drive manufacturing and power-on for each head/media and data zone combination. The equalizer settings are determined using a channel integration assist (CIA) block that processes the ADC samples and posts results via the serial port. Firmware determines the settings to be programmed on the chip. The filter incorporates circuits to ensure that variations due to temperature and power supply are negligible. Cutoff frequency range is 5 - 45MHz, and zero control gives a gain boost of 0 - 18dB at fc. Measured filter response along with ideal EPR4 spectrum using a Lorentzian model with channel PW_{50}/T of 2.5 and a channel rate of 165MHz, are shown in Figure 2. A programmable high-pass circuit between filter output and sample/hold (S/H) input removes dc offset produced by the VGA and filter.

During idle or write mode, the voltage controlled oscillator (VCO) is locked to the output of the frequency synthesizer. On entering read mode, the timing loop operates in a high-bandwidth acquisition mode to quickly lock to a 1/(4T) sinusoid in the preamble field. After the phase and frequency of the preamble signal are acquired, the timing loop switches to a lower-bandwidth tracking mode. In both acquisition and tracking modes, the phase error is obtained from equalized sample values from the ADC using a decision-directed approach based on a digital implementation. To minimize acquisition time, a zero-phase start (ZPS) circuit reduces the range of initial phase error uncertainty in the VCO clock. The ZPS method is especially-suited for EPRML, since optimum sampling phase for the preamble pattern coincides with the prescribed sampling phase for an EPR4 signal, at the peaks and zero-crossings of the 1/(4T) sinusoid. Measured S/H output showing ZPS, acquisition, and tracking at 180MHz channel rate with a 1% frequency offset and no added noise is shown in Figure 3. The PW_{50}/T is 2.5, with a Lorentzian model.

The 40-level differential flash ADC quantizes the filtered analog signal and produces a 6b digital word to be used by the gain and timing control blocks and the Viterbi detector. The 3 high-order bits represent the closest noise-free sample in the EPR4 signal and the 3 low-order bits represent the error sample. The analog signal path is composed entirely of bipolar devices (Figure 4), and offset cancellation is not required in the pre-amp/comparator slice. Measured signal-to-noise-plus-distortion ratio (SNDR) vs. input frequency for the S/H and ADC is shown in Figure 5.

The detection of the equalized and sampled signal is by the soft-decision Viterbi algorithm, implementing the 8-state EPR4 trellis [1]. The detector consists of a branch metric unit (BMU), an add-compare-select unit (ACS), and a survivor memory based on register-exchange operations. The BMU and ACS are a custom 8b datapath with optimized placement to ensure high-speed operation and minimum wiring overhead. The other back-end processing blocks include a 2- or 3B frame synchronizer, and a decoder for a rate 16/17 code to reduce survivor memory requirements and limit error propagation.

In write mode, the frequency synthesizer generates a stable frequency determined by the divide-by M and N registers, to clock out the encoded data. The center frequency is programmable up to 200MHz with a 3:1 range and better than 1% resolution. The write pre-compensation range is 0 - 35% with 1% resolution.

In servo mode, the AGC time constant is independently set with a separate capacitor from that used in read mode, and the filter fc and boost are programmed independently of the read path settings. The filter output is applied (a) to a peak detector to determine the locations of signal peaks and to qualify the peaks, and (b) to an area integrator and customer-specific circuitry.

The IC in 0.56μm 2-layer-metal 10GHz BiCMOS operates over a user data rate range from 50 to 165Mb/s. Measured bit error rate (BER) vs. input SNR (before equalization) at 180MHz channel rate is within 1dB of ideal (Figure 6). Read-mode power is 1.3W at 180MHz and 5.0V. A chip micrograph is shown in Figure 7. The die is 5.25x5.25mm².

Acknowledgments:

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References:

[1] Thapar, H., A. Patel, "A class of partial response systems for increasing storage density in digital magnetic recording," IEEE Trans. on Magnetics, vol. 23, no. 5, pp. 3666-68, Sept., 1987.

[2] Cideciyan, R. D., et al., "A PRML system for digital magnetic recording," IEEE J. Select. Areas in Commun., vol.10, no.1, pp.38-56, Jan., 1992.

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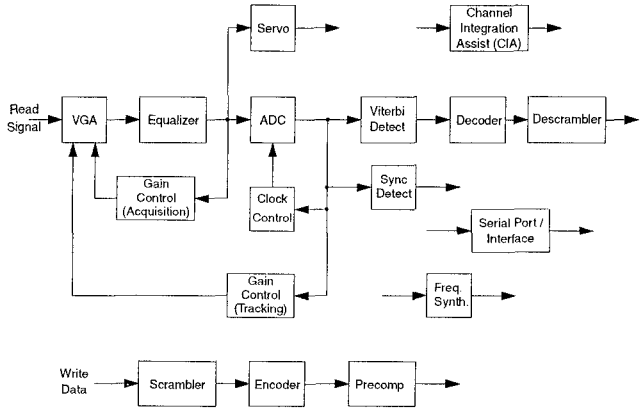

Figure 1: Chip block diagram.

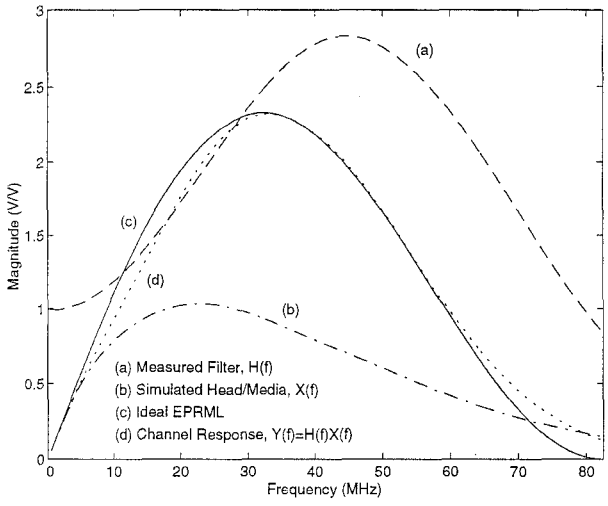

Figure 2: Measured filter response (fc=30MHz, boost=10.6dB).

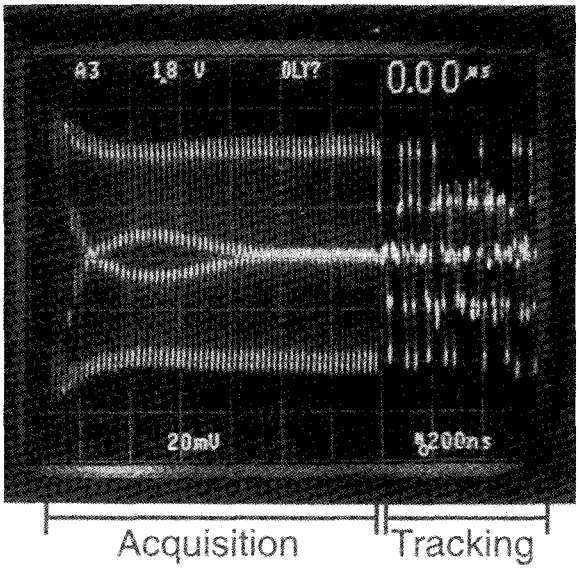

Figure 3: S/H output showing ZPS, acquisition (3 levels), and tracking (5 levels).

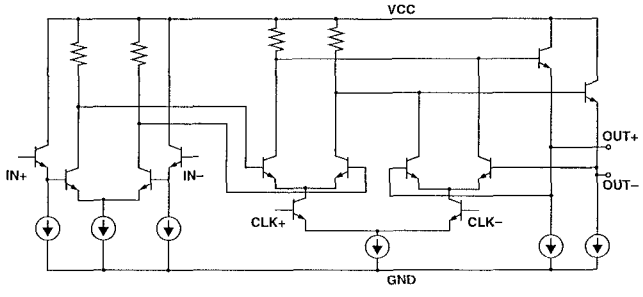

Figure 4: Simplified schematic of ADC pre-amp/latch cell.

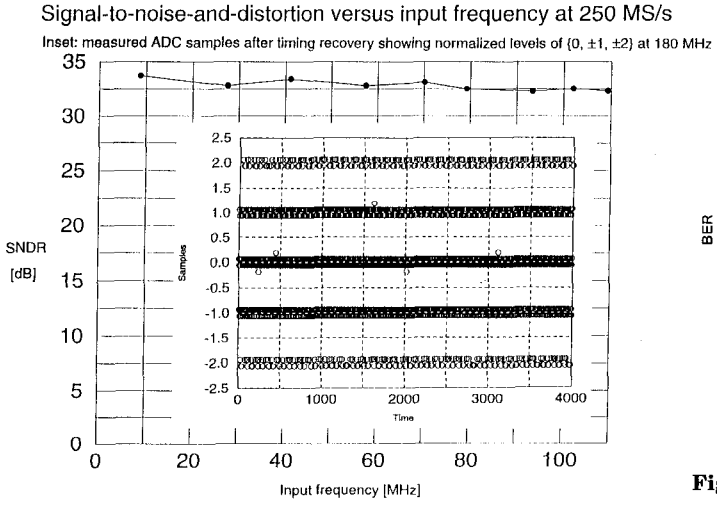

Figure 5: Measured ADC S/(N+D) vs. input frequency.

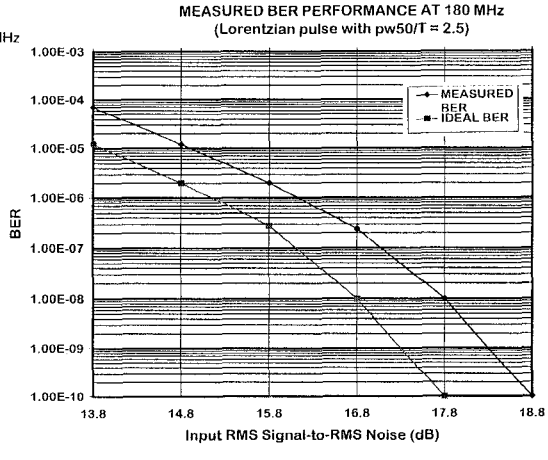

Figure 6: Plot of measured BER vs. SNR at 180MHz channel rate.

Figure 7: See page 479.

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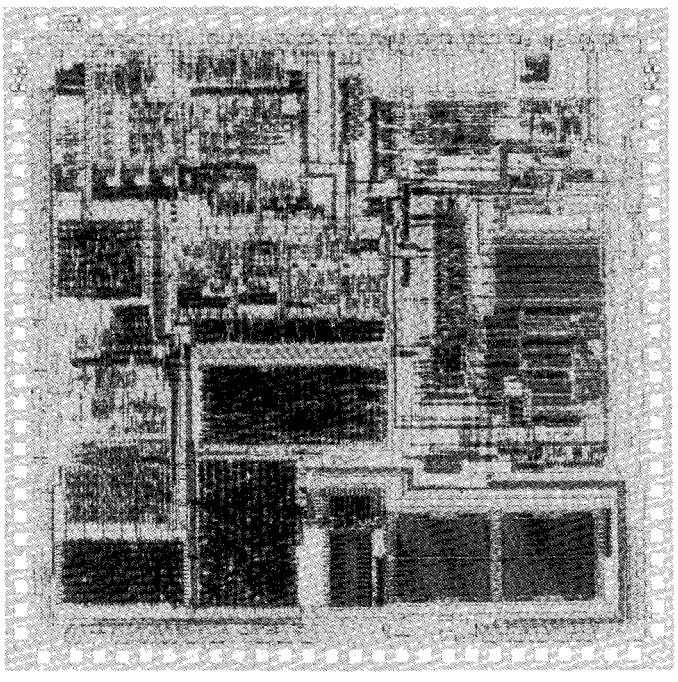

Figure 7: Die photo.

SA 19.5:A 160MHz Analog Equalizer for Magnetic Disk Read Channels

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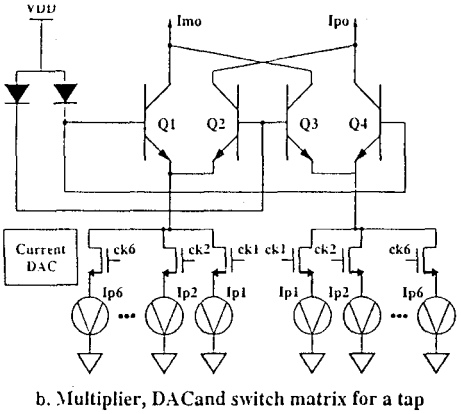
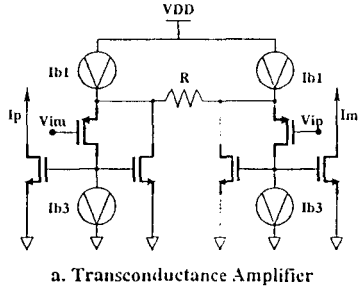
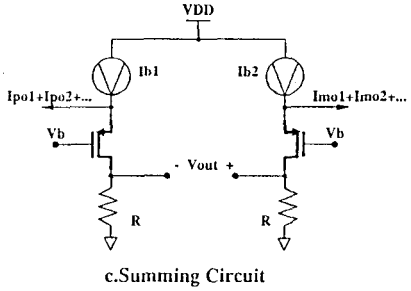


b. Multiplier, DACand switch matrix for a tap



a. Transconductance Amplifier



c.Summing Circuit

Figure 4: Signal shuffling circuits.