Impact of SOI, $Si_{1-x}Ge_xOI$ and GeOI substrates on CMOS compatible Tunnel FET performance

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Abstract

We report for the first time experimental investigations on SOI, $Si_{1-x}Ge_xOI$ & GeOI Tunnel FET (TFET). These devices were fabricated using a Fully Depleted SOI CMOS process flow with high k-metal gate stack, enabling 2 decades lower I_{OFF} (~30fA/µm) compared to co-processed CMOS. We successfully solve the TFET bipolar parasitic conduction by a novel TFET architecture, the Drift Tunnel FET (DTFET), with improved OFF state control. Concerning the ON current issue, we improve the SOI p (resp. n) TFET I_{ON} by a factor 55 (resp. 8) by source-drain profiles optimization (via spacers & extensions). Moreover, we demonstrate for the first time functional TFET & CMOS devices on $Si_{1-x}Ge_xOI$ (x=15-30-100%) co-integrated with the same SOI process flow, enabling TFET I_{ON} continuous improvement with Ge content increase: I_{ON} x2700 for GeOI (compared to SOI).

Introduction

Tunnel FET (TFET) operating as surface tunnel transistors have been proposed to solve many problems encountered in scaling down the conventional MOSFET, thereby turning the parasitic effect of tunnelling into an operating principle [1]. These devices have the potential for extremely low off current, and offer the possibility to lower the subthreshold swing beyond the 60 mV/dec limit of MOSFETs (at room temperature). The TFET device is a gated PiN diode (Fig. 1, Fig. 2), which presents significant differences compared to conventional MOSFET: *1)* The ON current is not limited by the transport but by the electron injection due to band to band tunneling (BtBt) [2]; *2)* A single TFET device can operate either in p or n channel mode, depending on the gate voltage value. The (few) number of TFET demonstration studies [3-6] have highlighted two major drawbacks of this device: *1)* the bipolar conduction (leading to parasitic conduction in the OFF state) and *2)* low ON currents [6]. In this experimental work, we address these two issues in order to determine the potentialities of TFET for Low Power Applications.

TFET, DTFET & CMOS Fabrication

We fabricated Tunnel FET devices using a Fully Depleted SOI CMOS compatible process flow (Fig. 1) starting from SOI (with t_{Si}=20nm) or $Si_{1-x}Ge_xOI$ wafers (x=15% or 30%). The second ones have been obtained by the "Ge enrichment technique" [7] with final 20nm SiGe layers [8]. The reduced band gap of the $Si_{1-x}Ge_x$ material enhances band to band tunneling leading to potentially higher ON currents [9]. The main characteristics of the process flow are described in Fig. 1: HfO_2 (3nm) & TiN (10nm) gate stack, with double epitaxially raised Si source-drain (further details of the SOI CMOS process can be found in [10]). The asymmetric N source & P drain (Fig. 1) were obtained by two successive lithography steps (P & N implantation masks) with TFET adapted layout. For the definition of the Drift TFET (DTFET) intrinsic area, a protection layer (SiN 50nm on SiO_2) was introduced (Fig. 3), in order to avoid an undesired silicidation of this area (length L_{IN}). In order to investigate the BtBt injection sensitivity with respect to dopant extension profile, different extension cases were studied (cf. split table in Fig. 4).

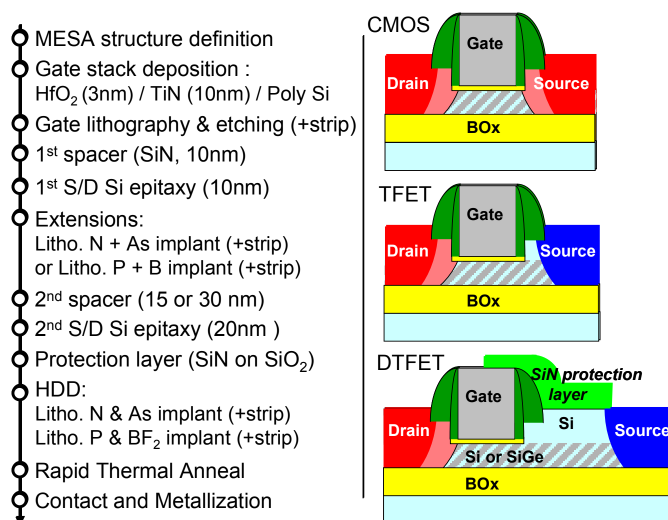


Fig. 1 : Summary of the CMOS process sequence used for the fabrication of the TFET (& DTFET) devices on SOI or $Si_{1-x}Ge_xOI$.

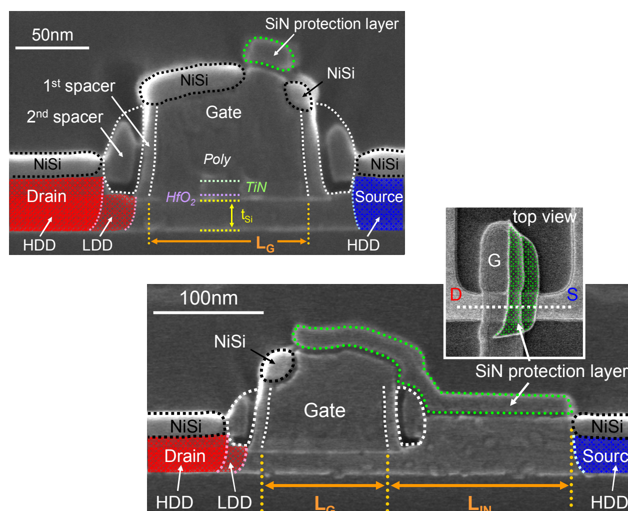
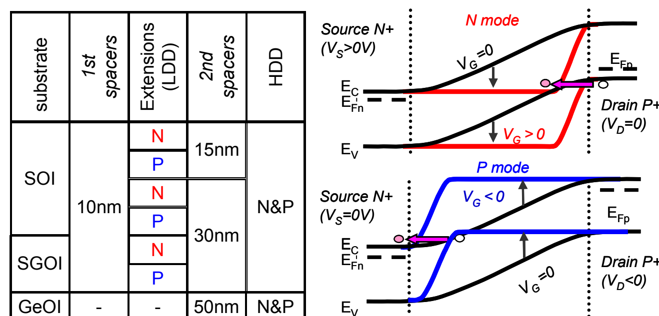


Fig. 2 (up) : SEM cross-section of a SOI TFET (L_G=100nm, t_{Si}=20nm, with nLDD and 30nm 2nd spacers).
Fig. 3 (down): SEM cross-section of a SOI Drift TFET (DTFET): L_G=100nm, L_{IN}=200nm, t_{Si}=20nm, with nLDD and 30nm 2nd spacers). (inset: TFET SEM top view with the protection layer).



substrate	1st spacers	Extensions (LDD)	2nd spacers	HDD
SOI	10nm	N	15nm	N&P
		P		
		N	30nm	
		P		
SGOI		N		
		P		
GeOI	-	-	50nm	N&P

Fig. 4 (left): Split table of the fabricated devices on SOI, SiGeOI and GeOI.
Fig. 5 (right): Band diagrams illustrating the electron Band to Band tunnelling in the n (up) and p (down) operation modes of the single TFET device.

Furthermore, MOSFET & TFET devices on Germanium-On-Insulator (GeOI) have been also fabricated for the very first

time (with the process described in [11] using HfO_2 & TiN, t_{Ge}=60nm), to investigate the 100% $Si_{1-x}Ge_x$ limit bandgap.

SOI TFET Operation in n & p Channel Modes

The TFET is intrinsically a bipolar device which can operate in n *and* p channel modes: Fig. 6 shows the $I_D(V_G)$ characteristics of a 100nm gate length SOI TFET for the two operation modes (Fig. 5). For the sake of simplicity, the source side always refers to the N+ doped side and the drain to the P+ doped side, independently of the considered operation mode. Thus, the required polarizations are V_{SD}>0 & V_{GD}>0 for the n mode and V_{DS}<0 & V_{GS}<0 for the p mode, because tunneling occurs at the drain junction in the n channel mode, whereas it happens at the source junction in the p channel mode.

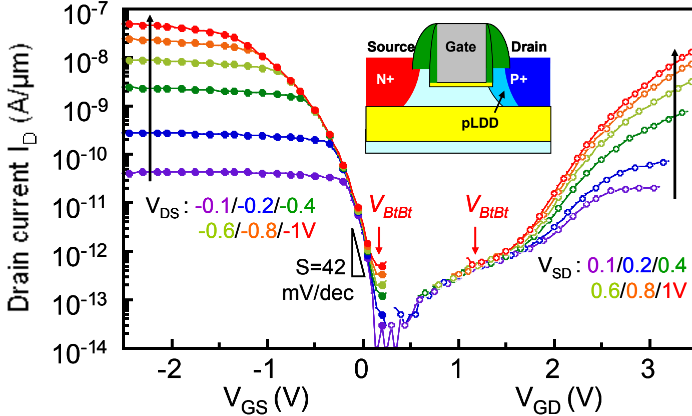


Fig. 6 : $I_D(V_G)$ characteristics of a L_G=100nm SOI TFET in p (left) and n (right) channel operation modes (t_{Si}=20nm; P30: pLDD, 30nm 2nd spacers). Local subthreshold slope at low as 42mV/dec is measured. We define V_{BtBt} as the voltage at which band to band tunneling occurs.

Note that local subthreshold slope values below 60mV/dec are obtained (42mV/dec at low V_{DS}). Fig. 7 shows the $I_D(V_{DS})$ of this device operating in the p channel mode. In agreement with theory [1-2], we obtained TFET I_{ON} current values independent of gate length (Fig. 8) (because I_{ON} is due to BtBT injection and is not limited by carrier transport). In CMOS circuits, L_G variation is one compound of the variability [12]. As the TFET ON current is insensitive to L_G, this kind of device may enable to reduce variability.

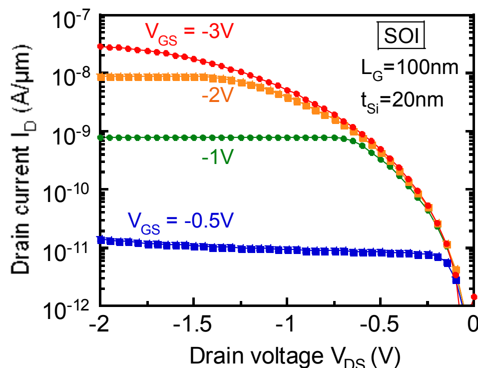


Fig. 7 : $I_D(V_{DS})$ characteristics of a L_G=100nm SOI TFET in p channel operation (t_{Si}=20nm; pLDD, 30nm 2nd spacers).

Moreover TFETs show very low I_{OFF} current values (~10-100fA/µm, cf. Fig. 6), as well as a small decrease when reducing L_G (Fig. 9). This is due to the fact that the OFF current of the TFET is a SRH generation current induced in the depleted area under the gate.

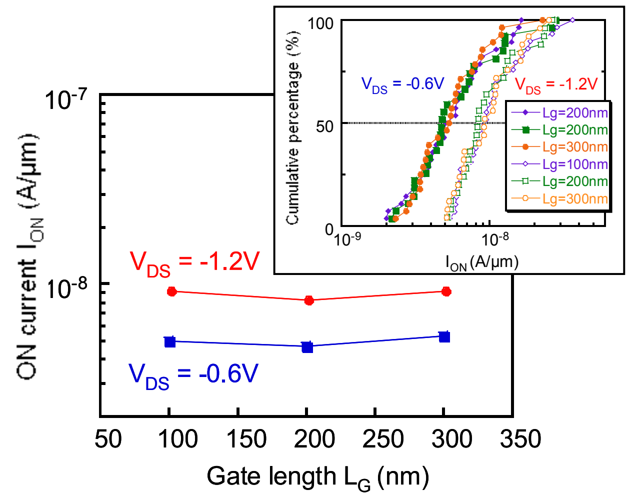


Fig. 8 : Impact of gate length on the ON current (at V_{GD}=-1.15V for two V_{DS} values) of SOI TFET in p channel operation (30nm spacers, pLDD). The values are extracted from the I_{ON} cumulative distributions at 50% (for the 3 gate lengths & 2 V_{DS}) shown in the inset. At a given V_{DS}, all the distributions are identical, with spread dispersion probably due to spacers length variation.

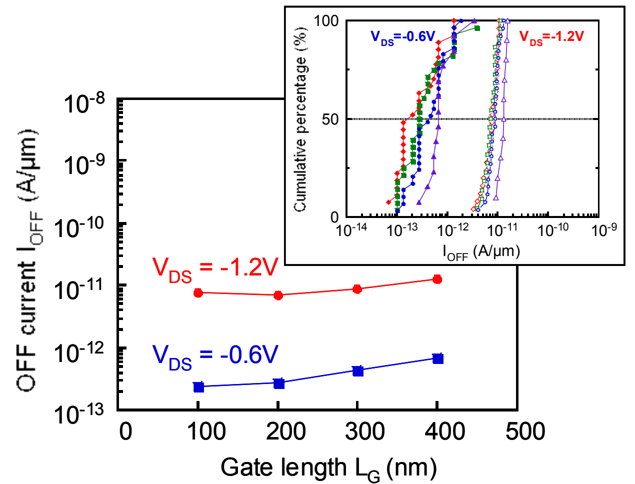


Fig. 9 : Impact of gate length on the OFF current (at V_{GD}=0V for two V_{DS} values) of SOI TFET in p channel operation (30nm spacers, pLDD). The values are extracted from the I_{OFF} cumulative distributions at 50% (for the 4 gate lengths & 2 V_{DS}) shown in the inset.

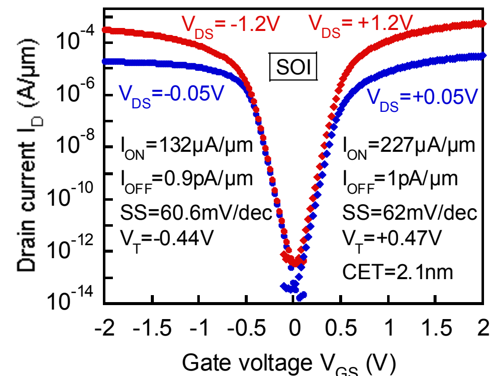


Fig. 10 : $I_D(V_{GS})$ characteristics of the SOI CMOS transistors (2nd 30nm spacers) co-integrated with the TFET & DTFET devices (L_G=350nm t_{Si}=20nm).

In order to compare the co-integrated SOI CMOS (Fig. 10) and TFET, we have extracted the I_{OFF} currents from 25 to 125°C of both transistors (Fig. 11): 30 times lower I_{OFF} values are obtained for TFET over the whole temperature range.

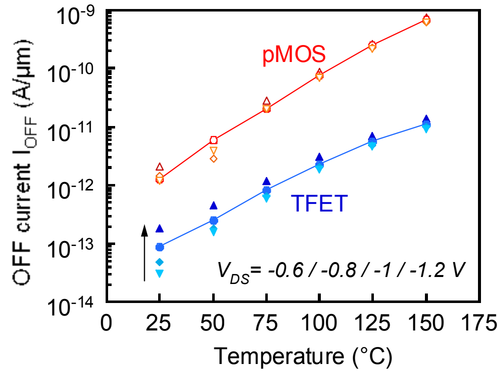


Fig. 11 : Impact of temperature on the OFF currents of co-integrated SOI pMOSFET & TFET (p mode; 30nm 2nd spacers, pLDD) with 350nm gate length.

Unlike the MOSFET, the TFET ON currents exhibit a positive variation with increasing temperature T (Fig. 12), as BtBt injection is thermally enhanced [6]. Moreover the I_{ON} gain with T (Fig. 12) increases for small V_{DD} (+250% at V_{DD}=-0.6V), which is an advantage for LOP applications.

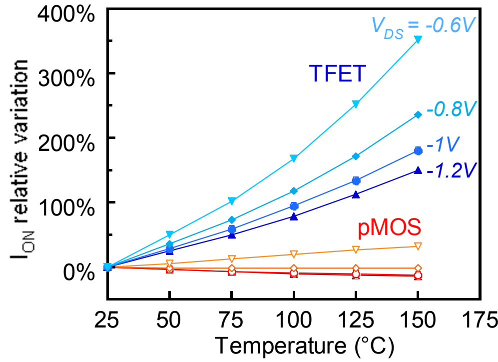


Fig. 12 : Impact of temperature on the ON currents variation of co-integrated SOI pMOSFET & TFET (p channel operation; 30nm 2nd spacers, pLDD)..

Drift Tunnel FET

One major drawback of the TFET comes from its bipolar parasitic conduction: for V_G<0 as well as for V_G>0. As predicted by simulation [2], the introduction of an intrinsic area (length L_{IN}) at the source side (Fig. 3) disables the parasitic conduction. This new device, called here Drift FET (DTFET), can be seen as an I-MOS transistor [13] operating in a tunneling mode. Fig. 13 shows the $I_D(V_G)$ curves of TFET & DTFET (with same L_G).

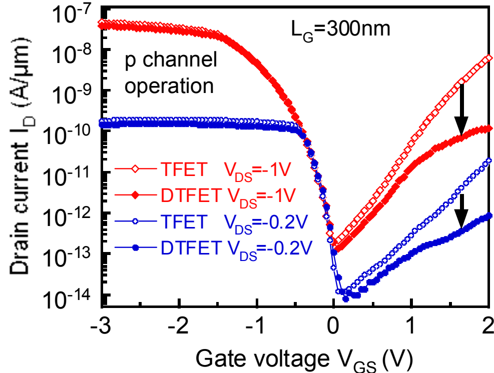


Fig. 13 : Interest of the DTFET (SOI L_G=300nm, L_{IN}=200nm here) for the bipolarity reduction: The current in the OFF state (at low and high V_{DS}) is reduced compared to the TFET (SOI L_G=300nm).

By introducing an 200nm intrinsic area, the electrical field located at the source side of the gate is decreased, leading to a reduced bipolarity (by a factor ~10). The impact of the additional intrinsic length on the device surface can be minimized by performing an L-shaped intrinsic area [14]. As predicted [2], TFET & DTFET demonstrate identical ON current values (Fig. 14), as long as the serial resistance of the intrinsic area remains negligible compared to the equivalent tunnel resistance. In our case, the current remains identical even when increasing the DTFET L_{IN} up to 300nm. Thus the intrinsic length of the DTFET does not introduce an additional component in variability compared to TFET.

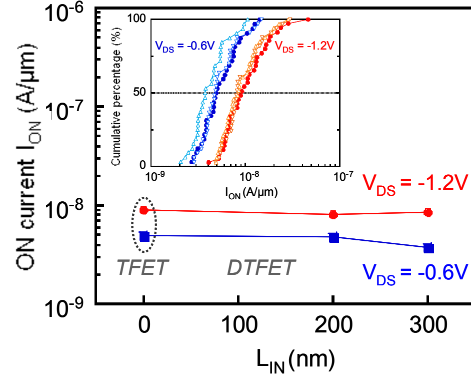


Fig. 14 : ON current comparison between SOI TFET & DTFET (in p mode). Impact of intrinsic area length on the extracted I_{ON} (at V_{GD}=+1.15V for 2 V_{DS} values). The inset shows the I_{ON} cumulative distributions.

Improved I_{ON} through Junction Optimization

As shown by TCAD simulations [1-13]-[15], the key parameter for TFET operation is the source and drain architecture (Fig. 5): N+/channel for p mode and P+/channel for n mode operation. The different extensions configurations of the fabricated SOI TFETs (Fig. 4) highlights this sensitivity as shown by $I_D(V_{Gx}-V_{BtBt})$ curves in Fig. 15. V_{BtBt} is defined as the voltage at which band to band tunneling occurs.

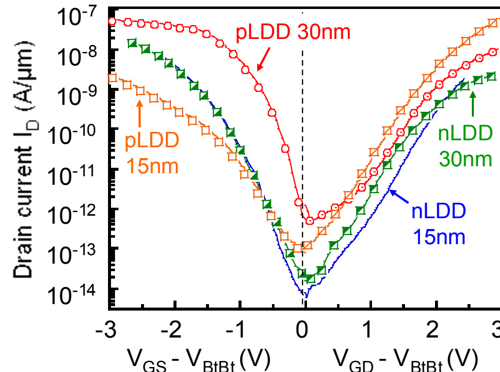


Fig. 15 : $I_D(V_G)$ characteristics (in p & n modes) at V_{Ds}=±0.8V of 100nm gate length SOI TFETs with various LDD (n/p & 2nd spacers lengths (15/30nm) configurations.

The experimental results reported in Fig. 16 show that N (resp. P) extensions determine the I_{ON} value in the p (resp. n) mode (whatever the spacer length is).

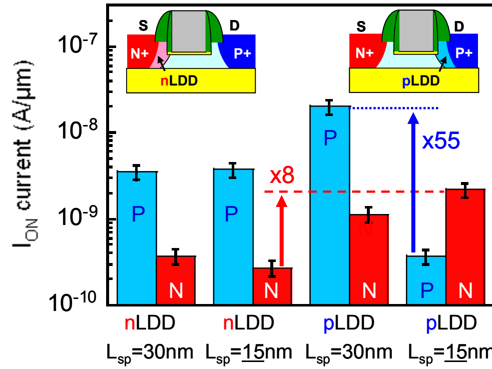


Fig. 16 : Extracted TFET ON current values (at V_{DS}= ±0.8V, V_{GS}=±3V, in p & n modes) for 100nm gate length SOI TFETs with various LDD (n/p) & 2nd spacers lengths (15/30nm) configurations.

Moreover, it appears that P extensions lead to increased N mode I_{ON} (compared to the N extensions TFET). One reason is probably the fact that the boron doped source is closer to the gate with P extensions. Moreover the increase of the 2nd spacers size to 30nm allows to increase the p I_{ON} x55 (Fig. 16).

Improved CMOS & TFET I_{ON} with SiGeOI & GeOI

The low tunneling TFET ON current can be enhanced by either optimized junctions or small band gap materials [1]. We report here on the first successful integration of TFETs on $Si_{1-x}Ge_xOI$ (x=15&30%), with the SOI process flow (without salicidation) described in Fig. 1. Moreover, the co-integrated CMOS transistors are functional (Fig. 17) and present improved hole mobility (+26%, Fig. 18), and larger I_{ON} (+44% for long channel) compared to SOI, in good agreement with pseudoMOS mobility values [16].

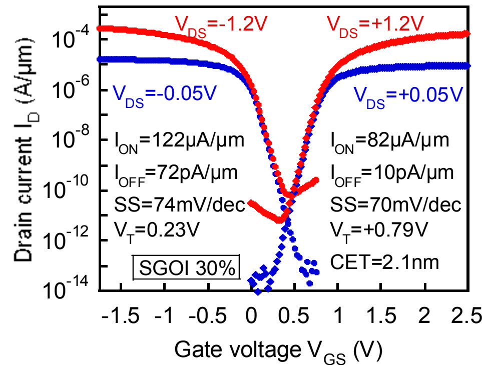


Fig. 17 : $I_D(V_{GS})$ characteristics of the SGOI 30% CMOS transistors (with extensions n, 15nm 2nd spacers) co-integrated with the TFET & DTFET devices (L_G=350nm, t_{Si}=20nm).

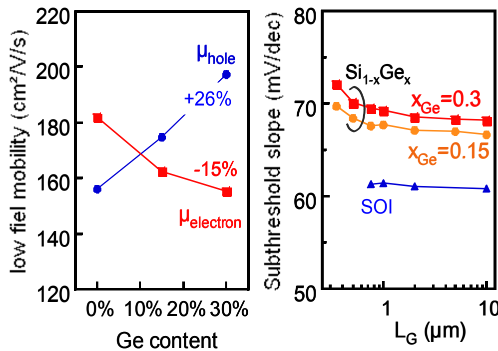


Fig. 18 : (left) SGOI CMOS low field mobility as function of the Ge content. (right) pMOSFET subthreshold slope as a function of gate length L_G for SOI & SGOI. Similar trends & values have been obtained for nMOS.

Fig. 19 shows $I_D(V_{Gx}-V_{BtBt})$ characteristics of 400nm gate length TFETs on $Si_{1-x}Ge_xOI$ (x=0-15-30%, t_{SiGe}=20nm), and GeOI (t_{Ge}=60nm) substrates.

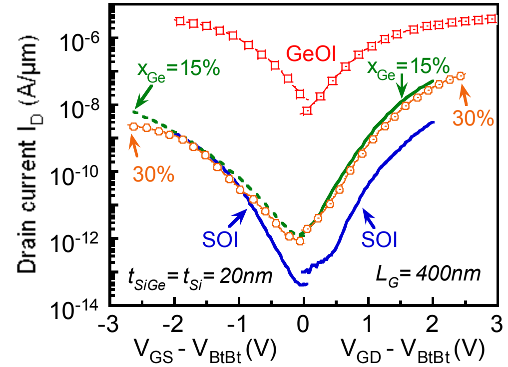


Fig. 19 : $I_D(V_G)$ characteristics (at V_{DS}=±0.8V) of 400nm gate length TFETs on $Si_{1-x}Ge_xOI$ (x=0-15-30%, t_{SiGe}= 20nm), and GeOI (T_{Ge}= 60nm) substrates.

Increasing the Ge content enables to boost the p & n TFET I_{ON}, as shown in Fig. 20: x335 (n) and x2700 (p). As shown in the previous paragraphs for SOI TFET, further OFF and ON currents improvements for SGOI TFETs are expected from junction optimizations.

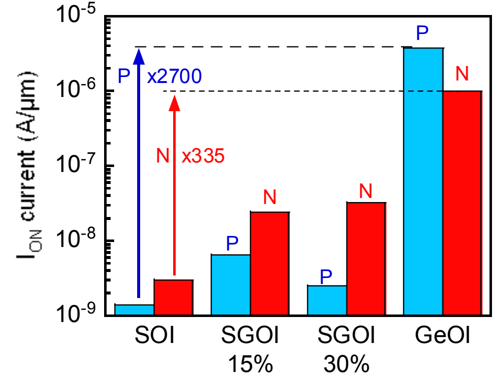


Fig. 20 : Extracted TFET ON current (at V_{DS}= ±0.8V, V_{GS}= ±2V) for 400nm gate length TFETs on $Si_{1-x}Ge_xOI$ (x_{Ge}= 0-15-30%, t_{SiGe}=20nm), and GeOI (T_{Ge}=60nm) substrates (in p & n modes).

Conclusion

We successfully demonstrated TFET devices with High K-Metal gate stack on SOI, and also for the first time on $Si_{1-x}Ge_xOI$ (0-15%-30%) and GeOI wafers. The TFET devices were fabricated using a Fully Depleted SOI CMOS process flow. The TFET show 2 decades lower I_{OFF} (~30fA/µm) compared to co-processed CMOS over a wide temperature range (25°C to 150°C). Furthermore, the I_{ON} is independent of L_G, which may improve the variability compared to the MOSFET technology. We introduce the DTFET architecture allowing the reduction of the usual TFET bipolar parasitic currents thanks to an intrinsic area between source and gate without sacrificing the ON current. Furthermore, the high sensitivity of the TFET towards the junction properties has been highlighted through source-drain profiles optimization (via spacers & extensions), leading to an x55 I_{ON}. Moreover, we explore the introduction of small band gap materials ($Si_{1-x}Ge_xOI$ with x_{Ge}: 15-30-100%) with the same SOI process flow, enabling TFET I_{ON} continuous improvement (compared to SOI) with Ge content increase: I_{ON} x2700 for GeOI.

Acknowledgement

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