An Accurate FinFET's Vmin Estimation Method for Extreme Low Operation Voltage Design

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***Abstract*—** In this paper, the minimum operating voltage (Vmin) estimation methodology for advanced FinFET technology is newly proposed with a manufacturability consideration. The experiment depicts that key factors to determine Vmin are the sum of threshold voltages of n-FET/p-FET, beta-ratio (n/p-FET strength ratio), and random variation. The new equation successfully captures the key electrical features, which is verified by both Monte-Carlo simulation and advanced 11nm/8nm FinFET experimental data. Based on the new model, the paper also provides the guideline for threshold voltage and local mismatch strategy for future advanced FinFET Vmin improvement.

I. Introduction

A new era of high performance computing (HPC) with big data, driven by the proliferation of the internet of things (IoT) and deep learning, demands both high performance and the utmost energy efficiency. The substantial increasing energy consumption has been considered as the most crucial constraint that hinders further steps in HPC system development. The most promising solution for reducing power consumption is scaling down the supply voltage (Vdd) [1]. The Vdd reduction, however, could severely cause functional fail on CMOS logic circuits without a careful technology assessment, as well as a circuit consideration. To design the technology for the extreme low voltage operation, the estimation of the minimum operating voltage (Vmin) is intensely essential. There have been many investigations and modeling for planar-FET [2-3]. However, for Advanced FinFET, although Si demonstration was shown [4], there is no Vmin estimation model yet.

In this paper, key transistor parameters impacting on Vmin were discussed using advanced sub-10nm CMOS process including SPICE and STD-Cell libraries. On the basis of the analysis, we propose the accurate expression for Vmin estimation as a figure of merit for CMOS technology, which is useful for transistor design guide suitable for low power application in early stage of technology development.

II. Vmin Impact of Device Parameters

Fig. 1 shows the logic gate delay and switching energy versus the supply voltage for advanced FinFET technology. Based on CMOS Inverter (INV), even though the energy optimum supply voltage (Vopt) shows a sweet spot in lower Vdd region, the actual technology Vmin is 200mV higher due to the logic circuit functional fail. The Vmin deviation from Vopt is an obstacle to overcome, which has strong connection with process parameters, such as global/local variability, and n-/p-FET balance.

The relative Vmin sensitivity with respect to key process parameters for INV and D Flip-Flop (DFF) is shown in Fig. 2. The basic functionality of INV is strongly influenced by drivability of transistors and a balance between n-/p-FET's strength, whereas the most critical factor for the dependency on Vmin of DFF is local Vth variation (Vtmm). The FF can be considered as a synchronous system which consists of cross-coupled inverters (latch), master and slave latches, and data propagation and clock paths. Because of the FF feature, the random variability component causes a functional failure in FFs. Overall, Vtmm plays a key role in the entire system. On the other hand, some performance boosting knobs induce a tradeoff to Vtmm due to short cannel effect control margin etc. (Fig.3). As a result, Vmin estimation methodology to define the technology scheme to give a guideline becomes critical.

III. Modeling and Experimental Result

A. Vmin modeling

In early stage of design and technology developments, estimating accurate Vmin can be a powerful guide for path-finding. Vmin estimating equation has already been reported by Fuketa et al [2]. However, there are some limitations on applying this to nano-scale devices and capturing entire technology, because of negligent in global variability and Vth absolute value. In this paper, we propose the effective formula for estimating Vmin based on process parameters as follows:

$$V_{min} = \frac{Vt_{sum} + \sigma_{glob}}{\sqrt{2}} + \frac{2\sigma_{mm}}{3H}\sqrt{\frac{\pi \ln(N/2)}{2}} + \frac{C + |B|}{H}, \quad (1)$$

where,

$$\sigma_{glob} = \sqrt{(\sigma Vtglob_n^2 + \sigma Vtglob_p^2)}, \sigma_{mm} = \sqrt{\sigma Vtmm_n^2 + \sigma Vtmm_p^2},$$
$$Vt_{sum} = Vth.n + Vth.p,$$
$$H = 1 + \lambda, \lambda = \Delta Vt/\Delta Vds,$$
$$B = \frac{n}{4}\phi_t \ln(\beta_p/\beta_n), C = 20 \cdot n\phi_t \ln[1 - (2/n)],$$
$$n = SS/60, SS = \Delta Vgs/\Delta Id,$$
$$\sigma Vtglob \quad 3\sigma \text{ tolerance for global variation},$$
$$\sigma Vtmm \quad 3\sigma \text{ tolerance for local variation},$$
$$\phi_t \quad \text{thermal voltage}.$$

β corresponds to the strength of transistor and the *I-V* characteristics of a transistor in sub-threshold regions is given by [2]

$$I_d = \beta \cdot e^{\frac{Vgs + \lambda \cdot Vds}{n\phi t}} \left(1 - e^{\frac{Vds}{\phi t}} \right), \quad (2)$$

$$\beta = I_0 \frac{W}{L} \cdot e^{-\frac{VT}{n\phi t}}, \quad (3)$$

where I_0 is the mobility-dependent parameter. This strength parameter can be derived using the critical threshold voltage current (*IVT*) in constant current extraction method and leakage source current I_{soff} as follows

$$\beta = \frac{IVT \cdot W/L - I_{soff}}{e^{(\lambda Vdd)/(n\phi t)} \left(e^{Vtsat/(n\phi t)} - 1 \right)}. \quad (4)$$

To capture the dependency of Vth and global variability, the proposed expression has been improved. As shown in Fig. 4, the proposed equation shows a good agreement with Mont-Carlo simulation for 3 key electrical parameters, compared to the previous model [2]. In particular, n-/p-FET strength dependence improvement contributes a key role, as shown in Fig. 4(d). The previous methodology [2] focuses only on n-/p-FET strength ratio in Fig.5, rather than the absolute n-/p-FET strength value, which cannot fully describe the Vmin characteristic with Vth lowering of the superior n-FET or p-FET (Fig.4 (a/d)). As shown in Fig. 6, Vmin has a strong correlation with the sum of Vth for n-/p-FETs, as well as with n-/p-FET drive strength. These two characteristics have been implemented in the proposed equation.

Another key concern is the manufacturability for extreme low Vdd circuit with the global variation, which is also incorporated in the new equation. The dependence of Vmin on global variation is shown in Fig 7. Vmin is directly proportional to the root-sum-squared global tolerance.

B. Experimental data and Vmin design guideline

Monte-Carlo simulation has been performed on INV RO with different number of stages from 11-stages to 101-stages in advanced sub-10nm CMOS process SPICE and STD-Cell libraries. Fig. 8 compares simulation result and Vmin by the new model for different RO stages. The calculated Vmin of INV RO for (a) various n-/p-FET balances and (b) global variation tolerances agrees very well with the Monte-Carlo simulation. For Si experimental data verification, the INV RO with 101 stages were compared using 11nm [5] and 8nm [6] logic technologies. Vmin was extracted from the measured RO frequency using a linear regression analysis as shown in Fig. 9. The measured Vmins for various n-/p-FET balances is shown in Fig. 10. The Vmin contour plot indicates that sum of threshold voltages of n-/p-FET is dominant over the skew of n-/p-FET's drive strength. Fig. 11 shows the comparison of Vmin between Si measurement and calculation using proposed and previous models. Vmin calculated using the new proposed expression is well matched with Si experimental results, which proves that the proposed equation is widely applicable to various technologies and n-/p-FET balances.

Lastly, Fig.12 provides Tr. design guideline for extreme low Vdd operation to set Vth position and AVT value with a target Vmin reduction (ΔVmin). As shown in Fig.12, Vth -20mV is equivalent to AVT -0.1 to obtain the same Vmin reduction. This indicates that AVT reduction is crucial for the future technology to improve the energy optimum supply voltage (Vopt), which is determined by the balance of leakage energy and dynamic energy. In this reason, we also investigated AVT improvement with FinFET process using 3D TCAD simulator as shown in Fig.13. At the fixed performance, an impurity profile and structure optimization can bring down local Vth mismatch value for both n-/p-FET successfully, which can contribute to 40~60mV Vmin reduction for logic circuits. Local mismatch driven Tr design is one of key considerations for the future HPC era.

IV. CONCLUSION

We have presented the investigation on the minimum operating voltage (Vmin) versus key process parameters using advanced sub-10nm CMOS process, showing that the significant contributors to Vmin are the sum of Vth for n-/p-FETs and random variability in respect of INV and FF, respectively. Based on the result, new Vmin estimation model has been proposed, which accurately predicts Vmin of logic CMOS circuit. The new equation has been verified through Monte-Carlo simulation and measurements for various n-/p-FET balances and different technology nodes.

REFERENCES

[1] V. De. S. Vangal, and R. Krishnamurthy, "Near-Threshold Voltage (NTV) Computing," IEEE Design and Test Nature, vol. 34, pp. 24–30, 2017

[2] H. Fuketa, S. Iida, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "A closed-form Expression for Estimating Minimum Operating Voltage (VDDmin) of CMOS Logic Gates," in *Proc. Design Automation Conference (DAC)*, pp. 984-989, 2011

[3] T. Yasufuku, S. Iida, H. Fuketa, K. Hirairi, M. Nomura, M. Takamiya, and T. Sakurai, "Investigation of Determinant Factors of Minimum Operation Voltage of Logic Gates in 65-nm CMOS," in *Proc. International Symposium on Low Power Electronics and Design (IDLPED)*, pp. 22-26, 2011

[4] F. Crupi, M. Alioto, J. Franco, P. Magnone, M. Togo, N. Horiguchi, and G. Groeseneken, "Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements," *IEEE Transactions on Circuits and Systems, II: Express Briefs,* Vol. 59, No. 7, pp. 439-442, 2012

[5] H.J. Kim, B.H. Choi, Y.H. Lee, J.H. Ahn, Y.S. Bang, Y.D. Lim, J.H. Do, J.H. Jung, T.J. Song, Y. Yasuda-Masuoka, K.C. Park, S.D. Kwon, and J.S. Yoon, "Highly Manufacturable Low Power and High Performance s11LPP Platform Technology for Mobile and GPU Applications," *2018 Symposium on VLSI Technology*, pp. 213 - 214, June, 2018

[6] H.S. Rhee, I.R. Kim, J.H. Jeong, N.K. Son, H.B. Hong, S.I. Cho, Y.M. Park, D.W. Kim, Y.K. Choi, J.H. Ahn, S.G. Kang, K.H. Yeo, J.T. Kim, E.C. Lee, J.M. Youn, and J.S. Yoon, "8LPP Logic Platform Technology for Cost-Effective High Volume Manufacturing," 2018 Symposium on VLSI Technology, pp. 217 - 218, June, 2018

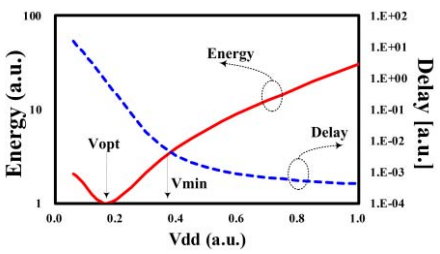


Fig. 1. Switching Energy and delay versus supply voltage Vdd for advanced FinFET CMOS logic circuit (Inverter, FO4).

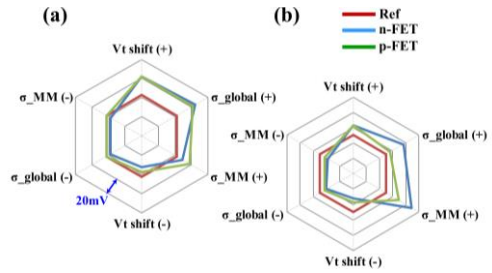


Fig. 2. Vmin sensitivity radar chart of key electrical parameters (ΔVth =25mV): (a) Inverter and (b) D-FlipFlop.

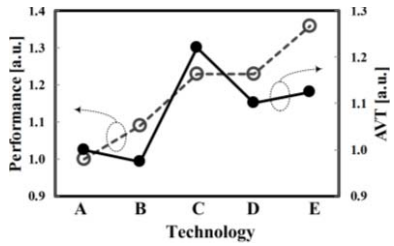
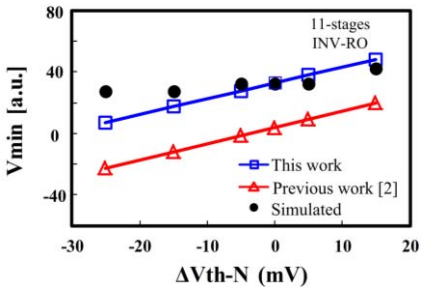
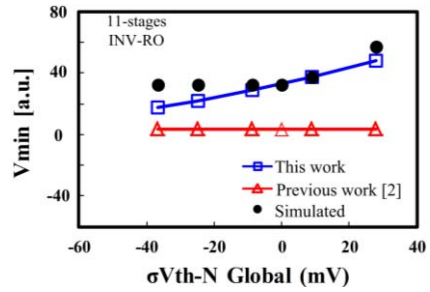


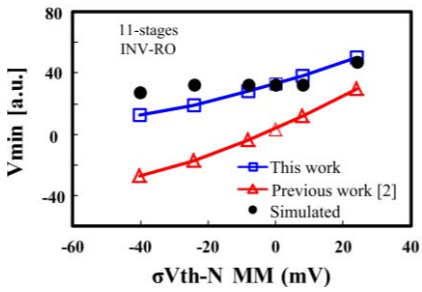
Fig. 3. Tr. AC performance and Vth mismatch (AVT) dependence with various processes conditions.



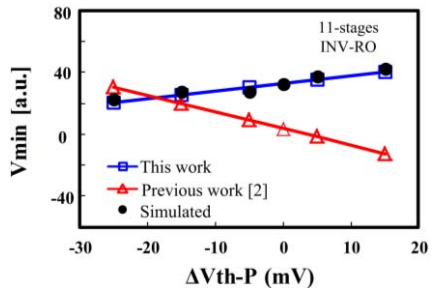
(a) n-FET: Vmin dependence on Vth shift (ΔVth-N).



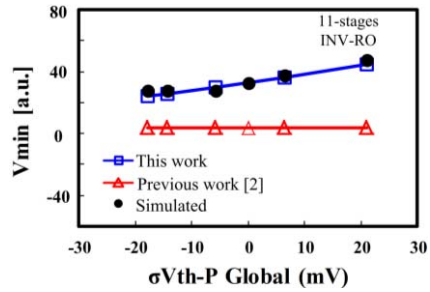
(b) n-FET: Vmin dependence on global variation (σVth-N Global).



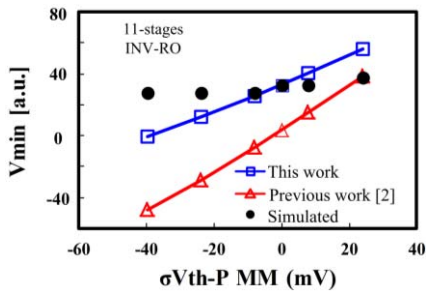
(c) n-FET: Vmin dependence on local variation (σVth-N MM).



(d) p-FET: Vmin dependence on Vth shift (ΔVth-N).



(e) p-FET: Vmin dependence on global variation (σVth-P Global).



(f) p-FET: Vmin dependence on local variation (σVth-P MM).

Fig. 4. Vmin dependence on each n-/p-FET's key electrical parameters, compared to SPICE simulation, previous expression [2] and newly proposed model.

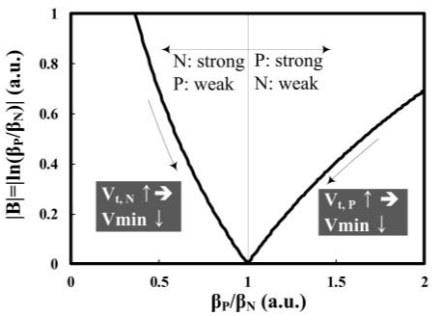


Fig. 5. |B| versus n-/p-FETs strength

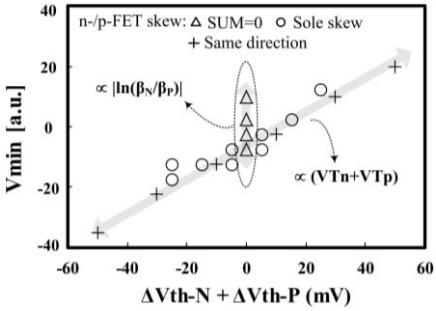


Fig. 6. Vmin dependence on summation of n/p-FET Vth shift (ΔVth-n + ΔVth-p)

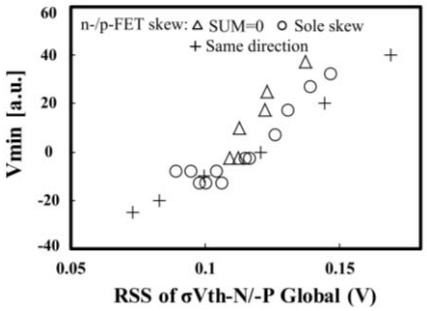


Fig. 7. Vmin dependence on RSS of n-/p-FET Vth global variation (σVth-n/-p global)

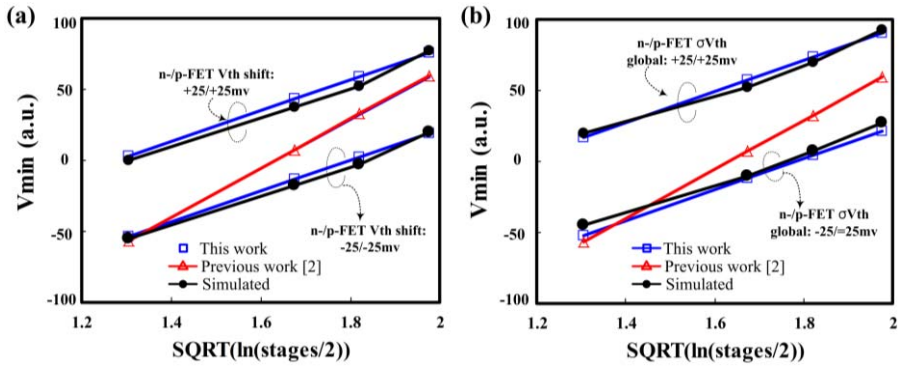


Fig. 8. Vmin of Inverter R.O. for various (a) Vth shifts and (b) global variation, compared to SPICE simulation, previous expression [2] and newly proposed model.

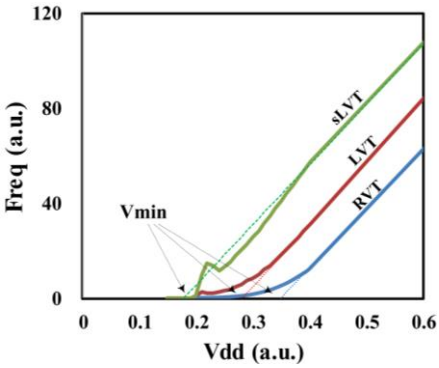
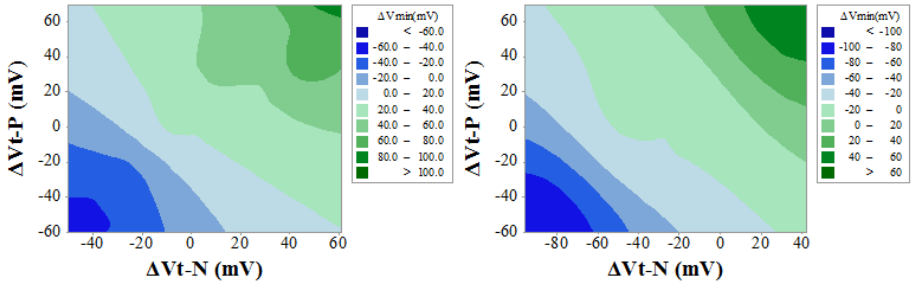


Fig. 9. Vmin extraction from experimental measurement data.



(a) 11nm FinFET Technology node [5] (b) 8nm FinFET Technology node [6]

Fig. 10. Experimental Vmin data with various Vth position in different advanced 11/8nm FinFET Technology nodes [5-6].

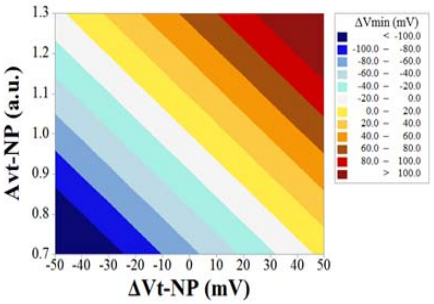
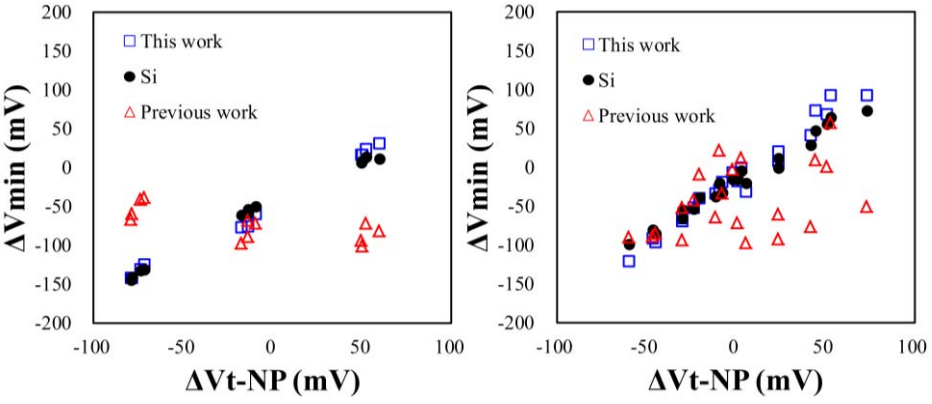


Fig. 12. Vmin dependence on Vth and random variation (proposed equation)



(a) 11nm Technology node [5] (b) 8nm Technology node [6]

Fig. 11. Vmin estimation comparison between Si experimental data and newly

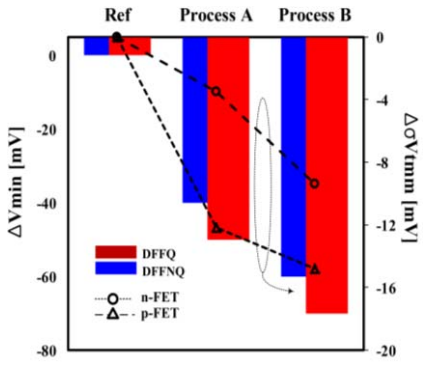


Fig. 13. Vmin and local mismatch value with various Fin process improvement.