8.4 A 0.7W Fully Integrated 42GHz Power Amplifier with 10% PAE in 0.13μm SiGe BiCMOS

Wei Tai[1], L.Richard Carley[1], David S. Ricketts[2]

[1]Carnegie Mellon University, Pittsburgh, PA,
[2]North Carolina State University, Raleigh, NC

In this paper, we report a fully integrated power amplifier (PA) architecture that combines the power of 16 on-chip PAs using a 16-way zero-degree combiner to achieve an output power of 0.7W with a power-added efficiency (PAE) of 10% at 42GHz and a -3dB bandwidth of 9GHz. This is 2.6 times more output power than a recently reported millimeter-Wave (mm-Wave) silicon-based PA [1]. The circuit is a fully integrated mm-Wave PA achieving a leading output power approaching 1 Watt in a silicon process.

To date only a few published mm-Wave PAs in silicon have achieved a saturated output power of more than 20dBm (100mW) [2-6]. The difficulty in achieving high output powers at mm-Wave frequencies lies in the limited output power of a single PA, which is constrained by maximum current density, breakdown voltage and parasitics of the technology. Moreover, to obtain maximum power from a single PA, its output impedance must be lowered due to the relative low breakdown voltage of silicon devices. In fully integrated designs, this low impedance must then be impedance transformed to the desired output impedance through a lossy on-chip impedance transformer, reducing the overall net output power.

Power combining multiple PAs is a common approach to obtaining larger output powers. As more unit PAs are combined, the required impedance transformation ratio as well as voltage and thermal stress on each unit PA is relaxed. However, the insertion loss of traditional power combiners, e.g. Wilkinson combiners [3] and transformer-based combiners [4,5], tends to scale up as the number of combined PAs increases due to increased size and complexity of the combiners. Part of the additional size and complexity stems from maintaining port-to-port isolation in the combiner, particularly with Wilkinson combiners. If we assume, however, that all combiner inputs have zero-degree phase difference (i.e. in-phase), port isolation is no longer a major constraint. In this case, the requirement for exact quarter-wavelength segments in the Wilkinson combiner is removed and arbitrary line lengths can be used subject only to layout constraints and impedance transformation requirements. It is then possible to significantly reduce the combiner size and insertion loss while simultaneously achieving the desired impedance transformation. In this work, we combine the power of 16 PAs using a 16-way zero-degree combiner that achieves low insertion loss and wideband impedance transformation.

The combiner is developed using scalable SPICE transmission line models derived from EM field simulations. The simulated insertion loss of the combiner is less than 0.5dB at 45GHz. It also performs the required impedance transformation and presents the optimum load impedance to each unit PA, whose value was obtained from load-pull simulations of the unit PA output stage. Since a dedicated impedance transformation network is no longer needed, the associated power loss is avoided. We improve the isolation between input ports to better than 10dB by inserting a small resistor between each pair of adjacent ports. This level of isolation is sufficient for maintaining PA stability under amplitude and phase mismatch caused by process variation. The size of the power combiner is 1.53×0.7 mm^2.

Using this combiner, a fully integrated power amplifier was designed in a 0.13μm SiGe BiCMOS technology. Figure 8.4.1 shows the block diagram of the PA and it also illustrates the layout placement of the power combiner, unit PAs, and the 2 input power dividers. By orienting the 16 unit PAs into 2 columns of 8 PAs facing the center, the area and insertion loss of the power combiner can be minimized. The PA is also configured so that the two columns of unit PAs can receive different input signal phases, allowing the outphasing technique to be employed for output power back-off. The unit PA design is similar to that reported in [7]. As shown schematically in Fig. 8.4.2, each unit PA consists of two cascode driver stages followed by a common-emitter output stage. SiGe HBT devices with 200GHz cutoff frequency (f_t) are used. To maximize gain and output power, all of the devices are laid out in a C-B-E-B-C configuration and biased near a peak-f_t current density. A "tapered" metal stack profile is used in the transistor fingers to reduce side-wall parasitic capacitances between terminals without sacrificing the current-handling capability. To ensure that the PA is unconditionally stable, small resistors are added serially to the base bias feeds to suppress potential resonances. The output stage of the PA operates at a 2.4V supply, whereas the two cascode driver stages use a 4V supply. The transistors operate safely under these supply voltages due to a low base bias impedance of approximately 300Ω [5,7]. A total of 91pF of decoupling capacitance per unit PA is spread across the supply feed lines to minimize trace inductance and further improve PA stability. L-C-based inter-stage matching is used, which consists of metal-insulator-metal capacitors and T-line inductors. The T-line inductors allow a compact unit PA layout, and their quality factor exceeds 20 at 45GHz. Spiral inductors with patterned ground shields are used as RF choke inductors in the bias feeds. The power divider and combiner are both designed using a conductor-backed coplanar waveguide structure (Fig. 8.4.2). All of the inductors and transmission lines are implemented on the 4μm thick top aluminum layer to achieve high quality factor.

The PA was tested on a probe station with coaxial RF probes and a pair of 12-needle DC probes for supply and bias. Figure 8.4.3 shows the small-signal performance of the PA. The measured peak gain (S_{21}) is 18.5dB and centered at 43GHz, which is slightly shifted in frequency from simulation most likely due to inaccuracies in parasitics extraction. Input return loss ($|S_{11}|$) is better than 10dB from 42.5 to 49GHz. The measured stability factor k is greater than 1 across the entire frequency range, indicating unconditional stability. The large signal performance of the PA was measured using 2 frequency quadruplers followed by highpass filters as signal sources. Power losses of all external components were de-embedded across the measurement frequency band, and the output power of the PA was measured with a power meter. Figure 8.4.4(a) shows the large signal characteristics of the PA at 42GHz versus the output stage supply voltage while the driver stage supply voltage remains at 4V. At 2.4V, a saturated output power of 28.4dBm (0.7W) is achieved with 10% PAE. Although output power increased to 28.7dBm with a 2.7V supply, it degraded slightly over time, which could indicate over-stress on the HBT devices. No such degradation was observed with a 2.4V supply. A large-signal frequency sweep is shown in Fig. 8.4.4(b). The output power -3dB bandwidth of the PA is greater than 9GHz, which corresponds to a 21% fractional bandwidth.

The saturated output power of the proposed PA is compared with recently reported mm-Wave PAs in silicon-based processes, as shown in Fig. 8.4.5. The achieved output power of 0.7W is 2.6 times the output power of state-of-the-art mm-Wave PAs (> 30GHz). A comparison of PA metrics from recently reported high-power mm-Wave PAs in silicon is summarized in Fig. 8.4.6. This work shows a PAE and gain comparable to the referenced works as well as one of the highest bandwidths for a non-distributed topology. Figure 8.4.7 shows the micrograph of the PA die, which occupies an area of 3×1.85 mm^2.

Acknowledgments:
This work was supported by the Defense Advanced Research Projects Agency (DARPA) ELASTx program and the US ARL Army Research Office under award number W911NF-10-1-0088. We thank L. Chomas, C. Li, and Z. George for valuable discussions and help with testing.

References:
[1] A. Balteanu, et al., "A 45GHz, 2b Power DAC with 24.3dBm Output Power, >14Vpp Differential Swing, and 22% Peak PAE in 45nm SOI CMOS," *IEEE Radio Frequency Integrated Circuits Symp.,* pp. 319 –322, June 2012.
[2] N. Kalantari and J. Buckwalter, "A Nested-Reactance Feedback Power Amplifier for Q-Band Applications," *IEEE Trans. Microwave Theory and Techniques,* vol. 60, no. 6, pp. 1667 –1675, June 2012.
[3] C. Law and A.-V. Pham, "A High-Gain 60GHz Power Amplifier with 20dBm Output Power in 90nm CMOS," *ISSCC Dig. Tech. Papers,* pp. 426 –427, Feb. 2010.
[4] Y. Zhao and J. R. Long, "A Wideband, Dual-Path, Millimeter-Wave Power Amplifier with 20dBm Output Power and PAE Above 15% in 130nm SiGe-BiCMOS," *IEEE J. Solid-State Circuits,* vol. 47, no. 9, pp. 1981 –1997, Sept. 2012.
[5] U. R. Pfeiffer and D. Goren, "A 23dBm 60GHz Distributed Active Transformer in a Silicon Process Technology," *IEEE Trans. Microwave Theory and Techniques,* vol. 55, no. 5, pp. 857 –865, May 2007.
[6] E. Afshari, et al., "Electrical Funnel: A Broadband Signal Combining Method," *ISSCC Dig. Tech. Papers,* pp. 751 –760, Feb. 2006.
[7] W. Tai, L. Carley, and D. Ricketts, "A Q-band SiGe Power Amplifier with 17.5 dBm Saturated Output Power and 26% Peak PAE," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting,* pp. 146 –149, Oct. 2011.

 978-1-4673-4516-3/13/$31.00

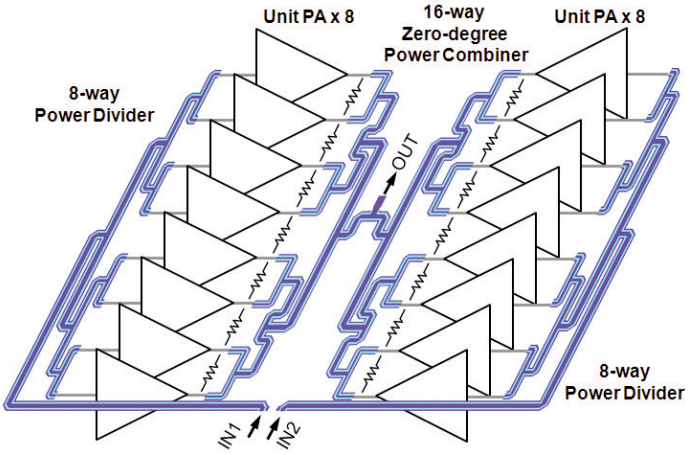

Figure 8.4.1: Block diagram of the 16-way power-combined PA.

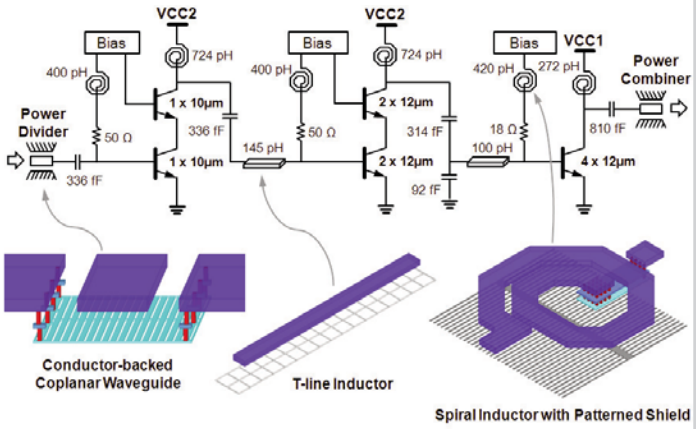

Figure 8.4.2: Schematic of the unit PA cell. 3-D views of on-chip passive devices are also shown.

8

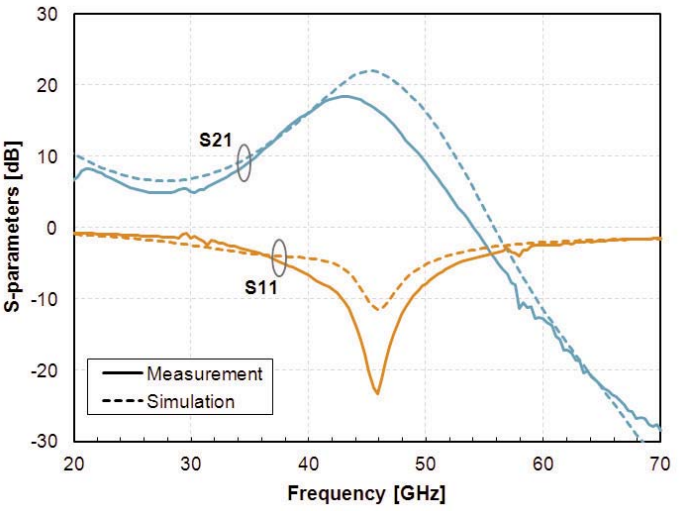

Figure 8.4.3: Simulated and measured S-parameters.

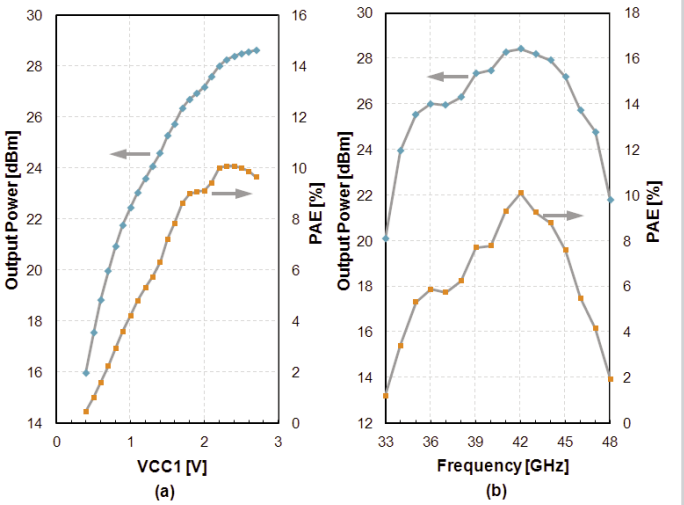

Figure 8.4.4: (a) Saturated output power and PAE versus supply voltage of the output stage (VCC1) at 42GHz. (b) Saturated output power and PAE versus frequency.

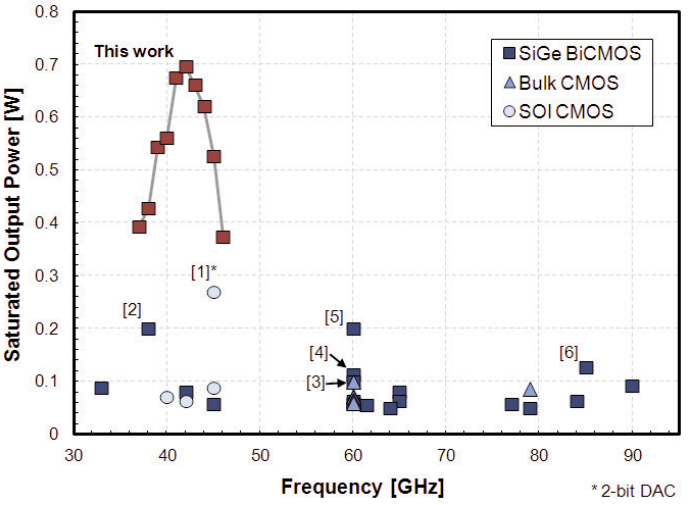

Figure 8.4.5: Saturated output power versus frequency of recent mm-Wave silicon PAs.

Reference	This work	[2]	[1]	[3]	[4]	[5]	[6]
Technology	0.13um BiCMOS	0.13um BiCMOS	45nm SOI CMOS	90nm CMOS	0.13um BiCMOS	0.13um BiCMOS	0.13um BiCMOS
Topology	16-way zero-degree combiner	Nested-reactance feedback	4-stacked 2-bit DAC	4-way Wilkinson combiner	4-way transformer combiner	4-way DAT combiner	Distributed PA
Freq. (GHz)	42	38	45	60	62	60	85
Supply (V)	4 / 2.4	3	5.1	1.2	1.8	4	2.5
P_{sat} (dBm)	28.4	23	24.3	20	20.1	23	21
PAE (%)	10	10.7	14.6	14.2	18	6.3	4
Gain (dB)	18.5	18.4	18	20.6	20.6	20	8
-3dB BW (GHz)	9	5	N/A	6.5	10	N/A	24

Figure 8.4.6: Performance comparison of mm-Wave silicon PAs with greater than 20dBm output power.

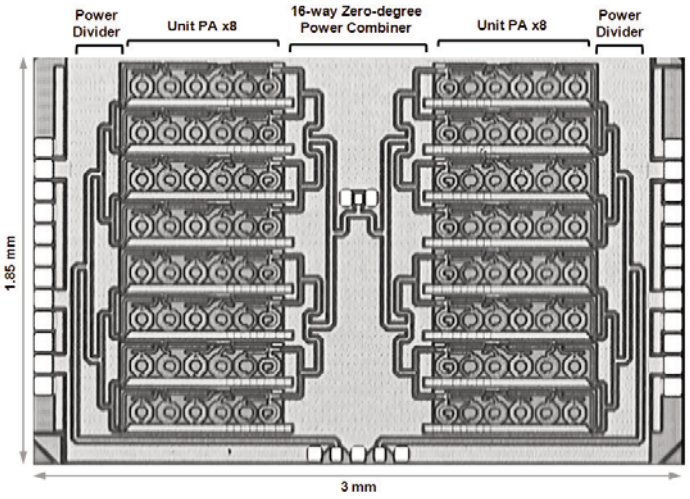

Figure 8.4.7: Die micrograph. The PA occupies 5.55mm^2 of die area.

978-1-4673-4516-3/13/$31.00