25.2 A Complex Image Rejection Circuit with Sign Detection Only

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In recent efforts to implement receivers without RF and IF SAW filters, the old phasing methods such as Hartley and Weaver down-conversion architectures have been renewed with DSP. Zero- or low-IF systems process complex signals with in-phase and quadrature (I/Q) components, and the gain and phase mismatches between them result from analog parameter variations in the I/Q local oscillators, mixers, AGCs, filters, and even ADCs. To improve the I/Q matching, analog solutions such as double quadrature mixing, complex ΔΣ modulator, complex/polyphase filter, and quadrature oscillator have been suggested, but they are only applicable to specific elements in the system, and the overall system-level image still exists. Many image-rejection techniques have been proposed to get higher image rejection than is achievable with these I/Q matching methods. Some methods require a test tone or a phase shifter [1-4]. Digital image rejection relies on signal processing, and requires ADCs with higher resolution than the system would otherwise need [5, 6]. The proposed gain and phase mismatch correction algorithm is based on an adaptive feedback concept using sign bit only, and requires no complicated digital processing with high ADC resolution. It rejects the total accumulated image of an I/Q system no matter what produces the image. The gain and phase errors for feedback are generated with four sign detectors using the orthogonal nature of the I/Q signals. Image correction and error detection can be implemented either in the analog or digital domain. Three combinations are feasible: *digital-digital*, *analog-digital*, and *analog-analog*. Using a complex-baseband sample-and-hold (S/H) circuit with digital sign detectors, which is a hybrid analog-digital system (analog image correction with digital error detection), reduces digital complexity. In the proposed system, the image is rejected at the system level, and any elaborate complex I/Q analog circuits are no longer necessary.

A non-ideal complex-I/Q channel with a path gain mismatch of α and a phase mismatch of θ is shown in Fig. 25.2.1. The parameters, α and θ are frequency independent. The image is defined as a negative frequency component of the signal that is folded into the signal band. That is, the signal and image coupling gains are modified by α and θ, but they can be corrected as shown in the shaded area of Fig. 25.2.1. Both α and θ are assumed to be small so that the 3rd or higher harmonics of α and θ can be neglected. Using the orthogonal nature of the I/Q signals, the gain and phase errors, α and θ, can be obtained from I^2–Q^2 and IQ, respectively. In this work, however, rather than calculating these values, their signs are detected so that both errors can be adaptively trimmed out using sign-only feedback. The error sensing algorithm and the sign detection scheme are shown in Fig. 25.2.2.

A simplified complex-baseband switched-capacitor S/H circuit is shown in Fig. 25.2.3. This circuit performs two functions: S/H for ADC, and image rejection. It samples I/Q inputs differentially on the capacitor bottom plates, and the capacitor values are trimmed using capacitor T-networks. A hybrid analog-digital image rejection system using this S/H is sketched in Fig. 25.2.4. To update the trim capacitors, the four signs of I, Q, I+Q, and I–Q should be known. For an image rejection of >70dB, the signs should be detected after accumulating 2^{20} samples, and then the 9b trim capacitors are updated. The S/H has a 1pF input capacitor, and each trim capacitor is an array of 100fF capacitors, which covers a ±6% range of α with a 0.024% step and a ±3.5° range of θ with a 0.014° step. Since α and θ are initialized to zero, a total of $2^{20}\times2^{8}$ cycles are needed in the worst case to complete the initial adaptation. The advantage of this hybrid analog-digital case is that it does not require high ADC resolution since only sign detection is needed. On the contrary, in the digital-digital case, the ADC resolution will limit the achievable image rejection. The performance of the proposed method depends on where these signs are detected. If the sign detectors are digital and detect the I/Q ADC outputs, the performance is only limited by the analog trimming step and its accuracy because the digital sign detection is highly accurate since it uses a high oversampling ratio. Since the I/Q ADCs are in the loop, mismatch between them is also corrected. However, in the analog-analog case using analog comparators, the ADC mismatch is not corrected, and the performance will be limited by the offset of the sign detectors. An offset as large as 1.5mV for a $1V_{pp}$ signal is acceptable for an image rejection of 70dB.

A prototype chip fabricated in 0.18μm CMOS occupies an area of $0.8\times0.45mm^2$, and consumes 23mW at 1.8V. A gain-boosted opamp is designed for 40MS/s operation with a 20pF load. The chip samples at 40MS/s and accommodates up to a 10MHz symbol rate. For testing, the symbol rate is reduced to allow the use of external ADCs. 256-QAM I/Q signals of $1V_{pp}$ are generated at 1MHz IF with an 800kHz symbol rate, 5% gain mismatch, and 3° phase mismatch. The signals sampled at 40MS/s are converted into digital at 5MS/s using two 15b ΔΣ ADCs. Complex FFTs of four different measured spectra are shown in Fig. 25.2.5. The image rejection is improved by 26dB, to about 65dB, for both the digital-digital and analog-digital cases. An analog sign detector (analog-analog) case exhibits about 62dB of image rejection, which is slightly worse than the other two digital sign detector cases. Due to the 1pF input capacitors, kT/C noise limits the SNR to 72dB. Measured 256-QAM constellations before and after image rejection are shown in Fig. 25.2.6. The constellation dislocation from the ideal location caused by the image seriously affects the receiver I/Q eyes. To facilitate testing the analog sign detector, four analog comparators with offset-cancelled preamplifiers are integrated on the test chip and use an extra area of $800\times150\mu m^2$ and power of 14mW. The chip micrograph is shown in Fig. 25.2.7.

Acknowledgements:
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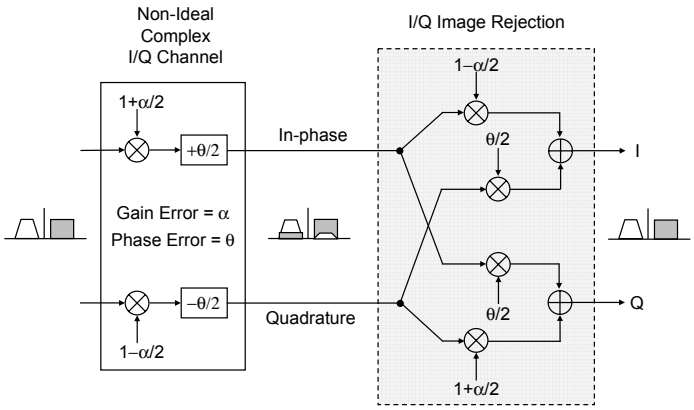


Figure 25.2.1: I/Q gain and phase error correction (image rejection) principle.

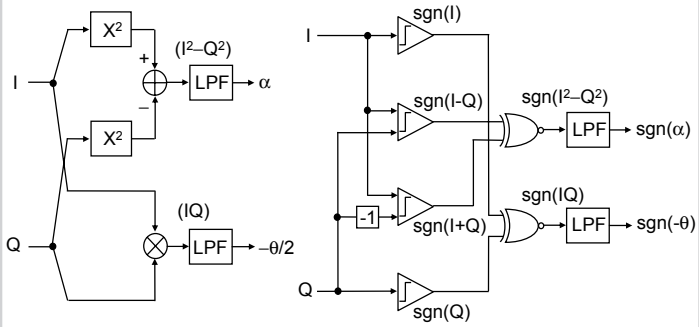


Figure 25.2.2: Generation of gain and phase errors, and proposed sign detection scheme.

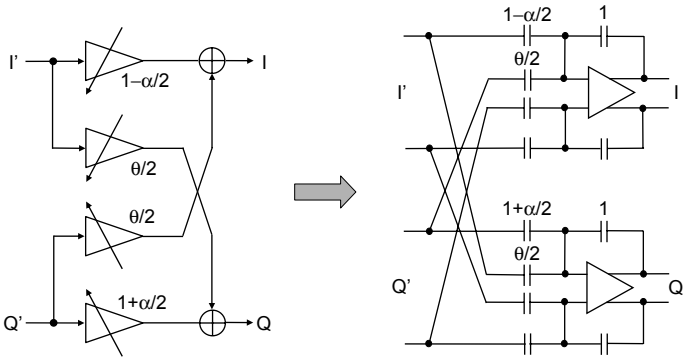


Figure 25.2.3: Switched-capacitor image-rejected complex S/H without switches shown.

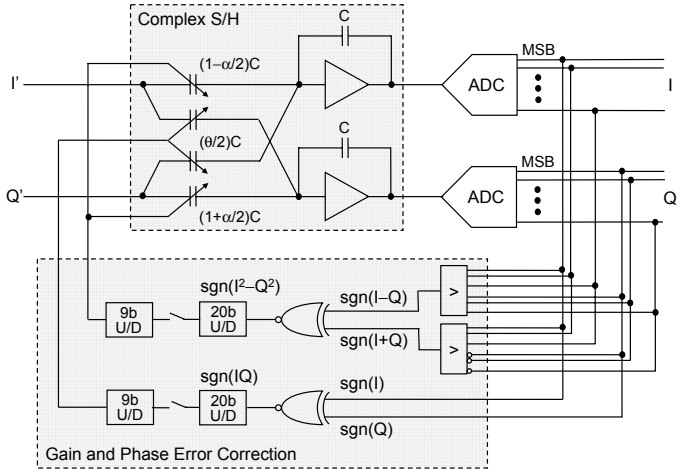


Figure 25.2.4: Complex S/H concept image-rejected with digital sign detectors.

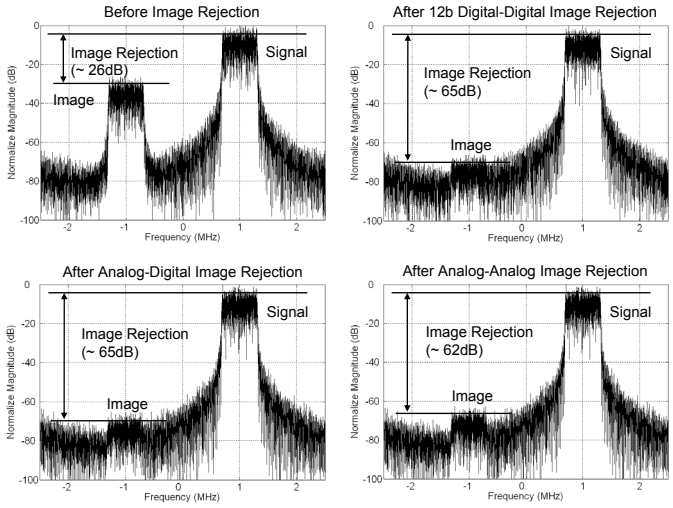


Figure 25.2.5: Measured 256-QAM spectra before and after image rejection.

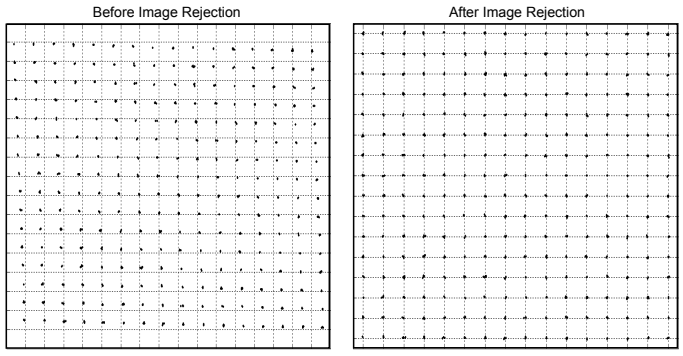


Figure 25.2.6: Measured 256-QAM constellation before and after image rejection.

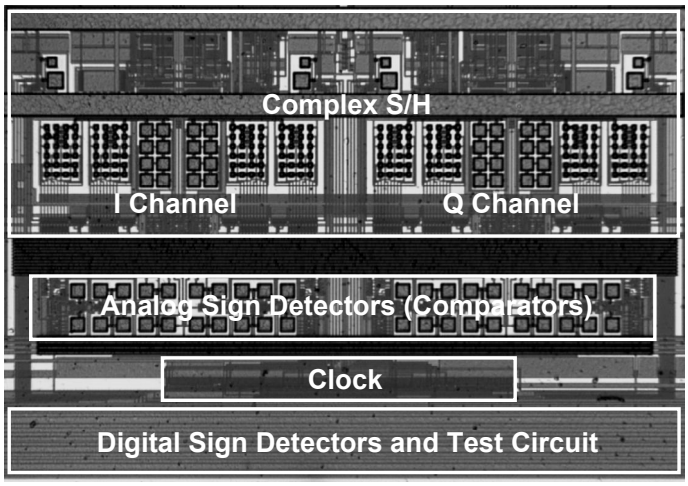
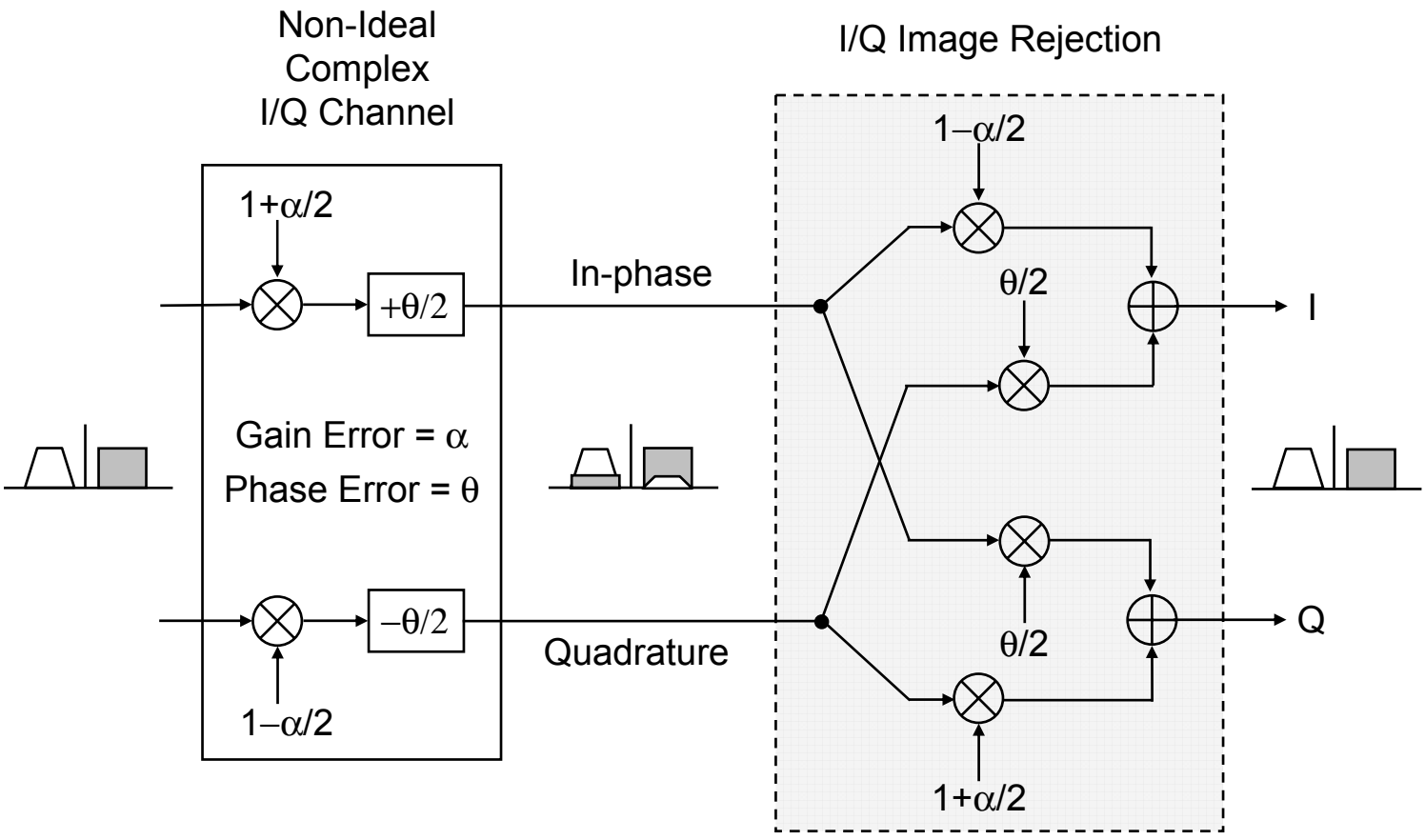


Figure 25.2.7: Chip micrograph.



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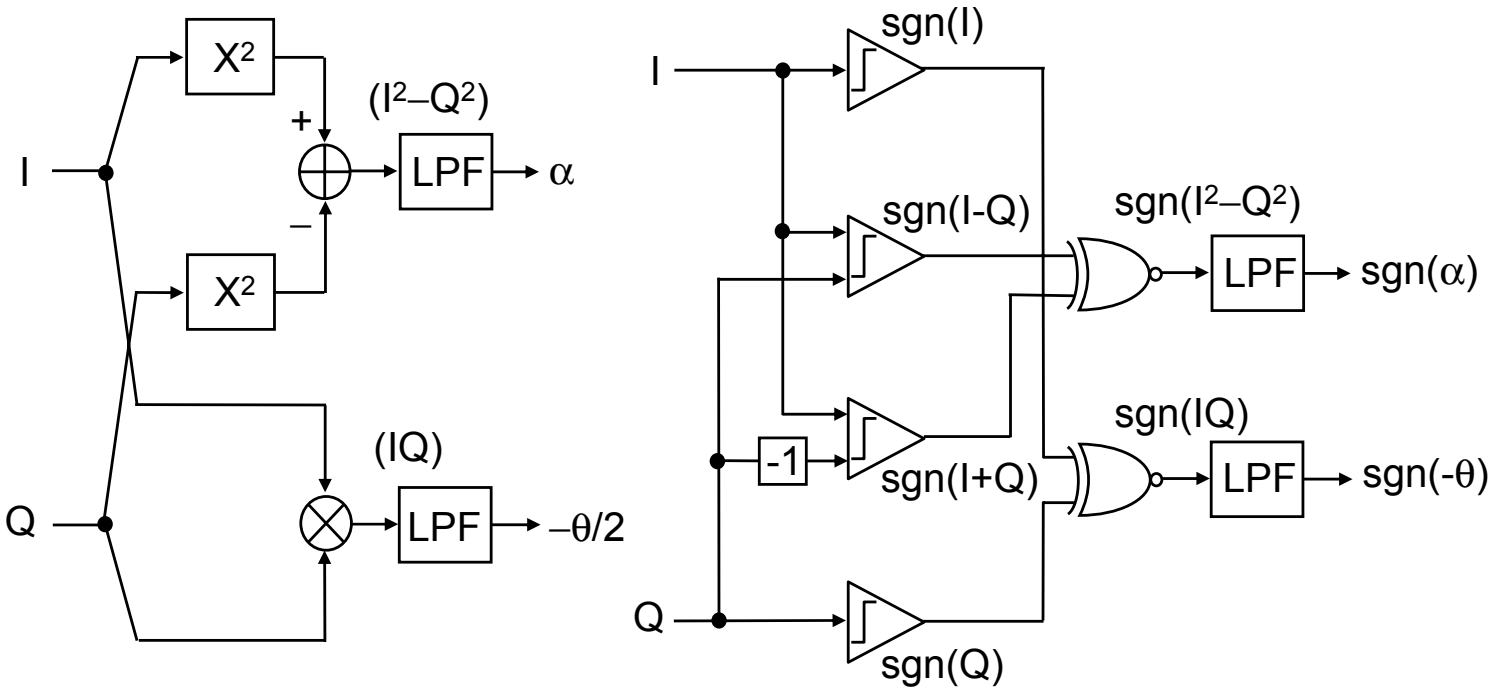

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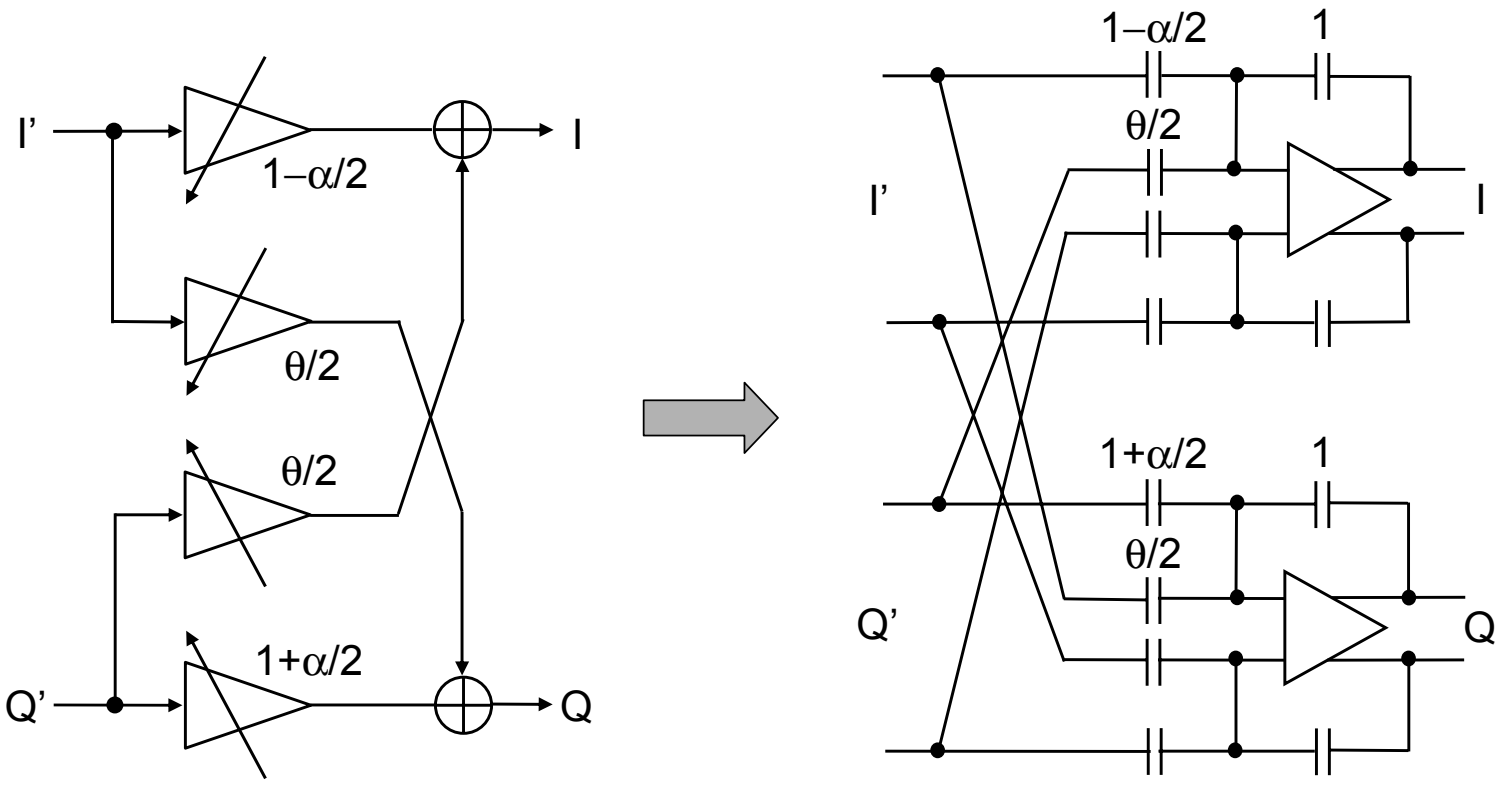

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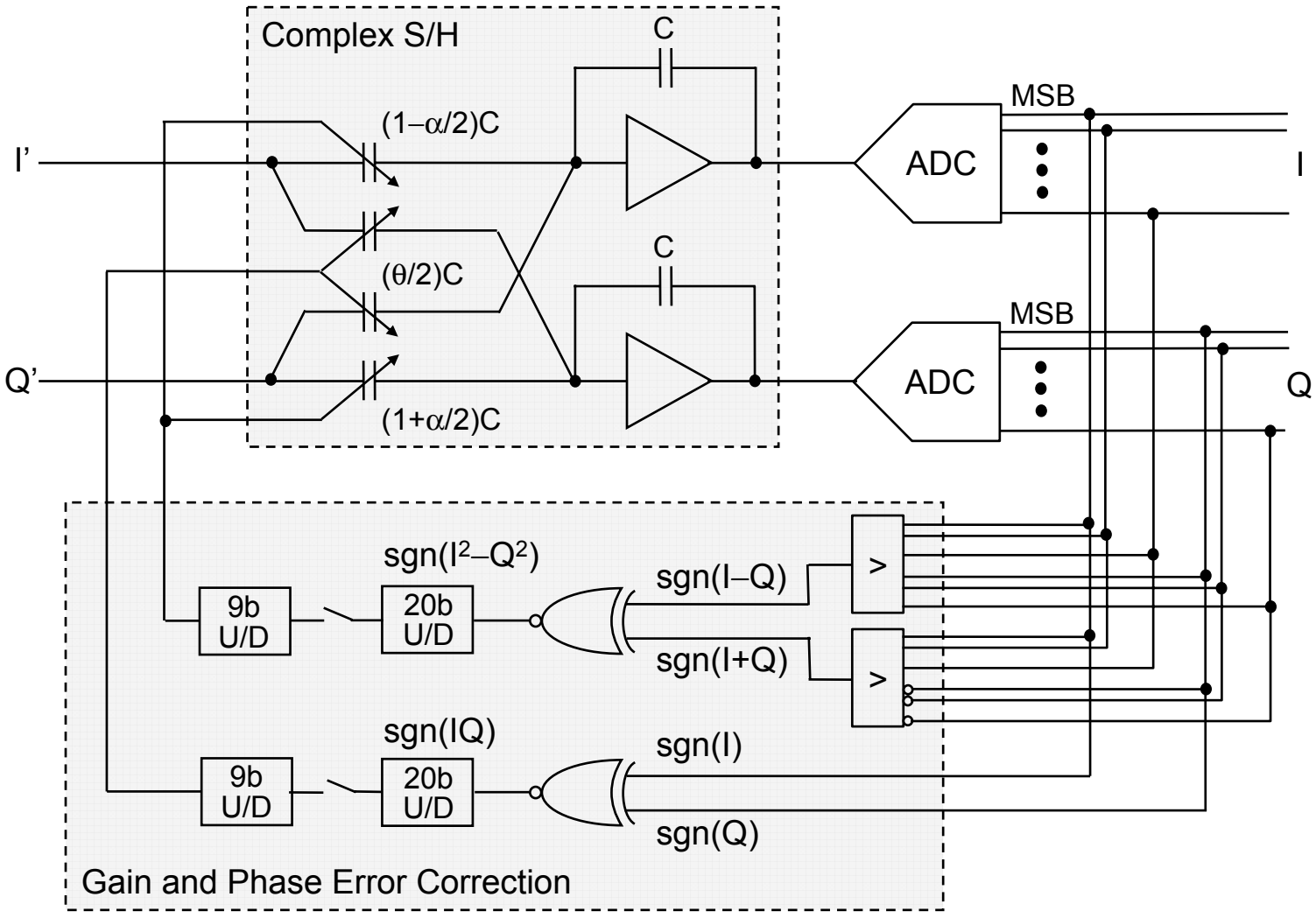

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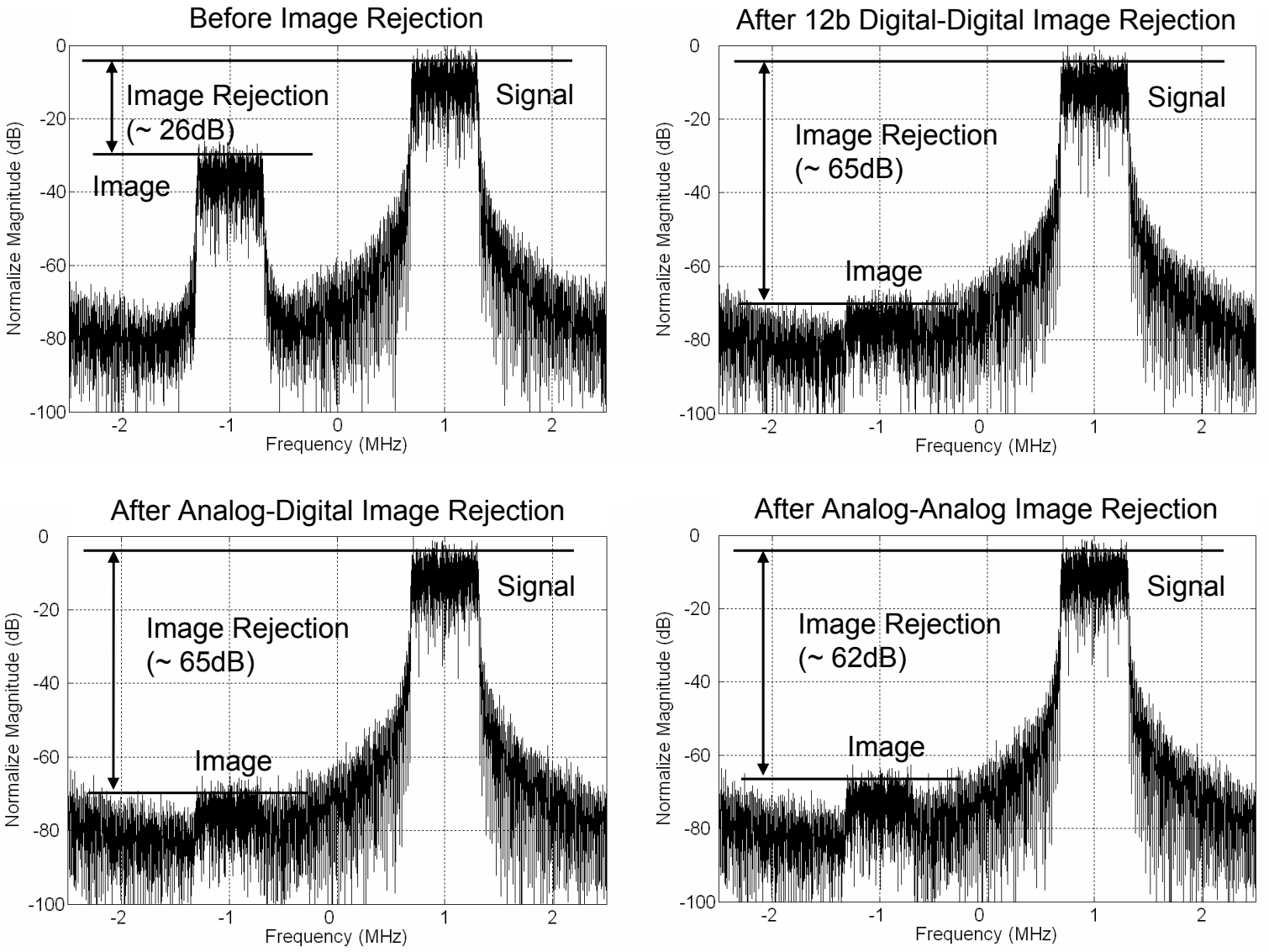

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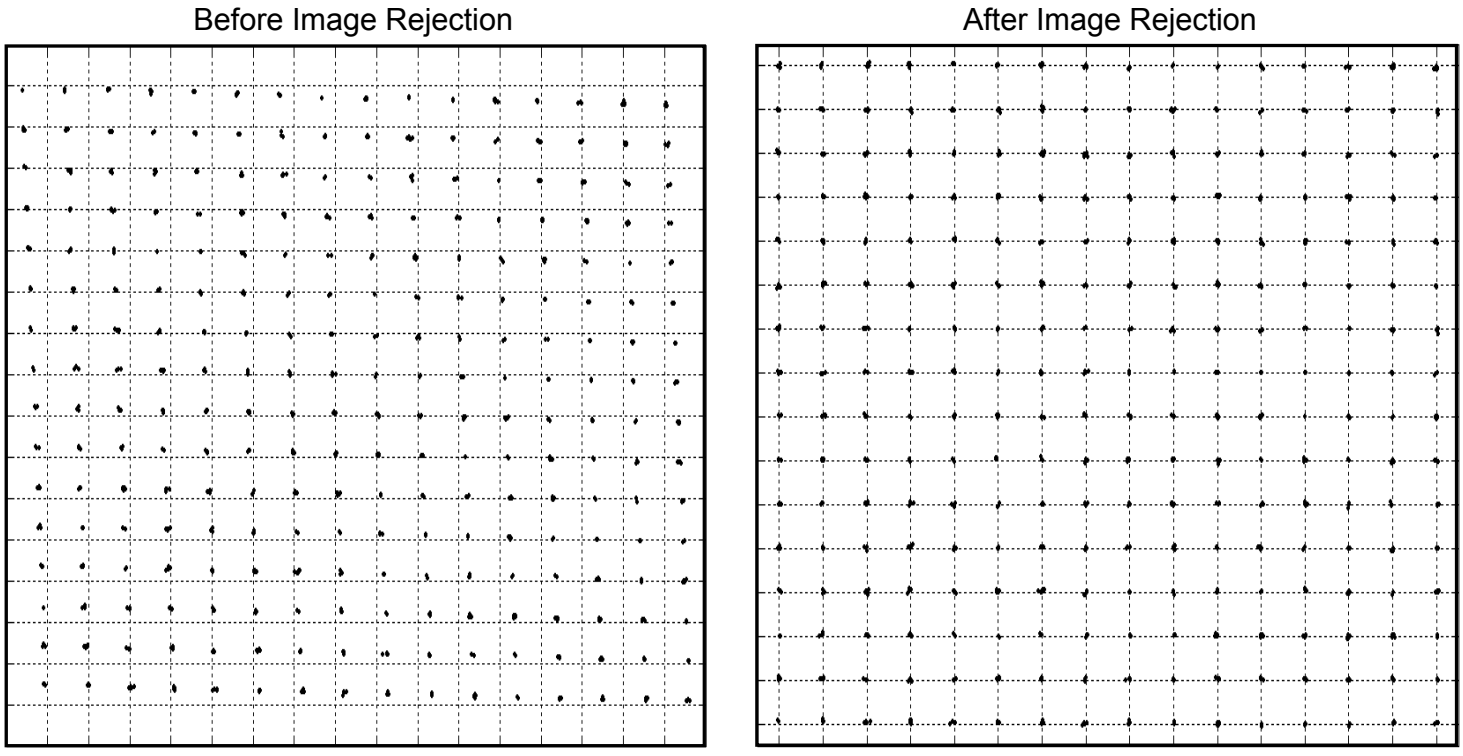

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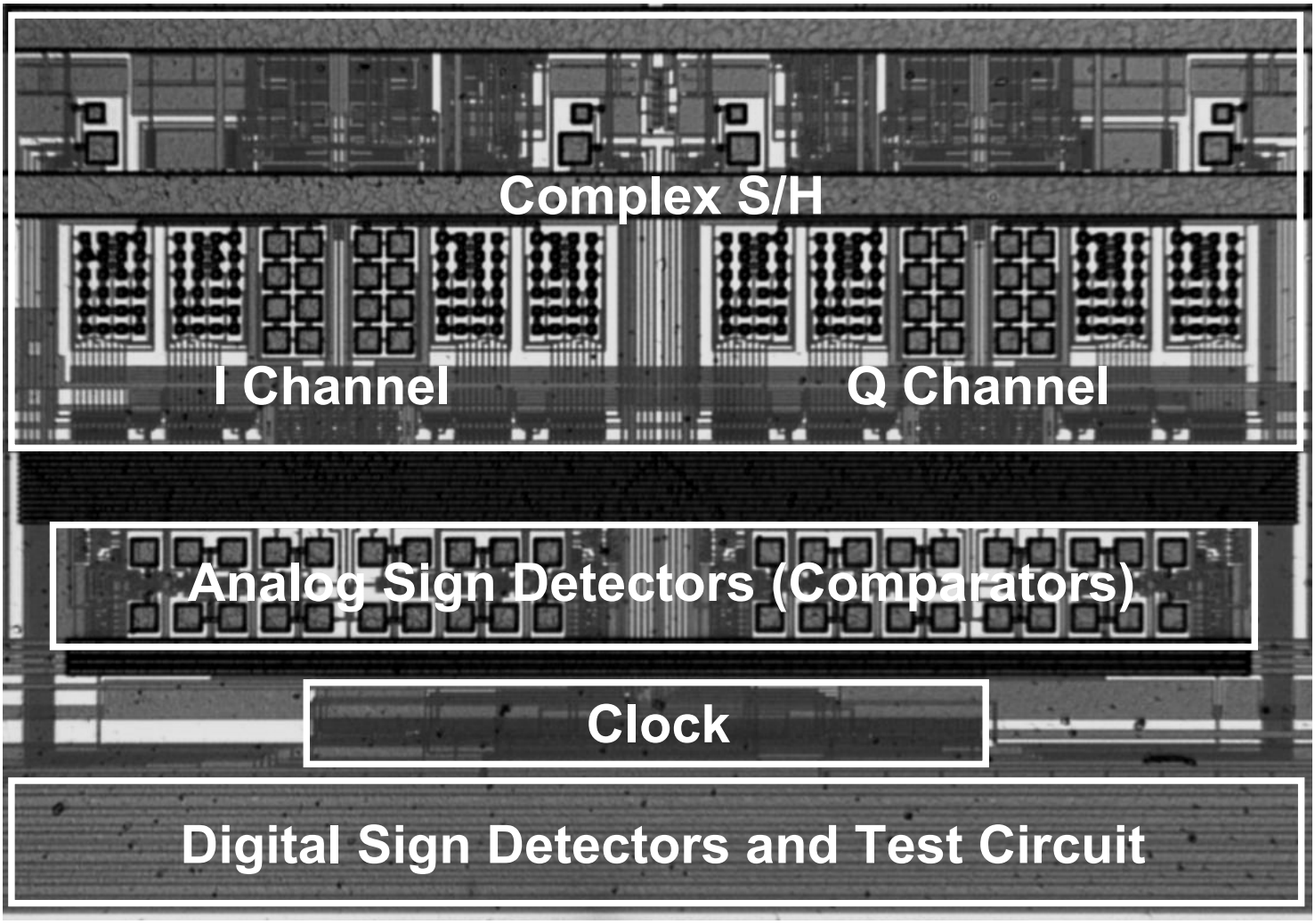

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