Wavelength Locking of a Si Ring Modulator using an Integrated Drop-Port OMA Monitoring Circuit

Saurabh Agarwal[*†], Mark Ingels[†], Michal Rakowski[†], Marianna Pantouvaki[†], Michiel Steyaert[*], Philippe Absil[†], Joris Van Campenhout[†]

[*]KU Leuven, ESAT-MICAS, Kasteelpark, Arenberg 10, B-3001, Leuven, Belgium
[†]IMEC, Kapeldreef 75, B-3001, Leuven, Belgium

***Abstract*—We demonstrate wavelength locking of a hybrid CMOS-silicon photonics ring-based transmitter through direct monitoring of the optical modulation amplitude (OMA) at the drop port of the ring modulator. The OMA is read from a Ge photodetector by a low-power 40nm CMOS circuit, which subsequently drives a feed-back loop that controls the modulator temperature using an integrated heater. OMA stabilization is demonstrated under abrupt laser wavelength variations of up to 150pm, under dynamic modulation at 2Gb/s.**

***Keywords*—Wavelength locking, CMOS, silicon photonics, Si ring modulator, flip-chip, transmitter, OMA, drop port.**

I. Introduction

Silicon micro-ring modulators (MRM) have the potential to enable wavelength-division multiplexing (WDM) high-bandwidth, low-footprint, energy-efficient optical interconnects in high performance systems such as data centers [1]. However, due to resonant behavior of the these ring modulators, any misalignment between the optimum wavelength and the incoming laser wavelength significantly reduces their modulation capability. Typically, a mismatch of as little as 100pm will render the device inoperable as a modulator. This misalignment may result from thermal (100pm/K), process and laser wavelength variations. As such, an active control strategy locking the optimum wavelength of the MRM to the laser wavelength is of key importance for the success of this technology.

In this paper we demonstrate a novel concept for automatic wavelength locking of a ring modulator at its maximum optical modulation amplitude (OMA), using a read-out circuit implemented at the drop port (DP) of the ring. The demonstration involves a flip-chip integrated transmitter comprising a 40nm CMOS chip with the OMA monitoring circuit and the modulator driver, flip-chipped onto a Si photonics (SiPh) chip with the Si ring modulator, integrated tungsten (W) heater and a Ge monitor photodiode (PD). The reported drop-port based approach has the advantage of not interfering with the through-port (TP) transmission, which ensures compatibility with WDM transmitter architectures [2,3]. But at the same time, it is more challenging since the OMA at the drop port is typically designed to be smaller than at the through port, as not to induce excessive optical loss in the modulator. Here, we demonstrate a sensitive and low-power CMOS circuit that reliably monitors OMA and drives a feedback loop effectively stabilizing the modulation quality of the ring modulator under laser wavelength fluctuations, as will be encountered in typical operation conditions.

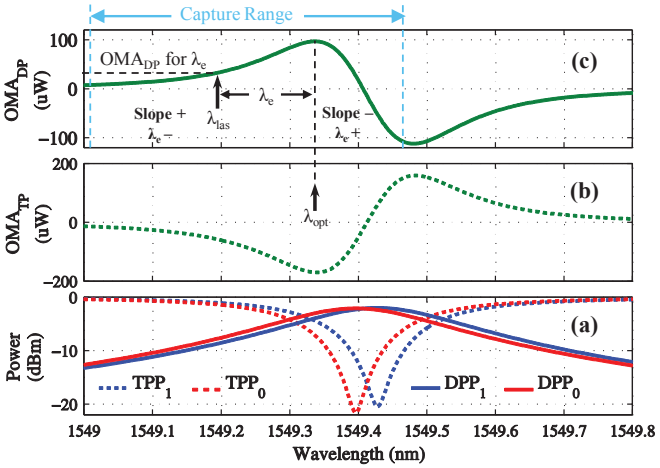

Fig. 1. Transmission characteristics of a MRM and concept of wavelength locking at maximum drop-port OMA.

Sign (λe)	Sign (Slope)	V_{SQ}	Effect on V_H
+	-	'1'	increase
-	+	'0'	decrease

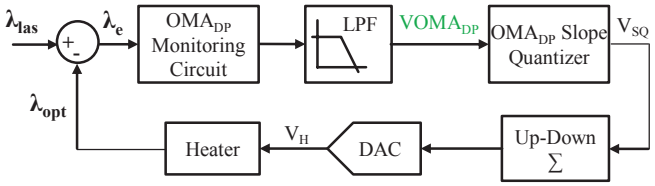

Fig. 2. Implemented block diagram for wavelength locking.

II. Wavelength Locking of a Ring Modulator

Simulated plots of the typical transmission characteristics of a MRM at a fixed temperature with 0dBm optical input power are shown in Fig. 1, illustrating our strategy for wavelength locking. The power levels of the transmitted signal at through-port for the two modulating voltages of $V_1 = -1V$ and $V_0 = 0.5V$, referred to as TPP_1 and TPP_0 respectively, are plotted in Fig. 1a. The corresponding power levels coupled from the ring into the drop waveguide are referred to as DPP_1 and DPP_0 respectively, and are also included in Fig. 1a. Moreover, the optical modulation amplitude OMA_{TP} at the through port, defined as $TPP_1 - TPP_0$, is shown in Fig. 1b. In addition, OMA_{DP} defined as $DPP_1 - DPP_0$, is plotted in Fig. 1c. OMA_{TP} is considered the figure of merit of a MRM modulator as its maximum value corresponds to the best combination of insertion loss and

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extinction ratio [4]. Furthermore, it is observed that the peak of OMA_{TP} coincides with the peak of OMA_{DP}. This allows maximization of the OMA_{TP} by stabilizing the system at the peak of OMA_{DP}. This can be achieved by locking the system with $\lambda_{opt} = \lambda_{las}$, where λ_{opt} denotes the optimum wavelength for the MRM corresponding to the maximum OMA_{DP}, and λ_{las} refers to the incoming laser wavelength. Hence, in the locked state, the wavelength error λ_e defined as $\lambda_{las} - \lambda_{opt}$, is minimized.

Fig. 2 shows the system diagram of the implemented wavelength-locking feedback loop. The monitoring circuit measures $VOMA_{DP}$ (electrical OMA_{DP}) corresponding to λ_e. $VOMA_{DP}$ is low-pass filtered to suppress high frequency noise and is used by the slope quantizer to produce the sign of the OMA_{DP} slope. As the sign of the slope and the sign of λ_e maps one to one, the output of the slope-quantizer (V_{SQ}) is simply equal to the 1-bit quantized λ_e. Hence, this is indeed a delta-modulator based negative feedback system wherein the average value of λ_e is minimized by the high loop gain at low-frequency provided by the counter [5]. The heater can be represented by a gain block, which red shifts λ_{opt} by scaling the DAC voltage with the gain $H_G = d\lambda_{opt}/dV_H = 2 \cdot V_H \cdot \eta_H / R_H$, where V_H, η_H and R_H denotes heater voltage, heater efficiency and electrical heater resistance respectively. This is a non-linear function which can be linearized to a certain extent by varying the counting steps.

III. Demonstrator Description

Fig. 3a shows a schematic of the flip-chip integrated transmitter demonstrator, while Fig. 4 shows various microscopic images. The CMOS chip, implemented in 40nm 1.1V Low-Power (LP) Foundry CMOS, contains the OMA_{DP} monitoring circuit along with a 1.5-V_{pp} differential 10Gb/s ring modulator driver [3]. The SiPh chip contains a ring modulator with integrated W heater and Ge PD connected to the drop waveguide. The slope quantizer along with the up-down counter is implemented in Matlab while the low-pass filter and DAC are placed off-chip. Instrumentation amplifier (IA) is also used at the output of the monitoring circuit for more reliable measurements. PRBS data and clock signals are fed into the CMOS chip through Cu traces on the SiPh chip from an external programmable pattern generator (PPG), using a 50Ω terminated GSGSG probe. The through-port optical transmission is analyzed in the time domain by an optical oscilloscope, after activating the driver and coupling the laser light of fixed wavelength into the ring. On powering-up the wavelength locking loop, the heater voltage is automatically adjusted to make λ_{opt} equal to λ_{las}, and thus maximizing the OMA of the modulated laser beam in the through port.

A. OMA_{DP} Monitoring Circuit

As illustrated in Fig. 3a, the optical signal at the drop waveguide is detected by the Ge PD and is further amplified and converted into a voltage by a TIA located on the CMOS chip. The monitoring circuit [6] samples the voltage corresponding to DPP_1 and DPP_0 on two capacitors C_1 and C_0 respectively such that $VDPP_1$ ($VDPP_0$) = DPP_1 (DPP_0)·R_p·R_{TIA} where, R_p refers to the responsivity of the PD and R_{TIA} denotes the gain of the trans-impedance amplifier (TIA). Conventional bit-by-bit sampling would have required high speed TIA with relatively high dynamic power. It should also be noted that in order to able to detect a small changes in OMA_{DP}, the requirement for settling accuracy is more stringent for this TIA than the ones typically used at the receiver of an optical link. Therefore, a bit counter is included which turns on T1 (or T0) only when the run-length of transmitted bit 1's (or 0's) is greater than 4 (Fig. 3b), thereby reducing the bandwidth requirement of the TIA by approximately a factor 4. This is indeed possible since the circuit is working at the transmitter side where the bit values are known. This allows us to use a resistor as a passive TIA with ~5GHz bandwidth for R_{TIA} = 150Ω and an estimated associated parasitic capacitance (C_P) of ~ 200fF. Owing to the relatively small R_{TIA}, large sampling capacitors (C_1 and C_0) of 10pF are needed to reduce kT/C noise and thus improve signal to noise ratio (SNR). They also mitigate the non-linearity due to charge injection. As a result of the large capacitors, $VDPP_1$ ($VDPP_0$) is integrated each time T1 (T0) turns on, till it settles at its final value. These down-converted signals, devoid of any flicker noise from T1 or T0, are further processed off-chip by an instrumentation amplifier (IA) of gain ~54dB, followed by a low-pass filter to further boost SNR and to carry out reliable measurements. The output of the low-pass filter for $VOMA_{DP}$, is indeed the OMA_{DP} in electrical domain.

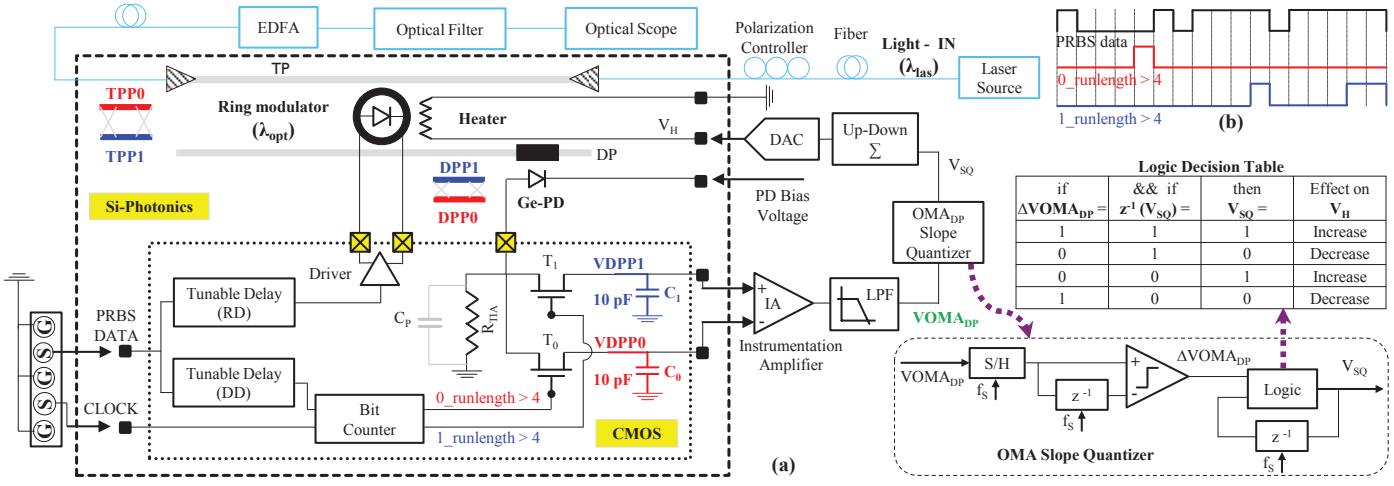

Fig. 3. (a) Implementation of wavelength locking in hybrid CMOS-SiPh transmitter. (b) Output of the bit-counter.

The overall time constant for the outputs of the monitoring circuit can be expressed as $R_S \cdot C0(C1) \cdot P_R$ where, R_S is the nominal on-state resistance of T0 (T1) and P_R is the probability of T0 (T1) being turned on. This is calculated to be 455ns for a PRBS-31 signal. It ensures that the dominant pole of the feedback loop is still formed by the heater-ring temperature time constant (~20µs).

To compensate for the difference in delay between the output of bit-counter and TIA, blocks of tunable delays are also required. 'Ring-delay' (RD) and 'data-delay' (DD) individually control the timing of the output of TIA and bit counter respectively. Each of them can delay its respective input signal by up to ~ 900ps in small steps of ~2ps. This allows fine alignment between the outputs of bit counter and TIA so that T1 and T0 are turned on exactly when the output of the TIA has fully settled. A large tuning range is incorporated just for measurement flexibility.

B. Slope Quantizer

The slope quantizer samples $VOMA_{DP}$ at the sampling frequency F_S. Subsequently, it generates a digital output (V_{SQ}) at every sampling instance to either increase or decrease the heater voltage (V_H), on the basis of internally computed sign of the OMA_{DP} slope. The sign of the OMA_{DP} slope is actually computed by the logic block, using the sign of the change in $VOMA_{DP}$ ($\Delta VOMA_{DP}$) and the previous output of the slope quantizer ($z^{-1}(V_{SQ})$). As such, the slope quantizer is robust to offset and has a very simple implementation consisting of only one comparator and some digital logic.

With heater-ring temperature time constant being ~ 20µs, F_S can go up to ~ 10kHz. However, in this demonstration, where slope quantizer and up-down counter are implemented in matlab, F_S is limited to be ~ 1Hz. $\Delta\lambda_{res}$ and ΔV_H are defined as the magnitude of change in λ_{res} and V_H respectively at each sampling instance. These two quantities are related as $\Delta\lambda_{res} = H_G \cdot \Delta V_H$.

C. System Level Parameters

The important system level parameters for wavelength locking feedback loop are: (1) The *maximum slope of the aggressor* that can be compensated by the feedback loop is expressed as $\Delta\lambda_{res} \cdot F_S$. (2) The *accuracy of stabilization* is largely defined by the quantization noise which increases with $\Delta\lambda_{res}$. However, for small $\Delta\lambda_{res}$ and small magnitude of OMA_{DP} slope, circuit noise needs to be taken into account. This is because of the increase in the probability of wrong decisions owing to the smaller change in OMA_{DP} to be detected by the comparator. (3) The heater provides *thermal tunability* of η_H ~ 150pm/mW. (4) The *capture range* is defined as the range of λ_e for which the feedback loop is able to automatically lock at the maximum OMA, without any start-up procedures, as shown in Fig. 1. If λ_e is too small, the OMA_{DP} curve becomes too flat for the slope quantizer to produce the correct output reliably. On the other hand, if it's too high then the sign of the slope and the sign of λ_e no longer maps one to one. Along with the MRM characteristics, the capture range is also dependent on $\Delta\lambda_{res}$.

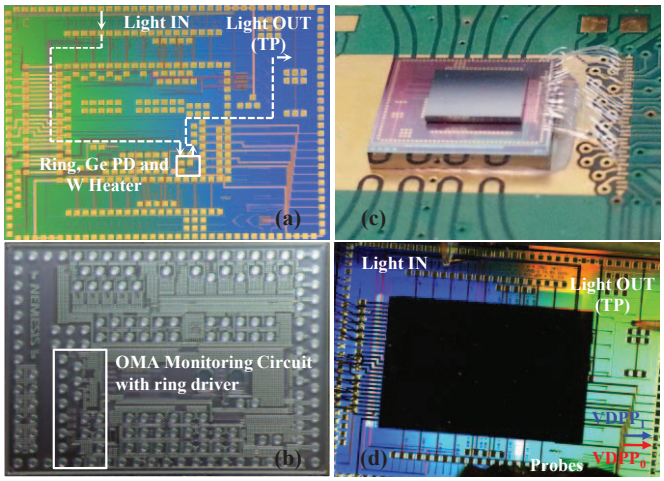

Fig. 4. (a) Silicon photonics chip (SOI, 130nm CMOS toolset) (b) 40nm LP CMOS chip (c) Side view of the CMOS-SiPh flip-chip transmitter assembly (d) Wavelength locking measurement setup.

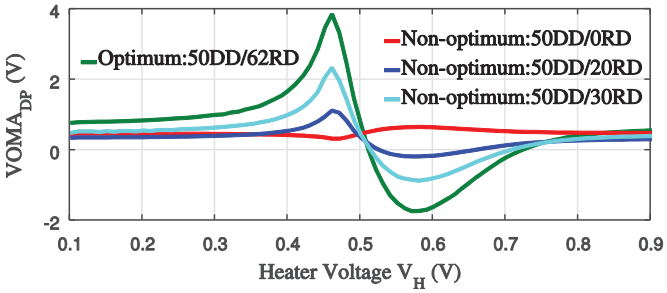

Fig. 5. Effect of delay position on measured electrical $VOMA_{DP}$ for varying heater voltages.

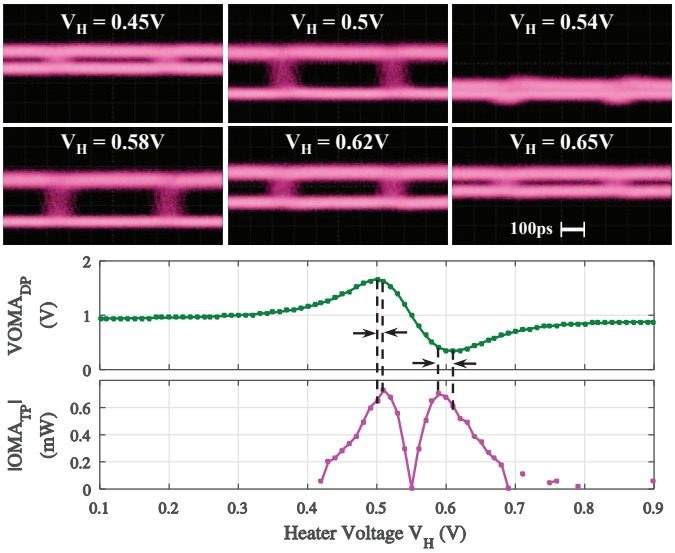

Fig. 6. Correlation of optical OMA_{TP} , as measured from the 2Gb/s eye diagrams on the optical oscilloscope, and measured electrical $VOMA_{DP}$.

IV. Measurment Results

For the first demonstrator experiment, the feedback loop is opened up by removing DAC, slope quantizer and up-down counter. Fig. 5 shows the measured $VOMA_{DP}$ for the optimum and non-optimum delay positions, with V_H being swept by an external source. The input optical power at the fiber grating coupler is 7dBm at 1554.95nm of laser wavelength, and is

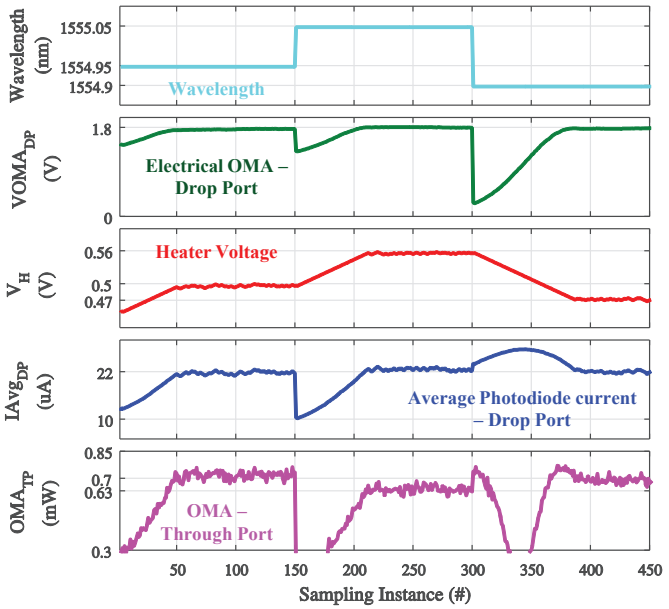

Fig. 7. Measurement results of wavelength locking (ΔV_H = 1mV).

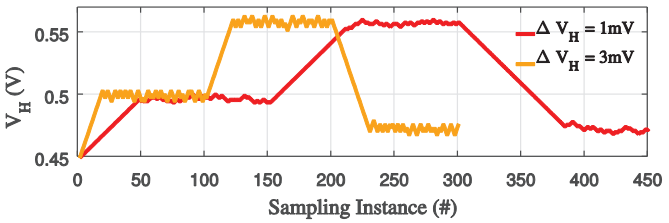

Fig. 8. Effect of ΔV_H on the speed and accuracy of wavelength locking.

modulated with PRBS data at 2Gbps. The maximum possible value of OMA_{DP} could only be extracted at the optimum delay position when the output of bit-counter and TIA are aligned properly.

In the second experiment, the $VOMA_{DP}$ is measured at the optimum delay position and correlated with the optical OMA_{TP} retrieved from the oscilloscope at the through port, while V_H is swept by an external source. This is shown in Fig. 6, along with captured eye diagrams for the through-port transmission for different V_H. A slight mismatch is observed between the peak of OMA_{TP} and the peak of OMA_{DP}, which likely originates from a non-linear effect in the MRM as the mismatch is found to be dependent on the input laser power. It should also be noted that OMA_{TP} has additional noise originating from the oscilloscope. Moreover, relatively large jitter in the eye diagrams for the through-port transmission, seems to be coming from the tunable delay before the driver circuit. In this experiment, 3dBm of input optical power at 1554.95nm of laser wavelength is set at the grating coupler, and modulated with PRBS data at 2Gbps. The feedback loop is still kept open.

In the third experiment (Fig. 7), the feedback loop is closed with ΔV_H (heater step voltage) equal to 1mV and the tunable delays set at their optimum position. Again, 3dBm of input power is used with 2Gbps of PRBS data. V_H is initially set to 450mV with 1554.95nm of laser wavelength. This results in a non-optimum OMA_{DP} which is detected by the feedback loop, which subsequently adjusts V_H to lock the system at the maximum OMA_{DP}. After some time, the laser wavelength is deliberately increased to 1555.05nm which again brings the system to the state of non-optimum modulation. Consequently, λ_{res} is red shifted by the increasing V_H until λ_e is minimized. Similarly, when the laser wavelength is again reduced to 1554.9nm, V_H is automatically reduced to lock the system to the optimum OMA_{DP}. Owing to the limited bandwidth of the optical filter used in the setup (Fig. 3a) to filter out the noise originating from EDFA used, the stabilized OMA_{TP} for the laser wavelength 1555.05nm is slightly less than that for the 1554.95nm and 1554.9nm. Also, due to the small mismatch between the peak of OMA_{DP} and OMA_{TP}, the feedback loop misses the maximum OMA_{TP} for 1554.9nm laser wavelength and stabilizes at a value little smaller than that. Fig. 8 shows measured V_H for the wavelength locking (as described above) achieved with two different ΔV_H. Increasing ΔV_H speeds up the feedback loop at the expense of increased quantization noise.

V. Discussion and Conclusion

The measured energy consumption of the monitoring circuit at 2Gb/s is 1.45pJ/bit where, tunable delays are the major contributors (1.4pJ/bit) owing to their large tuning range of 900ps. For a fixed data rate and with careful modelling of the path delays, the required range can be shortened to ~50ps, reducing energy consumption to ~200fJ/bit. Also, with the use of passive TIA and data-rate adjustable bit counter, the power efficiency should be improved further at higher transmission rates. Moreover, static power of the remaining circuit blocks will be substantially less than 1mW, since they operate at much lower speed (~10kHz) [7]. Combined with improved heater efficiency (>1nm/mW) [8], the proposed wavelength locking concept has the potential for power efficiencies substantially below 1pJ/bit at 25Gb/s and beyond, enabling low-power and thermally stabilized ring-based WDM SiPh transmitters.

Acknowledgment

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